Investigation of electron trapping behavior in *n*-channel organic thin-film transistors with ultrathin polymer passivation on SiO$_2$ gate insulator

Shinji Tanida[a], Kei Noda[a,*], Hiroshi Kawabata[b], Kazumi Matsushige[a]

[a]Department of Electronic Science and Engineering, Kyoto University,

Katsura, Nishikyo, Kyoto 615-8510, Japan

[b]Young Researchers Education Center, Hiroshima University, Kagamiyama,

Higashihiroshima, Hiroshima 739-8512, Japan

[*]Corresponding author. E-mail address: nodakei@kuee.kyoto-u.ac.jp

(Abstract)

Electron trapping behavior at the interface between *N,N'*-ditridecyl-3,4,9,10- perylene

tetracarboxylic diimide (PTCDI-C13) film and thermal SiO$_2$ was investigated by

utilizing ultrathin poly(methyl methacrylate) (PMMA) gate passivation layers. From the

capacitance-voltage analysis for the PTCDI-C13/PMMA/SiO$_2$ interface, it is found that

the electron tunneling appeared with PMMA thinner than 0.8 nm, and that the thickness

of the gate passivation layer should be at least 1 nm for preventing injection-type

hysteresis in   the capacitance-voltage curve. The effective electron mobility of organic

thin-film transistors (OTFTs) based on PTCDI-C13 with SiO$_2$ gate insulator was

increased by suppressing shallow-level interface traps on SiO_2 with the PMMA layer, which can be partially accounted for by the multiple trap and release model. In this work, the thickness and the density of the PMMA layers were precisely controlled with a simple spin-coating process. Even 1.3-nm thick PMMA layer caused the improvements of the electron mobility and the air stability of the *n*-channel conduction.

1. Introduction

Electron transport in organic thin film transistors (OTFTs) has been intensely examined for developing high-performance n-channel OTFTs [1]. However, in the usual case, the device characteristics of the n-channel OTFTs still becomes inferior to p-channel devices with respect to carrier mobility and air stability. One of the main reasons for that is electron traps at the interface between an organic semiconductor and a gate insulator. Especially it is well known that silanol (SiOH) groups can work as strong electron attracting species when silicon dioxide (SiO$_2$) was employed as gate insulator [2-5]. For suppressing the electron traps deriving from SiOH, the surface passivation of polymer dielectrics on SiO$_2$ is effective, resulting in the enhancement of n-channel conduction in transistors based on various organic semiconductors [3-6]. In these previous works, the thickness of the passivation layers was more than several tens of nanometer. However, these polymer spacers on gate dielectrics should be as thin as possible because the larger thickness causes the decrease of the gate capacitance. For discussing electron trapping behavior related to transistor characteristics in detail, the surface modification of the gate insulator without changing the gate capacitance is desirable.

Thus far, we have reported the improvement of electron field-effect mobility

and air stability of *n*-channel OTFTs by using spin-coated poly(methyl methacrylate) (PMMA) films as gate spacer on SiO$_2$ insulators [7-9]. In this work, the precise control of the thickness and the coverage of PMMA in a nanometer-scale has been achieved, which is in general quite difficult for polymer materials. Then, the relationship between the film properties (the thickness and the coverage) of the PMMA passivation layers and electron accumulation and transport in *n*-channel OTFTs based on *N,N'*-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C13) [10] was examined by measuring capacitance-voltage curves and transistor current-voltage characteristics. In this study, we chiefly discussed the passivation effects on gate SiO$_2$ with PMMA thinner than 3 nm. Our technique of fabricating ultrathin PMMA films enabled us not only to improve *n*-channel transport in OTFTs, but to investigate electron trapping behaviors at the insulator/semiconductor interface in detail.

2. Sample and experimental

The chemical structures of PMMA and PTCDI-C13 were shown in Fig. 1(a) and (b). PMMA (Mw 120,000, Aldrich) was purified with a precipitation method as described elsewhere [9,11]. Heavily-doped *n*-type silicon wafers (< 0.02 Ω cm, size: 1.5 cm $\times$ 1.5 cm) with a thermally grown SiO$_2$ were employed as substrate. The nominal

thickness of the SiO$_2$ layer was 300 nm. After cleaning these wafers by sonication and vapor degreasing with ethanol, ultraviolet (UV) ozone treatment was performed for 15 min. Then, PMMA layers were deposited by spin-coating onto these wafers using PMMA toluene solution at various concentrations. Finally, these PMMA films were baked for 15 min at 393 K. The X-ray reflectivity (XR) for the PMMA films was measured using a Rigaku ATX-G instrument with Cu K$_\alpha$ X-rays generated from a Cu rotating anode at 50 kV and 300 mA. The curve-fitting of measured XR profiles was carried out with Rigaku GXRR commercial software to obtain the thickness, the density, and the surface and interface roughness of each component of a multilayered structure. The data fitting process is based on the theory of Parratt [12]. Top-contact configuration of PTCDI-C13 thin-film transistors, as depicted in Fig. 1(c), was fabricated onto the heavily-doped wafers which worked as gate electrode. PTCDI-C13 (Aldrich) was sublimed twice in advance, and thermally evaporated onto a bare SiO$_2$ (untreated) and SiO$_2$ coated with PMMA simultaneously under a pressure of 1.0×10^{-4} Pa. The thickness of PTCDI-C13 films and the substrate temperature were set to be 30 nm and room temperature (293 K), respectively. Finally, 25-nm thick gold was deposited onto PTCDI-C13 films through a shadow mask to form a pair of source-drain electrodes. The channel length (L) and width (W) were 50 μm and 1 mm, respectively.

The capacitance(C)-gate voltage (V_G) curve of metal-insulator- semiconductor

(MIS) structure between source and gate electrodes was measured by an LCR meter

(HP4263A, Agilent) with a typical scan rate of 0.1 V/s. The modulation frequency and

voltage for the measurements were 100 Hz and 100 mV peak-to-peak, respectively. The

C-V_G measurements were performed in a vacuum (1.0×10^{-2} Pa).

Transistor current-voltage characteristics of OTFTs in a vacuum were

evaluated, followed by the measurements in air, which were commenced after 10 min

exposure of the device to the air. The ambient temperature and humidity were 293 K

and 30 %, respectively. Transfer characteristics (drain-source saturation current ($I_{D,sat}$)

vs. gate voltage (V_G)) were measured with a Keithley 4200-SCS semiconductor

parameter analyzer. The field-effect mobility for electron (μ_e) and threshold voltage

(V_T) were obtained from transfer characteristics in accordance with the following

equation:

$$I_{D,sat} = WC_i\mu_e\left(V_G - V_T\right)^2/(2L),\qquad\qquad(1)$$

where C_i is the gate capacitance. Here, the same value of dielectric constant ($\varepsilon = 3.9$)

was used for both SiO_2 and PMMA as reported elsewhere [13].

3. Results and discussion

3.1 Characterization of the ultrathin PMMA layers

Figure 2 shows XR profiles for the ultrathin PMMA films with different thicknesses prepared onto SiO_2. The thickness of the PMMA layer was calculated by fitting the experimental data and given in the same figure. The average thickness of the SiO_2 layers was also calculated to be 307.3 nm. Broader interference fringes appeared with smaller thickness of the PMMA, while only monotonic decay of reflectivity was observed for the bare SiO_2/Si substrate. This result indicates that very thin PMMA films were formed uniformly on top of the SiO_2 surfaces.

The thickness, the density, and the roughness of the PMMA layers prepared for the OTFT fabrication were summarized in Table 1. In the case of the thickness smaller than 1 nm, the density of the PMMA layer was smaller than the value of bulk PMMA(1.19 g/cm^3), suggesting that SiO_2 surface was partially covered with PMMA. This coverage became larger with the increase of the PMMA thickness, and finally the full coverage of PMMA on SiO_2 surface was attained for the thickness of 1.3 nm and over. The small surface roughness of the PMMA layer (smaller than 0.5 nm) was common for all the specimens. Thus, ultrathin polymer film with a uniform coverage and a very flat surface could be reproducibly fabricated by spin-coating, despite the fact that the film thickness was comparable to self-assembled monolayers such as silane coupling reagents [14,15]. The density of the 0.6-nm thick PMMA was 0.72 g/cm^3 (i.e.,

61 % of the surface coverage). Since the length between CH_3O and CH_3 groups in a side chain of a single molecular unit of PMMA is smaller than 0.6 nm, it can be considered for the 0.6-nm thick film that the SiO_2 surface was partially covered with small islands of PMMA monolayer.

3.2 Electron trapping in the MIS structures between PTCDI-C13 films and SiO_2 insulators with ultrathin PMMA layers

For discussing the trap suppression effect of the PMMA layers, the capacitance(C)-gate voltage(V_G) curve for the MIS structure between source and gate electrodes was measured in a vacuum. As shown in Fig. 3, typical injection-type hysteresis curves due to electron trapping appeared and the smaller hysteresis with the larger PMMA thickness and coverage was observed. The hysteresis suppression can be mainly attributed to the reduction of electric charges trapped at the semiconductor/insulator interface due to the coverage of SiO_2 with PMMA.

The amount of trap charge (N_t) was determined from the measured $C-V_G$ curves using the Berglund method which is applicable to the quasi-static capacitance-voltage data [16]. When the applied gate voltage is varied from V_{G1} to V_{G2}, the change in the potential at the semiconductor-insulator interface (Ψ) is given as

$$\Psi(V_{G2}) - \Psi(V_{G1}) = \int_{V_{G1}}^{V_{G2}} \left[1 - \frac{C(V_G)}{C_i} \right] dV_G, \qquad (2)$$

where $C(V_G)$ is the measured C-V_G curve (per unit area). Using this relation between Ψ

and V_G, the trap charge due to gate-biasing can be roughly estimated by calculating the

area surrounded by the forward ($C_f(V_G)$) and reverse ($C_r(V_G)$) gate-sweep $C-V_G$ curve as

follows;

$$N_t = \frac{1}{e} \int_{V_{G1}}^{V_{G2}} [C_f(V_G) - C_r(V_G)] dV_G, \qquad (3)$$

where e was the elementary charge. N_t values obtained here contained charges trapped

at both the semiconductor-insulator interface and inside the semiconductor films.

However, the film structures in the PTCDI-C13 films such as the surface morphology

and the crystal structure were almost identical for all the specimens employed in this

study (not shown here), so we assumed that there was almost no difference in trap states

inside the semiconductor films.

A plot of N_t vs. surface coverage is shown in Fig. 4. N_t was decreased by one

order of magnitude by the full-coverage PMMA layer (from 1×10^{12} (Region 1) to

1×10^{11} cm^{-2} (Region 4)). The rapid decrease of N_t at around 0.7 g/cm^3 (from Region 2 to

3 in Fig. 4) can not be explained only by the increase of the PMMA coverage of the

SiO$_2$ surface, because it can be simply considered that the decrease of the trap charge is

proportional to the increase of the coverage. Since the PMMA thickness was 0.6-0.7 nm

in Region 2 and 0.8-1.0 nm in Region 3, electron tunneling through gate spacers should be taken into account. The tunneling effect might be remarkable in Region 2, while the suppression of the electron tunneling effect can assist the rapid reduction of the trapped charges in Region 3. In Region 4 (the PMMA thickness of 1.3-3.1 nm), N_t was almost constant at the lowest value (1×10^{11} cm^{-2}) since all the specimens showed a full coverage of SiO$_2$ with PMMA. From this C-V analysis, it can be said that the electron tunneling at the semiconductor/insulator interface was prominent when the PMMA became thinner than 0.8 nm, and that the thickness of the gate passivation layer should be at least 1 nm for keeping carrier accumulation/depletion cycles without any hysteresis.

3.3 N-channel conduction of the PTCDI-C13 TFTs with ultrathin PMMA layers

Fig. 5 presents the transfer characteristics of the PTCDI-C13 OTFTs fabricated onto PMMA spacers with various thicknesses. As for the measurements in a vacuum, as shown in Fig. 5(a), the drain current (I_D) for the OTFTs with the PMMA spacer became larger than for the devices without PMMA. The hysteresis in I_D−V_G curve was also suppressed with the increase of the PMMA thickness, which is consistent with the results of C−V_G measurements.

The relationship between the PMMA density and corresponding electron field-effect mobility in a vacuum (Fig. 5(b)) showed that the electron mobility can be increased by coating PMMA on the SiO$_2$ surface. The increase of the mobility can be explained with the multiple trapping and release (MTR) model [17,18], where the effective electron mobility (μ_e) at temperature T is given by

$$\mu_e = \mu_0 \frac{1}{1 + \dfrac{N_{T0}}{N_{C0}} \exp(\dfrac{E_a}{kT})}. \qquad (4)$$

μ_0 is the free carrier mobility. N_{T0} and N_{c0} are the density of the available trap states and the density of states at the conduction band. E_a and k are the activation energy and Boltzmann constant. Eq. (4) suggests the possibility that the decrease of the density of available (shallow-level) trap states deriving from hydroxyls on SiO$_2$ leads to the increase of the effective mobility. In Eq. (4), the monotonic increase of μ_e with the decrease of N_{T0} is expected on the assumption of a single trap state at activation energy E_a. However, the data in Fig. 5(b) does not obey this formula completely. The measured mobility was almost kept constant regardless of the PMMA density and thickness (less than 3.1 nm), once after the mobility raised from 7.5×10^{-2} to 0.16 cm^2/Vs by employing 0.7-nm thick PMMA with the density of 0.60 g/cm^3. This means that a partial coverage of the passivation layer on SiO$_2$ is sufficient for improving the n-channel conduction.

One of the possible reasons for this discrepancy between the MTR model and Fig. 5(b) is that various interface states due to surface species on SiO_2 exist, so that the activation energy (E_a) for each interface state can show a certain distribution with nonuniform activities as electron trap.

In a past study on N,N'-didodecyl-3,4,9,10-perylene tetracarboxylic diimide (PTCDI-C12), it was reported that top-contact PTCDI-C12 OTFTs fabricated on both untreated SiO_2 and SiO_2 covered with poly(α-methylstyrene) (PS) showed similar field-effect mobility [18], which is distinct from our present result. Differing from PMMA, each molecular unit of PS has one benzene ring which might capture electrons at the semiconductor/insulator interface. Therefore, PMMA is presumably more suitable for reducing interface electron traps and enhancing the effective mobility.

The air stability of the OTFTs was also improved by using the PMMA gate spacer, while n-channel operation almost disappeared just after the air exposure of the transistor without any polymer layer as seen in Fig. 5(c). The positive shift of threshold voltage and the decrease of the drain current for the device with a partial coverage of PMMA (0.6-nm thick) proceeded faster than the specimen with a full coverage of PMMA (1.3-nm thick). Since it was reported that the direct water adsorption on SiO_2 surface deteriorates n-channel operation in ambient air [7,8], the data in Fig. 5(c) clearly

reveal that a uniform passivation layer on the gate insulator is prerequisite for improving the air stability of n-channel OTFTs.

It is worth noting that even 0.6-nm thick PMMA film contributed to the enhancement of the electron transport (Fig. 5(a) and (b)), and that 1.3-nm thick PMMA caused the similar improvement of air-stable n-channel operation with thicker PMMA spacers (Fig. 5(c)). This result reflects a very high degree of uniformity of the prepared PMMA ultrathin films over large areas of SiO_2 surface.

4. Conclusions

The electron trapping behavior at the interface between the PTCDI-C13 film and SiO_2 gate insulator was examined by inserting ultrathin PMMA gate passivation layers with well-controlled thickness and density.

In the C-V_G analysis for the MIS structures, electron tunneling through PMMA layer was prominent with the PMMA thinner than 0.8 nm. It was also suggested that the thickness of the gate passivation layer should be at least 1 nm for preventing injection-type hysteresis in carrier accumulation/depletion processes.

Transistor measurements demonstrated that ultrathin PMMA layer with a small surface roughness, which is comparable to self-assembled monolayers, can work as

enhancer for *n*-channel conduction in OTFTs. The effective electron mobility was increased by suppressing shallow-level interface traps with PMMA layer, which can be partially accounted for by the multiple trap and release model. Moreover, complete (full-coverage) passivation on the gate insulator is indispensable for air-stable *n*-channel operation.

Acknowledgements

References

[1] J. Zaumseil, H. Sirringhaus, Chem. Rev. 107 (2007) 1296.

[2] F.-C. Chen, C.-H. Liao, Appl. Phys. Lett. 93 (2008) 103310.

[3] D. Kumaki, T. Umeda, S. Tokito, Appl. Phys. Lett. 92 (2008) 093309.

[4] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, R. H. Friend, Nature 434 (2005) 194.

[5] Th. B. Singh, F. Meghdadi, S. Günes, N. Marjanonic, G. Horowitz, P. Lang, S. Bauer, N. S. Sariciftci, Adv. Mater. 17 (2005) 2315.

[6] T. Sakanoue, M. Yahiro, C. Adachi, K. Takimiya, A. Toshimitsu, J. Appl. Phys 103 (2008) 094509.

[7] S. Tanida, K. Noda, H. Kawabata, K. Matsushige, Thin Solid Films 518 (2009) 571.

[8] S. Tanida, K. Noda, H. Kawabata, K. Matsushige, Polym. Adv. Technol. (2009), doi:10.1002/pat.1474.

[9] K. Noda, S. Tanida, H. Kawabata, K. Matsushige, Synth. Met. 160 (2010) 83.

[10] S. Tatemichi, M. Ichikawa, T. Koyama, Y. Taniguchi, Appl. Phys. Lett. 89 (2006) 112108.

[11] N. Ohta, M. Koizumi, Y. Nishimura, I. Yamazaki, Y. Tanimoto, Y. Hatano, M. Yamamoto, H. Kono, J. Phys. Chem. 100 (1996) 19295.

[12] L. G. Parratt, Phys. Rev. 95 (1954) 359.

[13] J. Puigdollers, C. Voz, A. Orpella, R. Quidant, I. Martin, M. Vetter, R. Alcubilla, Org. Electron. 5 (2004) 67.

[14] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, Y. Iwasa, Nature Mater. 3 (2004) 317.

[15] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, F. Stellacci, Nature 431 (2004) 963.

[16] C.N. Berglund, IEEE Trans. Electron Devices 13 (1966) 701.

[17] N. Kawasaki, Y. Ohta, Y. Kubozono, A. Konishi, A. Fujiwara, Appl. Phys. Lett. 92 (2008) 163307.

[18] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva Filho, J.-L. Brédas, L. L. Miller, K. R. Mann, C. D. Frisbie, J. Phys. Chem. B 108 (2004) 19281.

Figure Captions

Fig. 1. Chemical structures of (a) poly(methyl methacrylate) (PMMA) and (b) *N,N'*-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C13). (c) A device structure of a PTCDI-C13 TFT with a PMMA gate spacer.

Fig. 2. X-ray reflectivity profiles for the PMMA films prepared onto SiO_2/Si substrates, using PMMA toluene solutions with various concentrations. The solid lines are the curves best-fitted for the experimental results (open circles). The PMMA thicknesses calculated from the fitting curves were indicated in the profile.

Fig. 3. Capacitance-voltage curves measured for the metal-insulator- semiconductor (MIS) structure between source and gate electrodes of the PTCDI-C13 OTFTs in a vacuum. The thicknesses of the PMMA gate spacers were (a) 0 (untreated), (b) 0.6 nm, and (c) 0.9 nm, respectively.

Fig. 4. A plot of the density of the ultrathin PMMA film against the trapped charge in the MIS structures for the PTCDI-C13 OTFTs. According to the PMMA thickness, the data points were categorized into the following four regions; untreated SiO_2 (Region 1),

0.6-0.7 nm (Region 2), 0.8-1.0 nm (Region 3) and 1.3-3.1 nm (Region 4).

Fig. 5. (a) Transfer characteristics of the PTCDI-C13 OTFTs measured in a vacuum and (b) A plot of the density of the ultrathin PMMA film against the electron mobility obtained from the measurements. (c) Transfer characteristics of the PTCDI-C13 OTFTs measured under ambient condition (10 minutes after the air exposure of the devices). The drain-source voltage (V_D) was set to be 60 V for all the measurements. In the figures of (a) and (c), the thicknesses of the PMMA gate spacers were 0 (untreated SiO_2, solid line), 0.6 nm (dashed line), and 1.3 nm (solid circle), respectively.

Table caption

Table 1 Structural parameters of the ultrathin PMMA films obtained from the X-ray

reflectivity profile in Fig. 2.

Figure1

(a)

~ 0.6 nm

(b)

$C_{13}H_{27}$-N   N-$C_{13}H_{27}$

(c)

Source		Drain

50 μm

Au   Au   25 nm

PTCDI-C13   30 nm

PMMA

SiO$_2$ 300 nm

n$^+$-doped Si   Gate

Figure2

Left panel — labels: PMMA, SiO$_2$ (300 nm), n$^+$-doped Si; curves labeled "untreated", "0.6 nm", "0.9 nm". Axes: Reflectivity (arb.unit) vs 2θ (deg.).

Right panel — curves labeled "1.3 nm", "2.2 nm", "3.1 nm". Axes: Reflectivity (arb.unit) vs 2θ (deg.).

Figure3

(a)

(b)

(c)

Figure4

Figure5

(a)

(b)

(c)
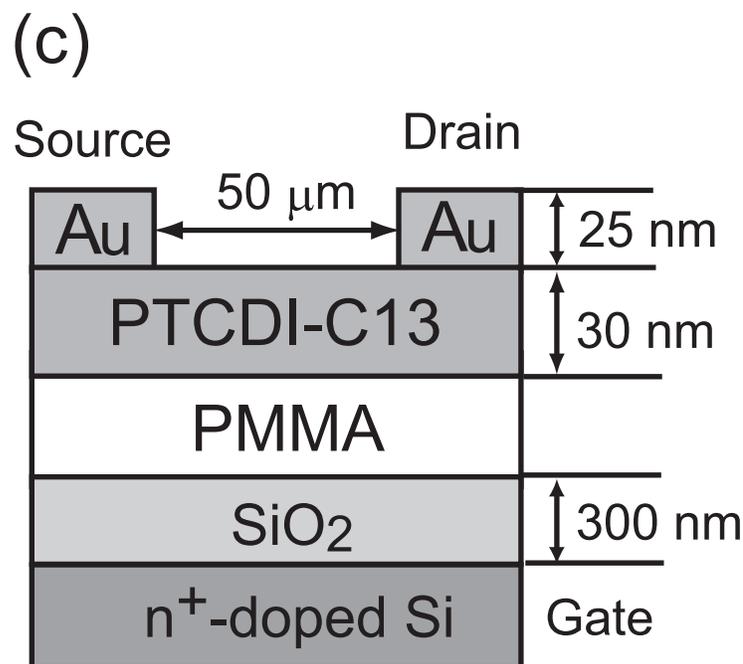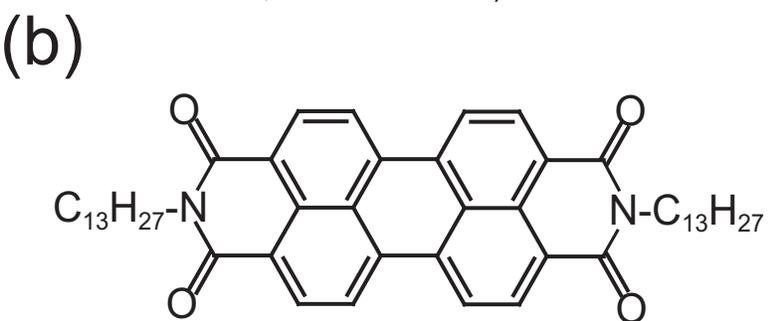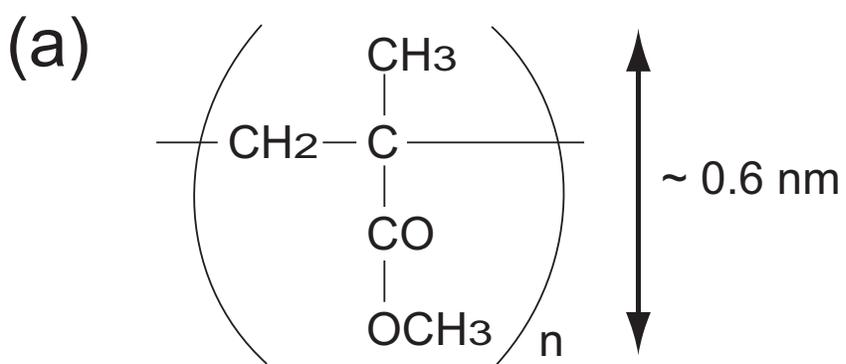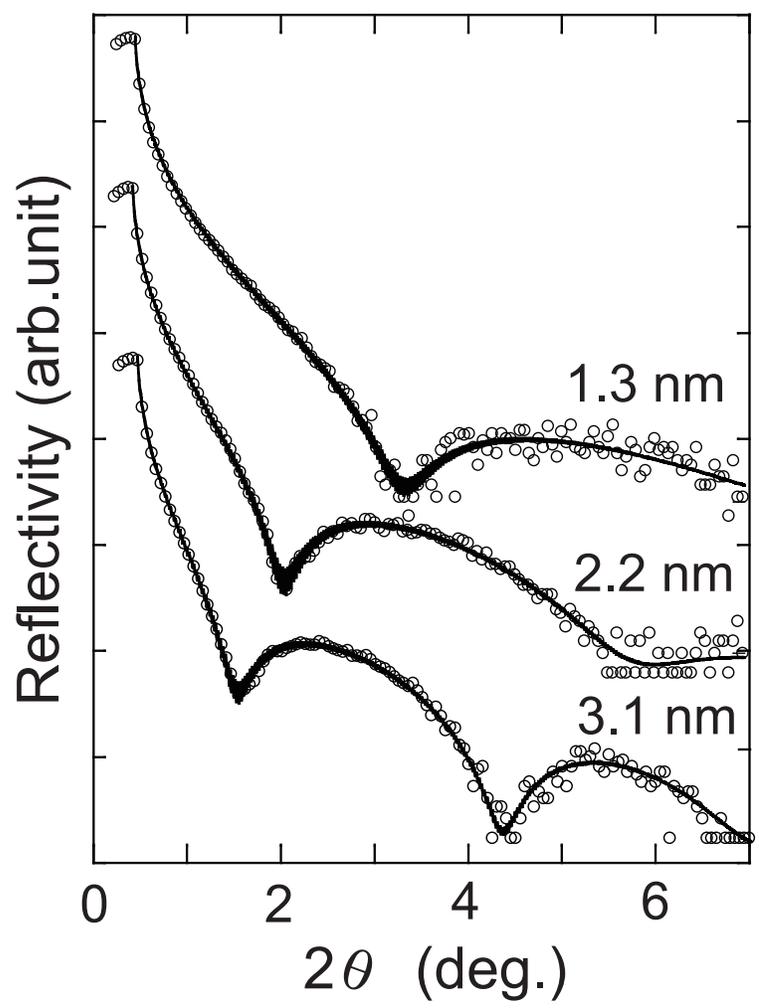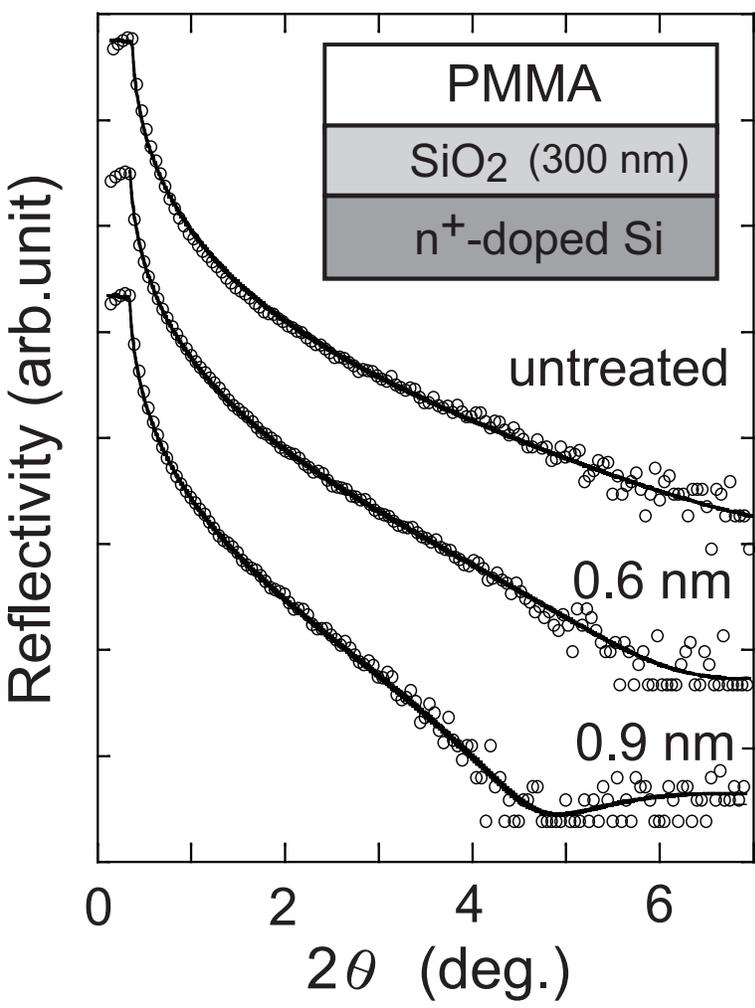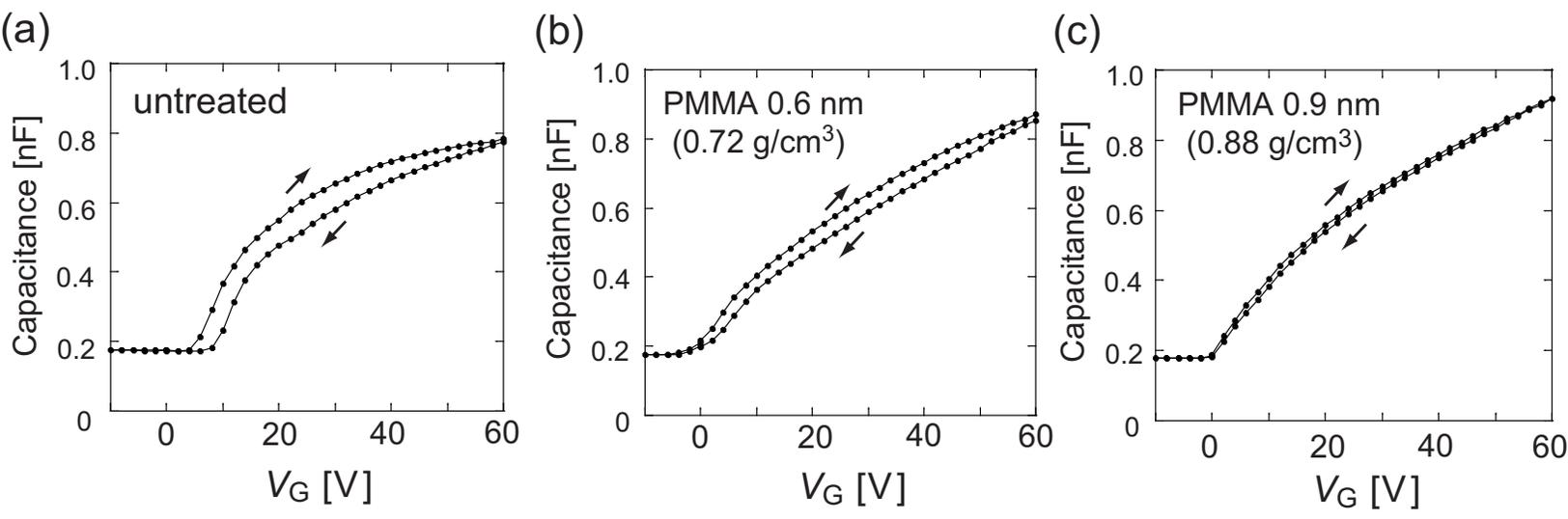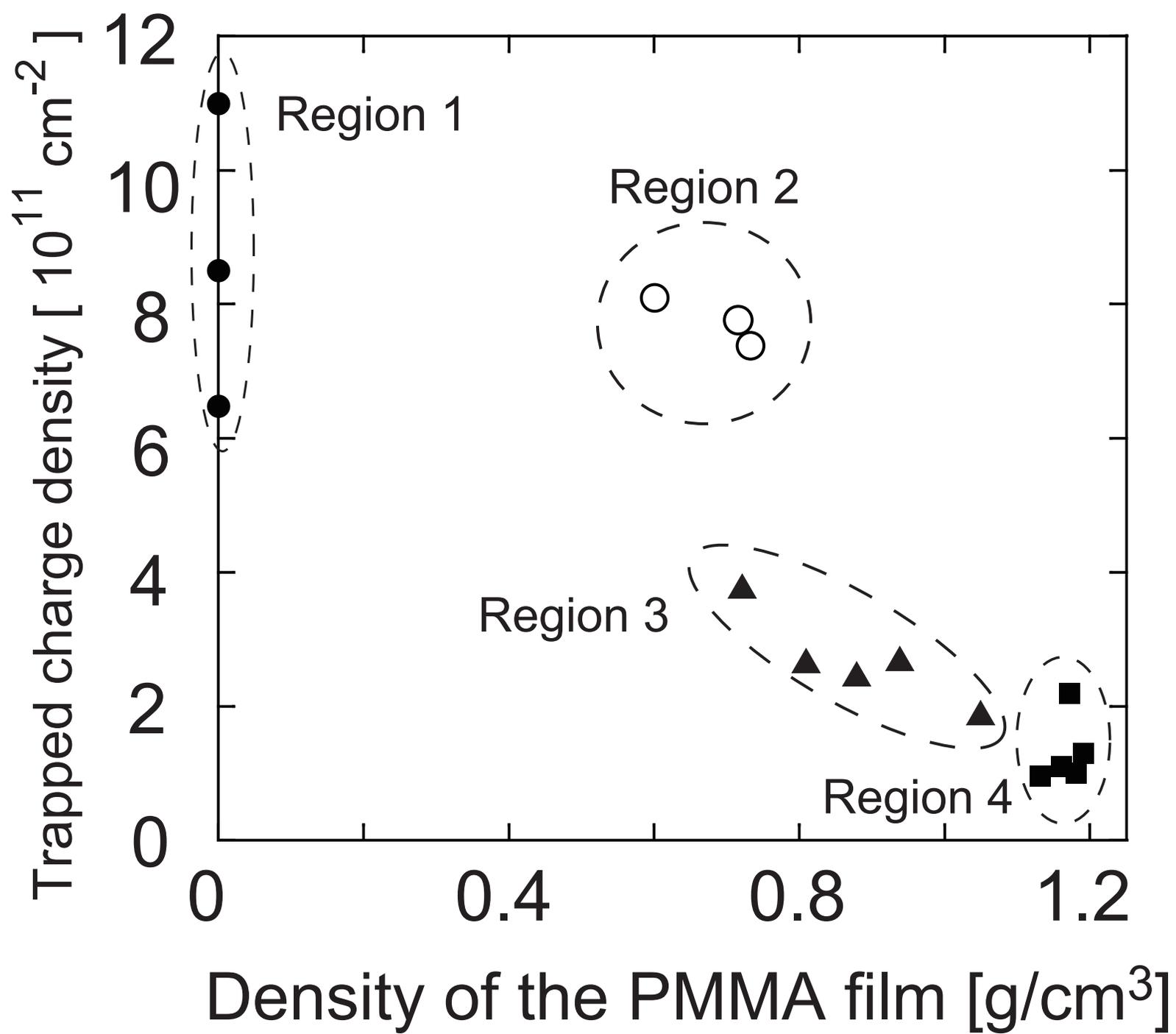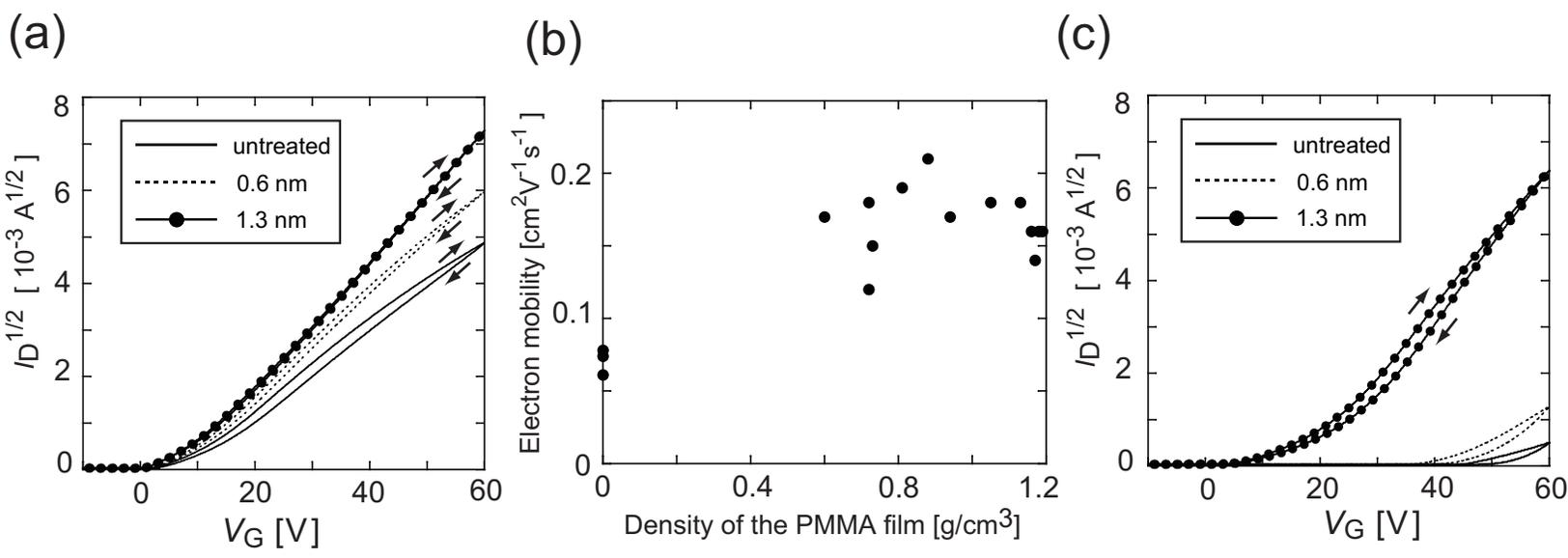
Table1

Thickness(nm)	Density(g/cm^3)	Roughness(nm)
0.6	0.72	0.15
0.9	0.88	0.26
1.3	1.13	0.30
2.2	1.17	0.40
3.1	1.18	0.32