Characterization of SiC Power Transistors for Power Conversion Circuits Based on C-V Measurement

Nathabhat Phankong

Abstract

Power switching devices are required for power electronics to regulate and distribute the power and energy from power conversion circuits. Silicon carbide (SiC) as a wide band gap semiconductor is the promising material for power switching device applications due to their inherent material characteristics. In present, SiC power transistors, especially SiC power MOSFETs and JFETs, are the most possible power switches for high switching frequency power conversion circuits due to fast turn-off capability. Transient behavior in switching operation of SiC power transistors responds to charge/discharge phenomenon of terminal capacitances in the devices. The differential capacitance in a semiconductor device varies with the applied voltage in accordance with the depleted region thickness.

In this dissertation, we developed the C-V characterization system for high-voltage power transistors, which realizes the selective measurement of a specified capacitance from among several capacitances integrated in one device. Three terminal capacitances are evaluated to specify device characteristics–the capacitance for gate-source, gate-drain, and drain-source. The input, output, and reverse transfer capacitances are also evaluated to assess the switching behavior of the power transistors in the circuit. Next, we characterized the voltage dependence of terminal capacitances of the SiC power MOSFET, lateral-type SiC JFET, and vertical-type SiC JFET, and also characterized the static I-V characteristics of the power devices. Then, we evaluated the switching operation of the power devices with considering the charge/discharge behavior of terminal capacitances of the devices. Their device structures decide the voltage dependence of the capacitance characteristics, so that the C-V characteristics govern their switching behaviors. The results give us a clue to understand the switch-

ing dynamics of the power devices. The simulated switching behavior of the power devices is validated with the experimental results. It is clearly shown that the simulated results in switching behavior of the power devices coincided with experimental results suitably.

In the end, we demonstrated the operation of the SiC power MOSFET in a high frequency switching converter circuit for evaluating its performances The experiment results showed smooth waveforms of the current and voltage. Therefore, the SiC power MOSFET can be suitably used in the high frequency switching converter circuit to regulate the output voltage.

Keywords: SiC, MOSFET, JFET, C-V characteristics, Switching behavior, Device structure

Acknowledgments

I cordially would like to express my deepest gratitude to Professor Takashi Hikihara, Department of Electrical Engineering, Graduate School of Engineering, Kyoto University, for his supervision, precisely continuous guidance, and kind encouragement to accomplish this study.

I deeply acknowledge Professor Tsuyoshi Funaki, Division of Electrical, Electronic, and Information Engineering, Graduate School of Engineering, Osaka University, for his valuable suggestion regarding experiments in this study, and critical concerning in the manuscript. Especially, I would like to acknowledge Professor Osami Wada and Professor Tsunenobu Kimoto, Graduate School of Engineering, Kyoto University, both for their helpful suggestions and for serving on my dissertation committee.

I am appreciated to express my sincere to Professor Kiyoshi Yoshikawa, Executive Vice-President for Research and International Relations, Kyoto University, for his recommendation to initiate my study in Department of Electrical Engineering, Kyoto University.

I would like to appreciate Assistant Professor Yoshihiko Susuki, Assistant Professor Keiko Saitoh, and Assistant Professor Nobuo Satoh, Department of Electrical Engineering, Kyoto University, for their contribution to accomplish this study. I also would like to give special thanks to all present members of Professor Hikihara's research group including the past members. In particular, I would like to thank Ms. Tomoko Oono, Mr. Suketu D. Naik, Mr. Yuuichi Yokoi, Mr. Tsuguhiro Takuno, Mr. Masataka Minami, and Mr. Keisuke Mima, for their facilitation to research environment.

I would like to convey my appreciate to the special support of the Global COE program, Environmental Nano-cluster project of the Ministry of Education, Culture,

Sports, Science and Technology in Japan, the 21st Century COE program, and Rajamangala University of Technology Thanyaburi. I am also grateful to ROHM Company, Ltd., Sumitomo Electric, Ltd., and Dr. P. Friedrichs (SiCED) for their supports to the samples of SiC power devices.

I would like to express my special gratitude to Assistant Professor Somchai Hiranvarodom, Assistant Professor Sommai Pivsa-art, and Dr. Surin Ngaemngam, Faculty of Engineering, Rajamangala University of Technology Thanyaburi, for their supports and suggestions. I also acknowledge the members of Department of Electrical Engineering, Rajamangala University of Technology Thanyaburi, and particularly Thai students society in Kyoto University.

Finally, I personally would like to express my grateful to my family, Mr. Pian Phankong, Mrs. Paradee Phankong, Ms. Thanaban Phankong, Mr. Kittithat Phankong , and Ms. Naparat Amornputtisathaporn, for their constant supports and inspiration as well as warm encouragement. I also would like to thank Associate Professor Jakaew Tanunath and Mrs. Niramol Tanunath, for their encouragement.

Contents

Abstract **i**

Acknowledgments **iii**

1 Introduction **1**

1.1 SiC power devices 1

1.2 Characterization of SiC power transistors 2

1.3 Purpose and overview 5

2 Device structure and internal parasitic capacitances of SiC power MOSFET and SiC JFET **9**

2.1 Introduction 9

2.2 Device structure and internal parasitic capacitances of SiC power MOSFET 10

2.2.1 Device structure of SiC power MOSFET 10

2.2.2 Internal parasitic capacitances of SiC power MOSFET 11

2.3 Device structure and internal parasitic capacitances of SiC JFET . . . 29

2.3.1 Device structure of SiC JFET 29

2.3.2 Internal parasitic capacitances of SiC JFET 30

2.4 Summary 35

3 Measurement of terminal capacitances and its voltage dependency for high-voltage power transistors **37**

3.1 Introduction 37

3.2 Capacitance of a power device and measurement circuit 39
3.2.1 Terminal capacitances of VDMOSFET 39
3.2.2 C_{GS} measurement circuit 41
3.2.3 $C_{GD}(C_{RSS})$ measurement circuit 43
3.2.4 C_{DS} measurement circuit 43
3.2.5 C_{ISS} measurement circuit 44
3.2.6 C_{OSS} measurement circuit 45
3.3 Measurement of C-V characteristics 47
3.3.1 Certification of the measurement circuit 48
3.3.2 Measured Results 49
3.4 Summary 52

4 Characterization of SiC power MOSFET **53**
4.1 Introduction 53
4.2 Characterization 55
4.2.1 Forward dc characteristics of power MOSFET 55
4.2.2 Reverse conduction dc characteristics of power MOSFET 58
4.2.3 C-V characteristics of power MOSFET 59
4.2.4 Dynamic behavior of power MOSFET 66
4.3 Evaluation of switching response 66
4.4 Summary 69

5 Characterization of SiC JFET **79**
5.1 Introduction 79
5.2 Characterization of SiC JFET devices 81
5.2.1 Static I-V characteristics 82
5.2.2 C-V characteristics 84
5.2.3 Switching characteristics 85
5.3 Results of C-V and switching characteristics of SiC JFETs 86
5.3.1 C-V characteristics 86
5.3.2 Switching characteristics 89

5.4 Summary 91

6 An application of SiC power transistors **93**

6.1 Introduction 93

6.2 Resonant-switch dc-dc step-up voltage converter 94

6.2.1 Power circuit 94

6.2.2 Control circuit 96

6.2.3 Modes of operation—resonant-switch dc-dc step-up voltage converter 98

6.3 Experimental results of resonant-switch dc-dc step-up voltage converter 103

6.4 Summary 111

7 Conclusions **113**

Bibliography **117**

List of Publications **125**

Chapter 1

Introduction

The purpose of this introductory chapter is to present motivations and overviews of the works done in this dissertation. A more in-depth introduction is given in each of main chapters of this dissertation.

1.1 SiC power devices

Silicon carbide (SiC) has several properties such as high breakdown voltage, high temperature operation capability, and high thermal conductivity, making them potentially superior to Silicon (Si) semiconductors and thus making them attractive for power devices [1–5]. Among the other SiC semiconductors, 4H-SiC is the most promising material for power switching device applications due to their inherent material characteristics, quality of the crystal growth, and the maturity of manufacturing process. Some of the electrical and material properties of Si and 4H-SiC are summarized and compared in Tab. 1.1, which are pertinent for power device applications [2, 6, 7].

For the great advantages of SiC power devices, SiC diodes have studied well [9–13] and Schottky Barrier Diodes (SBDs) made of 4H-SiC with sufficiently high current and voltage ratings have already been commercialized by some manufactures [14]. The advantages of SiC SBDs in power conversion circuits have been reported in [15–18]; e.g., no reverse recovery current, no temperature influence on the switching behavior, no forward recovery, fast switching, and so on. Various types of controllable switching

Table 1.1 A comparison of the electrical and material properties of Si and 4H-SiC for power device applications at room temperature 300 K.

Parameters	Si	4H-SiC
Energy band gap E_{G} (eV)	1.11	3.26
Intrinsic carrier concentration n_{i} (cm^{-3})	1.4×10^{10}	6.7×10^{-11}
Electron mobility μ_{n} (cm^{-3})	1400	947
Hole mobility μ_{p} (cm^{-3})	450	124
Relative dielectric constant ϵ_{s}	11.7	9.7
Saturation drift velocity v_{sat} (cm/s)	1×10^{7}	2.1×10^{7}
Critical electric field for breakdown E_{crit} (V/cm)	2.5×10^{5}	2.2×10^{6}
Thermal conductivity (W/cm-K)	1.5	3.7

devices have been proposed, but they are currently under development [19–21]. The main research now focuses on the unipolar devices of such as Junction Field-Effect Transistor (JFET) and Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). SiC JFETs are expected to be the first commercial transistor available in this technology, and SiC MOSFETs are nearing commercial viability. The characteristics of the switching devices must be analyzed and modeled, so that SiC power devices based applications can be designed and built.

1.2 Characterization of SiC power transistors

Power electronics require high efficiency and versatile power conversion. High voltage capability is preferable, especially in high-power conversion circuits, to reduce the conduction loss by large currents. High-frequency switching enables minimization of bulky passive components and provides control functionality. Power switching devices are the key components to realize them; therefore, the developments focus on a power device with a high breakdown voltage, low forward voltage drop, and fast switching capability [3, 7, 22, 23]. However, the limitations to the above requirements are not sufficient for the silicon (Si) power devices. To overcome the difficulty, SiC

power devices have been researched and developed to realize lower loss, higher voltage breakdown, and faster switching with a thin voltage blocking layer. And also, the largest efforts have concentrated on unipolar (SiC power switching devices). These include Field-Effect Transistors (FETs) such as JFET, MOSFET, and so on. Therefore, power MOSFETs and JFETs are the most possible power switches in present for high switching frequency power converters due to fast turn-off capability. Power MOSFETs have a high input impedance that makes the gate drive circuitry very simple [4, 5, 20]. JFETs, which have the possibility of lateral-type and vertical-type structure, are preferred because of the low resistance and ruggedness in harsh environments [21, 24–26].

The switching behavior of actual power devices cannot be ideal. The non-ideal characteristics of SiC power devices affect on the performance of power conversion circuits, especially at high switching frequency. Then, the characteristics of devices must be clarified and evaluated in advance of the design of power conversion circuits. Here, the switching characteristics of SiC power MOSFET and SiC JFET are discussed with relation to their ac characteristics and dc characteristics [27–30]. The ac characteristics are involved with their internal parasitic capacitances. The internal parasitic capacitances residing in the SiC power MOSFET are composed of the gate oxide and the depletion region formed in the semiconductor [7, 8, 31]. The internal parasitic capacitances residing in the SiC JFET are the depletion region formed at pn junction [29,32]. The capacitances of the SiC power MOSFET and the SiC JFET are integrated into the terminal capacitances, which are charged and discharged during turn-on and turn-off operations [33, 34]. The terminal capacitances of the power devices increase as the thickness of the voltage blocking layer is reduced to minimize conduction resistance. The capacitances vary widely with the applied bias voltage because of depletion region in the voltage blocking layer. Therefore, it is necessary to quantify these capacitances of the power devices as well as the voltage dependence of capacitances. There is no commercial apparatus that is able to measure the terminal capacitances of a high-voltage power device with applying the bias voltage up to its rated value. JEDEC [35] and IEC [36] standardized the capacitance measurement methods between the terminals of a power device with a capacitance bridge, but no actual configuration or circuit topology for the measurements are provided. Elferich *et al.* [37] measured the

C-V characteristics of a power MOSFET and validated the finite-element (FE) device simulation; however, the measurement setup is not clearly described and the applied voltage was low ($0\ \mathrm{V} \leq V_{\mathrm{DS}} \leq 20\ \mathrm{V}, -10\ \mathrm{V} \leq V_{\mathrm{GS}} \leq 0\ \mathrm{V}$). Therefore, we developed a C-V measurement system for high-voltage power devices. Funaki *et al.* [38, 39] presented the C-V measurement system for high-voltage power diodes with evolving [40] and clarified the punch-through structure of SiC SBDs from the measured results. This study develops a C-V measurement system for gate-controlled, high-voltage power devices, e.g., power MOSFET, JFET, and so on. There exist three terminals (Gate, drain, and source terminals) in a single device, and five specifications of the capacitance measurement circuit for C_{GS}, $C_{\mathrm{GD}}(= C_{\mathrm{RSS}})$, C_{DS}, C_{ISS}, and C_{OSS} are presented to measure the terminal capacitances. On the contrary, the dc characteristics of the power devices are easily measured by a curve tracer.

A model of semiconductor device is indispensable for evaluating the voltage and current responses at switching in circuit simulation and estimating the system performance in their applications. The dynamics at the transient state are obviously governed by these characteristics of power devices.

This dissertation characterizes the voltage dependency of terminal capacitances of the SiC power MOSFET, lateral-type SiC JFET, and vertical-type SiC JFET, models the I-V characteristics with discussing the C-V characteristics of the power devices, and extracts the model parameters from the measured C-V characteristics. Then, the switching behavior of the power devices is experimentally evaluated. Next, we discuss and compare the difference in voltage dependence of the terminal capacitances between the SiC power MOSFET and the Si power MOSFET, and also between the lateral-type SiC JFET and the vertical-type SiC JFET to estimate the difference in their switching behaviors based on their device structures and the semiconductor physics. In the end, the simulated switching behavior of the power devices is validated with the experimental results. The SiC power MOSFET is also experimentally evaluated its performances in a high frequency switching converter circuit.

1.3 Purpose and overview

This dissertation aims to characterize the C-V characteristics of the SiC power MOSFET, lateral-type SiC JFET, and vertical-type SiC JFET with capacitance measurement system at first. Then the static I-V and switching characteristics of the devices are experimentally evaluated with a curve tracer and in power conversion circuits. Also, this study discuses and clarifies the difference of these characteristics between SiC and Si power MOSFETs. The difference in device structures is also focused on between lateral-type and vertical-type SiC JFETs. Finally, the models of the devices are validated by comparing the experimental results on the switching response.

Chapter 2 begins with the introduction of physics and device structures of the SiC power MOSFET and SiC JFET. At first, the simplified cross section of single cell structure in a SiC Double-implanted MOSFET (DiMOSFET) is explained with considering the physical capacitances, which are composed of the gate oxide and the depletion layer formed in the semiconductor. They are integrated into the equivalent capacitances between terminals. Secondly, the cross sections of the lateral-type and vertical-type SiC JFET cells are also explained with considering that the depletion region formed at pn junction behaves as parasitic capacitances, which are lumped into terminal capacitances. The thickness of depletion region changes with the applied reverse bias voltage. Therefore, the dependence of the depletion capacitance on the reverse bias voltage can be represented by the uniformly doped and linearly graded doped capacitances.

In Chapter 3, we describe the developed C-V characterization system for high-voltage power transistors (e.g., MOSFET, IGBT, and JFET). The system realizes the selective measurement of a specified capacitance among several capacitances integrated in one device. Three capacitances between terminals are evaluated to specify device characteristics. They are the capacitances for gate-source, gate-drain, and drain-source. The input, output, and reverse transfer capacitance are also evaluated to assess the switching behavior of the power transistor in a circuit. Thus, this chapter discusses the five specifications of a C-V characterization system and its measurement results. Moreover, the developed C-V characterization system enables measurement

of the transistor capacitances from its blocking condition to the conducting condition with varying gate bias voltage. The measured C-V characteristics show intricate changes in the low-bias-voltage region, which reflect the device structure. The monotonic capacitance change in the high-voltage region is attributable to the expansion of the depletion region in the drift region. These results help us to understand the dynamic behavior of high-power devices during switching operation.

In Chapter 4, the characteristics of the SiC power MOSFET are characterized and modeled. The charge/discharge phenomenon of terminal capacitances and static I-V characteristics affect on its switching behavior of the device. Models for Si power MOSFET have already been obtained through the previous studies. Based on the model, a model for SiC power MOSFET is proposed with including the semiconductor physics, the structures of the device, and extracted parameters from the measured C-V characteristics. The static I-V characteristics are also discussed with the C-V characteristics. And also, this chapter characterizes the relationship between the input capacitance of the SiC power MOSFET and the gate voltage with considering the internal device structure. It compares the difference in gate-source voltage dependency between the SiC power MOSFET with Si power MOSFET in order to estimate the switching behavior. The results give us a clue to understand the switching characteristics of the power MOSFET. It is clearly shown that the simulated results in switching behavior of the proposed model coincide with experimental results suitably in some conditions.

In Chapter 5, the characteristics of the lateral-type and vertical-type SiC JFETs are characterized and modeled. The both types of SiC JFET studied here are normally-on type devices. The transient behavior in switching operation of the SiC JFETs is discussed with their intrinsic parasitic capacitances. Therefore, this chapter characterizes both C-V characteristics at first, and then the switching behavior is experimentally evaluated. The terminal capacitances of both types of SiC JFET are substantial for understanding the switching characteristics. Finally, the difference of these characteristics is discussed between lateral-type and vertical-type structures with the parasitic capacitances of the devices. The voltage dependency of the capacitance characteristics remarkably shows their device structure. Their switching phenomenon is clearly

grasped.

In Chapter 6, the SiC power MOSFET is experimentally evaluated its performances in a high frequency switching converter circuit. We demonstrate the operation of the SiC power MOSFET in the resonant-switch dc-dc step-up voltage converter as switch to control the output current and voltage. Additionally, the results of the resonant converter by using the SiC power MOSFET are compared with the results by using Si power MOSFET.

In Chapter 7, the conclusions of this study are summarized. Some proposals for the future works are also presented.

Chapter 2

Device structure and internal parasitic capacitances of SiC power MOSFET and SiC JFET

2.1 Introduction

Power semiconductor devices play a crucial role in the regulation and distribution of power and energy for many applications. Recently, power conversion circuits require the power switching devices to operate at high voltage, high-temperature, and fast switching. Power MOSFETs and JFETs are the most possible power switches for high frequency switching power converter circuits due to fast turn-off capability. The capacitances are inherently presented as internal parasitic devices in the structure of power MOSFETs and JFETs. These internal parasitic capacitances typically determine the high frequency behavior of the switching circuit. Also, the principle of operation of power MOSFETs and JFETs is essentially based on the capacitance effect.

Therefore, this chapter describes the device structure of a SiC power MOSFET, a lateral-type SiC JFET, and a vertical-type SiC JFET with considering the internal parasitic capacitances in their devices.

2.2 Device structure and internal parasitic capacitances of SiC power MOSFET

2.2.1 Device structure of SiC power MOSFET

Figure 2.1 illustrates the simplified cross section of one cell structure in a SiC Double-implanted MOSFET (DiMOSFET) studied in this study [7, 8]. SiC DiMOSFET is fabricated to have the structure similar to that of a Si Double-diffused MOSFET (DMOSFET) [27]. The main differences between these two devices are the fabrication process and dimensions of p well and n^+ source regions. They are formed by ion implantation for SiC DiMOSFET and shallower than a Si DMOSFET formed by diffusion. The various internal parasitic components of the device are superimposed on its cross section in Fig. 2.1.

The physical capacitances residing in the SiC DiMOSFET are composed of the gate oxide and the depletion layer formed in the semiconductor. They are integrated into the equivalent terminals capacitances of MOSFET, which are composed of gate-source capacitance C_{GS}, gate-drain capacitance C_{GD}, and drain-source capacitance C_{DS}. The C_{DS} corresponds to the junction capacitance stemmed by depletion at the junction

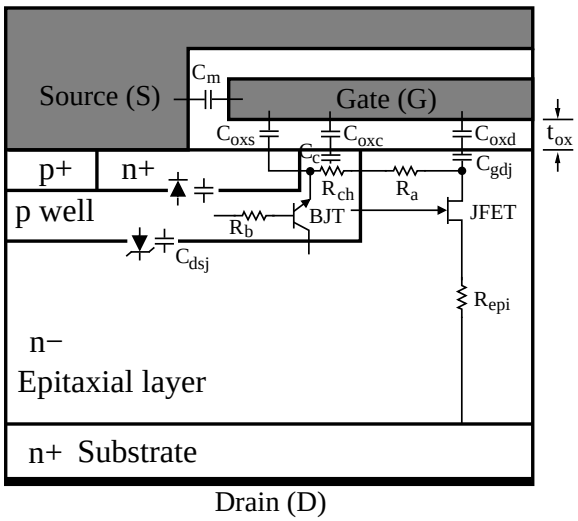


Figure 2.1 Cross section of a SiC DiMOSFET cell.

between the p well and the n^--epitaxial layer C_{dsj}. It largely depends on drain-source voltage V_{DS}. The two other C_{GS} and C_{GD} have MOS structures provided with inversion charge injectors. The C_{GS} is comprised of the gate oxide capacitance between the gate-source electrode C_{m}, the capacitance between the gate electrode and source n^+ region C_{oxs}, the capacitance between the gate electrode and the top surface of the p well region C_{oxc}, and the capacitance between the depletion region of the p well region under the gate C_{c}. The C_{c} varies depending on gate-source voltage V_{GS}. Though the polysilicon is utilized as gate electrode, it also depletes the applied gate voltage. It is heavily doped, so that its effect on the synthesized capacitance can be neglected [41]. As for C_{GD}, it is the series connection of the gate-drain oxide capacitance C_{oxd} and the drain depletion layer beneath the gate oxide capacitance C_{gdj}. It varies with gate-drain voltage $V_{\mathrm{GD}}(= V_{\mathrm{GS}} - V_{\mathrm{DS}})$.

2.2.2 Internal parasitic capacitances of SiC power MOSFET

Gate-Source capacitance C_{GS} [29, 42]

The dominant components of the gate-source capacitance C_{GS} of SiC DiMOSFET are shown in Fig. 2.1. C_{oxs}, C_{m}, and C_{oxc}, related to the gate oxide, do not change with the applied voltage. C_{c}, originated from the depletion layer in the top of p well, are associated with the depletion region formed in the semiconductor beneath the gate oxide. It can be derived from the depleted space charge Q_{s}, which varies as a function of the surface potential of semiconductor ψ_{s}. Here, the surface potential ψ_{s} is governed by gate voltage. The total gate-source capacitance C_{GS} can be given by Eq. (2.1):

$$C_{\mathrm{GS}} = C_{\mathrm{oxs}} + C_{\mathrm{m}} + C_{\mathrm{gb}}, \tag{2.1}$$

where

$$C_{\mathrm{gb}} = \frac{1}{1/C_{\mathrm{oxc}} + 1/C_{\mathrm{c}}}.$$

The surface potential ψ_{s} of p-type semiconductor (p well) obtained from the Pois-

son's equation:

$$\begin{aligned}\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} &= -\frac{\rho(x)}{\epsilon_\mathrm{s}} = -\frac{q}{\epsilon_\mathrm{s}}[p(x) - n(x) - N_\mathrm{A}] \\ &= -\frac{qN_\mathrm{A}}{\epsilon_\mathrm{s}}\Big[e^{-\psi(x)/\phi_\mathrm{t}} - 1 - e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(e^{\psi(x)/\phi_\mathrm{t}} - 1)\Big], \end{aligned} \tag{2.2}$$

where ρ denotes the charge density, N_A the accepter impurity concentration, ϕ_t the thermal voltage, and ϕ_F the Fermi potential. Multiplied both sides of Eq. (2.2) by $2\mathrm{d}\psi/\mathrm{d}x$;

$$\mathrm{d}\Big(\frac{\mathrm{d}\psi}{\mathrm{d}x}\Big)^2 = -\frac{2qN_\mathrm{A}}{\epsilon_\mathrm{s}}\Big[e^{-\psi(x)/\phi_\mathrm{t}} - 1 - e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(e^{\psi(x)/\phi_\mathrm{t}} - 1)\Big]\mathrm{d}\psi. \tag{2.3}$$

Integration both sides of Eq. (2.3) leads

$$\Big(\frac{\mathrm{d}\psi}{\mathrm{d}x}\Big)^2 = \frac{2qN_\mathrm{A}}{\epsilon_\mathrm{s}}\Big[\phi_\mathrm{t}e^{-\psi(x)/\phi_\mathrm{t}} + \psi - \phi_\mathrm{t} + e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{\psi(x)/\phi_\mathrm{t}} - \psi - \phi_\mathrm{t})\Big]. \tag{2.4}$$

When electric field potential $E(x) = -\mathrm{d}\psi/\mathrm{d}x$, therefore, the following is then obtained:

$$E(x) = -\frac{\mathrm{d}\psi}{\mathrm{d}x} = \pm\frac{\sqrt{2q\epsilon_\mathrm{s}N_\mathrm{A}}}{\epsilon_\mathrm{s}}\sqrt{\phi_\mathrm{t}e^{-\psi/\phi_\mathrm{t}} + \psi - \phi_\mathrm{t} + e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{\psi/\phi_\mathrm{t}} - \psi - \phi_\mathrm{t})}. \tag{2.5}$$

This gives $-E_\mathrm{s} = Q'_\mathrm{s}/\epsilon_\mathrm{s}$. Evaluating E_s with $\psi = \psi_\mathrm{s}$, the depleted space charge per unit area Q'_s is obtained as Eq. (2.6):

$$Q'_\mathrm{s} = \mp\sqrt{2q\epsilon_\mathrm{s}N_\mathrm{A}}\sqrt{\phi_\mathrm{t}e^{-\psi_\mathrm{s}/\phi_\mathrm{t}} + \psi_\mathrm{s} - \phi_\mathrm{t} + e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{\psi_\mathrm{s}/\phi_\mathrm{t}} - \psi_\mathrm{s} - \phi_\mathrm{t})}. \tag{2.6}$$

The electric field at the surface of the p-type semiconductor and the space-charge density in the p-type semiconductor are shown in Figs. 2.2 and 2.3, respectively. They vary with the surface potential ψ_s across the p-type semiconductor.

Therefore, the C_c is derived from the space charge Q_s. It can be discussed as a differential capacitance per unit area of the space-charge region in p-type semiconductor, which is given by Eq. (2.7):

$$C'_\mathrm{s} = -\frac{\mathrm{d}Q'_\mathrm{s}}{\mathrm{d}\psi_\mathrm{s}} = \pm\sqrt{2q\epsilon_\mathrm{s}N_\mathrm{A}}\Big[\frac{1 - e^{-\psi_\mathrm{s}/\phi_\mathrm{t}} + e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(e^{\psi_\mathrm{s}/\phi_\mathrm{t}} - 1)}{2\sqrt{\phi_\mathrm{t}e^{-\psi_\mathrm{s}/\phi_\mathrm{t}} + \psi_\mathrm{s} - \phi_\mathrm{t} + e^{-2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{\psi_\mathrm{s}/\phi_\mathrm{t}} - \psi_\mathrm{s} - \phi_\mathrm{t})}}\Big]. \tag{2.7}$$

Eqs. (2.6) and (2.7) are validated in all conditions as accumulation, depletion, and inversion.

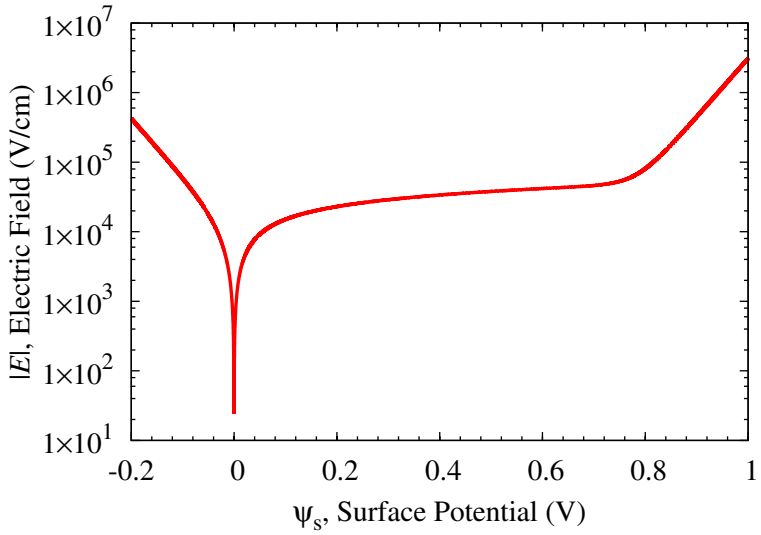


Figure 2.2 Electric field at the surface of the p-type semiconductor as a function of the surface potential.

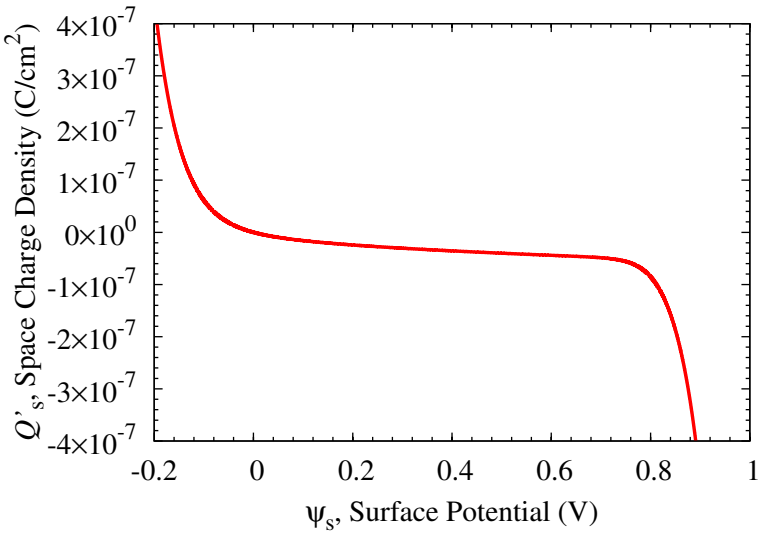


Figure 2.3 Variation of the space-charge density in the p-type semiconductor of a MOS junction as a function of the surface potential.

- Accumulation condition ($V_{GS} < V_{FB}$)

Figure 2.4(a) shows the structure of p-type semiconductor of power MOSFET, space-charge distribution $\rho(x)$, electric field strength $E(x)$, and internal potential ψ in ac-

cumulation condition. The condition in which $V_{\mathrm{GS}} < V_{\mathrm{FB}}$ is considered here. The surface potential ψ_{s} being less than zero ($\psi_s < 0$), Q'_s is positive and corresponds to the accumulation condition, which varies exponentially with the surface potential ψ_{s}. Because the first term on the right-hand side of Eq. (2.6) becomes dominant. The surface charge in p-type semiconductor for accumulation condition is given by

$$Q'_{\mathrm{s}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{A}}}\sqrt{\phi_{\mathrm{t}}e^{|\psi_{\mathrm{s}}|/\phi_{\mathrm{t}}}}, \tag{2.8}$$

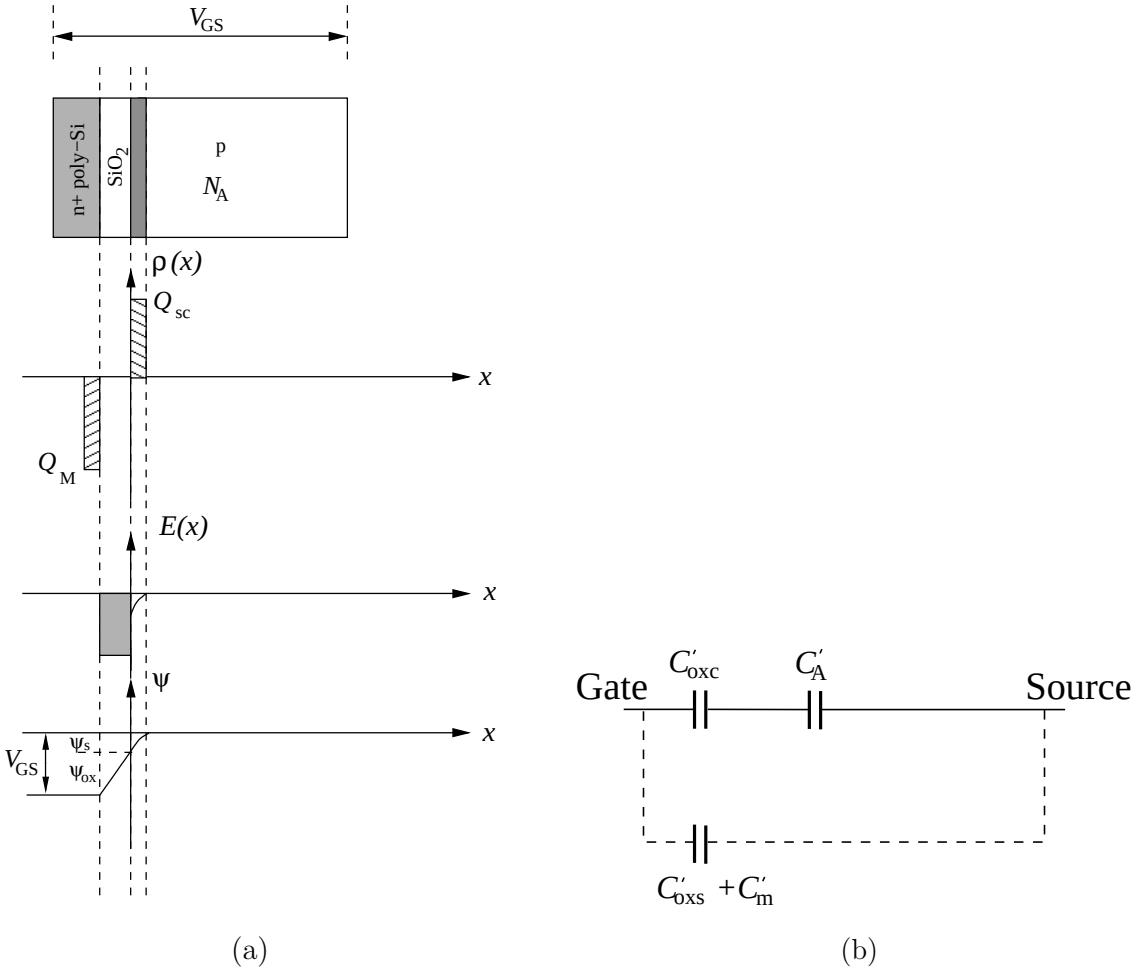


Figure 2.4 Formation of accumulation layer in p-type semiconductor. (a) Structure of p-type semiconductor of power MOSFET, space-charge distribution, electric field strength, and internal potential; (b) Equivalent capacitance C_{GS} in accumulation condition.

and the accumulation capacitance per unit area C'_{A}, which is shown in Fig. 2.4(b) as a part of the C'_{GS} capacitance, is equal to

$$C'_{\mathrm{A}} = -\frac{\mathrm{d}Q'_{\mathrm{s}}}{\mathrm{d}\psi_{\mathrm{s}}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{A}}}\frac{e^{|\psi_{\mathrm{s}}|/\phi_{\mathrm{t}}}}{2\sqrt{\phi_{\mathrm{t}}e^{|\psi_{\mathrm{s}}|/\phi_{\mathrm{t}}}}}. \tag{2.9}$$

Therefore,

$$\frac{1}{C'_{\mathrm{gb}}} = \frac{1}{C'_{\mathrm{oxc}}} + \frac{1}{C'_{\mathrm{A}}}. \tag{2.10}$$

where C'_{gb} is the gate-body capacitance per unit area and C'_{oxc} the gate-channel oxide capacitance per unit area.

- Depletion condition ($V_{\mathrm{T}} > V_{\mathrm{GS}} > V_{\mathrm{FB}}$)

Figure 2.5(a) shows the structure of p-type semiconductor of power MOSFET, space-charge distribution $\rho(x)$, electric field strength $E(x)$, and internal potential ψ in depletion condition. The condition in which $V_{\mathrm{T}} > V_{\mathrm{GS}} > V_{\mathrm{FB}}$ is considered here. The surface potential ψ_{s} being more than zero ($\phi_{\mathrm{F}} > \psi_{\mathrm{s}} > 0$), Q'_{s} is negative and corresponds to the depletion condition. The negative charge in the depletion region can also be calculated from Eq. (2.6). In this condition, the second term on the right-hand side of Eq. (2.6) becomes dominant. The surface charge in p-type semiconductor for depletion condition is given by

$$Q'_{\mathrm{s}} = -\sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{A}}\psi_{\mathrm{s}}}, \tag{2.11}$$

and the depletion capacitance per unit area C'_{D}, which is shown in Fig. 2.5(b) as a part of the C'_{GS} capacitance, is equal to

$$C'_{\mathrm{D}} = -\frac{\mathrm{d}Q'_{\mathrm{s}}}{d\psi_{\mathrm{s}}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{A}}}\frac{1}{2\sqrt{\psi_{\mathrm{s}}}}. \tag{2.12}$$

Therefore,

$$\frac{1}{C'_{\mathrm{gb}}} = \frac{1}{C'_{\mathrm{oxc}}} + \frac{1}{C'_{\mathrm{D}}}. \tag{2.13}$$

- Inversion condition ($V_{\mathrm{GS}} > V_{\mathrm{T}}$)

Figure 2.6(a) shows the structure of p-type semiconductor of power MOSFET, space-charge distribution $\rho(x)$, electric field strength $E(x)$, and internal potential ψ in inversion condition. The condition in which $V_{\mathrm{GS}} > V_{\mathrm{T}}$ is considered here. The surface

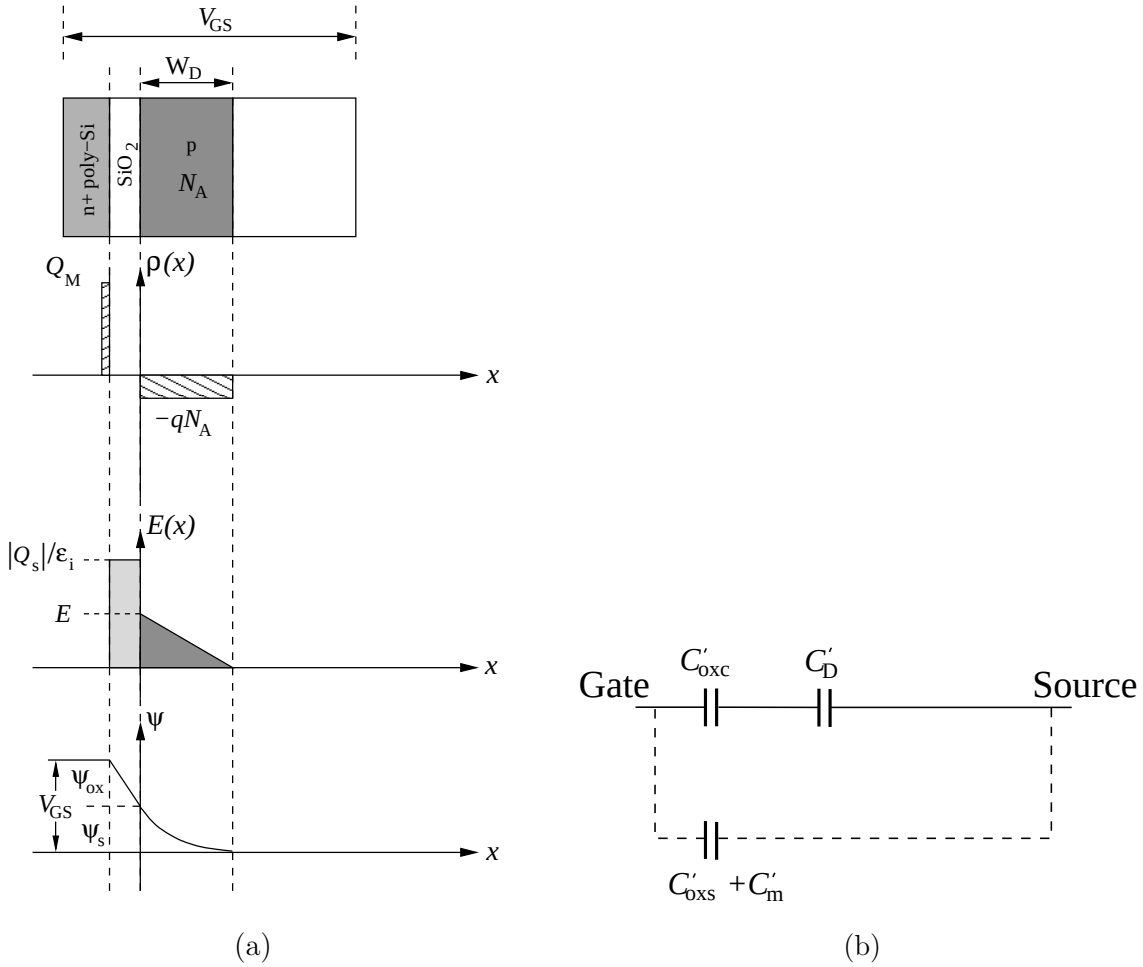


Figure 2.5 Formation of depletion layer at surface semiconductor of p-type. (a) Structure of p well of power MOSFET, space-charge distribution, electric field strength, and internal potential; (b) Equivalent capacitance C_{GS} in depletion condition.

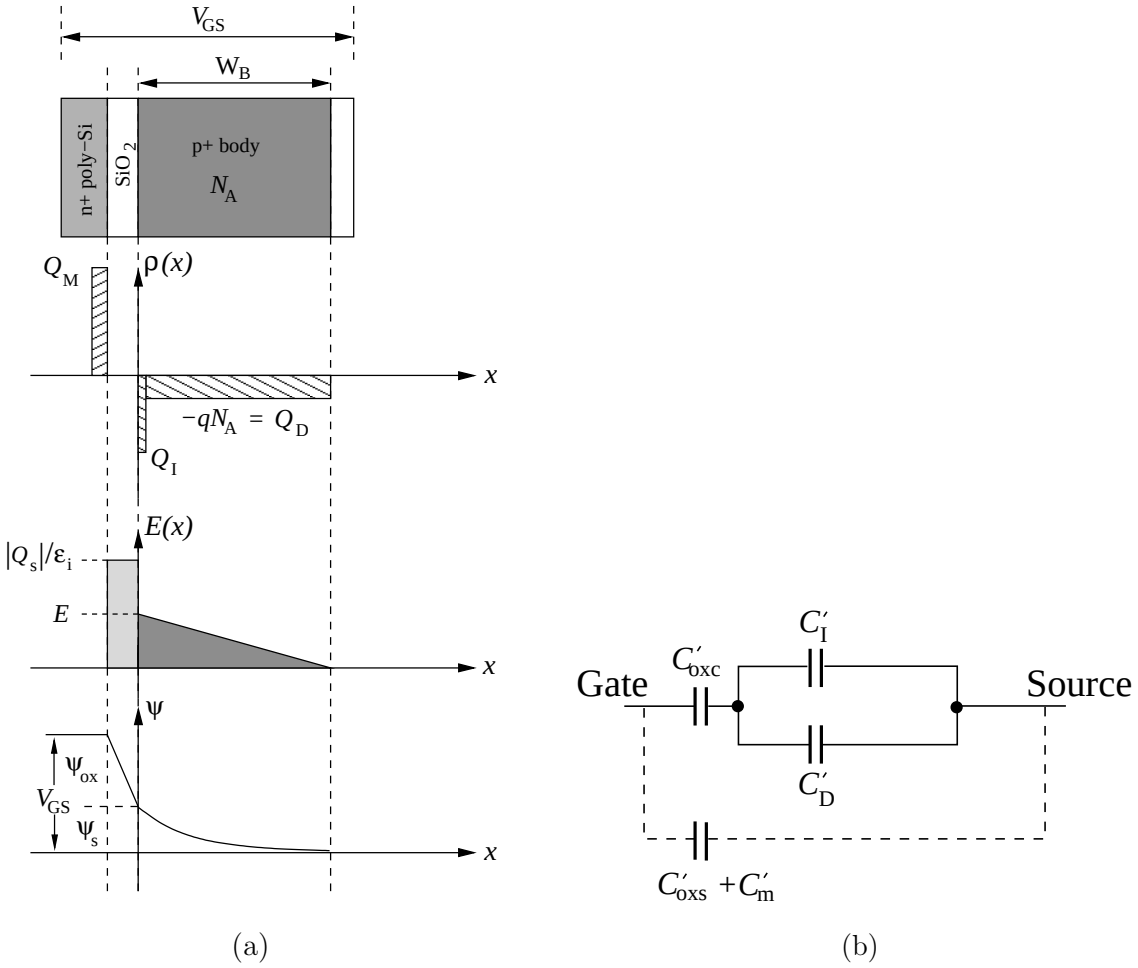
potential ψ_s being more than fermi potential ($\psi_s > \phi_F$), Q'_s is negative and corresponds to the inversion condition. The negative charge in the inversion region can also be calculated from Eq. (2.6). In this condition, the fourth term on the right-hand side of Eq. (2.6) becomes dominant. The total charge per unit area in the space-charge region Q'_s is then the sum of the charge of electron in the inversion layer Q'_I and the charge of the ionized acceptor atoms in the depletion region Q'_D. Therefore, the surface charge

in p-type semiconductor for inversion condition is given by

$$Q'_{\rm s} = Q'_{\rm D} + Q'_{\rm I} = -\sqrt{2q\epsilon_{\rm s}N_{\rm A}}\sqrt{\psi_{\rm s} + \phi_{\rm t}e^{(\psi_{\rm s}-2\phi_{\rm F})/\phi_{\rm t}}}, \tag{2.14}$$

and the inversion and depletion capacitance per unit area $C'_{\rm D} + C'_{\rm I}$, which is shown in Fig. 2.6(b) as a part of the $C'_{\rm GS}$ capacitance, is equal to

$$C'_{\rm D} + C'_{\rm I} = -\frac{{\rm d}Q'_{\rm s}}{d\psi_{\rm s}} = \sqrt{2q\epsilon_{\rm s}N_{\rm A}}\frac{1 + e^{(\psi_{\rm s}-2\phi_{\rm F})/\phi_{\rm t}}}{2\sqrt{\psi_{\rm s} + \phi_{\rm t}e^{(\psi_{\rm s}-2\phi_{\rm F})/\phi_{\rm t}}}}. \tag{2.15}$$



(a) (b)

Figure 2.6 Formation of inversion layer in p-type semiconductor. (a) Structure of p well of power MOSFET, space-charge distribution, electric field strength, and internal potential distribution; (b) Equivalent capacitance $C_{\rm GS}$ in inversion condition.

Therefore,

$$\frac{1}{C'_{\rm gb}} = \frac{1}{C'_{\rm oxc}} + \frac{1}{C'_{\rm D} + C'_{\rm I}}, \tag{2.16}$$

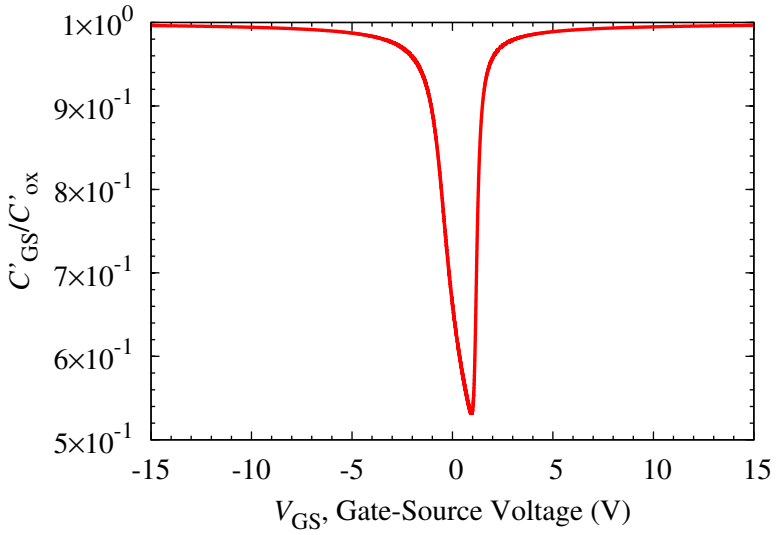


Figure 2.7 Variation of $C'_{\rm GS}/C'_{\rm ox}$ as a function of $V_{\rm GS}$ for a p-type semiconductor.

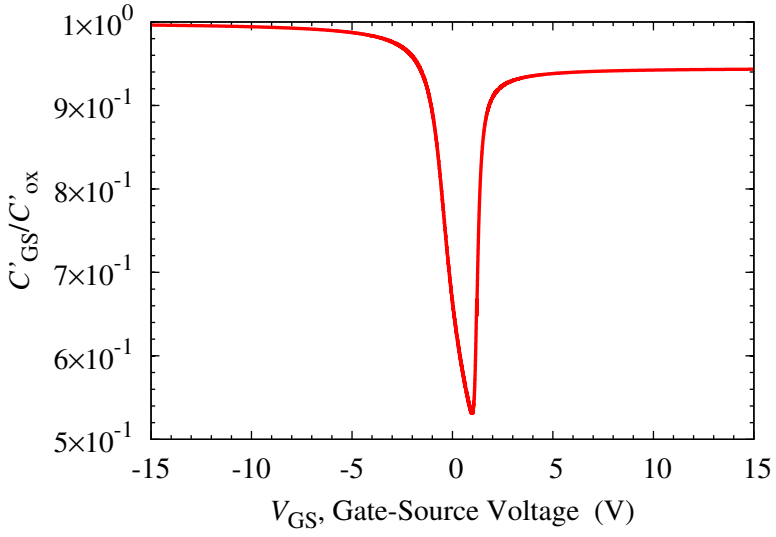


Figure 2.8 Variation of $C'_{\rm GS}/C'_{\rm ox}$ as a function of $V_{\rm GS}$ for a p-type semiconductor with considering the potential in the polygate.

Real C-V curves: Polysilicon depletion effects

Polysilicon gates have been used in MOS technologies since the seventies in order to obtain source and drain regions self-aligned to the gate [41]. When the p-semiconductor substrate is in depletion and/or inversion, the positive charge in the polygate is stored in a thin depletion layer. Thus, the capacitance of this depletion layer must be included in the MOS equivalent circuit.

Considering the potential drop in the polygate ψ_{poly}, the potential balance equation must be rewritten as

$$V_{\text{GS}} = V_{\text{FB}} + \psi_{\text{s}} + \psi_{\text{poly}} - \frac{Q'_{\text{s}}}{C'_{\text{oxc}}}. \tag{2.17}$$

$$C'_{\text{gb}} = \frac{1}{\frac{1}{C'_{\text{oxc}}} + \frac{1}{C'_{\text{c}}} + \frac{1}{C'_{\text{poly}}}}. \tag{2.18}$$

A very simple charge-control model of the capacitances is available when the semiconductor bulk is in inversion. The poly depletion capacitance per unit area C'_{poly} can be calculated as Eq. (2.19):

$$C'_{\text{poly}} = \frac{\sqrt{2q\epsilon_{\text{s}}N_{\text{poly}}}}{2\sqrt{\psi_{\text{poly}}}}, \tag{2.19}$$

and

$$\frac{\psi_{\text{poly}}}{\psi_{\text{s}}} = \frac{N_{\text{A}}}{N_{\text{poly}}}. \tag{2.20}$$

The variation of $C'_{\text{GS}}/C'_{\text{ox}}$ as a function of V_{GS} for a p-type semiconductor with considering the potential in the polygate are shown in Fig. 2.8.

Gate-Drain capacitance C_{GD} [29, 42]

The gate-drain voltage V_{GD} sweeps from a highly positive to a very low voltage, the n-drain interface starts in accumulation. Once V_{GD} drops below the drain flat-band voltage $V_{\text{FB}_{\text{D}}}$, the n-drain surface charges to depletion. Finally, when V_{GS} goes below the threshold drain voltage V_{TD}, the inversion layer starts to build up.

The surface potential ψ_{s} of n-type semiconductor obtained from the Poisson's equa-

tion:

$$\begin{aligned}\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} &= -\frac{\rho(x)}{\epsilon_\mathrm{s}} = -\frac{q}{\epsilon_\mathrm{s}}[p(x) - n(x) + N_\mathrm{D}] \\ &= -\frac{qN_\mathrm{D}}{\epsilon_\mathrm{s}}\Big[e^{2\phi_\mathrm{F}/\phi_\mathrm{t}}(e^{-\psi(x)/\phi_\mathrm{t}} - 1) - e^{\psi(x)/\phi_\mathrm{t}} + 1\Big], \end{aligned} \tag{2.21}$$

where N_D denotes the donor impurity concentration. Multiplied both sides of Eq. (2.21) by $2\mathrm{d}\psi/\mathrm{d}x$;

$$\mathrm{d}\Big(\frac{\mathrm{d}\psi}{\mathrm{d}x}\Big)^2 = -\frac{2qN_\mathrm{D}}{\epsilon_\mathrm{s}}\Big[e^{2\phi_\mathrm{F}/\phi_\mathrm{t}}(e^{-\psi(x)/\phi_\mathrm{t}} - 1) - e^{\psi(x)/\phi_\mathrm{t}} + 1\Big]\mathrm{d}\psi. \tag{2.22}$$

Integrate both sides of Eq. (2.22), the following relation is obtained:

$$\Big(\frac{\mathrm{d}\psi}{\mathrm{d}x}\Big)^2 = \frac{2qN_\mathrm{D}}{\epsilon_\mathrm{s}}\Big[\phi_\mathrm{t}e^{\psi/\phi_\mathrm{t}} - \psi - \phi_\mathrm{t} + e^{2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{-\psi/\phi_\mathrm{t}} + \psi - \phi_\mathrm{t})\Big]. \tag{2.23}$$

When $E(x) = -\mathrm{d}\psi/\mathrm{d}x$,

$$E(x) = -\frac{\mathrm{d}\psi}{\mathrm{d}x} = \pm\frac{\sqrt{2q\epsilon_\mathrm{s}N_\mathrm{D}}}{\epsilon_\mathrm{s}}\sqrt{\phi_\mathrm{t}e^{\psi/\phi_\mathrm{t}} - \psi - \phi_\mathrm{t} + e^{2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{-\psi/\phi_\mathrm{t}} + \psi - \phi_\mathrm{t})}. \tag{2.24}$$

This gives $-E_\mathrm{s} = Q'_\mathrm{s}/\epsilon_\mathrm{s}$. Evaluating E_s with $\psi = \psi_\mathrm{s}$, we obtain:

$$Q'_\mathrm{s} = \mp\sqrt{2q\epsilon_\mathrm{s}N_\mathrm{D}}\sqrt{\phi_\mathrm{t}e^{\psi_\mathrm{s}/\phi_\mathrm{t}} - \psi_\mathrm{s} - \phi_\mathrm{t} + e^{2\phi_\mathrm{F}/\phi_\mathrm{t}}(\phi_\mathrm{t}e^{-\psi_\mathrm{s}/\phi_\mathrm{t}} + \psi_\mathrm{s} - \phi_\mathrm{t})}. \tag{2.25}$$

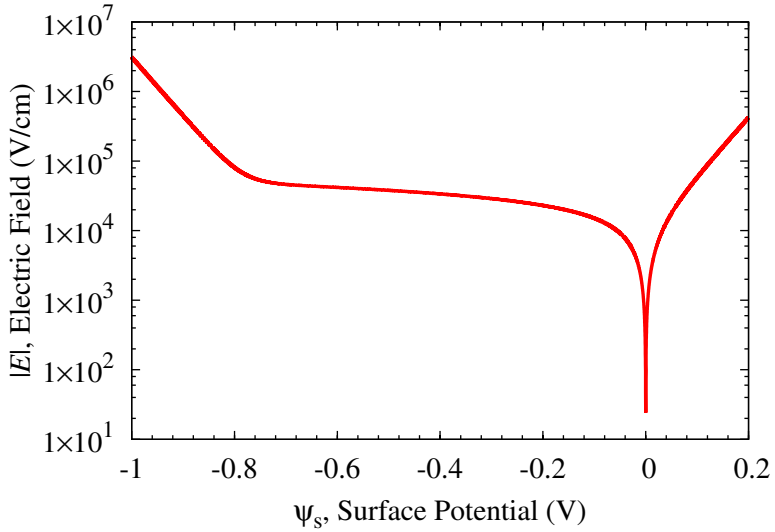


Figure 2.9 Electric field at the surface of the n-type semiconductor as a function of the surface potential across the n-type semiconductor.

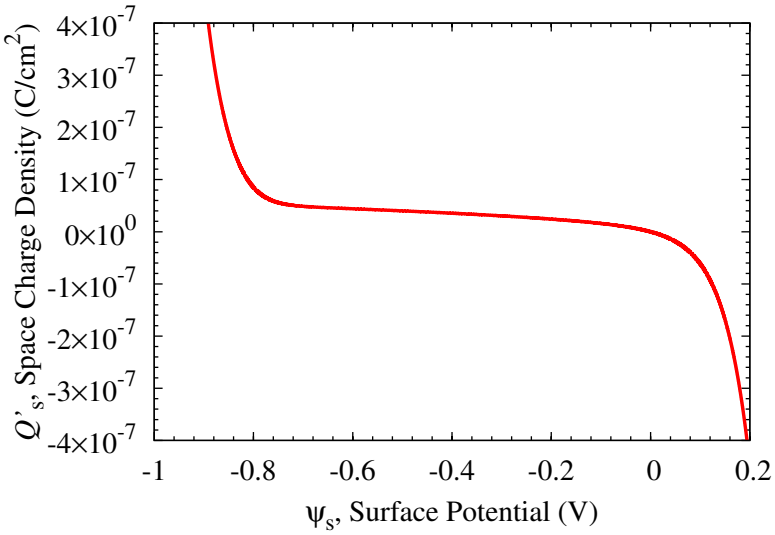


Figure 2.10 Variation of the space-charge density in n-type semiconductor of a MOS junction as a function of the surface potential.

Therefore, the C_{gdj} is derived from the space charge Q_{s}. It can be discussed as a differential capacitance per unit area of the space-charge region in n-type semiconductor, which is given by

$$C'_{\mathrm{s}} = -\frac{\mathrm{d}Q'_{\mathrm{s}}}{\mathrm{d}\psi_{\mathrm{s}}} = \pm\sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{D}}}\Big[\frac{-1+e^{\psi_{\mathrm{s}}/\phi_{\mathrm{t}}}-e^{2\phi_{\mathrm{F}}/\phi_{\mathrm{t}}}(e^{-\psi_{\mathrm{s}}/\phi_{\mathrm{t}}}-1)}{2\sqrt{\phi_{\mathrm{t}}e^{\psi_{\mathrm{s}}/\phi_{\mathrm{t}}}-\psi_{\mathrm{s}}-\phi_{\mathrm{t}}+e^{2\phi_{\mathrm{F}}/\phi_{\mathrm{t}}}(\phi_{\mathrm{t}}e^{-\psi_{\mathrm{s}}/\phi_{\mathrm{t}}}+\psi_{\mathrm{s}}-\phi_{\mathrm{t}})}}\Big]. \tag{2.26}$$

Eqs. (2.25) and (2.26) are validated in all conditions (accumulation, depletion, and inversion).

- Accumulation condition ($V_{\mathrm{GD}} > V_{\mathrm{FB_D}}$)

Figure 2.11(a) shows the structure of n^- drift region of power MOSFET, space-charge distribution $\rho(x)$, electric field strength $E(x)$, and internal potential ψ in accumulation condition. The condition in which $V_{\mathrm{GD}} > V_{\mathrm{FB_D}}$ is considered in this section. The surface potential ψ_{s} being more than zero ($\psi_{\mathrm{s}} > 0$), Q'_{s} is negative and corresponds to the accumulation condition that varies exponentially with the surface potential because the first term on the right-hand side of Eq. (2.25) becomes dominant. The surface charge in n-type semiconductor for accumulation condition is given by

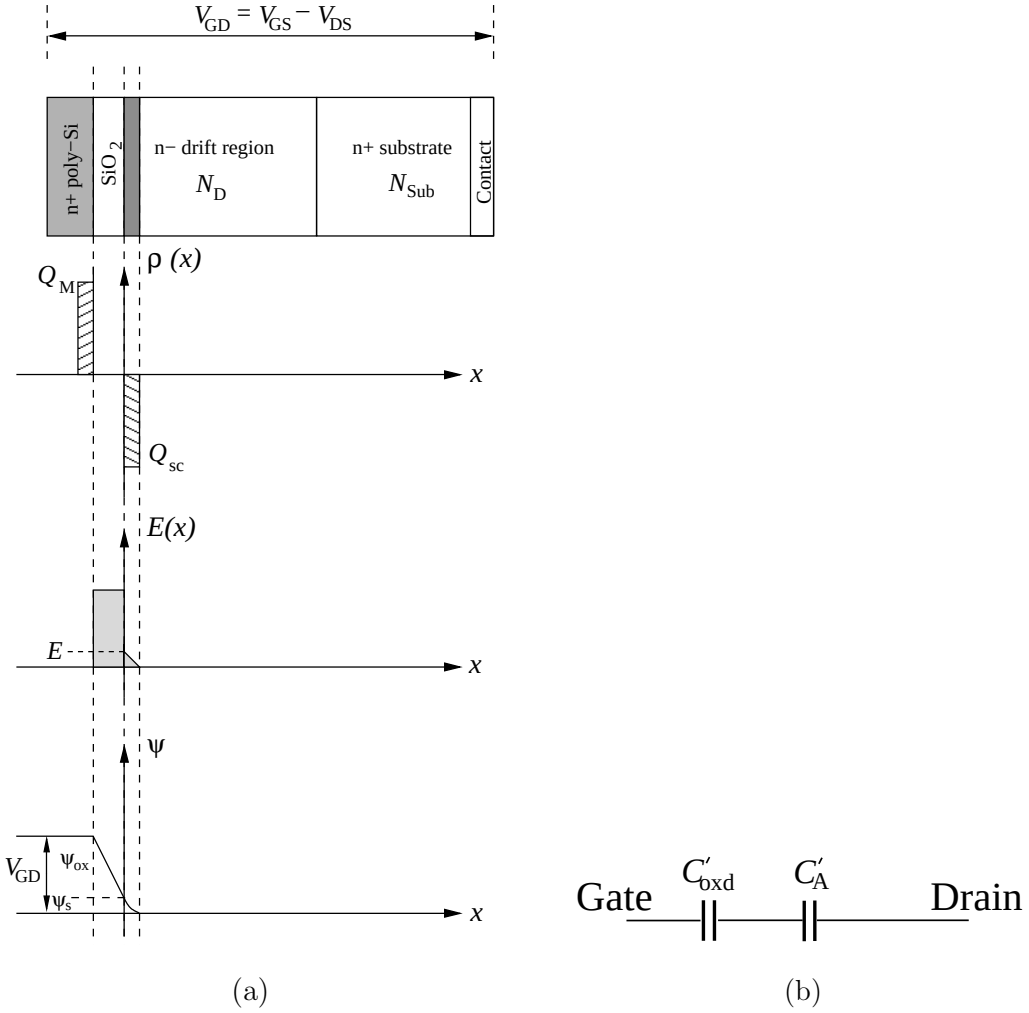


Figure 2.11 Formation of accumulation layer in n-type semiconductor. (a) Structure of n^- drift region of power MOSFET, space-charge distribution, electric field strength, and internal potential; (b) Equivalent capacitance C_{GD} in accumulation condition.

$$Q'_s = -\sqrt{2q\epsilon_s N_D}\sqrt{\phi_t e^{\psi_s/\phi_t}}, \tag{2.27}$$

and the accumulation capacitance per unit area C'_A is equal to

$$C'_A = -\frac{dQ'_s}{d\psi_s} = \sqrt{2q\epsilon_s N_D}\frac{e^{\psi_s/\phi_t}}{2\sqrt{\phi_t e^{\psi_s/\phi_t}}}. \tag{2.28}$$

Therefore,

$$\frac{1}{C'_{GD}} = \frac{1}{C'_{oxd}} + \frac{1}{C'_A}, \tag{2.29}$$

where C'_{GD} is the gate-drain capacitance per unit area and C'_{oxd} the gate-drain oxide capacitance per unit area. The gate voltage dependency of C'_{GD} capacitance in the accumulation condition is shown in Fig. 2.11(b).

- Depletion condition ($V_{\mathrm{FB_D}} > V_{\mathrm{GD}} > V_{\mathrm{TD}}$)

Figure 2.12(a) shows the structure of n^- drift region of power MOSFET, space-charge distribution $\rho(x)$, electric field strength $E(x)$, and internal potential ψ. The condition

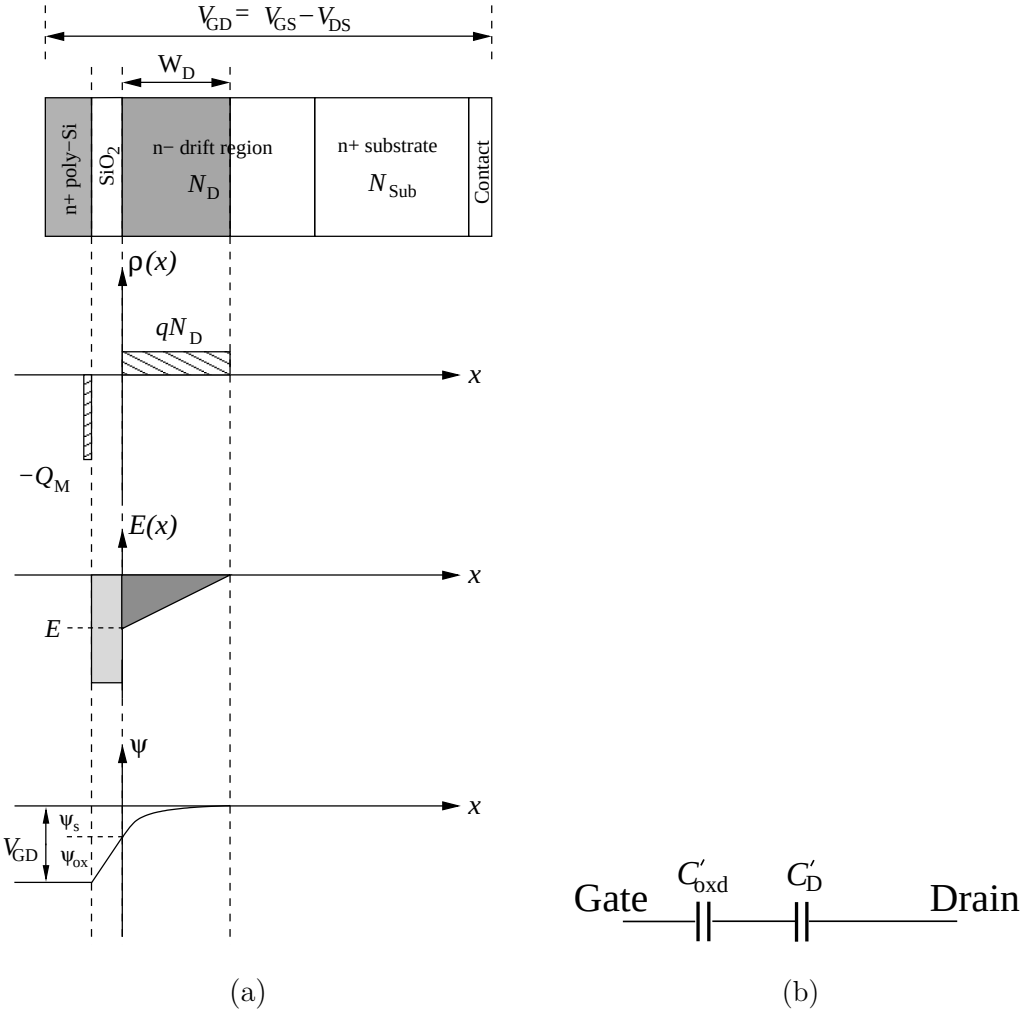


Figure 2.12 Formation of depletion layer at surface semiconductor of n-type. (a) Structure of n^- drift region of power MOSFET, space-charge distribution, electric field strength, and internal potential; (b) Equivalent capacitance C_{GD} in depletion condition.

in which $V_{\mathrm{FB_D}} > V_{\mathrm{GD}} > V_{\mathrm{TD}}$ is considered here. When the surface potential ψ_{s} is less than zero ($0 > \psi_{\mathrm{s}} > \phi_{\mathrm{F}}$), Q'_{s} is positive and corresponds to the depletion condition. The positive charge in the depletion region can also be calculated from Eq. (2.25). In this condition, the second term on the right-hand side of Eq. (2.25) becomes dominant. The surface charge in n-type semiconductor for depletion condition is given by

$$Q'_{\mathrm{s}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{D}}|\psi_{\mathrm{s}}|}, \tag{2.30}$$

and the depletion capacitance per unit area C'_{D} is equal to

$$C'_{\mathrm{D}} = -\frac{\mathrm{d}Q'_{\mathrm{s}}}{\mathrm{d}\psi_{\mathrm{s}}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{D}}}\frac{1}{2\sqrt{|\psi_{\mathrm{s}}|}}. \tag{2.31}$$

Therefore,

$$\frac{1}{C'_{\mathrm{GD}}} = \frac{1}{C'_{\mathrm{oxd}}} + \frac{1}{C'_{\mathrm{D}}}. \tag{2.32}$$

The gate voltage dependency of C'_{GD} capacitance in the depletion condition is shown in Fig. 2.12(b).

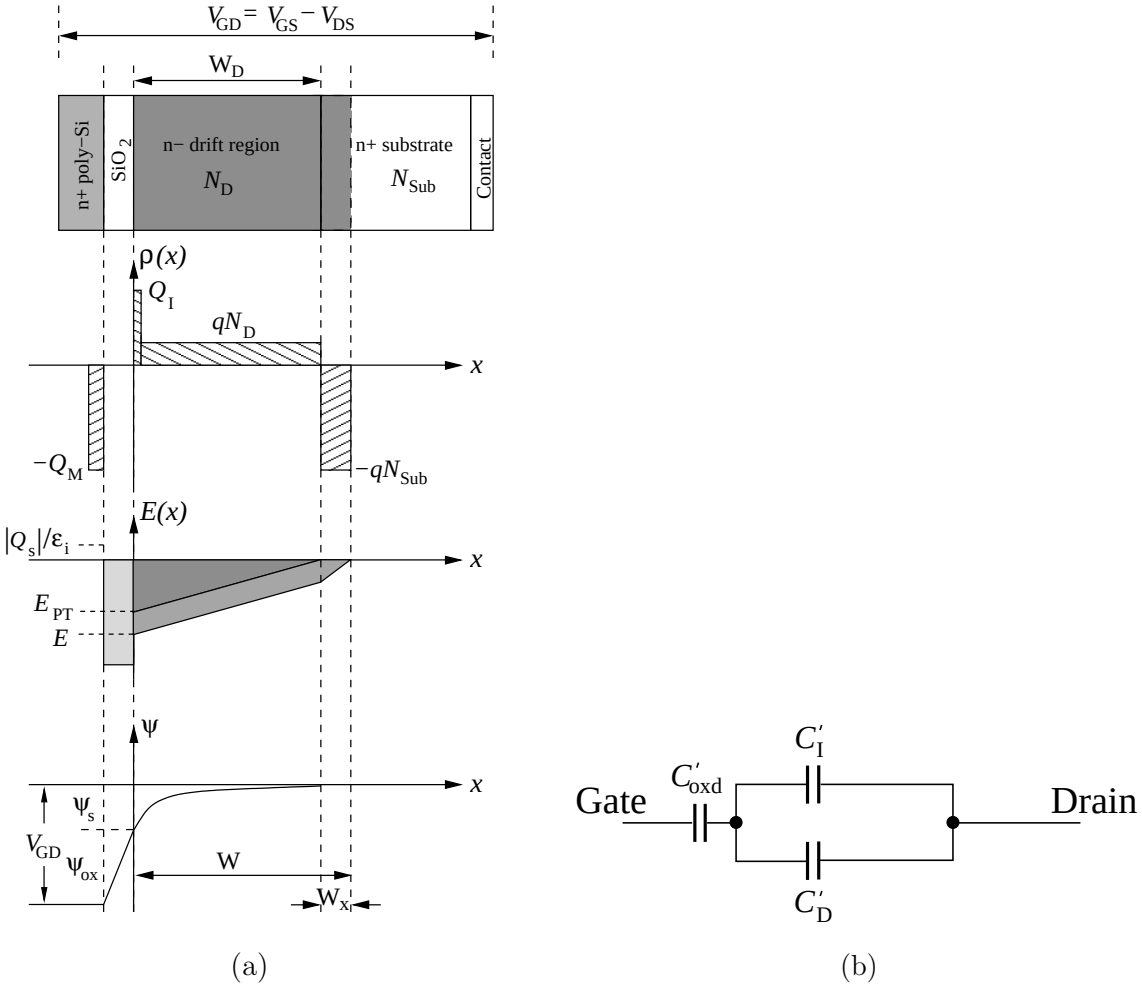
- Inversion condition ($V_{\mathrm{GD}} < V_{\mathrm{TD}}$)

Figure 2.13(a) shows the structure of n^- drift region of power MOSFET, space-charge distribution $\rho(x)$, electric field strength $E(x)$, and internal potential ψ in inversion condition. The condition in which $V_{\mathrm{GD}} < V_{\mathrm{TD}}$ is considered here. When the surface potential ψ_{s} is less than fermi potential ($\psi_{\mathrm{s}} < \phi_{\mathrm{F}}$), Q'_{s} is positive and corresponds to the inversion condition. The positive charge in the inversion region can also be calculated from Eq. (2.25). In this condition, the fourth term on the right-hand side of Eq. (2.25) becomes dominant. The total charge per unit area in the space-charge region Q'_{s} is then the sum of the charge of electron in the inversion layer Q'_{I} and the charge of the ionized acceptor atoms in the depletion region Q'_{D}. Therefore, the surface charge in n-type semiconductor for inversion condition is given by

$$Q'_{\mathrm{s}} = Q'_{\mathrm{D}} + Q'_{\mathrm{I}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{D}}}\sqrt{|\psi_{\mathrm{s}}| + \phi_{\mathrm{t}}e^{|(2\phi_{\mathrm{F}}-\psi_{\mathrm{s}})|/\phi_{\mathrm{t}}}}, \tag{2.33}$$

and the inversion and depletion capacitance per unit area $C'_{\mathrm{D}} + C'_{\mathrm{I}}$ is equal to

$$C'_{\mathrm{D}} + C'_{\mathrm{I}} = -\frac{\mathrm{d}Q'_{\mathrm{s}}}{\mathrm{d}\psi_{\mathrm{s}}} = \sqrt{2q\epsilon_{\mathrm{s}}N_{\mathrm{D}}}\frac{1 + e^{|(2\phi_{\mathrm{F}}-\psi_{\mathrm{s}})|/\phi_{\mathrm{t}}}}{2\sqrt{|\psi_{\mathrm{s}}| + \phi_{\mathrm{t}}e^{|(2\phi_{\mathrm{F}}-\psi_{\mathrm{s}})|/\phi_{\mathrm{t}}}}}. \tag{2.34}$$



(a) (b)

Figure 2.13 Formation of inversion layer in n-type semiconductor. (a) Structure of n^- drift region of power MOSFET, space-charge distribution, electric field strength, and internal potential; (b) Equivalent capacitance C_{GD} in inversion condition.

Therefore,

$$\frac{1}{C'_{GD}} = \frac{1}{C'_{oxd}} + \frac{1}{C'_D + C'_I}. \tag{2.35}$$

The gate voltage dependency of C'_{GD} capacitance in the inversion condition is shown in Fig. 2.13(b).

The n^- drift region of power MOSFET is divided into two regions: the space charge region and the ohmic region. The C_{GD} is the combination of the gate-drain

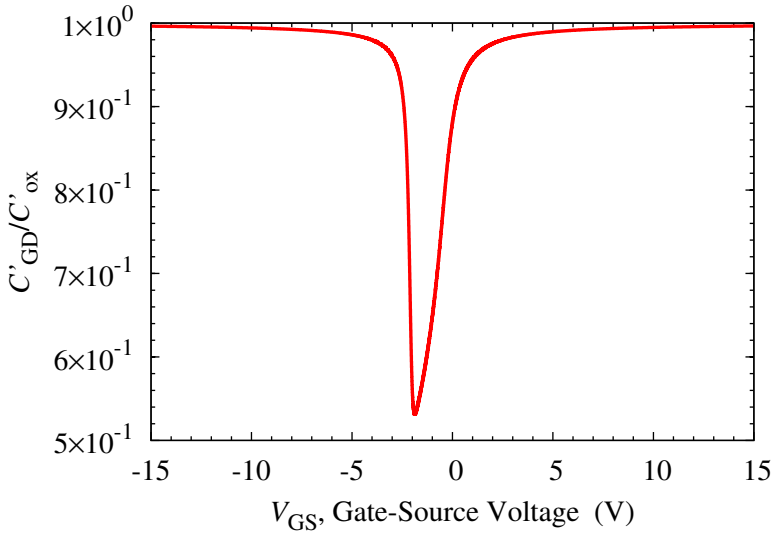


Figure 2.14 Variation of $C'_{\mathrm{GD}}/C'_{\mathrm{ox}}$ as a function of V_{GS} for a n-type semiconductor.

oxide capacitance C_{oxd} and the drain depletion layer beneath the gate oxide capacitance C_{gdj}, which is shown in Fig. 2.1. For approximate calculations of switching behaviors, C_{GD} is approximated by the two discrete values C_{oxd} and C_{gdj} with the change in value occurring at $V_{\mathrm{DS}} = V_{\mathrm{GS}}$ as Eq. (2.36):

$$C_{\mathrm{GD}} \cong \begin{cases} C_{\mathrm{oxd}} & \text{for } V_{\mathrm{DS}} \leq V_{\mathrm{GS}} - V_{\mathrm{TD}}, \\ C_{\mathrm{oxd}} \cdot C_{\mathrm{gdj}}/(C_{\mathrm{oxd}} + C_{\mathrm{gdj}}) & \text{for } V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{TD}}. \end{cases} \tag{2.36}$$

The C_{gdj} can be discussed as the C_{DS} in the next section.

Drain-Source capacitance C_{DS} [29, 32]

Figure 2.15(a) shows the structure of $\mathrm{p^+}$-$\mathrm{n^-}$-$\mathrm{n^+}$ of power MOSFET, space-charge distribution $\rho(x)$, and electric field distribution $E(x)$. The drain-source capacitance C_{DS} corresponds to the junction capacitance stemmed by depletion at the junction between the p well and the $\mathrm{n^-}$-epitaxial layer C_{dsj}. It largely depends on V_{DS}. Here, C_{DS} can be considered as $\mathrm{p^+}$-$\mathrm{n^-}$-$\mathrm{n^+}$ structure shown in Fig. 2.15. It is supported the punch-through structure at high breakdown voltage. When V_{DS} increases, the depletion region expands from the $\mathrm{p^+}$ to the uniformly doped drift region $\mathrm{n^-}$ and $\mathrm{n^+}$ substrate. Therefore, the depletion region will appreciably simplify the solution

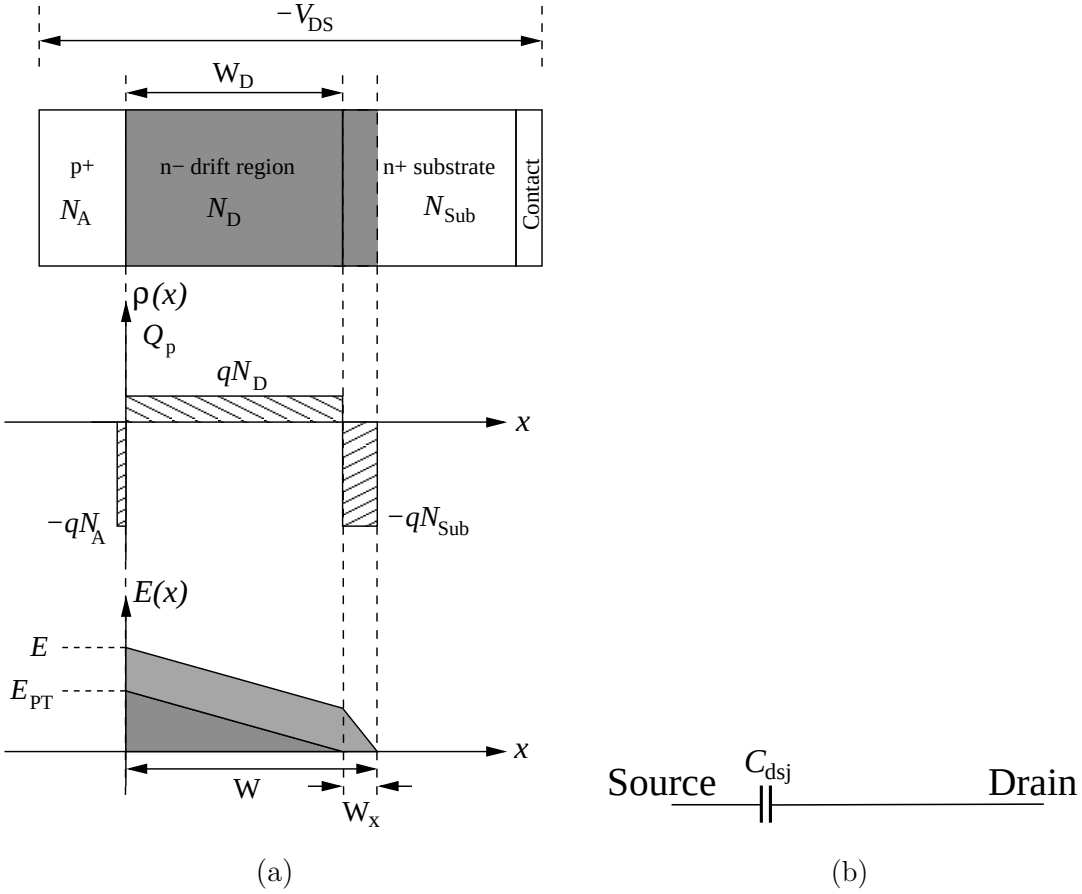


Figure 2.15 p^+-n^--n^+ junction under reverse bias voltage. (a) Structure of p^+-n^--n^+ of power MOSFET, space-charge distribution, and electric field strength; (b) Equivalent capacitance C_{DS}.

of Poisson's equation. Since the carrier concentrations are assumed to be much less than the net ionized dopant density in the depletion region. Poisson's equation can be written as

$$\frac{\mathrm{d}^2V(x)}{\mathrm{d}x^2} \cong \begin{cases} -\dfrac{qN_D}{\epsilon_s} & \text{for } 0 \le x \le W_D, \\ -\dfrac{qN_{Sub}}{\epsilon_s} & \text{for } W_D < x, \end{cases} \tag{2.37}$$

where N_D denotes the donor impurity concentration in n^--drift region, N_{Sub} the donor impurity concentration in n^+-substrate layer, and W_D the drift region width. When both sides of Eq. (2.37) are integrated in the depletion region from $x = 0$ to $x = W$,

the following is obtained in the differential equation by

$$\frac{\mathrm{d}V(W)}{\mathrm{d}W} = \begin{cases} -\dfrac{qN_{\mathrm{D}}}{\epsilon_{\mathrm{s}}}W & \text{for } 0 \leq W \leq W_{\mathrm{D}}, \\ -\dfrac{qN_{\mathrm{Sub}}}{\epsilon_{\mathrm{s}}}W & \text{for } W > W_{\mathrm{D}}. \end{cases} \tag{2.38}$$

From Eq. (2.38), depletion region width W can be expressed with voltage V and V_{bi} in Eq. (2.39):

$$W = \begin{cases} \sqrt{\dfrac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{D}}}(-V + V_{\mathrm{bi}})} & \text{for } 0 \leq W \leq W_{\mathrm{D}}, \\ \sqrt{\dfrac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{D}}}(-V + V_{\mathrm{bi}}) + \left(1 - \dfrac{N_{\mathrm{D}}}{N_{\mathrm{Sub}}}\right)W_{\mathrm{D}}^2} & \text{for } W > W_{\mathrm{D}}. \end{cases} \tag{2.39}$$

The depletion region capacitance can be related to the applied reverse-bias voltage V_{R} through depletion region width W:

$$C = A\frac{\epsilon_{\mathrm{s}}}{W} \tag{2.40}$$

Therefore, the drain-source capacitance C_{DS} can be expressed with applying V_{DS} by Eq. (2.41):

$$C_{\mathrm{DS}} = \begin{cases} A_{\mathrm{DS}}\dfrac{\epsilon_{\mathrm{s}}}{\sqrt{\frac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{D}}}(V_{\mathrm{DS}} + V_{\mathrm{bi}})}} & \text{for } 0 \leq W \leq W_{\mathrm{D}}, \\ A_{\mathrm{DS}}\dfrac{\epsilon_{\mathrm{s}}}{\sqrt{\frac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{D}}}(V_{\mathrm{DS}} + V_{\mathrm{bi}}) + \left(1 - \frac{N_{\mathrm{D}}}{N_{\mathrm{Sub}}}\right)W_{\mathrm{D}}^2}} & \text{for } W > W_{\mathrm{D}}, \end{cases} \tag{2.41}$$

where A_{DS} denotes the drain-source overlap area. And also, the drain depletion layer beneath the gate oxide capacitance C_{gdj} can be expressed with applying $V_{\mathrm{DG}}(= V_{\mathrm{DS}} - V_{\mathrm{GS}})$ and $V_{\mathrm{bi}} = V_{\mathrm{TD}}$ by Eq. (2.42):

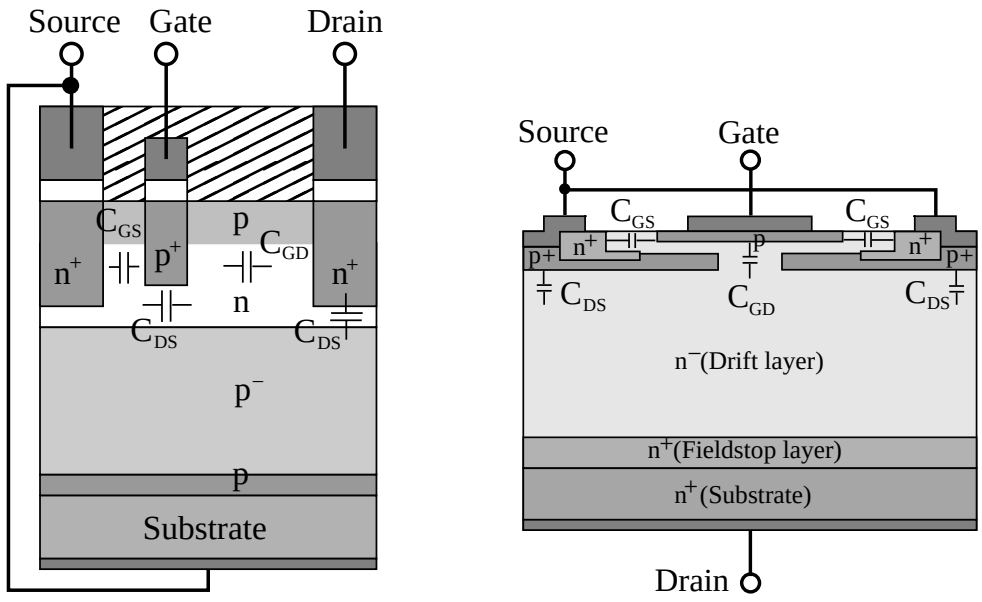
$$C_{\mathrm{gdj}} = \begin{cases} A_{\mathrm{GD}}\dfrac{\epsilon_{\mathrm{s}}}{\sqrt{\frac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{D}}}(V_{\mathrm{DS}} - V_{\mathrm{GS}} + V_{\mathrm{TD}})}} & \text{for } 0 \leq W \leq W_{\mathrm{D}}, \\ A_{\mathrm{GD}}\dfrac{\epsilon_{\mathrm{s}}}{\sqrt{\frac{2\epsilon_{\mathrm{s}}}{qN_{\mathrm{D}}}(V_{\mathrm{DS}} - V_{\mathrm{GS}} + V_{\mathrm{TD}}) + \left(1 - \frac{N_{\mathrm{D}}}{N_{\mathrm{Sub}}}\right)W_{\mathrm{D}}^2}} & \text{for } W > W_{\mathrm{D}}, \end{cases} \tag{2.42}$$

where A_{GD} denotes the gate-drain overlap area.

2.3 Device structure and internal parasitic capacitances of SiC JFET

2.3.1 Device structure of SiC JFET

Figure 2.16(a) shows the cross section of the lateral-type SiC JFET cell. The n-channel is formed between buried p^+ gate and p^- substrate. Their separation determines the n-channel thickness. The n-region between drain and source areas is designed to have a double reduced surface field (RESURF) effect to prevent electric field concentration [21]. Figure 2.16(b) shows the cross section of the vertical-type SiC JFET cell [60, 66]. It has lateral and vertical channels. The lateral channel is sandwiched between p gate at the center top of the device and buried p^+ gate sections connected to the source terminal at the top of the drift region. The vertical channel is located between the two buried p^+ gate regions.



(a) Lateral-type (b) Vertical-type

Figure 2.16 Cross section of a SiC JFET cell.

2.3.2 Internal parasitic capacitances of SiC JFET

The depletion region formed at pn junction behaves as internal parasitic capacitances, which are lumped into terminal capacitances C_{GS}, C_{GD}, and C_{DS}, as depicted in Fig. 2.16. The capacitances of pn junction depend on the doping profile, device structure, and reverse-bias voltage V_{R}. In practice, most impurity concentration profiles can be approximated by the following two limiting cases: the uniformly doped junction and the linearly graded doped junction [29, 32, 65]. The uniformly doped approximation provides an adequate description for alloyed junctions, shallowly diffused junctions, and ion-implanted junctions. The linearly graded doped approximation is reasonable for deeply diffused junctions. Therefore, the Poisson's equation is valid for the both approximation.

Uniformly doped junction capacitance

A pn junction is considered uniformly doped or abrupt if there dominates donor impurity concentration N_{D} on one side of the junction and acceptor impurity concentration N_{A} on the other side. Here, the impurity concentration in a semiconductor changes abruptly from N_{A} to N_{D}, as shown in Fig. 2.17. The charge density ρ around the pn junction is graphically shown in Fig. 2.17, which can be separated into four parts. Therefore, the relationship between the electric field E and the charge density ρ is given by the Poisson's equation as Eq. (2.43):

$$\frac{\mathrm{d}^2V(x)}{\mathrm{d}x^2} \cong \begin{cases} 0 & \text{for } x \leq -x_{\mathrm{p}}, \\ \dfrac{qN_{\mathrm{A}}}{\epsilon_{\mathrm{s}}} & \text{for } -x_{\mathrm{p}} \leq x < 0, \\ -\dfrac{qN_{\mathrm{D}}}{\epsilon_{\mathrm{s}}} & \text{for } 0 < x \leq x_{\mathrm{n}}, \\ 0 & \text{for } x \geq x_{\mathrm{n}}. \end{cases} \tag{2.43}$$

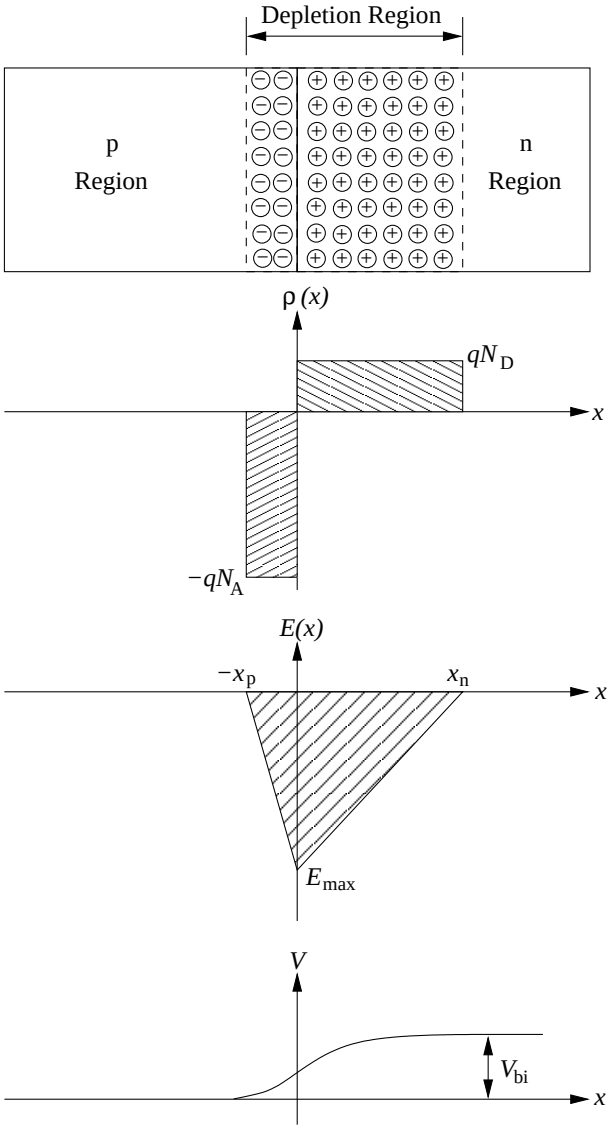


Figure 2.17 Uniformly doped pn junction in thermal equilibrium.

The electric field E is then obtained by integrating Eq. (2.43) on x:

$$-\frac{\mathrm{d}V(x)}{\mathrm{d}x} = E(x) = \begin{cases} 0 & \text{for } x \le -x_\mathrm{p}, \\ -\dfrac{qN_\mathrm{A}}{\epsilon_\mathrm{s}}(x + x_\mathrm{p}) & \text{for } -x_\mathrm{p} \le x < 0, \\ \dfrac{qN_\mathrm{D}}{\epsilon_\mathrm{s}}(x - x_\mathrm{n}) & \text{for } 0 < x \le x_\mathrm{n}, \\ 0 & \text{for } x \ge x_\mathrm{n}. \end{cases} \tag{2.44}$$

The integration of Eq. (2.44) gives the potential distribution $V(x)$ as:

$$V(x) = \begin{cases} 0 & \text{for } x \leq -x_{\mathrm{p}}, \\ \dfrac{qN_{\mathrm{A}}}{2\epsilon_{\mathrm{s}}}(x + x_{\mathrm{p}})^2 & \text{for } -x_{\mathrm{p}} \leq x < 0, \\ V_{\mathrm{bi}} - \dfrac{qN_{\mathrm{D}}}{2\epsilon_{\mathrm{s}}}(x - x_{\mathrm{n}})^2 & \text{for } 0 < x \leq x_{\mathrm{n}}, \\ V_{\mathrm{bi}} & \text{for } x \geq x_{\mathrm{n}}. \end{cases} \tag{2.45}$$

At the condition $E(0) = N_{\mathrm{D}}x_{\mathrm{n}} = N_{\mathrm{A}}x_{\mathrm{p}}$, x_{p} and x_{n} are obtained as

$$x_{\mathrm{p}} = \sqrt{\frac{2\epsilon_{\mathrm{s}}V_{\mathrm{bi}}}{qN_{\mathrm{A}}[1 + (N_{\mathrm{A}}/N_{\mathrm{D}})]}}, \tag{2.46}$$

$$x_{\mathrm{n}} = \sqrt{\frac{2\epsilon_{\mathrm{s}}V_{\mathrm{bi}}}{qN_{\mathrm{D}}[1 + (N_{\mathrm{D}}/N_{\mathrm{A}})]}}. \tag{2.47}$$

The total depletion region width W is obviously given by

$$W = x_{\mathrm{p}} + x_{\mathrm{n}} = \sqrt{\frac{2\epsilon_{\mathrm{s}}}{q}\Big(\frac{N_{\mathrm{A}} + N_{\mathrm{D}}}{N_{\mathrm{A}}N_{\mathrm{D}}}\Big)V_{\mathrm{bi}}}. \tag{2.48}$$

In Eq. (2.48), $V_{\mathrm{bi}} + V_{\mathrm{R}}$ will appear instead of V_{bi}:

$$W = \sqrt{\frac{2\epsilon_{\mathrm{s}}}{q}\Big(\frac{N_{\mathrm{A}} + N_{\mathrm{D}}}{N_{\mathrm{A}}N_{\mathrm{D}}}\Big)(V_{\mathrm{bi}} + V_{\mathrm{R}})}. \tag{2.49}$$

The depletion region capacitance is related to the applied reverse-bias voltage V_{R} through depletion region width W as Eq. (2.40), so that the depletion region capacitance can be expressed in the following compact form:

$$C = C_0\Big(1 + \frac{V_{\mathrm{R}}}{V_{\mathrm{bi}}}\Big)^{-1/2}, \tag{2.50}$$

where C_0 is

$$C_0 = \begin{cases} \dfrac{A}{2}\sqrt{\dfrac{2\epsilon_{\mathrm{s}}N_{\mathrm{A}}}{V_{\mathrm{bi}}}} & \text{for } N_{\mathrm{D}} >> N_{\mathrm{A}}, \\ \dfrac{A}{2}\sqrt{\dfrac{2\epsilon_{\mathrm{s}}N_{\mathrm{D}}}{V_{\mathrm{bi}}}} & \text{for } N_{\mathrm{A}} >> N_{\mathrm{D}}. \end{cases} \tag{2.51}$$

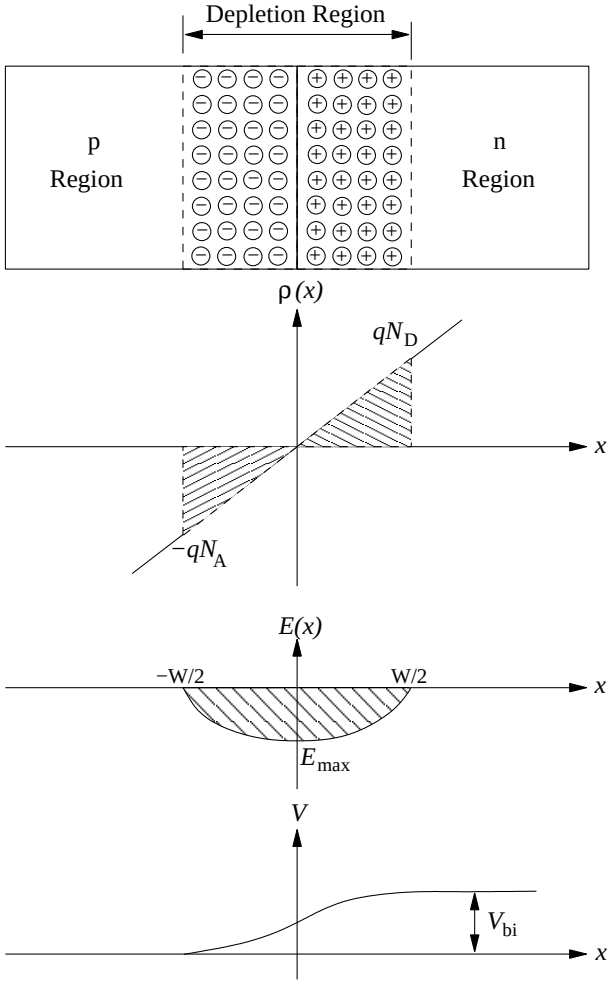


Figure 2.18 Linearly graded doped pn junction in thermal equilibrium.

Linearly graded doped junction capacitance

A pn junction is considered linearly graded doped, where the charge density ρ changes from the most negative value to the most positive value in the smoothest possible way, which is shown in Fig. 2.18. Therefore, the relationship between the electric field E and the charge density ρ is governed by the Poisson's equation as Eq. (2.52):

$$\frac{\mathrm{d}^2V(x)}{\mathrm{d}x^2} = -\frac{\rho}{\epsilon_\mathrm{s}} = \frac{qax}{\epsilon_\mathrm{s}}, \qquad \text{for } -W/2 \leq x \leq W/2, \tag{2.52}$$

where a denotes the slope of the linear dependence, which depends on the doping concentration. The electric field E is then obtained by integrating Eq. (2.52):

$$-\frac{\mathrm{d}V(x)}{\mathrm{d}x} = E(x) = -\frac{qa}{\epsilon_\mathrm{s}}\frac{(W/2)^2 - x^2}{2}, \qquad \text{for } -W/2 \leq x \leq W/2. \tag{2.53}$$

The potential distribution $V(x)$ is obtained by integrating the Eq. (2.53):

$$V(x) = \frac{qa}{2\epsilon_\mathrm{s}}\Big[\frac{x^3}{3} - \big(\frac{W}{2}\big)^2 x + \frac{W^3}{12}\Big]. \tag{2.54}$$

The built-in potential V_bi is given by

$$V_\mathrm{bi} = \frac{qaW^3}{12\epsilon_\mathrm{s}}. \tag{2.55}$$

The depletion region width W is obtained from Eq. (2.55) as

$$W = \Big(\frac{12\epsilon_\mathrm{s}V_\mathrm{bi}}{qa}\Big)^{1/3}. \tag{2.56}$$

The depletion region capacitance can be related to the applied reverse-bias voltage V_R through depletion region width W as Eq. (2.40). Therefore, the depletion region capacitance can be expressed in the following compact form:

$$C = C_0\Big(1 + \frac{V_\mathrm{R}}{V_\mathrm{bi}}\Big)^{-1/3}, \tag{2.57}$$

where C_0 is

$$C_0 = A\Big(\frac{qa\epsilon_\mathrm{s}^2}{12V_\mathrm{bi}}\Big)^{1/3}. \tag{2.58}$$

Eventually, the depletion capacitance depending on the applied reverse-bias voltage V_R can be expressed in the following compact form:

$$C = C_0\Big(1 + \frac{V_\mathrm{R}}{V_\mathrm{bi}}\Big)^{-m}, \tag{2.59}$$

where C_0 denotes the zero-bias capacitance, V_bi the built-in potential barrier, and m the junction grading coefficient. In addition, $m = 1/2$ is for the uniformly doped and $m = 1/3$ for the linearly graded doped.

2.4 Summary

This chapter illustrated the cross section of a SiC power MOSFET cell, a lateral-type SiC JFET cell, and a vertical-type SiC JFET cell. This chapter also described the two most commonly used types of capacitances, which are the MOS capacitance and pn junction capacitance. Their device structures decide the voltage dependence of the capacitance characteristics. The voltage dependence of the MOS capacitance is distinguished as accumulation, depletion, and inversion conditions. The voltage dependence of the pn junction capacitance is expressed as the uniformly doped and the linearly graded doped junctions. The capacitances of the SiC power MOSFET and SiC JFETs including the internal parasitic capacitances will be measured by the capacitance measurement system, which is explained in Chapter 3. The measured capacitances of the SiC power MOSFET and SiC JFETs will be also shown and discussed in Chapter 4 and Chapter 5, respectively.

Chapter 3

Measurement of terminal capacitances and its voltage dependency for high-voltage power transistors

3.1 Introduction

Power electronics require high efficiency and versatile power conversion. High-voltage capability is preferable, especially in high-power circuits, to reduce the conduction loss of large currents. High-frequency switching enables minimization of bulky passive components and provides control functionality. Power switching devices are the key components to realize for power electronics. Therefore, it is strongly focused on a developing power device with a high breakdown voltage, low forward voltage drop, and fast switching capability [3, 7, 22, 23].

It is well known that an Si-insulated gate bipolar transistor (IGBT) has been developed and improved to meet these requirements [45, 46]. Recently, a superjunction structure of Si power MOSFET was proposed to realize a high breakdown voltage using a pn junction and fast switching capability by majority carriers [47–49]. In addition to the Si-based power device, wide band gap semiconductor power devices

have been researched and developed to achieve lower loss, higher voltage breakdown, and faster switching with a thin voltage blocking layer. SiC and GaN devices are good examples [1, 3, 9, 11, 16, 31, 48, 50–57].

The terminal capacitances of a power device affect its switching behavior, because it must be charged and discharged during turn-off and turn-on operations [33,34]. The capacitances of a power device increase as the thickness of the voltage blocking layer is decreased to minimize conduction resistance. The capacitances vary widely with the applied bias voltage because of depletion in the voltage blocking layer. Therefore, it is necessary to quantify the terminal capacitances of the power device as well as the voltage dependency of capacitance. One method is to estimate the capacitance value with finite-element (FE) device simulation and validate it with circuit simulation or experiments [37, 58]. However, this approach requires physical parameters a detailed device structure, dimensions, and process parameters. Another method is to characterize the capacitances experimentally. However, there is no commercial product that is able to measure the terminal capacitances of a high-voltage power device by applying the bias voltage up to its rated value. JEDEC [35] and IEC [36] standardized the capacitance measurement between the terminals of a power device with a capacitance bridge, but no actual configuration or circuit topology for the measurements are provided. Elferich *et al.* [37] measured the C-V characteristics of a power MOSFET and validated the FE device simulation; however, the measurement setup is not clearly described and the applied voltage was low ($0\ \mathrm{V} \leq V_{\mathrm{DS}} \leq 20\ \mathrm{V}, -10\ \mathrm{V} \leq V_{\mathrm{GS}} \leq 0\ \mathrm{V}$). Therefore, we developed a C-V measurement system for high-voltage power devices. Funaki *et al.* [38, 39] presented the C-V measurement system for high-voltage power diodes with evolving [40] and clarified the punch-through structure of SiC Schottky barrier diodes (SBDs) from the measured results. This study develops a C-V measurement system for gate-controlled, high-voltage power devices, e.g., power MOSFET, JFET, and IGBT. There are three terminals in a single device, and five specifications of the measurement circuit are presented to measure the capacitance between gate-source (C_{GS}), gate-drain (C_{GD}), and drain-source (C_{DS}), and to measure input (C_{ISS}), output (C_{OSS}), and reverse transfer ($C_{\mathrm{RSS}} = C_{\mathrm{GD}}$) capacitances. The capacitances C_{GS}, C_{GD}, and C_{DS} are measured to clarify the device structure and physical behavior, and C_{ISS},

C_{OSS}, and C_{RSS} are used to estimate their influence on circuit operation.

The developed measurement circuit can apply a bias voltage between drain and source, and simultaneously to the gate with reference to the source potential. Thus, the circuit can measure the C-V characteristics for both normally-off and normally-on devices [60]. Also, it enables measurement of the capacitances from the blocking condition to the conducting condition with varying gate bias voltage. For instance, a power MOSFET is a high-voltage power device, and its measurements illustrate the physical phenomenon occurring in the device, which depends on the applied drain and gate bias voltages.

3.2 Capacitance of a power device and measurement circuit

This section examines the makeup of the capacitive component in a power transistor when assuming a planar gate device structure and a vertical drift region-type double-diffused MOSFET (VDMOSFET) [7]. Further, this chapter discusses a circuit for measuring the capacitance between the power device terminals. The circuit can apply bias voltages between drain and source V_{DS}, and gate and source V_{GS}, up to the rated voltage of the device.

3.2.1 Terminal capacitances of VDMOSFET

Figure 3.1(a) shows the cross section of one cell in a VDMOSFET chip. The main dielectrics for inducing capacitance in the cell are the depletion layer formed in the semiconductor and the gate oxide. The capacitances arising from the gate oxide have a constant value, irrespective of the voltage applied across it. However, the capacitance arising from the depletion layer, which is formed in the semiconductor, changes with the applied voltage across it, where the capacitance is treated as a differential capacitance $\mathrm{d}Q/\mathrm{d}V$. Here, $\mathrm{d}Q$ denotes the charge depleted to the incremental bias voltage $\mathrm{d}V$. The capacitance components residing in the VDMOSFET are integrated into three terminal capacitances C_{GS}, C_{GD}, and C_{DS}, when they are estimated from the terminal of the

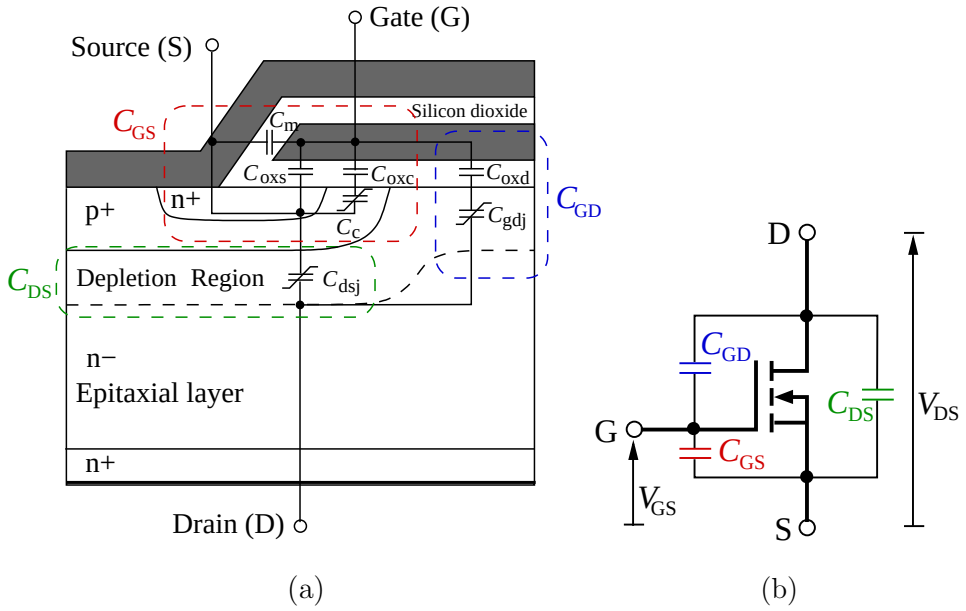


Figure 3.1 Example of a gate-controlled transistor to illustrate device capacitance. (a) Cross section of a VDMOSFET cell. (b) Equivalent capacitances between terminals of VDMOSFET.

electrode in a discrete device, as shown in Fig. 3.1(b). These terminal capacitances are configured by the capacitive components shown in Fig. 3.1(a) as

$$\begin{cases} C_{\mathrm{GS}} = C_{\mathrm{m}} + C_{\mathrm{oxs}} + \dfrac{1}{1/C_{\mathrm{oxc}} + 1/C_{\mathrm{c}}}, \\ C_{\mathrm{GD}} = \dfrac{1}{1/C_{\mathrm{oxd}} + 1/C_{\mathrm{gdj}}}, \\ C_{\mathrm{DS}} = C_{\mathrm{dsj}}. \end{cases} \tag{3.1}$$

Here, C_{m} denotes the capacitance between the gate electrode and the source electrode across the gate oxide, C_{oxs} the capacitance of the gate electrode and source n^+ region, C_{oxc} the capacitance of the gate electrode and the top surface of the p^+ region, C_{c} the capacitance of the depletion region for the p^+ region under the gate, C_{oxd} the capacitance of the gate electrode and top surface of the drain region across the gate oxide, C_{gdj} the capacitance of the depletion region for the drain under the gate, and C_{dsj} the capacitance of the depletion region for the drain under the source.

The combination of terminal capacitances in the power device determines circuit operation. The input capacitance is the equivalent capacitance when the transistor is

grasped from the gate terminal to drive the gate; it can be expressed as $C_{\mathrm{ISS}} = C_{\mathrm{GS}} + C_{\mathrm{GD}}$. The reverse transfer capacitance C_{RSS} is the same as C_{GD}. It induces the well-known Miller effect and deteriorates the gate driving response because of the effectively increased capacitance by the multiplier factor of device transconductance [22]. The output capacitance corresponds to the capacitance from the drain terminal, and its charge/discharge operation by the drain current affects the main circuit response. It can be expressed as $C_{\mathrm{OSS}} = C_{\mathrm{DS}} + C_{\mathrm{GD}}$. Thus, five capacitance specifications are needed to characterize the device.

3.2.2 C_{GS} measurement circuit

Figure 3.2 shows the circuit for measuring C_{GS}. This circuit can perform four-terminal (Kelvin sense) measurements—H_{pot} and L_{pot} (for detecting the small ac voltage of the measurement signal) and H_{cur} and L_{cur} (for detecting the current of the measurement signal). The four measurement terminals are connected to an LCR meter or impedance analyzer. $C1$ and $C2$ block the bias gate voltage, transferring only the ac measurement signal from terminals H_{pot} and H_{cur}. These blocking capacitors enable application of the V_{GS}, and the circuit measures the capacitance characteristics related to channel condition, such as accumulation, depletion, and inversion. Moreover, the blocking capacitance enables the measurement of C_{GS} for a normally-on device by applying a gate voltage and making the device channel operate in the blocking condition. The V_{GS} and V_{DS} impose the dc bias voltage, and the C-V characteristics are measured by sweeping one of them. The ac measurement signal at the source terminal is blocked by $L1$ (because of its high impedance at the operating frequency); therefore, it is transferred to terminals L_{cur} and L_{pot}. $L1$ shorts the source terminal to dc ground and establishes the dc bias voltages V_{GS} and V_{DS} at the device terminals with reference to ground potential. Diodes $D1$-$D12$ and $ZD1$-$ZD4$ provide protection. The RC circuit at the V_{GS} and V_{DS} input and the monitor output constitute a low-pass filter to block the measurement signal, and apply and measure the dc bias voltage. $C7$ shorts the drain terminal when measuring an ac frequency and blocks dc from the measurement.

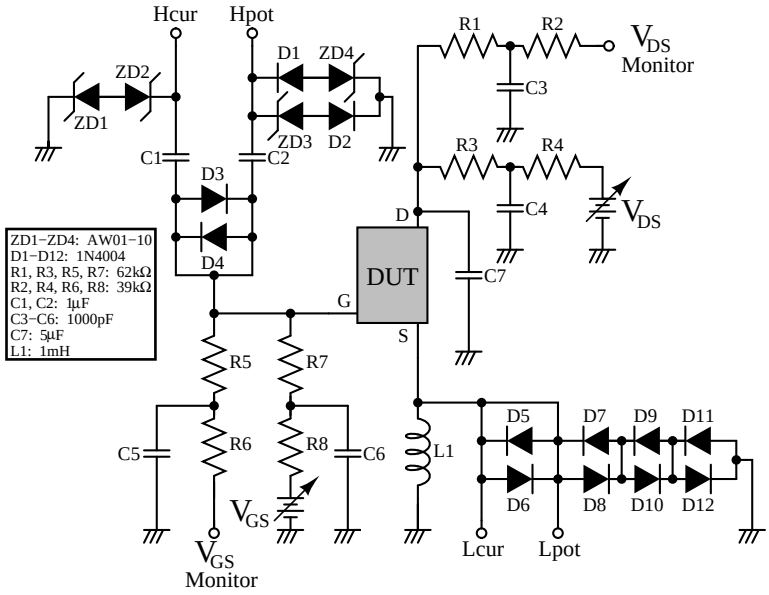


Figure 3.2 C_{GS} measurement circuit.

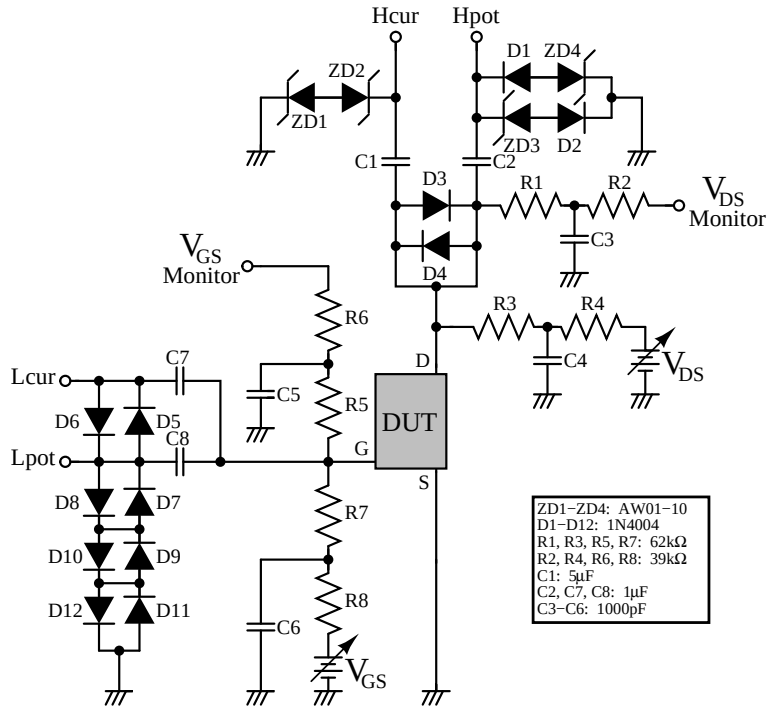


Figure 3.3 $C_{\mathrm{GD}}(C_{\mathrm{RSS}})$ measurement circuit.

3.2.3 $C_{\mathrm{GD}}(C_{\mathrm{RSS}})$ measurement circuit

Figure 3.3 shows the circuit diagram for measuring $C_{\mathrm{GD}}(C_{\mathrm{RSS}})$. This circuit has two groups of blocking capacitors for the drain and source terminals to ensure ground potential at the source terminal. $C1$ and $C2$ block the dc bias voltage of V_{DS}, and $C7$ and $C8$ block the dc bias voltage of V_{GS}. The capacitances transfer the ac measurement signal from H_{cur} and H_{pot} to L_{cur} and L_{pot}, respectively. The source terminal is directly grounded, and the capacitance component in the device related to the source terminal is excluded from the measurement. The dc bias voltages V_{DS} and V_{GS} are applied and monitored through the RC filter.

3.2.4 C_{DS} measurement circuit

Figure 3.4 shows the circuit diagram for measuring C_{DS}. $C1$ and $C2$ block the dc bias voltage V_{DS} and transfer the ac measurement signal from H_{cur} and H_{pot} terminals. The dc bias voltages V_{DS} and V_{GS} are applied and monitored through the RC filter

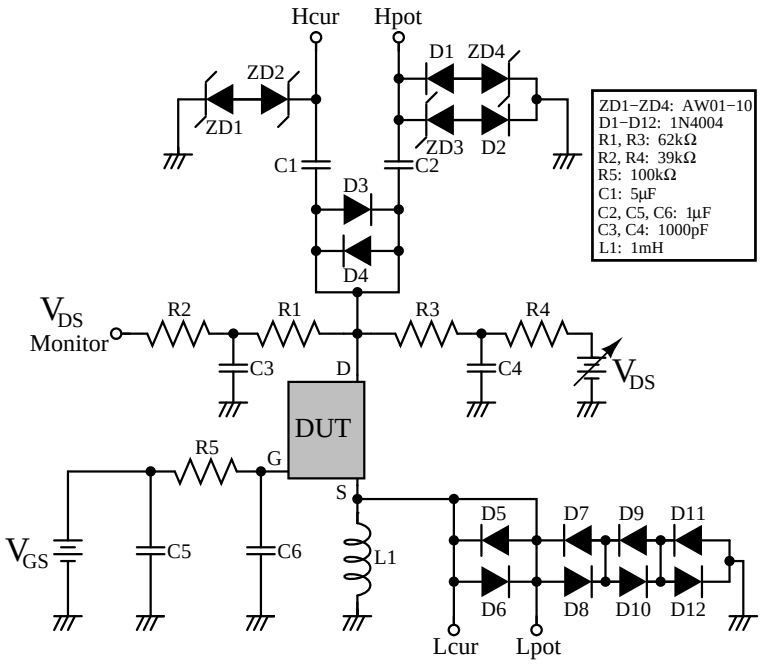


Figure 3.4 C_{DS} measurement circuit.

circuit. $L1$ connected to the source terminal, blocks the measurement ac signal and transfers it to L_{cur} and L_{pot}. However, it shorts the source terminal to dc ground and helps to establish the dc bias voltage with reference to the source terminal. $C6$ connected to the gate terminal, blocks the dc voltage, and establishes the dc potential of the gate terminal, but shorts ac signals to ground. Therefore, the capacitive component connected to the gate terminal is excluded from the measurement since it is shunted to the ground.

3.2.5 C_{ISS} measurement circuit

Figure 3.5 shows the circuit diagram for measuring the input capacitance C_{ISS}. This circuit differs from the former measurement circuits in that it measures the combined capacitance of C_{GS} and C_{GD}, which have different dc potentials for the drain and source. $C1$, $C2$, $C7$, and $C8$ block the dc bias voltages of V_{DS} and V_{GS}, and transfer the ac measurement signal from H_{cur} and H_{pot} to L_{cur} and L_{pot}, respectively. The dc bias voltages V_{DS} and V_{GS} are applied and monitored through the RC filter. $L1$ shorts dc signals at the source terminal to ground, establishes the reference potential for the

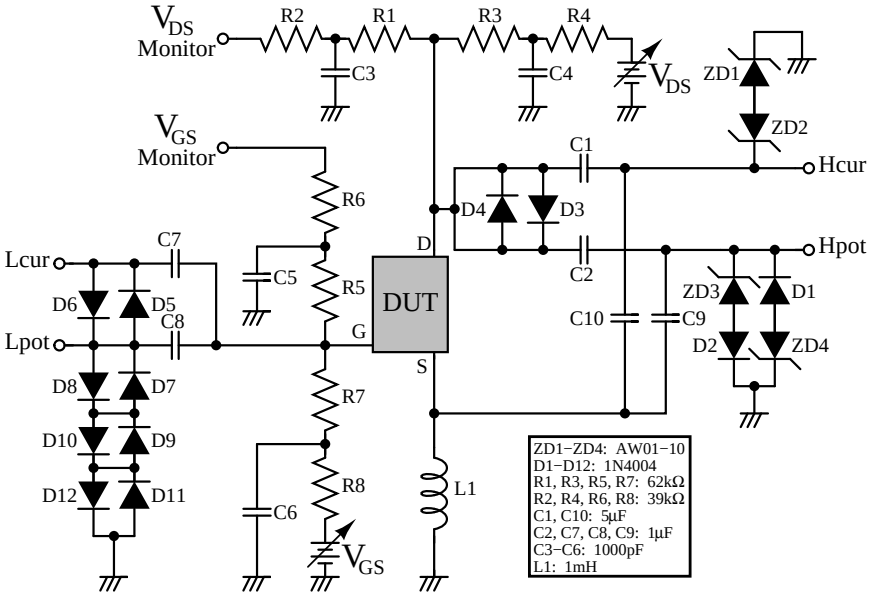


Figure 3.5 C_{ISS} measurement circuit.

dc bias voltage, and blocks the ac measurement signal from shorting to ground. The blocked ac measurement signal is transferred to H_{cur} and H_{pot} terminals through the bypass capacitors $C9$ and $C10$. Consequentially, the capacitance between the drain and source terminals are eliminated by bypass capacitors $C1$, $C2$, $C9$, and $C10$.

3.2.6 C_{OSS} measurement circuit

Figure 3.6 shows the circuit diagram for measuring the output capacitance C_{OSS}, which is the combined capacitance of C_{DS} and C_{GD}—the capacitances have different dc potentials at the gate and source terminals. Capacitors $C1$ and $C2$ block the dc bias voltage of V_{DS} and transfer the ac measurement signal from terminals H_{cur} and H_{pot}. The dc bias voltages V_{DS} and V_{GS} are applied and monitored through the RC filter. $L1$ shorts dc signals to ground at the source terminal and establishes the reference potential for the dc bias voltage. It also blocks the ac measurement signal from shorting to ground and helps transfer it to terminals L_{cur} and L_{pot}. $C6$ blocks the

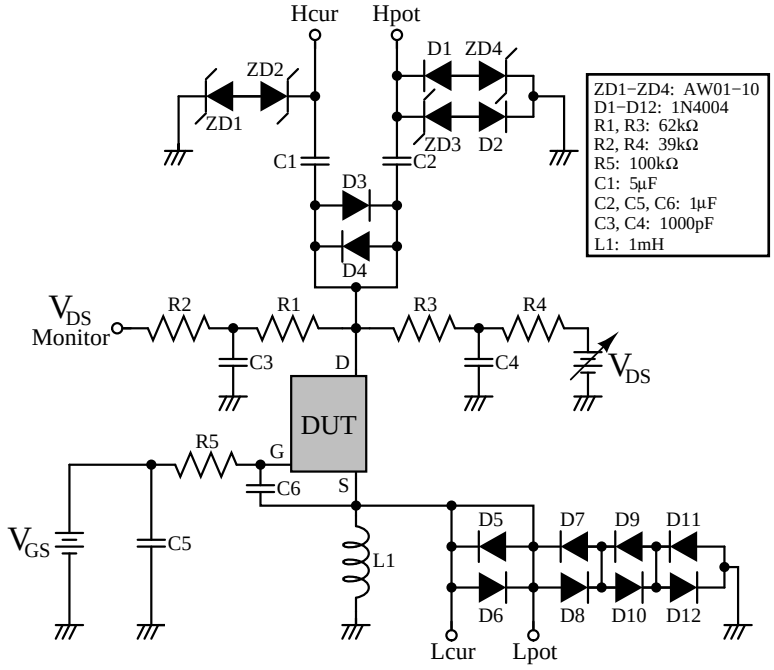


Figure 3.6 C_{OSS} measurement circuit.

dc bias voltage of V_{GS} from the source and passes the ac measurement signal, which is then transferred to L_{cur} and L_{pot} terminals. $L1$ provides a high ac resistance to ground. $C6$ bypasses and eliminates the C_{GS}.

The values of the blocking and bypass capacitances are selected to have sufficiently small impedance with relation to the capacitance measurement or elimination ability in the device. Film-type capacitors are adopted because of their superior high frequency performance, but high-voltage-blocking large capacitors tend to be bulky and

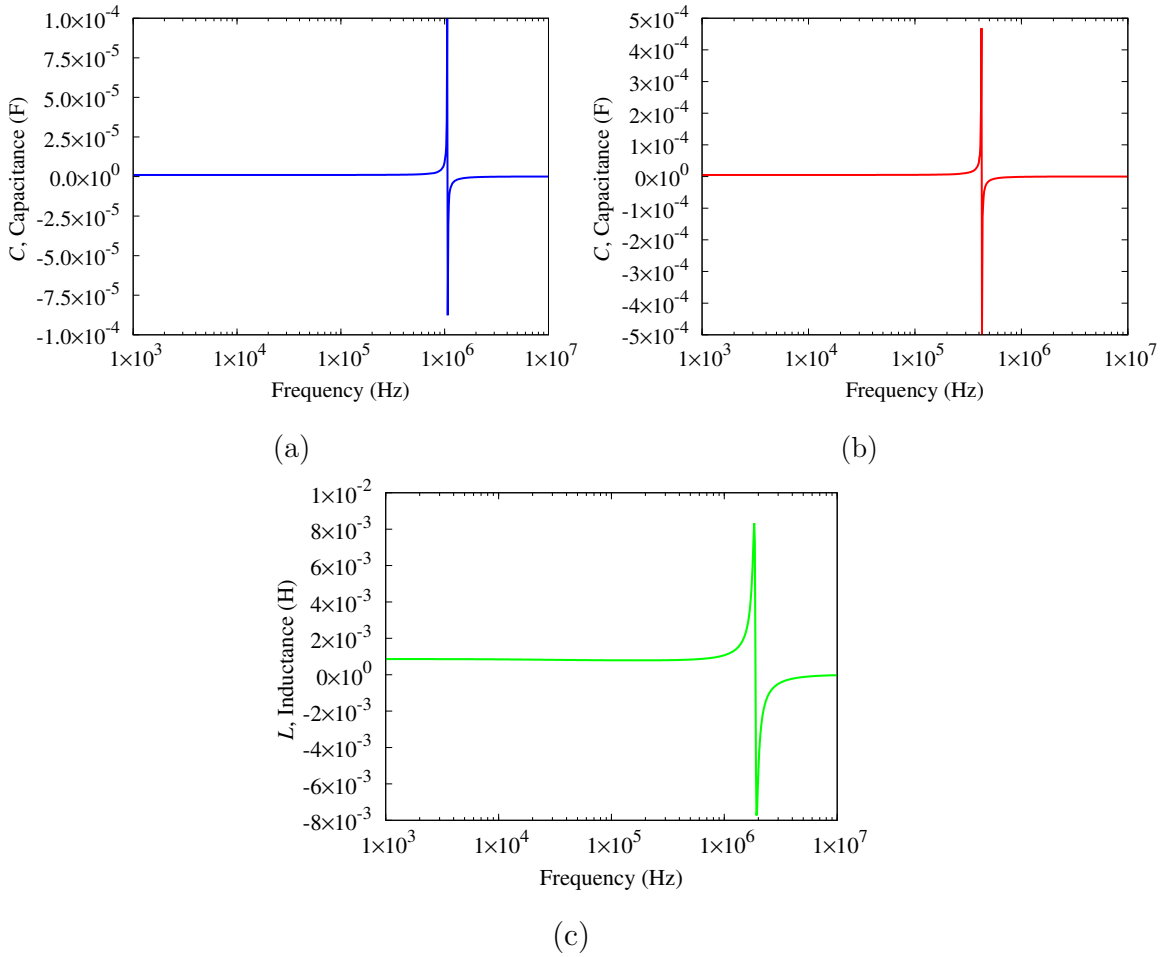


Figure 3.7 Frequency characteristics of blocking element. (a) Blocking capacitor (1 μF, 850 V) ($C_{\mathrm{S}} + R_{\mathrm{S}}$ measurement), (b) Blocking capacitor (5 μF, 700 V) ($C_{\mathrm{S}} + R_{\mathrm{S}}$ measurement), and (c) Blocking inductor (1 mH) ($L_{\mathrm{S}} + R_{\mathrm{S}}$ measurement)

have relatively large effective series inductance (ESL). Figure 3.7 shows the frequency characteristics of blocking element used for blocking high voltages and measurement ac signal as measured by an impedance analyzer (Agilent 4294A). The largest capacitance used in the measurement circuit has a self-resonant frequency around 300 kHz because of the capacitance and ESL, as shown in Fig. 3.7. JEDEC [60] suggests that the measurement frequency be low enough to prevent the introduction of the error stemming from parasitic components, and frequencies below 2 MHz are preferred. Therefore, 100 kHz was selected as the measurement frequency.

3.3 Measurement of C-V characteristics

This section certifies the measured capacitance using the developed capacitance measurement circuit, based on a reference capacitance set whose values are known a *priori*. The measured C-V characteristics of an example device are presented and their features discussed as associated with the device structure and composition.

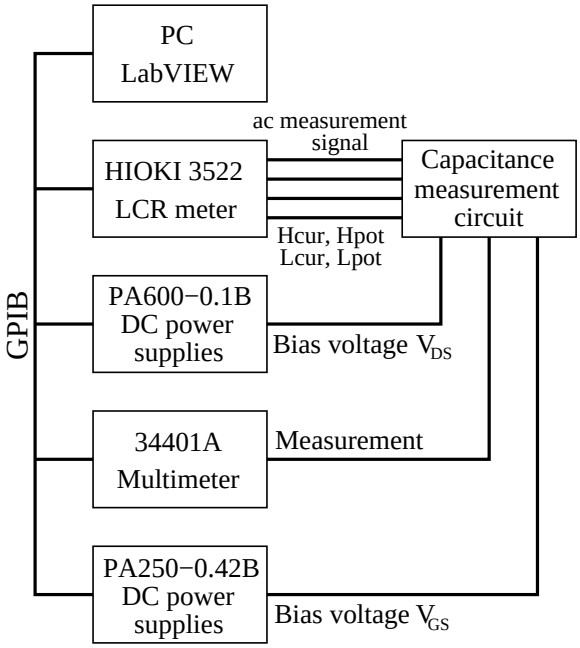


Figure 3.8 Configuration of C-V characterization system.

Table 3.1 Test results for reference capacitance (nF) [$C_a = 11.01$ nF, $C_b = 21.57$ nF, $C_c = 33.36$ nF].

GS	GD	DS	C_{GS} (err%)	C_{GD} (err%)	C_{ISS} (err%)	$C_{GS} + C_{GD}$ (err%)	C_{DS} (err%)	C_{OSS} (err%)	$C_{DS} + C_{GD}$ (err%)
C_a	C_b	C_c	11.47 (4.10)	21.44 (0.60)	32.64 (0.18)	32.90 (0.99)	33.35 (0.04)	54.50 (0.79)	54.79 (0.26)
C_a	C_c	C_b	11.33 (2.90)	33.25 (0.31)	44.46 (0.21)	44.59 (0.49)	22.11 (2.52)	53.89 (1.89)	55.37 (0.80)
C_b	C_a	C_c	22.02 (2.10)	11.02 (0.05)	32.72 (0.41)	33.04 (1.41)	34.05 (2.08)	44.30 (0.15)	45.07 (1.58)
C_b	C_c	C_a	21.74 (0.80)	33.42 (0.17)	55.18 (0.45)	55.16 (0.42)	11.46 (4.02)	43.35 (2.29)	44.87 (1.13)
C_c	C_a	C_b	33.83 (1.40)	11.05 (0.33)	44.65 (0.62)	44.88 (1.14)	22.40 (3.85)	32.47 (0.36)	33.45 (2.66)
C_c	C_b	C_a	33.59 (0.70)	21.38 (0.90)	55.25 (0.58)	54.97 (0.08)	11.51 (4.47)	32.16 (1.31)	32.88 (0.92)

3.3.1 Certification of the measurement circuit

The developed capacitance measurement circuit is connected to a HIOKI 3522 LCR meter to quantify the capacitance through measurement terminals H_{cur}, H_{pot}, L_{cur}, and L_{pot} as shown in Fig. 3.8. At the beginning of setting up the experiment, open- and short-circuit calibration of the measurement circuit is performed for LCR meter operation. Although the developed circuit applies a bias voltage between terminals, a dc short-circuit current flows through the bias voltage source. Therefore, a 0-V dc bias voltage is applied during circuit calibration. Three capacitances C_a, C_b, and C_c, whose values are given in the margin of Tab. 3.1 and are similar to those of an actual semiconductor device, are used to validate the measurement circuit. The test capacitors are constant capacitances connected in delta to imitate the terminal capacitance of a power device, and six possible combinations of the terminal connection are tested for the five capacitance measurements. The measured values for the respective combinations of reference capacitance connections are given in Tab. 3.1. The relative

percentage error of the actual value is also given in parentheses. The compound capacitances $C_{GS} + C_{GD}$ and $C_{DS} + C_{GD}$, which are, respectively, equivalent to C_{ISS} and C_{OSS}, are also shown in the table for comparison.

The measurement errors for C_{GD} and C_{ISS} were confirmed as less than 1% that is a low error. The error in measuring C_{GS} tends to become large when C_{DS} is larger than C_{GS}. This can be attributed to measurement signal leakage in the blocking inductor $L1$ and bypass capacitor $C7$ (see Fig. 3.2). The opposite effects are found in the measurement of C_{DS}. The error in C_{DS} becomes large when C_{GS} is larger than C_{DS}. This is attributed to measurement signal leakage in blocking inductor $L1$ and bypass capacitor $C6$ (see Fig. 3.4). Thus, the errors of compound capacitance $C_{GS} + C_{GD}$ tend to become larger than directly measured C_{ISS}, except when C_{DS} is small. The error in the measured C_{OSS} becomes large when C_{GD} is larger than C_{DS}. The leakage of the measurement signal through $L1$ in Fig. 3.6 cannot explain this phenomenon. Hence, this can be attributed to the residue of the measurement signal for the bypass capacitor $C6$ (see Fig. 3.6), i.e., the detection terminal for C_{DS} is directly connected to the LCR meter through L_{cur} and L_{pot} terminals, but the detection terminal for C_{GD} is connected to the LCR meter through $C6$. Therefore, the C_{OSS} measurement circuit is amenable to C_{GD} value. The errors of directly measured C_{OSS} tend to become larger than the compound capacitance $C_{DS} + C_{GD}$ when C_{GD} is small. The extracted error falls within 5% using the measurement circuit parameters, as shown in Figs. 3.2-3.7. This error can be reduced by increasing the value of the blocking and bypassing elements. The accuracy given in Tab. 3.1 is sufficient to characterize the device because of the dispersion of the characteristics among devices.

3.3.2 Measured Results

The measured C-V characteristics are exemplified here by considering a planar gate VDMOSFET with a 600-V-rated voltage (2SK3767) as an example, and the relationship of the capacitance characteristics to the device structure is discussed.

Figure 3.9(a) illustrates the relationship of the measured C_{GS}, C_{GD}, and C_{DS} to V_{DS} with $V_{GS} = 0$ V. C_{GS} is larger than C_{DS} and C_{GD} when $V_{DS} > 1$ V because of the

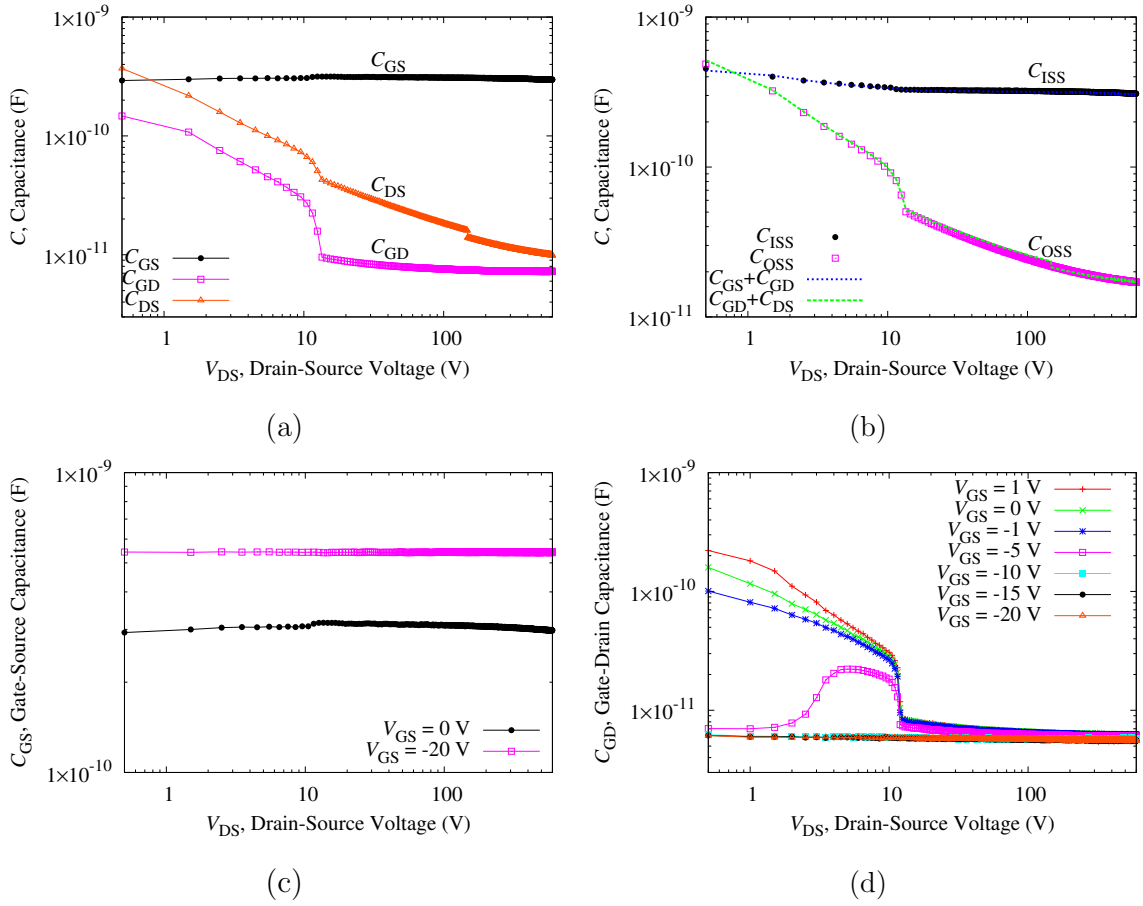


Figure 3.9 Measured C-V characteristics of VDMOSFET for V_{DS}. (a) C_{GS}, C_{GD}, and C_{DS} ($V_{GS} = 0$ V). (b) C_{ISS} and C_{OSS} ($V_{GS} = 0$ V). (c) C_{GS} for different V_{GS}. (d) C_{GD} for different V_{GS}.

closely spaced gate and source electrodes at the surface of the device. It barely changes with the applied V_{DS}, because V_{DS} does not affect the expansion of the depletion region across the gate and source. Also, depletion in the drift layer depends on V_{DS}. Therefore, C_{DS} and C_{GD} decrease with increasing V_{DS} in accordance with the expansion of the depletion region. There are irregular capacitance changes around $V_{DS} = 13$ V, which can be attributed to the transition of the expanding depletion region from the JFET region of the planar gate VDMOSFET to the entire drift region.

Figure 3.9(b) illustrates the directly measured C_{ISS} and C_{OSS} and the calculated $C_{ISS}(= C_{GS} + C_{GD})$ and $C_{OSS}(= C_{DS} + C_{GD})$ from the measured C_{DS}, C_{GS}, and C_{GD}.

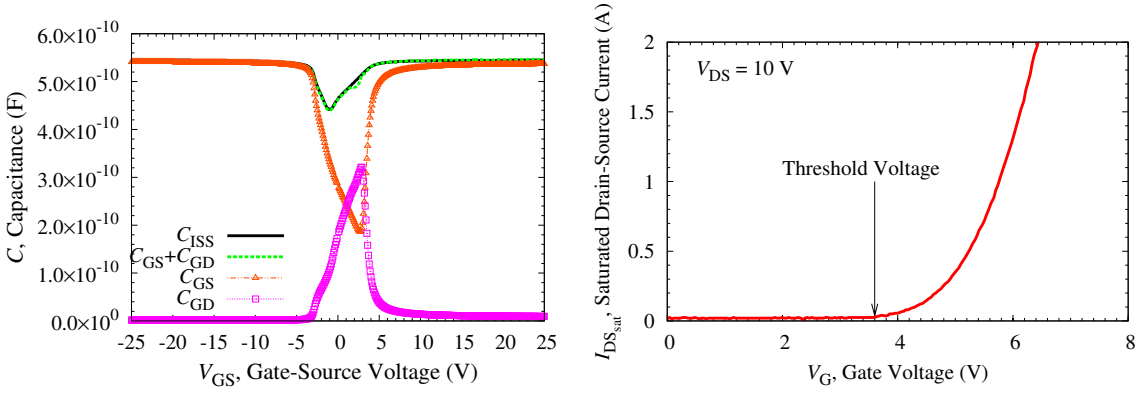


Figure 3.10 (a) Measured C-V characteristics of VDMOSFET for V_{GS}. (b) Measured $I_{\mathrm{DS_{sat}}}$-V_{G} characteristics of VDMOSFET.

The respective results coincide, validating the adequacy of the measured results. Figure 3.9(c) shows measured C_{GS} to V_{DS} for different V_{GS}. The accumulation of charge (holes) occurs at the device channel and results in a decrease in C_{c}, as shown in Fig. 3.1(a), when a gate voltage of $V_{\mathrm{GS}} = -20$ V is applied. C_{GS} becomes larger than the depleted condition of the channel by the time $V_{\mathrm{GS}} = 0$ V. This phenomenon is shown clearly in Fig. 3.10(a), where C_{GS} is measured to V_{GS} and $V_{\mathrm{DS}} = 0$ V. C_{GS} begins to decrease when V_{GS} becomes higher than -3 V and it reaches a minimum around $V_{\mathrm{GS}} = 3$ V. This indicates the depletion of the accumulated charge (holes) at the channel with increase in V_{GS}. The inversion at the channel begins to occur with increasing gate voltages when V_{GS} exceeds 3 V, and C_{GS} increases to the threshold voltage. The threshold voltage of this device is 3.5 V, as shown in Fig. 3.10(b), and the channel conducts for a higher gate voltage. Figure 3.9(d) shows $C_{\mathrm{GD}}(C_{\mathrm{RSS}})$ to V_{DS} for different V_{GS}. The accumulation phenomenon is also seen at the top of the JFET region in a planar device around C_{gdj}, as shown in Fig. 3.1(a), and C_{GD} varies with V_{GS}. It also shows that negative V_{GS} reduces C_{GD}. This phenomenon is clearly confirmed in Fig. 3.10(a), where C_{GD} is measured at V_{GS} and $V_{\mathrm{DS}} = 0$ V. The accumulation at the top of the JFET region tends to occur when voltages with different polarities are applied across that part, resulting in an increase in C_{gdj} as shown in Fig. 3.1(a). Then,

C_{GD} becomes large for low V_{DS} within the -3 V $< V_{GS} < 3$ V region. The capacitance measurement is by no means restricted to merely determining the capacitance between terminals, but it can also clarify a wide variety of physical phenomenon occurring in the device.

3.4 Summary

The capacitances between the terminals of a power device are important for understanding the dynamic behavior of the device, such as its switching operation. The device capacitances are not constant and change with the voltage applied between the terminals. Therefore, a C-V characterization system for gate-controlled power devices was developed in this study. Five measurement circuits were proposed to measure the three combinations of capacitances between the device terminals, and three combinations of device capacitance for circuit operation. The adequacy of the proposed measurement system was verified using a reference capacitance and the factor of error was discussed. The developed capacitance characterization system can measure capacitance from the blocking condition to the conducting condition while changing the gate bias voltage. The variation of the accumulation, depletion, and inversion conditions in the device was reflected to the device capacitance. The measured capacitance explained the device structure and the physical phenomenon occurring in the device.

Chapter 4

Characterization of SiC power MOSFET

4.1 Introduction

Power MOSFETs are practically used in high frequency switching power converter circuits due to the fast turn-off capability [27,28]. Recently, power converters have been requested to operate at high voltage, high-temperature, and fast switching to realize their high performances. However, the limitation to the above requirements is low for the silicon (Si) power devices. To overcome the difficulty, silicon carbide (SiC) power devices have been researched and developed because of its several superior physical characteristics than Si [1, 3, 7]. The device modeling is inevitable in circuit simulation to evaluate the voltage and current response in power converter circuit and to achieve system performance in their applications. This chapter focuses on the modeling based on detailed measurements.

In the references [28, 61, 62], the dynamic behavior of the device is discussed with relation to their internal parasitic capacitances, drain-source current I_{DS}, drain current $I_{\mathrm{T}}(= I_{\mathrm{D}})$, gate current I_{G}, gate-source voltage V_{GS}, and drain-source voltage V_{DS}. The equivalent capacitance between terminals of the device affects on its switching behavior. The capacitance in a power device changes nonlinearly with applied voltage between terminals (V_{GS} and V_{DS}), because it comprises the depletion capacitance in

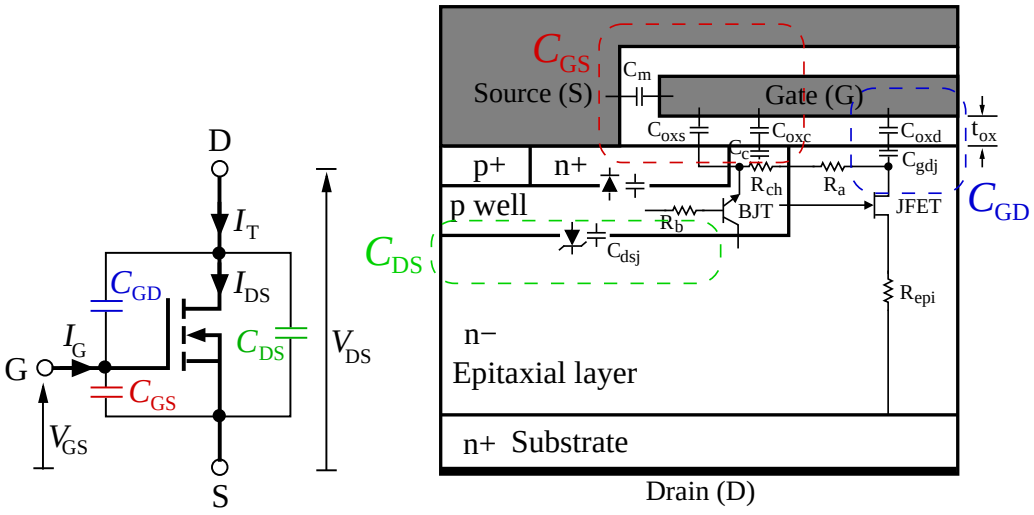


Figure 4.1 (a) Equivalent terminal capacitances. (b) Cross section of SiC DiMOSFET cell.

the device [29]. Then, it is important to characterize the C-V characteristics of the SiC MOSFET to estimate its switching performance. Figures 4.1(a) and (b) show the equivalent capacitance between terminals and the cross section of the SiC DiMOSFET cell, respectively [7, 8]. The equivalent terminal capacitances are composed of the capacitances C_{GS}, C_{GD}, and C_{DS}. Here, the C_{GS} and C_{GD}, which combine the gate oxide and depletion capacitance, constitute the input capacitance $C_{\mathrm{ISS}}(= C_{\mathrm{GS}} + C_{\mathrm{GD}})$. It is charged and discharged by the gate drive circuit for switching operation. C_{GD} is also equivalent to the reverse transfer capacitance C_{RSS}. The effective capacitance is multiplied the voltage gain of the MOSFET in switching operation by Miller effect. Also, $C_{\mathrm{GD}}(= C_{\mathrm{RSS}})$ and C_{DS} constitute the output capacitance $C_{\mathrm{OSS}}(= C_{\mathrm{GD}} + C_{\mathrm{DS}})$, which is charged and discharged by the load current, and governs the switching speed. The C_{GS} mainly depends on the applied V_{GS}, the C_{GD} varies with both the V_{GS} and V_{DS}, and the C_{DS} largely varies with the V_{DS}.

This chapter characterizes the voltage dependency of terminal capacitances of the power MOSFETs, models the I-V characteristics with discussing the C-V characteristics of the devices, and extracts the model parameters from the measured C-V

characteristics. Next, this chapter discusses and compares the difference in V_{GS} dependency of terminal capacitances between the SiC MOSFET and the Si MOSFET to estimate the difference in their switching behavior. The constitution of internal parasitic components in the devices are also addressed. Finally, the obtained model is validated by comparing the experimental results of the switching response.

4.2 Characterization

The details of the studied SiC power MOSFET are mentioned in Chapter 2. This section describes the characterization of the SiC power MOSFET, which has been carried out under room temperature. The static I-V characteristics for the forward conduction condition were measured as the dc characteristics using IWATSU IE-1198 curve tracer. The C-V characteristics for the reverse non-conducting condition were measured as the ac characteristics by the capacitance measurement system in Chapter 3.

4.2.1 Forward dc characteristics of power MOSFET

Figures 4.2 and 4.3 show the measured and modeled forward conduction characteristics of the 900-V, 1-A SiC DiMOSFET and 600-V, 2-A Si DMOSFET, respectively. The V_{GS} is set at a governing parameter. The charged/discharged currents for parasitic capacitance are neglected at steady-state condition. The steady-state forward I-V characteristics of a power MOSFET is drawn by a pentode like curve to a parameter of V_{GS}. The relationship between I_{DS} and V_{DS} is modeled as [27, 64] a function of V_{GS} and V_{DS} at the steady-state by Eq. (4.1) :

$$I_{DS} \cong \begin{cases} \dfrac{\beta}{2(1+\theta(V_{GS}-V_T))}\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right](1+\lambda V_{DS}) \\ \qquad \text{for } V_{DS} \le V_{GS}-V_T, \\ \dfrac{\beta}{2(1+\theta(V_{GS}-V_T))}(V_{GS}-V_T)^2(1+\lambda V_{DS}) \\ \qquad \text{for } V_{DS} > V_{GS}-V_T, \end{cases} \tag{4.1}$$

where β denotes the MOSFET channel transconductance, V_{T} the threshold voltage, λ the channel length modulation factor, and θ the mobility modulation coefficient. Here, the effect of drain resistance R_{D} and source resistance R_{S} in this model is neglected.

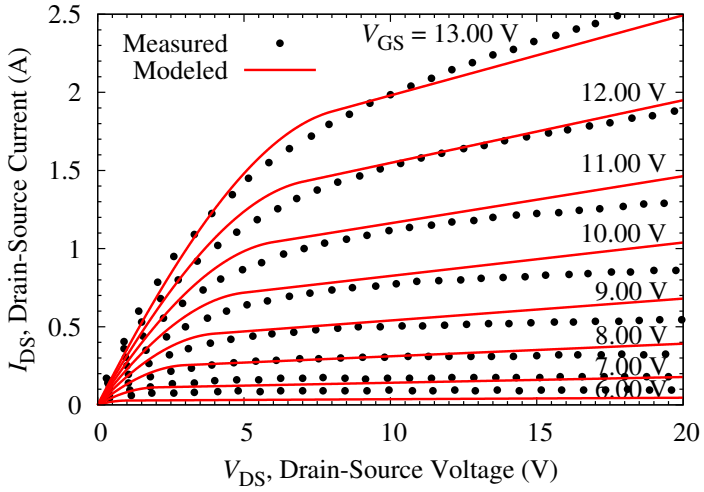


Figure 4.2 Static I-V characteristics of SiC DiMOSFET.

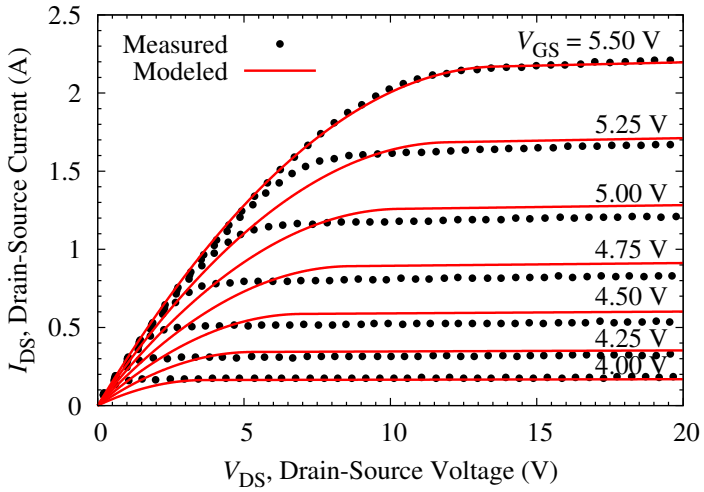


Figure 4.3 Static I-V characteristics of Si DMOSFET.

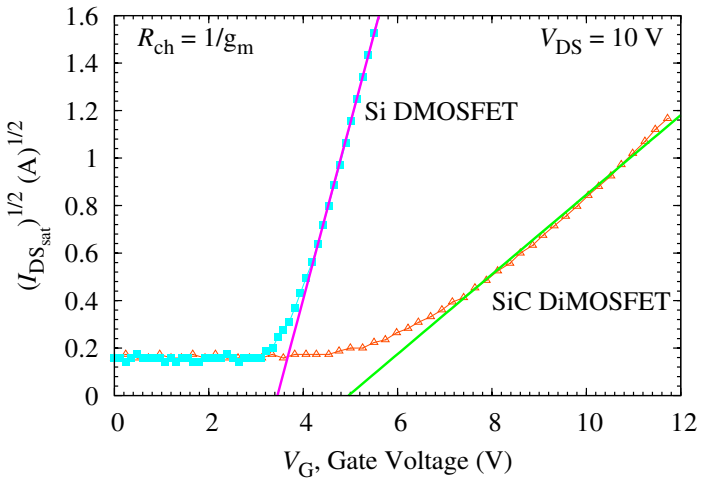


Figure 4.4 Transfer characteristics of power MOSFET.

Determination of β and V_T

The drain-source current of MOSFET I_{DS} is given irrespectively to the drain voltage by Eq. (4.1) for saturation region of $V_{DS} > V_{GS} - V_T$. Thus, the MOSFET channel transconductance β and the threshold voltage V_T can be estimated from Eq. (4.1) with the MOSFET transfer characteristics, which is shown in Fig. 4.4, when the λ is approximately equal to zero.

Determination of λ

The channel length modulation factor λ is determined from the rating current on a set of static I-V characteristics in the saturation region. The detailed definition on λ is given in Ref. [63].

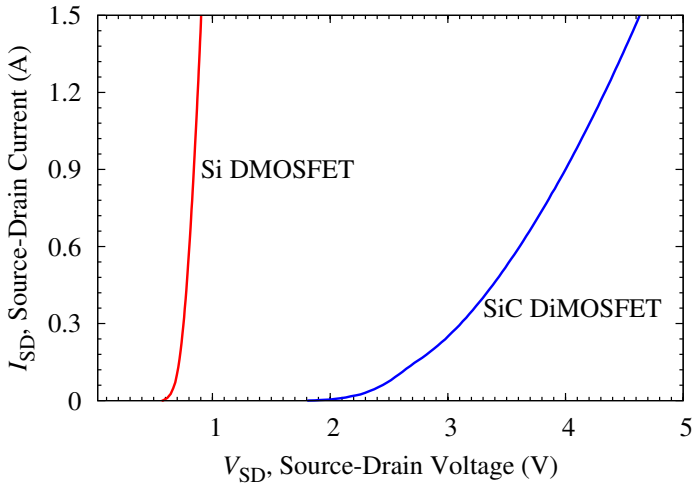
Determination of θ

The deviation of the measured I_{DS} current from the linear dependence in due to the mobility reduction effect, and is taken into account by the mobility modulation coefficient θ. Therefore, θ is determined from the linear region by Eq. (4.1) [65].

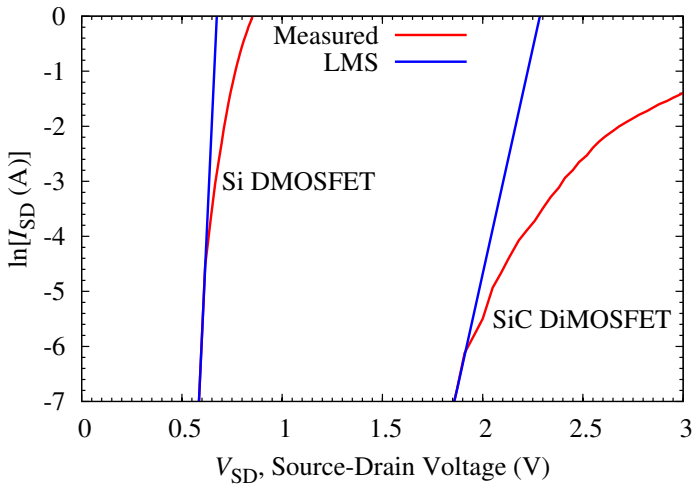
The model extracted parameters of static I-V characteristics of power MOSFET are summarized to Tab. 4.1.

4.2.2 Reverse conduction dc characteristics of power MOSFET

Due to the device structure, the power MOSFET has a body diode, which is connected anti-parallel to drain-source of the power MOSFET as depicted in Fig. 4.1(b). In the body diode I-V curve measurement, the device channel needs to be pinched off during the measurement. This implies shorting the gate-source terminals ($V_{GS} = 0$



(a) Linear-linear



(b) Logarithmic-linear

Figure 4.5 Reverse conduction characteristics of power MOSFET.

V) of the power MOSFET. Figure 4.5 shows the reverse conduction characteristics of power MOSFET. The dc characteristics of body diode of power MOSFET can be expressed as

$$I_{\mathrm{AK}} = I_{\mathrm{S}}\Big(e^{\frac{V_{\mathrm{D}}}{nV_{\mathrm{t}}}} - 1\Big), \tag{4.2}$$

where V_{t} denotes the thermal voltage, n the diode emission coefficient, and I_{S} the saturation current. Then, I_{S} and n are extracted by the LMS method by applying the measured data to Eq. (4.2).

4.2.3 C-V characteristics of power MOSFET

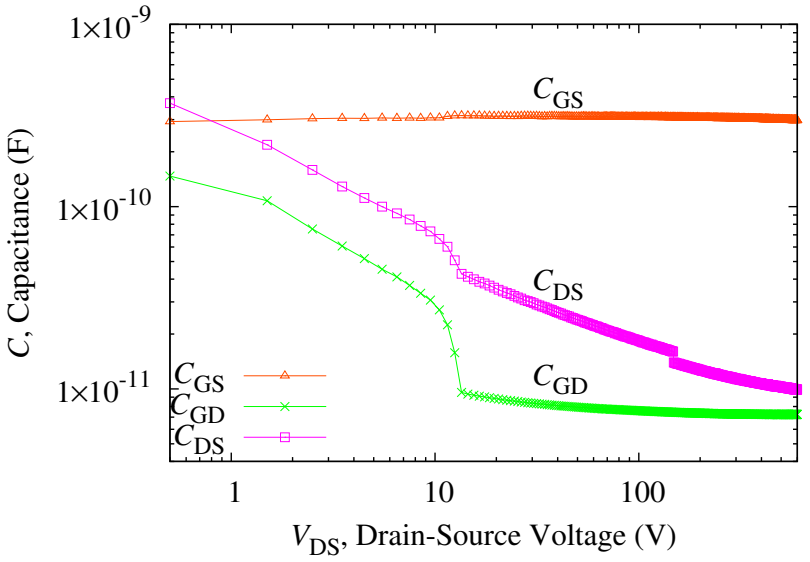
The various internal parasitic components of the device are superimposed on its cross section in Fig. 4.1(b). The physical capacitances residing in the SiC DiMOSFET are composed of the gate oxide and the depletion layer formed in the semiconductor. They are integrated into the equivalent terminal capacitances of power MOSFET C_{GS}, C_{GD}, and C_{DS}. C_{GS} and C_{GD} constitute the input capacitance $C_{\mathrm{ISS}}(= C_{\mathrm{GS}} + C_{\mathrm{GD}})$, which is charged and discharged by the gate drive circuit for switching operation. C_{GD} is also equivalent to the reverse transfer capacitance (or Miller capacitance) C_{RSS}. Also, $C_{\mathrm{GD}}(= C_{\mathrm{RSS}})$ and C_{DS} constitute the output capacitance $C_{\mathrm{OSS}}(= C_{\mathrm{GD}} + C_{\mathrm{DS}})$, which is charged and discharged by the load current, and governs the switching speed.

In the experimental setup for C-V characterization, the voltage dependence of the terminal capacitances is evaluated by the clarification of the device structure and fabrication. The C-V characteristics of power MOSFET are precisely measured by a LCR meter with applying the dc bias voltage V_{GS} and V_{DS} to the device, through C-V measurement fixture in Chapter 3.

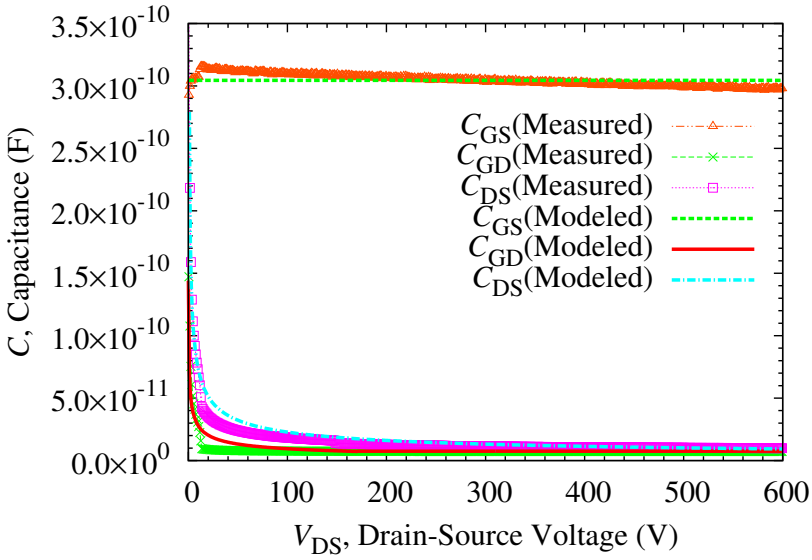
Characterization of the drain-voltage dependency of terminal capacitances

This section characterizes the drain-voltage dependency of terminal capacitances C_{GS}, C_{GD}, and C_{DS}. The C_{GS}, C_{GD}, and C_{DS} are individually measured with applying dc bias voltage V_{DS}.

Figures 4.6 and 4.7 show the C-V_{DS} characteristics of power MOSFET, which illustrate the relationships between the measured C_{GS}, C_{GD}, C_{DS}, and the V_{DS}, for a 600-V,



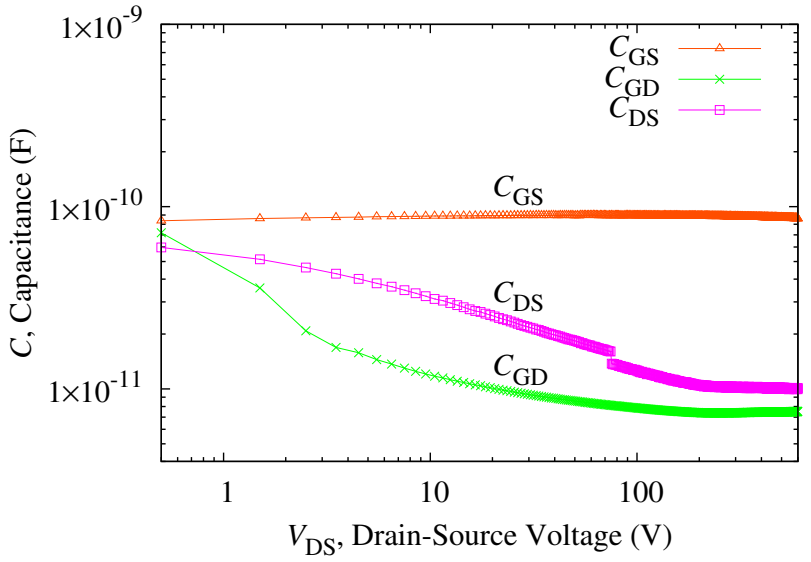
(a) Logarithmic-Logarithmic



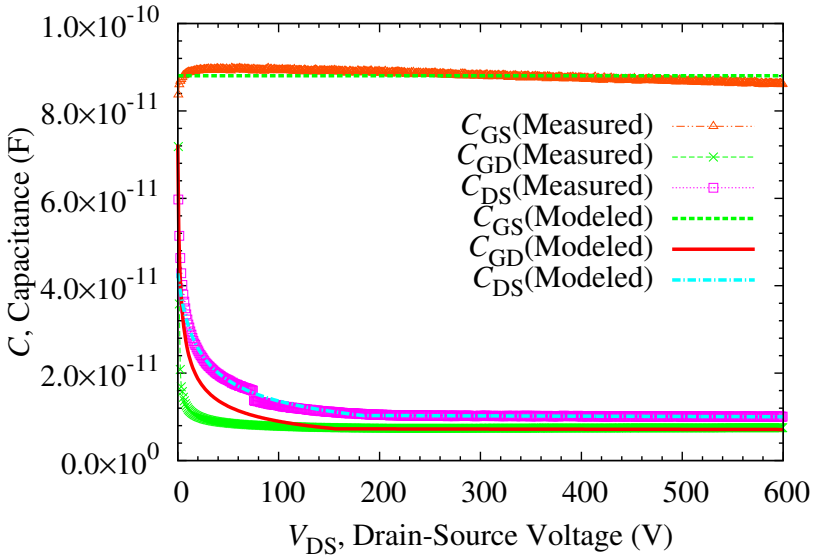
(b) Linear-Linear

Figure 4.6 C-V_{DS} characteristics of Si DMOSFET.

2-A Si DMOSFET and a 900-V, 1-A SiC DiMOSFET, respectively. The measured C-V_{DS} characteristics of the Si DMOSFET and SiC DiMOSFET are shown in Figs. 4.6(a) and 4.7(a) at logarithmic scale. The measured and modeled C-V_{DS} characteristics of the Si DMOSFET and SiC DiMOSFET are shown in Figs. 4.6(b) and 4.7(b) at linear



(a) Logarithmic-Logarithmic



(b) Linear-Linear

Figure 4.7 C-V_{DS} characteristics of SiC DiMOSFET.

scale. Setting $V_{GS} = 0$ V to block the device channel for V_{DS} dependency, V_{DS} is swept from 0 V to 600 V. The relationship between the capacitance characteristics can be obtained. C_{GS} hardly changes with the variation of V_{DS}. The values are around 304 pF for Si DMOSFET and 88 pF for SiC DiMOSFET. Because V_{DS} does not govern the

expansion of the depletion region across the gate and source. Also, depletion region in drift layer depends on $V_{\rm DS}$. On the other hand, $C_{\rm GD}$ and $C_{\rm DS}$ decrease with increase of $V_{\rm DS}$ in accordance with the expansion of the depletion region. For the Si DMOSFET, there are irregular capacitance changes around $V_{\rm DS} = 12$ V, which can be attributed to the transition of the expanding depletion region from JFET region of the planar gate MOSFET to the entire drift layer. For the SiC DiMOSFET, there are no irregular capacitance, and the decrease of the capacitance in $C_{\rm GD}$ and $C_{\rm DS}$ stops around $V_{\rm DS}$ = 200 V. It indicates that the expansion of the depletion region is terminated in the drift layer because of the punch-through structure of the device.

The C-$V_{\rm DS}$ characteristics of power MOSFETs are modeled by using Eqs. (2.36), (2.41), and (2.42). It can be expressed in the following compact form:

$$C_{\rm GS} = C_{\rm GS}(0), \tag{4.3}$$

$$C_{\rm gdj} = C_{\rm GD}(0)\Big(1 + \frac{V_{\rm DS} - V_{\rm GS}}{V_{\rm TD}}\Big)^{-1/2}, \tag{4.4}$$

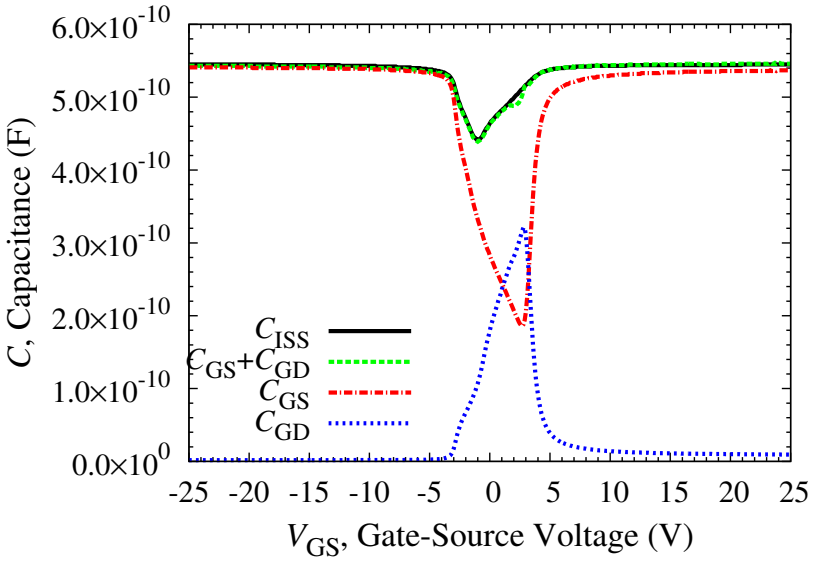
$$C_{\rm DS} = C_{\rm DS}(0)\Big(1 + \frac{V_{\rm DS}}{V_{\rm bi}}\Big)^{-1/2}, \tag{4.5}$$

where $C_{\rm GS}(0)$ denotes the gate-source zero-bias capacitance, $C_{\rm GD}(0)$ the gate-drain zero-bias capacitance, and $C_{\rm DS}(0)$ the drain-source zero-bias capacitance.

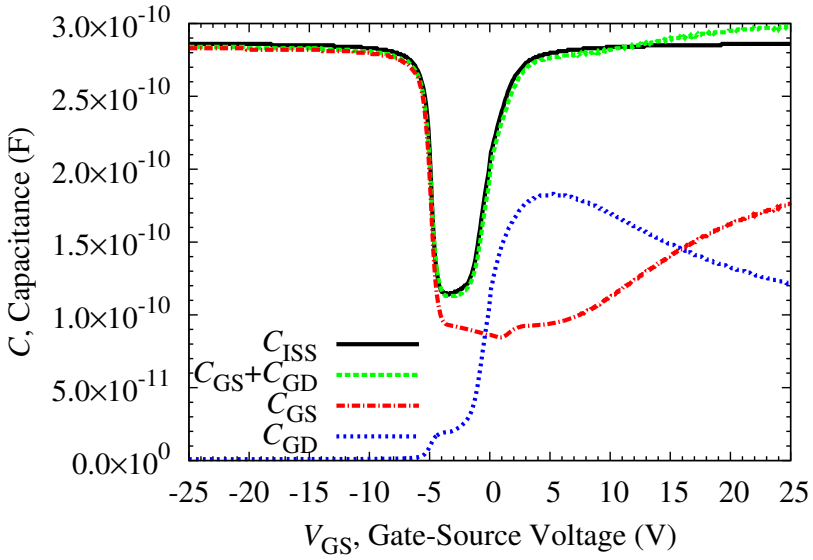
Characterization of the gate-voltage dependency of terminal capacitances

This section characterizes the gate-voltage dependency of input capacitance $C_{\rm ISS}(= C_{\rm GS} + C_{\rm GD})$. The $C_{\rm GS}$, $C_{\rm GD}$, and $C_{\rm ISS}$ are individually measured with applying dc bias voltage $V_{\rm GS}$.

Figures 4.8(a) and (b) show the measured C-V characteristics, which illustrate the relationships between the measured $C_{\rm GS}$, $C_{\rm GD}$, $C_{\rm ISS}$, and the $V_{\rm GS}$, for a 600-V, 2-A Si DMOSFET and a 900-V, 1-A SiC DiMOSFET, respectively. The measurements are performed with keeping $V_{\rm DS} = 0$ V to minimize the depletion region at the top of the n^--epitaxial layer ($C_{\rm gdj}$) and to neglect its influence in the equivalent capacitance. When $V_{\rm GS}$ is swept from -25 V to $+25$ V, the relationship between the capacitance characteristics and the device structure can be estimated.



(a) Si DMOSFET



(b) SiC DiMOSFET

Figure 4.8 Measured C-V_{GS} characteristics of power MOSFET.

When the applied voltage V_{GS} is lower than -5 V for a Si DMOSFET and -7 V for a SiC DiMOSFET, the capacitance holds a constant value. This is because the carrier accumulation occurs at the device channel in the top of the p well region. The C_c results in very large capacitance or disappears with conducting condition. Then,

the C_{GS} achieves their highest values. On the other hand, the inversion occurs at the top of the n^--epitaxial layer under the gate oxide as the negative V_{GS} attracts holes to the interface and constitutes depletion layer underneath. Then the C_{gdj} becomes very small. Thus, the C_{GD} achieves its lowest value.

When the applied voltage V_{GS} becomes higher than -5 V for the Si DMOSFET and -7 V for the SiC DiMOSFET, the C_{GS} begins to decrease and reaches to a minimum value. The minimum value occurs around $V_{\mathrm{GS}} = 3$ V for the Si DMOSFET and $=$ 1 V for the SiC DiMOSFET, because the holes in the p well are repelled from the surface. Thus, the depletion layer appears at the surface of the channel. The inversion at the channel begins to occur with increasing V_{GS} when V_{GS} exceeds 3 V for the Si DMOSFET and 1 V for the SiC DiMOSFET. The C_{GS} increases up to the threshold gate voltage V_{T} where the C_{c} disappears by channel conduction. At the same region of V_{GS}, the electrons are attracted to the top of the JFET region or the n^--epitaxial layer under the gate oxide. Thus, it induces the accumulation layer there, and increase of C_{gdj}. Then, the C_{GD} becomes large within -3 V $< V_{\mathrm{GS}} < 3$ V region for the Si DMOSFET and -5 V $< V_{\mathrm{GS}} < 5$ V for the SiC DiMOSFET. The V_{T} of the Si DMOSFET is 3.5 V and the V_{T} of the SiC DiMOSFET is 5.0 V, as shown in Fig. 4.3. The V_{T} from measured C-V characteristics corresponds to the V_{T} from the measured $\sqrt{I_{\mathrm{DS_{sat}}}}$-$V_{\mathrm{GS}}$ characteristics. In Fig. 4.4, when $V_{\mathrm{GS}} < V_{\mathrm{T}}$, the measured $\sqrt{I_{\mathrm{DS_{sat}}}}$ is kept around 0.1 $\mathrm{A}^{1/2}$. This does not imply the leakage current, but the residual error due to quantization of A/D converter in the curve tracer.

The channel conducts when the applied voltage V_{GS} becomes higher than the V_{T}. Then, the strong inversion of electrons occurs at the top of the p well region. The C_{GS} of the Si DMOSFET becomes abruptly large and saturates with increasing V_{GS}, but the C_{GS} of the SiC DiMOSFET becomes gradually large and hardly saturates due to V_{GS}. This non-saturable characteristics stem from the short channel effects [43]. The channel length of the SiC DiMOSFET is approximately equal to 0.75 μm. Thus, the channel resistance R_{ch} of the Si DMOSFET in Fig. 4.1(a) is much lower than that of the SiC DiMOSFET. At the same region of V_{GS}, the electrons are attracted to the surface of the JFET region and forms the accumulation layer when V_{DS} is lower than V_{GS}. The C_{GD} of the Si DMOSFET becomes abruptly small and saturates with

increasing V_{GS}, but the C_{GD} of the SiC DiMOSFET becomes gradually small and hardly saturates with increasing V_{GS}. The variation of the C_{GD} associates with the total of the parasitic resistance R_{JFET} and epitaxial resistance R_{epi}, which depend on the impurity concentration in n^--epitaxial layer [27] [44]. These resistances of the Si DMOSFET are higher than that of the SiC DiMOSFET, because the doped impurity concentration of Si DMOSFET is lower than that of SiC DiMOSFET [7,44]. The C_{GD} characteristics in Fig. 4.8 is validated for this facts.

As the results in Figs. 4.8(a) and (b), the C_{ISS} are obtained as the sum of C_{GS} and C_{GD}. In Fig. 4.8(b), the measured C_{ISS} is smaller than the sum of C_{GS} and C_{GD}. This can be attributed to the overlap area, between p well and n^--epitaxial layer, which appears through the strong inversion and the accumulation of electrons at the top of them individually. The difference of the C-V characteristics between the Si DMOSFET and the SiC DiMOSFET is explained by the short channel effects in SiC DiMOSFET and the doping density difference in the n^--epitaxial layer.

The model extracted parameters of C-V characteristics of power MOSFET are detailed in Tab. 4.1.

Table 4.1 Model extracted parameters for Si and SiC power MOSFETs.

Parameter	Si power MOSFET	SiC power MOSFET
β	1.1 A/V^2	0.055 A/V^2
V_T	3.5 V	5.0 V
λ	0.002 1/V	0.035 1/V
θ	0.046 1/V	0.025 1/V
C_{oxd}	293 pF	176 pF
$C_{GS}(0)$	304 pF	88 pF
$C_{GD}(0)$	98 pF	95 pF
$C_{DS}(0)$	228 pF	144 pF

4.2.4 Dynamic behavior of power MOSFET

The internal parasitic capacitances of the power MOSFET, which are shown in Fig. 4.1(a), mainly depend on the variable depletion capacitances and constant MOS layer capacitances in Fig. 4.1(b). The dynamic behavior of Si and SiC power MOSFET is governed by these capacitances that are the functions of the relative terminal voltages (V_{GS} and V_{DS}). The gate current I_{G} flowing through the input of power MOSFET is given by Eq. (4.6):

$$I_{\mathrm{G}} = \big(C_{\mathrm{GS}} + C_{\mathrm{GD}}\big)\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t} - C_{\mathrm{GD}}\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t}, \tag{4.6}$$

and the difference between drain current $I_{\mathrm{T}}(= I_{\mathrm{D}})$ and drain-source current I_{DS} is expressed by Eq. (4.7):

$$I_{\mathrm{T}} - I_{\mathrm{DS}} = \big(C_{\mathrm{DS}} + \frac{C_{\mathrm{GS}}C_{\mathrm{GD}}}{C_{\mathrm{GS}} + C_{\mathrm{GD}}}\big)\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t} - \frac{C_{\mathrm{GD}}}{C_{\mathrm{GS}} + C_{\mathrm{GD}}}I_{\mathrm{G}}. \tag{4.7}$$

Eventually, the dynamic behavior of Si and SiC power MOSFET is given by Eqs. (4.8) and (4.9) at charging/discharging these capacitances:

$$\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t} = \frac{I_{\mathrm{G}}}{C_{\mathrm{GS}} + C_{\mathrm{GD}}} + \frac{C_{\mathrm{GD}}}{C_{\mathrm{GS}} + C_{\mathrm{GD}}} \cdot \frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t}, \tag{4.8}$$

$$\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t} = \frac{I_{\mathrm{T}} - I_{\mathrm{DS}} + \frac{C_{\mathrm{GD}}}{C_{\mathrm{GS}}+C_{\mathrm{GD}}} \cdot I_{\mathrm{G}}}{C_{\mathrm{DS}} + \frac{C_{\mathrm{GS}}C_{\mathrm{GD}}}{C_{\mathrm{GS}}+C_{\mathrm{GD}}}}. \tag{4.9}$$

The depletion capacitance in gate-drain capacitance C_{GD} and drain-source capacitance C_{DS} is modeled by using the differential capacitance in Chapter 2.

4.3 Evaluation of switching response

The transient switching response of the Si and SiC power MOSFET is evaluated by the test circuit with a power supply, a load, and a gate drive circuit. The inductive load circuit is shown in Fig. 4.9. The state equations of the load circuit and gate drive circuit are given as Eqs. (4.10) and (4.11), respectively:

$$\frac{\mathrm{d}I_{\mathrm{D}}}{\mathrm{d}t} = \frac{1}{L_{\mathrm{L}}}\Big(V_{\mathrm{AA}} - R_{\mathrm{L}}I_{\mathrm{D}} - V_{\mathrm{DS}}\Big), \tag{4.10}$$

$$I_{\mathrm{G}} = \frac{V_{\mathrm{GG}} - V_{\mathrm{GS}}}{R_{\mathrm{G}}}, \tag{4.11}$$

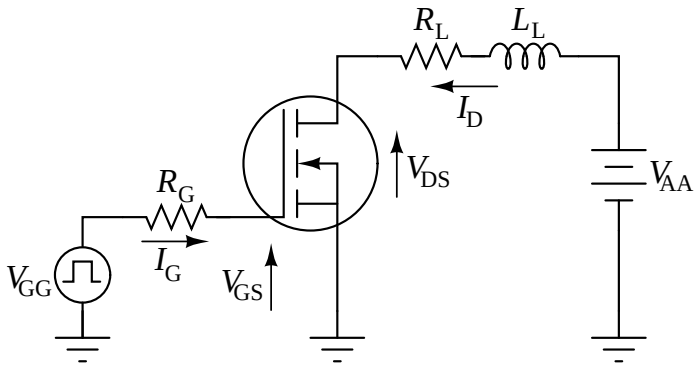


Figure 4.9 Inductive load circuit for measured switching characteristics of power MOSFET.

where I_D denotes the total current I_T, L_L the drain series inductance including parasitic, R_L the drain series resistance, V_{AA} the drain supply voltage, and V_{GG} the gate pulse generator voltage.

The state equations in Eqs. (4.8) and (4.9) of the power MOSFET can be solved simultaneously with state equations in Eqs. (4.10) and (4.11) of the load circuit.

Figures 4.10-4.13 show both simulated and measured waveforms of the Si power MOSFET at turn-on and turn-off. Figures 4.14-4.17 also show both simulated and measured waveforms of the SiC power MOSFET at turn-on and turn-off. The drain supply voltage V_{AA} is set at 100 V. The drain series inductance including parasitic L_L is 200 nH, and the drain series resistance R_L is 103 Ω. The gate pulse generator voltage V_{GG} is set at 20 V. The gate series resistance R_G is varied to provide different turn-on and turn-off speed for the Si and SiC power MOSFET by 10 Ω, 51 Ω, 100 Ω, and 200 Ω.

The turn-on process begins with the gate drive circuit when the gate drive voltage rises up to 20 V. Gate current I_G immediately begins to flow as the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} are charged passing through the gate series resistance R_G. When gate-source voltage V_{GS} increases to the threshold voltage V_T, the drain current I_D begins to increase and the drain-source voltage V_{DS} also begins to decrease to $I_D R_{DSon}$. The simulated and measured turn-on responses of I_G and V_{GS} are shown in Fig. 4.10 for Si power MOSFET and Fig. 4.14 for SiC power MOSFET. The

SiC power MOSFET shows faster turn-on speed of measured V_{GS} than the Si power MOSFET. Because the SiC power MOSFET has smaller the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} than the Si power MOSFET, as shown in Fig. 4.8. On the other hand, The simulated and measured turn-on responses of I_D and V_{DS} are shown in Fig. 4.11 for Si power MOSFET and Fig. 4.15 for SiC power MOSFET. The turn-on speed of V_{DS} between the SiC power MOSFET and the Si power MOSFET is slightly different, because the gate-drain capacitance C_{GD} and drain-source capacitance C_{DS} of the Si and SiC power MOSFETs respectively shown in Figs. 4.6 and 4.7 are rather same values.

Additionally, the turn-off process begins when the gate drive voltage falls to 0 V. The gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} are discharged with the gate current I_G passing through the gate series resistance R_G. Once gate-source voltage V_{GS} decreases to the threshold voltage V_T, the drain current I_D begins to decrease and the drain-source voltage V_{DS} also begins to increase to the drain voltage supply V_{AA}. The simulated and measured turn-off responses of I_G and V_{GS} are shown in Fig. 4.12 for Si power MOSFET and Fig. 4.16 for SiC power MOSFET. And also, the SiC power MOSFET shows faster turn-off speed of measured V_{GS} than the Si power MOSFET. Because the SiC power MOSFET has smaller the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} than the Si power MOSFET, as shown in Fig. 4.8. On the other hand, The simulated and measured turn-off responses of I_D and V_{DS} are shown in Fig. 4.13 for Si power MOSFET and Fig. 4.17 for SiC power MOSFET. The turn-off speed of V_{DS} between the SiC power MOSFET and the Si power MOSFET is slightly different, because the gate-drain capacitance C_{GD} and drain-source capacitance C_{DS} of the Si and SiC power MOSFETs respectively shown in Figs. 4.6 and 4.7 are rather same values. But the SiC power MOSFET has smaller delay time of I_D and V_{DS} than the Si power MOSFET during turn-off, when the gate series resistance R_G increases. Because the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} of the SiC power MOSFET in Fig. 4.8(b) are less than that of the Si power MOSFET in Fig. 4.8(a).

At small gate series resistance R_G about 10 Ω, the measured current and voltage oscillate due to the resonance between parasitic inductances of wiring and internal

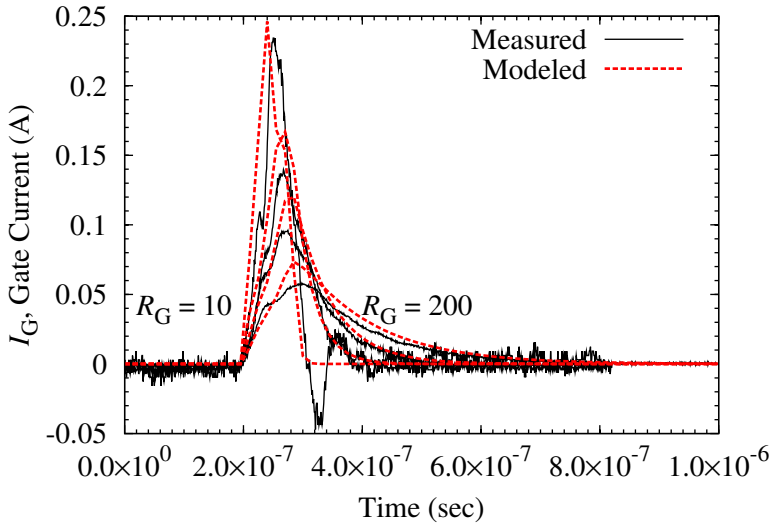
parasitic capacitances. There are differences between the simulated results through the model and the measured results for the gate current I_{G} and gate-source voltage V_{GS}, especially at turn-off of Si and SiC power MOSFET with high gate series resistance R_{G}. When gate series resistance R_{G} increases, the measured I_{G}, V_{GS}, and I_{D} become smooth waveforms. Because time constant increasingly associated with the gate series resistance R_{G} increase. Thereby, the responses of all of the current and voltage are not affected by parasitic components. Therefore, the current and voltage show the well correspondence with measured results. In this case, the simulated results cannot show the oscillation of the current and voltage at small gate series resistance R_{G} because its parasitic gate inductance L_{G} in the gate drive circuit are neglected.

The SiC power MOSFET shows faster turn-off speed than the Si power MOSFET. Because the SiC power MOSFET has smaller C_{GS}, C_{GD}, and C_{DS} than the Si power MOSFET as shown in Fig. 4.6 and 4.7 for Si power MOSFET and SiC power MOSFET, respectively. And also, the rise time and fall time of current and voltage for Si and SiC power MOSFET increase when R_{G} increases.

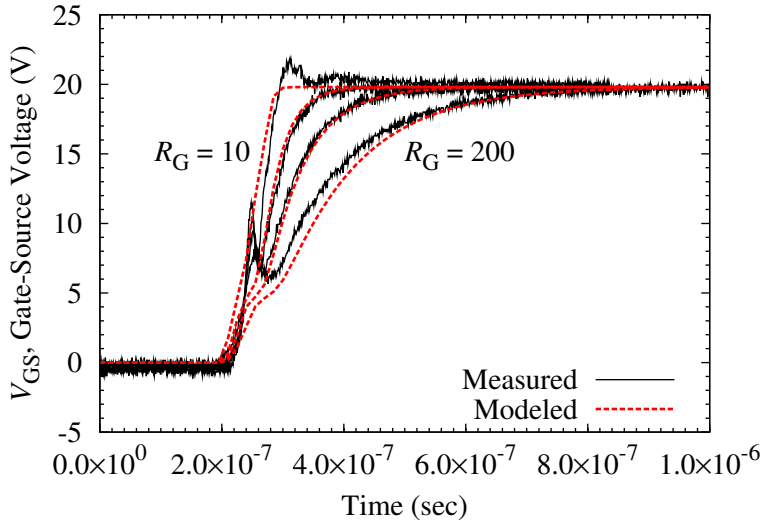
4.4 Summary

In order to predict the device characteristics of Si and SiC power MOSFET accurately over their wide range of operation, a physics-based model was studied and proposed based on terminal capacitances. This chapter also discussed the parameter extraction for the model and the I-V characteristics for model with precisely measured C-V characteristics of Si and SiC power MOSFETs. It was shown that the simulated results of the switching behavior well agree with the experimental results for some conditions of the model and extracted parameters.

In addition, this chapter characterized and discussed the switching characteristics of power MOSFETs through the voltage dependency of terminal capacitances. The difference between the switching characteristics of the Si and SiC power MOSFETs depends on their internal parasitic capacitances, which can be classified by the MOS capacitance and pn junction capacitance.

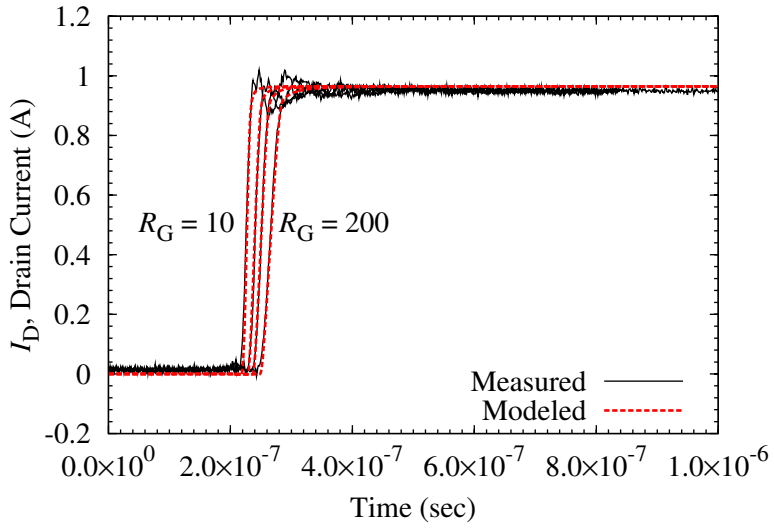


(a) I_{G} current

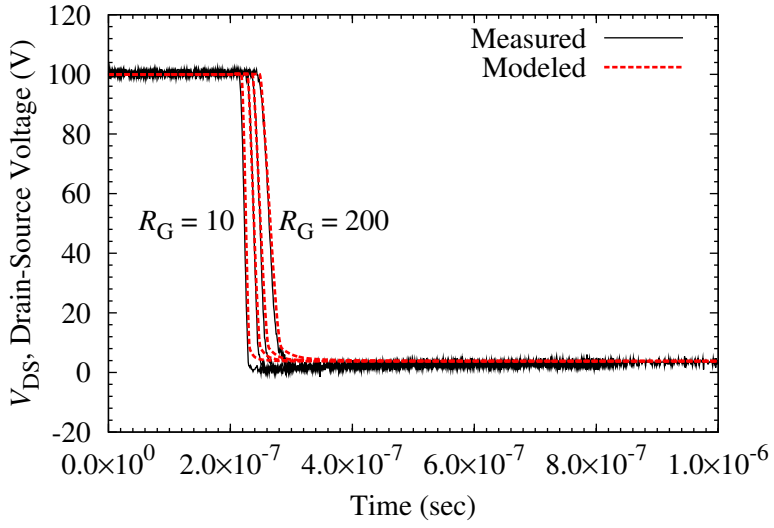


(b) V_{GS} voltage

Figure 4.10 Measured and simulated turn-on response of I_{G} and V_{GS} for Si power MOSFET as a function of gate series resistance.

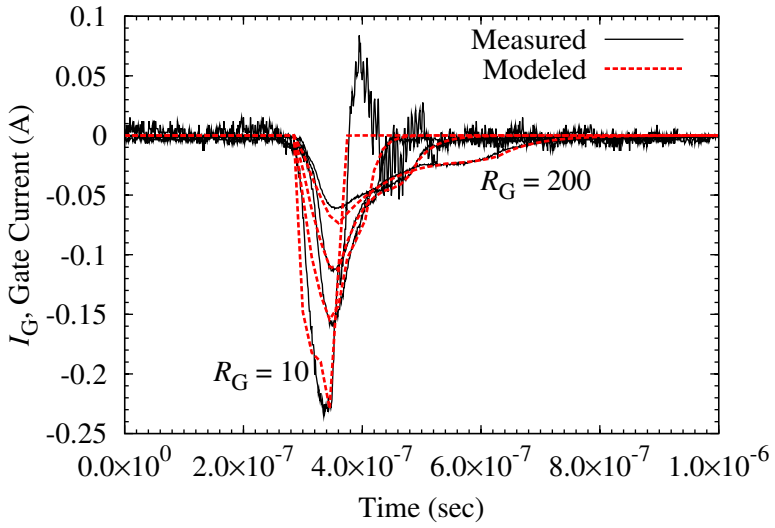


(a) I_D current

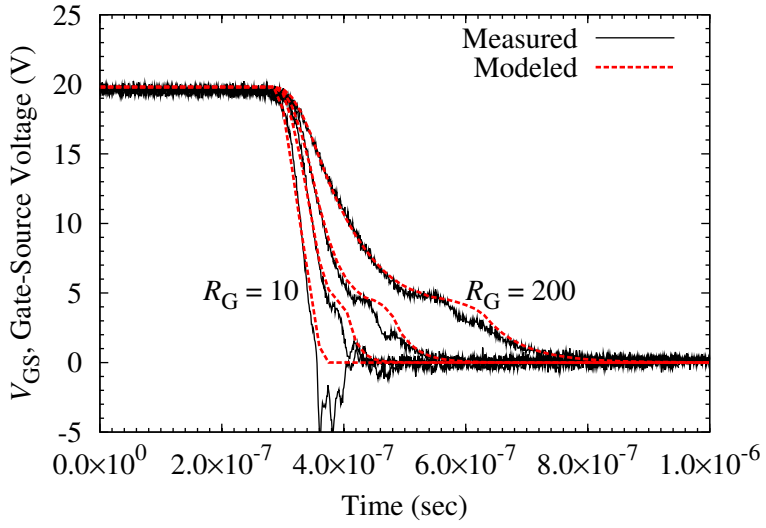


(b) V_{DS} voltage

Figure 4.11 Measured and simulated turn-on response of I_D and V_{DS} for Si power MOSFET as a function of gate series resistance.

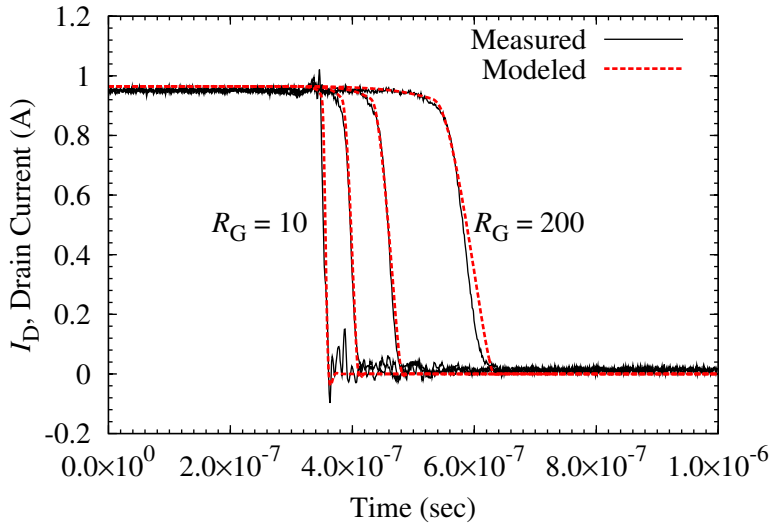


(a)

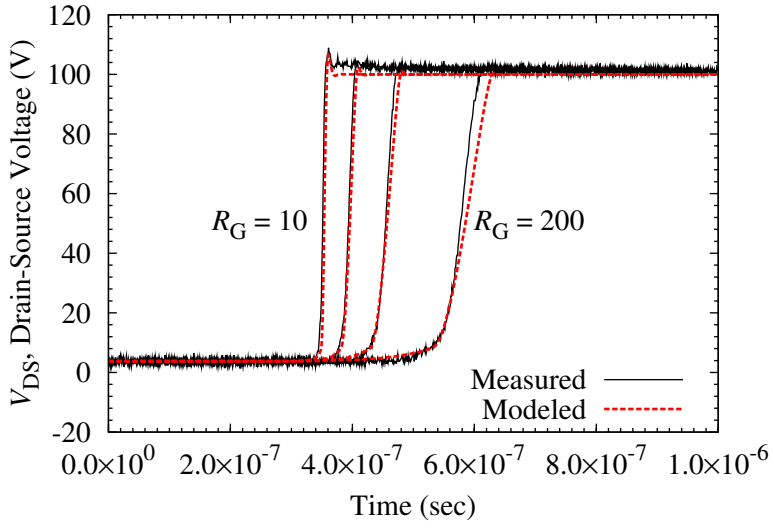


(b)

Figure 4.12 Measured and simulated turn-off response of I_G and V_{GS} for Si power MOSFET as a function of gate series resistance.

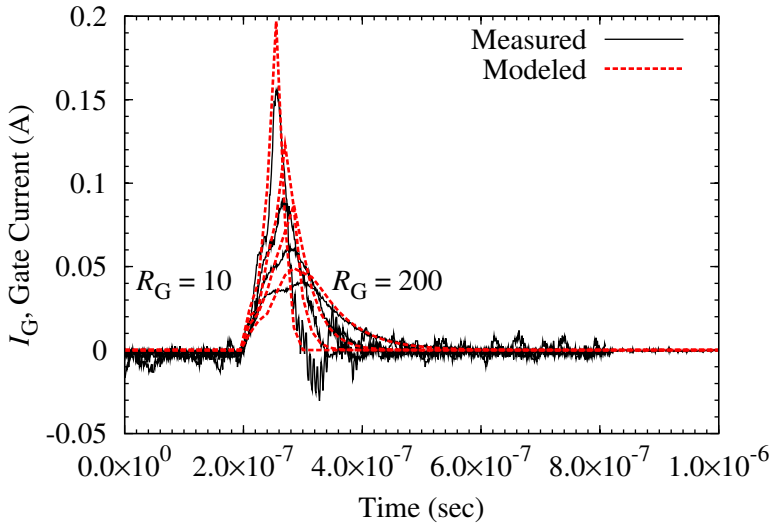


(a)I_{D} current

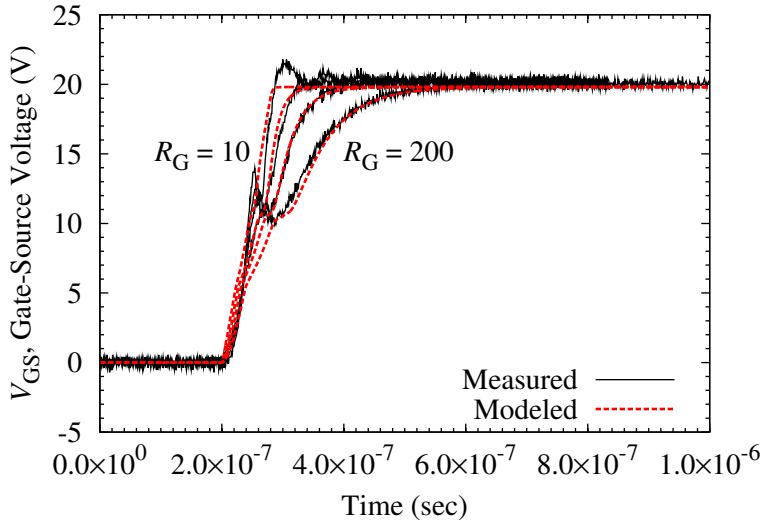


(b) V_{DS} voltage

Figure 4.13 Measured and simulated turn-off response of I_{D} and V_{DS} for Si power MOSFET as a function of gate series resistance.

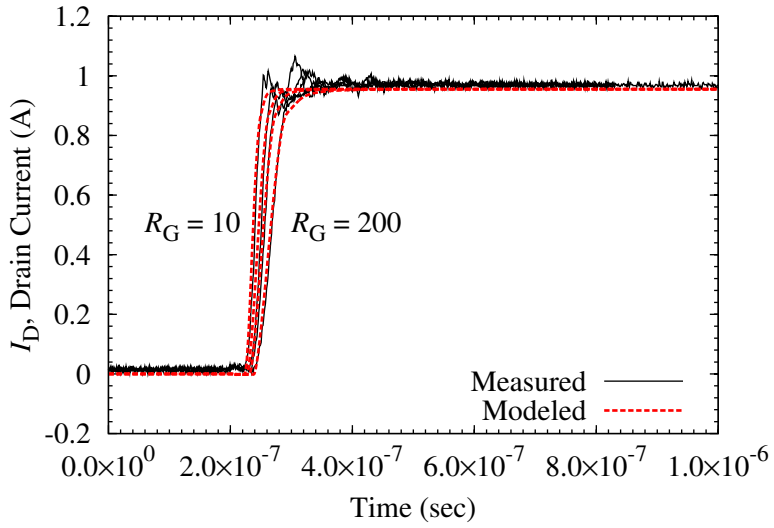


(a) I_G current

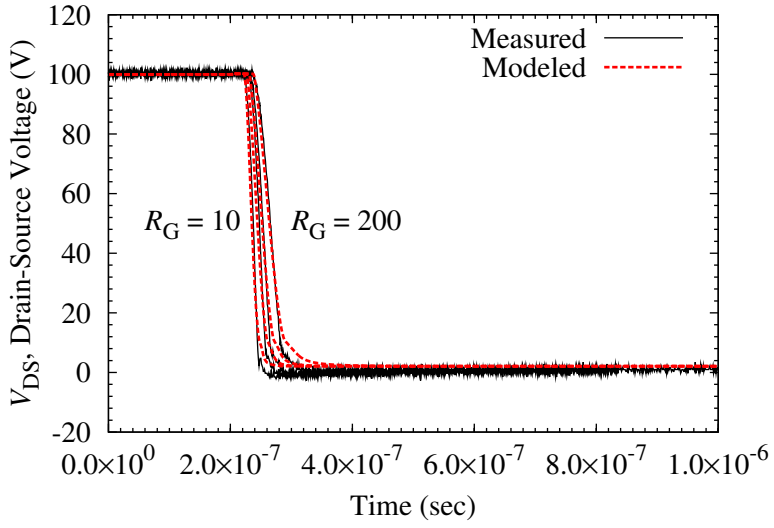


(b) V_{GS} voltage

Figure 4.14 Measured and simulated turn-on response of I_G and V_{GS} for SiC power MOSFET as a function of gate series resistance.

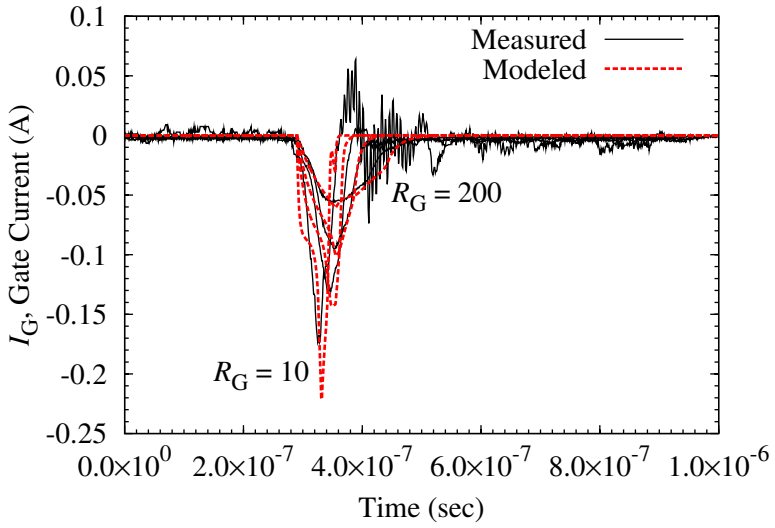


(a) I_D current

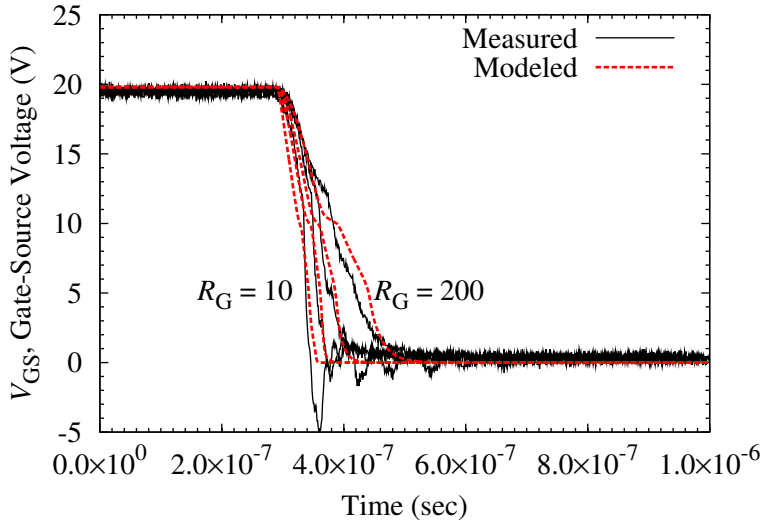


(b) V_{DS} voltage

Figure 4.15 Measured and simulated turn-on response of I_D and V_{DS} for SiC power MOSFET as a function of gate series resistance.

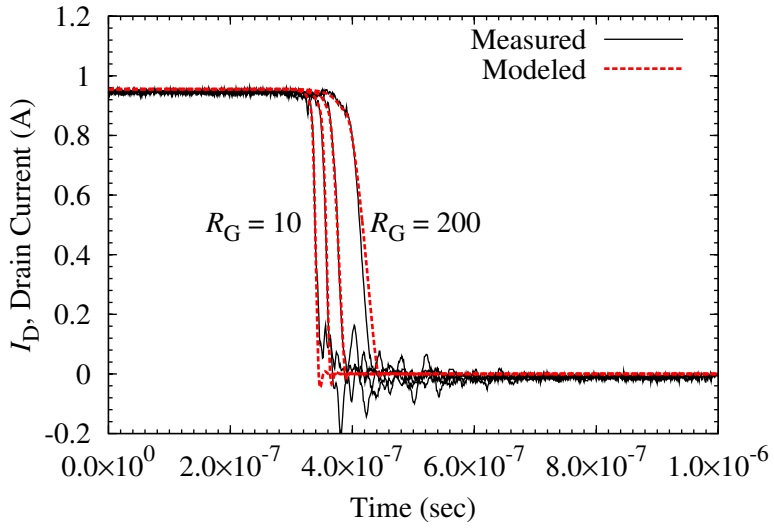


(a) I_G current

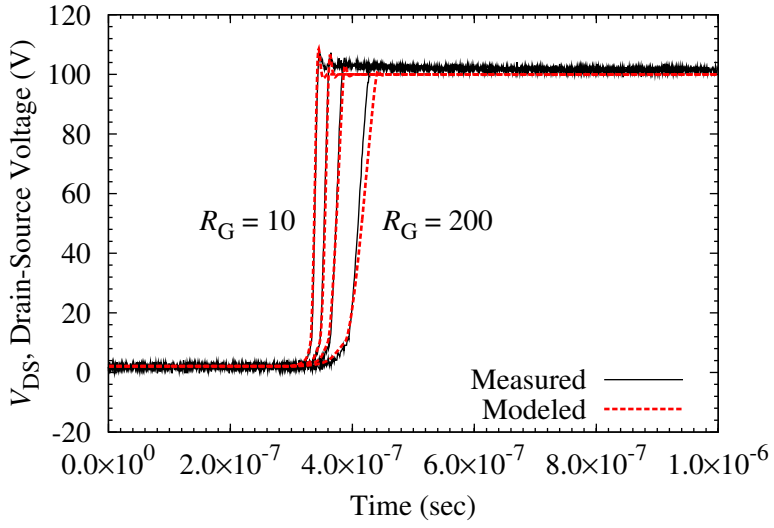


(b) V_{GS} voltage

Figure 4.16 Measured and simulated turn-off response of I_G and V_{GS} for SiC power MOSFET as a function of gate series resistance.



(a) I_{D} current



(b) V_{DS} voltage

Figure 4.17 Measured and simulated turn-off response of I_{D} and V_{DS} for SiC power MOSFET as a function of gate series resistance.

Chapter 5

Characterization of SiC JFET

5.1 Introduction

Recently, SiC-based semiconductor power devices are strongly expected to replace Si power devices at high-temperature, high switching frequency, and high voltage application [1]. Among the devices, transistors are the most possible power switches for power conversions. Several types of SiC-based transistors have been proposed and developed. Junction field-effect transistor (JFET) is preferred for its low on-resistance R_{DSon} and ruggedness in harsh environments. Lateral-type and vertical-type SiC JFETs [21, 60, 66] have been developed. Their structures have shown the normally-on characteristics for a long time, but recently the normally-off type devices were developed. In this dissertation, both types are under test experimentally. However, low on-resistance R_{DSon} characteristics of JFET are violated by achieving normally-off characteristics. Then, the SiC JFETs discussed in this study are limited in normally-on type devices.

The switching behavior of actual power devices is far from ideal. The non-ideal characteristics of SiC device affect on the performance of power conversion circuits, especially at high switching frequency. Then, the characteristics of the devices must be clarified and evaluated in advance of the design of power conversion circuits. Here, the switching characteristics of two different types SiC JFETs are discussed with relation to their internal parasitic capacitances, drain-source current I_{DS}, drain current

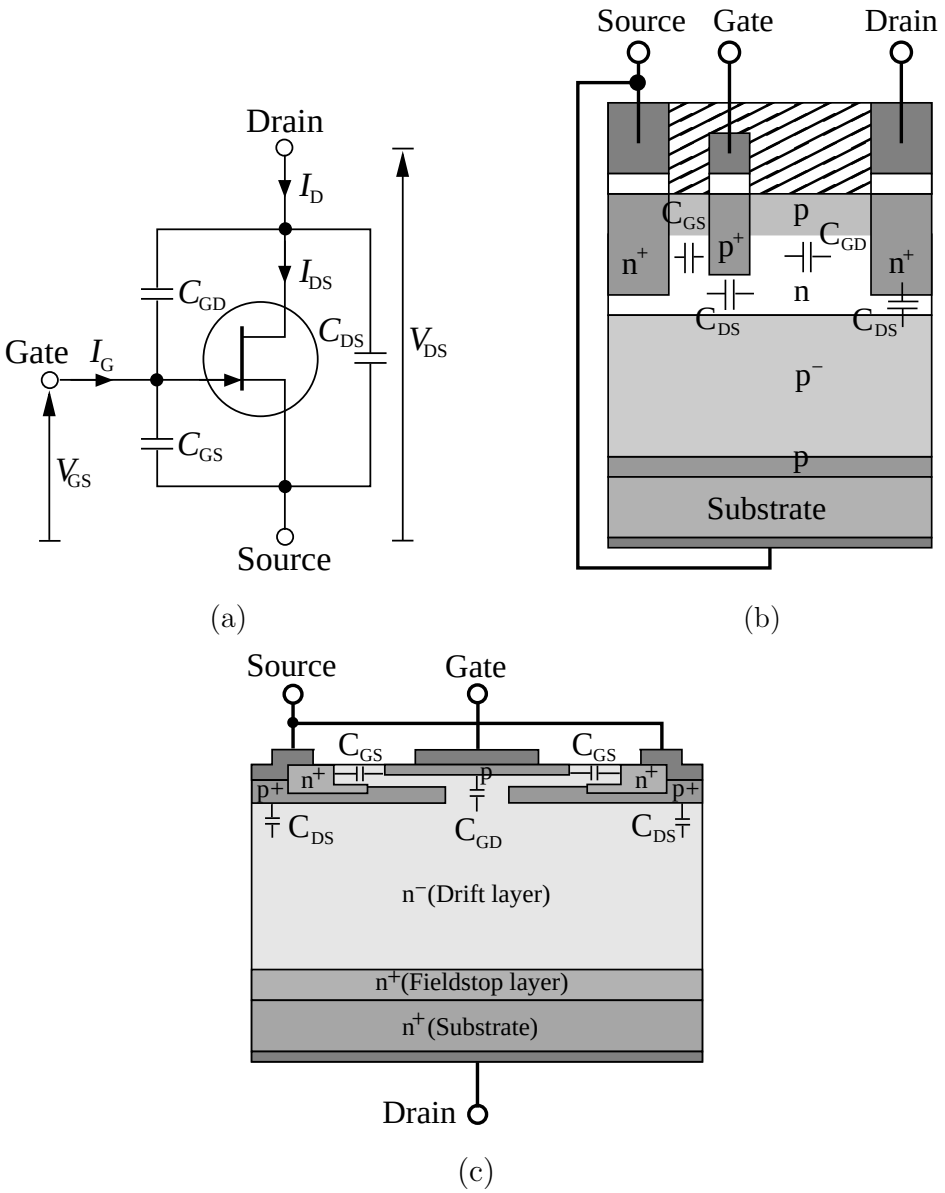


Figure 5.1 (a) Equivalent parasitic terminal capacitances of JFET, (b) Cross section of lateral-type SiC JFET cell, and (c) Cross section of vertical-type SiC JFET cell.

I_D, gate current I_G, gate-source voltage V_{GS}, and drain-source voltage V_{DS}. Their definitions are shown in Fig. 5.1(a). The parasitic capacitances in FET, which are shown in Figs. 5.1(b) and (c), are composed of gate-source capacitance C_{GS}, gate-drain capacitance C_{GD}, and drain-source capacitance C_{DS}. C_{GS} and C_{GD} constitute the input

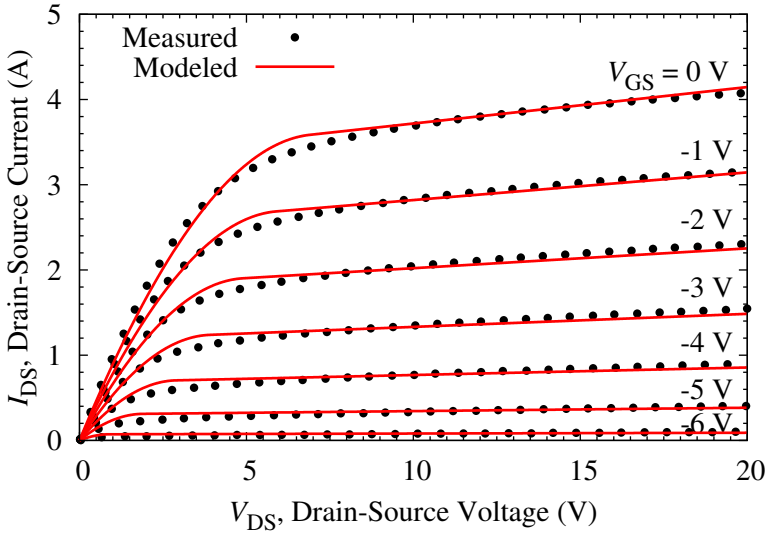
capacitance $C_{\mathrm{ISS}}(= C_{\mathrm{GS}} + C_{\mathrm{GD}})$, which is charged and discharged by the gate drive circuit for switching operation. C_{GD} is also equivalent to the reverse transfer capacitance C_{RSS}. The effective capacitance is multiplied by the voltage gain of the FET in switching operation by Miller effect. Also, $C_{\mathrm{GD}}(= C_{\mathrm{RSS}})$ and C_{DS} constitute the output capacitance $C_{\mathrm{OSS}}(= C_{\mathrm{GD}} + C_{\mathrm{DS}})$, which is charged and discharged by the load current and governs the switching speed. Major part of these effective capacitance is originated from the junction capacitances in the semiconductor, which vary in accordance with the applied voltage. Therefore, the characteristics of terminal capacitances are substantial for understanding the switching behavior.

A model of semiconductor device is indispensable for evaluating the voltage and current response at switching in circuit simulation and estimating the system performance in their applications. The dynamics at the transient state are obviously governed by these characteristics of devices.

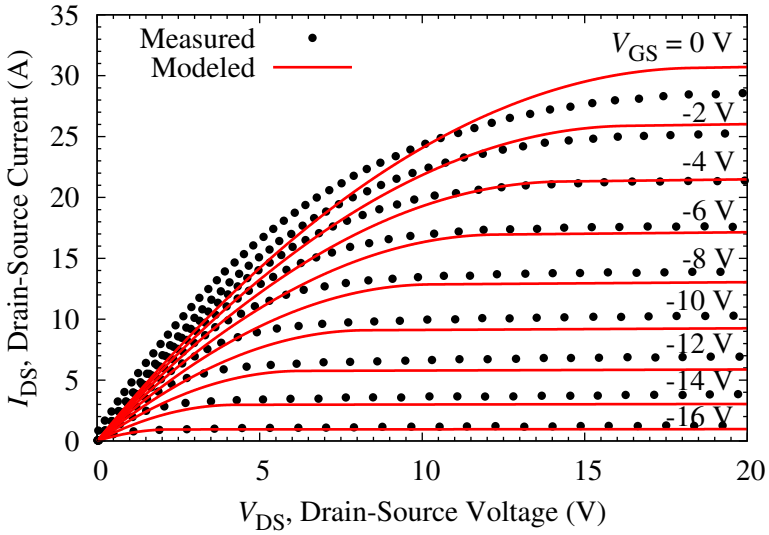
This chapter characterizes the static I-V characteristics and the voltage dependency of terminal capacitances of SiC JFETs at first, then the switching behaviors are experimentally evaluated. Next, we discuss the C-V and switching characteristics based on their device structures and the semiconductor physics. In the end, the simulated switching behaviors of both SiC JFETs are validated with the experimental results.

5.2 Characterization of SiC JFET devices

The details of the studied lateral-type and vertical-type SiC JFETs were explained in Chapter 2. In this section, the characterizations of both SiC JFETs are figured out under room temperature. The static I-V characteristics for the forward conduction condition were measured as the dc characteristics using IWATSU IE-1198 curve tracer. The C-V characteristics for the reverse non-conducting condition were measured as the ac characteristics by the capacitance measurement system in Chapter 3.



(a) Lateral-type



(a) Vertical-type

Figure 5.2 Static I-V characteristics of SiC JFET.

5.2.1 Static I-V characteristics

Figures 5.2(a) and (b) show the measured and modeled static I-V characteristics of lateral-type SiC JFET and vertical-type SiC JFET, respectively, for different values of gate-source voltage V_{GS}. The steady-state forward I-V characteristics of both SiC JFETs are drawn by pentode like curves to the gate-source voltage V_{GS}. The relation-

ship between the drain-source current I_{DS} and the drain-source voltage V_{DS} is modeled at the steady-state as a function of V_{GS} and V_{DS}. The both of SiC JFETs studied in this chapter are the normally-on type devices, so that I_{DS} flows at $V_{\mathrm{GS}} = 0$ V. The static I-V characteristics of both SiC JFETs in unipolar operation can be expressed by Eq. (5.1) [32, 65, 67]:

$$I_{\mathrm{DS}} \cong \begin{cases} \dfrac{\beta}{2(1+\theta(V_{\mathrm{GS}}-V_{\mathrm{T}}))}\left[2(V_{\mathrm{GS}}-V_{\mathrm{T}})V_{\mathrm{DS}} - V_{\mathrm{DS}}^2\right](1+\lambda V_{\mathrm{DS}}) \\ \qquad \text{for } V_{\mathrm{DS}} \leq V_{\mathrm{GS}} - V_{\mathrm{T}}, \\ \dfrac{\beta}{2(1+\theta(V_{\mathrm{GS}}-V_{\mathrm{T}}))}(V_{\mathrm{GS}}-V_{\mathrm{T}})^2(1+\lambda V_{\mathrm{DS}}) \\ \qquad \text{for } V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{T}}. \end{cases} \tag{5.1}$$

Here, β denotes the JFET channel transconductance, V_{T} the threshold voltage, λ the channel length modulation factor, and θ the mobility modulation coefficient. In this model, the effect of drain resistance R_{D} and source resistance R_{S} is neglected.

These four parameters used in Eq. (5.1) can be extracted from the measurement results. The threshold voltage V_{T} and JFET channel transconductance β are determined in advance to extracting the channel length modulation factor λ from the measured data as shown in Figs. 5.3 and 5.4 for lateral-type SiC JFET and vertical-type SiC

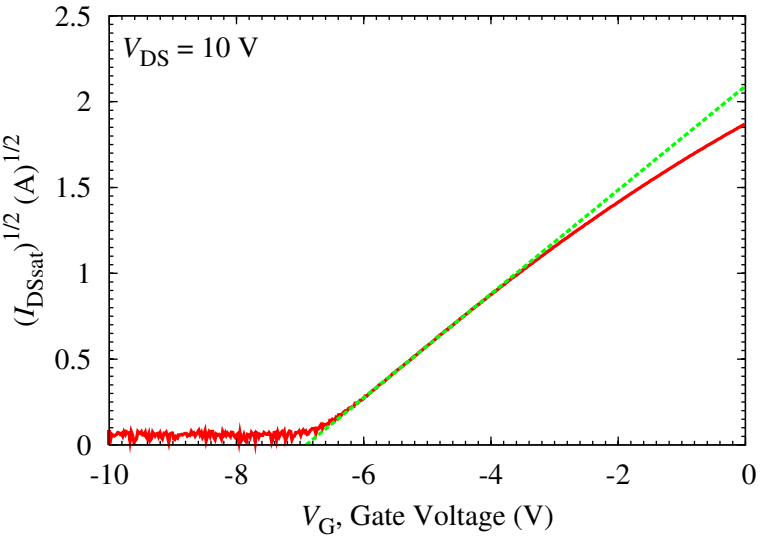


Figure 5.3 Measured $\sqrt{I_{\mathrm{DS_{sat}}}}$-$V_{\mathrm{GS}}$ characteristics of lateral-type SiC JFET.

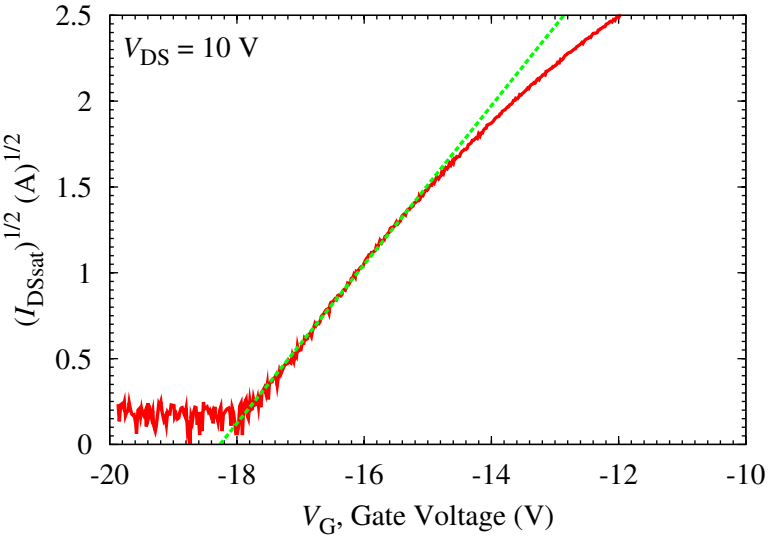


Figure 5.4 Measured $\sqrt{I_{DS_{sat}}}$-V_{GS} characteristics of vertical-type SiC JFET.

Table 5.1 Model extracted parameters for static I-V characteristics of both SiC JFETs.

Parameter	Lateral-type SiC JFET	Vertical-type SiC JFET
β	0.184 A/V^2	0.428 A/V^2
V_T	-6.9 V	-18.3 V
λ	0.013 1/V	0.0015 1/V
θ	0.048 1/V	0.077 1/V

JFET, respectively. The model extracted parameters for static I-V characteristics of both SiC JFETs are shown in Tab. 5.1.

5.2.2 C-V characteristics

The depletion region formed at pn junction behaves as parasitic capacitances, which are lumped into terminal capacitances C_{GS}, C_{GD}, and C_{DS}, as depicted in Fig. 5.1(a). The thickness of depletion region changes with the applied reverse bias voltage V_R (V_{GS} and V_{DS}). The dependence of the depletion capacitance on the V_R can be expressed in

the following compact form by Eq. (2.59) [29, 60, 65] in Chapter 2.

Both SiC JFETs are limited to the normally-on type as mentioned above. The lateral-type SiC JFET has 0.006×60-mm in RESURF and 0.36 mm^2 active area with 200 V blocking voltage and the rated 5 A drain current. The vertical-type SiC JFET has 2.32×2.32-mm in die size and 4 mm^2 active area with 900 V blocking voltage and the rated 2.5 A drain current.

In the experimental setup for characterization, the C-V characteristics of both devices are precisely measured by a LCR meter with applying dc bias voltages V_{GS} and V_{DS} to the devices, through C-V measurement fixture in Chapter 3. The measurements are performed with applying $V_{\mathrm{DS}} = 0$ V to avoid short circuit current for V_{GS} dependency, and $V_{\mathrm{GS}} = -20$ V to block the channel of devices for V_{DS} dependency. For characterizing the V_{GS} dependency, V_{GS} is swept from 0 V to -20 V for both SiC JFETs. For the measurement of V_{DS} dependency, V_{DS} is swept from 0 V to 200 V for lateral-type and from 0 V to 600 V for vertical-type.

5.2.3 Switching characteristics

The switching behaviors of both SiC JFETs are governed by the parasitic terminal capacitances (Fig. 5.1(a)) [28–30], which are the functions of the applied voltages between terminals. Eventually, the transient behavior of terminal voltages for both SiC JFETs can be represented by Eqs. (5.2) and (5.3) at charging/discharging states of the capacitances. When $V_{\mathrm{GS}} > V_{\mathrm{T}}$, JFET is conducting, then, $\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t} \approx 0$. V_{GS} changes as follows

$$\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t} \cong -\frac{V_{\mathrm{GS}} - V_{\mathrm{GG}}}{R_{\mathrm{G}}\big(C_{\mathrm{GS}}(V_{\mathrm{GS}}) + C_{\mathrm{GD}}(V_{\mathrm{GS}})\big)}. \tag{5.2}$$

When $V_{\mathrm{GS}} < V_{\mathrm{T}}$, JFET is blocked, V_{DS} is built up as follows

$$\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t} \cong -\frac{V_{\mathrm{DS}} - V_{\mathrm{AA}}}{R_{\mathrm{L}}\big(C_{\mathrm{GD}}(V_{\mathrm{DS}}) + C_{\mathrm{DS}}(V_{\mathrm{DS}})\big)}. \tag{5.3}$$

The switching behaviors of both devices are evaluated with the inductive load circuit, which is shown in Fig. 5.5. Then V_{DS}, V_{GS}, and I_{D} are measured in the experiments. V_{AA} is varied with setting three different V_{DS} at 25 V, 50 V, and 75 V.

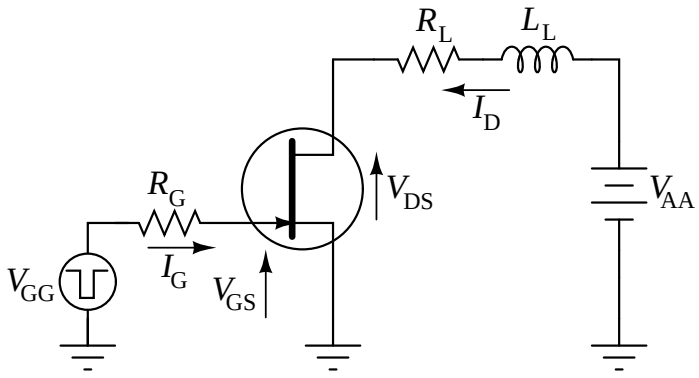


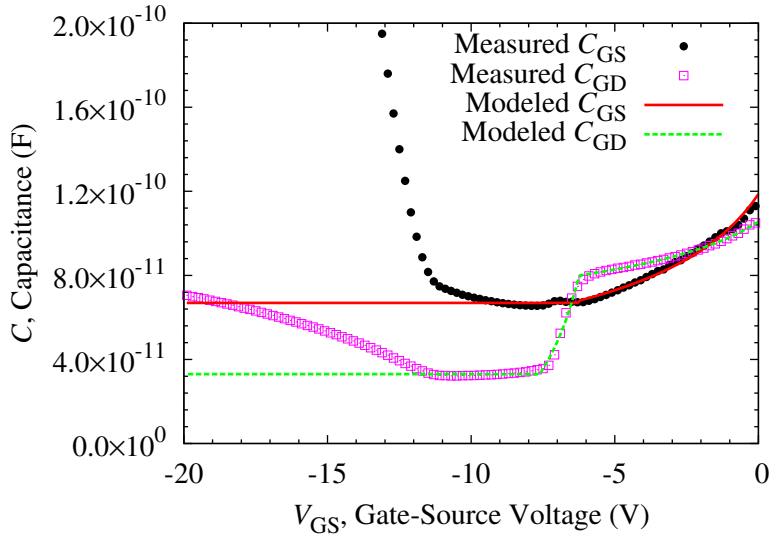
Figure 5.5 Inductive load circuit for measured switching characteristics of SiC JFET.

Here, L_L is set at 200 nH and R_L at 103 Ω. V_{GG} applied to the gate of JFET through R_G 5 Ω is switched between 0 V and −20 V.

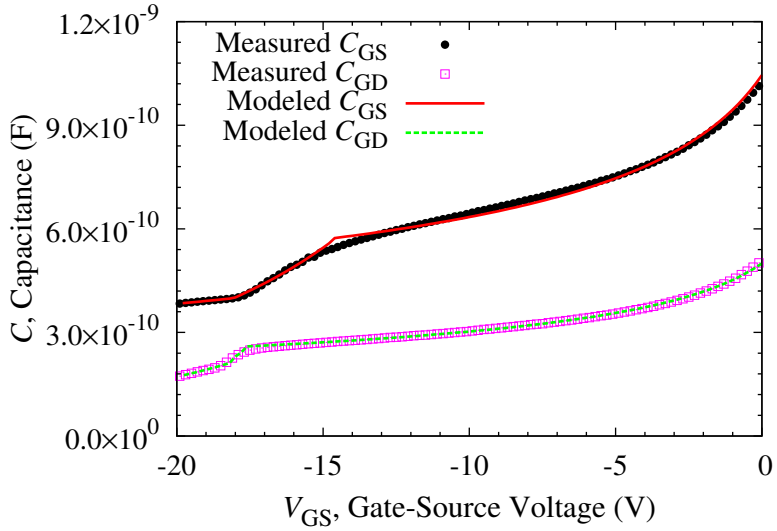
5.3 Results of C-V and switching characteristics of SiC JFETs

5.3.1 C-V characteristics

The measured and modeled C-V_{GS} characteristics are shown for both SiC JFETs in Figs. 5.6(a) and (b). C_{GS} and C_{GD} decrease with negative V_{GS}, because the depletion region expands in the n-region facing at p^+ gate in Fig. 5.1(b) and the n^--drift region facing at p gate in Fig. 5.1(c). Then, C_{GS} and C_{GD} become constant around 66 pF and 33 pF for lateral-type, respectively. They become 400 pF and 200 pF for vertical-type, respectively. Because the channel area is fully depleted for $V_{GS} < V_T$ (cut-off condition). The V_T is approximately equal to −6.9 V for lateral-type and −18.3 V for vertical-type. C_{GS} and C_{GD} of lateral-type increase for $V_{GS} < -11.3$ V as shown in Fig. 5.6(a). They stem from the leakage current at pn junction between gate and source. The capacitance model parameters of C_{GS} and C_{GD} are extracted for V_{GS} higher than cut-off voltage to neglect the influence of leakage current. They are $C_0 = 119$ pF, $m = 0.48$ (uniformly doped) and $C_0 = 106$ pF, $m = 0.24$ (linearly graded doped) for



(a) Lateral-type

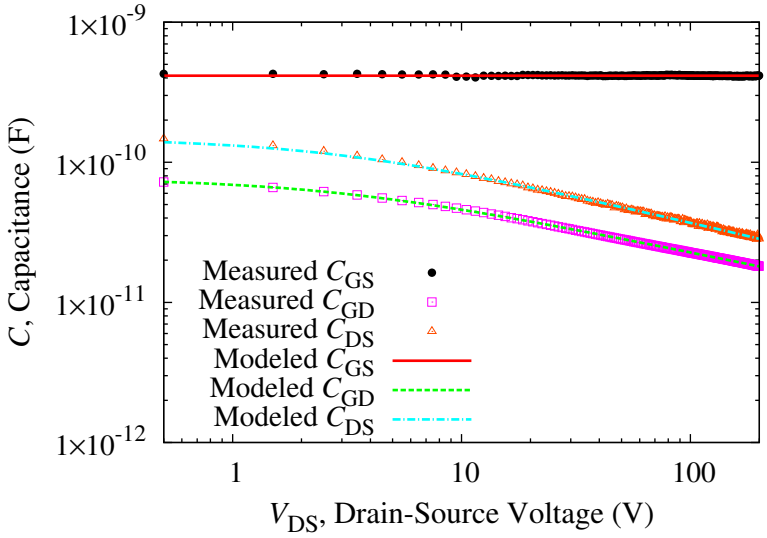


(b) Vertical-type

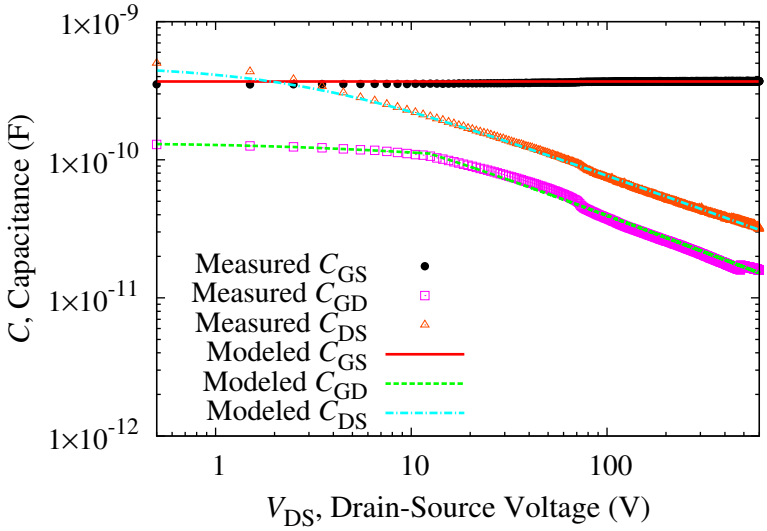
Figure 5.6 C-V_{GS} characteristics of SiC JFETs.

lateral-type, respectively. They are $C_0 = 1045$ pF, $m = 0.33$ (linearly graded doped) and $C_0 = 500$ pF, $m = 0.33$ (linearly graded doped) for vertical-type, respectively.

The measured and modeled C-V_{DS} characteristics for both SiC JFETs are shown in Figs. 5.7(a) and (b). C_{GS} hardly changes with the variation of V_{DS}. The values are around 415 pF for lateral-type and 368 pF for vertical-type. Because the electric



(a) Lateral-type



(b) Vertical-type

Figure 5.7 C-V_{DS} characteristics of SiC JFETs.

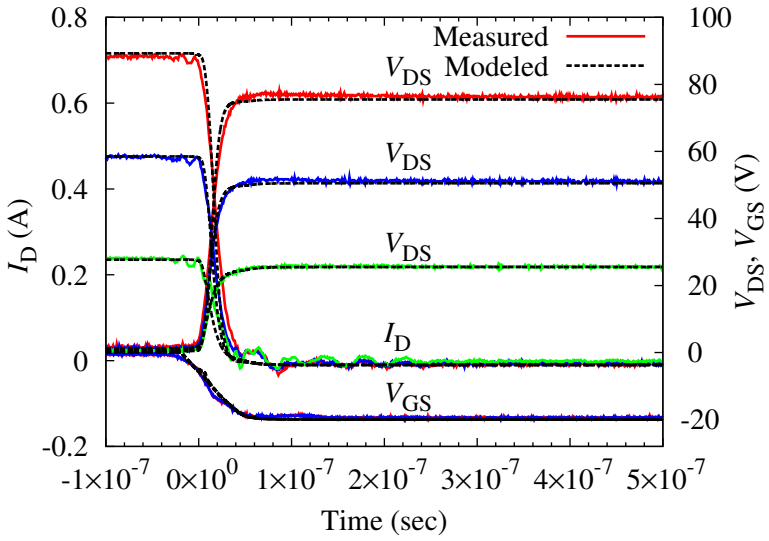
fields induced by V_{DS} does not affect on the electric field across gate and source due to the fixed V_{GS}. On the other hand, C_{GD} and C_{DS} decrease smoothly according to the increase of V_{DS}. The extracted capacitance model parameters of C_{GD} and C_{DS} are $C_0 = 77$ pF, $m = 0.34$ (linearly graded doped) and $C_0 = 148$ pF, $m = 0.38$ (linearly graded doped) for lateral-type, respectively. They are $C_0 = 278$ pF, $m = 0.55$

(uniformly doped) and C_0 = 481 pF, m = 0.52 (uniformly doped) for vertical-type, respectively. For the lateral-type in Fig. 5.1(b), C_{GD} and C_{DS} change slightly with the variation of V_{DS}, because the depletion region expands from the linearly graded doped n-region to p^+ gate and n-region to p^- region, respectively. For the vertical-type in Fig. 5.1(c), the n-channel is aligned in horizontal-axis, but the n-type semiconductor (n^- drift region) is aligned in vertical-axis. Therefore, C_{GD} has almost constant around 132 pF at $V_{DS} \leq 13$ V, because the depletion region expands around channel opened between buried p^+ region for low V_{DS}. Then, C_{GD} changes substantially with the variation of V_{DS} when $V_{DS} > 13$ V, because the depletion region expands from the p gate to the uniformly doped drift region. C_{DS} also changes substantially with the variation of V_{DS} in the low and high voltage ranges. It is because the depletion region expands from under the buried p^+ region to the uniformly doped drift region.

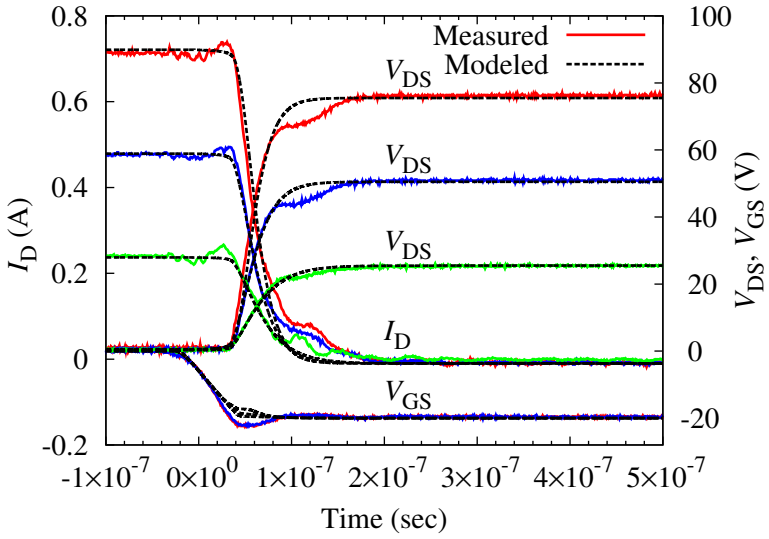
5.3.2 Switching characteristics

Figures 5.8(a) and (b) demonstrate the switching behaviors of both SiC JFETs for turn-off operation. Derivative of the V_{GS}, $\frac{dV_{GS}}{dt}$, in Eq. (5.2) obviously depends on $C_{ISS}(= C_{GS} + C_{GD})$ with variation of V_{GS}. The derivative of the V_{GS}, $\frac{dV_{GS}}{dt}$, is equal to -2.83×10^8 V/s (modeled) and -2.50×10^8 V/s (measured) for lateral-type in Fig. 5.8(a). It is also -3.14×10^8 V/s (modeled) and -3.59×10^8 V/s (measured) for vertical-type in Fig. 5.8(b). The simulated results by the model well coincide with experimental results. The lateral-type has smaller the derivative of the V_{GS}, $\frac{dV_{GS}}{dt}$, than the vertical-type. Because C_{GS} and C_{GD} of lateral-type SiC JFET increase substantially for $V_{GS} < -11.3$ V as mentioned above. The accumulated charge Q calculated from gate voltage dependency of capacitance is equal to 6.79 nC for lateral-type in Fig. 5.6(a) and 19.15 nC for vertical-type in Fig. 5.6(b). The lateral-type has smaller Q than the vertical-type. Because the lateral-type device has smaller C_{GS} and C_{GD} than the vertical-type while $V_{GS} \geq -11.3$ V.

Derivative of the V_{DS}, $\frac{dV_{DS}}{dt}$, in Eq. (5.3) depends on $C_{OSS}(= C_{GD} + C_{DS})$ with variation of V_{DS}. It affects on the switching behaviors when $V_{GS} < V_T$ (cut-off condition). It is obvious that Eqs. (5.2) and (5.3) cannot take the Miller effect into account. The



(a) Lateral-type



(b) Vertical-type

Figure 5.8 Switching characteristics of SiC JFET during turn-off.

derivatives of the V_{DS}, $\frac{dV_{DS}}{dt}$ for lateral-type in Fig. 5.8(a) at V_{DS} = 25 V, 50 V, and 75 V correspond to 7.89×10^8 V/s, 20.42×10^8 V/s, and 33.67×10^8 V/s by the model. They are 8.00×10^8 V/s, 17.06×10^8 V/s, and 23.88×10^8 V/s in the measurement. The derivatives of the V_{DS}, $\frac{dV_{DS}}{dt}$, for vertical-type in Fig. 5.8(b) at V_{DS} = 25 V, 50 V, and 75 V correspond to 3.07×10^8 V/s, 8.05×10^8 V/s, and 14.03×10^8 V/s by the model.

They are 2.60×10^8 V/s, 5.71×10^8 V/s, and 10.47×10^8 V/s in the measurement. The model accurately explains the experimental results. The accumulated charges Q, calculated from drain voltage dependency of capacitance at $V_{\mathrm{DS}} = 25$ V, 50 V, and 75 V, are equal to 3.27 nC, 5.35 nC, and 7.09 nC for lateral-type in Fig. 5.7(a). Those are 8.42 nC, 13.33 nC, and 17.12 nC for vertical-type in Fig. 5.7(b). The ratios of the derivative of the V_{DS}, $\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t}$, between lateral-type and vertical-type are equal to 2.57, 2.53, and 2.40. The ratios of Q between both types are equal to 1/2.57, 1/2.50, and 1/2.41. Therefore, the ratio of turn-off speed of V_{DS} between SiC JFETs depends on the inverse ratio of Q. The lateral-type shows about 2.5 times faster turn-off speed than the vertical-type. Because the lateral-type has smaller C_{DS} and C_{GD} than the vertical-type as mentioned above.

5.4 Summary

This chapter characterized and discussed the switching characteristics of SiC JFETs through the voltage dependency of terminal capacitances. The difference between the switching characteristics of the lateral-type and the vertical-type SiC JFETs depends on their internal parasitic capacitances, which can be classified by the dependence of depletion capacitance. Therefore, the device structure and switching phenomenon can be characterized and explained for these SiC JFETs by the measurement of C-V characteristics of devices. The simulated results of the switching behavior well agree with the experimental results for some conditions of the model and extracted parameter from the C-V and I-V characteristics of these devices.

Chapter 6

An application of SiC power transistors

6.1 Introduction

Silicon carbide (SiC) power devices have been researched and developed because of its several superior physical characteristics than Si. SiC power MOSFETs are currently under development almost closed to commercial use. The theoretical analysis predicts that the SiC power MOSFETs have potentials at high frequency, high temperature, and high voltage. Therefore, it is important to confirm these performances of SiC power MOSFET at high voltage and fast switching operation.

This chapter estimates the use of SiC power MOSFETs for the control of the voltages and currents in a high frequency switching converter circuit [28, 68]. To evaluate the performances of the power devices, the SiC power MOSFETs are here used in a resonant-switch converter to shape the switch voltage and current at zero-voltage switching (ZVS) and/or zero-current switching (ZCS) with comparison to the performances of the Si power MOSFETs.

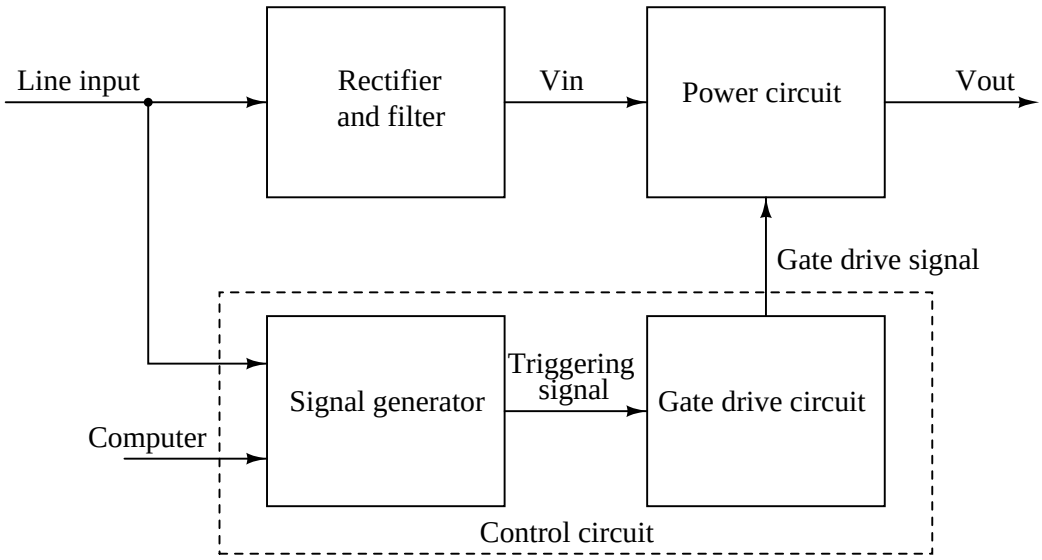


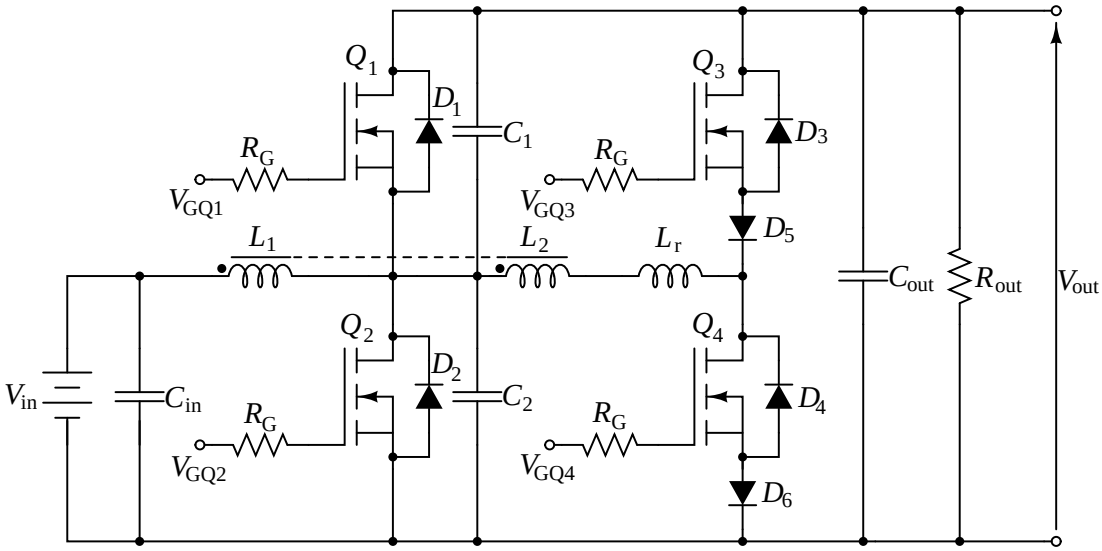
Figure 6.1 Functional block diagram of resonant-switch dc-dc step-up voltage converter

6.2 Resonant-switch dc-dc step-up voltage converter

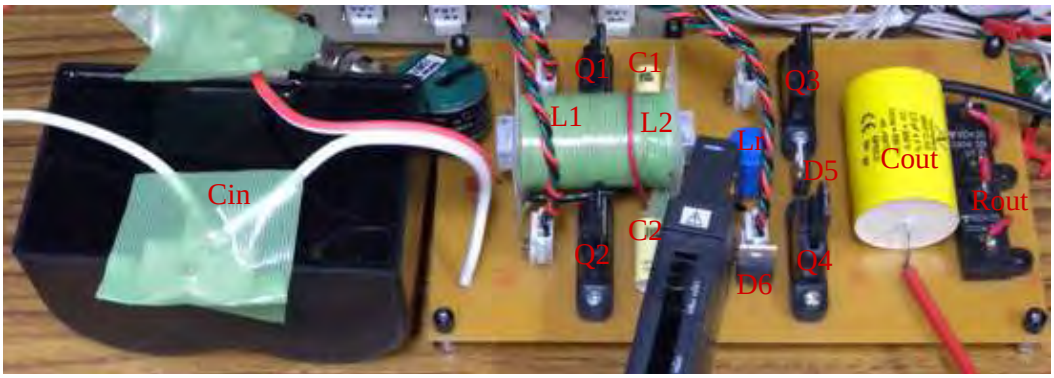
The functional block diagram of the resonant-switch dc-dc step-up voltage converter is shown in Fig. 6.1. It consists of the rectifier and filter, power circuit, and control circuit. Figure 6.2 shows the power circuit of the resonant-switch dc-dc step-up voltage converter. Its main application is in regulated dc power supplies. The converter transforms a dc voltage input to a dc voltage output that is greater in magnitude but has the same polarity as the input. It operates at a 25 μs (40 kHz) with involving a H-bridge circuit, which generates an ac square-wave voltage. The operation of circuit is originally similar to a boost converter [28, 68], but the circuit is performed by four switches Q_1, Q_2, Q_3, and Q_4 to shape the switch voltage and current to provide ZVS and/or ZCS. It can be utilized primarily by an LC resonance.

6.2.1 Power circuit

The power circuit of the resonant-switch dc-dc step-up voltage converter is shown in Fig. 6.2. The components of this converter are given in Tab. 6.1. The switches Q_1,



(a) Schematic power circuit



(b) Experimental power circuit

Figure 6.2 Resonant-switch dc-dc step-up voltage converter.

Q_2, Q_3, and Q_4 are operated by control signal to transform the dc voltage input to the dc voltage output. The inductances L_1 and L_2 are a transformer that performs a primary boosting function and provides nearly constant current to the output circuit through body diode D_1 of switch Q_1. The inductance L_r and capacitance $C_r(= C_2)$ provide a simple LC resonant circuit, thereby shaping the switch voltage and current in order to yield ZVS and ZCS in this converter. The capacitance C_1 is a snubber capacitor for switch Q_1. The diodes D_5 and D_6 are used to kill the effect of body

Table 6.1 Components of resonant-switch dc-dc step-up voltage converter.

Component	Value
Inductance L_1	3 mH
Inductance L_2	760 μH
Inductance L_r	10 μH
Input capacitance C_in	100 μF, 900 V
Capacitance C_1	10 nF
Capacitance C_2	10 nF
Output capacitance C_out	2.5 μF, 850 V
Diode D_5, D_6	30 A, 600 V (RHRP3060)
Gate resistance R_G	10 Ω
Output resistance R_out	660 Ω

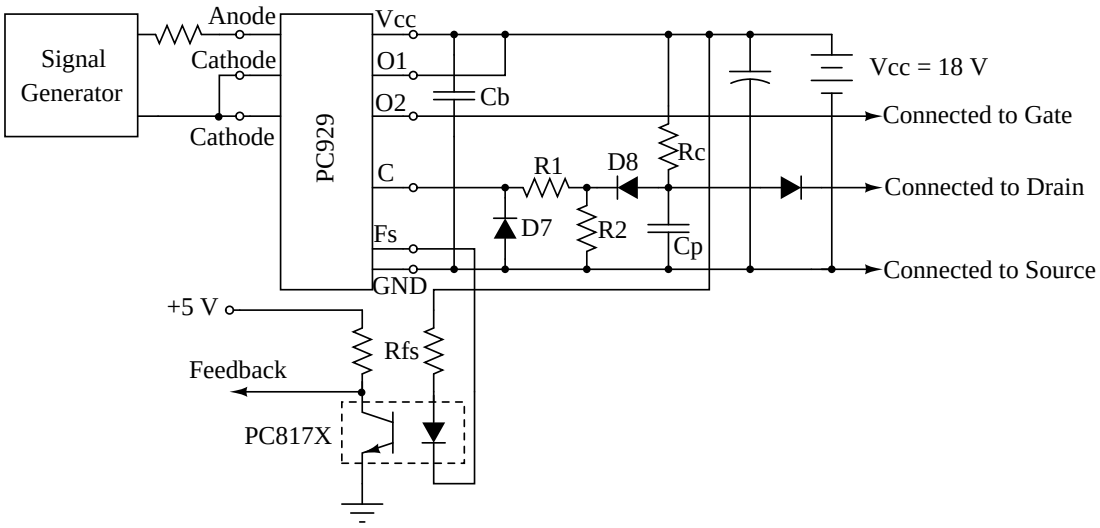
diodes D_3 and D_4 inside the switches Q_3 and Q_4, respectively. The capacitances C_in and C_out are the filter capacitor for input and output of the converter to keep a nearly constant instantaneous value. The $L_\mathrm{r}C_\mathrm{r}$ resonance around the switches Q_2 and Q_4 do not affect the primary boosting function of inductances L_1 and L_2. The L_1 and L_2 act as a step-up transformer to increase the input voltage V_in with setting a duty-cycle D and a turn ratio n_T of transformer between L_1 and L_2. Therefore, the ratio between the input voltage V_in and the output voltage V_out is expressed by Eq. (6.1):

$$\frac{V_\mathrm{out}}{V_\mathrm{in}} = \frac{1}{1-D} \cdot n_\mathrm{T}, \tag{6.1}$$

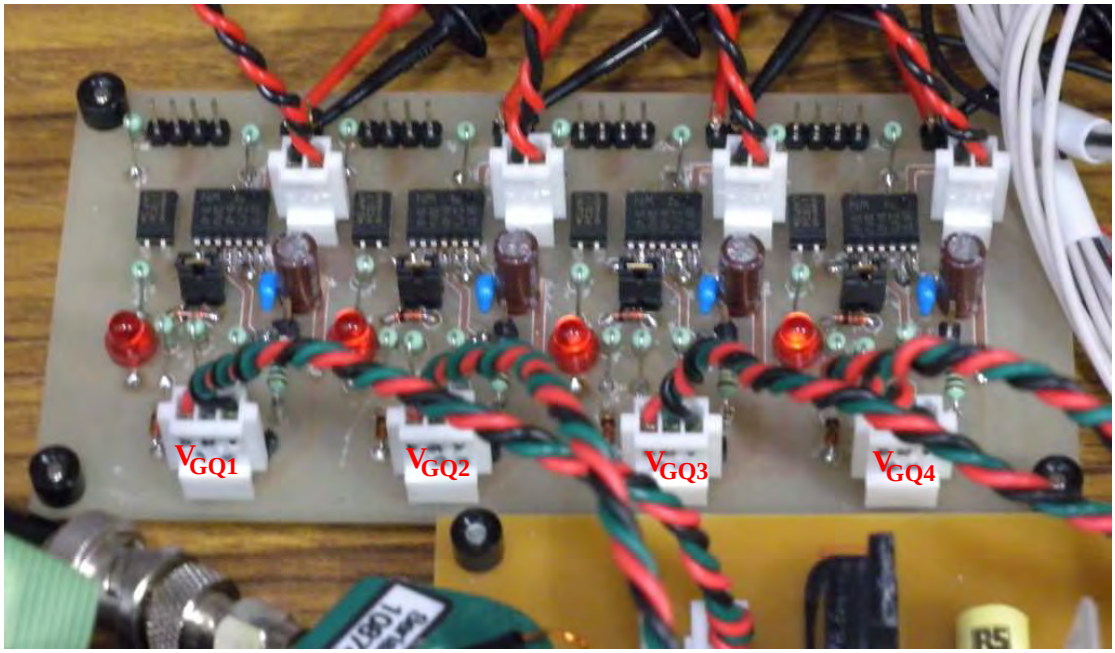
where $n_\mathrm{T} = \sqrt{L_1/L_2}$.

6.2.2 Control circuit

The control circuit is composed of the signal generator and gate drive circuit, which are shown in Fig. 6.1. Here, the signal generator is timing generator Time98-50MHz [69], which is utilized to generate the signal for gate drive circuit. The signal generator can be programmed by PC-computer. Figure 6.3 shows the gate drive circuit



(a) Schematic gate drive circuit



(b) Experimental gate drive circuit

Figure 6.3 Gate drive circuit for resonant-switch dc-dc step-up voltage converter.

of the resonant-switch dc-dc step-up voltage converter. PC929 photocoupler is used for gate drive circuit to drive the switches Q_1, Q_2, Q_3, and Q_4. The schematic gate drive circuit and experimental gate drive circuit are shown in Fig. 6.3. To stabilize

the operation of the photocoupler, it is recommended to connect a bypass capacitor Cb about 0.01 μF or more between Vcc and GND. For the detecting voltage of pin-C from drain terminal of power MOSFET, it is recommended to connect a capacitor Cp (approximately 1000 pF) between pin-C and GND, and a resistor Rc (approximately 1.0 kΩ) between Vcc and pin-C. For the blocking diode D, which is connected between pin-C and drain of power MOSFET, it is recommended to use a diode that has the withstand voltage characteristic equivalent to power MOSFET and also has little leak current. Then, for preventing the failure mode or breakdown of pin-C from variation voltage of power MOSFET, it is recommended to connect a resistor R1 (approximately 10 kΩ) and a diode D7 at near pin-C, and a resistor R2 (approximately 50 kΩ) and a diode D8 at between pin-C and GND.

6.2.3 Modes of operation—resonant-switch dc-dc step-up voltage converter

The sequence operation of the resonant-switch dc-dc step-up voltage converter depends on the gate drive signal, which is given by a signal generator. It is separated to 7 modes depending on the operation of switches Q_2 and Q_4. Here each mode is explained as follows:

Mode 1

The converter is operated in Mode 1 as shown in Fig. 6.4, when the switch Q_2 is turned on. The inductance L_1 provides nearly constant current to the output circuit. The input current $i_{\mathrm{L_1}}$ flows through inductance L_1 and switch Q_2. Therefore, the voltage dropping on inductance L_1 is given as Eq. (6.2):

$$L_1 \frac{\mathrm{d}i_{\mathrm{L_1}}}{\mathrm{d}t} = V_{\mathrm{in}}. \tag{6.2}$$

Mode 2

Figure 6.5 shows the operation of the converter in Mode 2, when the switch Q_2 is turned off. In this case, the output voltage V_{out} is higher than the input voltage

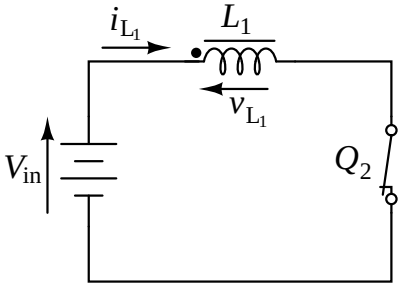


Figure 6.4 Operation of the converter in Mode 1.

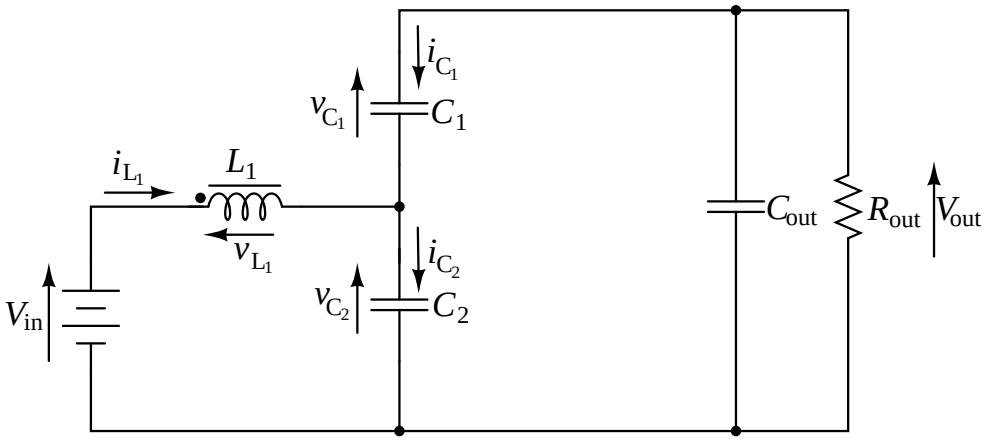


Figure 6.5 Operation of the converter in Mode 2.

V_{in}. The input current i_{L_1} and output current $i_{out}(= i_{C_1})$ flow through capacitance C_2. The input current i_{L_1} is equal to $-i_{C_1} + i_{C_2}$. Therefore, the input current i_{L_1} can be represented by Eq. (6.3):

$$i_{L_1} = -C_1 \frac{dv_{C_1}}{dt} + C_2 \frac{dv_{C_2}}{dt}. \tag{6.3}$$

Mode 3

Figure 6.6 shows the operation of the converter in Mode 3. The output voltage V_{out} is lower than the input voltage V_{in}. The input current i_{L_1} continuously flows through diode D_1 inside switch Q_1 to the output circuit. The voltage dropping inductance L_1

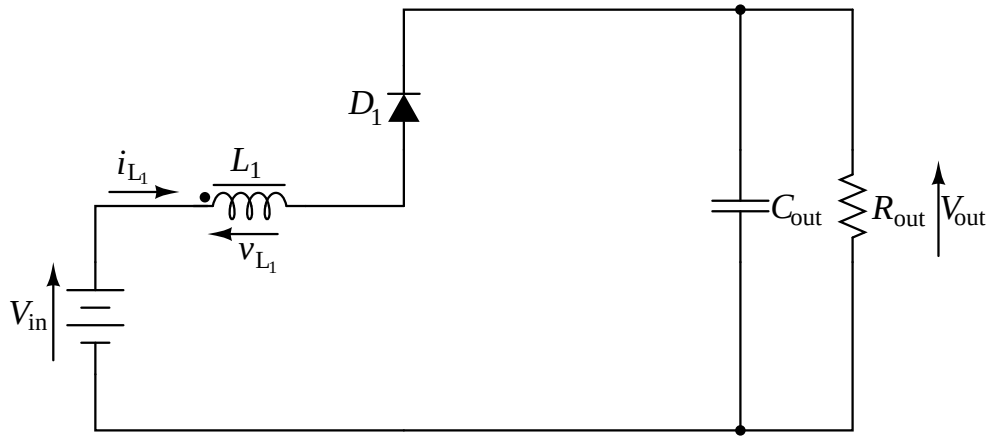


Figure 6.6 Operation of the converter in Mode 3.

can be represented by Eq. (6.4):

$$L_1 \frac{\mathrm{d}i_{\mathrm{L}_1}}{\mathrm{d}t} = -(V_{\mathrm{out}} - V_{\mathrm{in}}). \tag{6.4}$$

Mode 4

Figure 6.7 shows the operation of the converter in Mode 4, when the switch Q_4 is turned on and the switch Q_2 is still turned off. In this case, the output voltage V_{out} is lower than the input voltage V_{in}. Then, the input current i_{L_1} continuously flows through diode D_1, inductance L_2, and inductance L_{r}. The voltage dropping on inductance L_1 and L_2 in transformer is given by Eqs. (6.5) and (6.6):

$$v_{\mathrm{L}_1} = L_1 \frac{\mathrm{d}i_{\mathrm{L}_1}}{\mathrm{d}t} + M \frac{\mathrm{d}i_{\mathrm{L}_2}}{\mathrm{d}t}, \tag{6.5}$$

$$v_{\mathrm{L}_2} = L_2 \frac{\mathrm{d}i_{\mathrm{L}_2}}{\mathrm{d}t} + M \frac{\mathrm{d}i_{\mathrm{L}_1}}{\mathrm{d}t}, \tag{6.6}$$

where $M = k\sqrt{L_1 L_2}$ is the mutual inductance between L_1 and L_2, and k the coupling coefficient. Then, the input voltage V_{in} can be expressed by Eq. (6.7):

$$V_{\mathrm{in}} = L_1 \frac{\mathrm{d}i_{\mathrm{L}_1}}{\mathrm{d}t} + M \frac{\mathrm{d}i_{\mathrm{L}_2}}{\mathrm{d}t} + V_{\mathrm{out}}. \tag{6.7}$$

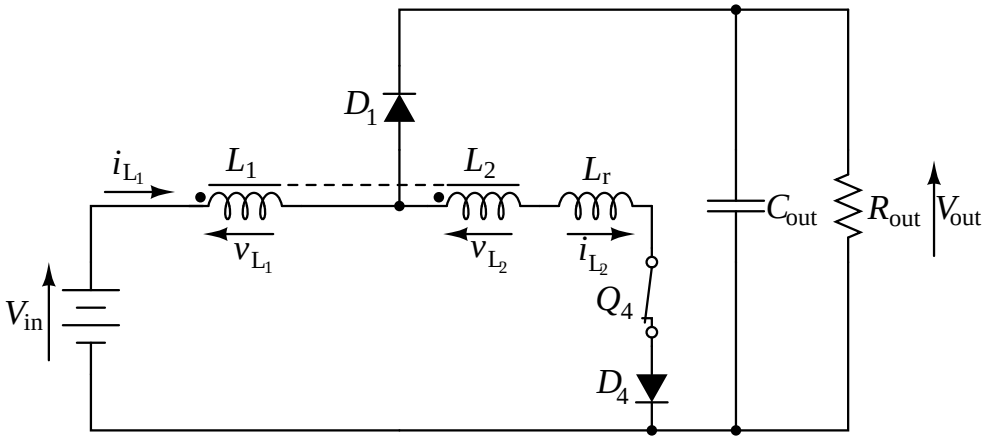


Figure 6.7 Operation of the converter in Mode 4.

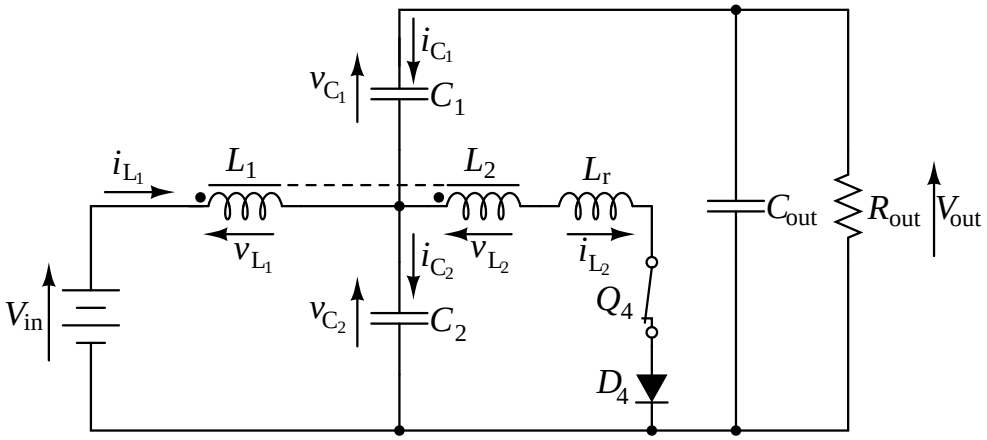


Figure 6.8 Operation of the converter in Mode 5.

Mode 5

Figure 6.8 shows the operation of the converter in Mode 5, when the switch Q_4 is turned on and the switch Q_2 is still turned off. In this case, the output voltage V_{out} is higher than the input voltage V_{in}. Then, the input current i_{L_1} and output current $i_{\text{out}}(= i_{\text{C}_1})$ continuously flows through capacitance C_2, inductance L_2, and inductance L_{r}. The voltage dropping on inductance L_1 and L_2 in transformer is given by Eqs. (6.5) and (6.6) and the current flows through capacitance C_1 and C_2 is given by Eqs. (6.8)

and (6.9):

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt}, \tag{6.8}$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt}. \tag{6.9}$$

Then, the input voltage V_{in} can be represented by Eq. (6.10):

$$V_{in} = (L_1 + M)\frac{di_{L_1}}{dt} + (L_2 + M + L_r)\frac{di_{L_2}}{dt}. \tag{6.10}$$

Mode 6

Figure 6.9 shows the operation of the converter in Mode 6, when the switch Q_4 is turned on and the switch Q_2 is still turned off. In this case, the inductance current $i_{L_2}(= i_{L_r})$ still flow through switch Q_4, diode D_6, and diode D_2. Because the voltage dropping on inductance L_r becomes higher than the voltage dropping on inductance L_1 and also the polarity of inductance L_r changes oppositely. The voltage dropping on inductance L_1 and L_2 in transformer is given by Eqs. (6.5) and (6.6). Then, the input voltage V_{in} can be expressed by Eq. (6.11):

$$V_{in} = L_1 \frac{di_{L_1}}{dt} + M\frac{di_{L_2}}{dt}. \tag{6.11}$$

Mode 7

Figure 6.10 shows the operation of the converter in Mode 6, when the switch Q_4 is turned on and the switch Q_2 becomes to turn on again. In this case, the inductance

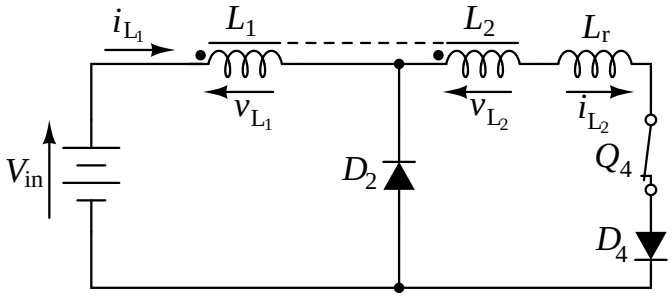


Figure 6.9 Operation of the converter in Mode 6.

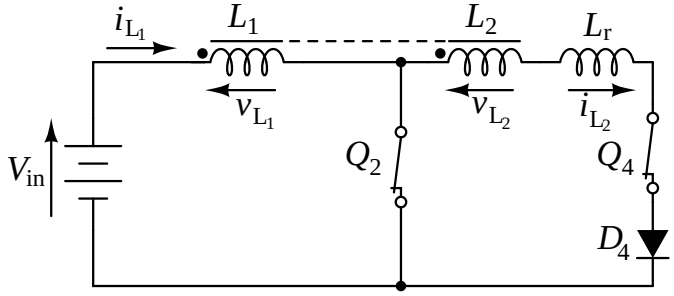


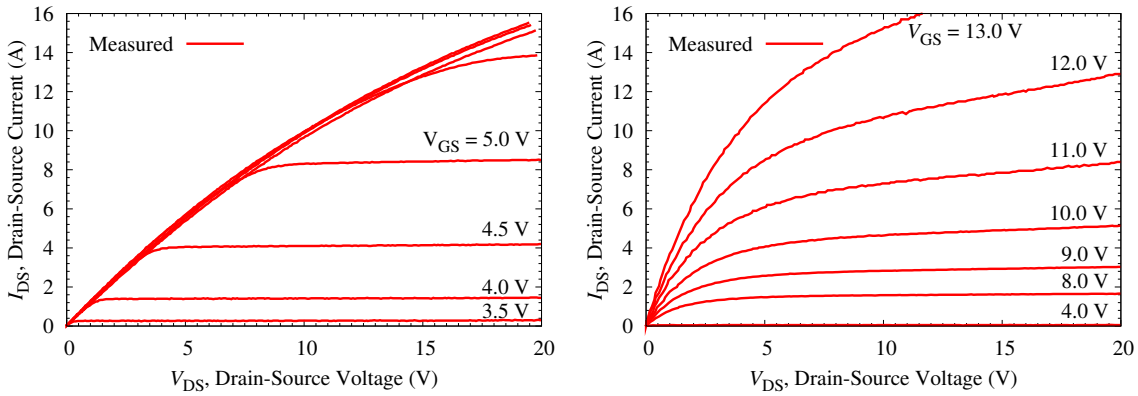
Figure 6.10 Operation of the converter in Mode 7.

current $i_{L_2}(= i_{L_r})$ still flows through switch Q_4, diode D_6, and switch Q_2. Because the voltage dropping on inductance L_r becomes higher than the voltage dropping on inductance L_1 and also the polarity of inductance L_r changes oppositely. The voltage dropping on inductance L_1 and L_2 in transformer is given by Eqs. (6.5) and (6.6). Then, the input voltage V_{in} represented by Eq. (6.11).

6.3 Experimental results of resonant-switch dc-dc step-up voltage converter

The operation of the resonant-switch dc-dc step-up voltage converter is governed by the switches Q_2 and Q_4 as mentioned above. The switches Q_1 and Q_3 are entirely turned off in this operation. Here, the Si and SiC power MOSFETs are used to be the switches Q_1, Q_2, Q_3, and Q_4. The Si power MOSFET has 700 V blocking voltage and the rated 10 A drain current. The SiC power MOSFET has 900 V blocking voltage and the rated 10 A drain current. The static I-V, transfer, and C-V characteristics of Si and SiC power MOSFET are shown in Figs. 6.11-6.13, respectively.

In comparison between the Si and SiC power MOSFET on-state curves, the Si curves, which is shown in Fig. 6.11(a), are linear in the on-state region and have a pronounced change in curvature as the saturation or pinch-off region is approached around $V_{GS} = 6$ V. This occurs because the Si power MOSFET has a large epitaxial layer resistance in series with the MOSFET channel and the channel has a very high



(a) Si power MOSFET (b) SiC power MOSFET

Figure 6.11 Measured static I-V characteristics of power MOSFET.

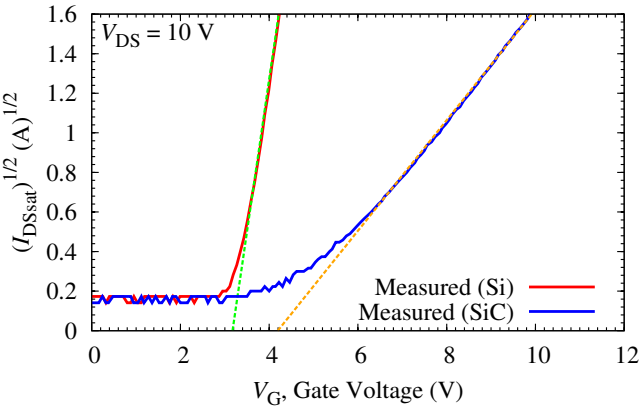
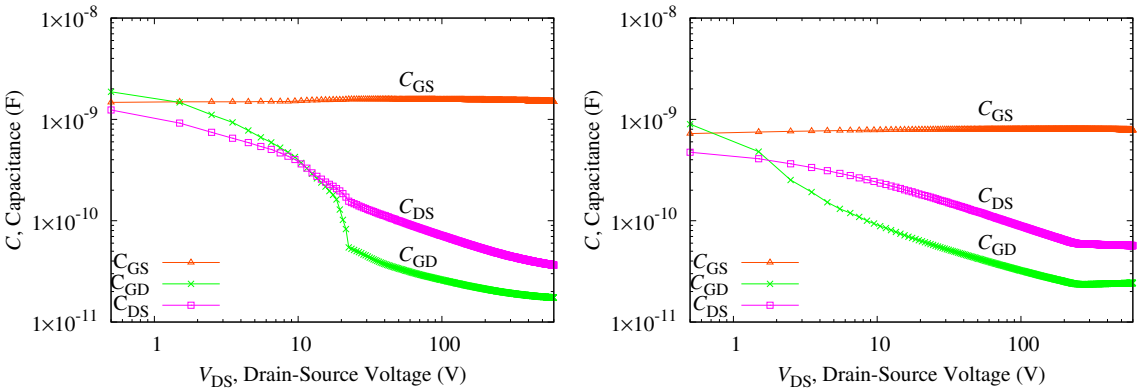


Figure 6.12 Transfer characteristics of power MOSFET.

transconductance [7, 44]. On the other hand, the SiC curves, which is shown in Fig. 6.11(b), gradually transit from the linear region to the saturation region. In SiC power MOSFET, the epitaxial layer resistance is much smaller and the channel resistance is higher, because of the non-saturable characteristics stemming from the short channel effects [43]. The V_T of the Si power MOSFET is 3.2 V and the V_T of the SiC power MOSFET is 4.2 V, as shown in Fig. 6.12.

The measured C-V_{DS} characteristics of the Si and SiC power MOSFETs are shown in Figs. 6.13(a) and 6.13(b) at logarithmic scale. The capacitances C_{GS}, C_{GD}, and C_{DS}



(a) Si power MOSFET (b) SiC power MOSFET

Figure 6.13 Measured C-V characteristics of power MOSFET.

of the SiC power MOSFET are slightly smaller that of the Si power MOSFET, when $V_{\mathrm{DS}} < 100$ V. For the SiC power MOSFET, there are no irregular capacitance, and the decrease of the capacitance in C_{GD} and C_{DS} stops around $V_{\mathrm{DS}} = 200$ V. It indicates that the expansion of the depletion region is terminated in the drift layer because of the punch-through structure of the device.

Figures 6.14 and 6.15 show the gate drive signals for Si and SiC power MOSFETs, respectively. The gate drive signals of both power MOSFETs for switches Q_2 and Q_4 are $V_{\mathrm{GQ_2}}$ and $V_{\mathrm{GQ_4}}$, which are shown in Figs. 6.2 and 6.3. The switching time T_{s} is equal to 25 μs, and the switch-on time T_{on} of $V_{\mathrm{GQ_2}}$ and $V_{\mathrm{GQ_4}}$ is equal to 12.3 μs and 13.3 μs, respectively. Here, the input voltage V_{in} is set at 50 V. The output voltage V_{out} of the converter is calculated by Eq. (6.1) as follows.

The duty cycle D of the converter, which depends on the switch-on time T_{on} of $V_{\mathrm{GQ_2}}$, is equal to

$$D = \frac{T_{\mathrm{on}}}{T_{\mathrm{s}}} = \frac{12.3 \times 10^{-6}}{25.0 \times 10^{-6}} = 0.49,$$

and the turn ratio n_{T} of transformer between L_1 and L_2 is equal to

$$n_{\mathrm{T}} = \sqrt{\frac{L_1}{L_2}} = \sqrt{\frac{3 \times 10^{-3}}{760 \times 10^{-6}}} = 1.99.$$

Therefore, the output voltage V_{out} of the converter is equal to

$$V_{\mathrm{out}} = \frac{1}{1-D} \cdot n_{\mathrm{T}} \cdot V_{\mathrm{in}} = \frac{1}{1-0.49} \times 1.99 \times 50 = 195.1 \text{ V}.$$

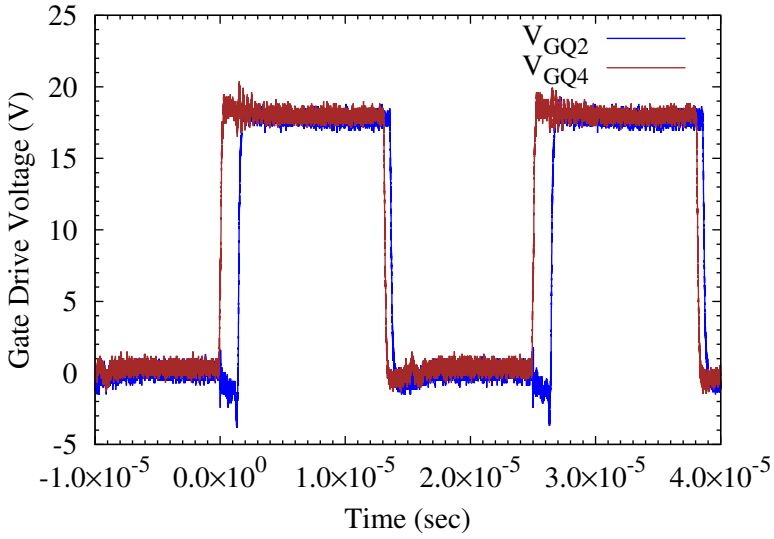


Figure 6.14 Gate drive signals for Si power MOSFET in the converter.

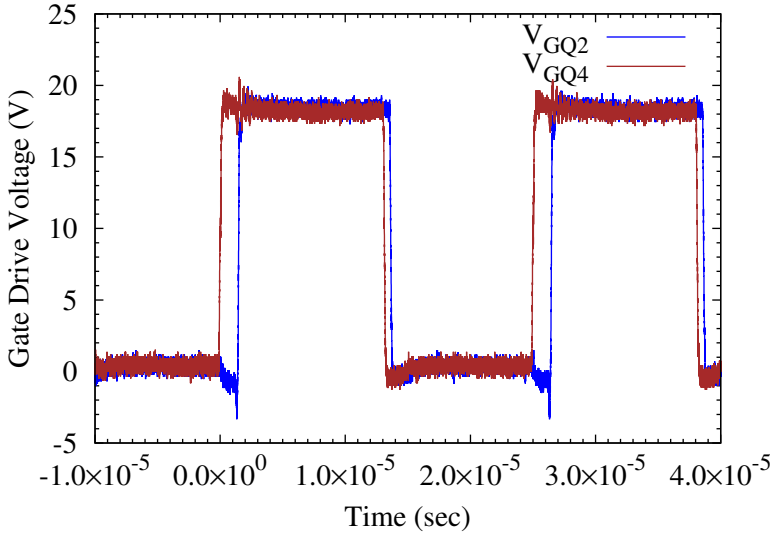
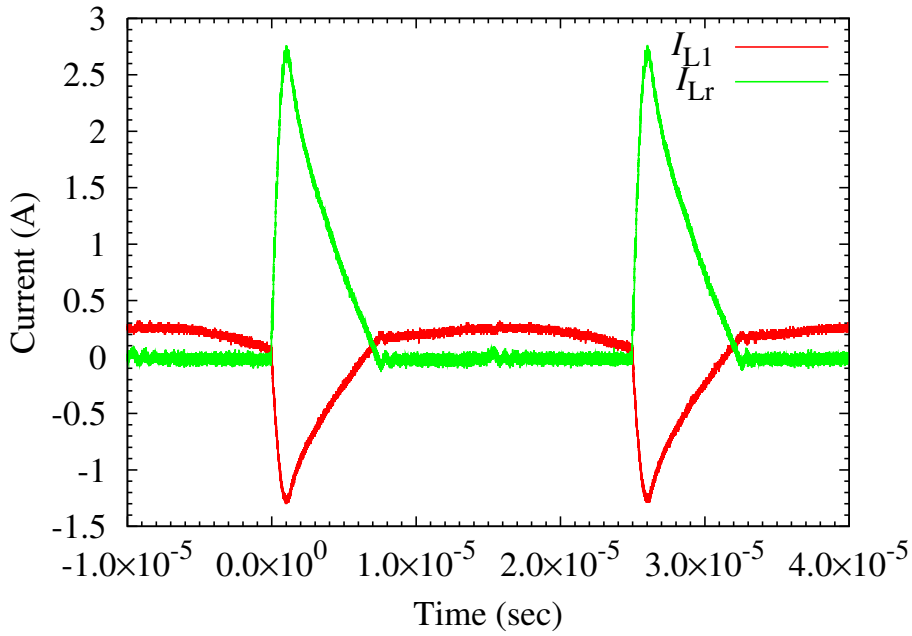
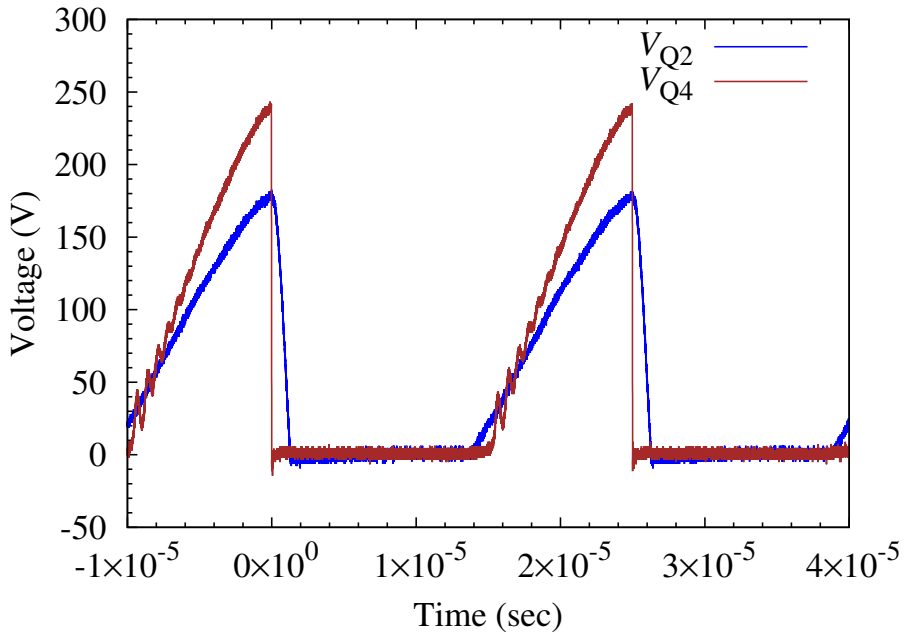


Figure 6.15 Gate drive signals for SiC power MOSFET in the converter.

Figures 6.16-6.19 show the currents and voltages of the resonant-switch dc-dc step-up voltage converter. The output voltage V_{out} is approximately equal to 194 V. It is almost similar to the calculated results. The circuit resonant frequency f_{o} can be

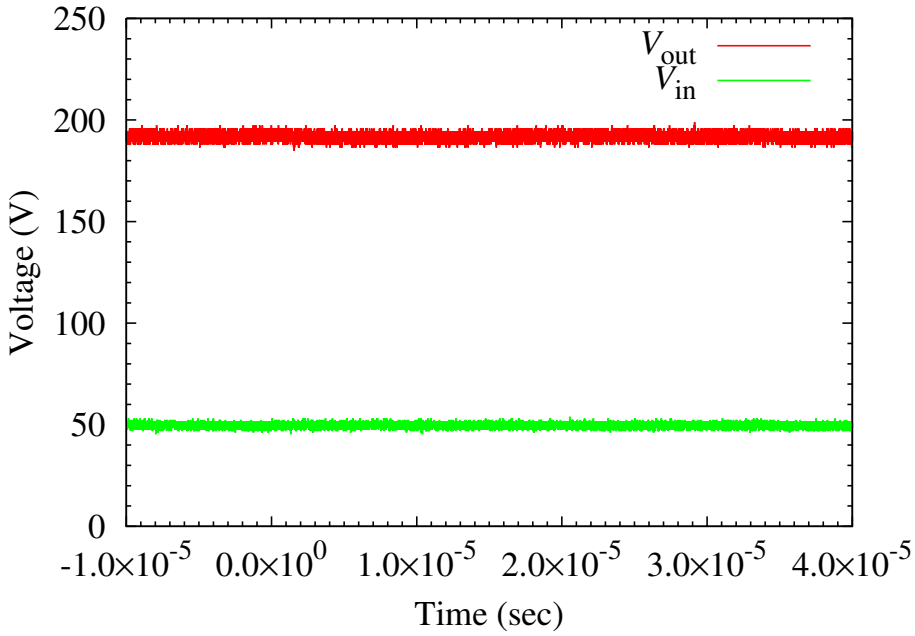


(a) Currents flowing through L_1, L_r

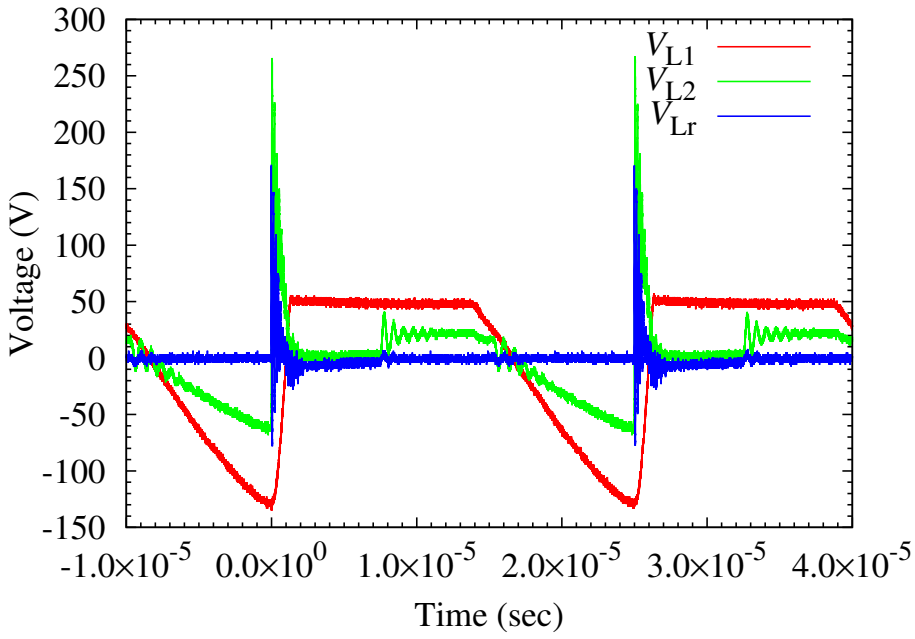


(b) Voltages dropping on switches Q_2, Q_4

Figure 6.16 Currents flowing through L_1, L_r and voltages dropping on switches Q_2, Q_4 in the converter by using Si power MOSFET as switch.

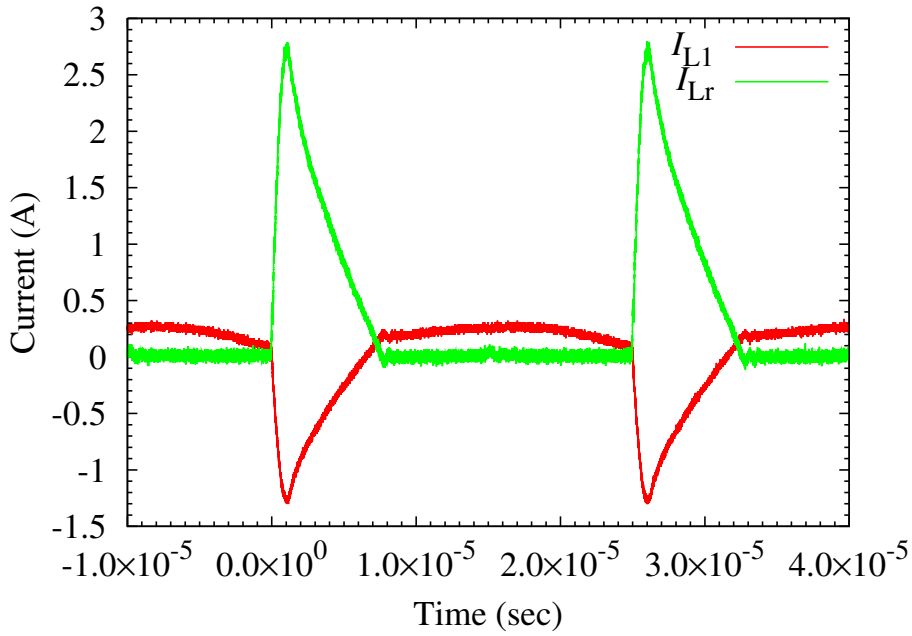


(a) Input and output voltages

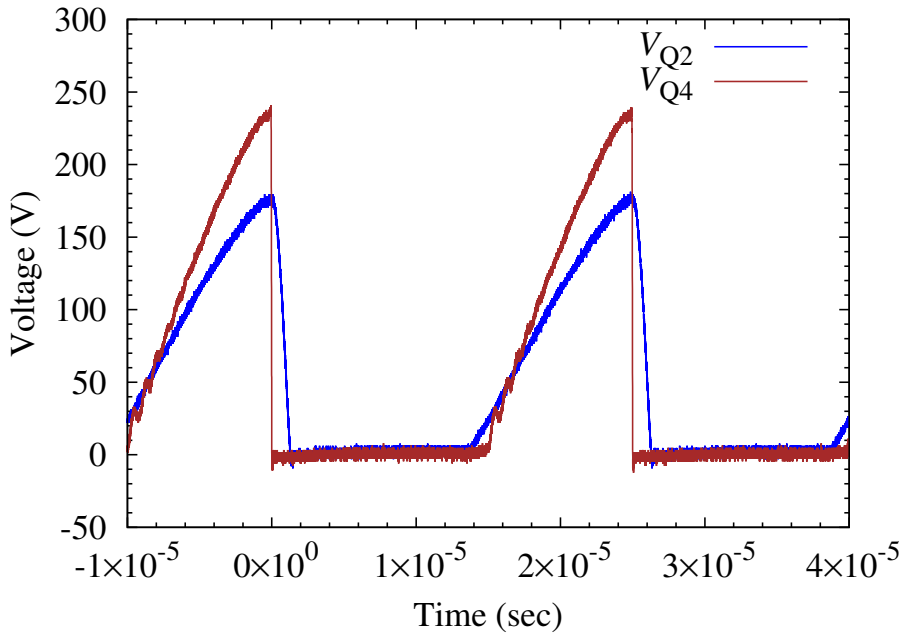


(b) Voltages dropping on inductances L_1, L_2, and L_r

Figure 6.17 Input voltage, output voltage, and voltages dropping on inductances L_1, L_2, and L_r in the converter by using Si power MOSFET as switch.

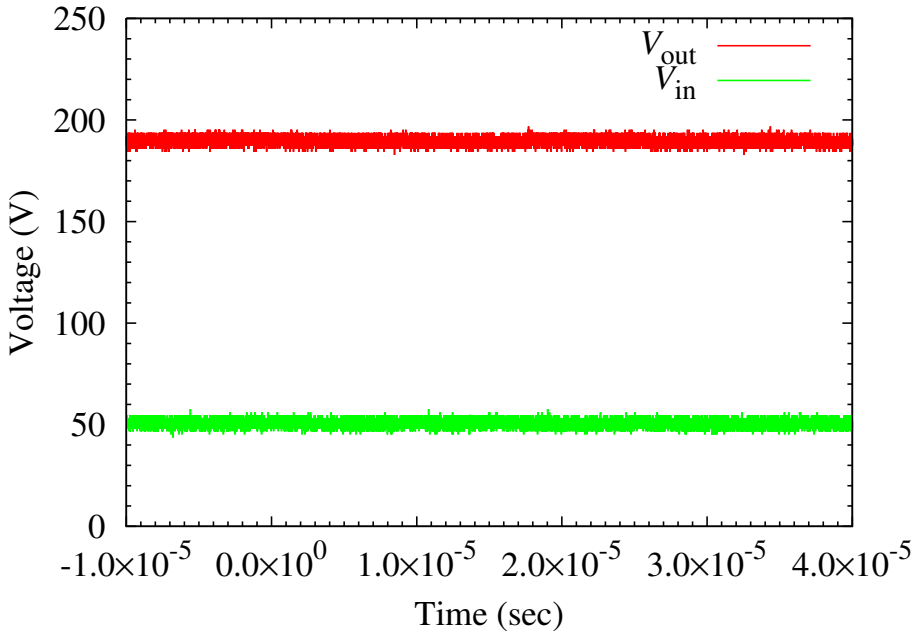


(a) Currents flowing through L_1, L_r

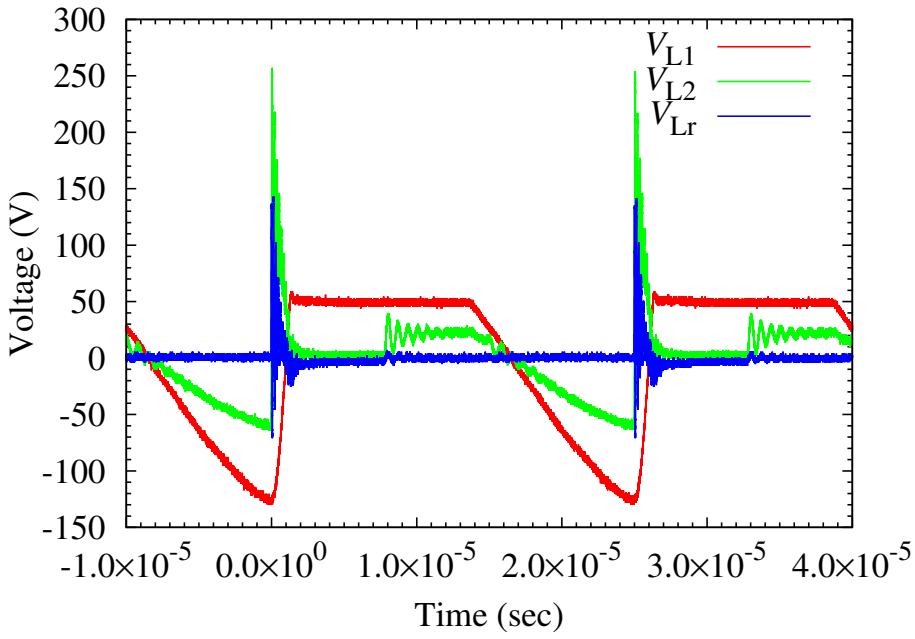


(b) Voltages dropping on switches Q_2, Q_4

Figure 6.18 Currents flowing through L_1, L_r and voltages dropping on switches Q_2, Q_4 in the converter by using SiC power MOSFET as switch.



(a) Input and output voltages



(b) Voltages dropping on inductances L_1, L_2, and L_r

Figure 6.19 Input voltage, output voltage, and voltages dropping on inductances L_1, L_2, and L_r in the converter by using SiC power MOSFET as switch.

calculated from the inductance $L_{\rm r}$ and capacitance $C_{\rm r}(= C_2)$, that is

$$f_{\rm o} = \frac{1}{2\pi\sqrt{L_{\rm r}C_{\rm r}}} = \frac{1}{2\pi\sqrt{10 \times 10^{-6} \times 10 \times 10^{-9}}} = 503 \quad \text{kHz}.$$

It is more than the switching frequency $f_{\rm s}$ tremendously. Therefore, the resonant-switch dc-dc step-up voltage converter can be operated in ZVS and ZCS resonant conditions properly.

The currents and voltages of each component in the converter, which are shown in Figs. 6.16 and 6.17 for Si power MOSFET and Figs. 6.18 and 6.19 for SiC power MOSFET, have smooth waveforms. The switch Q_2 shows the operation under the zero-voltage switching (ZVS) condition, and the switch Q_4 shows the operation under the zero-current switching (ZCS) condition. As the same components in the resonant-switch dc-dc step-up voltage converter, the voltage dropping on switch Q_4 by using SiC power MOSFET in Fig. 6.18(b) shows smaller oscillation than that by using Si power MOSFET in Fig. 6.16(b). The maximum voltage of inductances L_1, L_2, and $L_{\rm r}$ by using Si power MOSFET in Fig. 6.17(b) is equal to 50 V, 265 V, and 170 V, respectively. The maximum voltage of inductances L_1, L_2, and $L_{\rm r}$ by using SiC power MOSFET in Fig. 6.19(b) is equal to 50 V, 257 V, and 143 V, respectively. Therefore, the voltage dropping on inductances L_2 and $L_{\rm r}$ by using SiC power MOSFET shows smaller oscillation and magnitude than that by using Si power MOSFET. The output voltage $V_{\rm out}$ and currents flowing through L_1, L_2, and $L_{\rm r}$ by using SiC power MOSFET are similar to that by using Si power MOSFET.

6.4 Summary

This chapter demonstrated the operation of the SiC power MOSFET in the resonant-switch dc-dc step-up voltage converter as switch to control the output current and voltage. The experimental results show that the SiC power MOSFET achieves the resonant operation at the zero voltage and zero current switchings. The output voltage, which depends on duty cycle D and turn ratio $n_{\rm T}$ of transformer, was constant throughout the operation. Moreover, the results of the resonant converter by using the SiC power MOSFET were compared with the results by using Si power MOSFET.

The results by using SiC power MOSFET showed smoother waveforms of the current and voltage than the results by using Si power MOSFET. Therefore, the SiC power MOSFET can be used in the resonant-switch dc-dc step-up voltage converter.

Chapter 7

Conclusions

In this dissertation, SiC power transistors, especially power MOSFET and JFETs, were characterized for power conversion circuits. Transient behavior in switching operation of the SiC power devices is affected by their intrinsic parasitic capacitances. Therefore, it is important to characterize the C-V characteristics of the power devices to estimate their switching performance. The major conclusions obtained in the present study are summarized as follows.

Chapter 2 illustrated the simplified cross section of the SiC DiMOSFET cell, the lateral-type RESURF SiC JFET cell, the vertical-type bare die SiC JFET cell. In this chapter, we also described the two most commonly used types of capacitances in semiconductor devices. They are composed of the MOS capacitance type and the pn junction capacitance type. Their device structures decide the voltage dependence of the capacitance characteristics. The voltage dependence of the MOS capacitance in the SiC DiMOSFET can be distinguished as accumulation, depletion, and inversion conditions, which is similar to the Si power MOSFET. The voltage dependence of the pn junction capacitance in both SiC JFETs is expressed at the uniformly doped and the linearly graded doped junctions.

In Chapter 3, we described the developed C-V characterization system for high-voltage power transistors. Because the terminal capacitances of a power device are important to understand the dynamic behavior of the device, such as its switching operation. The device capacitances are not constant, but change with terminal ap-

plied voltage. Therefore, a C-V characterization system for gate-controlled power devices was developed in this study. It consists of five measurement circuits, which were proposed to measure the three combinations of terminal capacitances and three combinations of device capacitance for circuit operation. The developed capacitance characterization system can measure capacitance from the blocking condition to the conducting condition while changing the gate bias voltage. The variation of the depletion and accumulation condition in the device was reflected in the device capacitance. The measured capacitance explained the device structure and the physical phenomenon occurring in the device clearly.

In order to predict the device characteristics of the Si and SiC power MOSFETs accurately over their wide range of operation, a physics-based model was studied and proposed based on terminal capacitances in Chapter 4. In this chapter, we characterized the voltage dependence of terminal capacitances of the power devices, modeled the I-V characteristics with discussing the C-V characteristics of the power devices, and extracted the model parameters from their characteristics. And also, this chapter characterized and discussed the switching characteristics of power MOSFETs through the voltage dependence of terminal capacitances. The difference between the switching characteristics of the Si and SiC power MOSFETs depends on their internal parasitic capacitances, which can be classified by the MOS capacitance and pn junction capacitance. Finally, it was shown that the simulated results of the switching behavior well agree with the experimental results for some conditions of the model and extracted parameters. The SiC power MOSFET has faster turn-on and turn-off speed than the Si power MOSFET. Because the SiC power MOSFET has smaller terminal capacitances than the Si power MOSFET.

In Chapter 5, we characterized and discussed the switching characteristics of the lateral-type and vertical-type SiC JFETs through the gate and drain voltage dependency of terminal capacitances, and also the static I-V characteristics of both SiC JFETs. The difference between the switching characteristics of the lateral-type and the vertical-type SiC JFETs depends on their internal parasitic capacitances, which can be classified by the dependence of depletion capacitance. The lateral-type SiC JFET has faster turn-off speed than the vertical-type SiC JFET. Therefore, the de-

vice structure and switching phenomenon can be characterized and explained for these SiC JFETs by the measurement of C-V characteristics of devices. In the end of this chapter, it was shown that the simulated results of the switching behavior well agree with the experimental results.

Finally, the SiC power MOSFET was experimentally evaluated its performances in a high frequency switching converter circuit. The characterization of the SiC power MOSFET was examined via measured and simulated results in Chapter 4. In Chapter 6, we demonstrated the operation of the SiC power MOSFET in the resonant-switch dc-dc step-up voltage converter as switch to control the output current and voltage. As the experimental results, the SiC power MOSFET in the resonant converter was switched at the zero-voltage and zero-current switching conditions. The output voltage, which depends on duty cycle D and turn ratio n_{T} of transformer, was constant throughout the operation. And also, the results of the resonant converter using the SiC power MOSFET were compared with the results using Si power MOSFET. The results showed smoother waveforms of the current and voltage. Therefore, the SiC power MOSFET is preferable in the resonant converter towards power conversion circuits.

Through this study, several issues in characterization of SiC power transistors for power conversion circuits have been clarified. However, there remain several issues to be solved. They have emerged several goals to be accomplished in the future:

- **An analysis of switching behavior by equivalent circuit of SiC power transistors:**

  We have worked on characterization of SiC power transistor to characterize the static I-V, C-V, and switching characteristics of the SiC power devices for power conversion circuits. This dissertation shows that the transient behavior in switching operation of the SiC power devices are discussed with relation to their C-V characteristics and static I-V characteristics. The simulated results in switching behavior of the SiC power devices coincided with experimental results suitably in some conditions. Therefore, we now are analyzing on the dynamics model of SiC power devices with equivalent circuit based on C-V measurement for suitably all conditions.

- **Evaluation of SiC power transistors in a high frequency switching power conversion circuit:**

  SiC semiconductor is the most promising material for power switching devices due to their inherent material characteristics. For this reason, SiC power devices are also expected to have fast switching capability. Under development, SiC power MOSFETs and SiC JFETs now are the most possible power switches for high switching frequency power converters. To realize the fast switching with a thin voltage blocking layer, the switching characteristics of the SiC power MOSFETs and SiC JFETs have to be evaluated in a high frequency switching power conversion circuit.

- **Performance evaluation of a SiC power MOSFET in a resonant circuit application:**

  In Chapter 6, we demonstrated the operation of the SiC power MOSFET in a resonant converter to regulate the output voltage. The obtained experimental results of the resonant converter by using the SiC power MOSFET showed the smooth waveforms of the current and voltage of the converter. Therefore, the SiC power MOSFET can be used as a switch to control the output current and voltage appropriately. Next, we are evaluating and discussing the performance of the SiC power MOSFET in the resonant converter with comparing the Si power MOSFET.

Bibliography

[1] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907-914, May 2003.

[2] C. E. Weitzel, J. W. Palmour, C. H. Carter, K. Moore, K. K. Nordquist, S. Allen. C. Thero, and M. Bhatnagar, "Silicon carbide high-power devices," *IEEE Trans. Electron Devices,* vol. 43, no. 10, pp. 1732-1741, Oct. 1996.

[3] B. J. Baliga, *Silicon Carbide Power Devices*, Singapore: World Scientific, 2006.

[4] B. J. Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices,* vol. 43, no. 10, Oct. 1996.

[5] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," *IEEE Trans. Electron Devices,* vol. 40, no. 3, Mar. 1993.

[6] J. Steszewski, A. Jakubowski, and M. L. Korwin-Pawlowski, "Comparison of 4H-SiC and 6H-SiC MOSFET I-V characteristics simulated with Silvaco Atlas and Crosslight Apsys," *Journal of telecommunications and information technology,* pp. 93-95, Mar. 2007.

[7] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, New York: Springer, 2008.

[8] S. E. Saddow and A. Agarwal, *Advances in Silicon Carbide Processing and Applications,* Boston: Artech House, 2004.

[9] A. R. Hefner, R. Singh, J. Lai, D. Berning, S. Bouche, and C. Chapuy, "SiC power diodes provide breakthrough performance for a wide range of applications," *IEEE Trans. Electron Devices,* vol. 16, no. 2, pp. 273-280, Mar. 2001.

[10] R. Singh, J. A. Cooper, M. R. Melloch, T. P. Chow, and J. W. Palmour, "SiC power Schottky and PiN diodes," *IEEE Trans. Electron Devices,* vol. 49, no. 4, pp. 665-672, Apr. 2002.

[11] G. Spiazzi, S. Buso, M. Citron, M. Corradin, and R. Pierobon, "Performance evaluation of a Schottky SiC power diode in a boost PFC application," *IEEE Trans. Power Electron.,* vol. 18. no. 6, pp. 1249-1253, Nov. 2003.

[12] A. Elasser, M. H. Kheraluwala, M. Ghezzo, R. L. Steigerwald, N. A. Evers, J. Kretchmer, and T. P. Chow, "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," *IEEE Trans. Industry App.,* vol. 39. no. 3, Jul. 2003.

[13] A. Itoh, T. Kimoto, and H. Matsunami, "High performance of high-voltage 4H-SiC Schottky Barrier Diodes," *IEEE Trans. Electron Devices,* vol. 16, no. 6, Jun. 1995.

[14] Examples of SiC JFET, "SIDC02D60SIC2," from Infineon Technologies AG., and "CPWR-0600S004" from Cree Inc.

[15] M. S. Chinthavali, B. Ozpineci, and L. M. Tolbert, "High temperature characterization of SiC power electronic devices," *Proceeding of the IEEE WPET2004,* Sheraton Detroit Novi, Oct. 21-22, 2004.

[16] A. M. Abou-Alfotouh, A. V. Radun, H. R. Chang, and C. Winterhalter, "A 1-MHz hard-switched silicon carbide DC-DC converter," *IEEE Trans. Power Electron.,* vol. 21, no. 4, pp. 880-889, Jul. 2006.

[17] B. Ray and R. L. Spyker, "High temperature design and testing of a DC-DC power converter with Si and SiC devices," *Proceeding of the 39th IEEE IAS Annual Meeting,* vol. 2, pp. 1261-1266, Oct. 3-7, 2004.

[18] B. Ray, J. D. Scofield, R. L. Spyker, B. Jordan, and Sei-Hyung Ryu, "High temperature operation of a dc-dc power converter utilizing SiC power devices," *Proceeding of the IEEE APEC 2005,* vol. 1, pp. 315-321, Mar. 6-10, 2005.

[19] C. W. Hatfield, G. L. Bilbro, S. T. Allen, and J. W. Palmour, "DC I-V characteristics and RF performance of a 4H-SiC JFET at 773 K," *IEEE Trans. Electron Devices,* vol. 45, no. 9, pp. 2072-2074, Sep. 1998.

[20] Sei-Hyung Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, and A. R. Hefner, "10-kV, 123-m$\Omega \cdot$ cm^2 4H-SiC power DMOSFETs," *IEEE Trans. Electron Device Letters,* vol. 25, no. 8, pp. 556-558, Aug. 2004.

[21] K. Fujikawa, K. Shibata, T. Masuda, S. Shikata, and H. Hayashi, "800 V 4H-SiC RESURF-Type Lateral JFETs," *IEEE Electron Device Letters,* vol. 25, no. 12, pp. 790-791, Dec. 2004.

[22] B. J. Baliga, *Modern Power Devices*, New York: Wiley, 1987.

[23] B. J. Baliga, *Power Semiconductor Devices*, Boston, MA: PWS-Kent, 1995.

[24] P. Friedrichs, *el. al.,* "Static and dynamic characteristics of 4H-SiC JFETs designed for different blocking categories," *Materials Science Forum,* vol. 338-342, pp. 1243-1246, 2000.

[25] P. Friedrichs, H. Mitlehner, R. Schorner, K-O. Dohnke, R. Elpelt, and D. Stephani, "Application-oriented unipolar switching SiC devices," *Materials Science Forum,* vol. 389-393, pp. 1185-1190, 2002.

[26] P. Friedrichs, H. Mitlehner, R. Schorner, K-O. Dohnke, R. Elpelt, and D. Stephani, "Stacked high voltage switch based on SiC VJFETs," *Proceeding of the IEEE ISPSD 2003,* pp. 139-142, Apr. 2003.

[27] D. A. Grant and J. Gower, *Power MOSFETs*, New York: Wiley, 1989.

[28] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics; converters, applications, and design,* New Jersey: John Wiley & Sons, Inc., 2003.

[29] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices: 3rd edition,* New Jersey: John Wiley & Sons, 2007.

[30] R. Perret, *Power Electronics Semiconductor Devices,* London: ISTE Ltd and John Wiley & Sons, Inc., 2009.

[31] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and R. Sei-Hyung, "Silicon carbide power MOSFET model and parameter extraction sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353-363, Mar. 2007.

[32] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE: 2nd edition,* New York: McGraw-Hill, Inc., 1993.

[33] J. M. Miller, "The dependence of the amplification constant and internal plate circuit resistance of a three-electrode vacuum tube upon the structural dimensions," *Proc. IRE*, vol. 8, pp. 64-72, 1920.

[34] S. Pittet and A. Rufer, "The equivalent electron density concept for static and dynamic modeling of the IGBT base in soft- and hard-switching applications," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2223-2233, Nov. 2007.

[35] JEDEC Standard JESD6, Measurement of Small Values of Transistor Capacitance, 1967.

[36] IEC Standard 60747, Semiconductor Devices, 2006.

[37] R. Elferich, T. Lopez, and N. Koper, "Accurate behavioural modeling of power MOSFETs based on device measurements and FE-simulations," *The Eur. Conf. Power Electron. Appl.*, Dresden, Germany, Sep. 11-14, Paper 0708, 2005.

[38] T. Funaki, S. Matsuzaki, T. Kimoto, and T. Hikihara, "Characterization of punch-through phenomenon in SiC-SBD by capacitance-voltage measurement at high reverse bias voltage," *IEICE Electron. Exp.*, vol. 3, no. 16, pp. 379-384, Aug. 2006.

[39] T. Funaki, T. Kimoto, and T. Hikihara, "Evaluation of high frequency switching capability of SiC Schottky barrier diode based on junction capacitance model," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2602-2611, Sep. 2008.

[40] Impedance Measurement Handbook. Agilent Technol., Santa Clara, CA, AN-5950-3000, pp. 27-28, Jul. 2006.

[41] A. S. Spinelli, A. Pacelli, and A. L. Lacaita, "Simulation of polysilicon quantization and its effect on n- and p-MOSFET performance," *Solid State Electronics,* vol. 46, pp. 423-428, 2002.

[42] Y. Tsividis, *Operation and Modeling of the MOS Transistor: 2nd edition,* New York: McGraw-Hill, 1999.

[43] M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto, "Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs," *IEEE Trans. Electron Devices,* vol. 52, no. 9, pp. 1954-1962, Sep, 2005.

[44] R. S. Scott, A. Franz, and J. L. Johnson, "An accurate model for power DMOSFET's including interelectrode capacitance," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 192-198, Apr. 1991.

[45] B. J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, and N. D. Zommer, "The Insulated Gate Transistor: A new three-terminal MOS-controlled bipolar power device," *IEEE Trans. Electron Devices*, vol. 31, no. 6, pp. 821-828, Jun. 1984.

[46] K. Fujii, P. Koellensperger, and R.W. De Doncker, "Characterization and comparison of high blocking voltage IGBTs and IEGTs under hard- and soft-switching conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 172-179, Jan. 2008.

[47] X.-B. Chen and J. K. O. Sin, "Optimization of the specific on-resistance of the COOLMOS," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 344-348, Feb. 2001.

[48] Z. Liang, B. Lu, J. D. van Wyk, and F. C. Lee, "Integrated CoolMOS FET/SiC-diode module for high performance power switching," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 679-686, May 2005.

[49] Y. Chen, Y. C. Liang, and G. S. Samudra, "Design of gradient oxide bypassed superjunction power MOSFET devices," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1303-1310, Jul. 2007.

[50] B. Ozpineci and L. M. Tolbert, "Characterization of SiC Schottky diodes at different temperatures," *IEEE Power Electron. Lett.*, vol. 1, no. 2, pp. 54-57, Jun. 2003.

[51] Y. Jian, L. Zhenxian, and J. D. van Wyk, "High temperature embedded SiC chip module (ECM) for power electronics applications," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 392-398, Mar. 2007.

[52] T. Funaki, J. Balda, J. Junghans, A. Kashyap, A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, "Power conversion with SiC devices at extremely high ambient temperatures," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1321-1329, Jul. 2007.

[53] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, F. D. Barlow, H. A. Mantooth, T. Kimoto, and T. Hikihara, "SiC JFET dc characteristics under extremely high ambient temperatures," *IEICE Electron. Exp.*, vol. 1, no. 17, pp. 523-527, 2004.

[54] T. Funaki, J. C. Balda, J. Junghans,A. Jangwanitlert, S. Mounce, F. D. Barlow, H. A. Mantooth, T. Kimoto, and T. Hikihara, "Switching characteristics of SiC JFET and Schottky diode in high-temperature dc-dc power converters," *IEICE Electron. Exp.*, vol. 2, no. 3, pp. 97-102, 2005.

[55] P. Shah, B. Geil, M. Ervin, T. Griffin, S. Bayne, K. Jones, and T. Oldham, "Advanced operational techniques and pn-pn-pn structures for high power silicon carbide gate turn-off thyristors," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 1073-1079, Nov. 2002.

[56] T. R. McNutt, A. R. Hefner, H. A. Mantooth, J. Duliere, D. W. Berning, and R. Singh, "Silicon carbide PiN and merged PiN Schottky power diode models implemented in the saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 573-581, May 2004.

[57] T. Nomura, M. Masuda, N. Ikeda, and S. Yoshida, "Switching characteristics of GaN HFETs in a half bridge package for high temperature applications," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 692-697, Mar. 2008.

[58] T. Biondi, G. Greco,M. C. Allia, S. F. Liotta, G. Bazzano, and S. Rinaudo, "Distributed modeling of layout parasitics in large-area high-speed silicon power devices," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1847-1856, Sep. 2007.

[59] S. Rael and B. Davat, "A physics-based modeling of interelectrode MOS capacitances of power MOSFET and IGBT," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2585-2594, Sep. 2008.

[60] T. Funaki, T. Kimoto, and T. Hikihara, "Evaluation of capacitance-voltage characteristics for high voltage SiC-JFET," *IEICE Electron. Exp.*, vol. 4, no. 16, pp. 517-523, Aug. 2007.

[61] I. K. Budihardjo, P. O. Lauritzen, and H. A. Mantooth, "Performance Requirements for Power MOSFETs," *IEEE Trans. on Power Electron.*, vol. 12, no, 1, pp. 36-45. Jan. 1997.

[62] International Rectifier, SPICE Computer Models for HEXFETs, Application Note AN-975B.

[63] International Rectifier, SPICE-2 Computer Models for HEXFETs, Application Note AN-954.

[64] D. Foty, *MOSFET Modeling with SPICE: principles and practice,* New Jersey: Prentice-Hall, 1997.

[65] S. Dimitrijev, *Understanding Semiconductor Devices,* New York: Oxford University Press, Inc., 2000.

[66] T. B. Salah, S. Khachroumi, and H. Morel, "Characterization, modeling, and design parameters identification of Silicon Carbide junction field effect transistor for temperature sensor applications," *Sensors*, vol. 10, pp. 388-399, Jan. 2010.

[67] S. Zappe, M. Leone, F. Yang, and E. Obermeir, "Characterisation of silicon carbide JFETs with respect to microsystems for high temperature applications," *Springer-Verlag, Microsystem Technologies*, vol. 3, no. 3, pp. 134-138, May 1997.

[68] B. W. Williams, *Principles and Elements of Power Electronics: Devices, Drivers, Applications, and Passive Components,* Glasgow: University of Strathclyde Glasgow, 2006.

[69] Timing Generator Reference Manual (Time98-50MHz), AS-COM Japan Corporation.

List of Publications

The published papers, which contain most parts of this dissertation, by the author are listed below.

Archival journal articles

- T. Funaki, N. Phankong, T. Kimoto, and T. Hikihara, "Measuring terminal capacitance and its voltage dependency for high-voltage power devices," *IEEE Trans. on Power Electron.*, vol. 24, no. 6, pp. 1486-1493, Jun. 2009.

- N. Phankong, T. Funaki, and T. Hikihara, "Characterization of the gate-voltage dependency of input capacitance in a SiC MOSFET," *IEICE Electron. Express*, vol. 7, no. 7, pp. 480-486, Apr. 2010.

- N. Phankong, T. Funaki, and T. Hikihara, "Switching characteristics of lateral-type and vertical-type SiC JFETs depending on their internal parasitic capacitances," *IEICE Electron. Express*, vol. 7, no. 14, pp. 1051-1057, July. 2010.

- N. Phankong, T. Funaki, and T. Hikihara, "Characterization of switching behavior of SiC FETs based on measuring terminal capacitances," *IEEE Trans. on Power Electron.* (in preparation).

- N. Phankong, T. Yanagi, and T. Hikihara, "An analysis of switching behavior by equivalent circuit of SiC power MOSFET based on C-V measurement," *IEEE Trans. on Power Electron.* (in preparation).

International conference proceedings

- N. Phankong, T. Funaki, and T. Hikihara, "A static and dynamic model for a silicon carbide power MOSFET," *The 13th European Conference on Power Electronics and Applications (EPE2009)*, Barcelona, Spain, September 8-10, 2009.

Domestic conference proceedings and technical reports

- N. Phankong, T. Funaki, and T. Hikihara, "A Discussion on the High Level Carrier Lifetime Effect of IGBT Model," *The Papers of Joint Technical Meeting on Electron Devices and Semiconductor Power Converter, IEE Japan*, EDD-07-73/SPC-07-99, Mie University, Japan, October 25-26, 2007.

- N. Phankong, T. Funaki, and T. Hikihara, "Evaluation of base region parameters in IGBT based on capacitance-voltage characteristics," *Proceeding of the 2008 IEICE General Conference*, Kitakyushu Science and Research Park, Japan, March 18-21, 2008.

- N. Phankong, T. Funaki, and T. Hikihara, "Modeling of power MOSFET based on capacitance-voltage characteristics," *The 22nd Annual Conference of the Industry Applications Society of the Institute of Electrical Engineers of Japan (JIASC2008)*, Kochi City Culture-Plaza (CUL-PORT), Japan, August 27-29, 2008.

- N. Phankong, T. Funaki, and T. Hikihara, "Experimental study on dynamic behavior of power MOSFET based on capacitance-voltage characteristics," *The Papers of Joint Technical Meeting on Electron Devices and Semiconductor Power Converter, IEE Japan*, EDD-08-65/SPC-08-152, Kyushu Institute of Technology Tobata Campus, Japan, October 23-24, 2008.

- N. Phankong, T. Funaki, and T. Hikihara, "A study on C-V characterization of lateral-type silicon carbide JFET," *The 2009 Annual Meeting Record IEE Japan*, Hokkaido University, Japan, March 17-19,2009.

- T. Funaki, N. Phankong, and T. Hikihara, "Measurement of terminal capacitance of high voltage MOS power transistors," *The Papers of Joint Technical Meeting on Electron Devices and Semiconductor Power Converter, IEE Japan*, EFM-09-38/EDD-09-72/SPC-09-139, Tokyo Institute of Technology, Japan, October 29, 2009.

- N. Phankong, T. Yanagi, and T. Hikihara, "An analysis of switching behavior by equivalent circuit of power MOSFET," *The 2010 Annual Meeting Record IEE Japan*, Meiji University, Japan, March 17-19, 2010.