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Switching characteristics of lateral-type and vertical-type SiC JFETs depending on their internal parasitic capacitances

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Abstract: Transient behavior in switching operation of junction field-effect transistors (JFETs) is affected by their intrinsic parasitic capacitances. This paper focuses on the switching operation of lateral-type and vertical-type SiC JFETs with considering the charge/discharge behavior of parasitic capacitances in the device. Their device structure decides the voltage dependency of the capacitance characteristics, so that the C-V characteristics governs their switching behavior.

Keywords: C-V characteristics, switching characteristics, SiC, JFET, device structure

Classification: Electron devices, circuits, and systems

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1 Introduction

Recently, SiC-based semiconductor power devices are strongly expected to replace Si power devices at high-temperature, high switching frequency, and high voltage application [1]. Among the devices, transistors are the most possible power switches for power conversions. Several types of SiC-based transistors have been proposed and developed. Junction field-effect transistor (JFET) is preferred for its low on-resistance $R_{\rm DSon}$ and ruggedness in harsh environments. Lateral-type and vertical-type SiC JFETs [2, 3] have been developed. Their structures have shown the normally-on characteristics for a long time, but recently the normally-off type devices have been developed. Now we have both types in laboratory experiments. However, low on-resistance $R_{\rm DSon}$ characteristics of JFET are violated by achieving normally-off characteristics. Then, the SiC JFETs discussed in this paper are limited in normally-on type devices.

The switching behavior of actual power devices is far from ideal. The non-ideal characteristics of SiC device affect on the performance of power conversion circuits, especially at high switching frequency. Then, the characteristics of the devices must be clarified and evaluated in advance of the design of power conversion circuits. Here, the switching characteristics of two different types SiC JFETs are discussed with relation to their internal parasitic capacitances. The parasitic capacitances in FET are composed of three capacitances $C_{\rm GS}$, $C_{\rm GD}$, and $C_{\rm DS}$ as shown in Fig. 1 (a). $C_{\rm GS}$ and $C_{\rm GD}$ constitute the input capacitance $C_{\rm ISS}(= C_{\rm GS} + C_{\rm GD})$, which is charged and discharged by the gate drive circuit for switching operation. $C_{\rm GD}$ is also equivalent to the reverse transfer capacitance $C_{\rm RSS}$. The effective capacitance is multiplied the voltage gain of the FET in switching operation by Miller effect. Also, $C_{\rm GD}(= C_{\rm RSS})$ and $C_{\rm DS}$ constitute the output capacitance $C_{\rm OSS}(= C_{\rm GD} + C_{\rm DS})$, which is charged and discharged by the load current, and governs the switching speed. Major part of these effective capacitance is originated from the junction capacitances in the semiconductor, which vary

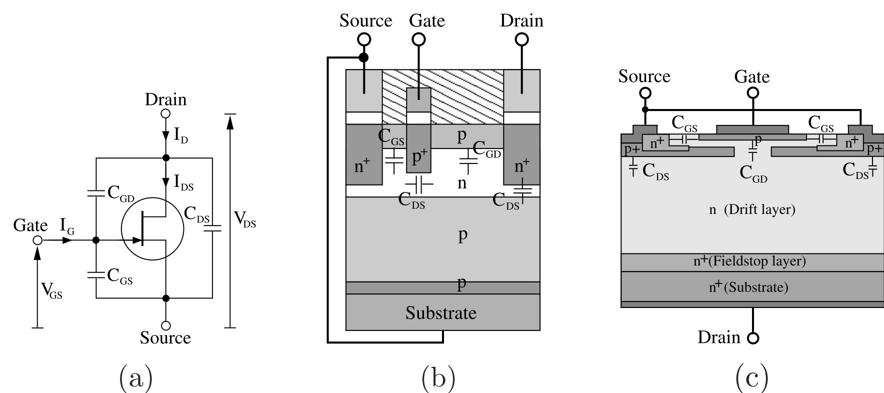

Fig. 1. (a) Equivalent parasitic terminal capacitances of JFET, (b) Cross section of lateral-type SiC JFET cell, and (c) Cross section of vertical-type SiC JFET cell.

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in accordance with the applied voltage. Therefore, the characteristics of terminal capacitances are substantial for understanding the switching behavior.

This paper characterizes the voltage dependency of terminal capacitances of SiC JFETs at first, then the switching behaviors are experimentally evaluated. Next, we discuss the C-V and switching characteristics based on their device structure and the semiconductor physics.

2 SiC JFET devices and setup for characterization

This section describes the specification of the discussed SiC JFET devices, and the experimental setup for characterizing the terminal capacitances and the switching behaviors of devices.

Figure 1 (b) shows the cross section of the lateral-type SiC JFET cell. The n-channel is formed between buried p^+ gate and p^- substrate. Their separation determines the n-channel thickness. The n-region between drain and source areas is designed to have a double reduced surface field (RESURF) effect to prevent electric field concentration [2]. Figure 1 (c) shows the cross section of the vertical-type SiC JFET cell. It has lateral and vertical channels. The lateral channel is sandwiched between p gate at the center top of the device and buried p^+ gate sections connected to the source terminal at the top of the drift region. The vertical channel is located between the two buried p^+ source regions.

The depletion region formed at pn junction behaves as parasitic capacitances, which are lumped into terminal capacitances C_{GS}, C_{GD}, and C_{DS}, as depicted in Fig. 1 (a). The thickness of depletion region changes with the applied reverse bias voltage V_{R} (V_{GS} and V_{DS}). The dependence of the depletion capacitance on the V_{R} can be expressed in the following compact form by Eq. (1) [3, 4]:

$$C = C_0\left(1 + \frac{V_{\mathrm{R}}}{V_{\mathrm{bi}}}\right)^{-m}, \tag{1}$$

where C_0 denotes the zero-bias capacitance, V_{bi} the built-in potential barrier, and m the junction grading coefficient. In addition, $m = 1/2$ is for the uniformly doped and $m = 1/3$ for the linearly graded doped.

Both SiC JFETs are limited to the normally-on type as mentioned above. The lateral-type SiC JFET has 0.006×60-mm in RESURF and $0.36\,\mathrm{mm}^2$ active area with 200 V blocking voltage and the rated 5 A drain current. The vertical-type SiC JFET has 2.32×2.32-mm in die size and $4\,\mathrm{mm}^2$ active area with 900 V blocking voltage and the rated 2.5 A drain current.

In the experimental setup for characterization, the C-V characteristics of both devices are precisely measured by a LCR meter with applying dc bias voltages V_{GS} and V_{DS} to the devices, through C-V measurement fixture in Ref. [5]. The measurements are performed with applying $V_{\mathrm{DS}} = 0\,\mathrm{V}$ to avoid short circuit current for V_{GS} dependency, and $V_{\mathrm{GS}} = -20\,\mathrm{V}$ to block the channel of devices for V_{DS} dependency. For characterizing the V_{GS} dependency, V_{GS} is swept from 0 V to -20 V for both SiC JFETs. For the measurement of V_{DS} dependency, V_{DS} is swept from 0 V to 200 V for lateral-type and from 0 V to 600 V for vertical-type.

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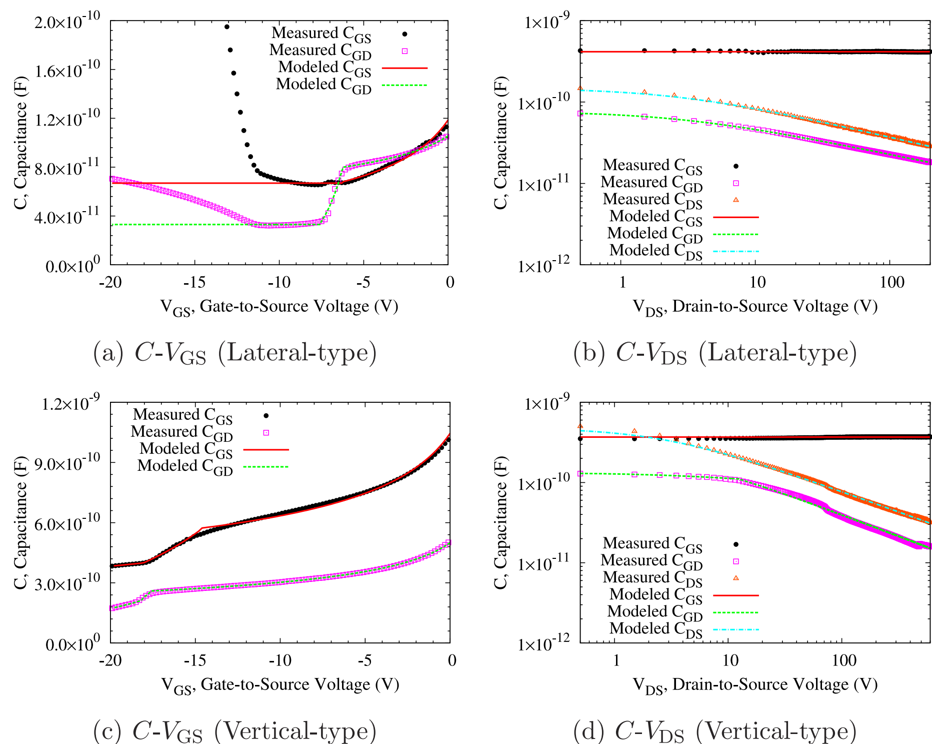
The switching characteristics of both devices are evaluated with the inductive load circuit, which is shown in Fig. 3 (a). Then V_{DS}, V_{GS}, and I_D are measured in the experiments. V_{AA} is varied with setting three different V_{DS} at 25 V, 50 V, and 75 V. Here, L_L is set at 200 nH and R_L at 103 Ω. V_{GG} applied to the gate of JFET through R_G 5 Ω is switched between 0 V and −20 V.

3 Results of *C-V* and switching characteristics of SiC JFETs

3.1 *C-V* characteristics

The measured and modeled C-V_{GS} characteristics are shown for both SiC JFETs in Figs. 2 (a) and (c). C_{GS} and C_{GD} decrease with negative V_{GS}, because the depletion region expands into the n-region facing at p^+ gate in Fig. 1 (b) and the n^--drift region facing to p gate in Fig. 1 (c). Then, C_{GS} and C_{GD} become constant around 66 pF and 33 pF for lateral-type, respectively. They become 400 pF and 200 pF for vertical-type, respectively. Because the channel area is fully depleted for $V_{GS} < V_T$ (cut-off condition). The V_T is approximately equal to −6.2 V for lateral-type and −17.6 V for vertical-type. C_{GS} and C_{GD} of lateral-type increase for $V_{GS} < -11.3$ V as shown in Fig. 2 (a). They stem from the leakage current at pn junction between gate and source. The capacitance model parameters of C_{GS} and C_{GD} are extracted for V_{GS} higher than cut-off voltage to neglect the influence of leakage current. They are $C_0 = 119$ pF, $m = 0.48$ (uniformly doped) and $C_0 = 106$ pF, $m = 0.24$ (linearly graded doped) for lateral-type, respectively. They are $C_0 = 1045$ pF, $m = 0.33$ (linearly graded doped) and $C_0 = 500$ pF, $m = 0.33$



(a) C-V_{GS} (Lateral-type) (b) C-V_{DS} (Lateral-type)

(c) C-V_{GS} (Vertical-type) (d) C-V_{DS} (Vertical-type)

Fig. 2. *C-V* characteristics of SiC JFET.

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(linearly graded doped) for vertical-type, respectively.

The measured and modeled C-V_{DS} characteristics for both SiC JFETs are shown in Figs. 2 (b) and (d). C_{GS} hardly changes with the variation of V_{DS}. The values are around 415 pF for lateral-type and 368 pF for vertical-type. Because the electric fields induced by V_{DS} does not affect on the electric field across gate and source due to the fixed V_{GS}. On the other hand, C_{GD} and C_{DS} decrease smoothly according to the increase of V_{DS}. The extracted capacitance model parameters of C_{GD} and C_{DS} are $C_0 = 77\,\mathrm{pF}$, $m = 0.34$ (linearly graded doped) and $C_0 = 148\,\mathrm{pF}$, $m = 0.38$ (linearly graded doped) for lateral-type, respectively. They are $C_0 = 278\,\mathrm{pF}$, $m = 0.55$ (uniformly doped) and $C_0 = 481\,\mathrm{pF}$, $m = 0.52$ (uniformly doped) for vertical-type, respectively. For the lateral-type in Fig. 1 (b), C_{GD} and C_{DS} change slightly with the variation of V_{DS}, because the depletion region expands from the linearly graded doped n-region to p^+ gate and n-region to p^- region, respectively. For the vertical-type in Fig. 1 (c), the n-channel is aligned in horizontal-axis, but the n-type semiconductor (n^- drift region) is aligned in vertical-axis. Therefore, C_{GD} has almost constant around 132 pF at $V_{\mathrm{DS}} \leq 13\,\mathrm{V}$, because the depletion region expands around the channel opened between the buried p^+ region for low V_{DS}. Then, C_{GD} changes substantially with the variation of V_{DS} when $V_{\mathrm{DS}} > 13\,\mathrm{V}$, because the depletion region expands from the p gate to the uniformly doped drift region. C_{DS} also changes substantially with the variation of V_{DS} in the low and high voltage ranges. It is because the depletion region expands from under the buried p^+ region to the uniformly doped drift region.

3.2 Switching characteristics

Figures 3 (b) and (c) illustrate the switching behaviors of both SiC JFETs for turn-off operation. The switching behaviors of both SiC JFETs are governed by the parasitic terminal capacitances (Fig. 1 (a)), which are the functions of the applied voltages between terminals. Eventually, the transient behavior of terminal voltages for both SiC JFETs can be represented by Eqs. (2) and (3) at charging/discharging states of the capacitances. When $V_{\mathrm{GS}} > V_{\mathrm{T}}$, JFET is conducting, then, $\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t} \approx 0$. V_{GS} changes as follows

$$\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t} \cong -\frac{V_{\mathrm{GS}} - V_{\mathrm{GG}}}{R_{\mathrm{G}}(C_{\mathrm{GS}}(V_{\mathrm{GS}}) + C_{\mathrm{GD}}(V_{\mathrm{GS}}))}. \tag{2}$$

When $V_{\mathrm{GS}} < V_{\mathrm{T}}$, JFET is blocked, V_{DS} is built up as follows

$$\frac{\mathrm{d}V_{\mathrm{DS}}}{\mathrm{d}t} \cong -\frac{V_{\mathrm{DS}} - V_{\mathrm{AA}}}{R_{\mathrm{L}}(C_{\mathrm{GD}}(V_{\mathrm{DS}}) + C_{\mathrm{DS}}(V_{\mathrm{DS}}))}. \tag{3}$$

$\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t}$ in Eq. (2) obviously depends on $C_{\mathrm{ISS}}(= C_{\mathrm{GS}} + C_{\mathrm{GD}})$ with variation of V_{GS}. The $\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t}$ is equal to $-2.83 \times 10^8\,\mathrm{V/s}$ (modeled) and $-2.50 \times 10^8\,\mathrm{V/s}$ (measured) for lateral-type in Fig. 3 (b). It is also $-3.14 \times 10^8\,\mathrm{V/s}$ (modeled) and $-3.59 \times 10^8\,\mathrm{V/s}$ (measured) for vertical-type in Fig. 3 (c). The simulated results by the model coincide with experimental results. The lateral-type has smaller $\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}t}$ than the vertical-type. Because C_{GS} and C_{GD} of lateral-type

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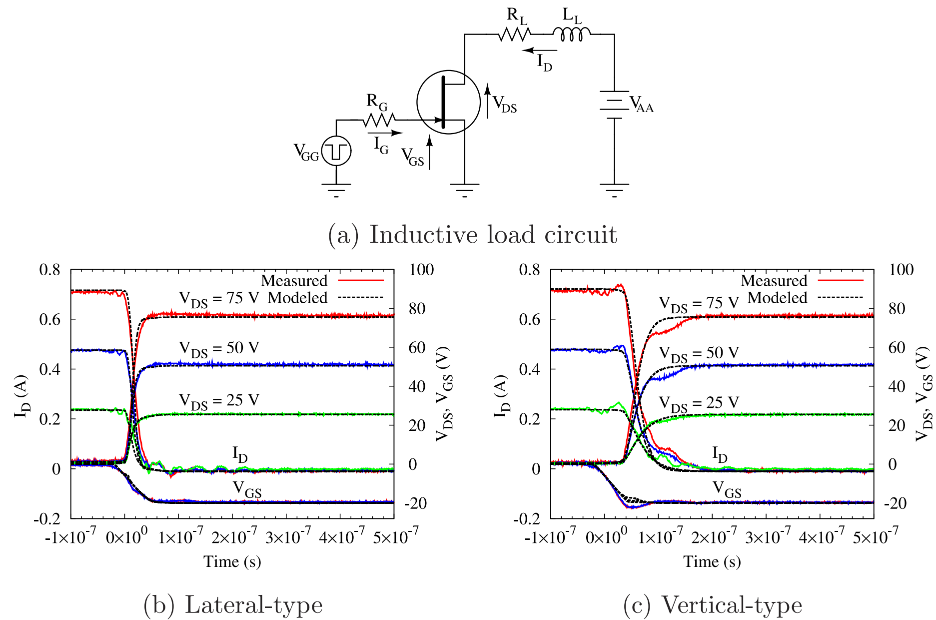

(a) Inductive load circuit

(b) Lateral-type

(c) Vertical-type

Fig. 3. Inductive load circuit and switching characteristics of SiC JFET.

SiC JFET increase substantially for $V_{\mathrm{GS}} < -11.3\,\mathrm{V}$ as mentioned above. The accumulated charge Q, calculated from gate voltage dependency of capacitance, is equal to 6.79 nC for lateral-type in Fig. 2 (a) and 19.15 nC for vertical-type in Fig. 2 (c). The lateral-type has smaller Q than the vertical-type. Because the lateral-type device has smaller C_{GS} and C_{GD} than the vertical-type while $V_{\mathrm{GS}} \geq -11.3\,\mathrm{V}$.

$\frac{dV_{\mathrm{DS}}}{dt}$ in Eq. (3) depends on $C_{\mathrm{OSS}}(= C_{\mathrm{GD}} + C_{\mathrm{DS}})$ with variation of V_{DS}. It affects on the switching behaviors when $V_{\mathrm{GS}} < V_{\mathrm{T}}$ (cut-off condition). It is obvious that Eqs. (2) and (3) cannot take the Miller effect into account. The $\frac{dV_{\mathrm{DS}}}{dt}$s for lateral-type in Fig. 3 (b) at V_{DS} 25 V, 50 V, and 75 V are equal to 7.89×10^8 V/s, 20.42×10^8 V/s, and 33.67×10^8 V/s by the model. They are 8.00×10^8 V/s, 17.06×10^8 V/s, and 23.88×10^8 V/s in the measurement. The $\frac{dV_{\mathrm{DS}}}{dt}$s for vertical-type in Fig. 3 (c) at V_{DS} 25 V, 50 V, and 75 V are equal to 3.07×10^8 V/s, 8.05×10^8 V/s, and 14.03×10^8 V/s by the model. They are 2.60×10^8 V/s, 5.71×10^8 V/s, and 10.47×10^8 V/s in the measurement. The model accurately explains the experimental results. The accumulated charges Q, calculated from drain voltage dependency of capacitance at V_{DS} 25 V, 50 V, and 75 V, are equal to 3.27 nC, 5.35 nC, and 7.09 nC for lateral-type in Fig. 2 (b). Those are 8.42 nC, 13.33 nC, and 17.12 nC for vertical-type in Fig. 2 (d). The ratios of $\frac{dV_{\mathrm{DS}}}{dt}$ between lateral-type and vertical-type are equal to 2.57, 2.53, and 2.40. The ratios of Q between both types are equal to 1/2.57, 1/2.50, and 1/2.41. Therefore, the ratio of turn-off speed of V_{DS} between SiC JFETs depends on the inverse ratio of Q. The lateral-type shows about 2.5 times faster turn-off speed than the vertical-type. Because the lateral-type has smaller C_{DS} and C_{GD} than the vertical-type as mentioned in section 3.1.

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4 Conclusions

This paper characterized and discussed the switching characteristics of SiC JFETs through the voltage dependency of terminal capacitances. The difference between the switching characteristics of the lateral-type and the vertical-type SiC JFETs depends on their internal parasitic capacitances, which can be classified by the dependence of depletion capacitance. Therefore, the device structure and switching phenomenon can be characterized and explained for these SiC JFETs by the measurement of C-V characteristics of devices.

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