High Frequency Switching of SiC Transistors and its Application to In-home Power Distribution

TAKUNO Tsuguhiro

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Abstract

Energy consumption has been steadily increasing year by year over the last decades. In particular, the demand for electrical energy is increasing due to the spread of home electrical appliances. However, environmental issues necessarily restrict energy consumption. As a result, alternative energy sources need to be considered, and the utilization of natural and renewable energy sources have been promoted. Along the situation, in-home electricity distribution systems are required to reduce total power consumption and, at the same time, to properly balance the production and consumption of individual households. To satisfy the requests, the information about demanded power and available supplies should be gathered. Power packet distribution is suggested as one of the solution to the problem, which is based on the method of packet transmission via information and telecommunications networks.

In this dissertation, two types of energy management systems are proposed and implemented in order to achieve the power packet dispatching. The system requires not only high-speed switching of power but also high-frequency switching for signal transmission. For the application, switching characteristics of normally-on SiC JFET are evaluated as basic element of the system. A gate driver circuit is newly designed for operating normally-on deices safely at high frequency. The JFET are tested under two types of circuit configuration, hard-switching circuit and class-E switching circuit as an example of soft-switching circuit. The experiments demonstrated the switching of 50 W of resistive load at 15 MHz.

At the end, the implemented power management system in which the JFETs are embedded exhibited the capability of power packet dispatching.

Keywords: SiC JFET, high-frequency switching, power conversion, class-E switching, power flow control in home, power packet

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Contents

Acronyms

List of frequently used acronyms in alphabetical order:

ac	Alternative Current
BJT	Bipolar Junction Transistor
dc	Direct Current
DUT	Device Under Test
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transformation
HEMS	Home Energy Management System
IPS	Intelligent Power Switch
JFET	Junction Field Effect Transistor
LCC	Laminated Ceramic Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PLC	Power Line Communications
PV	Photovoltaic
PWM	Pulse Width Modulation
RESURF	Reduced Surface Field
RF	Radio Frequency
SBD	Schottky Barrier Diode
Si	Silicon
SiC	Silicon Carbide
TDM	Time Domain Multiplexing
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

Our modern society has been developing on the basis of progresses in power electronics and information technology. The early-modern information technology begins with electric telegraph in the 19th century [1]. The invention of Morse code and the telecommunications system using it by Samuel F. B. Morse in 1830s expanded the electric telegraph rapidly [1]. Afterward, the development of telephone and subsequent information technologies brought telecommunications closer to the people. The early information technology was based on primitive digital technique, that is, opening and closing of a circuit in a transmitter. Then, it changed to analog communication system gradually. From the late 1950s digital system took over again [2]. The growth of digital communication technologies brought us World Wide Web, mobile phones, and other various wired or wireless means of telecommunications.

On the other hand, the history of electric power distribution started with the argumentation about superiority of dc and ac transmission by Thomas A. Edison and Nikola Tesla in the late 1880s. Consequently, ac transmission became mainstream and it continued up to present power distribution systems. The development of the silicon-controlled rectifier (SCR) by General Electric (GE) in 1958 was the beginning of power electronics [3]. Afterward, the development of power electronics enabled us to control electricity easily by utilizing power conversion circuits. According to the growth of semiconductor active switches, GW-class power conversion plants have been developed and adopted in power grids. For a long time, power distribution network connects large power stations and provides single-phase or three-phase constant-frequency fixed-voltage ac power up until now. Resent introduction of dispersed power sources in power grids have been changing the environment surrounding power distribution. However, power distribution technology

still remains on the basis of analog theory. This dissertation aims to expand power distribution systems using digital technology, and to unify the power distribution and the information transmission.

1.1 Local Electric Power Generation and Energy Management in Home

Energy consumption has been steadily increasing year by year over the last decades [4, 5]. In particular, the demand for electrical energy is increasing due to the spread of home electrical appliances. Also, new types of demands for electricity appear with growing use of plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs). However, environmental issues necessarily restrict energy consumption. As a result, alternative energy sources need to be considered, and the utilization of natural and renewable energy sources have been promoted. Examples of natural and renewable energy sources include photovoltaic panels, wind-power generators, and fuel cells [6, 7]. Secondary batteries are also employed to temporarily accumulate the generated power for load leveling. These trends accept the appearance of small power sources in the consuming area.

On the other hand, electric power utility companies have operated huge-capacity power plants and regulated supplying power to be compliant with load requirements for keeping the frequency and the voltage of distribution grid stable in power systems. In the situation, fluctuations in the voltage and the frequency are well suppressed by the control of power flows. The conditions surrounding power distribution grids, however, can not be the same as before. This is because the outputs of linked natural and renewable sources are strongly affected, for instance, by the weather conditions, which cause fluctuations in quantity, frequency, and voltage. Therefore, the more natural and renewable energy sources are connected to a power grid, the less qualities of frequency and voltage in power flows become. These renewable energy sources are similarly introduced in households. Spreading renewable and distributed energy sources among homes implies that houses and buildings are no longer only loads, but also power sources producing power flows in the opposite direction toward the main grid. In this situation, it is difficult for power utility companies to keep the balance between demand and supply. It is unavoidable to regulate the power generated by renewable sources and consumed by home appliances in order for a home to continue being a suitable consumer from the point of view of the

Table 1.1: Comparison of the degree of power and frequency in information transmission and power distribution in home.

	Power distribution	Information transmission
Power	$\mathrm{W} \sim 10\,\mathrm{MW}$	$\mu\mathrm{W} \sim \mathrm{W}$
Frequency	$10\,\mathrm{Hz} \sim \mathrm{MHz}$	$\mathrm{MHz} \sim \mathrm{GHz}$

distribution system. As a result, in-home electricity distribution systems are required to reduce total power consumption and, at the same time, to balance the production and the consumption of individual households properly.

Home energy management systems (HEMS) take on an important role in this situation. HEMS [8, 9] and management of smart grids [10] are hot topics. Handling power flows requires measurements and predictions of the power generated and demanded. J. Bialek has proposed the method of tracing power flows in a power grid for analyses of the cause of deregulation and unbundling in power transmission [11]. This method gave the amount of the real and the reactive power flowing from a particular generator to a particular load under the assumption that Kirchhoff's Current Law is always satisfied at any nodes in the transmission network and the power is shared proportionally at the nodes depending on the impedance of each line connected to the nodes. Most of these ideas base on observation of the quantity of electric power only. Moreover, the quantities are observed at given points such as outlets of generators, junctions of transmission lines, and input terminals of loads. These measurements assure the amounts of power flows only at the points and do not guarantee them on transmission lines between the observing points. In this dissertation, the quality of energy is focused on in addition to the quantity of energy. Here, the quality in electric power implies maximum available supplying power, frequency variation, and voltage fluctuation. In addition, the constant identification of amount of power is considered.

Power packet distribution is suggested as one of the solutions to the problem, which is based on the method of packet transmission via information and telecommunications networks. The concept of packetization has been proposed in [12,13] for trading of electric power in high-voltage power transmission networks. The key of the idea is "packetization" and "tagging". The former means dividing a power flow in arbitrary amount. The latter represents the attachment of the tag which records a destination and the amount of power to a power packet. Following the idea, a power line router has been presented based on

a matrix converter [14]. There is also an estimation on packet power distribution with pulse-shaped power transmission [15]. For dc power feeding in a data center, the power routing by changing the topology of power feeding network has been studied for reducing reserve capacity margins and redundancy of the network [16]. He *et al.* proposed the Intelligent Power Switch (IPS), which has both capabilities of an Internet router and a power conversion with protection equipment [17]. The IPS is also experimentally studied for simulating Smart Grid by small power electrical circuit [18]. In the study, solid state relays are employed for power switches in the IPS and information is transmitted by means of radio communication, separately. These researches are mostly theoretical or numerical simulation based studies. In the case of experimental studies, special communication paths are employed other than power line. Indeed it has been difficult to realize practical hardware to deal with information as same as electric power up to now. This is because there are differences between power distribution and information transmission in magnitude of power and modulating frequency as listed in Table 1.1, although they have been similalities in an aspect of electric signal. The packetization requires high switching frequency enough to generate pulses and high power switching capabilities, but there have been hitherto no switching devices capable of both functions. Therefore, the power devices which have features superior to conventional Silicon (Si) devices are required to make them come true.

1.2 SiC Power Switching Devices

Wide bandgap semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have been expected to be the next generation of power devices due to their superiority of; for example, high withstand voltage, high current density, high-frequency operation capability, and high temperature durability, to Si based power devices [19–27]. Silicon Carbide semiconductor devices are most attractive for applications to power conversion among the wide bandgap devices. SiC semiconductor has a couple of polytypes. The electrical and material properties depend on the crystal alignments. Some of the properties of Si and two main polytypes of SiC are listed in Table 1.2.

For the applications of the advantages of SiC semiconductor, SiC diodes, especially Schottky Barrier Diodes (SBDs), have been studied [28, 29] and were released as one of commercial SiC passive switches [30–32]. Various types of active switches have also

Table 1.2: Comparison of the electrical and material parameters of Silicon, 4H-SiC, and 6H-SiC [19, 21, 24, 28] at 300K.

Parameters	Si	4H-SiC	6H-SiC
Energy band gap (eV)	1.12	3.23	2.90
Intrinsic carrier concentration (cm^{-3})	10^{10}	1.5×10^{-8}	2.1×10^{-5}
Electron mobility (cm^{-3})	1400	947	415
Hole mobility (cm^{-3})	450	124	99
Relative dielectric constant	11.7	9.66	9.66
Saturated drift velocity (10^7cm/s)	1.0	2.1	2.0
Critical breakdown field (MV/cm)	0.25	2.2	2.5
Thermal conductivity ($W/cm \cdot K$)	1.5	3.7	3.7

been studied and some of them have been commercially manufactured. Among them, the normally-on SiC Junction Field Effect Transistor (JFET) connected with Si Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in series, that is, cascode configuration, appeared in the market first [33,34]. The single SiC JFET have been also studied on both normally-on and normally-off types [25, 35–38] and been also in the market [32, 39]. In SiC unipolar devices, MOSFETs have also been focused on [24, 36, 40] and commercial devices are now available [30]. SiC bipolar devices such as Bipolar Junction Transistors (BJTs) and Gate Turn-Off (GTO) Thyristors have been also subject of research [23, 36]. BJTs are now available in the market [41].

SiC JFET, MOSFET, and SBD proves their capability of operation under harsh environment by the experiments [40, 42]. Compared with Si power devices, SiC power devices exhibit that they improve performances of conversion circuits [43–46]. These results will open the path to integration of power feeding with telecommunications.

1.3 Purpose and Outline

This dissertation aims to realize power distribution based on the information of power and coincidence of transmitting information with power distribution. For the purpose, the application of SiC power devices to power conversion circuits is key technology. To begin with, the switching characteristics of SiC power transistors are evaluated for high-frequency power switching. In the evaluation, hard-switching type circuit is compared to resonant switching circuit with respect to efficiency and noise emission. Then the idea

of energy flow control is introduced in order to utilize distributed power generation in home, keeping up with demands of the amount and the quality of power from electric appliances. Electricity management systems are designed for achieving the idea based on ac power distribution and dc power dispatching. Finally, the systems examine the principle of power management.

Chapter 2 introduces a new architecture of gate driving circuit for high-frequency switching of normally-on SiC JFETs. This driver targets the operation at more than 5 MHz and the protection of power circuit from normally-on devices. Employing insulated signal coupler using RF signal instead of opto-coupler enables to drive SiC JFET up to 15 MHz. Special arrangements of the driver also enables normally-on devices to operate as same as normally-off devices.

Chapter 3 expresses the high-frequency hard switching of the SiC JFET. A couple of samples of the SiC JFET are experimentally studied on their switching characteristics of operation frequency from 1 MHz to 15 MHz by using gate drive circuit designed in Chapter 2 under resistive load. The parasitic elements in the device and the circuit are studied with respect to influences on oscillation of switching waveforms. Then the energy dissipation are evaluated during a switching with respect to the switching frequency.

In Chapter 4, a class-E switching circuit is introduced as one of the soft-switching circuits in order to reduce switching loss and higher harmonics emission. The same samples as used in Chapter 3 are examined, driven by the gate driver designed in Chapter 2. Physical principles and circuit equations of the class-E power amplifier are expressed to design the circuit. The operations of the power amplifier are simulated numerically to design circuit parameters because the parameters which satisfy class-E operation conditions are sensitive to parasitic elements in each component of the circuit. Then the circuit implemented on a printed circuit board (PCB) and measured their voltage and current waveforms. The waveforms analyzed in both time domain and frequency domain for estimation of harmonic components. The efficiency is also calculated and compared to that in the case of hard-switching.

In Chapter 5, the novel concept of in-home power management systems are presented to utilize renewable and natural power sources and reduce conversion losses in inverters and converters which spread all over the power distribution system in home and electrical equipments. To begin with, we advance the power distribution referring to the quantity and the quality of power. That means to match the supplied power to the demanded power

with respect to not only the amount but also frequency, voltage, permissible fluctuations of them, and so on. This method brings coexistence of power flows which differ in voltage, frequency, and so on in a distribution network. Therefore, some kind of multiplexing of power flows is required and the information of the power should be transmitted with the power in order to deliver electricity to the specified load. Two types of power management systems are proposed for achieving the multiplexing. One of them is the ac power switching circuit and the other is the dc power packet dispatching system. The former multiplexes power spatially and the communication is established by power line communications (PLC). The latter achieved by time division multiplexing of power packet and the information is included in the packet. The prototypes of the hardware which realize the two systems demonstrate the power feeding based on the information.

Chapter 6 concludes this dissertation. Some proposals for the future works are also presented.

Chapter 2

Insulated Gate Driving Circuit for Normally-on Power Devices

In this chapter, a design of a gate driving circuit is introduced in terms of high-frequency operation for normally-on devices. Optical couplers usually insulate a control logical circuit from a main high-current circuit in conventional gate drive circuits. However, the response speed of an LED and a photo transistor in a photo coupler is a bottleneck for high-frequency switching. Moreover large drive current is required in order to charge and discharge the input capacitor of the semiconductor switch as rapid as possible for fast turn-on and turn-off. Therefore, new architectures of insulated gate drive circuits are necessary instead of optically-based insulation circuit. The configuration introduced here employing radio frequency (RF) signal will be one of the solutions for above issues.

2.1 Introduction

Wide bandgap semiconductor devices have superiority in regards to their electrical and material characteristics to conventional devices such as Si semiconductor devices. They have capabilities; for example, high temperature, fast turn-on and turn-off, high switching frequency, and high withstand voltage operating [22, 34]. The SiC semiconductor device is one of the possible wide bandgap semiconductor devices applied in power conversion circuits.

As one of SiC passive switches, Schottky barrier diodes have already been provided for commercial use. Next to diodes, some active power switching devices such as JFETs and BJTs have gradually been produced for practical applications. Among SiC power switches, JFETs are expected as feasible devices compared with MOSFETs and BJTs up

to now. This is because SiC MOSFETs still have some problems such as an instability of oxide layer and higher on-state resistance than JFETs [22, 23, 47]. Therefore SiC JFETs are mainly studied in this dissertation.

Generally, JFETs are normally-on devices, which may cause a risk of failing to turn off circuits when their gate drive circuits are breakdown. The failure of switching may bring on severe damage on high power circuits from impossibility of shutting large current. Additionally, negative voltage is required between gate and source in order to turn off normally-on JFET. Hence designing circuits using normally-on devices needs special attention. To avoid these issues, devices having capability of normally-off operation have been developed from the point of device design. The cascode connection of an SiC JFET and an Si MOSFET is proposed as one of solutions for achieving normally-off operation [33]. However, it has several disadvantages as follows. There is a limitation of operating temperature depending on the Si MOSFET. The maximum switching frequency and switching speed is limited by performance of the Si MOSFET. On-state resistance increases due to series connection of two devices. It was also reported that the available cascode device shows undesired oscillation caused by the negative resistance of the parasitic body diode on the Si MOSFET at the moment of turning off depending on parameters [34]. Normally-off SiC JFETs were also developed and applied to three phase inverter circuit [35]. Normally-off JFETs have fine structure in their channel. The fine structure increases on-state resistance of the device. Hence, normally-on SiC JFETs are still more common than normally-off devices. Consequently, specially designed gate drivers for normally-on devices are required to avoid the issues. Along the plot, gate drive circuits with protection have also been studied for applications of normally-on SiC JFETs to power conversion circuits [48–55].

In this chapter, a simple structure gate drive circuit is designed and developed to have capabilities as follows:

- to insulate gate terminal of a device from gate control circuit,
- to turn on or off devices at the frequency more than 5 MHz,
- to operate normally-on devices safely as close as normally-off devices.

Target devices of the driver are normally-on SiC JFETs, of which gate-to-source threshold voltage V_{gsTH} is around $-10\,\mathrm{V}$. The drive circuit is mainly composed of a commercial gate driving device.

2.2 Architecture and Operation of Gate Driving Circuit

2.2.1 Architecture

Figure 2.1 shows a schematic diagram of the proposed gate drive circuit and Fig. 2.2 is a photograph of the driver circuit. This configuration simply consists of a gate driving IC, which does not require extra circuit elements except for decoupling capacitors. Here, Si8235, provided by Silicon Laboratories [56], is used as a isolated gate driving device. This device has two independent gate control channels in a Small Outline Integrated Circuit (SOIC) package. The device is designed to operate up to 8 MHz of frequency. The ground plane of the input side is separated from that of the output side in order to prevent switching noise from propagating to the switch control circuit and permit the voltage difference between two ground planes. The ground plane under the IC is also removed for noise immunity.

Fig.2.3 is a circuit block diagram for single channel of the device. The channel consists of three stages: Transmitter, Receiver, and Driver. As shown in the diagram (Fig. 2.3), the circuit is insulated between the Transmitter and the Receiver by the semiconductor-based isolation barrier. The RF signal is employed for the gate control signal transmission between the modulator and the demodulator instead of light in optical couplers. This method shortens the propagation delay and increases the operation frequency by avoiding photo transistors, whose response speed is slow. The modulator transforms input gate control logic signal v_{sig} into RF carrier using on/off keying. The modulation scheme is shown in Fig. 2.4. When v_{sig} is higher than the threshold voltage, the RF signal produced by the RF oscillator is enabled and transmitted to the demodulator. The demodulator receives the RF signal and decodes it into original square waveform [56].

V_{DDin} is an input constant-voltage source, which feeds the IC itself. The permissible range of it is from 4.5 V to 5.5 V. The output power source V_{DDout} is for supplying current to charge and discharge gate capacitors of devices. V_{DDout} must be within the range from 6.5 V to 24 V. It accepts only positive voltage so that it can use only for monopoler gate driving. These two power sources are isolated from each other. Two ground planes, the input side $\mathrm{GND_{in}}$ and the output side $\mathrm{GND_A}$, are also divided. As mentioned above, the output side of the device is perfectly insulated from the input side. The insulation ideally guarantees that the switch control circuit is less affected by conduction noise caused by

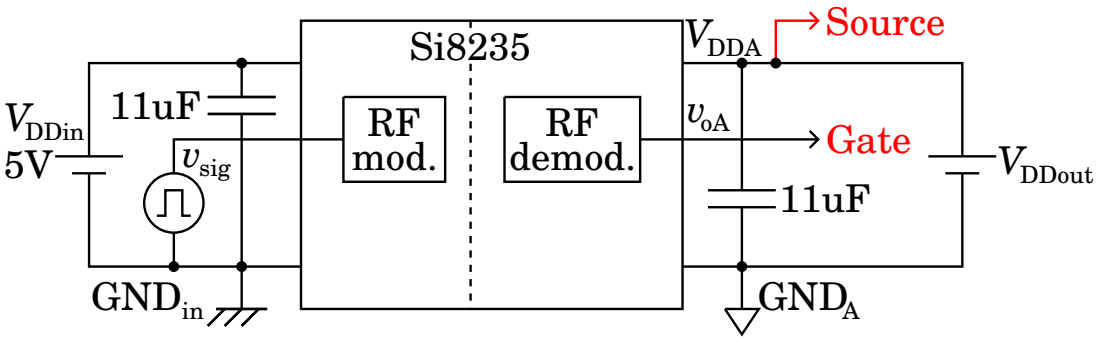


Figure 2.1: Schematic diagram of gate drive circuit. The circuit simply consists of a gate driving IC and decoupling capacitors.

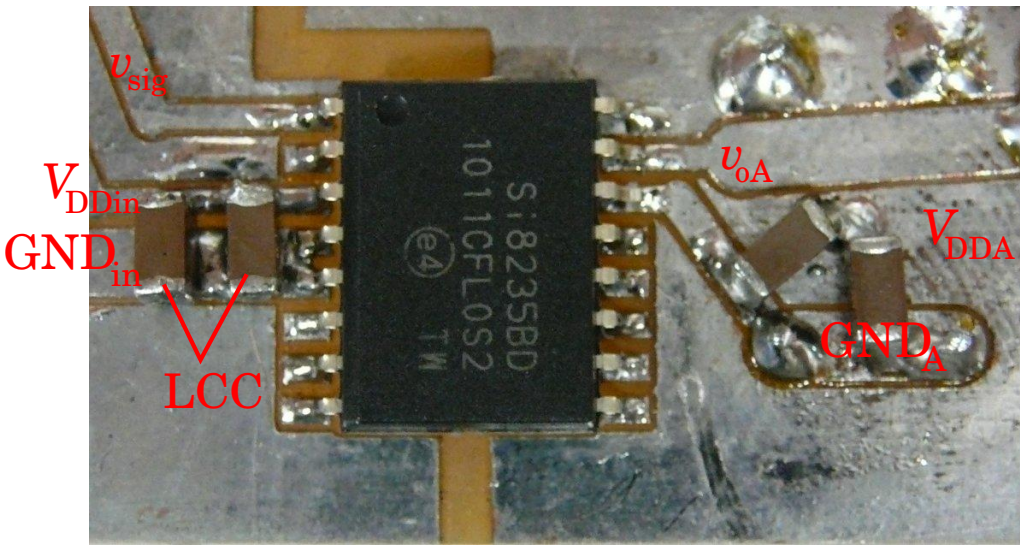


Figure 2.2: Photograph of gate drive circuit. The gate driver is packaged in a wide-body small outline integrated circuit. Chip laminated ceramic capacitors are added for decoupling. The ground plane of the input side and that of the output side are divided for noise blocking. Under the IC, there is no ground plane neither.

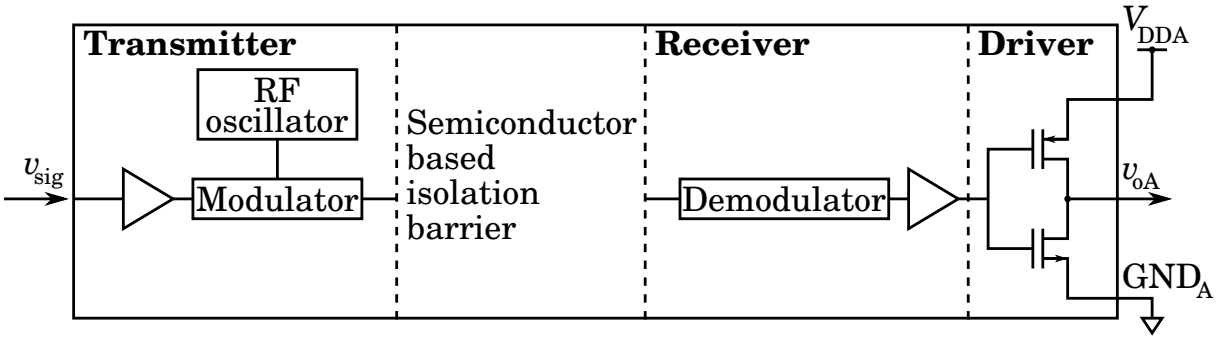


Figure 2.3: Block diagram of structure of gate driving IC Si8235 [56]. A channel consists of Transmitter, Receiver, and Driver stages. Between Transmitter and Receiver are divided.

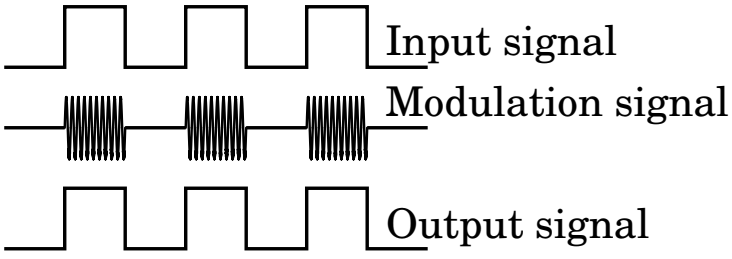


Figure 2.4: Modulation scheme of gate driving IC Si8235 [56]. The input signal is transmitted to the output by RF on/off keying.

high-frequency switching of power devices. It also allows driving the transistor of which the gate terminal is not connected with any ground plane.

Laminated ceramic capacitors (LCCs) of 11 μF, which consist of a parallel connection of 10 μF and 1 μF, are inserted as decoupling capacitors in parallel with the input and the output power sources V_{DDin} and V_{DDout} for supplying the IC with current immediately and suppressing harmonic noise to keep stable the operation of the driver. The driver supplies a transistor with current up to 4 A, which is large enough to charge gate capacitors of transistors.

The IC has several Ohms of resistance parasitizing internal wiring. This is why transistors connect to the driver directly without any external gate resistance.

2.2.2 Operation

The relationship of the input gate signal v_{sig} and the output signal v_{oA} is defined as follows:

$$v_{\mathrm{oA}} = \begin{cases} 0 & (v_{\mathrm{sig}} < V_{\mathrm{sigTH}}), \\ V_{\mathrm{DDA}} & (v_{\mathrm{sig}} \geq V_{\mathrm{sigTH}}), \end{cases} \tag{2.2.1}$$

where V_{sigTH} is the input signal threshold voltage.

Generally, the output (v_{oA}) terminal is connected to the gate of a transistor. And $\mathrm{GND_A}$ is connected to the source of the transistor. In contrast, for operating normally-on devices, the output of the gate drive circuit is connected to the gate terminal of an SiC JFET and the high potential side of V_{DDout} is connected to the source terminal of the SiC JFET as shown in Fig. 2.1 with red color. Then, the voltage difference between the gate and the source of the JFET v_{gs} becomes as follows:

$$v_{\mathrm{gs}} = v_{\mathrm{oA}} - V_{\mathrm{DDA}} = \begin{cases} -V_{\mathrm{DDA}} & (v_{\mathrm{sig}} < V_{\mathrm{sigTH}}), \\ 0 & (v_{\mathrm{sig}} \geq V_{\mathrm{sigTH}}). \end{cases} \tag{2.2.2}$$

As a result, the JFET is turned off at $v_{\mathrm{sig}} < V_{\mathrm{sigTH}}$ and turned on at $v_{\mathrm{sig}} \geq V_{\mathrm{sigTH}}$. Thus, the input gate signal to a normally-on JFET operates the same as the signal to a normally-off device. Therefore, circuits with normally-on switches can be controlled safely in so far as the input and output power are supplied to the IC.

The timing chart of the input logic signal and the output signal are roughly shown in Fig. 2.5. In the figure the red line shows v_{sig} and the green line v_{gs}. The propagation delay of signal transferring from input to output is unavoidable due to the modulation, the demodulation, and the output buffer in the Driver stage. Its typical value is specified to

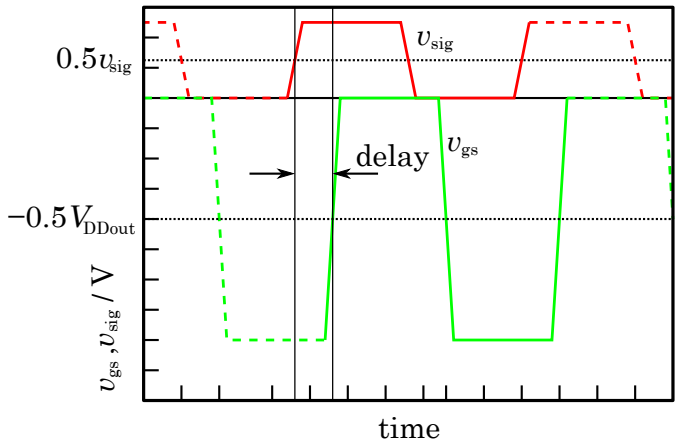


Figure 2.5: Schematic waveforms of input signal v_{sig} (red) and output signal v_{gs} (green) of gate drive circuit.

be around 30 ns in design [56]. The delay possibly induce some problems. For instance, in a closed loop feedback controlled pulse width modulation (PWM) system, a pulse width is calculated by microprocessors based on sampled state variables, such as voltages and currents to make the output voltage follow the desired value. In the case of huge delay, the sampled state variables is different from the values at the moment of switching. The delay limits the maximum available pulse width. This becomes worse with higher switching frequency. It may cause deviations of an effective PWM gain, which induce substantial distortion in the output voltage and affects system performance [57, 58]. Therefore, the delay should be much shorter than the gate control pulse width.

2.2.3 Power Dissipation

The estimation of power dissipation of the driver helps to design the circuit and anticipate the operating limit. The total power dissipation of the driver circuit is the sum of power dissipated by the bias current, internal switching losses, and load switching losses.

The total dissipation of the driver per channel P_{loss} is as follows:

$$P_{\mathrm{loss}} = \underbrace{V_{\mathrm{DDin}} I_{\mathrm{Bin}} + V_{\mathrm{DDout}} I_{\mathrm{Bout}}}_{\text{dissipation of bias current}} + \underbrace{C_{\mathrm{int}} V_{\mathrm{DDout}}^2 f_{\mathrm{sw}}}_{\text{internal switching loss}} + \underbrace{C_{\mathrm{L}} V_{\mathrm{DDout}}^2 f_{\mathrm{sw}}}_{\text{load switching loss}}, \quad (2.2.3)$$

where I_{Bin} is the input bias current, I_{Bout} the driver die bias current, C_{int} the internal parasitic capacitance, f_{sw} the switching (operation) frequency, and C_{L} the load capacitance. The typical values of them are listed in Table 2.1.

Table 2.1: Electrical and thermal characteristics of Si8235 [56]

Parameter		Value
I_{Bin}	input bias current	3 mA
I_{Bout}	driver die bias current	2.5 mA
C_{int}	internal parasitic capacitance	75 pF
T_{jmax}	maximum junction temperature	150 °C
θ_{ja}	junction-to-air thermal resistance	100 °C/W

The temperature of the IC is one of restrictions of the operation. It is determined by the power dissipation, the thermal resistance of the package, and the ambient temperature. Therefore, the maximum allowable temperature defines the maximum permissive power dissipation. The maximum power dissipation P_{lossmax} is represented by:

$$P_{\mathrm{lossmax}} \leq \frac{T_{\mathrm{jmax}} - T_{\mathrm{a}}}{\theta_{\mathrm{ja}}}. \tag{2.2.4}$$

Here, T_{jmax} means the maximum junction temperature of the IC, T_{a} the ambient temperature, and θ_{ja} the junction-to-air thermal resistance. Their typical values are shown in Table 2.1.

Substituting Eq. (2.2.3) in Eq. (2.2.4) results in the maximum operable load capacitance C_{Lmax} as follows:

$$C_{\mathrm{Lmax}} = \frac{T_{\mathrm{jmax}} - T_{\mathrm{a}}}{\theta_{\mathrm{ja}} V_{\mathrm{DDout}}^2 f_{\mathrm{sw}}} - C_{\mathrm{int}} - \frac{1}{f_{\mathrm{sw}}} \left(\frac{V_{\mathrm{DDin}}}{V_{\mathrm{DDout}}^2} I_{\mathrm{Bin}} + \frac{I_{\mathrm{Bout}}}{V_{\mathrm{DDout}}} \right). \tag{2.2.5}$$

Substitute the values in Table 2.1 into Eq. (2.2.5) and assume that T_{a} is the room temperature, that is, 27 °C and V_{DDin} is set at typical value, 5 V. Then C_{Lmax} is obtained as:

$$C_{\mathrm{Lmax}} = \frac{1}{f_{\mathrm{sw}}} \left(\frac{1.215}{V_{\mathrm{DDout}}^2} - \frac{2.5 \times 10^{-3}}{V_{\mathrm{DDout}}} \right) - 3.7 \times 10^{-10}. \tag{2.2.6}$$

Figure 2.6 depicts the maximum load capacitance versus the operation frequency with the output voltage. The higher the output voltage increases, the less the load capacitance can be operated at each frequency. Here, the load capacitance corresponds to an input capacitance of a semiconductor device C_{iss}. The input capacitor is represented by the parallel connection of gate-to-source and gate-to-drain parasitic capacitors of the device. V_{DDout} depends on the gate-to-source threshold voltage. Therefore, selection of a device

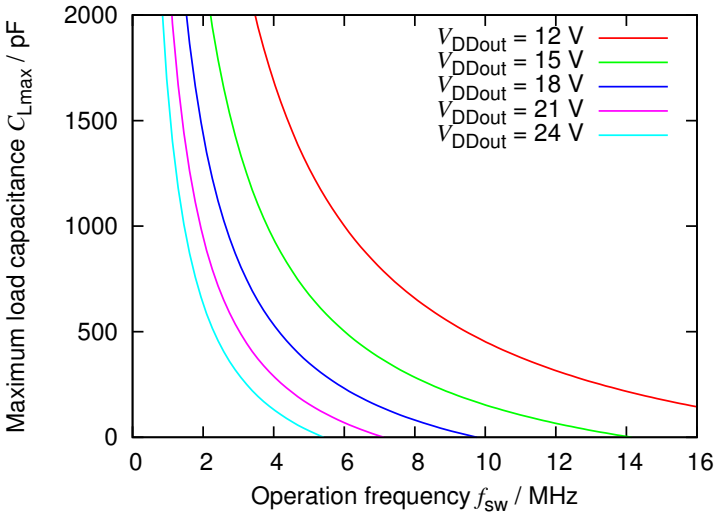


Figure 2.6: Maximum load capacitance versus operation frequency with output voltage variation calculated with Eq. (2.2.6).

determines the operating frequency limit. Small input capacitance and low threshold voltage enable the driver to operate at high frequency.

2.3 Experimental Results of Driving Operation

2.3.1 Experimental Settings

An unloaded SiC RESURF (Reduced Surface Field) JFET is driven by the designed gate driving circuit in order to examine the driving ability of the circuit. The schematic diagram of a testing circuit is shown in Fig 2.7. The test carried out using a couple of samples. The devices are developed and produced by Sumitomo Electric Industries, Ltd. In this configuration, a load capacitance is C_{iss} of the sample, which is around 200 pF at $V_{\mathrm{gs}} = 0$ measured in [59]. The gate-to-source threshold voltages of them are different from device to device because they are still under development. The range of V_{gsTH} is from -12 V to -7 V. In experiments, v_{sig} is given as square wave by function generator (KENWOOD; FG-281). Its amplitude is set at 5 V and the duty ratio is 50%. V_{DDout} is fixed to be 16 V and supplied by stabilized power supply (TEXIO; PA18-3B). The voltage is large enough to shorten the turn-off time of the JFET. Fig. 2.6 indicates that the maximum operation frequency is around 12 MHz in terms of the heat produced by losses.

Table 2.2: Output rise and fall times and propagation delay of Si8235 under $C_{\mathrm{L}} = 200\,\mathrm{pF}$, $4.5\,\mathrm{V} < V_{\mathrm{DDin}} < 5.5\,\mathrm{V}$, $V_{\mathrm{DDout}} = 12\,\mathrm{V}$. "—" in the table means that the value is not indicated in the datasheet [56].

Parameter		Minimum	Typical	Maximum
t_{R}	output rise time	—	30 ns	60 ns
t_{F}	output fall time	—	—	20 ns
t_{delay}	propagation delay	—	—	12 ns

2.3.2 Results of Driving Operation

Figure 2.8 shows the measured waveforms of v_{sig} and v_{gs} at the operation frequency of 5 MHz. A red line indicates v_{sig} and green v_{gs}. The output rise time t_{R} is defined as an interval from the cross point of rising v_{gs} with -90% level to the cross point of rising v_{gs} with -10% level. Similarly, the output fall time t_{F} is an interval from when v_{gs} reaches to -10% level of falling edge to when v_{gs} crosses -90% level of falling edge. The propagation delay t_{delay} is defined as the time span from the cross point of rising v_{sig} with 50% level of its amplitude to the cross point of rising v_{gs} with 50% level of its amplitude. t_{R}, t_{F}, and t_{delay} obtained by the measurement are 5.6 ns, 4.9 ns, and 17.2 ns, respectively. These values are within the typical ones of Si8235 listed in Table 2.2. The rise and fall times are sufficiently short even in the case of operating actual SiC JFETs. The propagation delay is also substantially small compared to a cycle of the operation frequency, i.e. 200 ns. Even in the case of operation at 8 MHz, the delay is just around 14% of the cycle. These results support that the candidate gate driver is eligible for normally-on devices at high-frequency operation.

Measurements at more than 8 MHz up to 15 MHz was carried out to examine practical operation limit. The frequency 15 MHz is limit of generating frequency of the function generator (FG-281). Figure 2.9 is measured waveforms at 15 MHz. This figure suggests that the circuit has capability of operation at 15 MHz however the designed frequency of the gate driving IC is 8 MHz and the limitation with respect to thermal production. Note that the operation at the frequency more than 12 MHz makes the IC heat up because of losses explained in Section 2.2.3. This issue can be solved by attaching a proper heat sink on the IC.

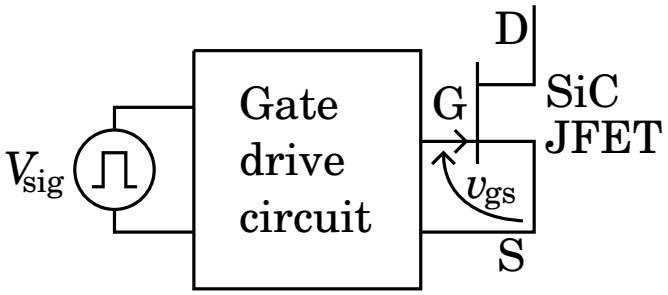


Figure 2.7: Testing circuit for operation of gate drive circuit. The load of the driver circuit is an input capacitance of an unloaded JFET.

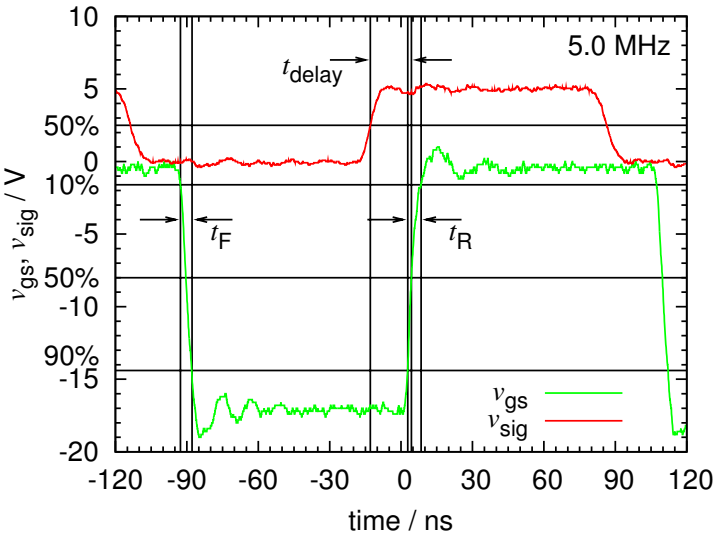


Figure 2.8: Measured waveforms of v_{sig} (red) and v_{gs} (green) at 5 MHz.

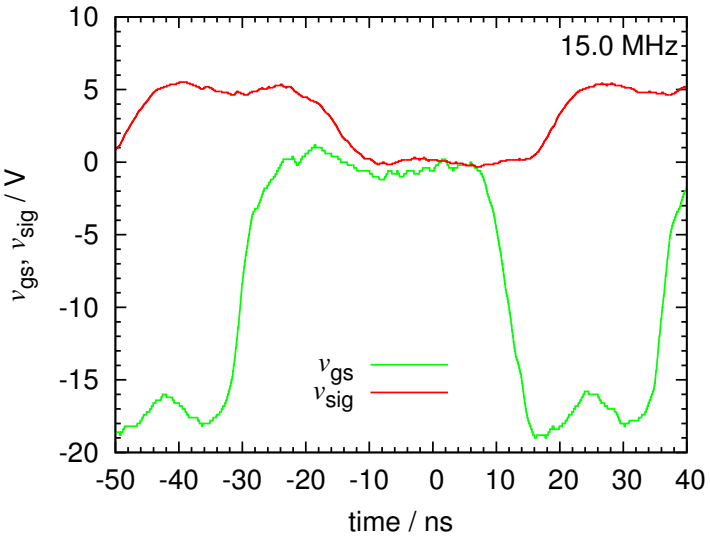


Figure 2.9: Measured waveforms of v_{sig} (red) and v_{gs} (green) at 15 MHz.

2.4 Summary

A high speed gate drive circuit with inherent safety is proposed for normally-on power switching devices to operate in megahertz range. The circuit employs the gate driving IC which utilizes RF on/off keying for the insulated signal transmission instead of optical based insulation method. The arrangement of connection between the circuit and the operated device enables us to control normally-on power devices which have negative gate-to-source threshold voltage with the same control logic as for normally-off devices.

The experiments on operating an unloaded normally-on SiC JFET were carried out. The designed circuit has ability of operation at up to 15 MHz. This circuit pushes forward applications of normally-on SiC JFETs to power conversion circuits more widely. SiC power switching devices allow switching power conversion circuits to operate at high frequency, which will lead to decrease dimensions of power sources and to give new functions to conversion circuits. In the research, though the driver design relied on commercial IC, this kind of insulating technique can be integrated with semiconductor devices on the same substrate [37]. This configuration indicates a direction of designing new gate drive circuits.

Experiments of switching circuit with normally-on SiC JFETs will be carried out by using the driver circuit in following chapters. In Chapter 3, SiC JFETs are operated by

the drive circuit under a hard-switching conditions. In Chapter 4, the circuit operates the JFETs in a class-E switched power amplifier. Moreover in Chapter 5, it is applied in the power packet mixer and router of a dc power packet dispatching system.

Chapter 3

High-Frequency Hard Switching of Normally-on SiC JFETs

In this chapter, switching characteristics of SiC RESURF JFETs are tested in a hard-switching circuit for the application to switches in power and information distribution systems. These systems require high-power and high-frequency active switches in order to deal with power and information all together. It is important for the high-frequency applications to evaluate the behavior of the switch and influences of parasitic elements in the circuit on the operation. For the purpose, switching voltage and current waveforms are observed in time domain, power dissipation is calculated, and the output power is analyzed in frequency domain for the estimation of noise emission. In the experiments the JFETs are driven with the gate drive circuit introduced in Chapter 2.

3.1 Introduction

Power electronics plays a crucial role in industry and our modern lives from power distribution to power conversion circuits in mobile equipment. Small power capacity and compact switching power conversion circuits have been applied more and more widely to power sources in home electrical appliances, information and telecommunications equipment, mobile devices, and so on. For the purpose, power semiconductor switches have a key role in regulation and conversion of electric energy. Recently, power switching devices have been required to operate at high frequency, high voltage, and high temperature for power conversion circuits in harsh environment, such as an engine room of a hybrid electric vehicle and aerospace. Most of switching power sources utilize class-D switching, that is, hard switching condition. High-frequency switching provides passive components

in conversion circuits with reduction of their volume and the circuits with functions. SiC power devices are expected to respond to the needs of high-frequency operation among possible semiconductor power devices.

Switching characteristics of transistors strongly affect circuit operation. Parasitic components of devices and circuits also dominate behaviors of high-frequency circuits. The higher switching frequency goes, the more obvious the effect is. Therefore, it is necessary for high-frequency switching to evaluate the influence of them. The power dissipation tends to increase with the rising of switching frequency. Therefore, this chapter expresses the switching voltage and current characteristics of normally-on SiC RESURF JFETs in not only time domain but also frequency domain and switching losses are also evaluated.

3.2 Configuration for Measurements

Switching characteristics of the normally-on SiC JFET are obtained in the test circuit with the gate drive circuit as shown in Fig. 3.1. The circuit consists of a voltage source V_{in} (TEXIO; PA36-3B), an SiC JFET as the device under test (DUT), and a low-inductive resistor R of $47\,\Omega$. They are all connected in series. While the experiments, V_{in} is set at $36\,\mathrm{V}$. The capacitor C is inserted in parallel with input voltage source in order to stabilize input voltage during switching transition. Fig. 3.2 shows the photograph of the JFET and its schematic with parasitic junction capacitors. The device is developed by Sumitomo Electric Industries, Ltd. and sealed in TO247 package. Ratings of the JFET under test are as follows: drain-to-source voltage $200\,\mathrm{V}$, drain current $5\,\mathrm{A}$, and gate threshold voltage $-12\,\mathrm{V}$. Square wave is supplied as gate control signal by a function generator (KENWOOD; FG-281). The signal is provided to the device via the gate drive circuit introduced in Chapter 2.

Photographs of the circuit are shown in Fig. 3.3. The top view of the circuit is Fig. 3.3(a). The gate driving circuit is detached from the main circuit and modularized on an independent printed circuit board (PCB) so as to isolate noise path and make it easy to replace the driver circuit. The DUT is connected to the test circuit by a socket which is compliant with the package of the device. A heatsink is attached on the JFET in order to conduct the experiments under constant temperature. The voltage stabilizing capacitor C consists of parallel connection of two series connected $820\,\mu\mathrm{F}$. The total capacitance of C is $1680\,\mu\mathrm{F}$. Fig. 3.3(b) depicts the back side of the main PCB. The ground plane

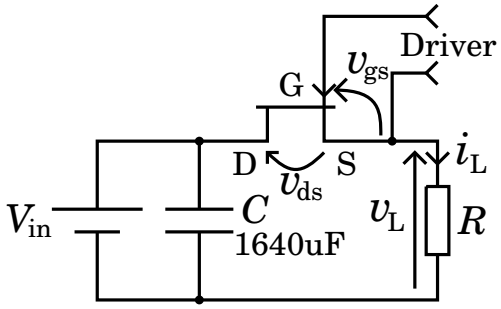
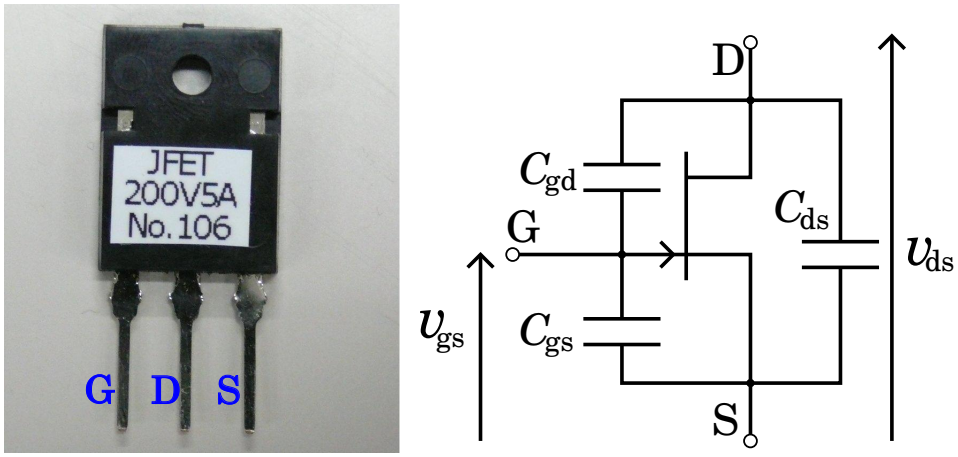


Figure 3.1: Schematic diagram of test circuit for switching characteristics of SiC JFET.



(a) (b)

Figure 3.2: (a) Photograph of SiC RESURF JFET (200 V, 5 A) manufactured by Sumitomo Electric Industries, Ltd., which is molded in TO247 package. (b) Schematic diagram of JFET with its parasitic junction capacitors.

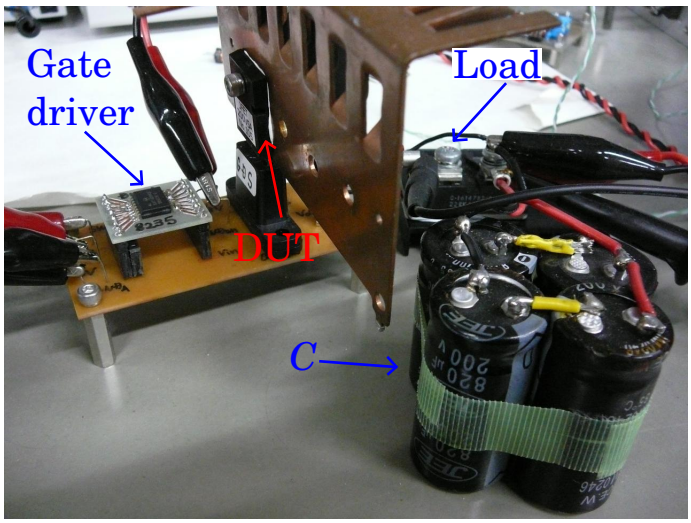
of signal input is divided from that of main circuit for reducing the influence of the noise to the control circuit. Fast switching of large current significantly increases surge voltage affected by parasitic inductors. Thus, cables connecting apparatus and power sources with the circuit are formed similar to twisted pair cable so as to make current loops small (Fig. 3.3(a)). Furthermore, conducting layer width of the PCB is as broad as possible and length is as short as possible in order to reduce inductance (Fig. 3.3(b)).

Under these settings, the gate-to-source voltage v_{gs}, the drain-to-source voltage v_{ds}, the voltage across the load resister v_{L}, and the load current i_{L} are measured by an oscilloscope (Tektronix; TPS2024). Voltage probes for measurements of v_{gs} and v_{ds} is connected via sockets designed for the probes to reduce parasitic inductance in the probes by eliminating ground lead (Fig. 3.4). i_{L} is measured by a current probe (Tektronix; TCP305) with an amplifier (Tektronix; TCPA300).

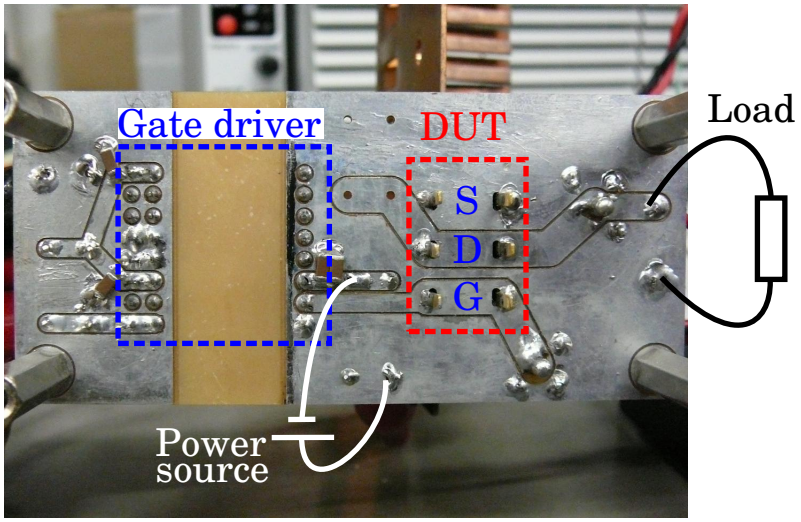
3.3 Switching Characteristics of JFET

Figure 3.5 shows measured waveforms of the gate-to-source voltage v_{gs}, the drain-to-source voltage v_{ds}, the load voltage v_{L}, and the load current i_{L}. The gate drive circuit is operated at 5 MHz in Fig. 3.5(a), 8 MHz in Fig. 3.5(b), and 15 MHz in Fig. 3.5(c). v_{gs} is represented by red line, v_{ds} green, v_{L} blue, and i_{L} purple.

The waveforms, except for the case of 15 MHz, have similar switching characteristics. Immediately after the JFET turns off, v_{ds} reaches to the supplied voltage $V_{\mathrm{in}} = 36$ V. i_{L} also exceeds -0.3 A at the moment. After the v_{ds} reaches to the supplied voltage, it oscillates around 36 V. The amplitude of the oscillation is around 4 V. Its frequency is obtained to reach up to 250 MHz. v_{L} also oscillates at the same frequency. i_{L} seems not to oscillate at 250 MHz. This is because the bandwidth of the current probe and the amplifier is restricted to 50 MHz. Soon after the JFET turns on, v_{ds} falls to about 0 and simultaneously oscillates from -5 V to 5 V. The frequency is up to 250 MHz. In contrast, i_{L} oscillates around 25 MHz during turn-on and turn-off. v_{ds} and v_{L} don't have significant overshoot and undershoot due to the stabilizing capacitor C. Just before turn-on, v_{ds} has overshoot, especially in the case of $f_{\mathrm{sw}} = 5$ MHz and 15 MHz. This overshoot is the induced voltage of line inductance caused by rapidly rising i_{L}. In the case of $f_{\mathrm{sw}} = 8$ MHz, i_{L} is decreasing when the switch turns on. This is why v_{ds} has no significant peak at the instant of turn-on.



(a) Top view of experimental circuit



(b) Bottom view of PCB

Figure 3.3: Photographs of experimental circuit.

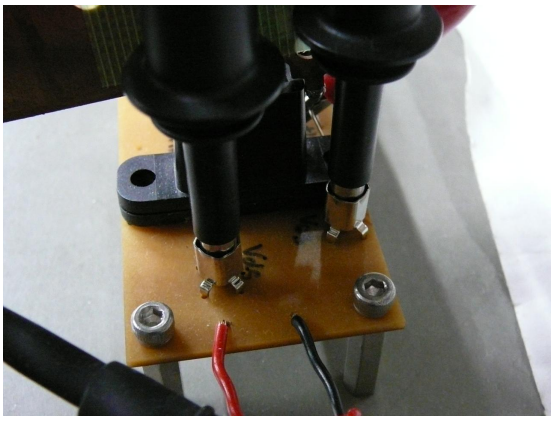


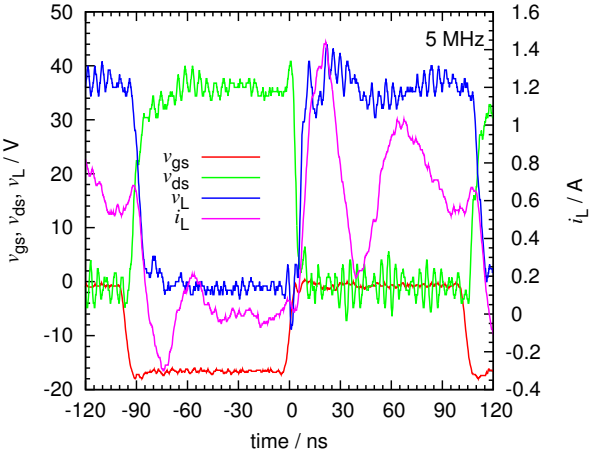
Figure 3.4: Photograph of sockets for probes of oscilloscope. The sockets are used in measurement of v_{gs} and v_{ds}. They reduce line inductance in the probe of the oscilloscope by omitting the grounding wire of the probe.

The current changing rate at switching is very high because of fast switching ability of the JFET. In this instance, the rate reaches up to about $120\,\mathrm{A}/\mu\mathrm{s}$ at turning on and off. Such a high current changing rate may make surge of v_{ds} significantly high while operating it under inductive load.

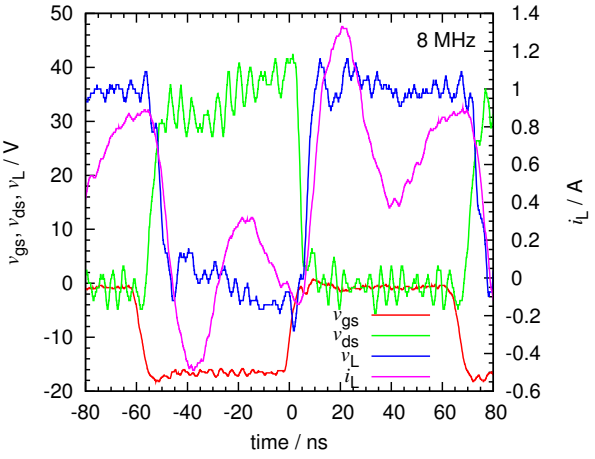
It is impossible to ignore parasitic elements completely while parasitic inductance is desired to be decreased in circuits and devices. Therefore, the oscillations of voltage and current, ringing, are caused by resonance of parasitic inductance with capacitance of p-n junction inside an SiC JFET. So the ringing frequency is represented by f_{r}:

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{L_{\mathrm{p}}C_{\mathrm{p}}}}, \tag{3.3.1}$$

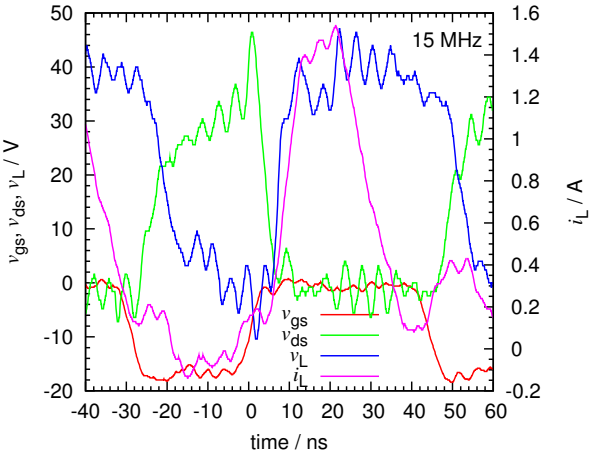
where L_{p} is the total parasitic inductance and C_{p} is the total parasitic capacitance, which consists of wiring and junction capacitance. Here, we assume C_{p} is the output capacitance C_{oss} which is defined by junction capacitance as $C_{\mathrm{oss}} = C_{\mathrm{gd}} + C_{\mathrm{ds}}$. C_{gd} and C_{ds} depend on v_{ds}. These values are determined by static C-V measurements. The C-V characteristics of the DUT have been measured in [59]. The following values are all referred from the dissertation [59]. When the JFET is on, i.e., $v_{\mathrm{ds}} = 0$, $C_{\mathrm{gd}}|_{v_{\mathrm{ds}}=0} = 77\,\mathrm{pF}$ and when the JFET is off, $v_{\mathrm{ds}} = 36\,\mathrm{V}$, $C_{\mathrm{gd}}|_{v_{\mathrm{ds}}=36\,\mathrm{V}} \approx 30\,\mathrm{pF}$. The drain-to-source junction capacitor is also $C_{\mathrm{ds}}|_{v_{\mathrm{ds}}=0} = 148\,\mathrm{pF}$ and $C_{\mathrm{ds}}|_{v_{\mathrm{ds}}=36\,\mathrm{V}} \approx 50\,\mathrm{pF}$. Thus, C_{oss} obtained as $C_{\mathrm{oss}}|_{v_{\mathrm{ds}}=0} \approx 225\,\mathrm{pF}$ and $C_{\mathrm{oss}}|_{v_{\mathrm{ds}}=36\,\mathrm{V}} \approx 80\,\mathrm{pF}$. The total parasitic inductance of the main loop of the testing circuit L_{p} is 586 nH, measured by impedance analyzer (Agilent Technologies;



(a) 5 MHz



(b) 8 MHz



(c) 15 MHz

Figure 3.5: Measured waveforms of voltages and current related to SiC JFET switching at 5 MHz, 8 MHz, and 15 MHz. Red line indicates v_{gs}, green line v_{ds}, blue line v_L, and purple i_L

4294A).

Then, prospective ringing frequency during off state, that is, the resonant frequency of 80 pF and 586 nH, is determined by Eq. (3.3.1) to be 23.24 MHz. The obtained frequency corresponds to measured value. It is clear that the ringing is caused by the resonance of parasitic elements. On the other hand, during on state, the calculated resonant frequency is 13.86 MHz. However, the measured value is around 25 MHz. The cause of the difference has not specified yet.

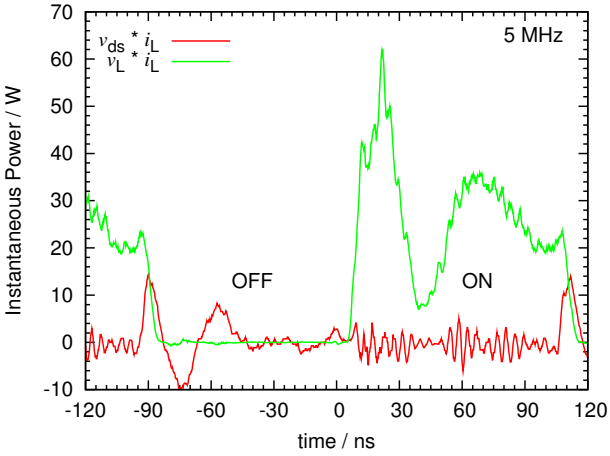
The origin of the high frequency ringing whose frequency is around 250 MHz is not specified. It is possibly induced by the resonance of smaller parasitic inductors and capacitors, such as inductance of bonding wires in the semiconductor device and stray capacitance in the main circuit.

In the case of 15 MHz, waveforms have slight difference from others especially in v_{ds} and i_{L}. v_{ds} does not immediately reach dc input voltage, 36 V, after turn-off. There is little undershoot in i_{L} at turn-off. The amplitude of ringing in i_{L} is also smaller than other results during off-state. These features are similar to the waveforms under resonance-switching conditions, which is discussed in Chapter 4. This is because the switching frequency gets close to the ringing frequency. Thus, the parasitic L-C resonance elements act as band pass filter and make output waveforms nearly sinusoidal.

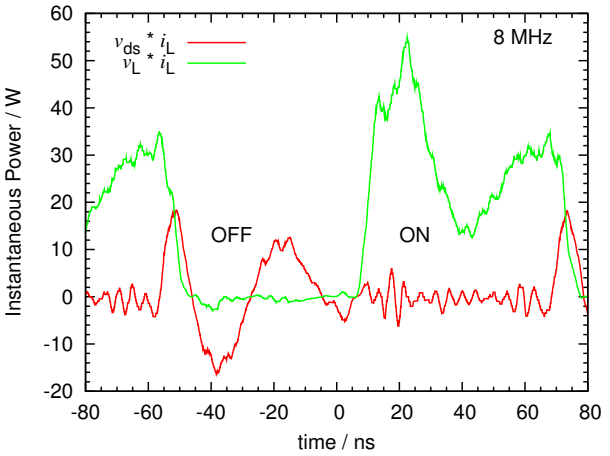
3.4 Power Dissipation and Efficiency

The instantaneous power waveforms of the JFET and the load are shown in Fig. 3.6. The power consumed in the JFET is calculated by multiplying of v_{ds} and i_{L} in Fig. 3.5. The load power also estimated by multiplying of v_{L} and i_{L} in Fig. 3.5. Each figure in Figs. 3.6(a) to (c) is corresponding to each of Figs. 3.5(a) to (c), respectively. For example, Fig. 3.6(a) corresponds to Fig. 3.5(a). Red line indicates the dissipation in the switch, that is, $v_{\mathrm{ds}} \cdot i_{\mathrm{L}}$, and green the load power, $v_{\mathrm{L}} \cdot i_{\mathrm{L}}$. The ringing during turn-off mainly contributes to power dissipation in the transistor. On the other hand, the ringing during turn-on appears in load power. As with the voltage and current waveforms, the case of 15 MHz shows difference from others. The amplitude of the oscillation of power dissipation in the device is much smaller than others in the off-state. This is also because of the small distance of the switching frequency from the resonant frequency of parasitic elements.

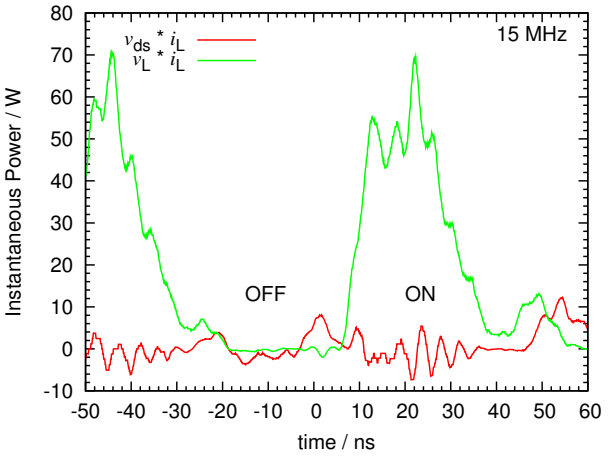
The average consumed power over a cycle is drawn in Fig. 3.7. Red line represents the



(a) 5 MHz (corresponding to Fig. 3.5(a))



(b) 8 MHz (corresponding to Fig. 3.5(b))



(c) 15 MHz (corresponding to Fig. 3.5(c))

Figure 3.6: Instantaneous power waveforms of the JFET and the load under switching frequencies at 5 MHz, 8 MHz, and 15 MHz. Red line indicates power dissipated in the JFET and green line is load consuming power.

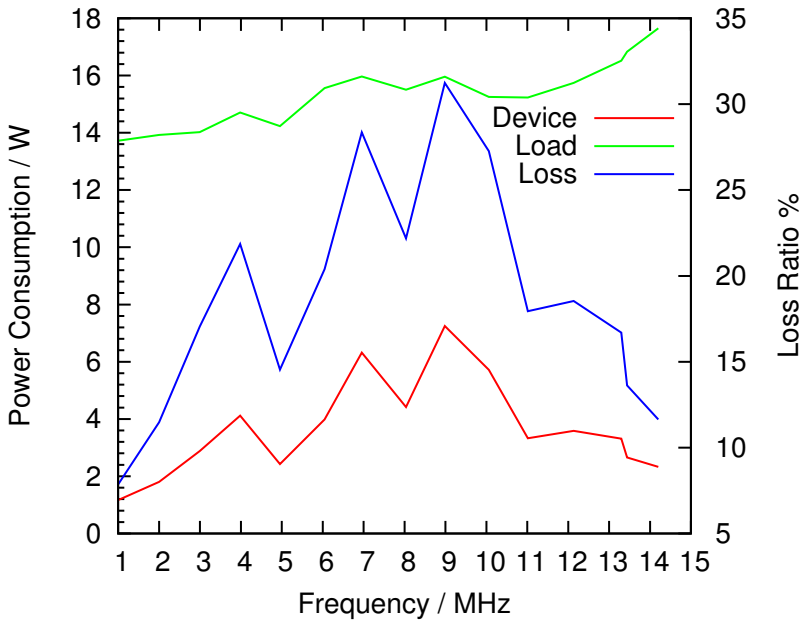


Figure 3.7: Power dissipation and ratio of loss.

power consumption in the switching device p_{dev}, green line the load power p_{L}, and blue the Loss Ratio. These values are calculated by the averaging over a switching cycle of integrated instantaneous power with respect to the cycle. That is, assuming the instantaneous powers, $p_{\mathrm{dev}}(t) = v_{\mathrm{ds}}(t)i_{\mathrm{L}}(t)$, $p_{\mathrm{L}}(t) = v_{\mathrm{L}}(t)i_{\mathrm{L}}(t)$, and T_{sw} is a switching cycle, the average powers are:

$$P_{\mathrm{dev}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} p_{\mathrm{dev}}(t)\,\mathrm{d}t, \tag{3.4.1}$$

$$P_{\mathrm{L}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} p_{\mathrm{L}}(t)\,\mathrm{d}t. \tag{3.4.2}$$

The integral is calculated numerically by using trapezoidal approximation because the measured voltage and current values are discrete depending on the sampling ratio of oscilloscope.

The load power is slightly proportional to the switching frequency. In contrast, the power dissipation in the device is not proportional to the frequency, in addition, it has peaks. The peaks appear every 3 MHz from 4 MHz. The power dissipation in the device goes small with increasing switching frequency more than 10 MHz due to the resonance-like switching.

The Loss Ratio is calculated under the assumption that no power losses except for in

the device and the load as follows:

$$\text{Loss Ratio} = \frac{P_{\text{dev}}}{P_{\text{dev}} + P_{\text{L}}} \times 100. \tag{3.4.3}$$

Hence, the efficiency η is approximately estimated as:

$$\eta = 1 - \text{Loss Ratio}. \tag{3.4.4}$$

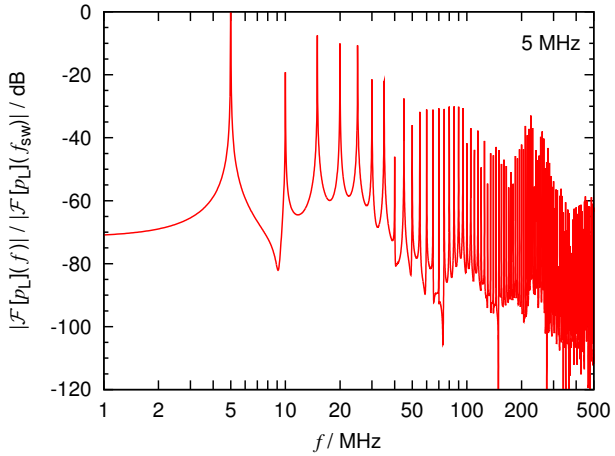
In the experiments, the efficiency achieved 88 % at 14 MHz and at least 69 %. 88 % of efficiency is sufficiently high under the switching frequency and hard-switching conditions due to the resonance-like operation.

3.5 Switching Characteristics in Frequency Domain

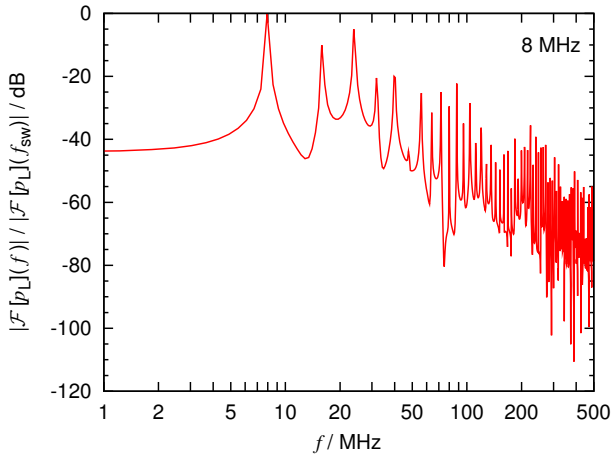
In hard-switching circuits, the load voltage and current shape pulsed waveforms. Moreover, they oscillate much higher than the switching frequency, that is, ringing. Therefore they have a lot of higher harmonics components and energy spreads over wide spectra in frequency domain. Here, the spread of energy is evaluated by calculation of the spectra of the instantaneous load power. The spectra are derived by the Fast Fourier Transformation (FFT). One cycle of instantaneous power waveform is repeated proper times in order to improve frequency resolution for the calculation.

Here, $\mathcal{F}[\cdot]$ represents the operation of Fourier transformation. The spectra is obtained by $|\mathcal{F}[p_{\text{L}}](f)|$. Then the ratio of each frequency component over the component of switching frequency is calculated by $|\mathcal{F}[p_{\text{L}}](f)| \,/\, |\mathcal{F}[p_{\text{L}}](f_{\text{sw}})|$.

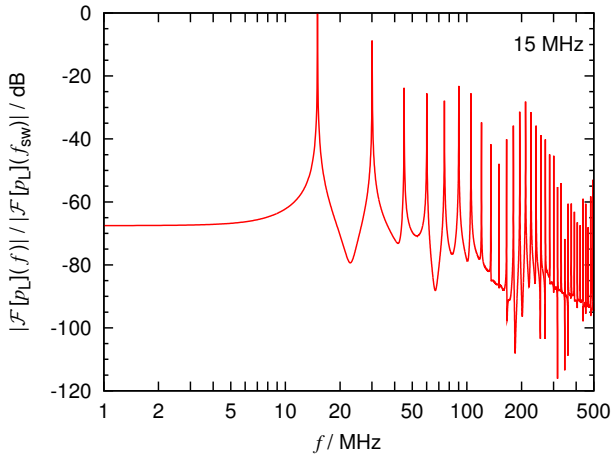
Fig. 3.8 depicts the ratio in the case that switching frequency is 5 MHz, 8 MHz, and 15 MHz. In Fig. 3.8(a), the second to fifth harmonics are relatively large. Especially, the fifth harmonic frequency of 25 MHz corresponds to the ringing frequency. Hence, the strength of the fifth harmonic spectrum is large. The spectra around the higher resonance frequency, that is, 250 MHz, have a peak. The spectra in Fig. 3.8(b) also have similar features to Fig 3.8(a). Fig. 3.8(c) shows that the second harmonics is larger than the third harmonics because of ringing frequency. Due to the ringing, the strength low-order harmonics are more than -20 dB. It means, the strength of radiated and conducted noise can be large enough to interfere in the operations of other circuits and the control circuit of the switching circuit itself.



(a) 5 MHz (corresponding to Fig. 3.6(a))



(b) 8 MHz (corresponding to Fig. 3.6(b))



(c) 15 MHz (corresponding to Fig. 3.6(c))

Figure 3.8: Power spectrum of load power of 5 MHz, 8 MHz, and 15 MHz switching.

3.6 Summary

In this chapter, a normally-on SiC RESURF JFET is driven by the gate drive circuit designed in Chapter 2 at high switching frequency under hard-switching conditions. The switching characteristics of the JFET are evaluated by observing voltage and current waveforms in time domain and frequency domain.

The analysis in time domain shows that the ringing consists of a couple of oscillations of several frequencies and one of them is induced by the resonance of wiring inductance in the circuit and junction capacitors in the semiconductor device. Increase in switching frequency makes it come closer to the ringing frequency. That implies high-frequency hard switching can be changed into soft switching by careful prediction and design of parasitic elements. Power dissipation with respect to switching frequency indicates that ringing significantly contributes to the amount. Soft switching should be considered for high-frequency switching, due to the large power dissipation in the device and strong low-ordered harmonic components in the spectra of load power. Therefore, in Chapter 4, the switching characteristics will be examined under soft switching, that is, resonance-switching, conditions.

Chapter 4

Soft Switching of Normally-on SiC JFETs with Class-E Power Amplifier

In Chapter 3, it showed that high-frequency soft switching possibly reduces noise emission and sinusoidal-like waveforms improve the switching efficiency. Then, in this chapter, the class-E switching circuit is discussed as an example of soft-switching circuit topologies. The class-E switching circuit is low loss even in RF operation and has less harmonic component in switching waveforms than hard-switching circuits. These features may solve the problems which occur in hard-switching circuits. The operation of the class-E switching power amplifier is discussed by numerical simulation and experimental study.

4.1 Introduction

The class-E switching circuit appeared in literature for the first time in 1975 [60]. This type of switching circuit has been applied to RF power amplifiers and power conversion circuits due to its high efficiency in high frequency range [61–64].

Figure 4.1 depicts the class-E power amplifier as an example of basic class-E swintcing circuits. Switching class of "E" is defined by following conditions.

Condition 1. After a power switch is turned off, v_{ds} raises with certain delay time.

Condition 2. At the instance of turning off, the switch v_{ds} equals zero.

Condition 3. At the moment when the switch is turned on, $\dfrac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t}$ is zero.

Condition 1 represents a requirement for zero current switching (ZCS) at turn-off. When the switch is turned off, the current flowing through the switch is zero while high voltage is

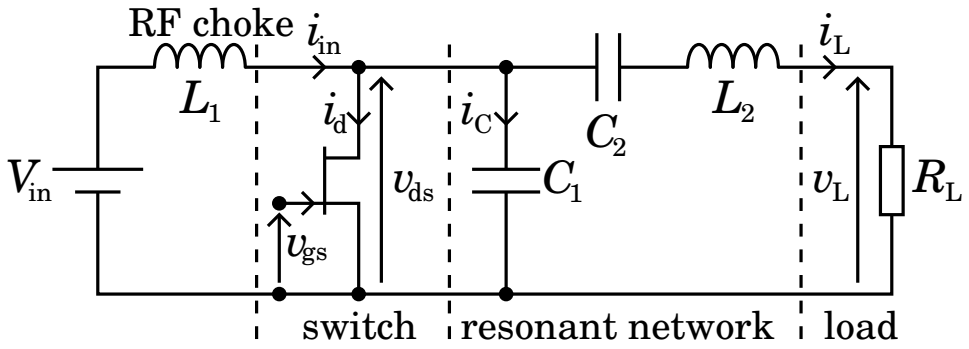


Figure 4.1: Schematic diagram of class-E power amplifier [60].

applied across the switch. That means that energy dissipation is sufficiently small during turn-off. Condition 2 is required to achieve zero voltage switching (ZVS) at turn-on. The voltage across the switch is zero while large current is flowing at turn-on. It implies that turn-on power loss becomes small. Switching power loss is described by means of energy dissipation during charging and discharging gate capacitor of a semiconductor switch. Referring to Condition 3, the current which flows from a parasitic capacitor C_{p} at the moment of turn-on is as follows:

$$i = C_{\mathrm{p}} \frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t} = 0. \tag{4.1.1}$$

Even in the case that the operating point of the switch is slightly different from theoretical value, power loss can be kept low, for the voltage and the current are zero simultaneously at the moment of turn-on. Furthermore, the switch is turned on after the parasitic capacitor is fully discharged, which also contributes to reduction of switching loss.

With regard to noise emission, the class-E switching circuit produces little high-order harmonic components theoretically. The voltage across the load oscillates sinusoidally at the resonance frequency in the class-E circuit. Hence, waveform analysis in frequency domain shows that energy spectra concentrate in the resonance frequency. Noise suppression can be easier than hard-switching circuits because frequency bandwidth of harmonic is limited.

On the other hand, designing and circuit implementation are not so easy. Recalculation of circuit constants is required whenever circuit operating conditions are changed, for the constants depend on the switching frequency, the load, and so on. Fine adjustment of circuit values based on experimental results is essential to comply with these three conditions shown above.

4.2 Physical Principles of Class-E Power Amplifier

This section describes physical principles of the class-E power amplifier. The class-E switching power amplifier operates following three conditions described in Section 4.1. The principles of operation is explained based on the circuit topology shown in Fig. 4.1. This circuit mainly consists of four blocks, that is, a power source, a semiconductor power switch, a resonant network, and a load. The resonant network is composed of a combination of an inductor L_2 and capacitors C_1 and C_2. L_1 performs as RF choke coil. So L_1 is required to have inductance large enough to prevent ac current from flowing. The value of the capacitor connected in parallel with the transistor C_1 includes the output capacitor of the transistor C_{oss} and stray capacitors between lines and ground planes. R_{L} is sum of load resistance, wiring resistance, and equivalent series resistance of C_2 and L_2. Line inductance and equivalent inductance of the load are added to L_2. C_2 includes equivalent series capacitance of the load. The operation of the class-E switching power amplifier in cyclostationary state is shown below under above settings.

The resonant network converts dc input current i_{in} into ac load current i_{L} oscillating at the resonance frequency when the semiconductor switch operates at the resonance frequency of the network. Hence, i_{d} or i_{C} is difference of i_{in} and i_{L}. When the switch is turned off, the resonant network and the load act as damped second-order resonance circuit which is composed of series connection of L_2, R_{L}, and $C_1//C_2$. Here, $C_1//C_2$ means parallel connection of C_1 and C_2. i_{d} begins to decrease before the transistor is switched off. Then, it reaches zero soon after the transistor is turned off. During that period, the energy stored in C_1, C_2, and L_2 over a preceding cycle is delivered to the load R_{L}. i_{C} does not flow until i_{d} falls to zero. As a result, C_1 is not charged and v_{ds} is kept zero. Here, Condition 1 is fulfilled.

When i_{d} reaches zero, i_{C} begins to flow and charge C_1. Then, the voltage across C_1, which equals to v_{ds}, increases depending on the equation:

$$v_{\mathrm{ds}}(t) = \frac{1}{C_1}\int i_{\mathrm{c}}\mathrm{d}t. \tag{4.2.1}$$

The increment of v_{ds} causes the decrement of i_{C} and result in the increment of i_{L}. The situation continues until v_{ds} rises to a peak after that the voltage starts to decrease. Following behavior of v_{ds} is classified into three cases according to the damping.

Case 1: Over damping In the case that the damping is larger than the correct value, the waveform of v_{ds} is as sketched in Fig 4.2(a). v_{ds} falls to the minimal voltage more than zero and starts to rise. Whenever the transistor is turned off, C_1 is not fully discharged and voltage is applied across the switch. C_1 is discharged through the transistor after turn-on. It means that current flows through the transistor while v_{ds} is not zero. As a result, power dissipates in the transistor.

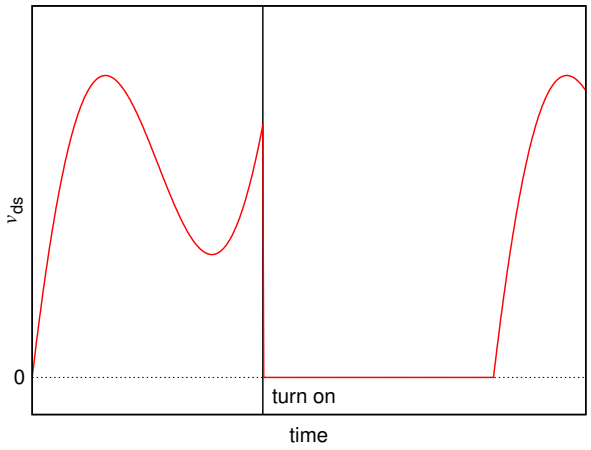
Case 2: Under damping Figure 4.2(b) depicts the waveform of v_{ds} in the under damping condition. v_{ds} decreases to negative value. Then, the body diode of the transistor turns on and current begins to flow through the diode. The current causes power loss and releases energy stored in C_1.

Case 3: Critical damping The correct damping makes the waveform of v_{ds} to be shown in Fig. 4.2(c). v_{ds} falls to the minimal value, which just reaches 0 V under the critical damping condition. This is Condition 2. At the instance, there is no electric charge stored in C_1 and i_{C} equals zero. Consequently, derivative of v_{ds} is zero when it reaches minimal value. If switching frequency is appropriate, the switch turns on at the moment. Finally, Condition 3 is satisfied.

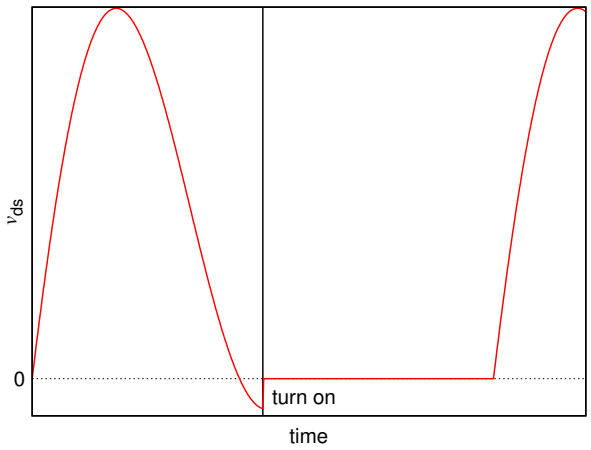
After the transistor is turned on, the dc voltage source V_{in} is short-circuited and i_{d} begins to flow. In this situation, the resonant circuit and the load behave as a series resonant circuit which consists of C_2, L_2, and R_{L}. The waveform of i_{L} is shaped approximately sinusoidal wave depending on response of the resonance circuit. i_{d} also changes sinusoidally. C_2 and L_2 store energy during this period. Then the transistor is switched off at the instance that i_{d} reaches zero if circuit constants are set at proper values. Consequently, sinusoidal current is supplied to the load by repeating this step.

4.3 Designing of Class-E Switching Circuit

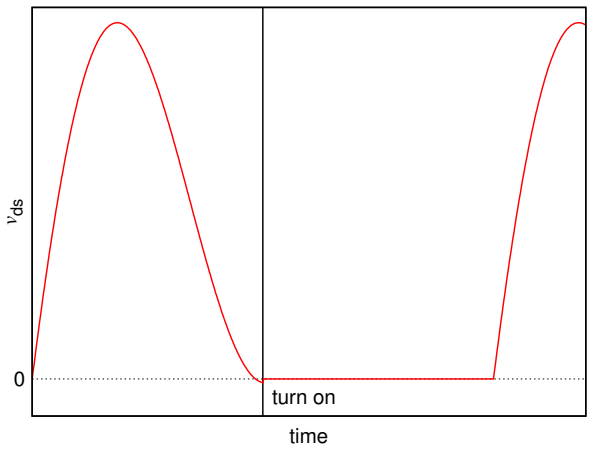
The circuit values are required to be set properly for operating the class-E switching circuit appropriately as mentioned in Section 4.1, according to the load, the switching frequency f_{sw}, and so on. The circuit operation have been analyzed and the derivation of circuit constants have been studied by a lot of methods [60, 61, 65–72]. These papers are roughly classified into two main groups: assuming L_1 has infinite inductance [60,61,65–70]



(a) Case 1: Over damping



(b) Case 2: Under damping



(c) Case 3: Critical damping

Figure 4.2: Sketches of waveforms of v_{ds} in class-E power amplifier under over, under, and critical damping conditions.

and L_1 is finite [71–76]. The early studies in the former group suppose ideal operation of the class-E switching [60, 65, 66]. Some of the researches in latter group consider realistic conditions supported by waveform analyses and/or experimental results [72, 73]. The derivation of design equations based on these two assumptions are shown below.

4.3.1 Ideal Operation Analysis

Here, the analytical design equations are shown, referring to the literature [60, 61, 65]. Following four assumptions are employed for simplicity in analyses, considering ideal operation of the circuit.

Assumption 1. The RF choke L_1 has infinite inductance without any equivalent series resistance and supplies only dc current.

Assumption 2. The loaded quality factor of the series resonant circuit (L_2 and C_2) Q_{L} is high enough in order for output current i_{L} to be sinusoidal at the switching frequency f_{sw}.

Assumption 3. The semiconductor switch operates as ideal switch, that is, lossless, zero on-state resistance, and infinite off-state resistance.

Assumption 4. The switching action of the transistor is instantaneous.

The voltage across the switch v_{ds} can be represented by the function of the current flowing into and from C_1, i_{C}, as mentioned in Section 4.2. In the case that L_1 is enough large and supplies only dc current (Assumption 1), i_{C} is denoted by the function of $v_{\mathrm{L}}(= R_{\mathrm{L}} i_{\mathrm{L}})$ because i_{C} depends on i_{L}. If the inverse functions of i_{C} and v_{L} are derived, they can be determined by the waveform of v_{ds}. To begin with, Fourier analysis is applied to v_{ds} because the dc component of v_{ds} depends on the input voltage V_{in} and fundamental frequency component related to the load current i_{L}. From the analysis, C_1 is represented by:

$$C_1 = \frac{1}{\omega_{\mathrm{sw}} R_{\mathrm{L}} \left(\dfrac{\pi^2}{4} + 1 \right) \dfrac{\pi}{2}} \approx \frac{0.184}{\omega_{\mathrm{sw}} R_{\mathrm{L}}}, \tag{4.3.1}$$

where $\omega_{\mathrm{sw}}(= 2\pi f_{\mathrm{sw}})$ is the switching angular frequency.

The relationship of the input voltage V_{in} to the output power P is determined as follows, considering no dc voltage drop exists across the RF choke.

$$P = \frac{V_{\mathrm{in}}^2}{R_{\mathrm{L}}} \left(\frac{2}{\frac{\pi^2}{4} + 1} \right) \approx 0.577 \frac{V_{\mathrm{in}}^2}{R_{\mathrm{L}}}. \tag{4.3.2}$$

Then, the load and desired power determine the input voltage according to the equation:

$$V_{\mathrm{in}} = \sqrt{\frac{PR_{\mathrm{L}}}{\frac{2}{\pi^2/4 + 1}}} \approx 1.32\sqrt{PR_{\mathrm{L}}}. \tag{4.3.3}$$

The quality factor of the series resonant circuit Q_{L} is defined as:

$$Q_{\mathrm{L}} = \frac{\omega_{\mathrm{sw}} L_2}{R_{\mathrm{L}}}. \tag{4.3.4}$$

Hence, L_2 is described by the function of R_{L} and ω_{sw}:

$$L_2 = \frac{Q_{\mathrm{L}} R_{\mathrm{L}}}{\omega_{\mathrm{sw}}}. \tag{4.3.5}$$

C_2 is extracted by waveform analyses:

$$C_2 = \frac{1}{\omega_{\mathrm{sw}}^2 L_2} \left(1 + \frac{1.42}{Q_{\mathrm{L}} - 2.08} \right). \tag{4.3.6}$$

These equations enable to determine the circuit constants.

4.3.2 Finite Inductance Analysis Based on Experimental Results

In the previous section, design equations are derived for the circuit consists of ideal elements. However, the RF choke has finite inductance in practice. Furthermore, it is unavoidable for the choice of Q_{L} to involve a trade-off between low harmonic component of output voltage and current (high Q_{L}) and high efficiency (low Q_{L}). The usual range of Q_{L} is from 1.8 to 10 [63, 64, 66, 72]. To consider effects of these two realistic conditions, Assumption 1 and Assumption 2 are omitted from the four assumptions in Section 4.3.1. Under this situation, design equations are modified by using experimental results [64, 72].

To begin with, the inductance of L_1 is determined by the cutoff frequency of the low pass filter which is composed by L_1 and C_1.

If the power delivered to the load through the resonant circuit returns to the input voltage source, the efficiency would decrease. Therefore, L_1 should be large enough to make cutoff frequency of the filter f_c sufficiently smaller than switching frequency f_sw. The cutoff frequency of the low pass filter is defined as:

$$f_\mathrm{c} = \frac{1}{2\pi\sqrt{L_1 C_1}}. \tag{4.3.7}$$

Then, L_1 is obtained:

$$L_1 = \frac{k}{\omega_\mathrm{sw}^2 C_1}, \tag{4.3.8}$$

where $\sqrt{k}$ is the ratio of the cutoff frequency to the switching frequency, defined as $\sqrt{k} = f_\mathrm{sw}/f_\mathrm{c}$. The choice of the cutoff frequency determines the gain of low pass filter at the switching frequency according to this equation. k is set arbitrarily to make the gain proper value. In the paper [61] $k \approx 10$ is employed.

Next, the effects of finite Q_L on circuit values are considered. Eq. (4.3.5) does not change, for L_2 is not affected by finite Q_L. The output power P is affected and Eq. (4.3.2) is modified. Refined equation of P is given by the third-order polynomial in Q_L which is extracted by a least-squares fitting to the experimental results.

$$P = 0.5768\frac{V_\mathrm{in}^2}{R_\mathrm{L}}\left(1.001 - \frac{0.4144}{Q_\mathrm{L}} - \frac{0.5776}{Q_\mathrm{L}^2} + \frac{0.2060}{Q_\mathrm{L}^3}\right) \tag{4.3.9}$$

The values of C_1 and C_2 are influenced by both finite Q_L and finite L_1. They are obtained by a polynomial function of Q_L and L_1 based on experimental results as:

$$C_1 = \frac{1}{\left(\frac{\pi^2}{4}+1\right)\frac{\pi}{2}\omega_\mathrm{sw}R_\mathrm{L}}\left(0.999 + \frac{0.914}{Q_\mathrm{L}} - \frac{1.03}{Q_\mathrm{L}^2}\right) + \frac{0.6}{\omega_\mathrm{sw}^2 L_1}, \tag{4.3.10}$$

$$C_2 = \frac{1}{\omega_\mathrm{sw}R_\mathrm{L}}\left(\frac{1}{Q_\mathrm{L} - 0.105}\right)\left(1.00 + \frac{1.01}{Q_\mathrm{L} - 1.79}\right) + \frac{0.2}{\omega_\mathrm{sw}^2 L_1}. \tag{4.3.11}$$

Constant values in Eqs. (4.3.9), (4.3.10), and (4.3.11) are extracted from experimental waveforms.

4.4 Experiments

In this section, the measurements of switching characteristics are carried out under two kinds of circuit parameters. The parameters are designed according to Section 4.3.2. The waveforms in time domain, power dissipation, and spectra of load power in frequency domain are discussed.

Table 4.1: Designed circuit parameters in experiments.

Frequency	2 MHz	13.56 MHz
V_{in}	6.0 V	6.0 V
R_{L}	3.3 Ω	10 Ω
L_1	100 μH	10 μH
Q_{L}	10	5
L_2	2.626 μH	587 nH
C_1	4.819 nF	254 pF
C_2	2.754 nF	313 pF

4.4.1 Experimental Settings

Experiments were carried out under the conditions that switching frequencies are 2 MHz and 13.56 MHz. The latter frequency is especially defined by the Japanese government as one of the bands for industrial, scientific and medical (ISM) applications [77]. According to the definition, radio-communication services operating within these bands must accept harmful interference that may be caused by these applications [77]. The frequency band usually applied for induction heating [72].

For measurements, the circuit parameters are designed as follows, according to Section 4.3.2. To begin with, switching frequency f_{sw} is set at 2 MHz, V_{in} is 6.0 V, and load resistance R_{L} is 3.3 Ω. Then C_1 is obtained by Eq. (4.3.10). The setting of Q_{L} to be 10 gives L_2 with Eq. (4.3.5). To set the value of choke coil, k is set to 10. Then L_1 can be calculated by Eq. (4.3.8). Finally C_2 is derived with these values by Eq. (4.3.11). In the same way, the circuit parameters are set for switching frequency of 13.56 MHz. Note that in 13.56 MHz, Q_{L} is set at 5 because too much Q_{L} brings too small values of C_1 and C_2 which can not implement in the circuit. Consequently, the designed values are shown in Table 4.1.

According to the calculated value, L_1, C_1, C_2, and R_{L} are selected from commercialized products. Only L_2 is winded by hand. The SiC JFET tested in Chapter 3 is adopted to the switch. Then, all the true values of selected components measured by the impedance analyzer. The parasitic elements which affect the circuit operation such as wiring resistances and inductance, equivalent series resistance (ESR) of capacitors and inductors, inductance of the load, junction capacitors of the semiconductor switch are also evaluated. Here, the junction capacitor of the semiconductor switch is the drain-to-source

Table 4.2: Parasitic components of the class-E experimental circuit.

Frequency	2 MHz	13.56 MHz
ESR of L_1	10 Ω	3.3 Ω
stray capacitance of the circuit	14 pF	14 pF
$C_{\mathrm{ds}}\vert_{v_{\mathrm{ds}}=6\,\mathrm{V}}$	95 pF	95 pF
wiring resistance	0.47 Ω	0.47 Ω
wiring inductance	151 nH	151 nH

Table 4.3: Designed and readjusted circuit parameters. Designed values are the same as in Table 4.1.

Frequency	2 MHz		13.56 MHz	
	design	readjust.	design	readjust.
V_{in}	6.0 V	6.0 V	6.0 V	6.0 V
R_{L}	3.3 Ω	3.3 Ω	10 Ω	10 Ω
L_1	100 μH	102 μH	10 μH	10 μH
Q_{L}	10	9.9	5	4.26
L_2	2.626 μH	2.55 μH	587 nH	500 nH
C_1	4.819 nF	3.7 nF	254 pF	250 pF
C_2	2.754 nF	3.3 nF	313 pF	398 pF

capacitance C_{ds} of off-state [64]. The value of C_{ds} is referred to [59]. The parasitic values are listed in Table 4.2. The wiring resistance and ESR equivalently add to R_{L}, wiring inductance and inductive component of the load increases L_2, and junction capacitors add to C_1. Hence, estimations of them and tuning of the circuit parameters are required at the design phase in advance. The circuit parameters are readjusted by experiments referring to the measured true values and parasitic components. The readjusted values are shown in Table 4.3 with the designed values (shown again).

4.4.2 Experimental Results

Voltage and Current Waveforms in Time Domain

Figure 4.3 shows measured waveforms of the class-E power amplifier. Aqua line is the input current i_{in}, red line the voltage across the transistor v_{ds}, purple line the load current i_{L}, green the load voltage v_{L}, and blue the gate-to-source voltage of the switch v_{gs}. Fig. 4.3(a) is the result of 2 MHz switching. Though ringing occurs after turn-off of the transistor, the waveforms roughly trace class-E switching waveforms. i_{in} is constant

dc current due to the sufficient value of the choke coil L_1. The load current i_{L} shapes almost sinusoidal. v_{ds} draws 0 during on-state and a positive phase of sinusoidal wave during off-state. Soon after the switch turns on, v_{ds} goes under 0 V, which is also one of differences from the class-E switching.

On the other hand, in the case of 13.56 MHz in Fig. 4.3(b), the waveforms are strongly affected by the ringing. Especially, v_{gs} and v_{ds} oscillate in large amplitudes. This may be also caused by the resonance of parasitic elements.

Power Dissipation

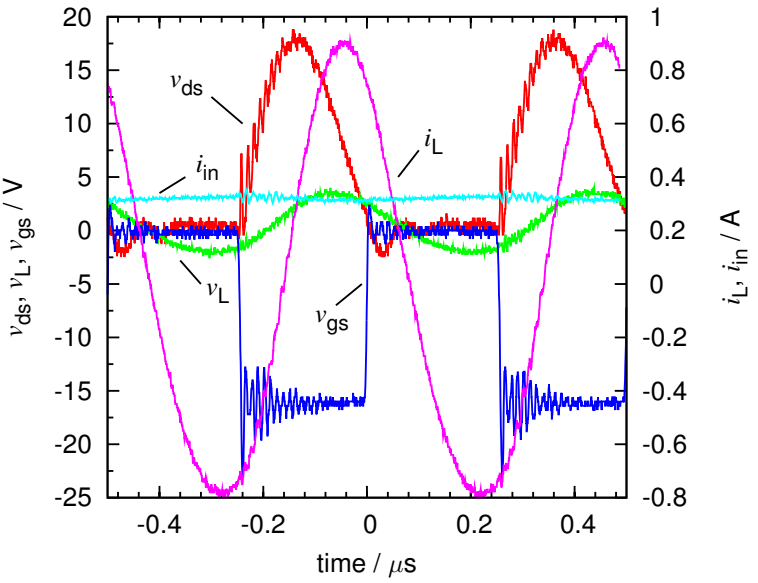
Power consumption of the circuit is also estimated. Fig. 4.4 represents instantaneous input and load power. Red line is the input power p_{in} and green the load power p_{L}. Here, the result of 2 MHz is only shown because the result of 13.56 MHz is far from the class-E operation. The efficiency of the circuit is estimated by a similar way in Section 3.4. The efficiency obtained is 60.3 %. This is much lower than a theoretically expected value. This low efficiency is brought by the ringing and power dissipation at large ESR of L_1. The dissipation can be roughly evaluated by a simplified calculation using the values of i_{in}, 0.3 A and the ESR of L_1, 10 Ω. The dissipation of the 10 Ω of resister by the 0.3 A of current is around 0.9 W. The input power is around 2 W. Therefore, around half of the input power consumed by the ESR of L_1.

Output Power in Frequency Domain

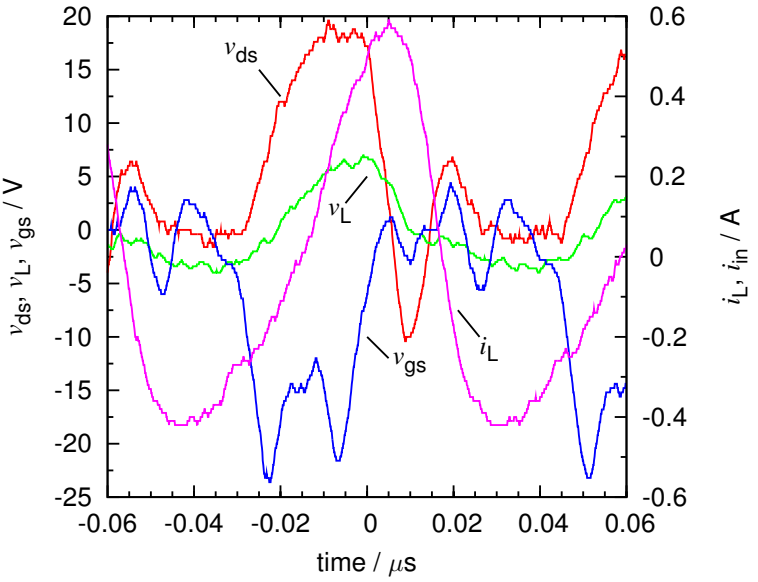
Finally, the waveforms analyzed in frequency domain. The spectrum of the load power is obtained by the similar way in Section 3.5 and shown in Fig. 4.5. Compared to Fig. 3.8, high-ordered components more than the 3rd order is smaller by up to 20 dB. It suggests that soft-switching circuits can suppress high order harmonics noise emission.

4.5 Numerical Simulation of Class-E Power Amplifier

Designing the class-E power amplifier and determining its circuit parameters take a time due to existence of parasitic components in the circuit. The parasitic components have an influence on the operation of the circuit. The influence of some components can be evaluated to increase proper circuit values as explained in Section 4.4.1. On the other



(a) 2 MHz



(b) 13.56 MHz

Figure 4.3: Measured waveforms of voltage and current of class-E power amplifier. Aqua line is input current i_{in}, red line voltage across the transistor v_{ds}, purple line load current i_{L}, green load voltage v_{L}, and blue gate-to-source voltage of the switch v_{ds}.

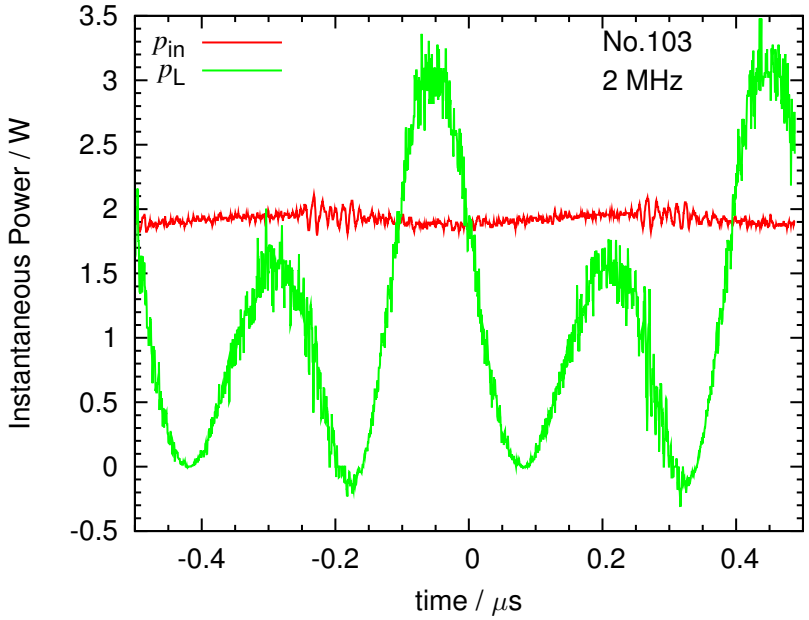


Figure 4.4: Instantaneous power waveforms of input and load. Red line is input power p_{in} and green is load power p_{L}.

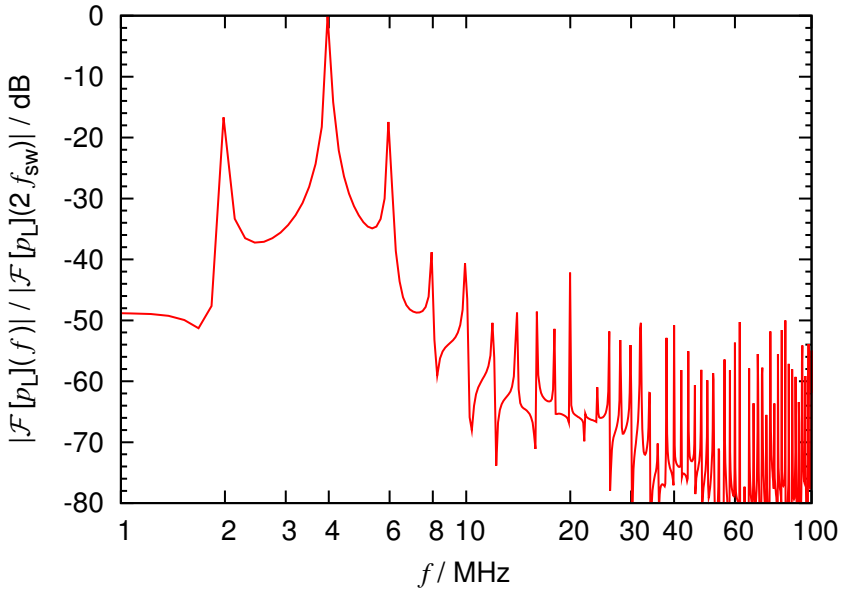
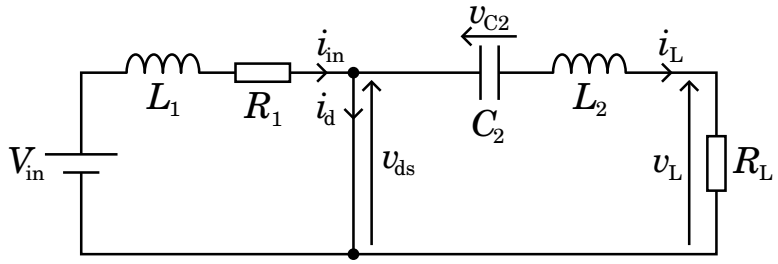
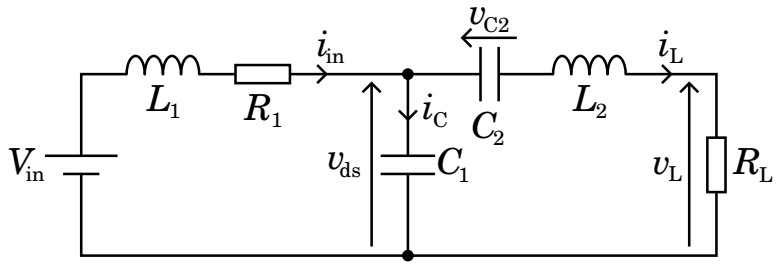


Figure 4.5: Power spectrum of load power at switching frequency of 2 MHz.



(a) On-state



(b) Off-state

Figure 4.6: Schematic diagram of class-E power amplifier in on-state and off-state.

hand, the parasitic components of L_1 and C_1 do not simply affect a specific component, for the change of circuit topologies induced by switching. Hence, it is unavoidable to readjust circuit parameters with experiments. It requires the cut-and-try method in designing stage. The method takes to long time and is inefficient. Therefore, numerical simulation is important for designing circuit values. For the simulation, R_1 is introduced to take account of the influence of the equivalent series resistance of choke coil.

4.5.1 Circuit Model

For numerical analyses, the circuit in Fig. 4.1 is divided into two topologies: on-state and off-state, according to the state of the switch. Schematic diagram of on-state is shown in Fig. 4.6(a) and that of off-state is Fig. 4.6(b). Here, it is assumed that the transistor has zero on-state resistance and infinite off-state resistance. Circuit equations of each topology are denoted by using state variables, $i_{\rm in}$, $i_{\rm L}$, $v_{\rm ds}$, and $v_{\rm C2}$ as follows.

On-state

In the on-state, there are two minor current loops in the circuit. One is the loop including input voltage source. Kirchhoff's voltage low describes the equation of the

circuit as:

$$\frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} = -\frac{R_1}{L_1} i_{\mathrm{in}} + \frac{V_{\mathrm{in}}}{L_1}. \tag{4.5.1}$$

The other consists of the resonant network without C_1 and the load. The loop is represented by following equations:

$$\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = -\frac{R_{\mathrm{L}}}{L_2} i_{\mathrm{L}} - \frac{v_{\mathrm{C2}}}{L_2}, \tag{4.5.2}$$

$$\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = \frac{i_{\mathrm{L}}}{C_2}, \tag{4.5.3}$$

$$v_{\mathrm{ds}} = 0. \tag{4.5.4}$$

Off-state

In the off-state, the equations are:

$$\frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} = -\frac{R_1}{L_1} i_{\mathrm{in}} - \frac{v_{\mathrm{ds}}}{L_1} + \frac{V_{\mathrm{in}}}{L_1}, \tag{4.5.5}$$

$$\frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t} = \frac{i_{\mathrm{in}} - i_{\mathrm{L}}}{C_1}, \tag{4.5.6}$$

$$\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = -\frac{R_{\mathrm{L}}}{L_2} i_{\mathrm{L}} + \frac{v_{\mathrm{ds}} - v_{\mathrm{C2}}}{L_2}, \tag{4.5.7}$$

$$\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = \frac{i_{\mathrm{L}}}{C_2}. \tag{4.5.8}$$

Equation (4.5.4) can be omitted because the assumption of the transistor as the ideal switch automatically satisfies the equation. Then, the equations above except for Eq. (4.5.4) are combined into following four equations by using the switching function s which defined as:

$$s = \begin{cases} 0 & \text{switch is } \textbf{on state} \\ 1 & \text{switch is } \textbf{off state}. \end{cases} \tag{4.5.9}$$

Consequently, the circuit equations of the class-E power amplifier are:

$$\frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} = -\frac{R_1}{L_1} i_{\mathrm{in}} - s\frac{v_{\mathrm{ds}}}{L_1} + \frac{V_{\mathrm{in}}}{L_1}, \tag{4.5.10}$$

$$\frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t} = s\frac{i_{\mathrm{in}} - i_{\mathrm{L}}}{C_1}, \tag{4.5.11}$$

$$\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = -\frac{R_{\mathrm{L}}}{L_2} i_{\mathrm{L}} + s\frac{v_{\mathrm{ds}}}{L_2} - \frac{v_{\mathrm{C2}}}{L_2}, \tag{4.5.12}$$

$$\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = \frac{i_{\mathrm{L}}}{C_2}. \tag{4.5.13}$$

Table 4.4: Circuit parameters used in simulations. These values are the same in experiments (Table 4.3).

Frequency	2 MHz	13.56 MHz
L_1	102 μH	10 μH
R_1	10 Ω	3.3 Ω
Q_{L}	9.9	4.26
L_2	2.55 μH	500 nH
C_1	3.7 nF	250 pF
C_2	3.3 nF	398 pF
R_{L}	3.3 Ω	10 Ω

These equations are numerically integrated by means of fourth-order Runge-Kutta to analyze the behaviors of the voltage and current in the circuit. The step size of iteration is set small enough for the calculation to converge. The analysis covers only periodic steady state.

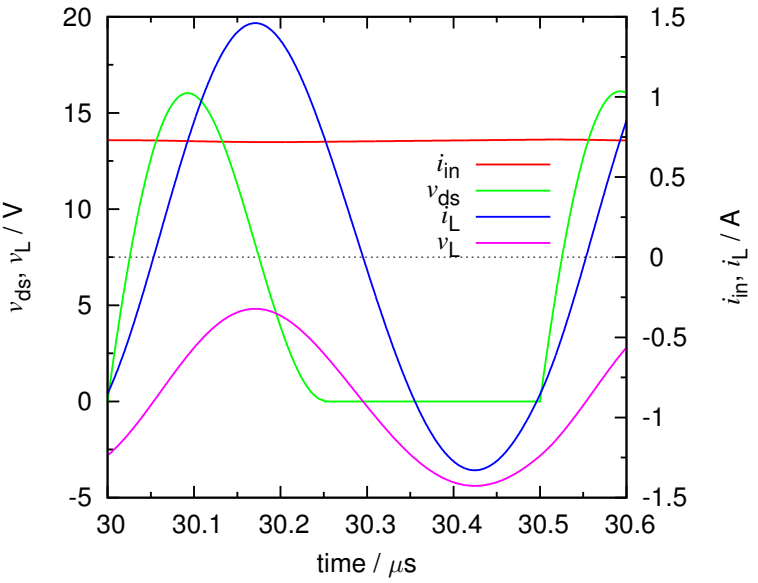
4.5.2 Settings for Simulation

The circuit parameters are set the same way as in Section 4.4.1. For considering ESR of L_1, the value of R_1 uses the ESR of L_1 in Table 4.2. The values used in the simulations are listed in Table 4.4. Under the setting, the behaviors of the voltage and current are calculated.

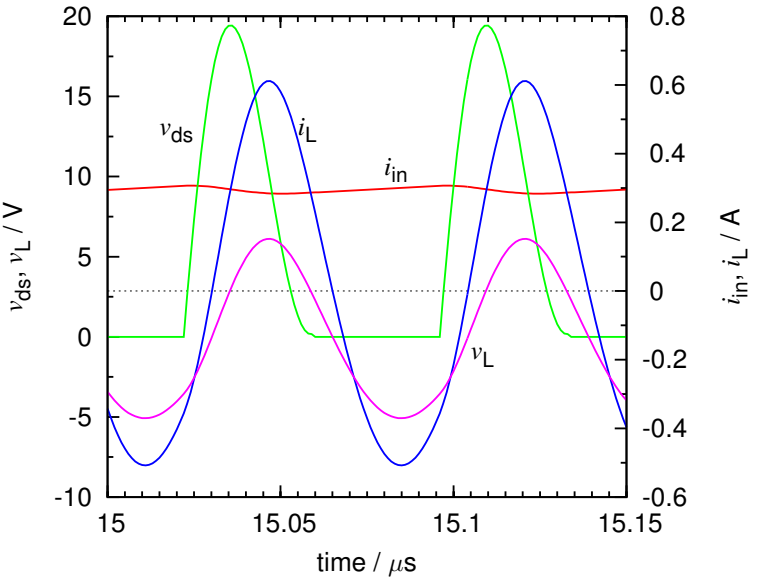
4.5.3 Numerical Results

Figure 4.7 depicts simulated waveforms of class-E power amplifier. Red line is the input current i_{in}, green line the voltage across the transistor v_{ds}, blue the load current i_{L}, and purple the load voltage v_{L}. In the case of 2 MHz, compared with Fig. 4.3(a), v_{ds} and v_{L} take similar values. Simulated i_{in} and i_{L} are larger than measured values. It may be caused by parasitic resistance which does not considered in the simulations. However, the phase relationships between each waveform are well simulated.

In the case of 13.56 MHz, compared to Fig. 4.3(b), the amplitude of each waveform conforms to the measured one although the ringing is not simulated. In the simulation, the parasitic and circuit components are summed up. Therefore, the method can not consider the resonance among parasitic components. It is important for accurate simulation to deal with dispersed parasitic elements.



(a) 2 MHz



(b) 13.56 MHz

Figure 4.7: Simulated waveforms of voltages and currents of class-E power amplifier. Red line is input current i_{in}, green line voltage across the transistor v_{ds}, blue line load current i_{L}, and purple load voltage v_{L}.

4.6 Summary

In this chapter, the class-E power amplifier is studied as one of the soft-switching circuits in order to improve the efficiency of high-frequency switching circuits and depress noise emission. Numerical simulations and experiments are carried out under switching frequency of 2 MHz and 13.56 MHz. In case of lower frequency, the circuit operates almost class-E condition. However, the upper frequency, the circuit operates out of the condition due to the existence of ringing. The large ESR of the choke coil decreases the efficiency of the circuit. The spectrum of load power shows the possibility of suppression of high-order harmonics emission. From these results, the class-E circuit has the potential to operate in high switching frequency.

Simulated voltage waveforms coincide with the experimental results. Regarding current waveforms, there still exist differences in the amplitude. Improving accuracy of simulated current waveforms will help us to design class-E switching circuits without cut-and-try readjustments of circuit parameters.

Chapter 5

Electric Power Dispatching in Home Based on Information of Power

In this chapter, the idea of power feeding based on the quality of power is proposed to manage electric power flows in home utilizing distributed power sources. Section 5.2 introduces the idea. Two kinds of electric power distribution systems which differ in the circuit topology are designed to realize the concept as applications of high-frequency hard switching explained in Chapter 3. These systems allow electric power differing in voltage and frequency to flow in a single power distribution network in home. For simplicity the systems are classified into ac based and dc based systems. Section 5.3 explains ac circuit switching system as one of the systems. The other one, dc power packet dispatching system is described in Section 5.4. Their designs are discussed in detail. Finally, experiments on power flow control exhibit the validity of the systems.

5.1 Introduction

The demand for electrical energy has recently increased due to the spread of home electrical appliances. Also, new types of demands for electricity appear with growing use of plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs). However, environmental issues necessarily restrict energy consumption. As a result, alternative energy sources need to be considered, and the utilization of natural and renewable energy sources have been promoted. Secondary batteries are also employed to temporarily accumulate the generated power for power and load leveling. These trends are dispersing small power sources into the consuming area.

On the other hand, electric power utility companies have operated huge-capacity power

plants and regulated supplying power to be compliant with load requirements for keeping the frequency and the voltage of distribution grid stable in power systems. In the system, fluctuations in the voltage and the frequency are well suppressed by the control of power flows. The conditions surrounding power distribution grids, however, can not be the same as before. This is because the outputs of linked natural and renewable sources are strongly affected, for instance, by the weather conditions, which cause fluctuations in quantity, frequency, and voltage. Therefore, the more natural and renewable energy sources are connected to a power grid, the less the qualities of frequency and voltage in power flows arises in grids. These renewable energy sources are similarly introduced in households. Spreading renewable and distributed sources among homes implies that houses and buildings are no longer pure loads, but also power sources producing power flows in the opposite direction toward the main grid. It is unavoidable to regulate the power generated by renewable sources and consumed by home appliances in order for a home to continue being a suitable consumer from the viewpoint of the distribution system. As a result, in-home electricity distribution systems are required to reduce total power consumption and, at the same time, to properly balance the production and the consumption of individual households.

Home energy management systems (HEMS) take on an important role in this situation. HEMS [8, 9] and management of smart grids [10] are hot topics. Handling power flows requires measurements and predictions of the power generated and demanded. Most of the ideas of power management mainly base on the observation of the quantity of electric power. Moreover, the quantities are observed at given points such as outlets of generators, junctions of transmission lines, and input terminals of loads. These measurements do not guarantee the amount of power flows on transmission lines between the observing points, except for the points. This chapter focuses on not only the quantity but also the quality of energy. Here, the quality in electric power implies maximum available supplying power, frequency variation, and voltage fluctuation. In addition, constant identification of the amount of power is considered.

Power packet distribution is suggested as one of the solutions to the problem, which is based on the method of packet transmission via information and telecommunications networks. The concept of packetization has been proposed in [12,13] for trading of electric power in high-voltage power transmission networks. The key of the idea is “packetization” and “tagging”. The former means dividing a power flow in arbitrary amount. The latter

represents the attachment of the tag which records a destination and the amount of power to a power packet. He *et al.* proposed the Intelligent Power Switch (IPS), which has both capabilities of an Internet router and a power converter with protection equipment [17]. The IPS is also experimentally studied for simulating Smart Grid by small power electrical circuit [18]. In the study, solid state relays are employed for power switches in the IPS and information is transmitted by means of radio communication, separately. These researches are mostly theoretical or numerical simulation based studies. In the experimental studies, special communication paths are employed other than power line. Indeed it has been difficult to realize practical hardware up to now because packetization requires high switching frequency enough to generate pulse and high power switching capabilities, but there have been hitherto no switching devices capable of both functions.

Recent progress of development of wide bandgap semiconductor devices probably realizes high-frequency and high-power switches. Chapter 3 showed that SiC JFETs have capabilities enough to produce power packet. It indicates possibilities of developing hardware which realizes the concept for the power packet. As a result, we are able to integrate the physical paths of power transmission and communication. Then, the power packet redefined as the series of pulses which include power and information about itself, for example, the amount of the power, the source, and the destination of the packet. It means that power packet includes the tag.

This chapter presents the idea of in-home power management with referring to the source of the electricity, the quality of the power, and demands. Then, two kinds of prototypes of hardware which achieve in-home power routing are designed and examined their capability of operation. In the former type, conventional techniques are employed, *i.e.*, a circuit switching system based on ac power distribution. The system is designed in order to confirm the proposing principle for adding information to electric power and distributing power according to the information. The latter system utilizes power packet dispatching to the full, which is based on dc power feeding. Power and information are concurrently transmitted via single indoor network with each types of hardware. Experimental results demonstrate that the circuit switching system can configure a route from a certain source to an arbitrary load and power packets can be delivered to the correct destinations. Finally, future tasks are discussed for the application in practice.

5.2 Concept of On-demand Power Management Based on Information of Power

5.2.1 Principle of Management

Once photovoltaic generators, wind turbine generators, and/or fuel cells are installed in addition to commercial power, electricity of different quality is delivered via single in-home power distribution network after conversion. Generally, the power generated by renewable sources is inferior in the quality to the commercial power.

At present, secondary batteries are combined with distributed power sources to compensate the fluctuations of output power. Then, the output is adjusted to the quality of commercial power through converters and inverters. Most of the electric apparatus possesses conversion circuits internally in order to provide each components in the apparatus with suitable quality of power. However, this scheme is less efficient because the total losses increase due to multiple conversions. Some kind of electrical equipment which has built-in batteries, such as laptop computers, does not require high-quality input power. Besides, charging batteries in mobile devices is not necessarily a high-priority task, meaning that it is generally enough for charging to use intermittent surplus power. Furthermore, most of home appliances need dc feeding eventually. Therefore, the output power is not required to keep as high quality as commercial power. It it reasonable to connect a power source of sufficient quality with a given load depending on each request.

For achieving source-and-load matching, the quality and the amount of generated power must be known. Those of required power by loads also must be gathered. These information can be transmitted by means of Ethernet, wireless LAN, or other radio communication methods. However, these conventional means of communication require their own paths other than the distribution lines. As a result, when a distribution line is divided into several branches with power strip, one to one relation between the transmitted power and the information of the power is not necessarily sustained. It gives a conflict of supposed power flows to actual flows because of a lack of identification. In order to overcome the conflict, information should be transmitted concurrently with power via the same wiring.

Figure 5.1 depicts the conceptual diagram of the on-demand power distribution system in home. House service cables from power sources are connected into power routing equipment. Indoor network cables are also linked with the routing equipment. All the

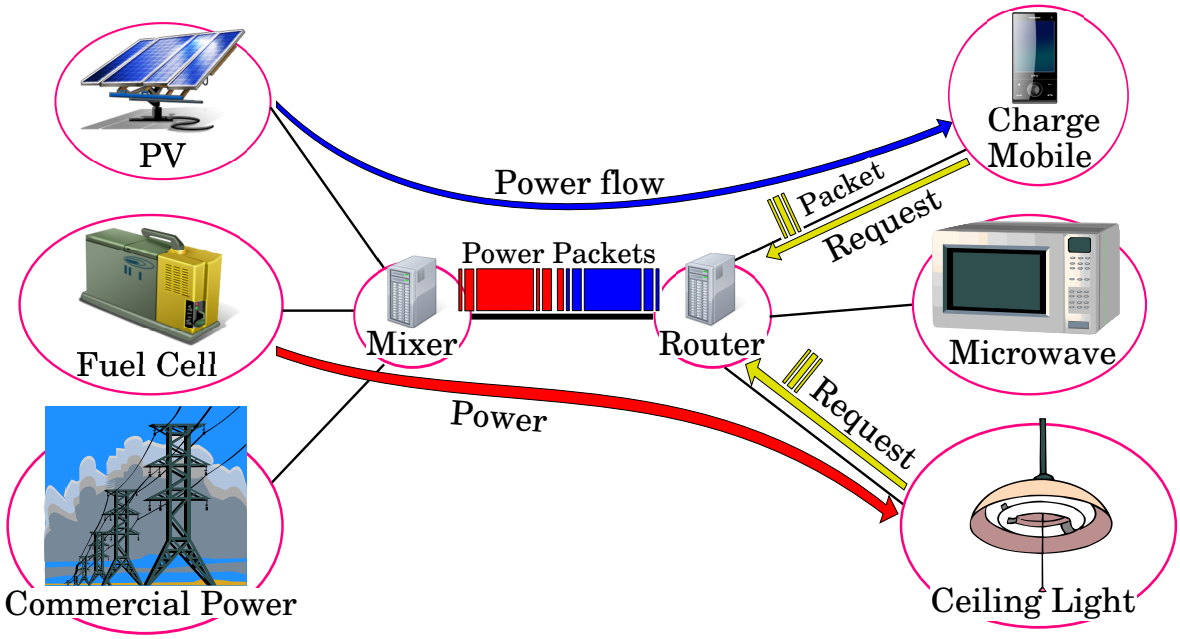


Figure 5.1: On-demand power distribution system in home. The system consists of power source, mixers, transmission lines, power routers, and loads. In the beginning, loading apparatus request for the router to supply power. Then electric power delivered by power packet.

power sources and loads are assigned unique IDs. Firstly, when the user wants to use an electric appliance, the appliance sends a request for supply of power to the router. The request consists of the amount of necessary power, quality of power required, ID number of the appliance, priority of the requests, and so forth. The routing equipment receives the information and selects a suitable power source correspondingly. Then the equipment configures the route from the suitable source to the load. Finally, it supplies power concurrently with its information, for example, the destination appliance, the amount of power, and the quality of power. The equipment collects all the information from sources and loads. It implies that this system is centrally managed, and on-demand feeding.

Two kind of system configurations are proposed to achieve the concept: the ac circuit switching system and the dc power packet dispatching system. In order to identify electricity with its source and a destination load, a power flow needs to be discriminated from others in proper way. The circuit switching system is based on a crossbar switch (Fig.5.2). The system divides power flows spatially. It means that each source-and-load pair is assigned with an unique transmission line. The information is superimposed on

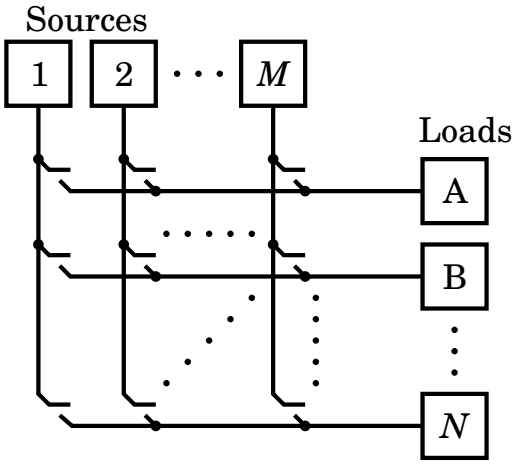


Figure 5.2: Simplified circuit topology of ac circuit switching system, which is equivalent to crossbar switch.

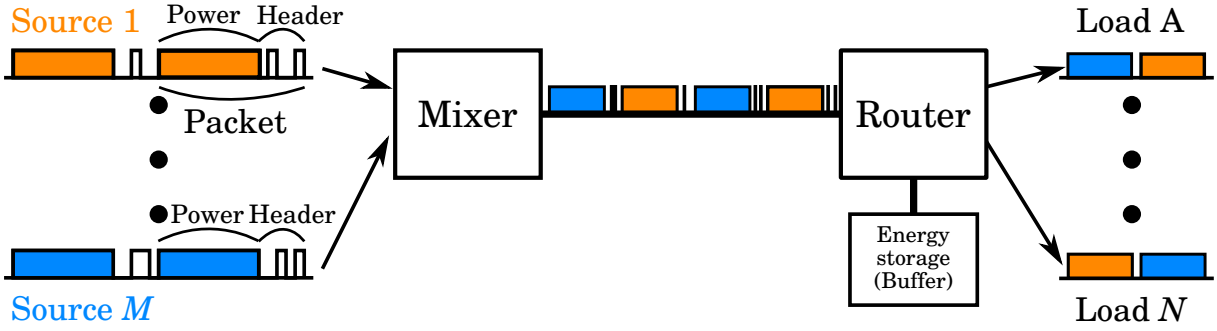


Figure 5.3: Schema of time division multiplexing (TDM) packet dispatching system. A mixer and a router are main components.

power waveforms by means of power line communications (PLC). The power in finite duration with its information can be recognized as an ac power packet. That is, the system is considered an ac power packet dispatching system. On the other hand, a dc power packet dispatching system is shown in Fig. 5.3. It introduces temporally separated power flows, which represents that power packets sent from each sources are transmitted by means of time division multiplexing (TDM). Therefore, all the source-and-load pairs share the feeder wires less than the number of coupling. The information of power is appended to each power packets as its header and/or footer. Though these systems are named as "ac" or "dc" for simplicity in designs and experiments, their configurations are essentially valid for both ac and dc.

5.2.2 Possible Scenarios

Here it is illustrated how to work the system by a couple of examples. At the moment when electric apparatus is turned on, electricity is not provided more than the power consumed for information transmission. After turning on the apparatus, it sends the unique ID of itself, the voltage ratio, necessary power, and so on to the routing equipment. In the case that the apparatus has built-in batteries and they are charged, the supplied power accepts relatively low quality, and the priority of request can be low. Charging mobile batteries and lighting may also be low priority task, according to the circumstances. On the contrary, commercial power of high quality is preferentially applied for important loads or equipment, like medical instruments, which do not have the tolerance to momentary voltage drop. The routing equipment decides suitable pairs of a power source and a load, referring to priorities, desired quality of power, and so on. The equipment can be optimized to choose renewable and natural power sources as much as possible. Finally, electric power is transmitted to the apparatus.

There is also a possibility of energy capping. It enables the consumer to set the maximum amount of whole consuming energy for a given period [78]. When the demand of electricity is likely to exceed the maximum value, the supply to low-priority load is shut until consuming energy drops below the threshold. For instance, air conditioners and heaters consume large amount of power at start-up. Microwave oven also needs much electricity. When this equipment is in use, charging batteries may be stopped or ceiling lights turned off for a while in order to reduce total power consumption. In this way, saving energy consumption is achieved unconsciously. Along the concept of power management, the power flow can be optimized to adjust the demand to the supply.

5.3 AC Power Distribution System by circuit switching with Power Router

This section describes the design of ac power routing equipment and shows experimental results on the power routing under a priori routing rules.

5.3.1 AC Power Routing equipment

The routing equipment is divided into two components in the ac circuit switching system according to their functions. One is an information terminal. The other is an

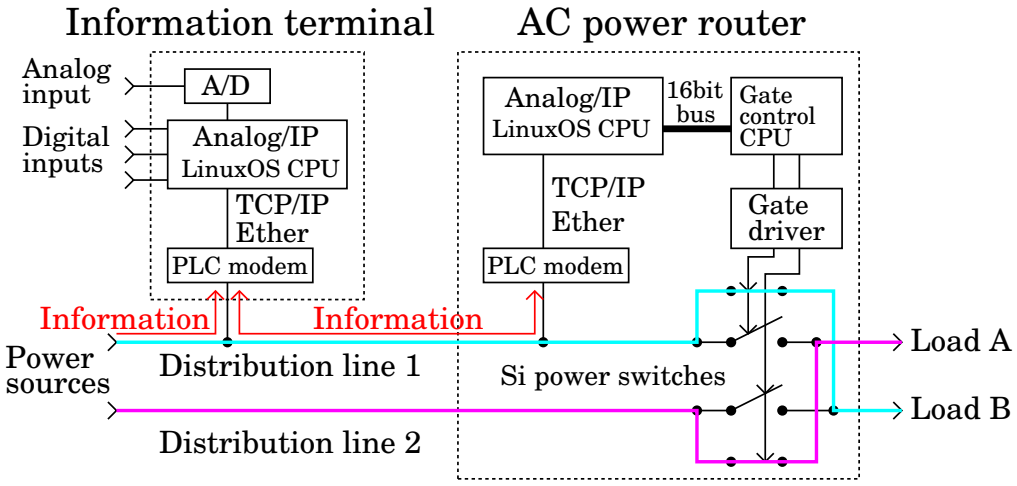


Figure 5.4: Block diagram of ac power routing system. Information transfers through PLC. Si power switches change line connections.

ac power router. Fig. 5.4 shows the schematic diagram of the system and Fig. 5.5 is a photograph of the developed ac power router and the accompanied information terminal. Each of the component includes a PLC modem (Sumitomo Electric Networks; MegaBit Gear MH2250) and the microprocessor (CPU, Renesas Electronics; SH7619) in which Linux OS is installed. The information terminal also has digital and analog I/O (Input and Output) ports as additional communication gateway except for the PLC modem.

The terminal gathers information from both power sources and loads. The CPU in the terminal decides the optimal combinations of the sources and the loads according to the information on supply and demand of power. The information of the source-and-load pairs is transferred to the power router through PLC.

The ac power router receives information about source-and-load pairs. The router has inputs of power and information and outputs of power. It possesses semiconductor power switches in order to change circuit topology. Here, Si MOSFETs (Toshiba; 2SK3935, 450 V, 17 A) are applied as switches because a number of uniform and optimized SiC devices are not available at this moment. The devices are selected to confirm the possibility of the proposed system. Even if SiC semiconductor switches are adopted, the system configuration of a circuit is fundamentally the same as the circuit under test. The router is equipped with extra CPU (Renesas Electronics; H8/3052F) to control these switches. The switches are split into two groups as shown in Fig. 5.5. The maximum number of operable sources and loads can be expanded by adding another group. In Fig, 5.5, two

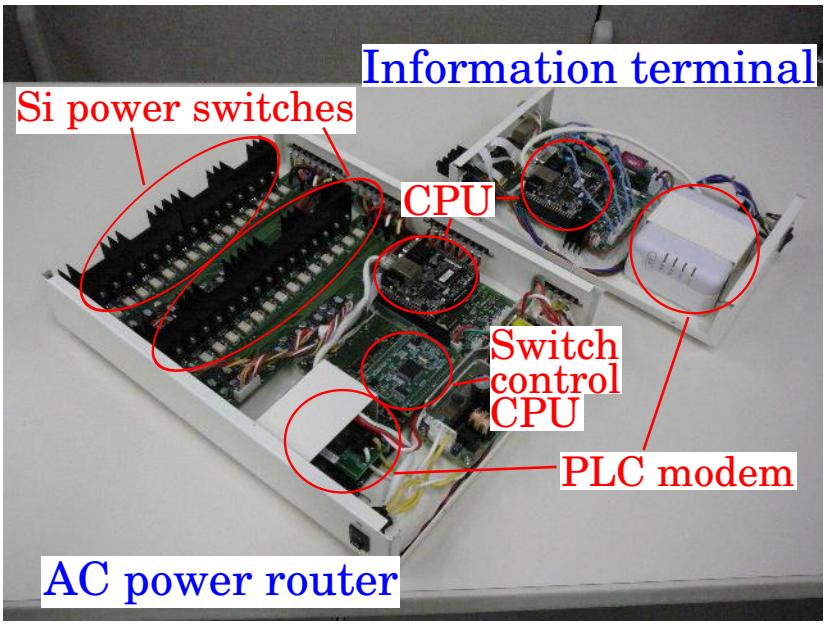


Figure 5.5: Photograph of prototype of ac power router (left) and information terminal (right). Each of them has a PLC modem and a CPU. The power router has two power inputs, two information inputs, and four power and information outputs.

inputs and four outputs are considered for illustration.

Figure 5.6 shows circuit exchange switches. The switch A is coupled with the switch B via logical inverter. Switches C and D are also connected by the hardware. These two groups are operated simultaneously by software. Therefore, whenever the switch A is close, the switch B and the switch C are opened and the switch D is close, and vice versa. Each switch A, B, C, and D consists of series connection of two transistors, whose polarities are reversed so as to block ac voltage as shown in Fig. 5.7. Note that it is not CMOS configuration. Circuit topologies are changed at the instant when v_{a} equals to v_{b} in order to suppress short current and prevent switches from breaking down by surge voltage. This technique of determining switching timing is named "equipotential switching".

5.3.2 Experiments of Circuit Switching

Experiments of power transmission were carried out using the existing technology a for proof-of-concept validation. Fig. 5.8 depicts the experimental setting of the ac power routing. For simplicity, the inputs and outputs of this setup are limited to two sources

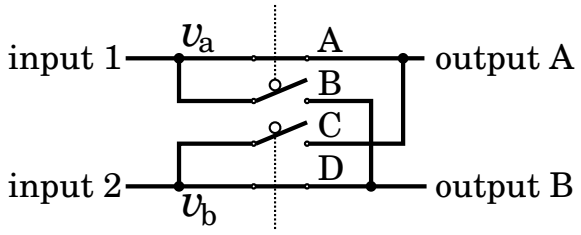


Figure 5.6: Schematic diagram of circuit exchange switches. Switch A interlocks switch B and switch C does D. A circle on the switch represents inverted operational logic, which means that switch A is close while switch B is open.

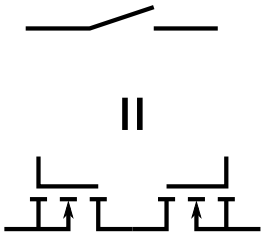


Figure 5.7: Schematic diagram of the composition of an exchange switch. The switch is made from two nMOS FETs which are connected in series but inverted polarity so as to block both positive and negative phases of ac voltage.

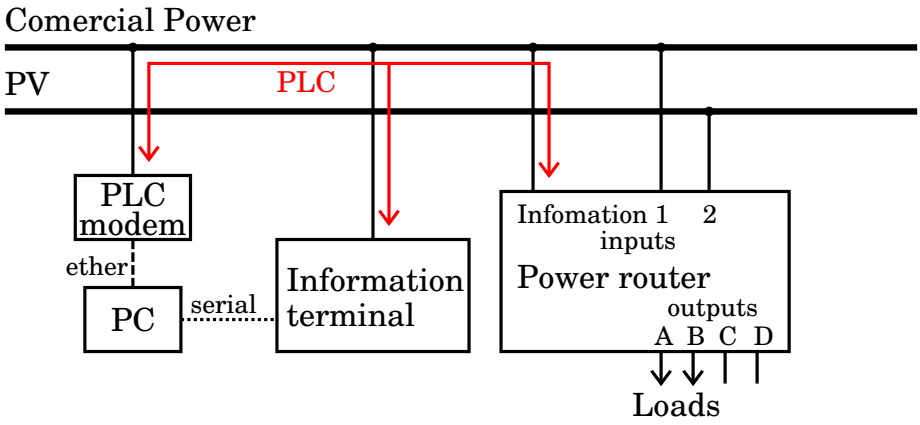


Figure 5.8: Schematic diagram of configuration of experiments. The routing of two inputs by two outputs is examined. The output C and D are not in use during the experiments. The routing rules are configured and programmed in PC in advance. Hence switching order go through the information terminal.

and two loads although the router has four output terminals. Inductive loads such as motors are excluded from the consideration. This is because most home appliances are equipped with switched power supply with a power factor correction (PFC) circuit, of which input current keeps in phase with the input voltage. Then resistive loads are only considered here without loss of generality.

The power rating of the system depends on the rating of power switches. Therefore, replacing power switch units improves the maximum operable power. Si power switches of 450 V, 17 A are adopted in the experiments under assumption of applying 100 V to the system. Hence, the router can switch at most 1.7 kW in the case.

A computer (PC) is connected with distribution line via a PLC modem and the information terminal via serial communication cable during the experiments. The PC sends switching commands to the information terminal by means of serial communication. Then the terminal sends information to the power router through PLC. The router changes connections of the circuit. In practice, however, the information terminal operates according to the input of digital I/O port, analog I/O port, or information sent via PLC. Therefore, the PC is not essential in practical use. Here, it produces simulated information from appliances programmed in advance and monitors the status of the power router.

Two power sources are available in the experiments. One is a 100 V/60 Hz commercial voltage source. The other is from photovoltaic (PV) panels. Regarding latter one, dc

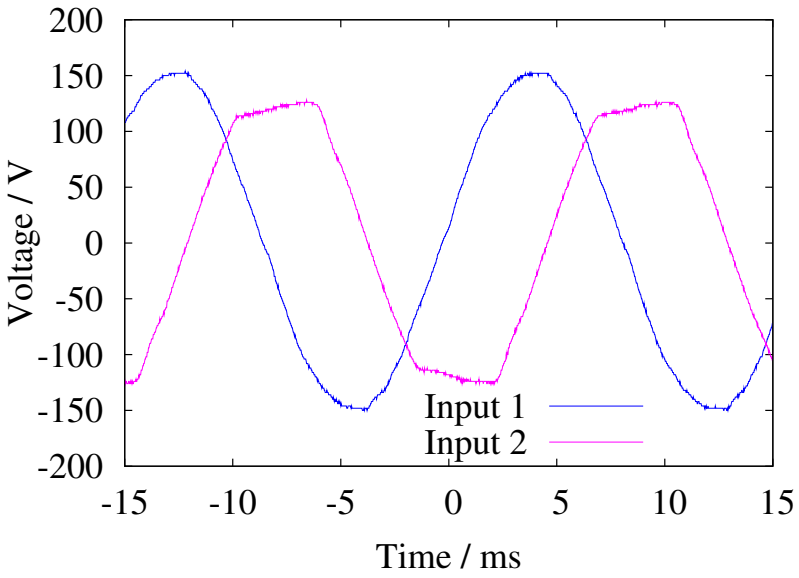
Table 5.1: Connecting pattern of inside power router.

Pattern	**Input**	
	1	2
(a)	Output A	Output B
(b)	Output B	Output A

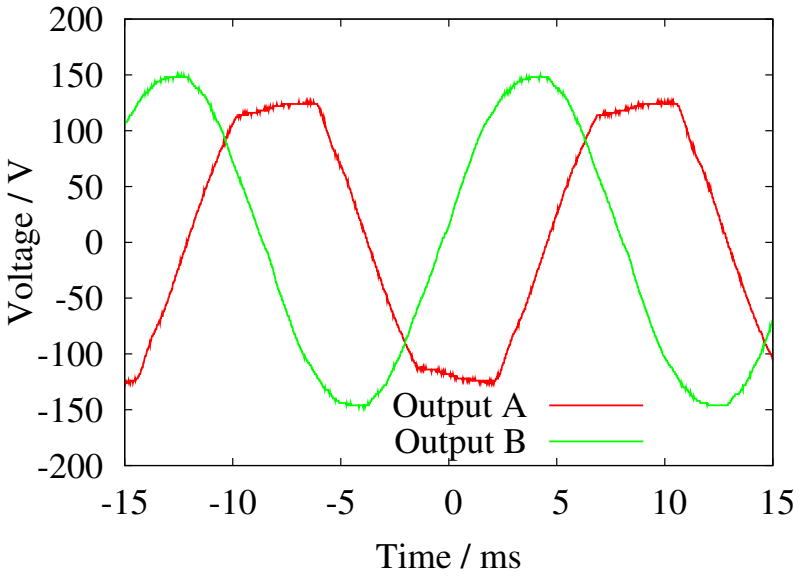
power generated by PV panels is converted into 100 V/60 Hz ac voltage by a power conditioner. The power conditioner can drive both independently from the commercial grid and interconnected with the grid. It operates in stand-alone mode (i.e. independent from the grid) during the experiments. In this case, the output voltage of the power conditioner has slight difference in frequency from the commercial voltage source. The frequency difference is less than 0.01 Hz. It changes depending on the amount of the power generated by the PV. The more power the PV generates, the faster the frequency becomes. It may be caused by the self-operating control scheme of the conditioner. The initial phase of voltage is determined voluntarily. An example of input voltage waveforms are shown in Fig. 5.9(a). Input 1 (blue line) is the commercial voltage and input 2 (purple line) is the voltage of the power conditioner. The phase of voltage of the power conditioner is different from that of commercial source, and the waveform of power conditioner is distorted particularly at the peak. These differences do not occur in general, depending on control schemes of power conditioners.

Two incandescent bulbs of 30 W are used as resistive loads A and B, connected to router outputs A and B, respectively. Fig. 5.9(b) shows voltage waveforms at output terminals A and B under the connection pattern (b) in Table 5.1. Red line indicates output A and green line indicates output B. Comparing with Fig. 5.9(a), the same waveforms appear to output waveforms. The transition from the pattern (a) to the pattern (b) is shown in Fig. 5.10. Although the circuit is designed to operate switches soon after cross point is detected, a delay of 1.05 ms appears. Around 50 V of difference in voltage between two inputs at the instant of switching is induced due to the delay. This delay is caused by processing time of the switch control CPU. In spite of the voltage difference, transient time of switching itself is less than 10 μs. Even in case that the loads include power conversion circuits internally, the transient is short enough to keep operation. Therefore, the circuit exchange is achieved successfully under the configuration.

The efficiency of the router for sinusoidal input voltage is estimated from the measure-



(a) Input voltage waveforms of the power router. Input 1 is from commercial grid and input 2 from PV through power conditioner. The waveform of input 2 is distorted.



(b) Output voltage waveforms of the power router. The red line draws voltage of output A and the green line output B.

Figure 5.9: Input and output voltage waveforms of power router. In the case that input 1 is connected to output A and input 2 to output B.

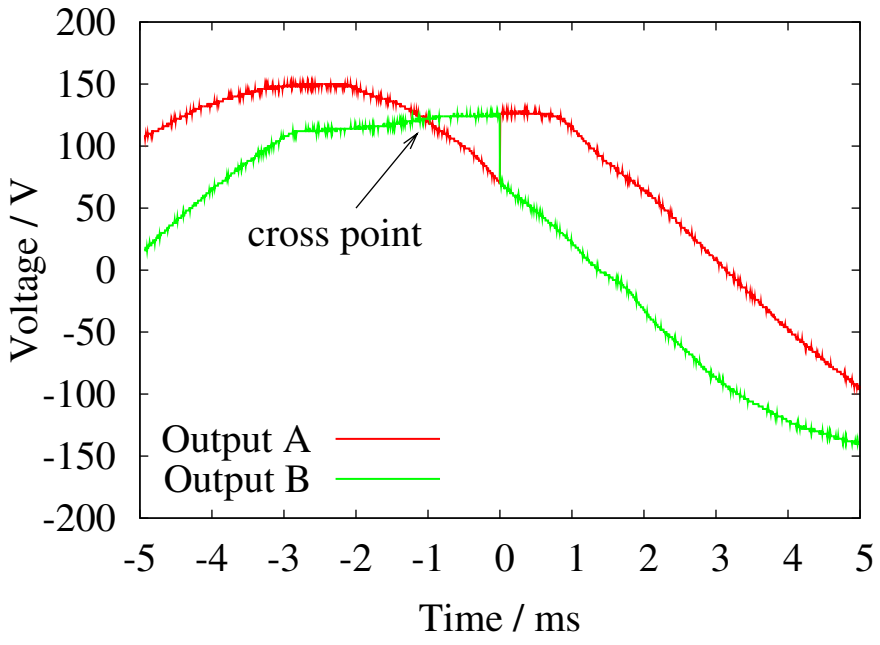


Figure 5.10: Output voltage waveforms of the power router around the instant of switching. The circuit switching is completed around 1 ms after the cross point is detected.

Table 5.2: Measured input and output voltage, current, and power.

	Input	**Output**
Voltage	104.31 V	104.13 V
Current	0.2359 A	0.2361 A
Active power	24.78 W	24.70 W

ment of input and output power under steady state with a power meter (HIOKI; 3193). Measured input voltage, current, power and those of output are shown in Table 5.2. The efficiency of the router is calculated to be 99.67 %. The system is significantly high efficient because the switching of circuit configurations arise much less frequently than switching power sources. Consequently, power dissipation in on-state resistance of semiconductor switches is more significant than switching loss. In the experiments, Si devices are utilized. Replacing Si switches with SiC transistors, of which on-state resistance is expected smaller than that of Si devices, will make the router more efficient.

5.4 DC Power Packet Dispatching System

The system explained in Section 5.3 is designed under assumptions that electrical power is analog and continuous quantity in a similar way with conventional discussions. Analog power is defined only by supplied voltage and impedance of loads according to Kirchhoff's law. Though, it is desirable to regulate supplying power actively. The system distinguish each power flow in it by dividing circuit spatially. Here, power distribution by power packets is proposed for advanced method referring to information transmission on IP-based network. This method can feed a number of loads with electric power by time domain multiplexing (TDM) of the packets, that is, temporally division of electricity. The packetization of electricity is equivalent to digitization of electricity. Using power packets, providing power is easily regulated by controlling the number of sending packets. In addition, almost all of recent electric instruments are driven by dc power and have built-in power conversion circuit to commutate ac input voltage. Thus, dc base power distribution is feasible with respect to efficiency improvement, for conversion losses can be eliminated by removing dc-dc converters from the instruments.

5.4.1 System Configuration and Power Packet

Figure 5.3 depicts the schematic diagram of the power packet dispatching system. The system consists of multiple sources, multiple loads, a mixer, a router, and single distribution line which connects the mixer and the router. Each source and load is assigned unique address individually. The system is designed for TDM. Therefore single source supplies power to single corresponding load at an instant.

Power packet

The supplied power from sources is divided into several units of payload. A header and a footer are attached to the unit in order to form a power packet and to attach a tag. The structure of a power packet is shown in Fig. 5.11. A power packet is composed of a header, a payload, and a footer. The header consists of the start signal which marks the start of the packet. It also includes the destination address to the load and information of power such as quality of power and quantity of it. The header may also contains the address of the sender.

The payload carries power. The amount of supplied power per packet is regulated

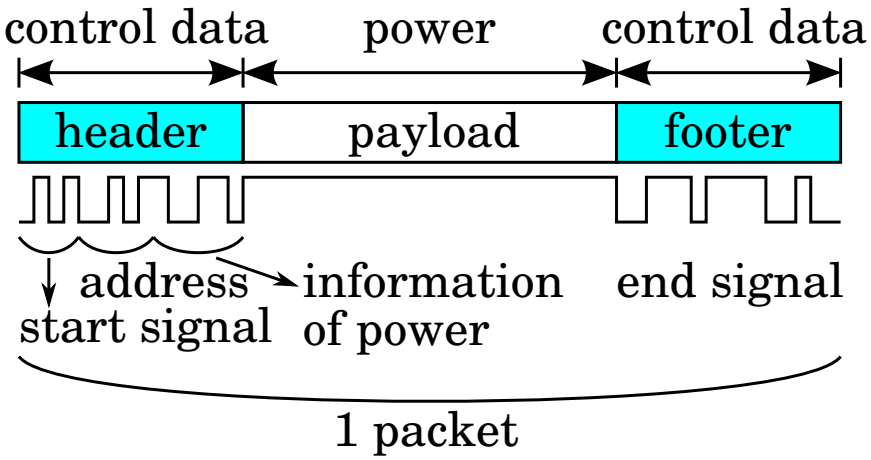


Figure 5.11: Sketch of structure of power packet. The power packet consists of a header, a payload, and a footer. The header and the footer contains information about power, destination, and its origin. The payload is transmitted power.

by changing the length of payload or modulating power waveform in the payload. The modulation can be achieved, for example, by a pulse width modulation, a pulse density modulation, and so on.

The footer contains the end signal. It represents the end of the packet. The other information can be included in it for the use of the operation.

The frequency of header and footer should be set at several mega hertz in order to shorten the time when the power does not transmitted to the loads. On the other hand, modulation frequency of payload is less than 10 times lower than that of the header, that is, around several tens to hundreds kilo hertz, in order to reduce switching loss. That frequency range is high enough for loads to receive continuous power flow if capacitors as a buffer are connected with loads properly, referring to the operation of switching power sources. An amplitude of the header and the footer is not necessarily the same as the payload because the header and the footer are only used for communications. A request to send power is given by transmitting packet with null payload.

Mixer

Figure 5.12 depicts the configuration of one channel of the mixer. In the application, the channels connected each other in parallel, corresponding to the power sources. The mixer processes power packets and sends them to single distribution line. Each input

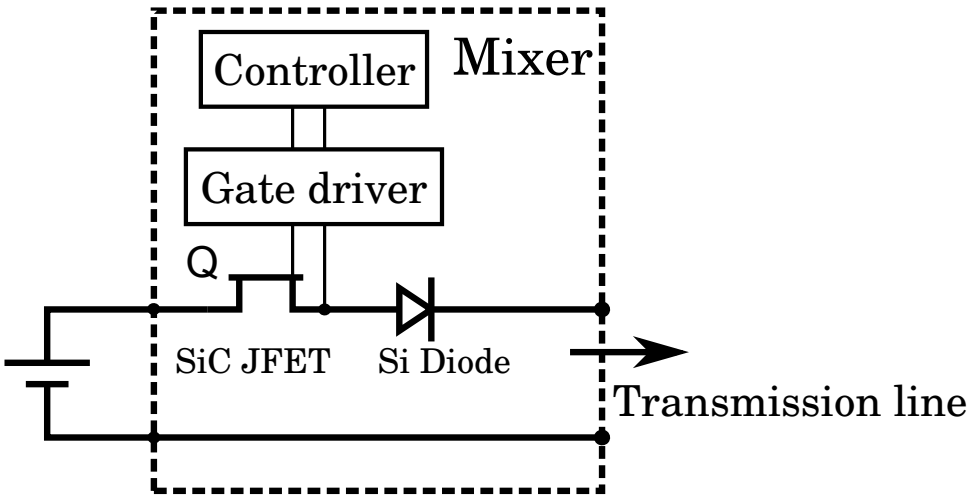


Figure 5.12: Sketch of one channel of mixer. The mixer forms power packets by switching power from the source.

terminal has the semiconductor switch in order to select a power source and form packets by chopping the continuous power flow. While one switch is operating, the others keep off-state so as to process only one input power. The SiC JFETs which are examined in Chapter 3 are used as the switches. An FPGA (Field Programmable Gate Array, Xilinx; Spartan-6 XC6SLX16), of which clock frequency is 200 MHz, is adopted as a controller. The JFET is operated by the controller with the gate driver which was introduced in Chapter 2. A diode inserted next to the JFET prevents returning current to the power supply.

Router

The schematic of the router is shown in Fig. 5.13. It consists of load select switches and a controller. The figure shows the case of one input and two outputs setup. The output channel can be expanded by adding output brunch including a load select switch. The SiC JFETs shown in Chapter 3 are used as the switches and driven by the gate driver introduced in Chapter 2. When the router receives packets, they are sorted according to the address in the header by the controller and sent to loads. Data for control is shunted from the distribution line and its voltage is divided into proper amplitude for signal processing. The signal is input into the controller through an isolator to insulate the low-power signal circuit from the high-power main circuit. The switches are off in a normal

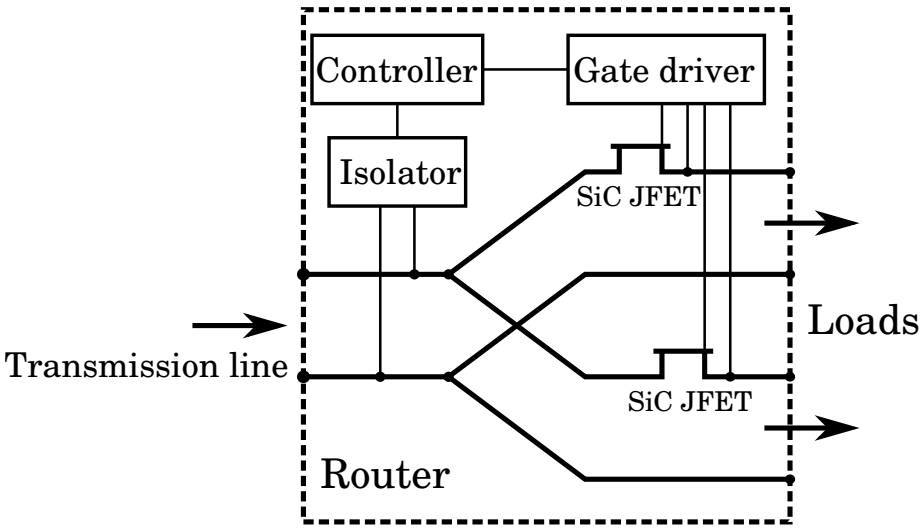


Figure 5.13: Schematic diagram of the router, which has one input terminal and two outputs.

state. When the controller detects the destination address in the header, the switch of the output terminal which corresponds to the address is closed. An energy storage can be connected to the router for buffering packets and/or smoothing power distributed to the load.

5.4.2 Experiments of Power Packet Dispatching

An experiment of packet processing and dispatching was performed under following assumptions for simplicity:

- Testing system has the minimum number of sources and loads: one source and two loads,
- Only the start signal and the address of the receiver are given to the header,
- The footer only contains the end signal,
- Routing rules are fixed and embedded in the controller in advance,
- Payload is not modulated.

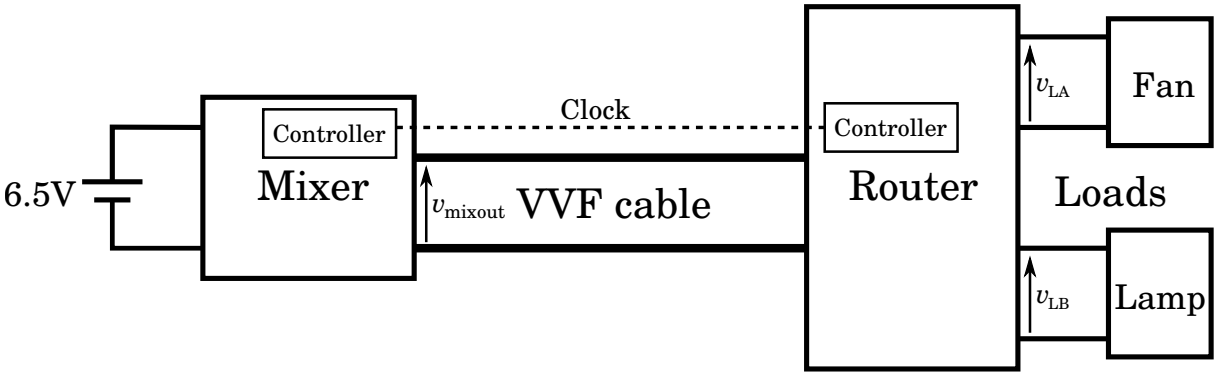


Figure 5.14: Experimental configuration of dc packet dispatching system.

Experimental Settings

Figure 5.14 shows the experimental configuration of the dc power packet dispatching system. A VVF (vinyl insulated vinyl sheathed flat-type) cable connects the mixer and the router. The cable is typically used for in-home feeding cables. In addition, an extra cable ties between the controller in the mixer and that in the router in order to share a clock signal for a synchronous operation. A voltage source of 6.5 V supplies power. A dc fan and a lamp are adopted for the loads.

Under the settings, power flow from the source is formed into power packets and the each destination address of the two loads is added to the packets alternately. The experiments were carried out under very long packet length and very low frequency of the header and the footer so that it can visibly exhibit the packet transmission by TDM. The length of payload is set at 1 s. The frequency of header and footer is 100 Hz. This frequency is lower than supposed value but it does not loose the generalities for the confirmation of the concept. From the experimental results in Section 3.3, the circuit possibly operates at sufficient high frequency for packet processing. The header of the packet consists of 3 bits of start signal and 3 bits of address. The footer is 5 bits. These codes are indicated in Table 5.3.

The controller of the router is designed for processing the header and the footer of above settings. In this experiments, it is composed by standard logic ICs. For designing sequential circuit, the state diagram of the controller is set as in Fig. 5.15. The diagram represents the followings: when the controller receives the address of load A, the control signal is generated to make only the switch A on and others off, and vice versa. Con-

Table 5.3: Binary codes of header and footer. The header consists of 3bits of start signal and 3bits of address. The footer is 5bits.

header	
start signal	101
address of load A	011
address of load B	010
footer	
end signal	10100

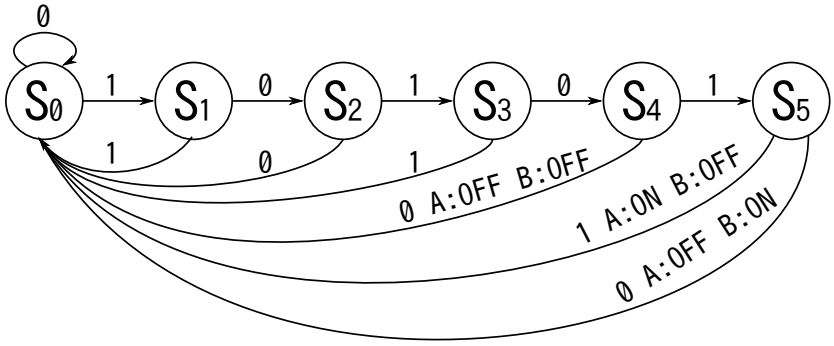


Figure 5.15: State diagram of the controller in the router.

sequently, the controller is designed as in Fig. 5.16. The photograph of the controller is Fig. 5.17. This controller includes optcouplers as isolators in Fig. 5.13.

Experimental Results

Figure 5.18 shows the measured waveforms of the output voltage of the mixer v_{mixout} and the load voltages v_{LA} and v_{LB}. Red line is v_{mixout}, blue v_{LA}, and purple v_{LB}. The entire waveforms appear in Fig. 5.18(c). Fig. 5.18(a) is enlarged waveforms of region A. It shows a footer of the packet which goes to the load A, a header of the packet to load B, and v_{mixout}. When time is around 0, v_{mixout} and v_{LA} present the same waveforms. This is the packet's end signal whose pattern is 10100 (see Table 5.3). After the end signal, the load select switch A is opened, and tens of pulses appear on v_{LA}. The pulses are the voltage induced by the back electromotive force due to idling of the fan. Afterward, the header of the next packet which pattern is 101011 appears. Power is supplied after the header is processed. In the figure, it is confirmed that v_{LB} rises after the entire header passing through. On the contrary, Fig. 5.18(b) depicts a header of the packet to B and a

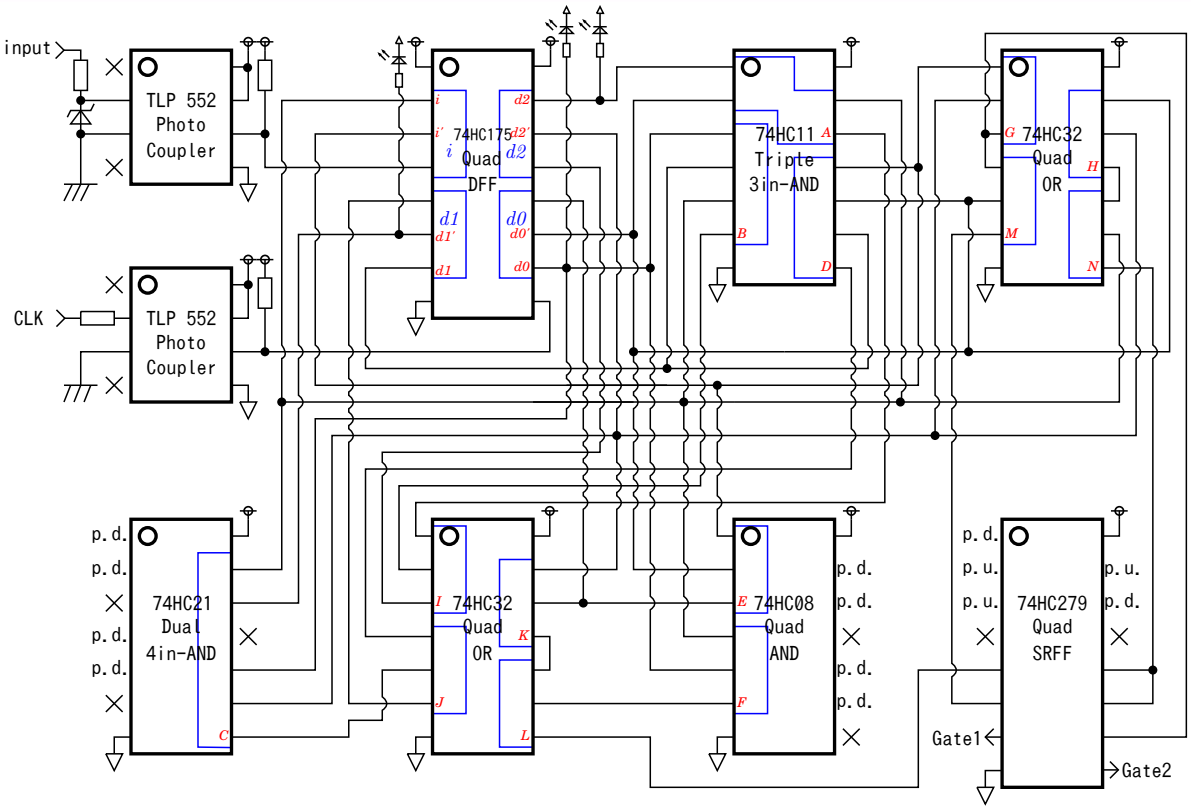


Figure 5.16: Schematic diagram of the controller in the router.

Figure 5.17: Photograph of the controller.

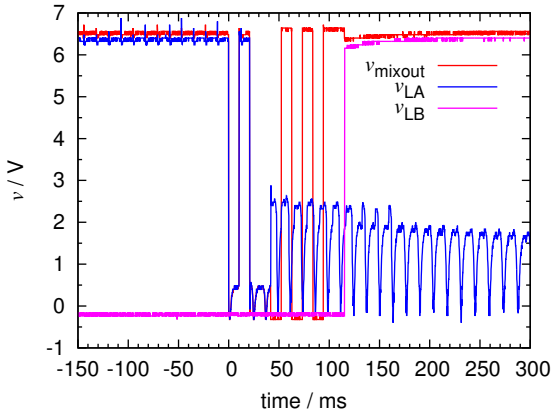
footer of the packet to A. After the footer of the packet to load B is detected, v_{LB} falls to 0. Then, v_{LA} rises after the header of the pattern of 101010 ends. From these figures, power packets are configured and correctly sent with TDM. It means that signal processing and power waveform shaping are achieved simultaneously by a single semiconductor switch in the mixer. And power routing is accomplished in the rooter.

5.5 Summary

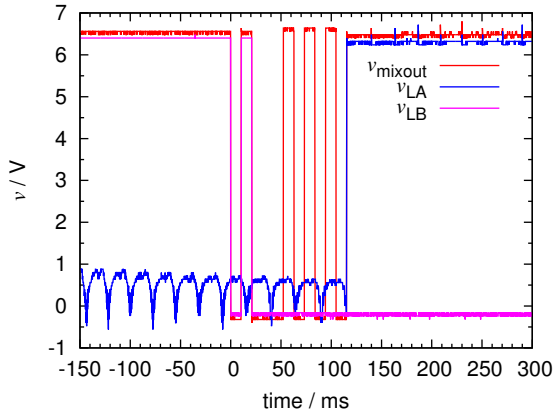
The circuit switching type power routing system was proposed for regulating electricity in home utilizing both renewable energy sources and commercial power sources. The ac circuit switching system was designed on the basis of conventional technologies and operated successfully for the examination of the routing concept. As a result, the ac power with the information can be routed and dispatched to resistive loads with temporal and special matching while keeping the identification of power information. This paves the way for the development of power distribution methods based on the power packet dispatching. The operations of the system with inductive and capacitive loads also need to be confirmed. The modulation method of the power packet is our next step for the realization of the proposed system.

In the application of SiC power devices as the main switches, the equipotential switching will not be necessary due to the high breakdown voltage of SiC in the ac circuit switching system. In addition, the system will promote the efficiency of in-home power distribution system and manage the in-home energy flows to adjust supply and demand much easier.

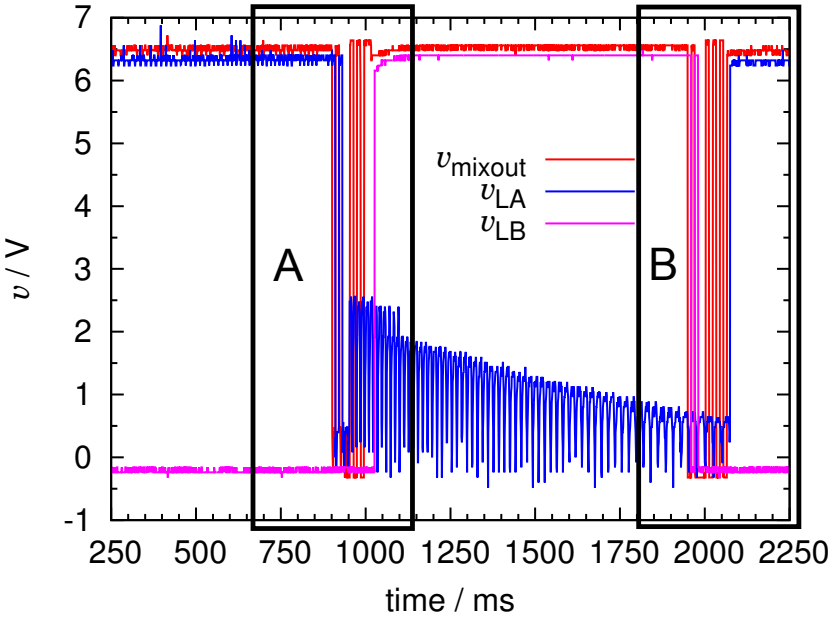
The dc based packet dispatching system was also proposed with an exhibit of packet processing. For the dc packet dispatching system, the amplitude of dc packet can become higher. The frequency of header and footer can be also set higher, which lead to decrease of the ratio of the control signal length to the length of the payload. Experimental results show that new power distribution methods are achievable. And these systems will make in-home power distribution system more efficiency and more easier to control energy flow.



(a) Enlarged headers and footers of region A.

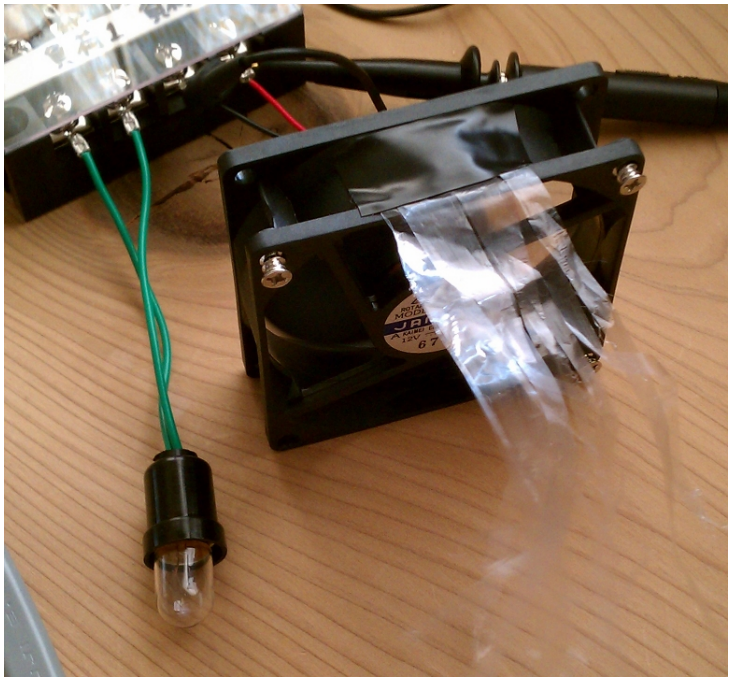


(b) Enlarged headers and footers of region B.

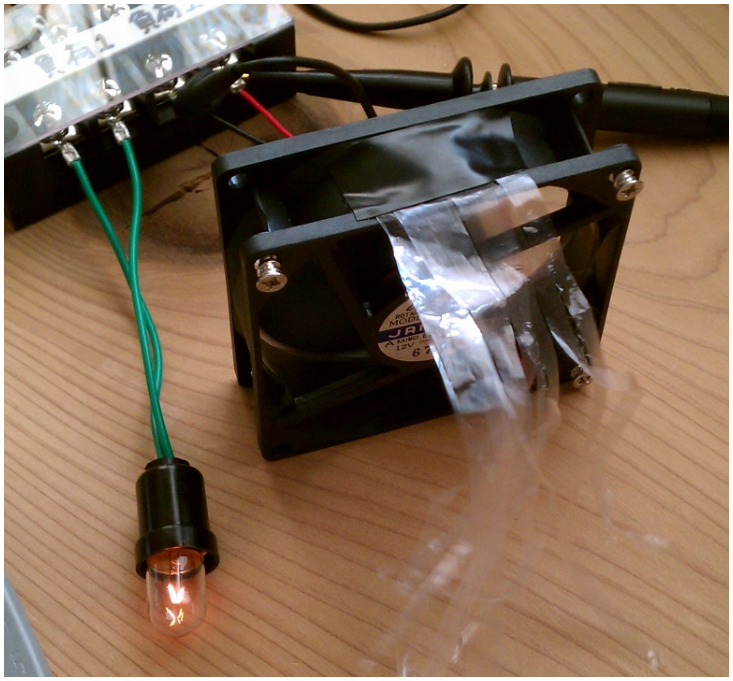


(c) Entire waveforms.

Figure 5.18: Waveforms of packets. v_{mixout} is output voltage of the mixer. v_{L1} is output voltage of the output terminal for the load A of the router. v_{L2} is that of load B. Red line is v_{mixout}, blue line V_{LA}, and purple v_{LB}. (a) The footer of packet for the load A and the header of packet for the load B. (b) The footer of packet for the load B and the header of packet for the load A. (c) Whole shape of the packets.



(a) A packet is delivered to the load A. The fan is running. The lamp turns off.



(b) A packet is delivered to the load B. The fan is idling. The lamp turns on.

Figure 5.19: The photographs of loads while packets are dispatched.

Chapter 6

Conclusions and Future Works

In this dissertation, normally-on SiC JFET were characterized in high-frequency switching circuit under hard-switching condition and soft-switching condition for application to in-home power distribution system which transmit information and electricity together. Then, the two kind of power management systems were designed and produced for evaluation of the possibilities of the system. The major conclusions and future works are presented as follows.

6.1 Conclusions

In Chapter 2, a high speed gate drive circuit was proposed for a normally-on power switching devices with inherent safety. Employing insulated signal coupler using RF signal instead of photo coupler enables to drive SiC JFET up to 15 MHz. Special arrangement of driver also permits normally-on devices to operate as same as normally-off devices. This circuit pushes forward applications of normally-on SiC JFETs to power conversion circuits more widely. SiC power switching devices allow switching power conversion circuits to operate at high frequency, which will lead to decrease dimensions of power sources and to give new functionality to conversion circuits. The configuration indicates criteria of designing new gate drive circuits.

In Chapter 3, normally-on SiC RESURF JFET was driven by the gate drive circuit designed in Chapter 2 at high switching frequency under hard-switching condition. The switching characteristics of the JFET were evaluated by observing voltage and current waveforms in time domain and frequency domain. The analysis in time domain showed that the ringing induced by the switching is caused by the resonance of wiring induc-

tance in the circuit and junction capacitors in the semiconductor device. An increase in switching frequency makes it come closer to ringing frequency. That implies high frequency hard-switching can be change into soft-switching by careful prediction and design of parasitic elements. Power dissipation with respect to switching frequency indicated that ringing significantly contributes to the amount. Due to the large power dissipation in the device and high-ordered harmonics components in the spectrum of load power, soft-switching should be considered for high-frequency switching.

In Chapter 4, class-E power amplifier was studied as one of the soft-switching circuits in order to improve the efficiency high-frequency switching circuit and depress noise emission. Numerical simulation and experiments were carried out under switching frequency of 2 MHz and 13.56 MHz. In case of lower frequency, the circuit operated almost class-E condition. However. the upper frequency, the circuit operated out of the condition due to the existence of ringing. The large ESR of the choke coil decreased the efficiency of the circuit. The spectrum of load power showed the possibility of suppression of high-order harmonics emission. From these results, class-E circuit has the potential to operate in high switching frequency.

In Chapter 5, two types of power routing systems were proposed for regulating electricity in home utilizing both renewable energy sources and commercial power sources. These are new applications of SiC power devices utilizing their capability instead of the applications to the replacement of conventional power devices. The ac circuit switching system was designed on the basis of conventional technologies and operated successfully for the examination of the routing concept. As a result, the ac power with the information can be routed and dispatched to resistive loads with temporal and special matching while keeping the identification of power information. This paves the way for the development of power distribution methods based on the power packet dispatching. The operations of the system with inductive and capacitive loads also need to be confirmed.

In the application of SiC power devices as the main switches, the equipotential switching will not be necessary due to the high breakdown voltage of SiC in the ac circuit switching system. In addition, the system will promote the efficiency of in-home power distribution system and manage the in-home energy flow to adjust supply and demand much easier.

The dc based packet dispatching system was also proposed with an exhibit of packet processing. In the case of using SiC devices for switches, zero-cross switching will not be

necessary due to the high breakdown voltage of SiC in the ac circuit switching system. For the dc packet dispatching system, the amplitude of dc packet can become higher. The frequency of header and footer can be also set higher, which lead to decrease of the ratio of the control signal length to the length of payload. Experimental results show that new power distribution methods are achievable. And these systems will make in-home power distribution system more efficiency and more easier to control energy flow.

6.2 Future Works

In this dissertation, the results presented above have been clarified. For the progress of studies, there still remain some issues to be considered as follows.

Ringing in class-E power amplifier at high-frequency The ringing reduce the efficiency of the circuit. Furthermore too much amplitude of ringing breaks class-E operation of the circuit. Therefore the suppression of ringing is important issue. However, from the point of view of resonance, the ringing is also a kind of resonance phenomenon. Hence, there is possibilities to utilize parasitic elements as circuit components in resonant network in a positive manner by fine designing of the circuit and device.

Large ESR of the choke coil in class-E circuit The ESR of the choke coil also reduce the efficiency very much. The ESR mainly comes from two factors. One is iron loss in ferrite core of the choke. And the other is self induction of winding wire. The former can be reduced by using alternative material. The latter may be solved by changing the manner of wire winding.

Soft-switching in power distribution system In Chapter 5, hard-switching configuration is adopted in both ac and dc power distribution systems because of simplicity of the circuit configuration. However, if the problem of low efficiency in class-E switching circuit have solved, the soft-switching circuit would be suitable from a standpoint of noise suppression. For the practical application of the distribution systems, the routers and mixers are surrounded by a lot of home appliances. In the environment, electromagnetic compatibility is strongly required.

High-frequency propagation characteristics of house distribution cables In the power packet dispatching, power waveforms become square-shaped. The square-shaped wave has a lot of high-ordered harmonics in its spectrum. In order to transmit the power packets keeping their shapes, the propagation characteristics of distribution line play a crucial role. However, generally it is not considered that high-frequency signal transmission through the house distribution cables. Therefore, the characteristics and the problems which will occur should be predicted, referring to the researches [79, 80]

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