Interface Control of AlGaN/SiC Heterojunction and Development of High-Current-Gain SiC-Based Bipolar Transistors

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Abstract

In this thesis, SiC-based bipolar junction transistors (BJTs) are studied toward advanced high-power and low-loss switching applications. To realize high performance BJTs, this thesis focuses on the improvement of current gain that is one of the critical parameters determining the power loss in bipolar transistors. Device design, epitaxial growth, and device processing of SiC BJTs are investigated. Record-breaking current gain ($\beta > 250$) as well as record-high blocking voltage ($V_{\mathrm{CEO}} > 17$ kV) in SiC BJTs are demonstrated. In addition, toward further improvement of current gain, an alternative device structure, Ⅲ-N/SiC heterojunction bipolar transistors (HBTs), are proposed as next-generation power switches. To develop high-current-gain HBTs, growth of Ⅲ-N on SiC as well as the interface control of Ⅲ-N/SiC heterojunction are investigated. Fabrication process optimized for Ⅲ-N/SiC HBTs is also established. With these efforts, the author demonstrates the first common-emitter-mode operation ($\beta > 10$) in AlGaN/SiC HBTs.

In Chapter 3, suppression of surface, interface, and bulk recombination in SiC BJTs are investigated to improve the current gain. The author proposes a novel deep-level-reduction process based on thermal oxidation to suppress the bulk recombination. Then impacts of suface passivation processes on the current gain of SiC BJTs are investigated. Using deposited-oxide passivation with post-deposition anneal in N_2O or NO, a high current gain β of 73 – 102 is achieved due to the suppressed surface recombination, whereas BJTs having conventional thermally-grown oxides show a current gain β of 50.

Moreover, continuous growth of emitter-base junction in SiC BJT structure is investigated to reduce the interface recombination. A record current gain β of 257 at room temperature and 127 at 250°C are demonstrated in 4H-SiC BJTs, which is twice as high as the previous record gain. The results suggest that the combination of the surface passivation with deposited oxides annealed in NO, continuous epitaxial growth of the emitter-base junction, and deep-level-reduction process based on thermal oxidation dramatically improve the current gain. Toward further reduction of the surface recombination, SiC $(000\bar{1})$C-face is utilized. The author achieves C-face BJTs showing the highest current gain β of 439 among the SiC BJTs ever reported.

Furthermore, ultrahigh-voltage SiC BJTs with novel edge termination techniques featuring two-zone-junction termination extension and space-modulated guard rings are reported. The author achieved ON-resistance of 242 $\mathrm{m\Omega cm^2}$, which is below the SiC unipolar limit,

as well as the open-base blocking voltage V_{CEO} of > 17 kV, which is the highest blocking voltage among any semiconductor switching devices.

In Chapter 4, growth of GaN on SiC off-axis surface and fabrication of GaN/SiC HBTs are presented. Crystal quality of GaN is evaluated by various charaterization methods. The GaN layers grown on off-axis SiC showed step bunching due to the large off-angle of the substrates. It contributes to the annihilation of edge dislocations as revealed by XRD and TEM analysis. Hall-effect measurement shows the GaN layer has adequate electron mobility as well as carrier concentration, suggesting that the GaN on off-axis SiC substrate is applicable for the emitter of GaN/SiC HBTs.

Subsequently, the impact of base doping concentration on electronic properties of the GaN/SiC heterojunction and HBTs are investigated. By utilizing reduced doping of 1×10^{18} cm^{-3} instead of 1×10^{19} cm^{-3}, tunneling current via interface traps is suppressed, resulting in significantly improved rectifying behavior in GaN/SiC heterojunction diodes. *C-V* characteristics revealed that the band lineup of GaN/SiC is type Ⅱ with a potential barrier of $0.65-0.76$ eV. In accordance with diode characteristics, GaN/SiC HBTs show improved current gain by employing reduced base doping concentration. A common-base current gain α of $0.01-0.03$ is obtained in GaN/SiC HBTs.

Next, GaN/SiC HBTs with ultrathin ($1-4.5$ nm) AlN spacer layers at the n-GaN/p-SiC emitter junction are proposed in attempt to improve the electronic properties of GaN/SiC heterojunction. The insertion of AlN spacer is found to be promising in terms of electron injection efficiency due to the reduced potential barrier (0.46 eV-0.54 eV) to electron injection and smaller recombination via interface traps, resulting in an improved current gain α of $0.1-0.2$.

In Chapter 5, AlGaN/SiC HBTs with AlN/GaN short-period superlattice as a widegap emitter are proposed to obtain better electronic properties in Ⅲ-N/SiC heterojunction. Crystal quality of AlGaN as well as the impact of Al composition on the electronic properties of AlGaN/SiC heterojunction and HBTs are evaluated. By utilizing Al composition of over 0.5, the band lineup of AlGaN/SiC can be controlled from type-Ⅱ to type-I, and tunneling current via interface traps in AlGaN/SiC heterojunction is greatly suppressed, resulting in the first common-emitter mode operation with β of 2.7 in the HBTs. Toward further improvement of current gain, the effects of n$^-$-SiC spacer between n-AlGaN and p-SiC, and p-SiC base width are also investigated. By utilizing 200 nm-thick n-SiC spacer and 250 nm-thick p-SiC base layer, an improved current gain β of 13 was realized. Finally, trials of atomic control of AlGaN/SiC heterointerface is described toward high-current-gain AlGaN/SiC HBTs.

In Chapter 6, a summary of the present study as well as the future outlook are given.

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Contents

Chapter 1

Introduction

1.1 Background

The success of the semiconductor industry over the last several decades traces back to the discovery of the transistor effect in 1947. With the subsequent development of semiconductor devices, notably, metal-oxide-semiconductor field-effect transistors (MOSFETs) in the late 1950 s, semiconductor technology rapidly expanded beyond its bulky vacuum-tube origins due to the compact and advanced characteristics, and realized various kinds of electronic devices such as integrated circuits (ICs), large-scale integration (LSI), power transistors, and radio-frequency (RF) devices as well as optoelectronic devices such as light-emitting diodes (LEDs) and laser diodes (LDs). The advent of such devices has without any doubt transformed the way people live, creating modern societies and high standards of living. On the other hand, increased energy consumption and related CO_2 emission due to rapid economic growth have become serious areas of concern related to depletion of fossil fuels and global climate change. Thus, efficient use of energy and development of environmentally friendly devices have become increasingly important for achieving a sustainable society along with economic growth. Accordingly, a strong need has emerged for the development of low-loss, highly efficient semiconductor devices.

When it comes to the electronic devices, silicon (Si) has been widely used in modern semiconductor technology. Its application ranges from home applications such as personal computers and related electronic devices, to industrial applications such as motor control and electric power conversion, and the device structure changes from nano-scale, low-voltage transistors to large-scale, high-voltage power transistors according to their applications. Among these devices, power transistors which handle hundreds of amps play an important role in achieving high energy efficiency. At present, Si power MOSFETs or insulated-gate bipolar transistors (IGBTs) are employed as power switches. Although intensive efforts have been devoted to improving their performance, these devices are approaching a theoretical limit determined from the material properties of Si, so that there has been a strong need for next generation semiconductor materials which enable ultra-low loss switching and therefore

energy saving. To meet these demands, a wide bandgap semiconductor, silicon carbide (SiC), has become a promising candidate owing to its excellent properties.

1.2 SiC Power Devices for High Energy Efficiency

1.2.1 Properties of SiC

SiC is a group IV–IV compound semiconductor composed of tetrahedrally bonded silicon (Si) and carbon (C) atoms in a close-packed structure. Historically speaking, SiC has been used for polishing powders and heat-resistant coatings over about 100 years due to the excellent thermal and chemical stabilities thanks to the strong bonding of Si–C. At the same time, SiC has superior characteristics as a semiconductor material. The physical properties of SiC and other semiconductor materials such as Si, gallium arsenide (GaAs), gallium nitride (GaN), and aluminum nitride (AlN) are listed in Table 1.1. As shown in Table 1.1, SiC shows wide bandgap, high critical electric field, high thermal conductivity and high saturation velocity, making it an excellent material for high power, high temperature, and high frequency applications. Note that SiC has numerous crystal structures with the same chemical composition, which are so called polytypes, and the most popular and important polytypes for electronic device applications, namely 3C-, 4H-, and 6H-SiC, are chosen in Table 1.1. Here polytypes are represented by the number of Si–C bilayers in the unit cell and the crystal structure (C for cubic and H for hexagonal) according to the Ramsdell's notation [1]. The polytypes are simply explained as follows: Considering the Si–C pair as a sphere, there are three possible occupation sites denoted by A, B, and C as shown in Fig. 1.1. For example, the B- or C-site bilayer can be placed on the A-site bilayer. Two simple stacking sequences are ABCABC... and ABAB..., so-called "zincblende (3C)" and "wurtzite (2H)" structures, respectively. More than 200 polytypes have been found in the case of SiC. The schematic structures of 3C-, 4H-, and 6H-SiC are shown in Fig. 1.2. The mechanical properties are almost invariant with polytype, whereas the electrical and optical properties drastically change with the polytype. Among 3C-, 4H-, and 6H-SiC, 4H-SiC is considered to be the most suitable polytype for power devices, because of a wider bandgap and high mobility. Compared with Si, which has been the mainstream semiconductor to date, the bandgap of 3.26 eV at room temperature (RT) is 3 times higher so that the low intrinsic carrier density is obtained in SiC. This feature makes it possible to operate SiC power devices at high temperatures above 500°C, whereas Si power devices are typically limited to 150°C. The breakdown electric field of 3 MV/cm is by a factor of 10 higher than that of Si, allowing the reduction of ON-resistance R_{ON} in power devices, as discussed later. In addition, the high saturation drift velocity (2×10^7 cm/s) enables devices to operate at high frequencies. Moreover, heat generated in devices by Joule heating can easily be transferred to a heat sink due to the high thermal conductivity of SiC (5 W/cmK). With those excellent material properties of 4H-SiC, power devices in 4H-SiC are expected to show several advantages

Table 1.1: Physical properties of GaN, AlN, SiC and most common other semiconductor materials.

Properties	GaN	AlN	SiC			Si	GaAs
			4H	6H	3C		
Crystal structure	WZ	WZ	4H	6H	ZB	Dia.	ZB
Lattice constant [Å]	3.189^a 5.186^c	3.112^a 4.982^c	3.081^a 10.05^c	3.081^a 15.12^c	4.36	5.43	5.65
Band structure	D.	D.	I.D.	I.D.	I.D.	I.D.	D.
Bandgap [eV]	3.42	6.0	3.26	3.02	2.3	1.12	1.42
Electron mobility [cm^2/Vs]	900	400	$1000^{\perp c}$ $1200^{/\!/c}$	$450^{\perp c}$ $100^{/\!/c}$	1000	1500	8500
Hole mobility [cm^2/Vs]	20	14	100	50	50	450	400
Electron saturation velocity [10^7 cm/s]	2.7	1.9	2.2	1.9	2.7	1	1
Breakdown field [MV/cm]	3.3	1.5	3	3	2	0.3	0.4
Thermal conductivity [W/cmK]	1.3	2.9	4.9	4.9	4.9	1.5	0.46
Relative dielectric constant	$9.5^{\perp c}$ $10.4^{/\!/c}$	8.5*	$9.7^{\perp c}$ $10.2^{/\!/c}$	$9.7^{\perp c}$ $10.2^{/\!/c}$	10	11.9	12.8
Conductivity control	△	△	◯	◯	△	◯	◯
Thermal oxide	×	×	◯	◯	◯	◯	×
Conductive wafer	△ (SiC)	△ (SiC)	◯	◯	△ (Si)	◯	◯
Insulating wafer	△ (Sap.)	△ (Sap.)	◯	◯	×	△ (SOI)	△

WZ: Wurtzite ZB: Zincblende Dia.: Diamond
D.: Direct I.D.: Indirect
◯: Excellent △: Fair ×: Difficult
Sap.: Sapphire SOI: Silicon on insulator
*The data of anisotropy reported are uncertain.

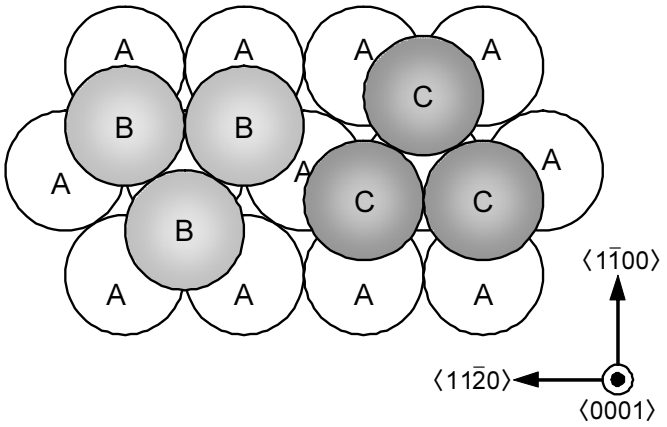


Figure 1.1: Hexagonal close packing of Si–C pairs.

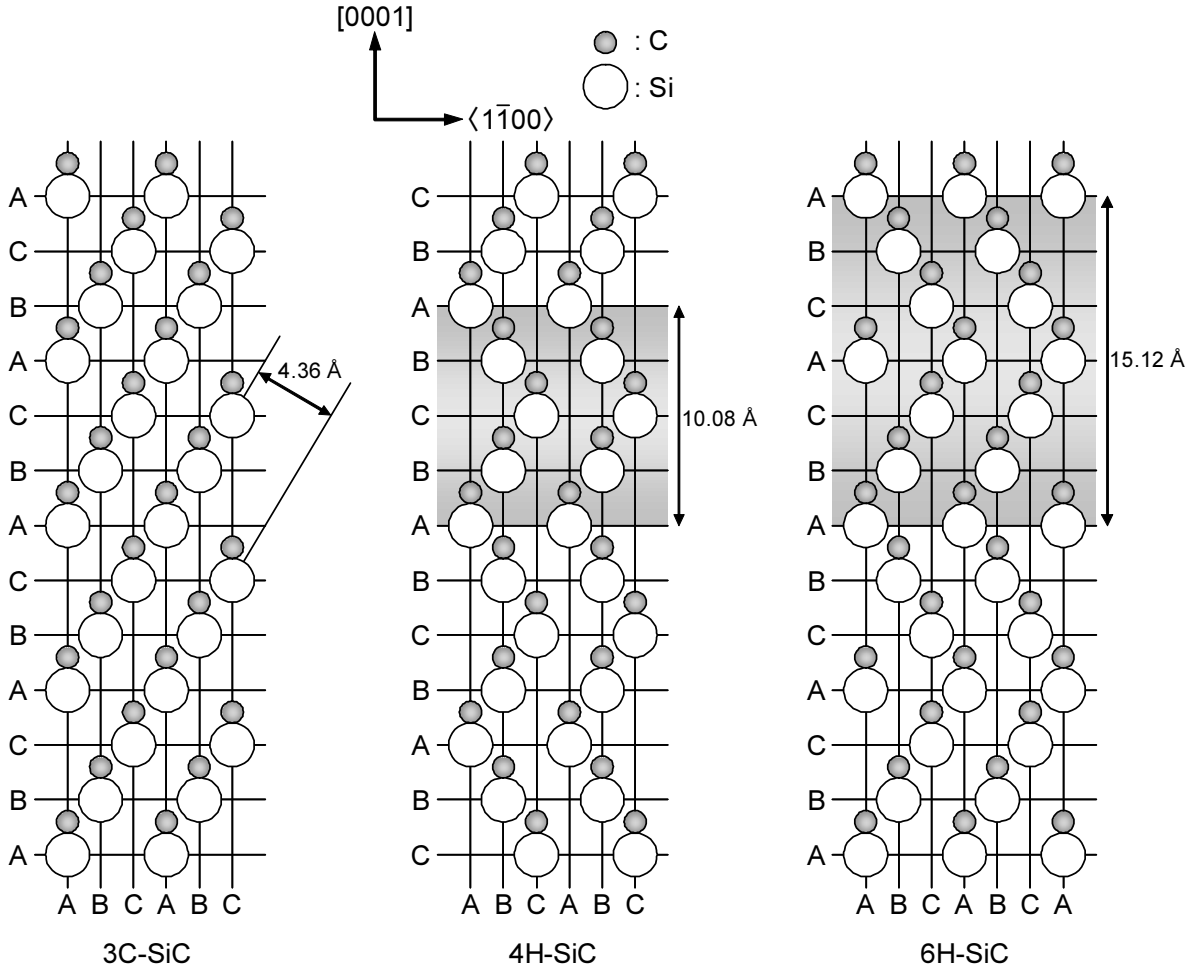


Figure 1.2: Stacking orders along *c*-axis for 3C, 4H, and 6H. Open and closed circles represent Si and C atoms, respectively.

compared to those fabricated by Si and GaAs, as discussed in the following subsection. Although the research on SiC was limited because of the absence of high quality crystals, it has been accelerated after the two technological breakthroughs in crystal growth in 1980 s. The first one was the development of a large-area bulk growth technique called "seeded sublimation" or "modified Lely method" [2]. This method has become a standard technique to grow high-quality and large-area 4H- and 6H-SiC bulk crystals through the optimization of furnace design and thermal distribution during growth. The size of commercially available 4H- and 6H-SiC wafers is 3 inch to 4 inch in diameter, and both low resistivity (about 0.015 Ωcm) and semi-insulating (over 10^5 Ωcm) wafers are commercially available with high-quality (threading dislocation (TD) density is $\leq 10^4$ cm^{-2}). Furthermore, development of 6 inch (150 mm) wafer was demonstrated in 2010 [3].

The second breakthrough was the successful development of epitaxial growth on off-oriented 6H-SiC (0001) substrates by chemical vapor deposition (CVD) [4]. This technique is called "step-controlled epitaxy", and its growth mechanism has been discussed in detail [5, 6]. By using step-controlled epitaxy concepts, device-quality epitaxial layers of 4H- and 6H-SiC can be obtained without any inclusions of other polytypes at growth temperatures of about 1500°C, which are over 300°C lower than previous methods. Both n- and p-type doping can be controlled in a wide range (10^{14}–10^{19} cm^{-3}) by introducing N_2 for n-type and trimethylaluminum (TMA: $Al(CH_3)_3$) for p-type.

These two breakthroughs allowed us to develop the SiC-based power devices. In 1995, the first 1750 V Schottky barrier diodes (SBD) in SiC were demonstrated on the epilayer grown by step-controlled epitaxy [7]. The SiC SBDs showed very low ON-resistance far below Si unipolar limit. Subsequently, research on any kinds of diodes and transistors has been accelerated. 600 V-, 1200 V-class SBDs are now commercially available [7, 8], and intensive effort has been devoted to PiN diodes for over 5 kV application. 3-terminal transistors such as JFETs, MOSFETs, and BJTs are also studied for middle voltage (< 10 kV) application, and gate turn-off thyristors (GTOs) and IGBTs are also under development for ultra-high voltage (> 10 kV) application. The details will be discussed in the next section.

1.2.2 Current Status of SiC Power Devices and Their Applications

In power devices, breakdown voltage is one of the key parameters since they must stand high voltage operation without failure. When we assume the simple case of an abrupt one-dimensional junction in a uniformly doped semiconductor, the breakdown voltage V_B is represented as the area of triangle shown in Fig. 1.3 and is described as:

$$V_B = \frac{E_B W_M}{2}, \tag{1.1}$$

where E_B is the breakdown electric field and W_M the maximum width of depletion region. At the breakdown, the maximum depletion width is given by:

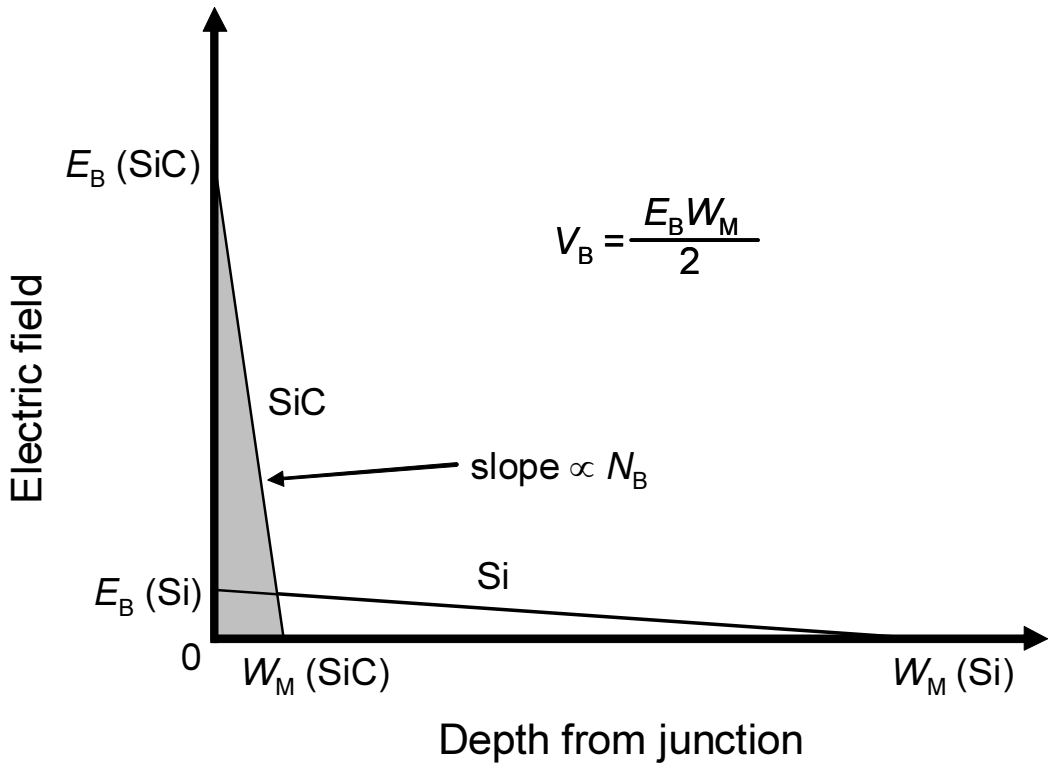


Figure 1.3: Distribution of electric field for Si and SiC abrupt one-dimensional junction at breakdown.

$$W_{\mathrm{M}} = \frac{\varepsilon_{\mathrm{S}} E_{\mathrm{B}}}{e N_{\mathrm{B}}}\,, \tag{1.2}$$

where ε_{S} is the permittivity of the semiconductor, e the elementary charge, and N_{B} the doping concentration of the semiconductor. From Eq. 1.1 and Eq. 1.2, the breakdown voltage of semiconductor devices is expressed as:

$$V_{\mathrm{B}} = \frac{\varepsilon_{\mathrm{S}} {E_{\mathrm{B}}}^2}{2 e N_{\mathrm{B}}}\,. \tag{1.3}$$

Equation 1.3 means that a high breakdown electric field and a low doping concentration are required to achieve the high breakdown voltage. Since SiC has a high breakdown electric field (about 3 MV/cm), a significantly higher breakdown voltage can be achieved for SiC with the same doping concentration as for Si.[1]

Another key parameter is ON-resistance which determines ON-state loss in power semiconductor switches. For the forward bias condition (ON-state), the drift region behaves as a resistor in unipolar devices. The drift resistance (R_{Drift}) for unipolar devices can be calculated by [9]:

$$R_{\mathrm{Drift}} = \frac{4 {V_{\mathrm{B}}}^2}{\varepsilon_{\mathrm{S}} \mu {E_{\mathrm{B}}}^3}\,, \tag{1.4}$$

where μ is the carrier mobility in the semiconductor. Equation 1.4 tells that for a given breakdown voltage, the drift resistance is inversely proportional to the carrier mobility and the cube of breakdown field. In the unipolar device with an optimum structure, the drift resistance is the dominant component of the ON-resistance. Thus, a decrease in the drift resistance brings a significant reduction of power losses because a power device handles a large amount of current, resulting in high energy efficiency. Thanks to the high breakdown electric field of SiC, the design of SiC power devices with a thinner and more highly doped voltage-blocking layer can be accepted, resulting in more than 300 times lower drift resistance than Si devices with the same breakdown voltage.

In addition to above mentioned excellent nature of SiC, high thermal conductivity of SiC contributes to the quick elimination of heat produced by power losses, making it more durable against higher power losses from high current or high-frequency switching. Furthermore, SiC devices can operate at much higher temperature than Si and GaAs devices, owing to the wide bandgap and high thermal stability of SiC. Therefore, SiC is expected to realize much higher energy efficiency and much wider operating range than ever achieved with Si and GaAs, as shown in Fig. 1.4.

[1] Similarly, a higher doping can be utilized for SiC for the same breakdown voltage, resulting in the reduced ON-resistance.

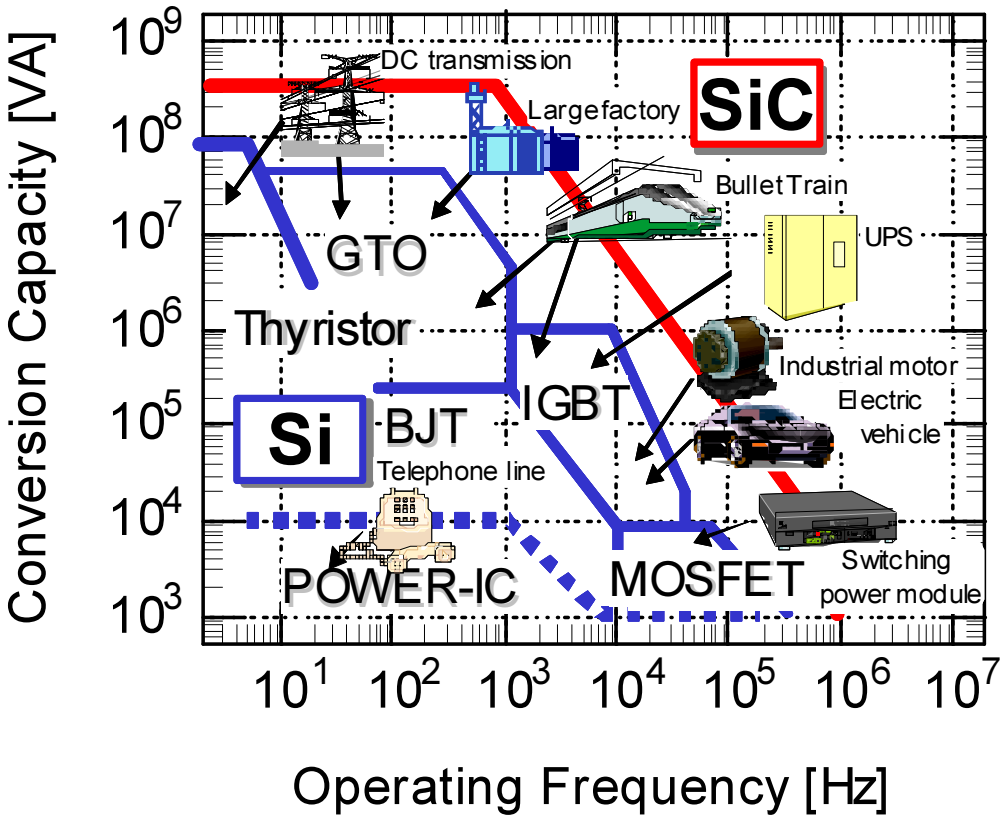


Figure 1.4: Possible range of operation for Si and SiC power devices.

SiC Power Diodes

In Si power diodes, SBDs (unipolar diode) are widely used for 0 – 200 V applications. For high voltage application like 200 V – 6600 V, Si PiN diodes (bipolar diode) can be a better option since bipolar devices can show the lower ON-resistance due to the effect of so called conductivity modulation (Fig. 1.5). During the operation of PiN diodes, minority carriers are injected to the lightly-doped drift region and exceed its impurity concentration. As a result, to meet the neutrality, majority carriers are also injected to the drift region therefore conductivity is modulated, resulting in the low resistance. One of the drawbacks of bipolar diode is slow switching speed since it deals with minority carries, resulting in the large power switching loss. Accordingly, Si PiN diodes are used for high voltage applications where the low ON-resistance is more important than the switching loss, as shown in Fig. 1.6.

In contrast to Si diodes, SiC SBDs can be used for 0 – 5 kV application, and PiN diodes can be used for 5 – 20 kV applications thanks to the excellent properties and thereby wider voltage rating of SiC devices. In the last decade, marked progress has been made in SiC technology for manufacturing power devices, and intensive studies on fundamentals of SiC SBDs [10] as well as on such practical issues as reliability [11] and scaling-up [12] have led to commercial production of 600 V- and 1.2 kV-class 4H-SiC SBDs [7, 8]. The superior switching behavior in SBDs (without reverse recovery observed in PiN diodes) and the simplification of the cooling system (due to lower switching loss for SBDs and higher thermal endurance of SiC devices) make them attractive for power modules needing power rectifiers.

SiC Power Transistors

While the first commercially available SiC power devices were SBDs, SiC power "switching" devices have also been investigated extensively. In Si power transistors, BJTs and GTOs were previously used for both low and high voltage switching, but later they are replaced with MOSFETs and IGBTs due to their superior performance such as fast switching and voltage-controlled, simple gate-drive circuits.

When it comes to SiC power transistors, IGBTs (or GTOs) cannot always be a good option since they need an additional voltage drop ($\sim$ 2.7 V) caused by a built-in potential of *pn* junction, making them less attractive. Their application is limited to ultra-high voltage ($>$ 10 kV) range used for electric power supply or advanced electric grid.

Looking at low ($<$ 1.2 kV), middle (1.5–3 kV), and high voltage ($>$ 5 kV) range, where the Si power transistors are developed, not only SiC MOSFETs but also SiC JFETs and SiC BJTs seem to be a good choice. From the historical point of view, SiC MOSFETs seem to be an natural choice to replace Si MOSFETs. However, due to the poor quality of SiO_2/SiC interface in SiC MOSFETs, they were suffering from their low channel mobility and oxide unreliability. In response to this, the first developed transistor in SiC was JFET. JFETs do not require the gate oxide so that they are free from such gate oxide related

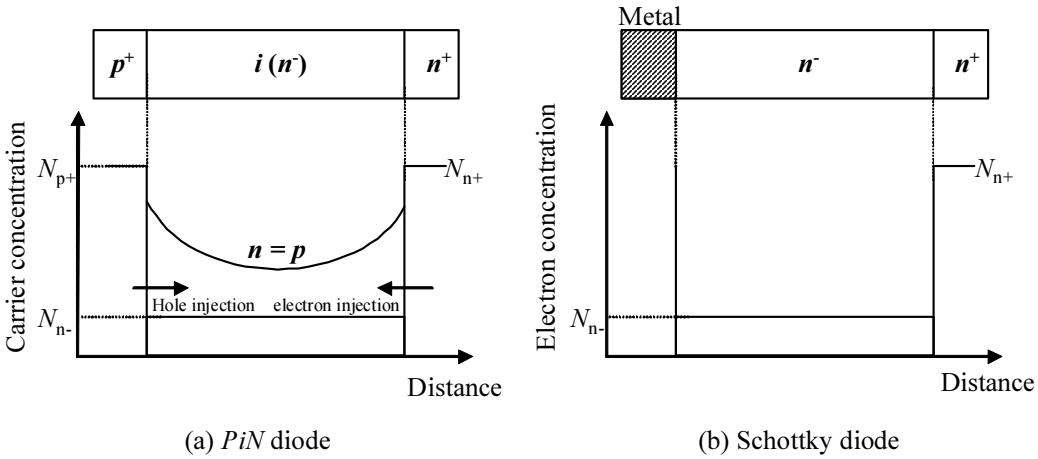


Figure 1.5: Carrier distribution profiles in (a) PiN diode and (b) Schottky barrier diode under forward bias condition.

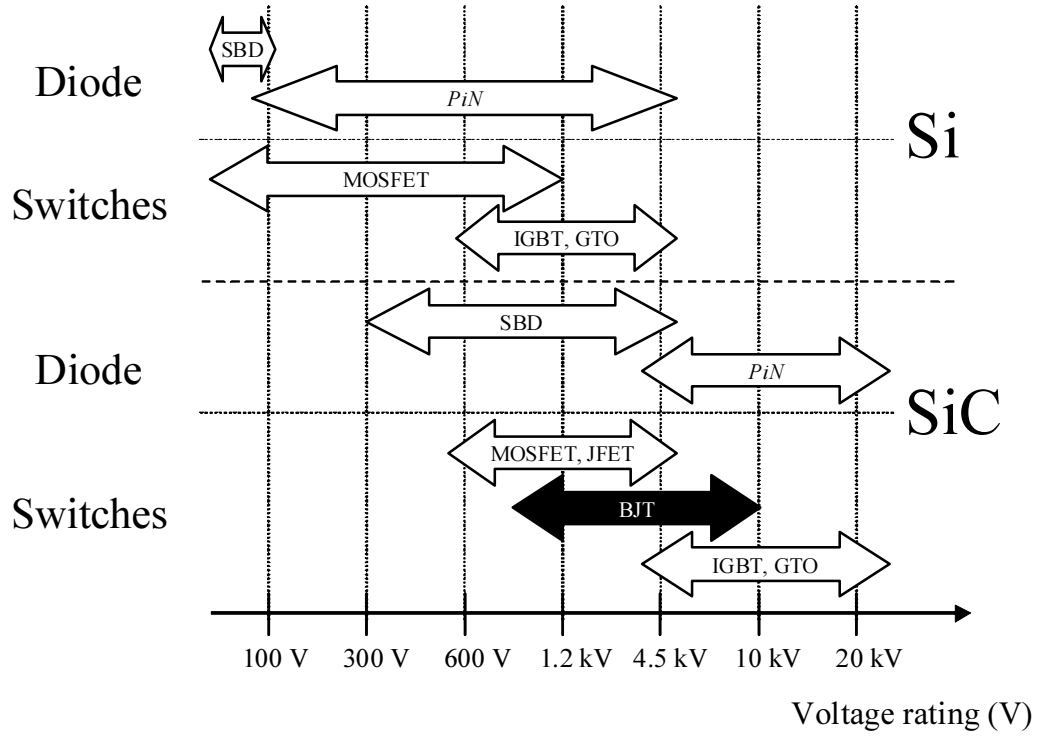


Figure 1.6: Voltage rating of Si and SiC power devices.

problems as low channel mobility and oxide unreliability. One of the drawbacks of JFET is, however, normally-ON nature so that it requires additional complicate process to achieve normally-OFF operation. Taking into account such problems in making high performance MOSFETs or normally OFF JFETs, SiC BJTs have become more attractive candidates for power switching devices. The details will be described in the following section.

1.3 SiC BJTs and Beyond: Ⅲ-N/SiC HBTs

1.3.1 Advantages of SiC-Based Bipolar Transistors

As described in the previous section, SiC BJTs are now recognized as attractive device structure to overcome the drawbacks of MOSFETs or JFETs. BJTs are normally OFF devices, and free from such oxide-related problems as low channel mobility and oxide-reliability issues. SiC power BJTs were first reported in the early 2000 s [13, 14] and in the past 10 years, intensive efforts have been devoted to obtaining high performance BJTs. Fig. 1.7 illustrates the ON-resistance as a function of breakdown voltage reported so far [14–29], and now we can get high performance BJTs close to the SiC unipolar limit in a wide range of voltages. Attractive characteristics such as fast switching, low voltage drop BJTs have also been demonstrated [28, 29]. Although Si BJTs were replaced with Si MOSFETs or Si IGBTs because of their narrow safe operating area, SiC BJTs show no 2nd breakdown; therefore a large safe operating area can be obtained [30]. Unlike MOSFETs, BJTs are gate-oxide free so that high temperature operation is easier. Furthermore, degradation-free BJTs on low basal plane dislocation substrates have been demonstrated [31]. Therefore, high performance and robust BJTs are now available. The target of SiC BJTs are ranging from (1) low voltage (notably 1.2 kV) application such as inverters for hybrid/electric vehicle (HEV/EV) and solar cells to (2) middle voltage (notably 1.7/3.3 kV) application like train inverters or (3) high voltage ($\sim$ 5 kV or higher) for industrial motor application (Table 1.2). In these applications, Si inverter modules based on Si PiN diodes and Si IGBTs are commonly used (an example with HV is illustrated in Fig. 1.8). If high performance SiC BJTs combined with SiC SBDs can replace them, high efficiency can be expected so that high fuel or energy efficient drive can be realized. In addition, low power loss operation or capability of high temperature operation make it enable to replace the bulky water cooling system with small air cooling. Thus, power modules with SiC BJTs can provide spacious, energy-friendly system.

1.3.2 Key Issues in SiC BJTs: How To Improve Current Gain ?

As described in the previous section, SiC BJTs are very attractive candidates for high-power switching devices because of such characteristics as high breakdown voltage, low ON-resistance, and high current density. The first SiC power BJT showed the performance

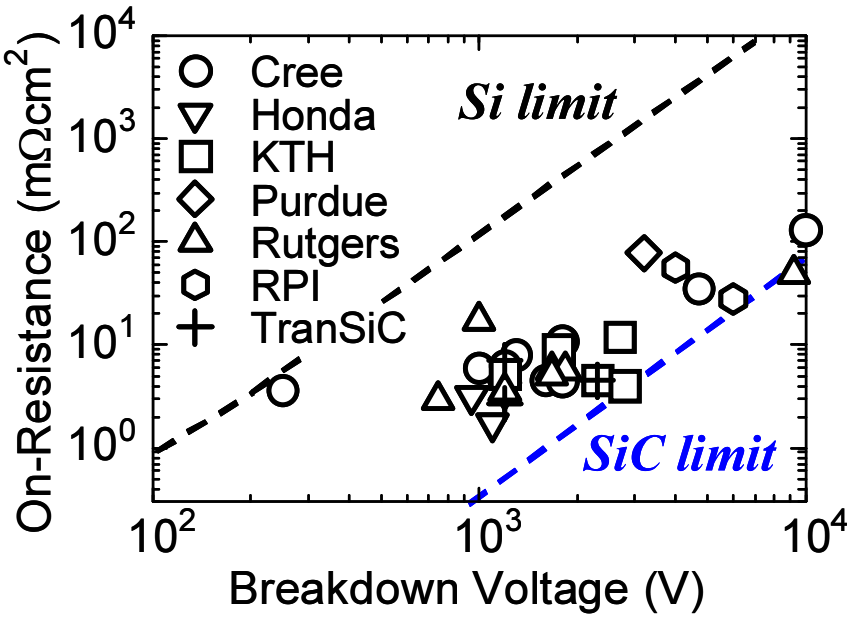


Figure 1.7: Relationship between breakdown voltage and ON-resistance for major vertical 4H-SiC BJTs reported so far [14–29]. Dashed line denotes theoretical performance of either Si or SiC unipolar device, which are predicted by material properties.

Table 1.2: Major application of SiC power devices and their possible device structure based on voltage rating.

Voltage Range	Voltage Rating	Major Application	Possible Device
Low	600/1200 V	AC, Solar Cells, HEV, EV	MOS or BJT
Middle	1700/3300 V	Train Inverter	MOS or BJT
High	$>$ 5000 V	Infra, Industrial Motor	BJT
Ultra-high	$>$ 10000 V	Electric Power Supply / Grid	IGBT or GTO

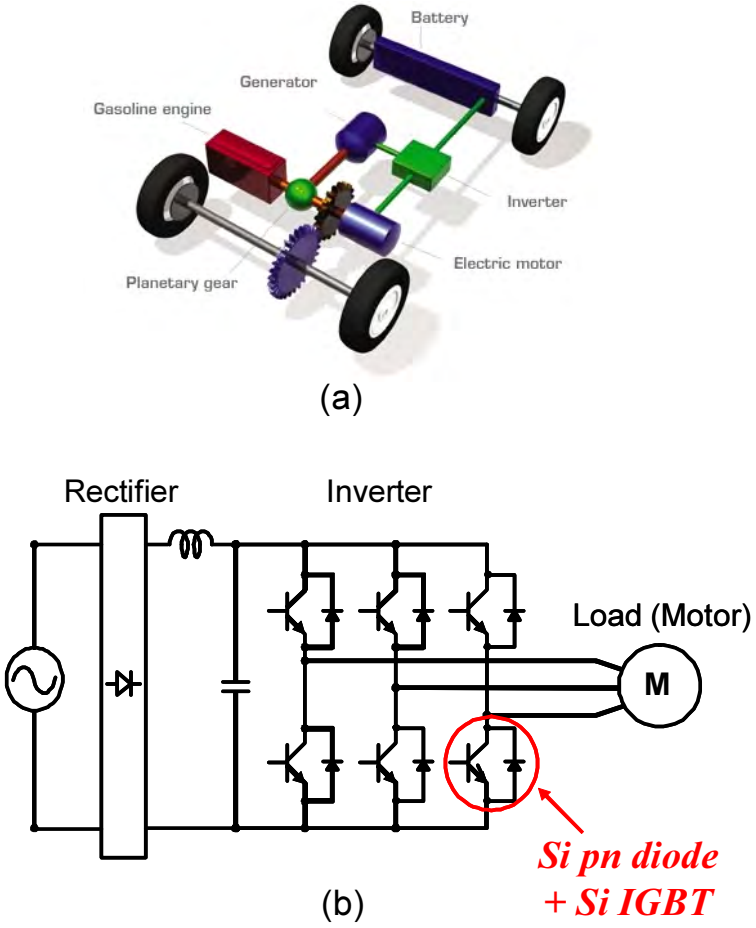


Figure 1.8: An application example of Si power module based on Si PiN diodes and Si IGBTs.

of 1800 V, 10.8 mΩcm^2 [14]. Following study on improving their performance has made it possible to approach theoretical limit of SiC. As shown in Fig. 1.7, low ON-resistance, high voltage BJTs in a wide range of voltages have been realized. For instance, 1100 V, 1.7 mΩcm^2 [17], 2800 V, 4.0 mΩcm^2 [23], and 9200 V, 49 mΩcm^2 [21] BJTs are already demonstrated. The results of reported BJTs are summarized in Table 1.3.

On the other hand, since BJTs are current-controlled devices, a high current gain, which determines the input current necessary to operate them, is required for the practical application to minimize the losses in the drive circuits. However, SiC BJTs have been suffering from their low current gain, resulting in large power dissipation at the base drive circuit. For practical application, the requirement for the current gain is 100 at operation temperature. So far the current gain is typically in the range of 60–70 at room temperature [16, 25, 26], and only a few groups have achieved current gains in the range of 110–134 [17, 19]. In addition, it falls off to about 50 at 250°C since BJTs show negative temperature coefficient of current gain due to the reduced emitter injection efficiency caused by the activation of base impurities at high temperature. Thus, a current gain of 200 at room temperature that gives rise to a current gain of 100 at 250°C is desired, which is illustrated in Fig. 1.9

For the reasons of the low current gain, previous reports pointed out the possibility of implantation defects [15, 18], surface recombination [15, 17, 32], and interface recombination [15, 16, 25]. For example, reduced implantation [18] and optimization of emitter-base spacing [15, 18] have been proposed to avoid recombination at the implantation defects. And surface passivation technique based on thermal oxidation [15, 17] or deposited oxide passivation [32, 33] has been proposed to suppress the surface recombination. In addition, continuous epitaxy from the base to emitter was suggested to minimize the interface recombination [15, 16, 25]. However, regardless of minimization of these recombination currents, the current gain still lies around 100. Therefore, ultimate reduction of those recombination current is necessary to achieve higher current gain. In addition, we assume that a 4th factor, bulk recombination, plays an important role in limiting the current gain because SiC has short lifetime regardless of its indirect band structure.

1.3.3 Ⅲ-N/SiC HBTs as Next-Generation Power Switches

Another approach for achieving high current gain in SiC BJTs is to introduce a hetero-emitter as a wide bandgap emitter. This device structure is so called heterojunction bipolar transistor (HBT) [34], which made great success for high-frequence power amplifier using AlGaAs/GaAs, InP/GaAs, or SiGe/Si heterojunction. When the wide bandgap material is utilized as an emitter, it makes a band offset at the emitter/base interface, so that the current flow from the base to emitter is prevented as shown in Fig. 1.10. As a result, current gain is exponentially improved:

$$\beta = \frac{J_\mathrm{n}}{J_\mathrm{p}} \propto \frac{\exp(\Delta E_\mathrm{c}/kT)}{\exp(\Delta E_\mathrm{v}/kT)} \propto \exp(\frac{\Delta E_\mathrm{c} - \Delta E_\mathrm{v}}{kT}) \propto \exp(\frac{\Delta E_\mathrm{g}}{kT}). \tag{1.5}$$

Table 1.3: Review of major SiC BJTs reported so far [14–19, 21–29].

Published Year	Institute	Gain	V_{CEO} (V)	R_{ON} (mΩcm^2)
2001	Cree	20	1800	10.8
2005	Cree	40	1000	6
2008	Cree	70	1200	6.3
2008	Cree	110	250	3.6
2010	Cree	28	10000	130
2002	Purdue	15	3200	78
2003	Purdue	55	500	26
2005	RPI	9	4000	56
2007	RPI	3	6000	28
2003	Rutgers	32	1000	17
2004	Rutgers	7	9200	49
2006	Rutgers	11	1830	5.7
2008	Rutgers	70	1670	5.1
2011	Rutgers	37	1200	3.5
2005	KTH	64	1100	38
2007	KTH	60	1200	5.2
2008	KTH	42	1750	9
2010	KTH	55	2800	4
2008	TranSiC	50	1200	7
2009	TranSiC	35	2300	4.5
2010	TranSiC	71–83	1200	N/A
2011	TranSiC	117	1200	2.7
2009	Honda	134	950	3.2
2009	Honda	145-135	1100-1200	1.7–3.5

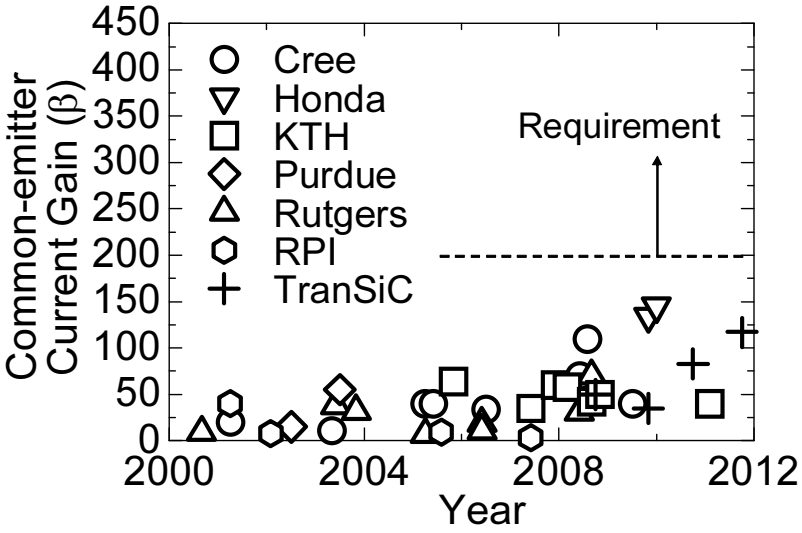


Figure 1.9: Room temperature current gain of 4H-SiC BJTs reported in the past 10 years. For practical application, current gain of 200 at room temperature is required.

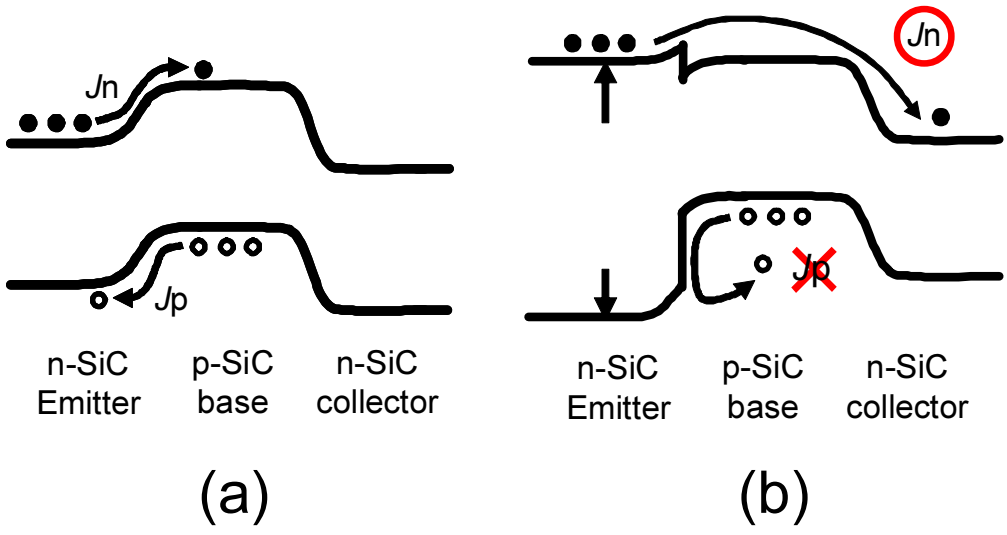


Figure 1.10: Band diagram and concept of BJT and HBTs.

Therefore, SiC HBT can be expected as an ultimate alternative device structure to improve the current gain.[2] Since it is impossible to grow Si_xC_{1-x} solid solutions with x near 0.5, SiC-based HBTs cannot be fabricated within group-IV semiconductors. Heteroepitaxial growth of wider bandgap group-Ⅲ nitride on SiC is one possible way to achieve bandgap engineering in SiC devices.

Properties of Ⅲ-Nitrides

Group-Ⅲ nitrides (InN, GaN and AlN) are Ⅲ-V compound semiconductors composed of tetrahedrally bonded cation and anion atoms in a closed-packed structure as the case of SiC. All three binaries and their alloys crystallize in both wurtzite (2H) and zincblende (3C) structures, where the wurtzite structure (shown in Fig. 1.11) is thermodynamically more stable [35]. The physical properties of GaN and AlN are listed in Table 1.1. Since these compounds show direct band structure and their alloy can cover continuously from 0.7 eV (the bandgap of wurtzite InN) to 6.0 eV (the bandgap of wurtzite AlN), they have attracted much attention as the candidates for light-emitting devices [36] (Fig. 1.12). Although the research on GaN and related alloys was limited because of the absence of high quality crystals, it has been accelerated after technological breakthroughs in the late 1980 s where Amano *et al.* succeeded in growth of high-quality GaN with low-temperature AlN buffer layers [37] and realization of p-GaN by low-energy electron beam irradiation [38]. In response to this, blue/green LEDs and violet-blue LDs were developed and commercialized in the 1990 s [39–42]. At the same time, GaN has been also recognized as a promising candidate for high power, high frequency devices since GaN has wide bandgap, high breakdown field, and high saturation velocity. GaN-based MOSFETs and high electron mobility transistors (HEMTs) have been considerably studied.

One of the present issues in Ⅲ-N is the lack of large single crystals. Although the 2–4 inch GaN wafers with a threading dislocation (TD) density of 10^4–10^6 cm^{-2} are demonstrated [43, 44], they are still costly and small to produce large number of devices. Instead, heteroepitaxy on foreign substrates such as sapphire, Si, and SiC is widely used. The recent GaN growth technique of epitaxial lateral overgrowth (ELO) [45, 46] or high temperature buffer layer made it possible to obtain reasonably high quality crystal (TD density of 10^7–10^8 cm^{-2}). Among these foreign substrates, SiC is one of the best candidates for high-quality Ⅲ-N growth because of the relatively small lattice mismatch between Ⅲ-N and SiC ($\Delta a \sim 0.9$–3 % as shown in Fig. 1.12). GaN-based both electronic and optical devices on SiC show superior performance compared with those on Si or sapphire due to high crystal quality. In other words, SiC is expected as a promising candidate for Ⅲ-N epitaxy, which motivates us to make a device using the Ⅲ-N/SiC heterojunction: Ⅲ-N/SiC HBTs.

[2] This feature enables us to keep high current gain even if very high base doping is employed to reduce the base access resistance for radio-frequency (RF) application. Thus, high current gain as well as high frequency performance can be achieved using HBT strctures, which is one of the major reason that HBTs made great success in RF-power application.

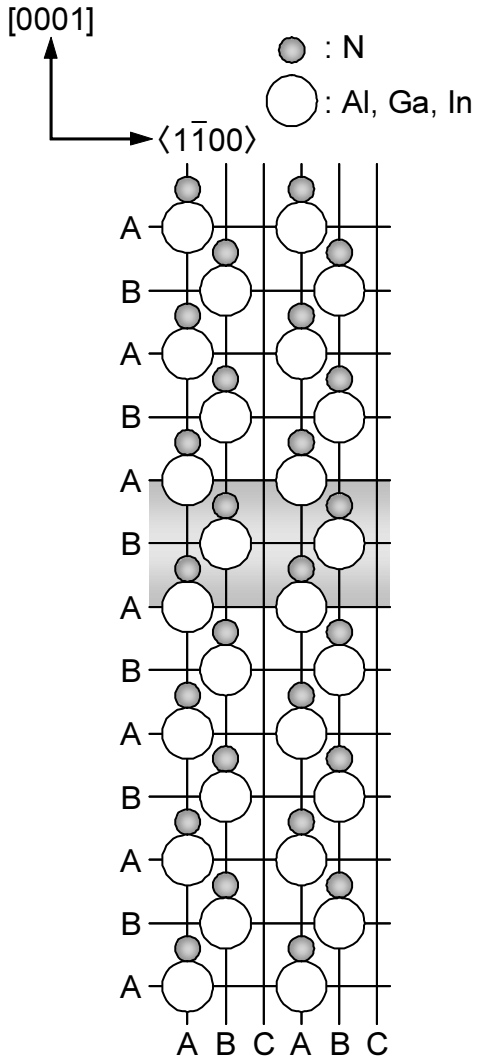
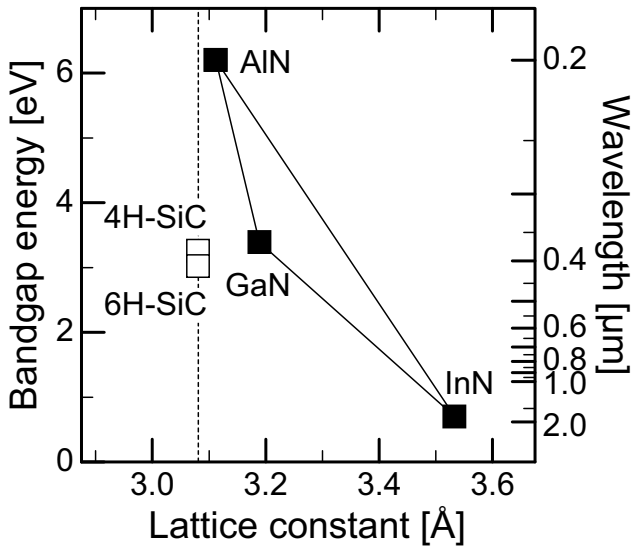
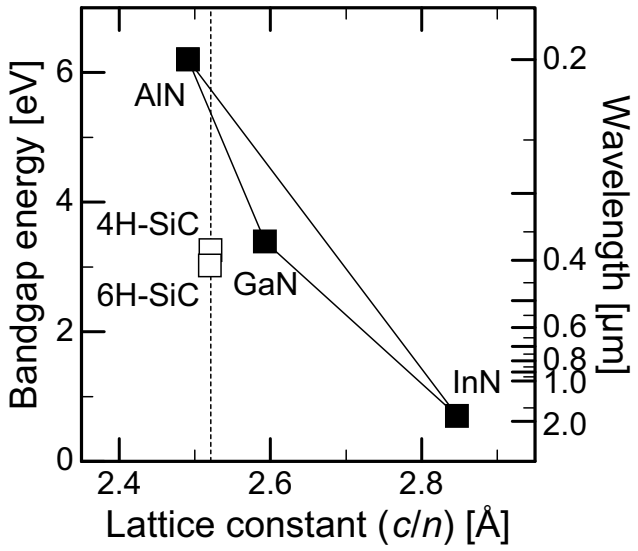


Figure 1.11: Stacking orders along *c*-axis for 2H-Ⅲ-N (Ⅲ: Al, Ga, In). Open and closed circles represent Ⅲ and N atoms, respectively.



(a) a-axis



(b) c-axis

Figure 1.12: Relationships between bandgap and (a) a-axis / (b) c-axis lattice constant for hexagonal group–Ⅲ nitrides (Ⅲ–Ns) and SiC. The dashed lines show the lattice constants of 4H-SiC.

Key Issues in Ⅲ-N/SiC HBTs

Fabrication of GaN/SiC HBTs was first reported by Pankove *et al.* in 1994 [47]. They showed extremely high current gain of $\alpha \sim 0.99999$ at room temperature and $\alpha \sim 0.99$ at high temperature of 535°C in common-base configuration, so that the results seemed promising [48]. However, no groups could reproduce the common-base results, and so far only a few reports are available on GaN/SiC HBTs only in common-base configuration [49, 50]. In addition, it turned out that the promising results could not be easily reproduced [51]. After all, although there are large number of reports on GaN/SiC heterojunction diodes in response to the first demonstration of GaN/SiC HBTs [52–57], common-emitter operation has not been achieved in the HBTs, and focused research on n-GaN/p-SiC emitter junctions is necessary to achieve common-emitter-mode operation in the HBTs.

The key issue in achieving high performance Ⅲ-N/SiC HBT is how to control the interface properties of the heterojunction. To begin with, there is a lattice mismatch and polytype mismatch between SiC and Ⅲ-N materials, so that there is a possibility of defect formation at the heterojunction. Since such defects can work as traps of electrons, epitaxial growth of Ⅲ-N on SiC especially focusing on the initial growth stage should be developed to minimize the generation of such defects. In addition, in the case of AlGaN/SiC heterojunction, where the materials with different valency (SiC: Ⅳ-Ⅳ, Ⅲ-N: Ⅲ-Ⅳ) form the heterojunction (referred to as *heterovalent heterojunction*), there are electron-excess and electron-deficient bonds at the interface, e.g. Si-N or Al(Ga)-C, which form donor or acceptor states, reducing the emitter injection efficiency. Thus, detail investigation on the heterojunction as well as the atomic control of the heterointerface is required. Furthermore, the band offset control of Ⅲ-N/SiC heterojunction has to be investigated since it plays an important role in determining the carrier transport. Although there have been some reports on the band offset of GaN/SiC, the reports are still limited so that it should be intensively investigated.

1.4 Aim of This Study and Outline of This Thesis

In this thesis, both SiC BJTs and Ⅲ-N/SiC HBTs are intensively investigated toward advanced high-power and low-loss switching applications. To realize high performance BJTs and HBTs, we concentrate on the improvement of current gain that is one of the critical parameters determining the power loss in bipolar transistors. To achieve high current gain, we investigate from the design to growth, device processing and characterization of SiC BJTs. In addition, to overcome the potential limitation of current gain in BJTs, an alternative structure, Ⅲ-N/SiC HBTs, are proposed as next-generation power switches. To develop high-current-gain HBTs, we investigate the growth of Ⅲ-N on SiC as well as the control of electronic properties of Ⅲ-N/SiC heterojunction. We also develop the fabrication process of Ⅲ-N/SiC HBTs. With these efforts, much improved current gain is demonstrated.

In chapter 2, chemical vapor deposition (CVD) and molecular beam epitaxy (MBE) system, which are used for SiC and Ⅲ-N epitaxy and play an important role in determining the performance of BJTs and HBTs, are described. From the system configuration to the detail growth procedure established in this study are presented.

In chapter 3, development of high-current-gain SiC BJTs is presented. To improve the current gain in SiC BJTs, three techniques, surface passivation to suppress the surface recombination, continuous epitaxy to reduce the interface recombination, and deep-level-reduction process to enhance the lifetime of p-SiC base layer, as well as appropriate design of the BJTs will be discussed. With optimized design and processing, a record-breaking current gain in SiC BJTs is demonstrated. A first operation of SiC BJTs on $(000\bar{1})$C-face with highest current gain to date is also presented. Moreover, BJTs with a record blocking voltage among SiC switching devices to date is also reported.

In chapter 4, growth and characterization of GaN/SiC HBTs are presented. Crystal quality of GaN heteroepitaxially grown on SiC off-axis surface is characterized. Then, the band alignment and current transport of GaN/SiC heterojunction with different base doping followed by their impact on GaN/SiC HBT performance are discussed. In addition, effect of ultrathin AlN spacer layer between GaN and SiC as well as N* pre-irradiation prior to the GaN growth is also presented to improve the electronic properties of GaN/SiC heterojunction. We present an improved rectifying behavior in GaN/SiC heterojunction diodes as well as an improved current gain in GaN/SiC HBTs.

In chapter 5, growth and characterization of AlGaN/SiC HBTs are presented. To obtain better electronic properties in Ⅲ-N/SiC heterojunction, growth of AlN/GaN short-period superlattice (SPSL) is proposed, and its crystal quality is evaluated. Subsequently, impact of AlN/GaN SPSL with various Al compositions on the band offset and current transport of Ⅲ-N/SiC heterojunction as well as the performance of Ⅲ-N/SiC HBTs are presented. We demonstrate the successful band offset control of AlGaN/SiC heterojunction and the first common-emitter-mode operation in AlGaN/SiC HBTs. Furthermore, toward further improvement of current gain, atomic control of Ⅲ-N/SiC by Si and C pre-irradiation prior to the Ⅲ-N growth are described.

In chapter 6, conclusions and future outlook are given.

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Chapter 2

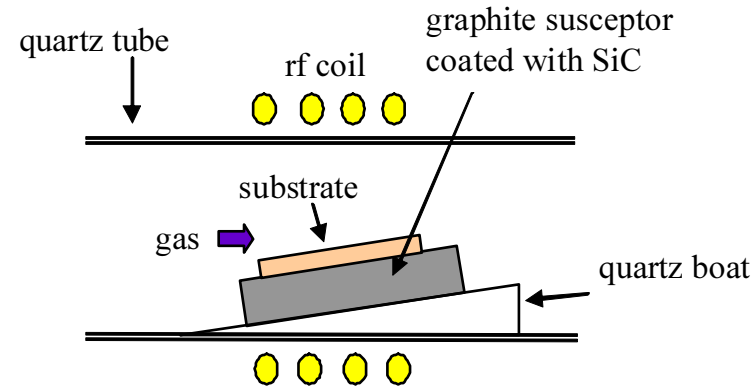
Experimental Details of Crystal Growth

2.1 Introduction

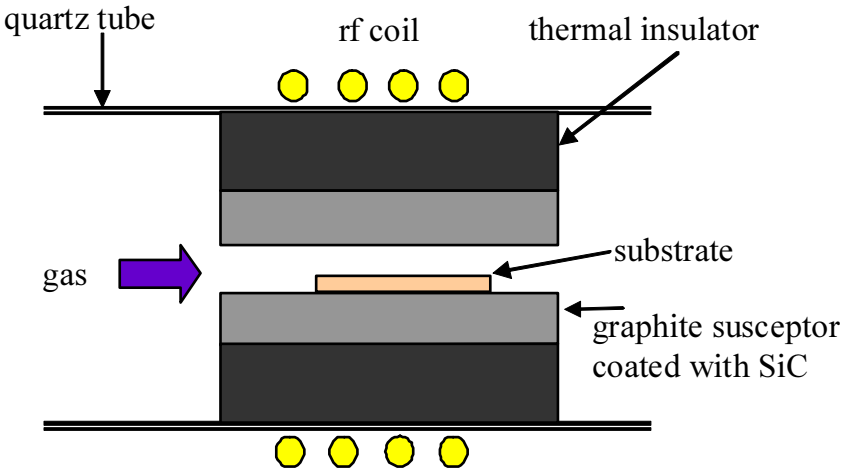
To realize high performance SiC bipolar junction transistors (BJTs) and Ⅲ-N heterojunction bipolar transistors (HBTs), crystal growth of the epilayer is a crucial step to determine the performance since the devices are fabricated on the epilayer. Currently, chemical vapor deposition (CVD) is mainly used to obtain high quality epilayer with good uniformity for SiC epitaxy. In contrast, either CVD or molecular-beam epitaxy (MBE) is used for Ⅲ-N epitaxy based on the research objectives. In this study, we employed cold-wall CVD for SiC and plasma-assisted MBE for Ⅲ-N epitaxy. The motivation of using these system, their features, and detailed growth procedure are explained in this chapter.

2.2 Cold-Wall Chemical Vapor Deposition for SiC Epitaxy

To produce SiC devices with high yield and throughput, SiC epilayer used in devices should be grown at reasonably high growth rate with keeping good uniformity of film thickness and doping, as well as good surface morphology. To meet these requirements, CVD system has been developed in the last decades [1]. A CVD growth system is roughly divided into two types, cold-wall CVD and hot-wall CVD. Fig. 2.1 shows schematic illustrations of CVD reactors used for SiC growth. When step-controlled epitaxy was invented, cold-wall CVD was used for SiC epitaxy [2]. It features a simple system, and can produce good uniformity and controllability of impurity doping. The main drawbacks of the cold-wall CVD are its relatively low growth rate and short lifetime of susceptor (limited growth time) due to the high sublimation rate of SiC coated suceptor, caused by large thermal gradients between the susceptors and samples. To overcome these issues, hot-wall CVD which features a susceptor



(a) cold-wall CVD



(b) horizontal hot-wall CVD

Figure 2.1: Schematic illustrations of SiC CVD reactors: (a) cold-wall CVD and (b) hot-wall CVD.

covered with the thermal insulator set inside the quartz tube, has been developed [3–6]. The susceptor can be heated up with minimized temperature increase of the quartz tube owing to the presence of the thermal insulator. Therefore, high temperature CVD (usually 1500–1600°C) can be accomplished with this reactor. In addition, since the source gases and substrates in the gas-flow channel surrounded by the susceptor can be heated efficiently, the thermal gradient between the susceptor and substrates is very small, so that sublimation of the coated SiC can be suppressed, making long-time growth possible. Since source gases are also heated efficiently, they are effectively cracked, and source species take part in the reaction, resulting in high growth rate. Therefore, hot-wall CVD is becoming a mainstream for growth of high-purity and thick SiC epilayers.

When it comes to SiC epitaxy for BJTs and HBTs, relatively thin layer of 0.35–1.2 μm (for base and emitter) and very thin epilayer of 0.05–0.20 μm (for spacer) are required for BJTs and HBTs, respectively. Thus, the precise control of film thickness is important. Although hot-wall CVD is commonly used for SiC epitaxy, the growth rate is typically too high to obtain such a thin epilayer. In addition, due to the existence of thermal insulator which slows down the change of temperature, SiC can be etched by a carrier gas (H_2) during the "slow" cool-down process after growth, making it uncontrollable to get a very thin epilayer. Accordingly, cold-wall CVD reactor, which allows us to grow SiC with relatively low growth rate of 1–2 μm/h and as well as fast cool down, is employed for SiC BJTs and HBTs.

2.2.1 System Configuration

Fig. 2.2 shows a schematic diagram of the CVD system used in this study. Source gases are silane (SiH_4) and propane (C_3H_8), and a carrier gas is H_2 (typical flow rate: 3 slm) purified with a Ag–Pd purifier. The SiH_4 flow rate used in this study is 0.15–0.30 sccm (corresponding growth rate: 1–2 μm/h), and the C/Si ratio defined as the ratio of a triple of the C_3H_8 flow rate to the SiH_4 flow rate is 3. Nitrogen (N_2) was used for n-type doping, and trimethylaluminum (TMA) for p-type. The growth temperature is typically 1500°C. Hydrogen chloride (HCl) was used for surface pretreatment prior to the growth, as described below. The substrates were set on graphite susceptors coated with high-purity polycrystalline SiC, and they were inductively heated by a radio-frequency (RF) generator operating at 150 kHz. The substrate temperature was monitored by an optical pyrometer. The susceptor was inclined by 10° toward the upper stream of gas flow to improve the uniformity of epilayers [7].

2.2.2 High Temperature HCl Gas Etching

Surface pretreatments prior to the growth are important in epitaxial growth to obtain highly uniform epilayer. Generally speaking, as-received, mechanical polished SiC wafers include

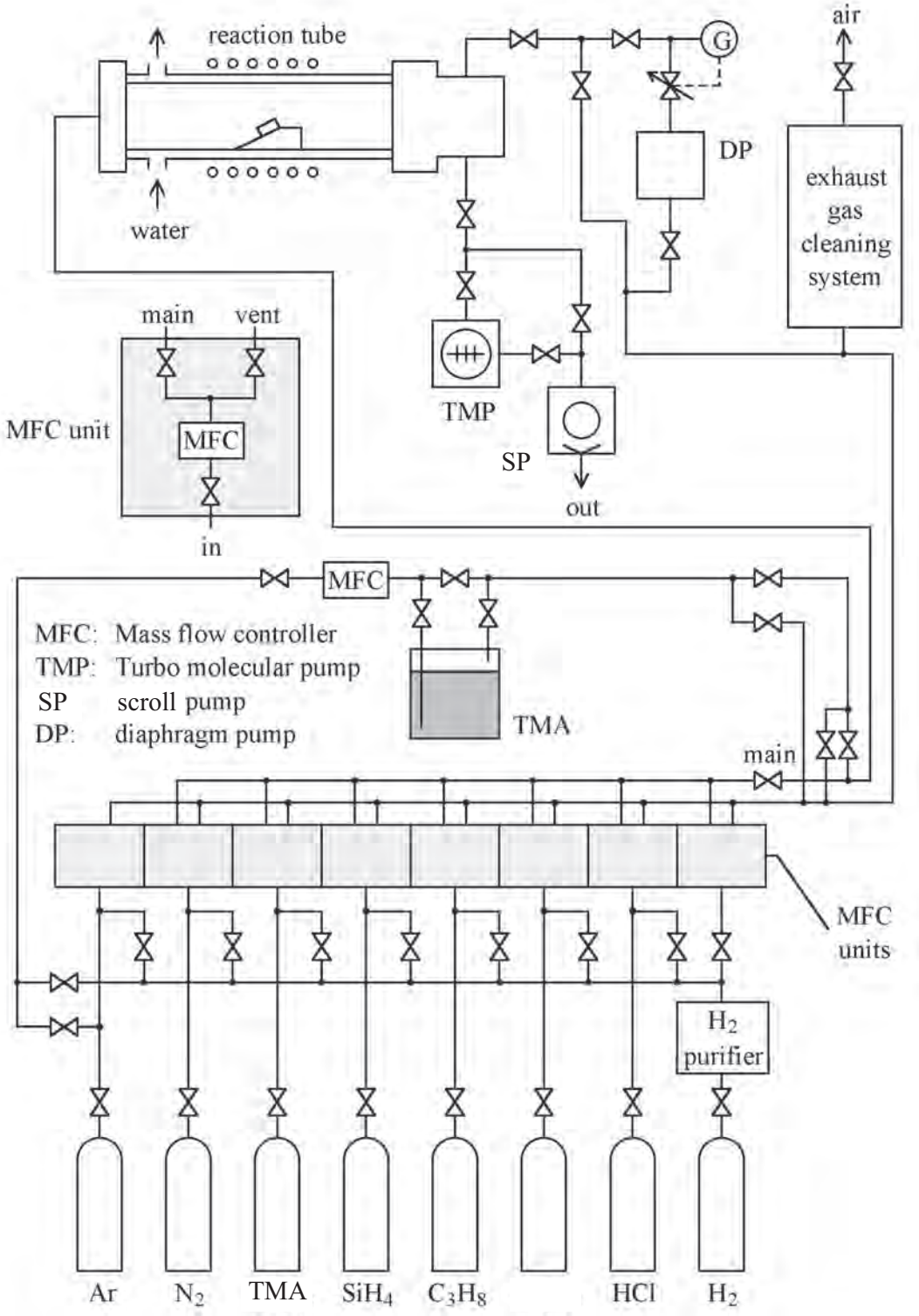
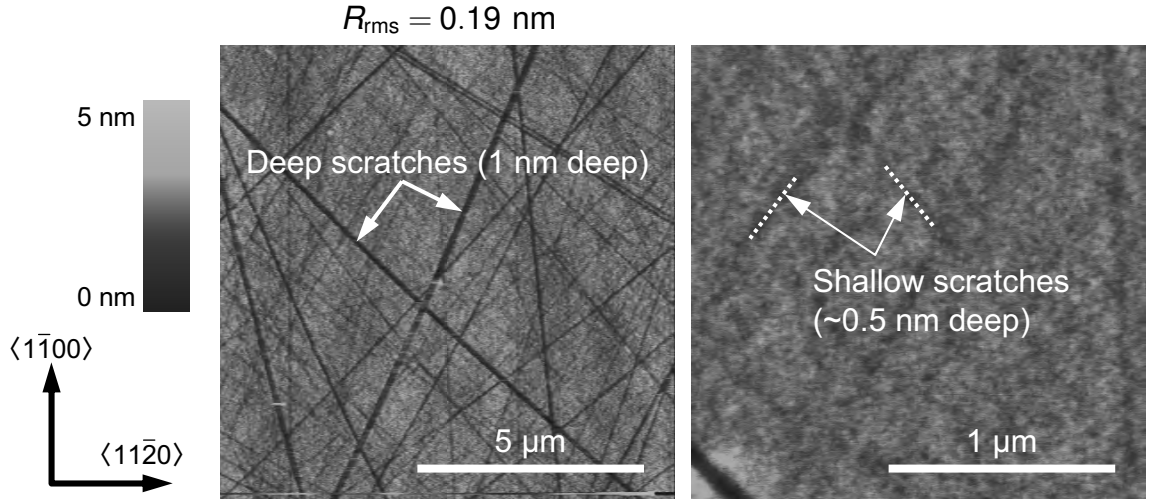


Figure 2.2: Schematic diagram of the cold-wall CVD system used in this study.

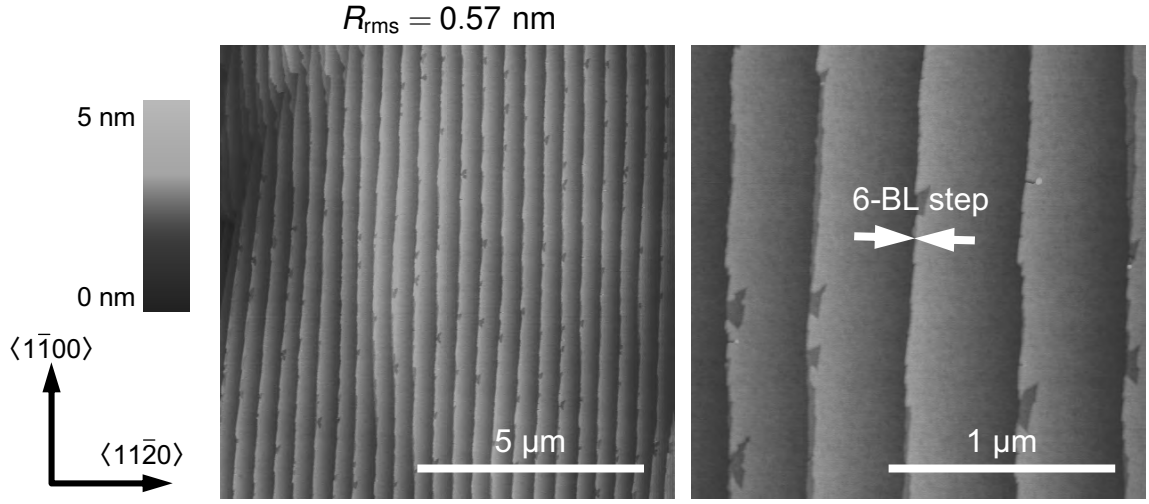
a number of polishing scratches [8] (Fig. 2.3 (a)). To remove these scratches, either HCl-gas etching [9] or H_2-gas etching [10, 11] is reported to be effective as a surface pretreatment without mechanical damage. In this study, gas etching based on the mixture of HCl and H_2 prior to the growth or device processing is employed to etch the SiC surface. In HCl gas etching, H_2 carrier gas etches carbon in SiC and leaves excess Si on SiC surface, which is expected to be taken away by HCl [9]. The samples were put on a SiC-coated graphite susceptor and etched in an HCl/H_2 gas mixture in an induction-heated atmospheric-pressure horizontal cold-wall CVD reactor at 1300°C for 10 min. The flow rates of HCl and H_2 were 3 sccm and 1 slm, respectively, where the concentration of HCl was 0.3%. The temperature program during the HCl gas etching is shown in Fig. 2.4. Fig. 2.3 shows the surface morphologies of 6H-SiC (0001) on-axis substrates before and after the treatments. As shown in Fig. 2.3, the smooth surface morphology with 6-bilayer-height steps was observed [12]. The etching rates of SiC substrates were measured using scanning electron microscopy (SEM), and typical etching rate for the (0001) surfaces was 0.42 μm/h.

2.2.3 Growth Procedure for SiC Epitaxy

Fig. 2.5 shows the growth procedure for atmospheric-pressure CVD. Prior to growth, the substrates are etched with HCl gas etching technique at 1300°C as mentioned in the previous subsection. After the surface pretreatment, the temperature is raised up to the growth temperature (typically 1500°C) with an additional flow of C_3H_8 (0.15 sccm), which contributes to the suppression of SiC etching as well as the suppression of Si droplet formation when the SiH_4 is introduced later. Subsequently, SiH_4 (typically 0.15 sccm) and dopant gas of N_2 or TMA are introduced while supply of HCl is shut down. Both SiH_4 and C_3H_8 flow can be slowly increased up to 0.30 sccm, which corresponds to the growth rate of 2 μm/h. Similarly, when the growth ends, both SiH_4 and dopant gas are cut off followed by cool-down process with supplying C_3H_8 to avoid Si droplet formation. However, this process can cause the growth of thin layer of SiC with extremely high C/Si ratio by residual SiH_4 and C_3H_8. Since this C-rich epi-layer can affect the performance of Ⅲ-N/SiC HBTs where Ⅲ-N/SiC heterojunction is formed on the SiC surface, HCl gas etching was performed once again in the case of HBT processing. A typical secondary ion mass spectroscopy (SIMS) depth profile of the *npn* BJT structure grown with this procedure is shown in Fig. 2.6, which clearly exhibits top n region (N concentration [N]: 1.5×10^{19} cm^{-3}), middle p region ([Al]: 8–9×10^{17} cm^{-3}), and bottom n region ([N]: 8×10^{15} cm^{-3}), indicating a successful formation of abrupt *npn* junctions.



(a) as-mechanical-polished samples



(b) HCl-gas-etched samples following chemical mechanical polishing (CMP)

Figure 2.3: Surface morphologies of 6H-SiC $(0001)_{Si}$: (a) as-mechanical-polished samples and (b) HCl-gas-etched samples following CMP [8, 12]. Each of right figures shows a magnified image of the left one.

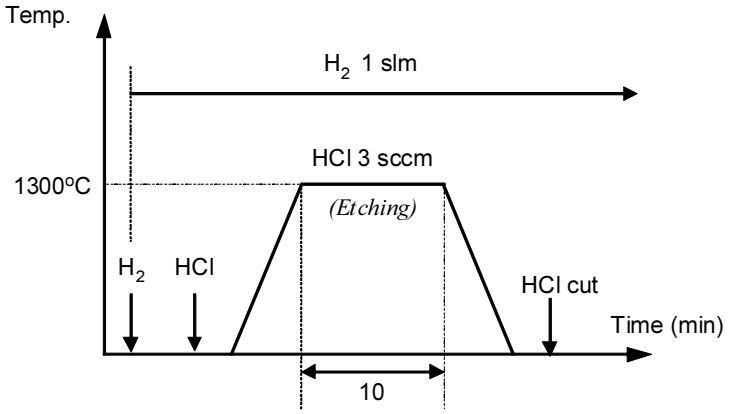


Figure 2.4: HCl gas etching program in cold-wall CVD reactor.

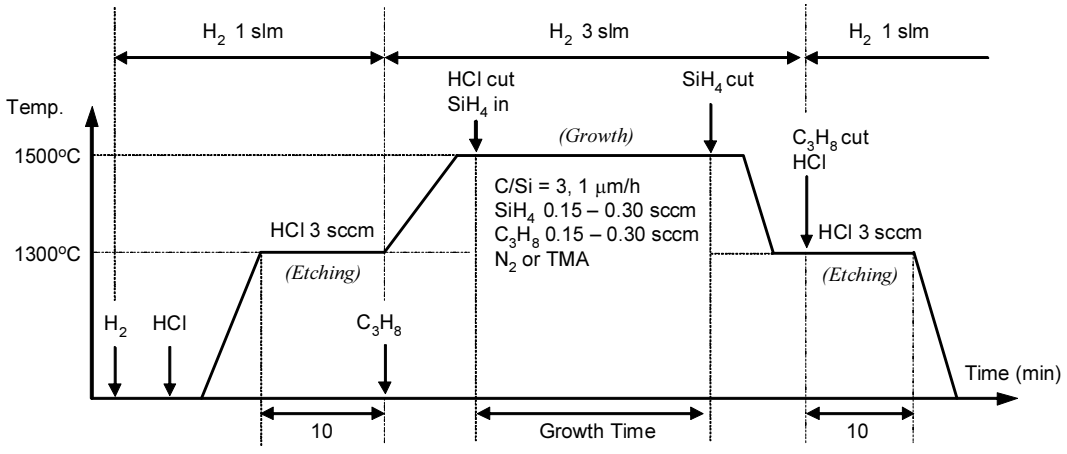


Figure 2.5: Typical growth program of SiC in cold-wall CVD reactor.

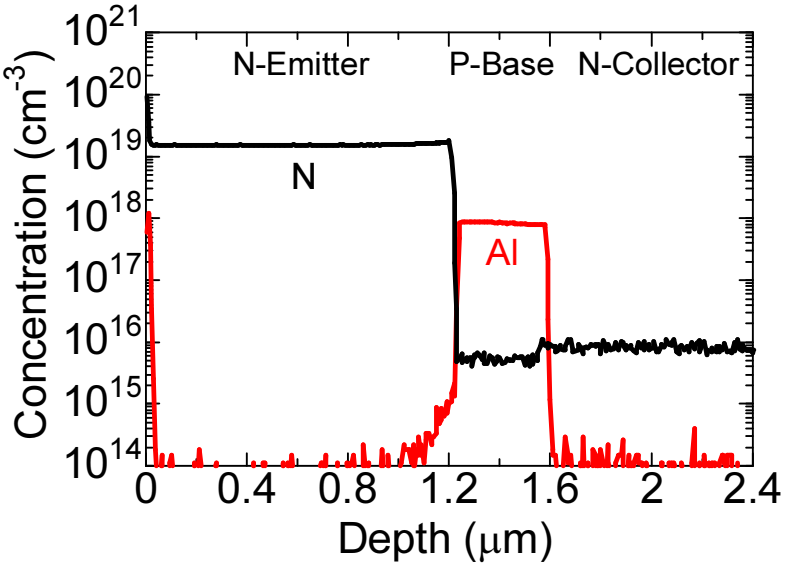


Figure 2.6: A typical SIMS depth profile of *npn* BJT structure grown by cold-wall CVD. It clearly shows top n region (N concentration [N]: 1.5×10^{19} cm^{-3}), middle p region ([Al]: 8–9×10^{17} cm^{-3}), and bottom n region ([N]: 8×10^{15} cm^{-3}), indicating a successful formation of abrupt *npn* junctions.

2.3 Plasma-Assisted Molecular Beam Epitaxy for Ⅲ-N Epitaxy

In contrast to SiC epitaxy, either CVD or MBE is used for Ⅲ-N epitaxy. CVD is preferably used in Ⅲ-N epitaxy since it is easy to scale up and thereby suitable for the mass production. In addition, it requires less maintenance period than MBE which uses an ultra-high vacuum (UHV) system. However, the CVD growth generally requires a high temperature at the range of 900–1200°C for Ⅲ-N growth which accelerates the three-dimensional (3D) growth in heteroepitaxial growth on SiC. In addition, CVD is difficult to equip *in-situ* monitoring system, which makes it more difficult to get the information at the initial growth stages.

Based on our research objectives, namely, getting an abrupt Ⅲ-N/SiC interface for Ⅲ-N/SiC HBTs by controlling initial growth stages of Ⅲ-N on SiC, we have employed MBE in this study. By using an MBE growth system, thermal decomposition of source materials is unnecessary because of assisting of plasma, resulting in the decrease of the growth temperature to the range of 600–1000°C, which makes it possible to achieve two-dimensional (2D) growth. In addition, characterization tools such as *in-situ* analysis of crystal growth kinetics and real-time monitoring of transitional surface structure are available thanks to its UHV system, providing more information on the initial growth stages [13–16]. In the following section, configuration of the MBE system used in this study is presented. Substrate pretreatments prior to the MBE growth and growth procedures are also described.

2.3.1 System Configuration

Ultra-High Vacuum System

The epitaxial growth of Ⅲ-N described in this study is carried out using an MBE growth system shown schematically in Fig. 2.7 (EV-1000S, EIKO). The system consists of a growth chamber, a sample-transfer chamber and a sample-exchange chamber. The sample-transfer chamber and sample-exchange chamber separated by gate valves are installed to prevent air from coming directly into the growth chamber when loading and unloading samples. A schematic diagram of the pumping system is presented in Fig. 2.7 (a). The sample-exchange chamber is exhausted by a turbo-molecular pump (TMP) connected to a rotary pump (RP). The background pressure is 3×10^{-6} Pa. The sample exchange chamber is equipped with an infrared lump, where loaded samples can be heated up to 200°C for degassing. The pressure in the sample-transfer chamber is exhausted to normally below 7×10^{-7} Pa with a sputter ion pump (SIP). The growth chamber, shown in Fig. 2.7 (b), is pumped by a TMP connected to a scroll pump (SP), which is accomplished to an oil-free system. The exhaust velocity of the TMP is 1300 l/s and the pressure reaches 3×10^{-8} Pa. The growth chamber is equipped with a liquid N_2 cryo-shroud, cooled to liquid N_2 temperature (77K) during growth for adsorption of residual gases. By using the cryo-shroud, the background pressure

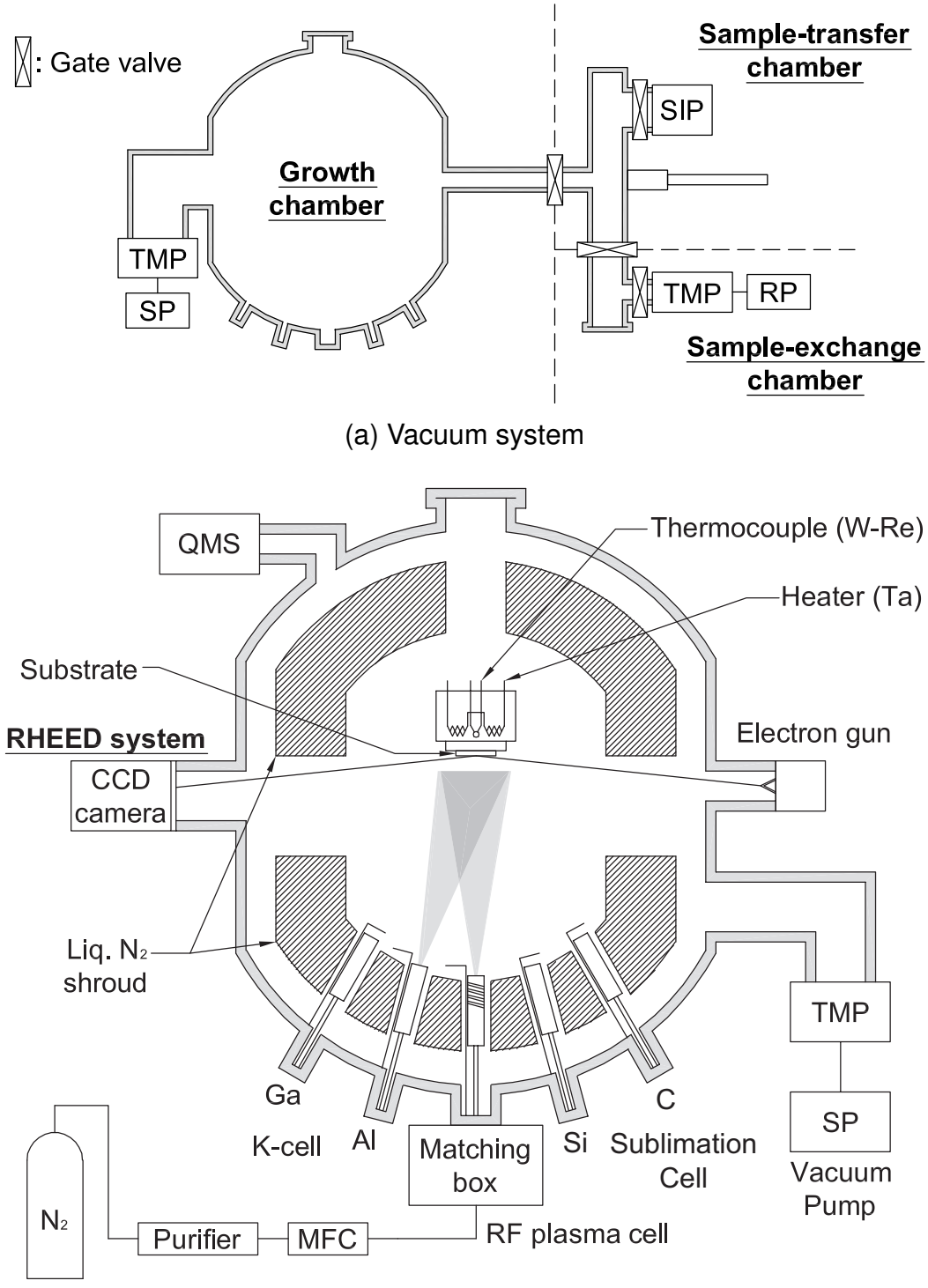


Figure 2.7: Schematic view of MBE (a) vacuum system and (b) growth chamber used in this study.

inside the chamber can be below 7×10^{-9} Pa. During epitaxial growth of Ⅲ-N, the pressure is $> 10^{-3}$ Pa due to the inflow of N_2 source gas. The growth chamber is equipped with a quadrupole mass spectroscopy (QMS) system, which can detect residual gases in UHV as well as impurity in N_2 source gas.

Substrate Heating and *In-Situ* Reflection High-Energy Electron Diffraction Systems (RHEED)

The SiC substrates used in this study are installed into a substrate holder. The substrate holder is made of molybdenum (Mo) and heated up to 1000°C by a tantalum (Ta) heater placed behind it (Fig. 2.8). The substrates are secured to the holder using a retaining ring which is made of tungsten (W). A diffuser plate made of pyrolytic boron nitride (PBN) is used for improved heating uniformity. The substrate temperature (T_{sub}) is measured by a thermocouple located just behind the substrate. Although the actual substrate temperature may be lower than the thermocouple temperature, the measured temperature without any corrections is given as the substrate temperature in this study.

An MBE growth system which operates in UHV allows incorporation of several surface monitoring tools. Among the analytical tools available, reflection high-energy electron diffraction (RHEED) has contributed to advances in epitaxial technology and improvements in the quality of epitaxial layers. The electron beam emitted from a sharpened filament is diffracted at the surface atoms of sample, and builds up a diffraction pattern on a fluorescent screen. In this study, an electron beam accelerated by 20 kV is applied for RHEED observation. RHEED monitoring is conducted for *in-situ* analyses of the kinetics in Ⅲ-N growth, and patterns are recorded through a 16-bit gradient Charge Coupled Device (CCD) camera. The monitoring of diffracted intensities is carried out by using a real-time image processing system (kSA400 RHEED system, k-Space Associates).

Effusion Cells and Radio-Frequency Plasma Source

The growth chamber is equipped with effusion cells for elemental Al and Ga evaporation, sublimation cells for elemental Si and C, and a radio-frequency (RF) plasma cell for producing active nitrogen (N*). Each cell has an individual shutter blade made of Ta. The RF plasma cell is mounted perpendicularly to substrates while Al, Ga, Si, and C cells are installed with 35°–tilting to the perpendicular of substrates.

Elemental Al of 6N (99.9999%) purity and Ga of 7N (99.99999%) purity are evaporated from Knudsen effusion cells. Al and Ga metals are held in 200g–SUMO$^{\mathrm{TM}}$ effusion cell crucibles made of PBN. The Al and Ga effusion cells have different heater configurations. For use with Al, a cold-lipped SUMO effusion cell, which is operated with the bottom filament only, is used. This cell is designed to prevent overflow caused by Al wetting of the PBN crucible under N_2 atmosphere. For use with Ga, a hot-lipped SUMO cell with a dual filament configuration is employed since metallic Ga tends to recondense at the crucible orifice. Intensities of the Al and Ga beam fluxes on the substrate surface are measured by

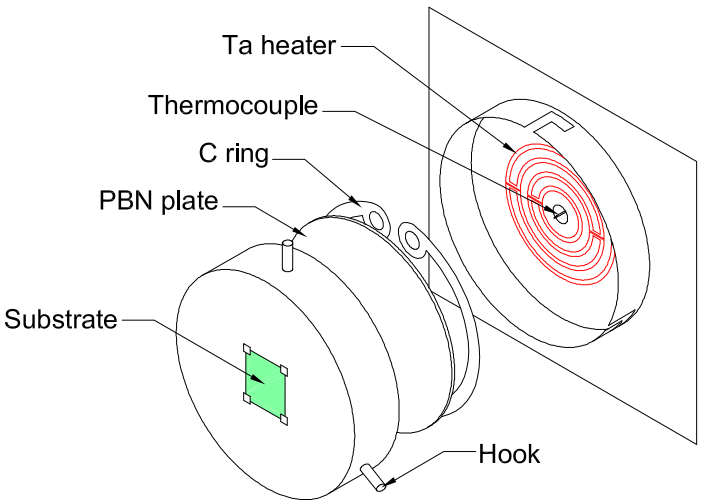


Figure 2.8: Schematic illustrations of heater and sample holder configuration.

a nude ion gauge located just below the sample. The operating temperature for the Al and Ga effusion cells used in this study are around 1170°C and 950°C , respectively, whereas the standby temperature are 750°C and 150°C, respectively. Note that the standby temperature of Al was kept above its melting point (660°C) since the lattice mismatch between Al and PBN causes mechanical stress or crack if Al was solidified.

Current-heating sublimation sources are used for Si and C sublimation. Si and C filaments are installed in the sublimation cells shielded by Si and C itself to provide pure Si and C. These cells are designed to provide very thin layer or doping of Si and C. For operation, they are heated by directly passing electrical current through it. In the case of Si, high resistivity Si filaments (FZ-Si, R $>$ 1000Ωcm) are used. The flux was controlled by applied current. The typical operation current used in this study is 50 A, corrsponding to the operation temperature of 1100°C, whereas the standby current is 5 A, corrsponding to the standby temperature of 500°C. In the case of C, high purity C filaments are used. The flux was controlled by applied current. The typical operation current used in this study is 75 A, corrsponding to the operation temperature of 1540°C, whereas the standby current is 10 A, corrsponding to the standby temperature of 200°C.

As for a source to produce N*, an RF plasma cell is employed. A microwave of 13.56 MHz is applied for N_2 activation. The plasma unit (UNI-Bulb RF Plasma Source, Applied EPI) is fitted with an optical emission detector that gives a photo-current reading correlated with the N* flux intensity. N_2 gas of 6N (99.9999%) purity is supplied to the RF plasma cell through a gettering-type purifier. The flow rate of N_2 gas is controlled to 1.00 sccm by a mass flow controller (MFC) and the applied RF power is set to 300 W in this study.

2.3.2 *In-situ* Ga Deposition and Desorption Treatment

Growth kinetics at the initial stages is affected by not only the surface morphology of SiC substrates but also the chemical condition. In the case of AlN (0001) growth on SiC (0001), removal of residual oxygen and realization of a 1/3 monolayer (ML) silicon-adsorbed superstructure has been reported to be effective in realization of initial two-dimensional (2D) growth of AlN [17]. A chemically-stable silicate adlayer was formed after the HCl gas etching, which was characterized by *in-situ* x-ray photoelectron spectroscopy (XPS) analysis. Although the silicate adlayer is impossible to decompose at 1000°C in an UHV, *ex-situ* HF treatment could successfully remove it from the HCl-gas-etched surface. However, a few oxygen atoms still remained on the surface treated with HF due to the adsorption of oxygen atoms during transfer through the air. An additional treatment, *in-situ* Ga deposition and desorption process, was effective to eliminate those residual oxygen atoms [18, 19] and a multiple treatment was more valid in particular [17]. In this procedure, the following reaction process proceeds [19, 20];

$$SiO_2 + 2Ga \longrightarrow SiO \uparrow + Ga_2O \uparrow . \tag{2.1}$$

Fig. 2.9 shows the *in-situ* XPS spectra obtained from the HCl-treated, HF-treated and Ga-treated surfaces of 6H-SiC (0001)Si-face substrates [17, 21]. Since the silicate adlayer was removed by HF treatment, the Si $2p_{3/2}$ peak tended to shift from SiO_2 to SiC. Although the silicate adlayer was removed, the O 1*s* peak was still observed due to the sticking of oxygen atoms to the surface. The residual oxygen was removed after 3 cycles of Ga treatment.

2.3.3 Growth Procedure for Ⅲ-N Epitaxy

HCl gas-etching treatments are effective to remove polishing scratches and reduce surface roughness on SiC surface. Well-organized step-and-terrace structures are obtained after HCl gas etching. Although a chemically-stable silicate adlayer was formed after the HCl gas etching, *ex-situ* HF treatment could successfully remove it from the HCl-gas-etched surface. Although a few oxygen atoms are still remained on the surface treated with HF, they are successfully removed with *in-situ* Ga deposition and desorption process.

In this study, based on the results described above, the growth of Ⅲ-N is carried out in the procedures as follows. First, the substrates are treated by HCl gas etching at 1300°C for 10 min under the HCl/H_2 flow of 3 sccm/1 slm. After the *ex-situ* HF treatment, the samples are loaded into the sample-exchange chamber. After the chamber evacuated to 10^{-5} Pa, the substrate is outgassed by infrared heating at around 200°C and then transferred into the growth chamber via the sample-transfer chamber. Fig. 2.10 represents a typical procedure for epitaxial growth of Ⅲ-N. The substrate temperature is raised to 600°C at a ramp rate of 30°C/min. Ga metal is deposited to the substrate at 600°C and then the substrate temperature is increased to 900°C. This Ga deposition and desorption process is performed three times and the substrate temperature is maintained at 1000°C for 10 min after the third Ga deposition process. After that, the temperature is decreased to growth temperature of 600°C. Active nitrogen (N*) is generated by the RF plasma cell and stabilized for 0–3 min with the shutter closed. After the stabilization of nitrogen plasma, vaporized Al, Ga and active nitrogen are introduced simultaneously to the substrate surface. At the end of growth the shutters of the cells are closed simultaneously and then the substrate temperature is lowered to room temperature at a rate of –20°C/min.

2.4 Summary

In this chapter, cold-wall CVD was proposed to achieve relatively thin layer of 0.35-1.2 μm or very thin epilayer of 0.05-0.20 μm required for BJTs and HBTs, respectively. Its system configuration, high temperature HCl gas etching prior to the growth, and growth procedure for SiC epitaxy were presented. In addition, plasma-assisted MBE was introduced for low temperature Ⅲ-N epitaxy with *in-situ* monitoring. Such features as ultra-high vacuum system, *in-situ* RHEED systems as well as *in-situ* Ga deposition and desorption treatment prior to the growth, and growth procedure for Ⅲ-N epitaxy were presented. With these

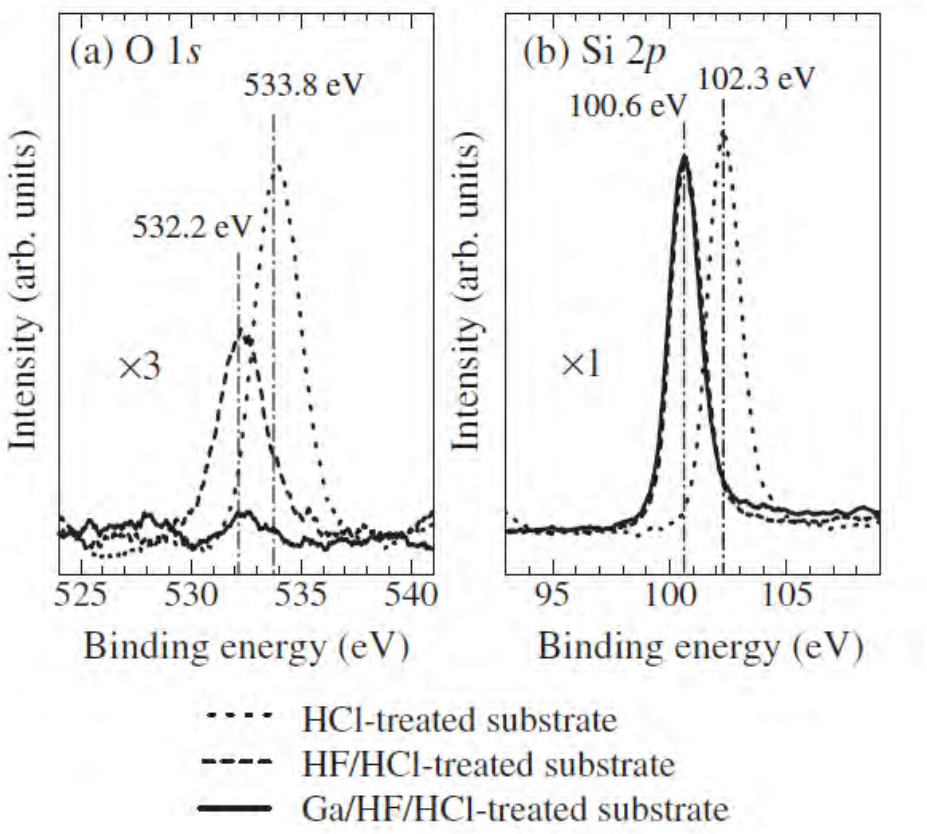


Figure 2.9: XPS spectra of Ga/HF/HCl-treated surface: (a) Si 2*p* (b) O 1*s* [17, 21].

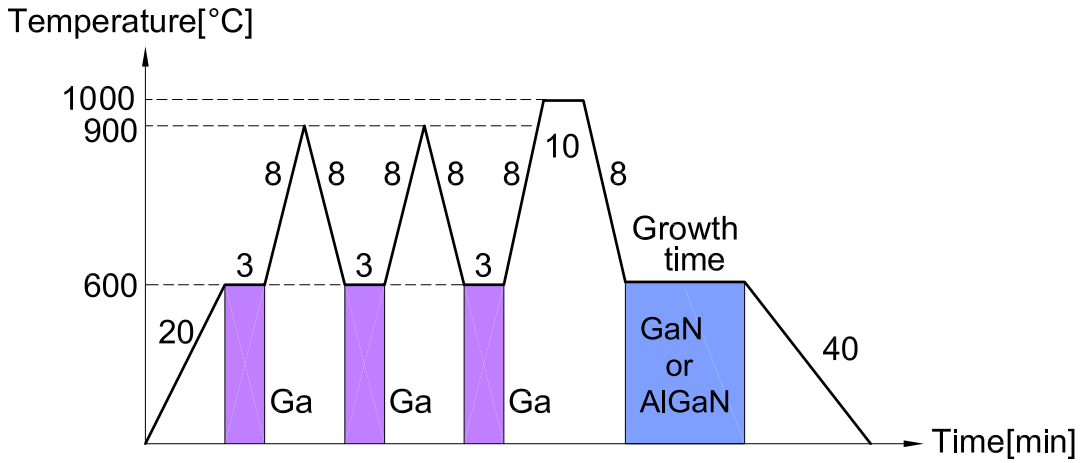


Figure 2.10: Typical growth program of III-N by plasma-assisted MBE.

systems, SiC BJT and Ⅲ-N/SiC HBT structure are successfully grown, which are explained in the next chapters.

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Chapter 3

Development of High-Current-Gain 4H-SiC Bipolar Junction Transistors

3.1 Introduction

Power bipolar junction transistors (BJTs) based on 4H-SiC are very attractive candidates for high-power switching devices because of such characteristics as high breakdown voltage, low on-resistance, and high current density [1]. For the best use of the advantages of SiC BJTs, they can be used at elevated temperature because they are free of gate-oxide reliability issues observed in metal-oxide-semiconductor field effect transistors (MOSFETs). Therefore, the current gain at both room and elevated temperatures should be high enough for practical applications to avoid power losses at the base-drive circuit since they are current-controlled devices. Several approaches have been reported to improve the current gain by optimizing device geometry [2, 3], by continuous epitaxial growth [2, 4, 5], by optimizing surface passivation [2, 6, 7], and by utilizing suppressed surface recombination structure [6]. However, SiC BJTs continue to suffer from limited current gains. In this chapter, we focus on improving current gain in SiC BJTs. We introduce various techniques such as new surface passivation technique, continuous epitaxy, and deep-level-reduction process based on thermal oxidation to achieve high current gain.

3.2 Key Issues for Achieving High-Current-Gain 4H-SiC BJTs

In this section, we describe what limits the current gain in SiC BJTs and how it can be improved. The issues for improving current gain can be divided into 2 parts: device design considerations and process considerations (Fig. 3.1).

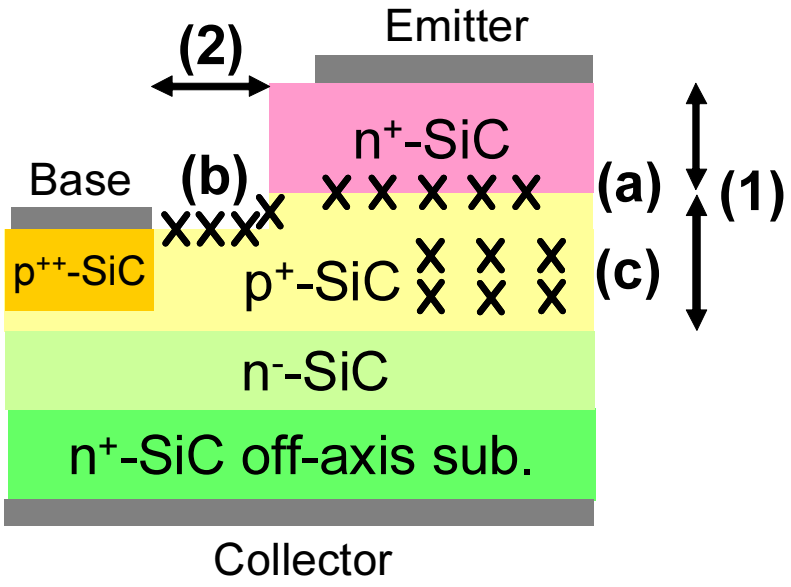

Figure 3.1: Current gain limiting parameters and defects in SiC BJTs.

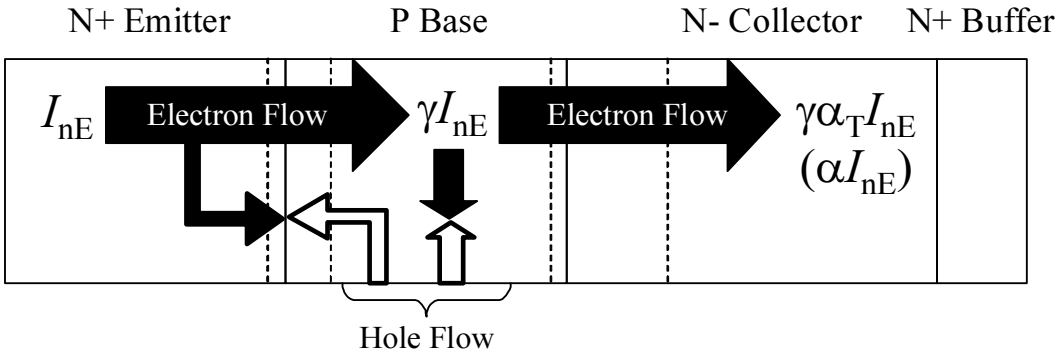

Figure 3.2: Current flow and recombinations in bipolar junction transistor (BJT).

3.2.1 Device Design Considerations

The design of BJT is very important since it determines the current gain. There are two important parameters limiting the current gain, which are optimized before starting the device fabrication.

(1) Thickness and Doping of Emitter and Base Epilayer

To begin with, the theoretical current gain of BJT is given by:

$$\alpha = \gamma \times \alpha_{\mathrm{T}}\,, \tag{3.1}$$

where α common-base current gain, γ emitter injection efficiency, and α_{T} base transport factor (Fig. 3.2). When we assume the base transport factor α_{T} of unity,

$$\alpha = \gamma = \frac{D_{\mathrm{nB}} L_{\mathrm{pE}} n_{\mathrm{B}}}{D_{\mathrm{nB}} L_{\mathrm{pE}} n_{\mathrm{B}} + D_{\mathrm{pE}} W_{\mathrm{B}} p_{\mathrm{E}}}\,, \tag{3.2}$$

where D_{nB} diffusion coefficient of electron in p-base, D_{pE} diffusion coefficient of holes in n-emitter, L_{pE} diffusion length of hole, W_{B} base width, n_{B} minority carrier concentration in equilibrium within the p-base, p_{E} minority carrier concentration in equilibrium within the n-emitter. Then, common-emitter current gain β will be given by

$$\beta = \frac{\gamma}{1-\gamma} = \frac{D_{\mathrm{nB}} L_{\mathrm{pE}} n_{\mathrm{B}}}{D_{\mathrm{pE}} W_{\mathrm{B}} p_{\mathrm{E}}}\,. \tag{3.3}$$

Note that emitter thickness $t_{\mathrm{E}} > L_{\mathrm{pE}}$ is satisfied otherwise β will be given by

$$\beta = \frac{\gamma}{1-\gamma} = \frac{D_{\mathrm{nB}} t_{\mathrm{E}} n_{\mathrm{B}}}{D_{\mathrm{pE}} W_{\mathrm{B}} p_{\mathrm{E}}}\,. \tag{3.4}$$

These equations tell that the emitter thickness t_{E} should be larger than a minority carrier diffusion length L_{pE} to achieve a high current gain. In the case of the t_{E} smaller than the minority carrier diffusion length, the recombination of minority carriers injected from the base to the emitter more frequently occurs at the emitter ohmic contact region, where the recombination velocity is assumed to be very large. As a result, reduced emitter injection efficiency and thus low current gain are observed. Accordingly, t_{E} more than 1 μm was typically used in previous reports [4–6, 8, 9]. In this study, emitter thickness of 1.2 μm is used. W_{B} is also an important factor to determine the current gain. It should be thin enough to obtain high current gain, while it should be thick enough to support the blocking voltage. In addition, the ratio of emitter doping to base doping is a key factor to limit the current gain. In this thesis, we have chosen the emitter and base doping of 2×10^{19} cm^{-3} and 1×10^{18} cm^{-3}, and base width of 350 nm. The caluculated theoretical current gain is 343 assuming $n_{\mathrm{B}} \sim 5\times10^{18}$ cm^{-3}, $p_{\mathrm{E}} \sim 5\times10^{16}$ cm^{-3}, $t_{\mathrm{E}} = 1.2$ μm $< L_{\mathrm{pE}}$, $W_{\mathrm{B}} = 0.35$ μm, and $D_{\mathrm{nB}} = D_{\mathrm{pE}}$ (Table 3.1), whereas this BJT theoretically blocks 1.8 kV without base punch through when 10-μm-thick collector ($N_{\mathrm{d}} = 5\times10^{15}$ cm^{-3}) is adopted. For comparison, device structures of reported SiC BJTs are also shown in Table 3.2.

Table 3.1: Design of fabricated SiC BJTs. Theoretical current gain is 343, whereas theoretical blocking voltage is 1.8 kV.

Layer	Thickness	Doping	Carrier Concentration
Emitter	1.2 μm	2×10^{19} cm^{-3}	5×10^{18} cm^{-3}
Base	350 nm	1×10^{18} cm^{-3}	5×10^{16} cm^{-3}
Collector	10 μm	5×10^{15} cm^{-3}	—

Table 3.2: Device structures of reported high-current-gain SiC BJTs [4–6, 8, 9].

SiC BJT	Emitter ($cm^{-3}/\mu m$)		Base (cm^{-3}/nm)		Collector ($cm^{-3}/\mu m$)		Gain	V_{CEO} (V)	R_{sp-on} ($m\Omega cm^2$)
Honda (2009)*	2×10^{19}	1.0	1×10^{18}	100	5×10^{15}	10	134	950	3.2
	1×10^{16}	0.2							
Cree 1 (2008)	2×10^{19}	2.0	1×10^{18}	250	5×10^{15}	14	110	250	3.6
Cree 2 (2008)	3×10^{19}	2.0	4×10^{17}	1000	5×10^{15}	14	70	1200	6.3
Rutgers (2009)	2×10^{19}	0.5	3×10^{17}	700	7×10^{15}	12	70	1600	5.1
	1×10^{19}	0.5							
KTH (2008)	5×10^{19}	0.1	4×10^{17}**	700	4×10^{15}	15	60	1200	5.2
	2×10^{19}	0.9							
Kyoto (This work)	2×10^{19}	1.2	1×10^{18}	350	5×10^{15}	10	-	-	-

*Suppressed Surface Recombination-BJT (SSR-BJT) **graded

(2) Emitter–Base Spacing

To achieve low resistivity base ohmic contacts, ion implantation technique is usually employed in SiC BJTs. However, this process causes implantation defects underneath the base contact region. Although subsequent annealing at high temperature ($> 1700°C$) minimizes the contribution of such defects on BJT performance, it is reported that current gain is affected by carrier recombination at the heavily implanted base contact region so that the emitter–base spacing L_{BE} plays an important role determining current gain [2, 3]. According to [2, 3], the current gain is improved by widening the L_{BE}, and remains almost constant when the emitter–base spacing exceeds 3–4 μm. To avoid undesirable recombination associated with implantation defects, BJTs with emitter-base spacing of 10 μm is investigated in this thesis. It should be noted that the L_{BE} can be reduced to 1 μm without current gain degradation if the BJTs don't utilize base contact implantation [10].

3.2.2 Process Considerations

In contrast to the design of the BJT, processing of the BJTs needs technological insights to achieve high current gain. This thesis mainly deals with this process related issues, as explained in followings.

(a) Continuous Epitaxial Growth

Emitter injection efficiency can be affected by the interface recombination at the space-charge region in emitter–base junction. If these layers are grown in a continuous run, the emitter-base junction would show an abrupt junction without any additional defect formation. In contrast, when these epilayers are grown in a different reactor, crystall defects or point defects can be generated at the junction due to the deviation of growth condition especially at the initial stage of regrowth. As a result, the current gain can be reduced. Accordingly, continuous epitaxial growth of the all epilayer (collector, base, and emitter) has been proposed to achieve high current gain [2, 4, 5].

(b) Surface Passivation

Once electrons are injected from the emitter to the base region, they have an opportunity to recombine via the traps at the extrinsic base surface. So the quality of surface passivation technique for the extrincic SiC base surface is one of the critical steps to suppress the surface recombination and thus to improve the current gain. In previous works, it has been demonstrated that the current gain is improved by surface passivation processes, such as wet oxidation [3, 4], thermal oxidation in nitric oxide (N_2O) [2] or nitrous oxide (NO) [8]. However, a systematic study on the effect of surface passivation and correlation between MOS interface states and BJT current gain are not clearly addressed so far, and such study should be intensively conducted.

(c) Bulk Recombination

Point defects observed in p-base region can work as recombination centers that reduce the current gain. Zhang *et al.* investigated the impact of base width to enhance the base transport factor, and they successfully demonstrated high current gain of 110 with reduced base width [8]. However, there have been no reports on the reduction of deep levels to enhance the lifetime of p-base and current gain. Therefore, suppression of the bulk recombination (improvement of poor lifetime in p-SiC regardless of indirect band structure) should be considered.

3.2.3 Strategy for High-Current-Gain SiC BJTs

Since the recombination current (I_{r}) that limits the current gain can be described as

$$I_{\mathrm{r}} = I_{\mathrm{r\_Interface}} + I_{\mathrm{r\_Surface}} + I_{\mathrm{r\_Bulk}}, \tag{3.5}$$

ultimate reduction of all these recombination current should be considered.

In this thesis, we propose a novel deep-level-reduction process (DLR process) to reduce the bulk recombination. This DLR-process features 2 step thermal oxidation (1150°C, 5 h × 2), which is reported to reduce major deep levels such as $Z_{1/2}$ and $EH_{6/7}$ observed in as-grown epi-layer and enhance the lifetime in both n-SiC [11] and p-SiC [12] (Fig. 3.3). We assume these processes to minimize the recombination in the p-SiC base and to make it clear the effect of surface recombination and interface recombination.

Then we have investigated various surface passivation technique and device geometries to suppress the surface recombination at the emitter-mesa sidewalls. For the surface passivation, up to now, most SiC BJTs have been fabricated using thermally-grown oxides as the surface passivation layer. On the other hand, it has been reported that the deposited oxides with post-deposition anneal in N_2O or NO (nitridation anneal) show lower interface trap density than thermally-grown oxides, which has attracted much attention for high performance SiC MOSFETs [13]. In other words, surface recombination in SiC BJTs may be suppressed by passivating with the deposited oxide. Recently, 3 kV SiC BJTs with an improved current gain of 40 was reported by utilizing deposited oxides with N_2O-annealing [14]. However, there are still few reports regarding deposited oxides for the surface passivation of BJTs, and systematic investigation of deposited oxides including the annealing condition is necessary to achieve higher current gains. In this way, we investigate the impacts of various post-deposition annealing processes for deposited oxides on the current gain in SiC BJTs.

Finally, continuous growth of the emitter junction to reduce the interface states at the emitter–base junction is investigated.

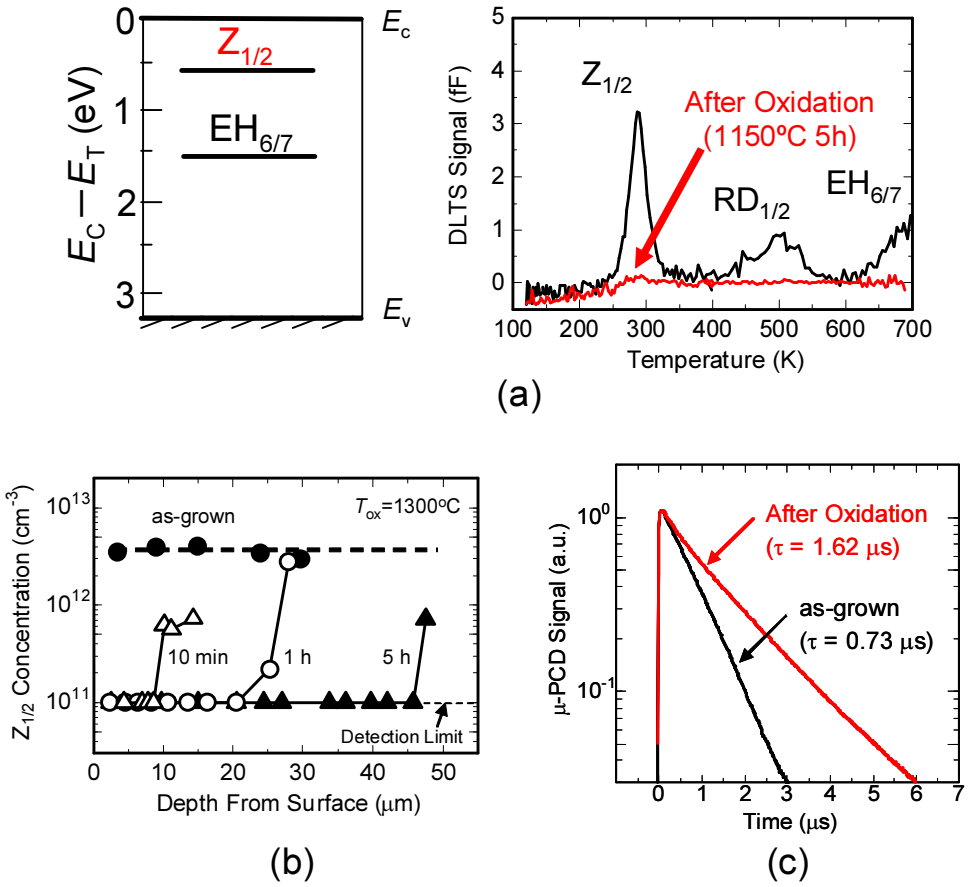

Figure 3.3: (a) DLTS spectra of an n-type 4H-SiC(0001) epilayer before and after thermal oxidation (1150°C, 5 h) (b) Depth profile of the $Z_{1/2}$ center concentration before and after thermal oxidation (1300°C) measured for n-type 4H-SiC(0001) epilayers with a thickness of 40-50 μm and N_d = 2–4×10^{15} cm^{-3} (c) Photoconductance decay curves for an n-type 4H-SiC(0001) epilayer (100 μm, N_a = 1×10^{15} cm^{-3}) before and after thermal oxidation (1300°C, 5 h × 2) [11].

3.3 Device Structure and Fabrication Process

Fig. 3.4 and Fig. 3.5 show the schematic structure and the process flow of a fabricated BJT. The BJT has an epitaxially-grown, N-doped n^--SiC collector (10 μm, $N_d = 5\times10^{15}$ cm^{-3}), an Al-doped p^+-SiC base (0.35 μm, $N_a = 1\times10^{18}$ cm^{-3}), and an N-doped n^+-SiC emitter (1.2 μm, $N_d = 2\times10^{19}$ cm^{-3}) grown on n-type 4H-SiC (0001) off-axis substrates (8° off-oriented toward [11$\bar{2}$0]) by chemical vapor deposition (CVD). In some sections, the emitter and base layers were grown in a different reactor to examine the effect of continuous epitaxy. Double-mesa BJTs were fabricated using reactive ion etching based on a mixture of CF_4 and O_2 using a deposited SiO_2 mask. Multiple Al^+ ion implantations at 500°C with an impurity concentration of 3×10^{20} cm^{-3} were carried out to form p^{++} base contact regions. It is reported that heavy implantation underneath the p-SiC base metal can decrease the current gain [3]. To minimize that effect, activation annealing was carried out at as high as 1800°C for 10 min. Ni ohmic contacts were formed on the emitter and base surface using a standard lift-off technique. Rapid thermal annealing was performed at 950°C in Ar.

All the BJTs discussed in this thesis have a single finger with a finger length of 100 μm and if not indicated, the width of 20 μm (active area excluding contact pads: 0.002 mm^2), and the distance between the emitter and the base contact regions (L_{EB}) is 10 μm.

3.3.1 Concept of Deep-Level-Reduction Process

To maximize the lifetime in the p-SiC base layer, we have developed DLR-process based on thermal oxidation for all BJTs investigated in this thesis. (Fig. 3.6). In order to develop DLR-process, we took into account both effect of as-grown defects and process-induced defects. As already mentioned, as-grown defects such as $Z_{1/2}$ and $EH_{6/7}$ are eliminated by thermal oxidation [11]. To completely eliminate these defects in SiC BJTs, we included thermal oxidation 1150°C for 5 h twice. However, process-induced defects, namely HK0 center associated with CF_4-based RIE, are generated after the oxidation, and subsequent anneal at 1550°C is required to eliminate this [15].

Accordingly, for the BJTs on (0001), we performed first thermal oxidation step in O_2 at 1150°C for 5 h *before* activation annealing of implants to the p-SiC base contact region. This process contributes to the reduction of major deep levels such as $Z_{1/2}$ and $EH_{6/7}$ observed in as-grown epi-layer [11], and gives rise to the HK0 center associated with CF_4-based RIE [15] which can be eliminated at the following high temperature annealing. Then, we employed the activation annealing of implants at 1800°C for 10 min. This will regenerate $Z_{1/2}$ and $EH_{6/7}$, whereas the HK0 center that anneals out at 1550°C will disappear [15]. To re-eliminate $Z_{1/2}$ and $EH_{6/7}$, we utilized thermal oxidation in O_2 at 1150°C for 5 h once again. This process may reduce the deep levels in p-SiC base layer and implanted layer [16]. By this deep-level-reduction process, all the existing deep levels may be eliminated.

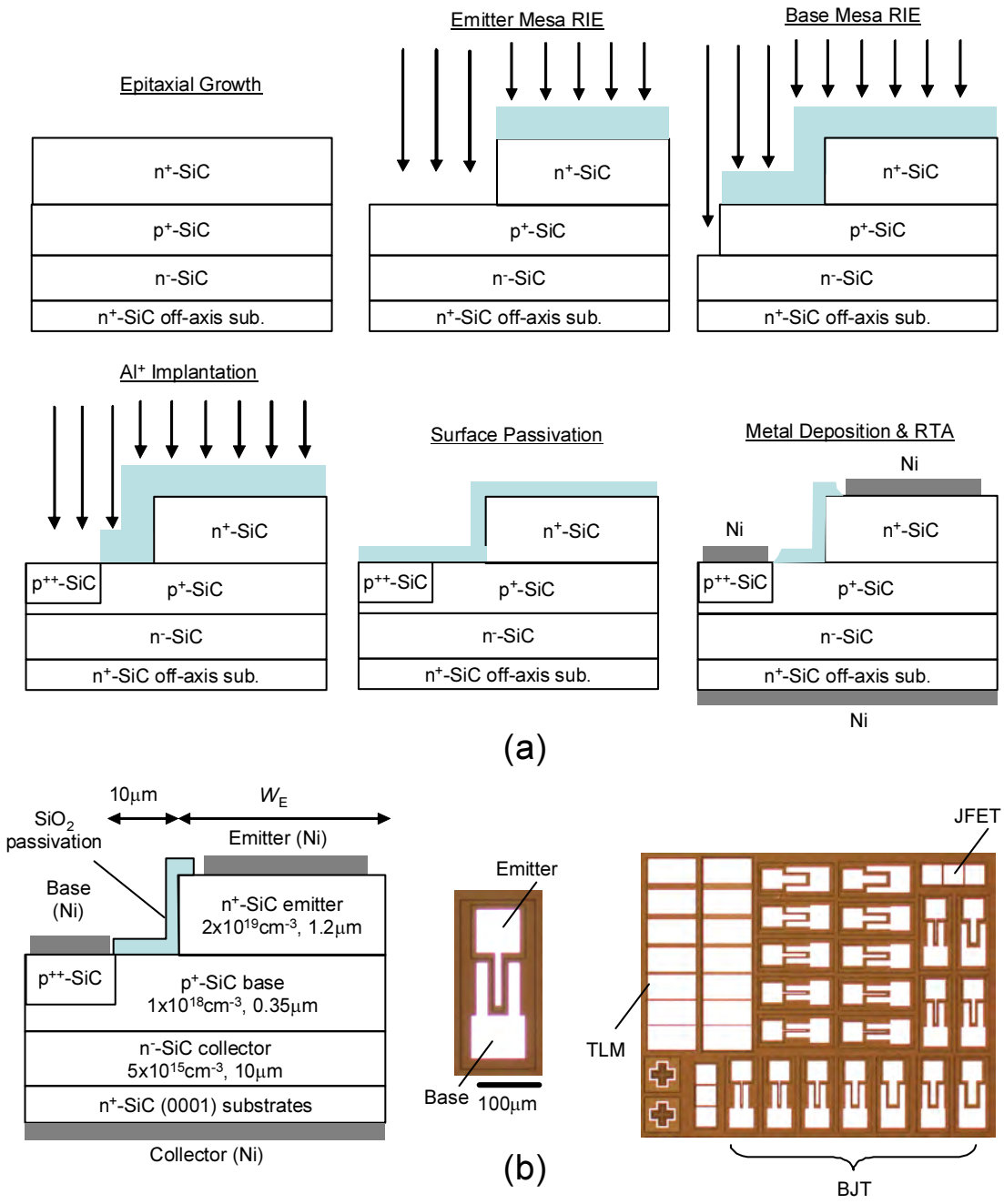

Figure 3.4: Schematic cross section of a fabricated 4H-SiC BJT and optical images of fabricated single finger BJT.

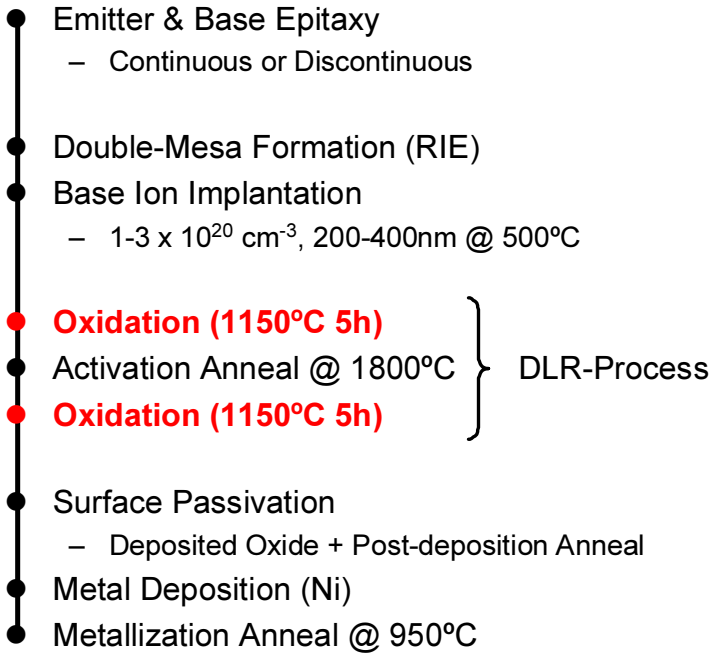

Figure 3.5: Fabrication process of 4H-SiC BJTs featuring deep-level-reduction process based on thermal oxidation.

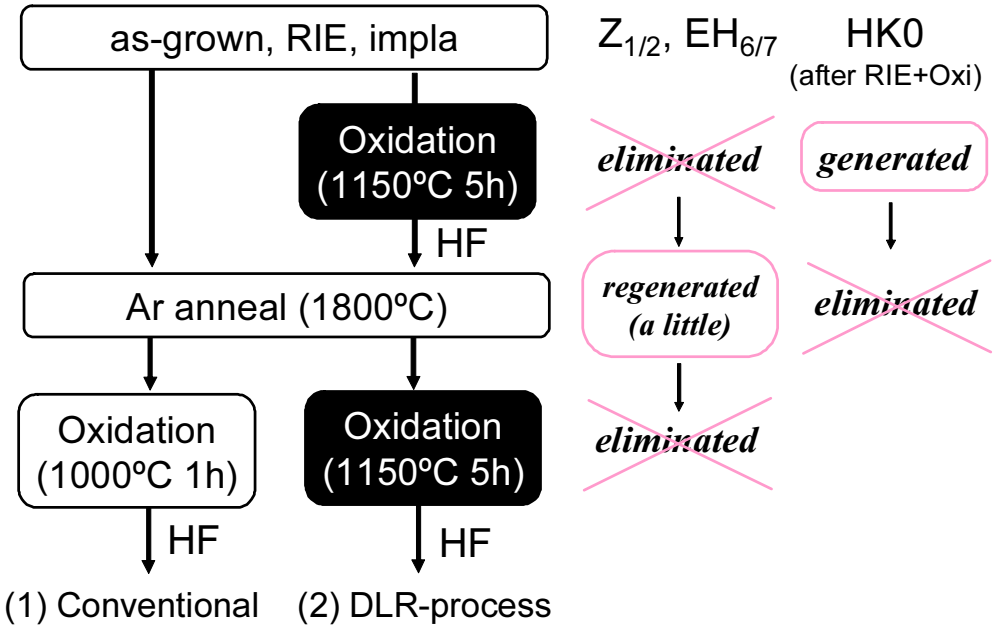

Figure 3.6: Schemetic illustrations of deep-level-reduction process based on thermal oxidation and its impact on deep levels.

3.4 Impact of Deposited Oxide Passivation on BJT Performance

3.4.1 Deposited Oxide Passivation and Post-Deposition Annealing

In this section, the BJTs prepared by separated growth run for the emitter and base layer are investigated. For the passivation, 80-nm-thick SiO_2 films were prepared by plasma-enhanced chemical vapor deposition (PECVD) at 400°C using tetraethoxysilane (TEOS) and O_2 as source gases. Oxides were then nitrided by 10%-diluted N_2O or NO in N_2 at 1300°C for 2 h followed by N_2 annealing at 1300°C for 30 min (Table 3.3). For comparison, device D, a BJT passivated with a thermally-grown oxide in O_2 at 1300°C (65 nm) followed by nitridation annealing in N_2O at 1300°C for 4 h, was fabricated. Fig. 3.7 shows the measured current gain as a function of collector current for the four BJTs (devices A-D in Table 3.3). The current gains were measured under $V_{CB} = 0$ V. The four BJTs exhibited a tendency where the current gain increases with increasing the collector current in the low-current region and falls at high collector current. As discussed in [17], the increase of the current gain at low collector current is explained by the low injection efficiency that is attributed to the interface recombination at the emitter-base junction and the surface recombination at SiO_2/SiC. The drop of current gain at high collector current is attributed to the saturation of the injected carriers in the base.

The BJTs passivated with deposited oxides annealed in N_2 showed a peak current gain of 35, whereas the BJTs passivated with deposited oxides annealed in N_2O showed a two times higher peak current gain of 73 (the common-emitter I_C-V_{CE} characteristics and a Gummel plot of the BJT are shown in Fig. 3.8). Higher current gain could be achieved by utilization of NO anneal, resulting in a peak current gain of 85 (the common-emitter I_C-V_{CE} characteristics and a Gummel plot of the BJT are shown in Fig. 3.9). Since the BJTs are processed simultaneously except for the surface passivation process, the current gain improvement is attributed to the lower surface recombination at the SiO_2/SiC interface by utilizing nitridation anneal in N_2O or NO for the deposited oxides. The utilization of N_2O or NO anneal is effective to reduce the interface traps at the SiO_2/SiC, resulting in lower surface recombination. It has been reported that the interface nitridation by N_2O or NO leads to the reduced interface state density near the both conduction band edge [18, 19] and valence band edge [20], and for (0001) as well as $(11\bar{2}0)$ [21].

The reference BJTs passivated with thermally-grown oxides annealed in N_2O showed a current gain of 50, which is lower than that of the BJTs passivated with deposited oxides annealed in N_2O, indicating that the utilization of the deposited oxide instead of the thermally-grown oxides for the surface passivation contributed to the reduction of surface recombination. Note that these tendencies of BJTs are consistent with those of the MOS interface trap density, i.e., the oxide deposition and NO annealing processes, which is re-

Table 3.3: Process conditions for deposited and thermally-grown oxides.

Device	Oxide	Annealing Conditions	
		Annealing 1 (1300°C) →	Annealing 2 (1300°C)
A	PECVD	—	N_2 30min
B	PECVD	10%-diluted N_2O 2h	N_2 30min
C	PECVD	10%-diluted NO 2h	N_2 30min
D	Thermally-grown	10%-diluted N_2O 4h	N_2 30min

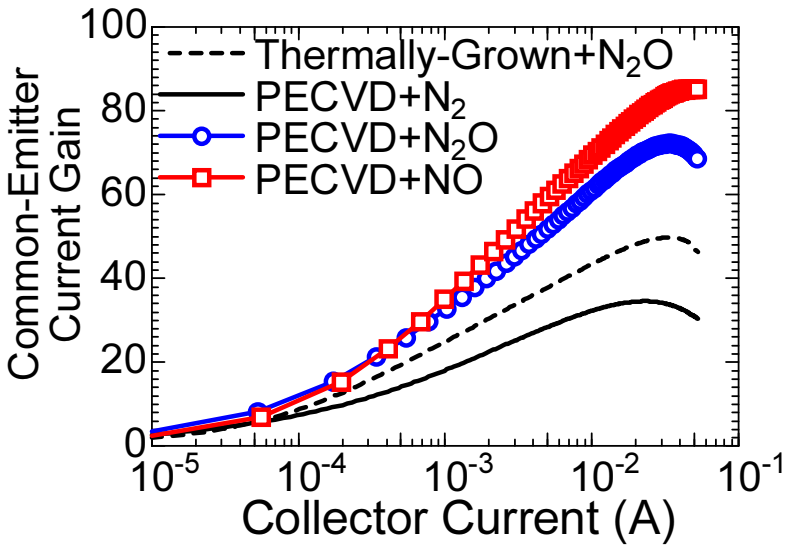

Figure 3.7: Measured current gain as a function of collector current for four BJTs (devices A–D in Table 3.3). Peak current gains were 35 for N_2-annealed-deposited oxide, 50 for N_2O-annealed-thermal oxide, 73 for N_2O-annealed-deposited oxide, and 85 for NO-annealed-deposited oxide.

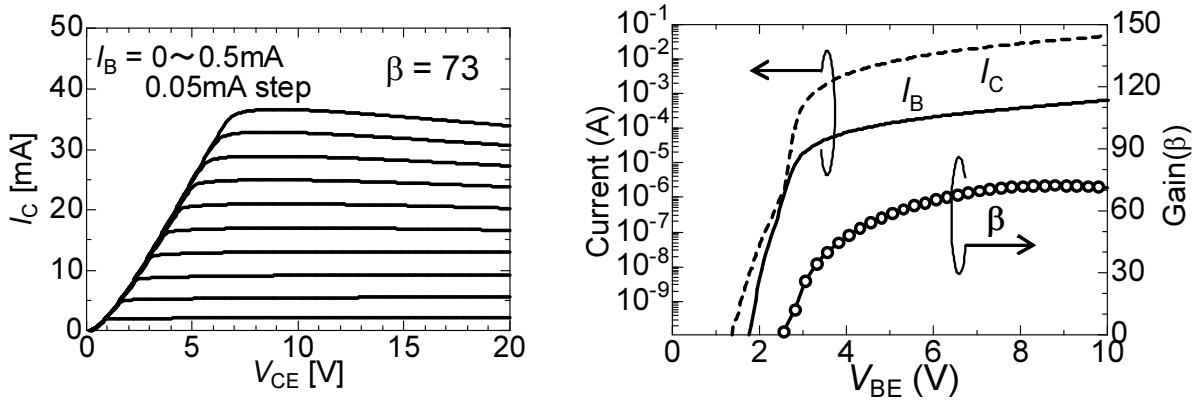

Figure 3.8: (left) Common-emitter I_C-V_{CE} characteristics of a BJT with a deposited oxide annealed in N_2O for 2 h. Maximum current gain of 73 was observed. (right) Gummel plot of the BJT. Current gain was calculated from the ratio of collector and base current.

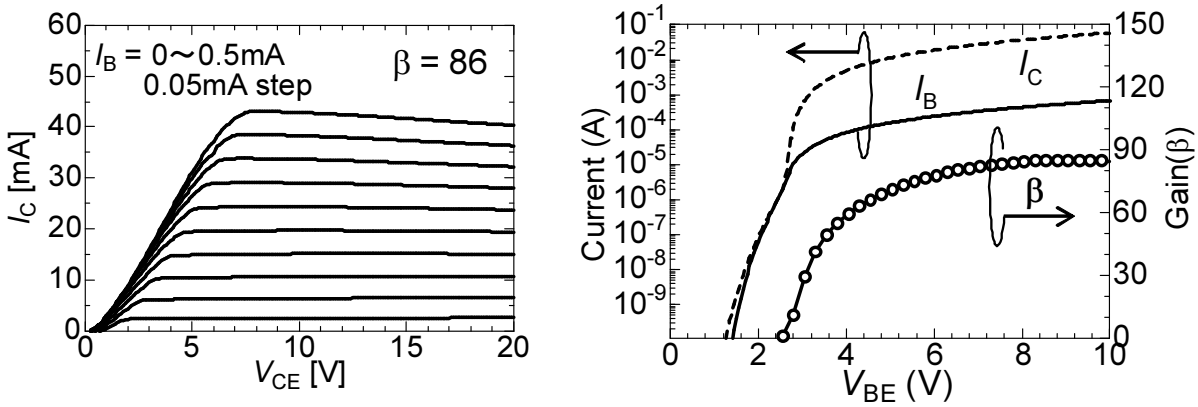

Figure 3.9: (left) Common-emitter I_C-V_{CE} characteristics of a BJT with a deposited oxide annealed in NO for 2 h. Maximum current gain of 86 was observed. (right) Gummel plot of the BJT. Current gain was calculated from the ratio of collector and base current.

ported to show the lowest interface trap density among the processes discussed here [13], contributing to the highest current gain in the BJTs, as shown in Fig. 3.10. These results suggest that advanced processes developed for high performance MOSFETs such as oxide deposition followed by NO anneal are promising for the surface passivation of the BJTs.

3.4.2 NO-Annealing Time Dependence

To achieve even higher current gain, we have investigated the NO annealing time dependence on the current gain in BJTs. Fig. 3.11 shows the measured current gain as a function of collector current for the BJTs passivated with deposited oxides annealed in NO for 0.5 h, 1 h, and 2 h. BJTs passivated with deposited oxides annealed in N_2 (without NO anneal) are also shown as a reference. Peak current gains were 85 for 2 h NO-anneal sample, whereas a much improved current gain of 97 for 1 h NO-anneal sample and 99 for 0.5 h NO-anneal sample were achieved. Short-period NO anneal contributed to enhancement of the current gain.

Fig. 3.12 shows the common-emitter I_C-V_{CE} characteristics and a Gummel plot of a BJT with a deposited oxide that was annealed in NO for 30 min. A maximum current gain of 102 was achieved at a base current of 0.5 mA and V_{CE} = 9 V. The negative resistance of the collector current in the high-current region is attributed to the self-heating effect during measurement that increased the hole concentration in the p-SiC base and reduced the current gain. We obtained the open-base blocking voltage V_{CEO} of 600 V, although these BJTs do not have junction termination.

3.4.3 Geometrical Effect

To further investigate the effect of surface recombination, BJTs with variable emitter finger width and different finger directions having a $\{11\bar{2}0\}$ sidewall or a $\{1\bar{1}00\}$ sidewall were fabricated. From this subsection, surface passivation by deposited oxide nitrided in 10%-diluted NO at 1300°C for 30 min was employed to minimize the surface recombination for BJTs.

Fig. 3.13 summarizes the current gain of BJTs on (0001) with various finger width and directions grown by discontinuous and continuous runs. Fig. 3.13 clearly shows that the current gain depends on the finger width and direction. The current gain increases with the finger width because a wider BJT can reduce the effect of surface recombination at the sidewalls (emitter-size effect), and the gain saturated for finger width over 20 μm. BJTs with $\{1\bar{1}00\}$ sidewalls showed higher current gains than BJTs with $\{11\bar{2}0\}$ sidewalls, indicating a lower surface recombination on $\{1\bar{1}00\}$ sidewalls. Yano *et al.* pointed out that MOS interface properties of the trench sidewalls fabricated on SiC 8° off-axis substrates strongly depend on the crystal planes [22]. According to their report, $(11\bar{2}0)$ 8° off channel plane showed a lower interface state density (D_{it}), whereas $(\bar{1}\bar{1}20)$ –8° off channel plane

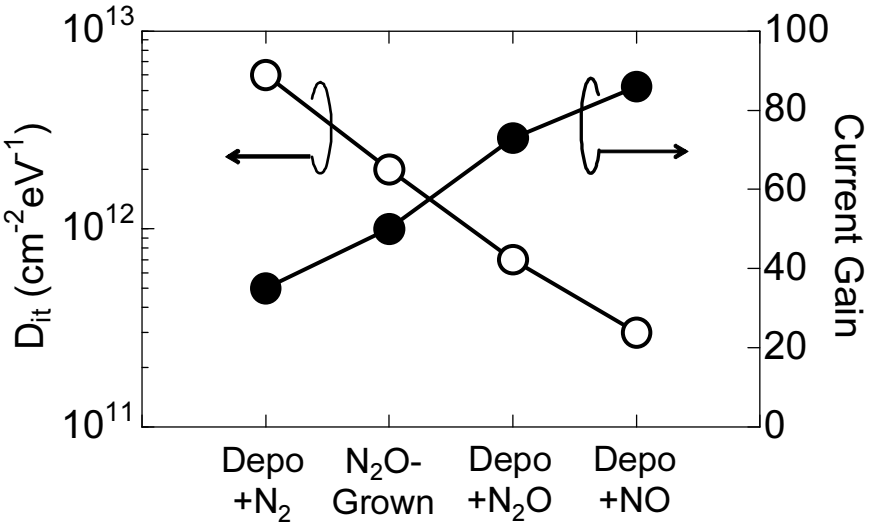

Figure 3.10: Comparison of D_{it} at SiO_2/SiC interface and current gain of BJT. BJT processed with low D_{it} process showed high current gain.

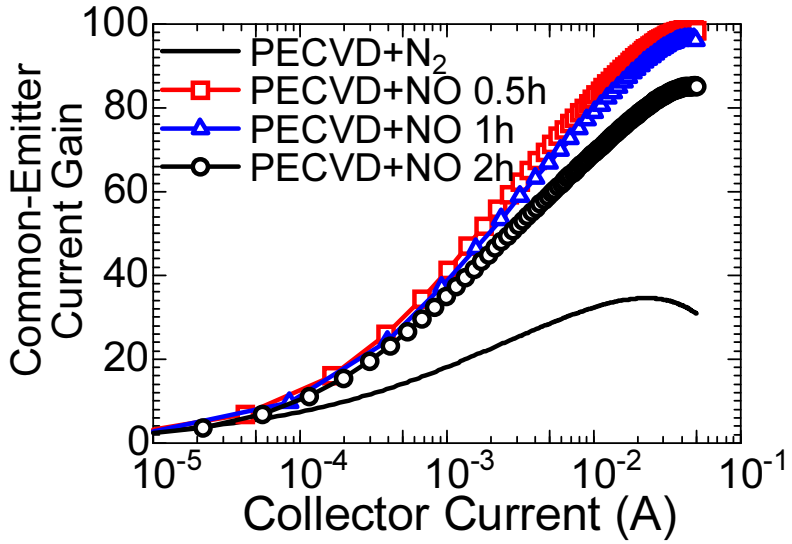

Figure 3.11: Measured current gain as a function of collector current for BJTs passivated with deposited oxides annealed in NO. NO annealing time has been changed from 0.5 h to 1 h, 2 h. Peak current gains were 85 for 2 h NO anneal sample, 97 for 1 h NO anneal sample, 99 for 0.5 h NO anneal sample.

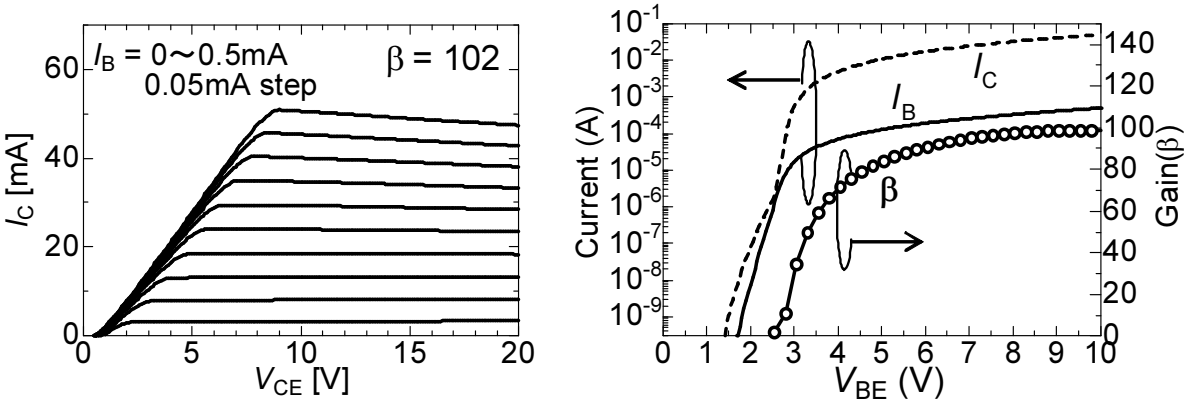

Figure 3.12: (left) Common-emitter I_C-V_{CE} characteristics of a BJT with a deposited oxide annealed in NO for 30 min. Maximum current gain of 102 was observed. (right) Gummel plot of the BJT. Current gain was calculated from the ratio of collector and base current.

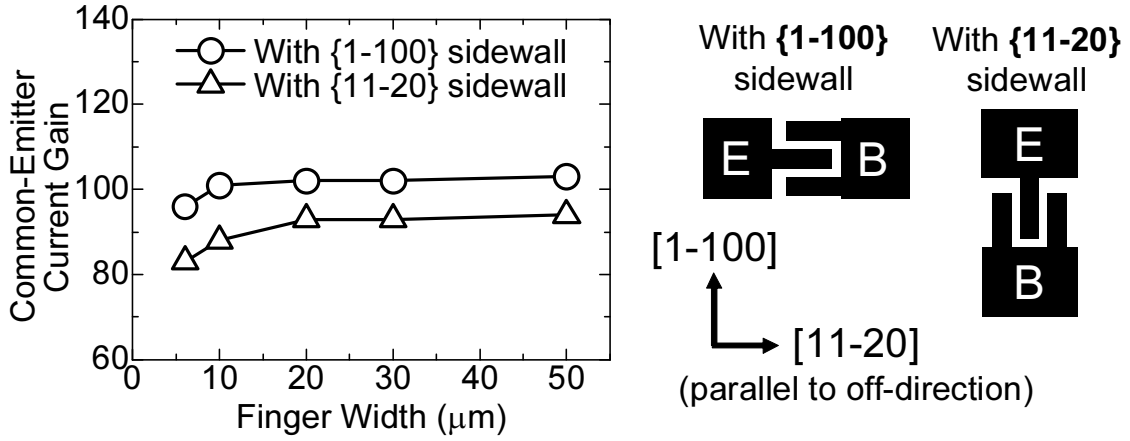

Figure 3.13: Summary of current gain of BJTs with various device geometries fabricated on (0001). Current gain increases with finger width. BJTs with $\{1\bar{1}00\}$ sidewalls exhibited higher current gain compared with those with $\{11\bar{2}0\}$ sidewalls.

exhibited a higher D_{it} compared with $\{1\bar{1}00\}$, due to the large off-angle of the substrate. As a result, the sum of the D_{it} at $SiO_2/SiC\{1\bar{1}00\}$ is smaller than that at $SiO_2/SiC\{11\bar{2}0\}$. Since the D_{it} value has correlation with the current gain in BJTs [7, 23], we infer that the high current gain in the BJTs with $\{1\bar{1}00\}$ sidewalls is attributed to the smaller D_{it} at $\{1\bar{1}00\}$ planes that may suppress the surface recombination. With 20-μm-wide fingers and $\{1\bar{1}00\}$ sidewalls, we achieved a current gain of 102, whereas we achieved a current gain of 93 with $\{11\bar{2}0\}$ sidewalls.

3.5 Impact of n-SiC Passivation on BJT Performance

Toward further reduction of surface recombination, we investigate the effect of n-SiC surface passivation combined with high temperature HCl treatment on the current gain of 4H-SiC BJTs in this section.

3.5.1 Aim and Concept

When we gain insights from AlGaAs/GaAs HBT, where extrinsic base surface was characterized by a surface recombination velocity [24], it is reported that graded-bandgap-base structure [25] or fully-depleted AlGaAs passivation layer [26–28] is effective to reduce the surface recombination. The graded-bandgap-base structure technique produces built-in internal electric field in p-base layer which bends lateral flow of injected electron toward the collector, eliminating emitter size effect. Similar approach is investigated by simulation in SiC BJTs [29], where a thin, highly-doped p-SiC layer between emitter-base region blocked injected electrons toward the surface. However, this is technologically difficult since it needs very thin (10 nm) top-base layer. In contrast, fully-depleted AlGaAs surface passivation techniques were developed to cut the access of electron toward the p-GaAs surface. Similar approach is investigated experimentally in SiC BJTs [6], where an extrinsic base is covered by a highly resistive p-type (HRP) region. Although this structure is applicable to SiC BJTs, it requires precise control to form the HRP region.

In this section, to further reduce the surface recombination and gain insights on it, we investigate an alternative structure that employs lightly-doped n-SiC as a passivation layer. This structure can be fabricated in almost the same way as conventional BJTs. We investigate the effect of n-SiC surface passivation layer, and technological issues observed in this structure are discussed. We also investigated the effect of high temperature HCl treatment, which is reported to reduce the surface roughness of SiC. We discuss the effect of different high temperature HCl treatment on the current gain of SiC BJTs.

In addition to ON-state characteristics, we present our newly established 11-μm-deep-mesa edge termination technique based on inductively coupled plasma (ICP) etching using Cl_2/O_2 gas and SiO_2 mask. We successfully demonstrate 1.0-1.5 kV BJTs with this technique. The advantages of this technique and the experimental details on the formation of

deep trench are also discussed in this section.

3.5.2 Low-Doped n-SiC Passivation

Fig. 3.14 shows the schematic structure of a fabricated BJT. We prepared BJT structure having 0.2-μm-thick N-doped n$^-$-SiC spacer ($N_\mathrm{d} = 1{\times}10^{16}$ cm^{-3}) between emitetr and base. Note that the emitter and base layer are grown in a different reactor. In this study, emitter was etched down to the middle of n-SiC spacer so that the n-SiC works as a passivation layer. We designed the final thickness of n-SiC surface passivation layer after all the processing should be 100 nm.

Fig. 3.15 shows the current gain as a function of collector current for the BJTs with n-SiC passivation layer. Measurement was performed under $V_\mathrm{CB} = 0$ V. Here, the base thickness was fixed to 350 nm. For comparison, BJTs without n-SiC passivation fabricated by etching emitter edge down to the extrinsic p-SiC base surface, and conventional BJT without n-SiC spacer and n-SiC passivation layer are shown. As shown in Fig. 3.15, they showed a tendency that the current gain increased with collector current, indicating recombination current is dominant at low collector current. Reference BJT showed a peak current gain of 100. By utilizing n-SiC spacer layer, the current gain was reduced to 86. By employing surface n-SiC passivation, the current gain was reduced to 43. As already discussed, if n-SiC surface passivation layer is fully depleted, it blocks the access of injected electrons in p-SiC toward the surface so that higher current gain is expected. However, our results showed opposite tendency. One possible explanation for this is that the n-SiC layer is not fully depleted under forward bias (see Fig. 3.16). In AlGaAs/GaAs HBT technology, it was pointed out that it is important to ensure the n-AlGaAs layer fully depleted. Otherwise parasitic emitter current flows through the undepleted portion of the passivation ledge, and then upon reaching the end of the ledge (nearby the base contacts), be injected into the base [30]. Since an ohmic contact region is considered to have very high surface recombination velocity, the recombination current at the base contacts would limit current gain. Although we designed n-SiC layer above p-SiC is as thin as 100 nm, it might not be sufficient enough to be fully depleted. On the other hand, utilization of thinner n-SiC passivation layer is technologically difficult. So our results indicate that to employ such n-SiC passivation layer, we need lower doping ($< N_\mathrm{d} = 5{\times}10^{15}$ cm^{-3}) to make it fully depleted.

3.5.3 High-Temperature HCl Treatment

To further gain insights on the surface recombination in SiC BJTs, we conducted high temperature HCl gas etching. This aims at suppression of surface roughening after RIE, which may contribute to the reduction of interface states at SiO_2/SiC and thus surface recombination current. We conducted high temperature HCl gas etching (0.3% HCl diluted in H_2) at 1300°C or 1500°C. Typical etching rate was 0.42 μm/h and 0.51 μm/h, respectively. The

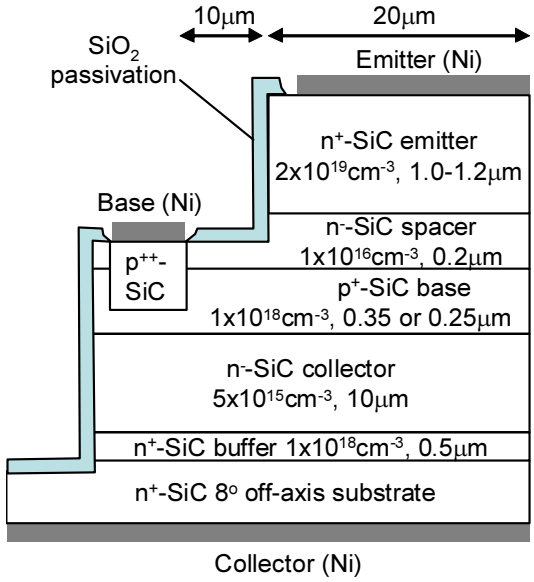

Figure 3.14: Schematic cross section of 4H-SiC BJT with n-SiC spacer layer.

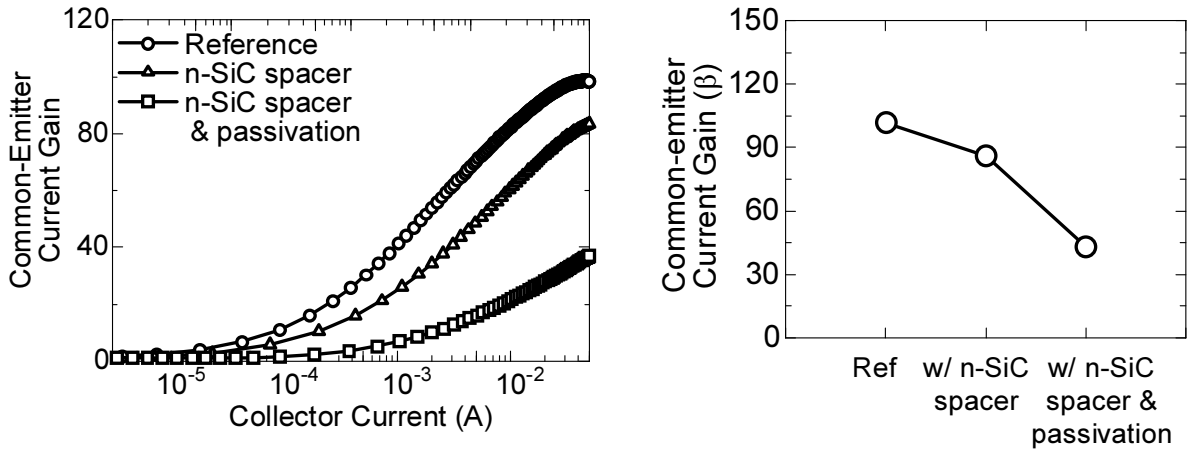

Figure 3.15: (left) Current gain as a function of collector current and (right) summary of peak current gains for BJTs with n-SiC passivation layer, BJTs without n-SiC passivation fabricated by etching emitter edge down to the extrinsic p-SiC base surface, and conventional BJT without n-SiC spacer and n-SiC passivation layer. Base thickness was fixed to 350 nm.

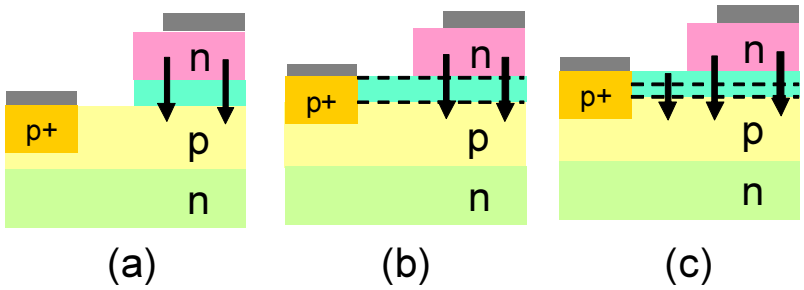

Figure 3.16: Schematic illustration of electron flow under forward bias. (a) reference BJT (b) BJT with fully depleted n-SiC surface passivation layer having (ideal case) (c) BJT with n-SiC surface passivation layer which is not fully depleted under forward bias.

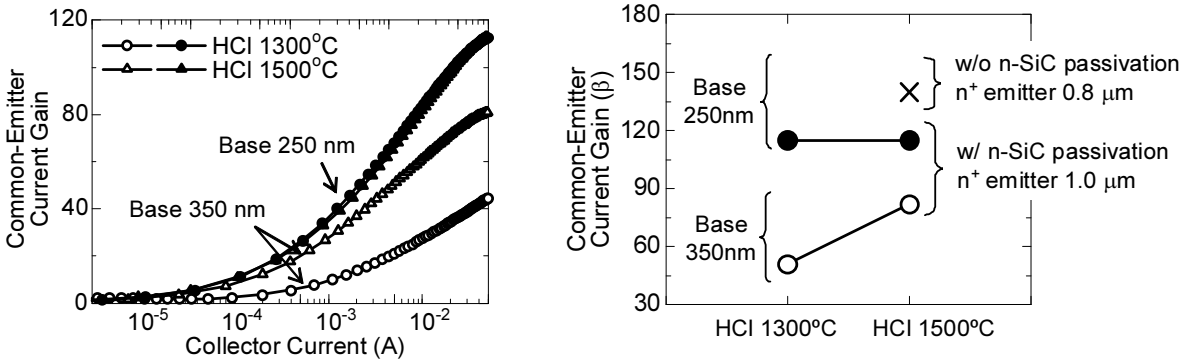

Figure 3.17: (left) Current gain as a function of collector current and (right) summary of peak current gains for BJTs with n-SiC passivation layer treated with HCl gas etching. Base thickness was varied from 350 nm to 250 nm.

etching time was adjusted to get an etched SiC thickness of 200 nm. Fig. 3.17 shows the current gain as a function of collector current for the BJTs with n-SiC passivation layer. When the base thickness is 350 nm, peak current gains of 51 and 83 were obtained in the case of HCl gas etching at 1300°C and HCl gas etching at 1500°C, respectively. On the other hand, when the base thickness is 250 nm, a peak current gain of 115 was obtained in both cases of HCl gas etching at 1300°C and 1500°C. The common-emitter I_C-V_{CE} characteristics of the BJTs are shown in Fig. 3.18.[1]

Judging from the results on BJTs with base thickness of 250 nm, we speculate that surface recombination current was independent on HCl gas etching temperature. In other words, the fact that we observed significant difference in the case of base thickness of 350 nm with different HCl gas etching temperature might not be associated with the suppression of surface recombination but another mechanism. One explanation of this may be the suppression of bulk recombination by annealing at 1500°C. Although we reported that the deep-level-reduction process based on thermal oxidation may greatly reduce the bulk recombination in SiC BJTs [31], final oxidation steps still leaves a new center, namely, HK0 center associated with C-interstitials [32], which may contribute to the bulk recombination in p-SiC. It is also known that such HK0 center can be eliminated by high temperature annealing at 1500°C [15, 32]. Therefore, we assume that HCl gas etching at 1500°C contributed to the elimination of the HK0 center, resulting in improved current gain. When the base thickness is 250 nm, there is no difference in current gain, which may be attributed to the sufficient lifetime in p-SiC base when the base thickness was 250 nm.

3.5.4 Deep-Mesa Edge Termination for 1 kV SiC BJTs

In addition to ON-state characteristics, the OFF-state characteristics of the BJTs are also characterized in this study. It is known that the edge termination is important to achieve high blocking capability under reverse bias, since electric-field crowding mostly occurs at the mesa edge. To solve this, we utilized deep-mesa edge termination in this study. This technique was introduced recently in SiC devices, where 6 μm [33] or 2.5 – 7.5 μm [34] deep trench was formed to obtain 1.2 kV-class performance. There are several advantages of this technique beyond conventional junction termination extension (JTE) [23, 35] or guard-rings (GRs) [5, 6]: (1) Compared with JTE, additional ion implantation process (usually once or twice) and optimization of dose sensitive to surface charge is unnecessary; (2) GRs need lithography step with a few micron ring space, which can give some deviation in blocking performance; (3) Compared with both JTE and GRs, chip area can be saved, contributing to the reduction of fabrication cost. One of the problems in deep-mesa edge termination is micro-masking as well as a metal contamination since Ni is usually used as a mask to obtain high etching selectivity. Alternatively, we developed a Cl_2-based RIE with high selectivity

[1] A 250 nm-base BJT treated with HCl gas ethcing at 1500°C (without n-SiC passivation) is also shown. This BJT has emitter width of 0.8 μm, and exhibited a current gain of 140.

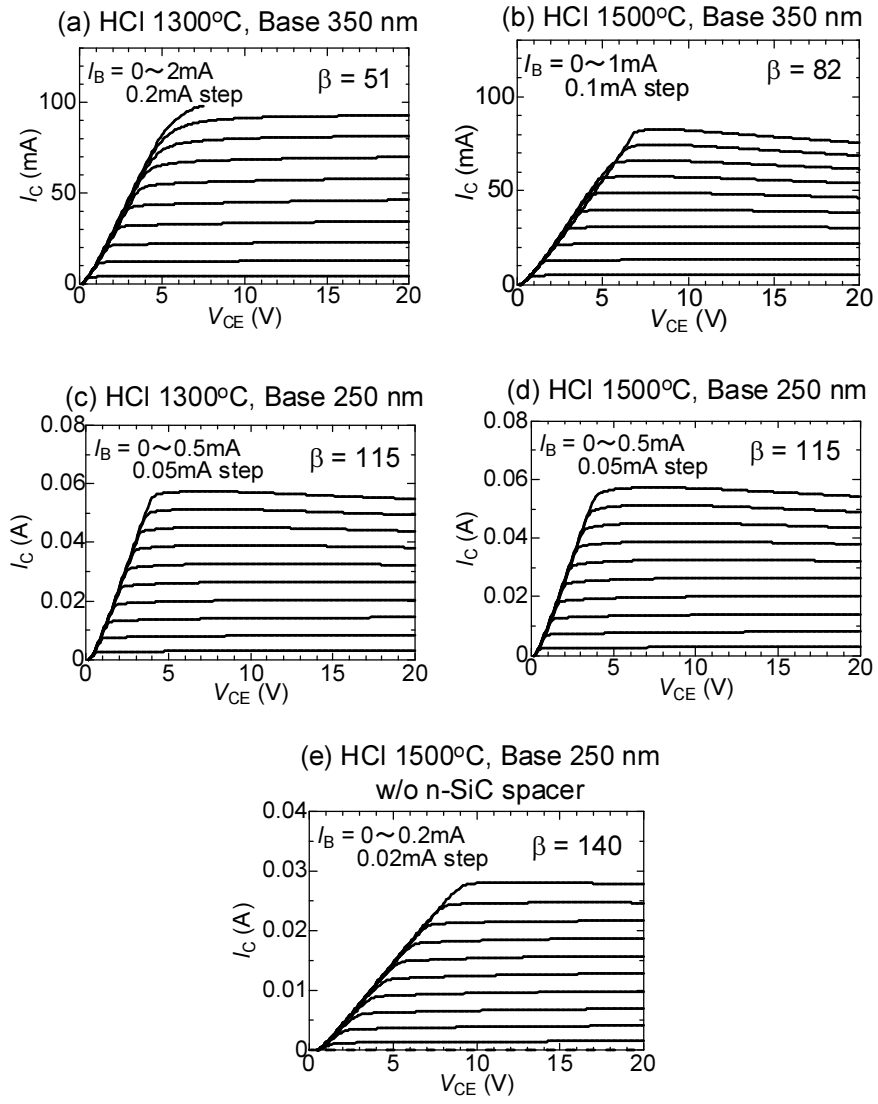

Figure 3.18: Common-emitter I_C-V_{CE} characteristics of BJTs: 350 nm-base BJTs treated with HCl gas ethcing at (a) 1300°C and (b) 1500°C, 250 nm-base BJTs treated with HCl gas ethcing at (c) 1300°C and (d) 1500°C, and (e) 250 nm-base BJT treated with HCl gas ethcing at 1500°C (without n-SiC passivation).

using a deposited SiO_2 mask in this study.

The RIE was performed with Samco RIE-101iPH etcher under 1 Pa with a Cl_2 flow rate of 25 sccm, and ICP/Bias was set to 300/150 W. Fig. 3.19 shows the impact of additional O_2 flow on the etching rate and selectivity. Without O_2 flow, the selectivity was 2.8. By increasing O_2 flow, we found that the selectivity was increased when the O_2 flow was below 15 sccm. This may be because Cl_2 gas primarily attacks Si while additional O_2 gas supports the reaction with C as follows:

$$SiC + 2Cl_2 \longrightarrow SiCl_4 + C \tag{3.6}$$

$$C + O_2 \longrightarrow CO_2\,. \tag{3.7}$$

The similar tendency that the etching rate of SiC and thus selectivity become large with additional flow of O_2 can be found in CF_4/O_2 based RIE. The advantage of Cl_2 based RIE over CF_4-based RIE is the low etching rate of SiO_2. Thus, high selectivity of SiC over SiO_2 can be obtained in Cl_2/O_2-based RIE. As shown in Fig. 3.19, the maximum selectivity of 6.5 and 7.7 were obtained in the case of O_2 flow of 10 sccm and 15 sccm, respectively. It should be noted that in the case of O_2 flow of 15 sccm, however, we observed micro-masking. This may be because too much flow O_2 causes additional reaction with $SiCl_4$, which was produced by SiC etching:

$$SiCl_4 + O_2 \longrightarrow SiO_2 + 2Cl_2\,. \tag{3.8}$$

Accordingly, O_2 flow of 10 sccm (SiC etching rate: 245 nm/min) was used for BJT fabrication. A SEM top-view and cross-sectional view were shown in Fig. 3.20. We successfully fabricated 11-μm-deep trench with a little micro-masking. In this case, the base mesa edge was etched down to the substrates so that the effect of electric field crowding at the mesa edge is completely eliminated.

Blocking characteristics of the BJTs are shown in Fig. 3.21. The BJTs showed open-emitter blocking voltage (V_{CBO}) of 1680 V and 1390 V when the base thickness was 350 nm and 250 nm, respectively. Since V_{CBO} reflects blocking characteristics of base-collector diodes (theoretical breakdown voltage: 1850 V), this result suggests that base-collector diodes are successfully fabricated with the deep-mesa edge termination. The lower V_{CBO} in the case of base thickness of 250 nm may be associated with ion implantation underneath the base contact region. In this study, we utilized an ion implantation with a high dose of 1.2×10^{16} cm^{-2} (corresponding impurity concentration and depth: 3×10^{20} cm^{-3}, 0.4 μm). These implanted atoms penetrate the base-collector junction in the case of base thickness of 250 nm, whereas it does not occur in the case of base thickness of 350 nm. Since such high-dose implantation causes defective region especially near the tail region of implanted species and may generate leakage current, we assume that such deep implantation penetrating base-collector junction affected the blocking characteristics. As for open-base blocking voltage (V_{CEO}), BJTs showed 1390 V and 1030 V when that base thickness was 350 nm and 250 nm,

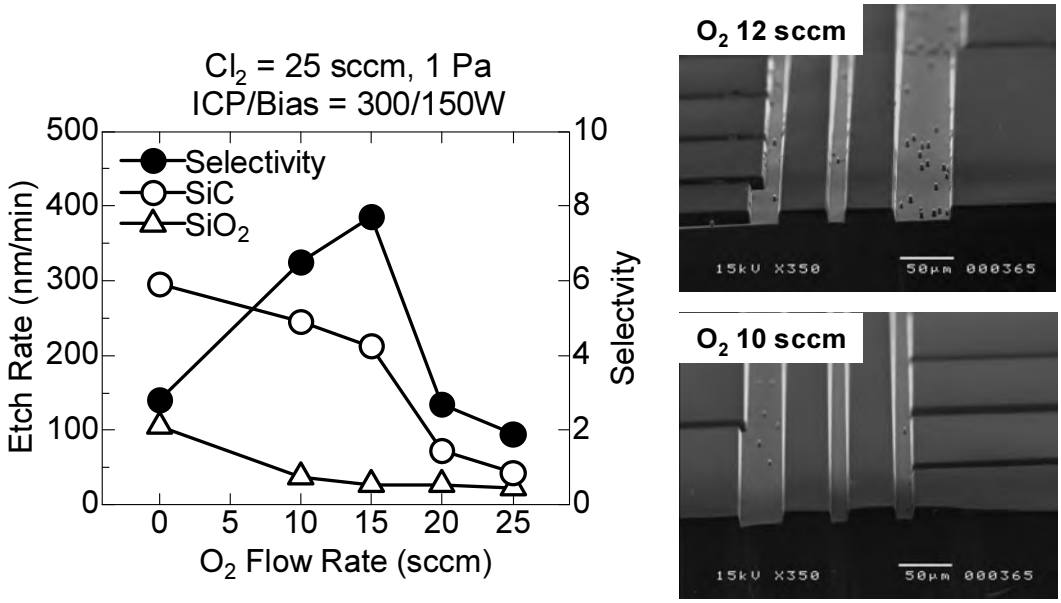

Figure 3.19: (left) Etching rate of SiC and SiO_2, and calculated etching selectivity in Cl_2/O_2 RIE under 1 Pa, Cl_2 flow of 25 sccm, and ICP/Bias = 300/150W. (right) SEM top-views of fabricated 11-μm-deep mesa with different O_2 flow.

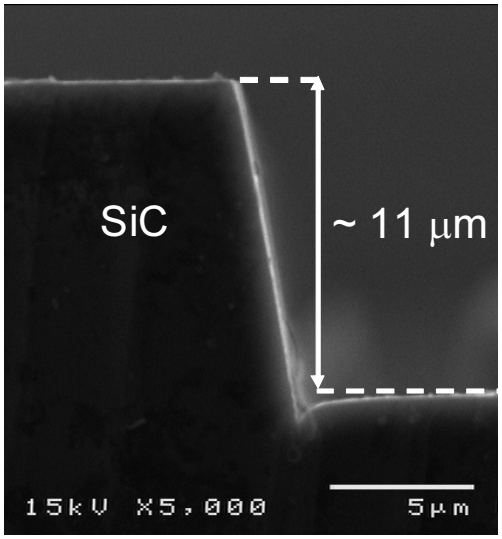

Figure 3.20: A SEM cross-sectional view of fabricated 11-μm-deep mesa.

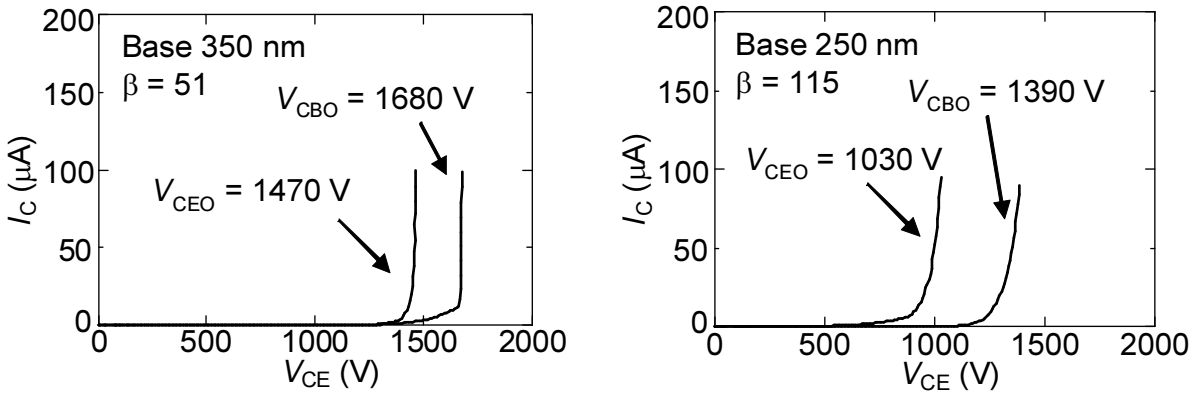

Figure 3.21: Open-base (V_{CBO}) and open-emitter blocking voltage (V_{CEO}) of fabricated BJTs. BJT with base thickness of 350 nm showed V_{CEO} of 1470 V and V_{CBO} of 1680 V. BJT with base thickness of 250 nm showed V_{CEO} of 1030 V and V_{CBO} of 1390 V.

respectively. Although reduced blocking voltage was obtained in the case of base thickness of 250 nm due to the deep ion implantation mentioned above, we successfully demonstrated a 1 kV-class BJT with these techniques.

3.6 Impact of Continuous Epitaxy on BJT Performance

3.6.1 Effect of Continuous Epitaxy

In the previous sections, effect of surface passivation was investigated. Altough the surface recombination was suppressed, the current gain was still around 100. So we utilized a continuous growth run from the base to the emitter to suppress the interface recombination. Fig. 3.22 shows the current gain as a function of collector current for the BJTs on (0001) with 20-μm-wide fingers and $\{1\bar{1}00\}$ sidewalls grown by discontinuous and continuous runs. A higher current gain in the entire collector current range was obtained in a BJT using continuous growth. As shown in Fig. 3.23, the peak current gain in the continuously grown sample showed current gain of 257. The gain of 257 is twice as large as the previous record current gain [6, 8]. This improvement in current gain is attributed to the reduction of the recombination current at the emitter junction due to the reduction of the interface states by continuous growth as is previously reported [2, 4]. However, when we compare with the BJTs that have similar device structure and fabrication process reported by other group [11], the improvement of current gain is very significant. Since the recombination current (I_r) that limits the current gain and effective lifetime of minority carriers ($1/\tau$) can be described as

$$I_\mathrm{r} = I_\mathrm{r\_Interface} + I_\mathrm{r\_Surface} + I_\mathrm{r\_Bulk} \tag{3.9}$$

and

$$1/\tau = 1/\tau_\mathrm{surface} + 1/\tau_\mathrm{interface} + 1/\tau_\mathrm{bulk}\,, \tag{3.10}$$

we assume that not only continuous growth but also well-optimized surface passivation combined with an intentional DLR-process described in this thesis contributed to such high current gains. It should be noted that the BJT showed a clear emitter-size effect, as discussed in Section 3.4.3. A maximum current gain of 262 was obtained with a finger width of 50 μm (Fig. 3.24).

3.6.2 High Temperature Characteristics

High temperature characteristics of the BJTs with a finger width of 20 μm were investigated. Fig. 3.25 (a) shows the Gummel plots and measured current gains as a function of collector current for the BJTs at elevated temperature. The current gains were measured under $V_\mathrm{CB} = 0\,\mathrm{V}$. The current gain was calculated to be the ratio of collector current to base

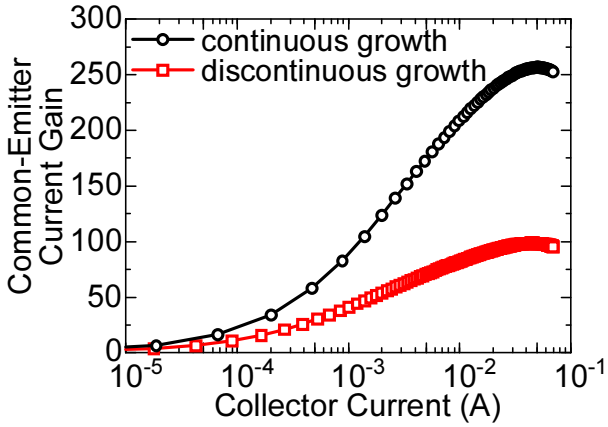

Figure 3.22: Current gains as function of collector current for BJTs with 20-μm-wide fingers and $\{1\bar{1}00\}$ sidewalls grown by discontinuous and continuous growth runs.

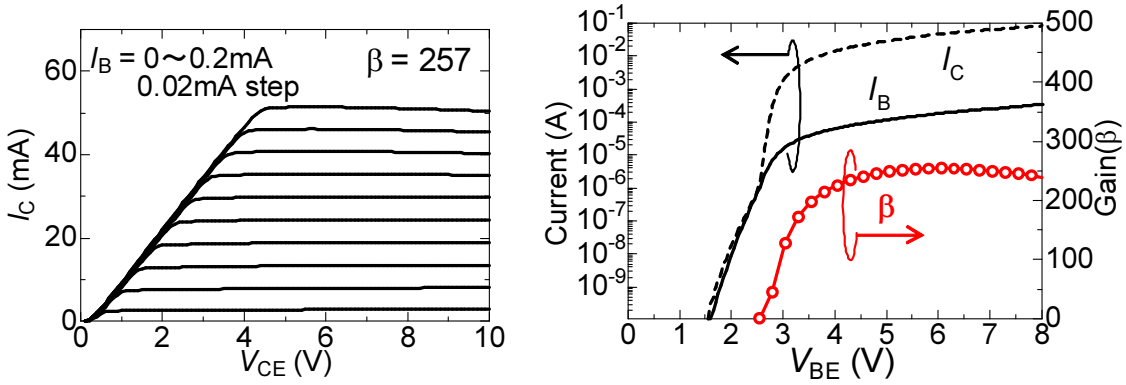

Figure 3.23: Common-emitter I_C-V_{CE} characteristics and Gummel plot of SiC BJT on (0001) with 20-μm-wide finger and $\{1\bar{1}00\}$ sidewall. Record current gain of 257 was achieved in BJT.

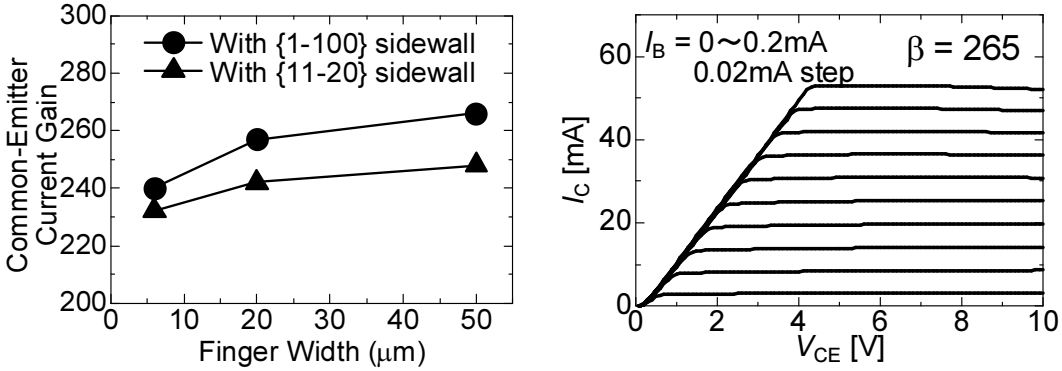

Figure 3.24: Summary of current gain of BJTs with various device geometries fabricated on (0001). Current gain increases with finger width. BJTs with $\{1\bar{1}00\}$ sidewalls exhibited higher current gain compared with those with $\{11\bar{2}0\}$ sidewalls.

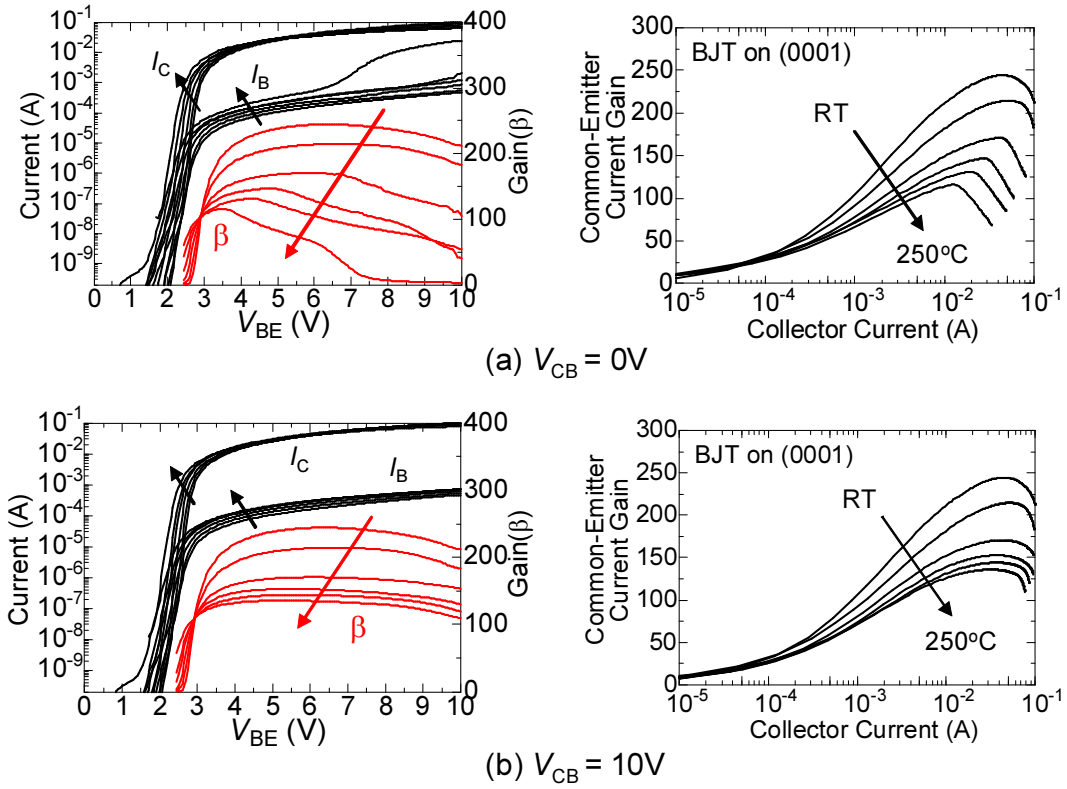

Figure 3.25: Gummel plots and current gains as a function of collector current for the BJTs at elevated temperature measured under (a) $V_{CB} = 0$ V (b) $V_{CB} = 10$ V. Current gain gradually decreased with temperature due to the activation of base acceptors. Current gain drop at lower collector current was observed due to a voltage drop across the collector.

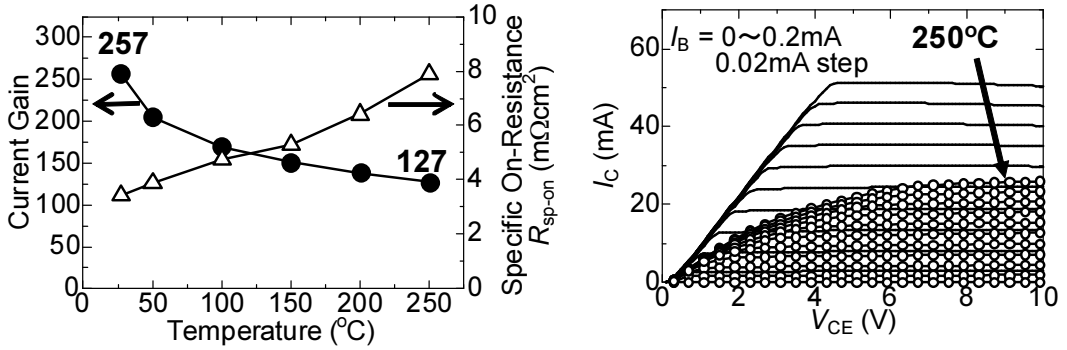

Figure 3.26: High temperature characteristics of SiC BJTs. The current gain of 257 and R_{sp_on} of 3.4 mΩcm^2 was obtained at RT, whereas the current gain of 127 and R_{sp_on} of 7.9 mΩcm^2 was achieved at 250°C.

current. We observed a tendency that the current gain gradually decreased with temperature due to the activation of base acceptors. It is worth noting that at elevated temperature, the current gain drop at lower collector current was observed. This is assume to be due to the decreased mobility and thus increased resistance in collector region, which gives rise to a voltage drop across the collector region and causes forward biasing of base-collector junction. To confirm this, we also carried out the same measurement under $V_{\mathrm{CB}} = 10\mathrm{V}$. As shown in Fig. 3.25 (b), current gain drop was not observed by appling V_{CB}, suggesting that the voltage drop across the collector which forward biases base-collector junction affected the measurements.

High temperature I_{C}-V_{CE} characteristics of the BJTs are shown in Fig. 3.26. Assuming an active area of 100 μm $\times$ 40 μm (0.004 mm^2) including contact pads, a current gain of 257 and $R_{\mathrm{sp\_on}}$ of 3.4 mΩcm^2 were obtained at RT, whereas the current gain of 127 and $R_{\mathrm{sp\_on}}$ of 7.9 mΩcm^2 were achieved at 250°C.

3.7 Utilization of (000$\bar{1}$) C-face for SiC BJTs

3.7.1 Motivation

In the previous section, record-breaking current gain was achieved in the BJTs. However, they still showed an emitter-size effect which indicates the presence of surface recombination. It is reported that lower interface state density can be obtained for SiO_2/SiC(000$\bar{1}$) structures adequately processed on (000$\bar{1}$)C-face [13], so that there is a possibility of reduction of recombination current in SiC BJT. Therefore, we attempt to utilize SiC(000$\bar{1}$)C-face to fabricate the BJTs.

3.7.2 Fabrication Process

C-face BJTs were grown in a same run as Si-face BJTs. Due to the difference of incorporation mechanisms of impurities, the base doping was reduced to 2×10^{17} cm^{-3}, whereas it was 1×10^{18} cm^{-3} on Si-face, as shown in Fig. 3.27. For the deep-level-reduction process, due to the fast oxidation rate on C-face, we utilized a short oxidation of 15 min to obtain similar oxide thickness as on Si-face.

3.7.3 Operation of SiC BJTs on (000$\bar{1}$) C-face

Fig. 3.28 shows the current gains as a function of collector current for the BJTs with 20-μm-wide fingers and $\{1\bar{1}00\}$ sidewalls fabricated on (0001) and (000$\bar{1}$). Since the doping concentration of the base layer on (000$\bar{1}$) is a factor of 5 smaller than that on (0001), the BJT on (000$\bar{1}$) enters a high injection mode at a lower collector current compared with BJTs on (0001); thus it showed a peak current gain at a lower collector current. As shown in Fig. 3.29, a very high current gain of 439 was obtained in the BJT fabricated on (000$\bar{1}$),

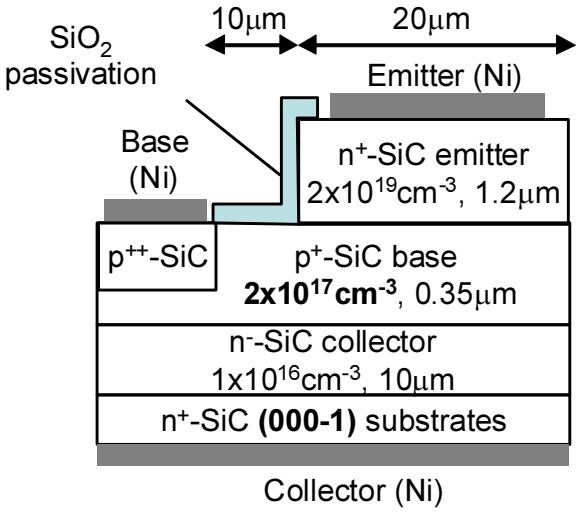

Figure 3.27: Schematic cross section of 4H-SiC BJT fabricated on $(000\bar{1})$.

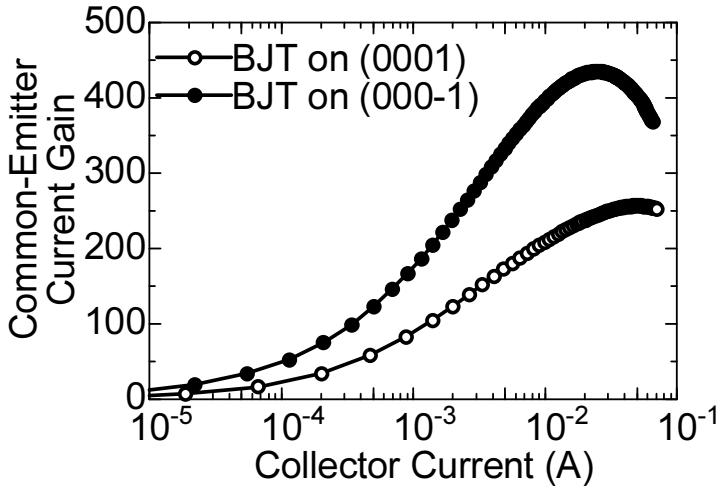

Figure 3.28: Current gains as a function of collector current for BJTs with 20-μm-wide fingers and $\{1\bar{1}00\}$ sidewalls fabricated on (0001) and $(000\bar{1})$. A very high current gain of 439 was obtained in BJT fabricated on $(000\bar{1})$.

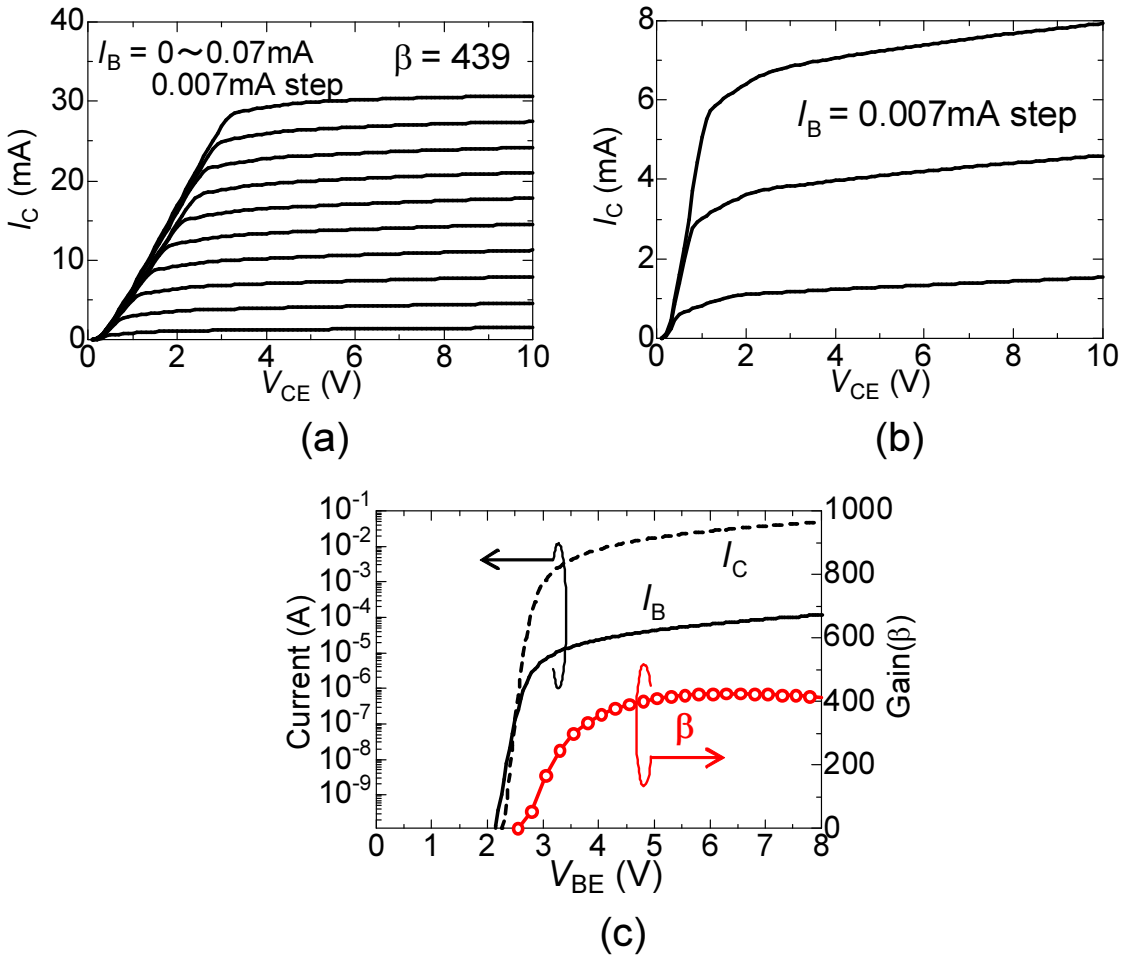

Figure 3.29: (a)(b) Common-emitter I_C-V_{CE} characteristics and (c) Gummel plot of SiC BJT on (000$\bar{1}$) with 20-μm-wide finger and $\{1\bar{1}00\}$ sidewall. Record current gain of 439 was achieved in BJT.

which is the highest value ever reported among the SiC BJTs. It should be noted that we applied the surface passivation process and DLR-process optimized for SiC(0001) thus there is still room for improvement in the fabrication processes. However, the operation of C-face BJTs with such high current gain described in this thesis indicates the future possibility of C-face BJTs.

3.7.4 High Temperature Characteristics

High temperature characteristics of the BJTs were investigated. Fig. 3.30 (a) shows the Gummel plots and measured current gains as a function of collector current for the BJTs at elevated temperature. The current gains were measured under $V_{\mathrm{CB}} = 0\,\mathrm{V}$. The current gain was calculated to be the ratio of collector current to base current. We observed a tendency that the current gain gradually decreased with temperature due to the activation of base acceptors. Current gain drop at lower collector current was observed at elevated temperature. As discussed in Section 3.6.2, this is due to the decreased mobility and thus increased resistance in collector region, which gives rise to a voltage drop across the collector region and causes forward biasing of base-collector junction. To confirm this, we also carried out the same measurement under $V_{\mathrm{CB}} = 5\,\mathrm{V}$. As shown in Fig. 3.25 (b), current gain drop was not observed by appling V_{CB}, suggesting that the voltage drop across the collector which forward biases base-collector junction affected the measurements.

High temperature I_{C}-V_{CE} characteristics of the BJTs are shown in Fig. 3.31. Assuming an active area of 100 μm $\times$ 40 μm (0.004 mm^2) including contact pads, a current gain of 439 and $R_{\mathrm{sp\_on}}$ of 4.2 mΩcm^2 were obtained at RT, whereas the current gain of 165 and $R_{\mathrm{sp\_on}}$ of 7.9 mΩcm^2 were achieved at 250°C. Although the C-face BJT is not suitable for high voltage application (> 600V) due to the low base doping, the operation of C-face BJTs with such high current gain at elevated temperature is attractive for high temperature SiC integrated circuits (ICs).

3.7.5 Reliability

It is reported that the bipolar devices can degrade when the stacking fault is included in the active region. This phenomena is so called *bipolar degradation* [36, 37]. This phenomena is caused by the expansion of stacking fault in the epilayer, which is driven by recombination of electron–hole pairs. To investigate this degradation phenomena, a C-face BJT is stressed under the condition of collector current $I_{\mathrm{C}} = 10$ mA and base current $I_{\mathrm{B}} = 0.05$ mA, corresponding to the current density of approximately 250 A/cm^2. As shown in Fig. 3.32, no degradation was observed after the stress test of 30 min. Since such degradation phenomena is observed from the early stage of stress test, it is shown that no bipolar degradation and thereby no stacking fault was observed in the C-face BJT.

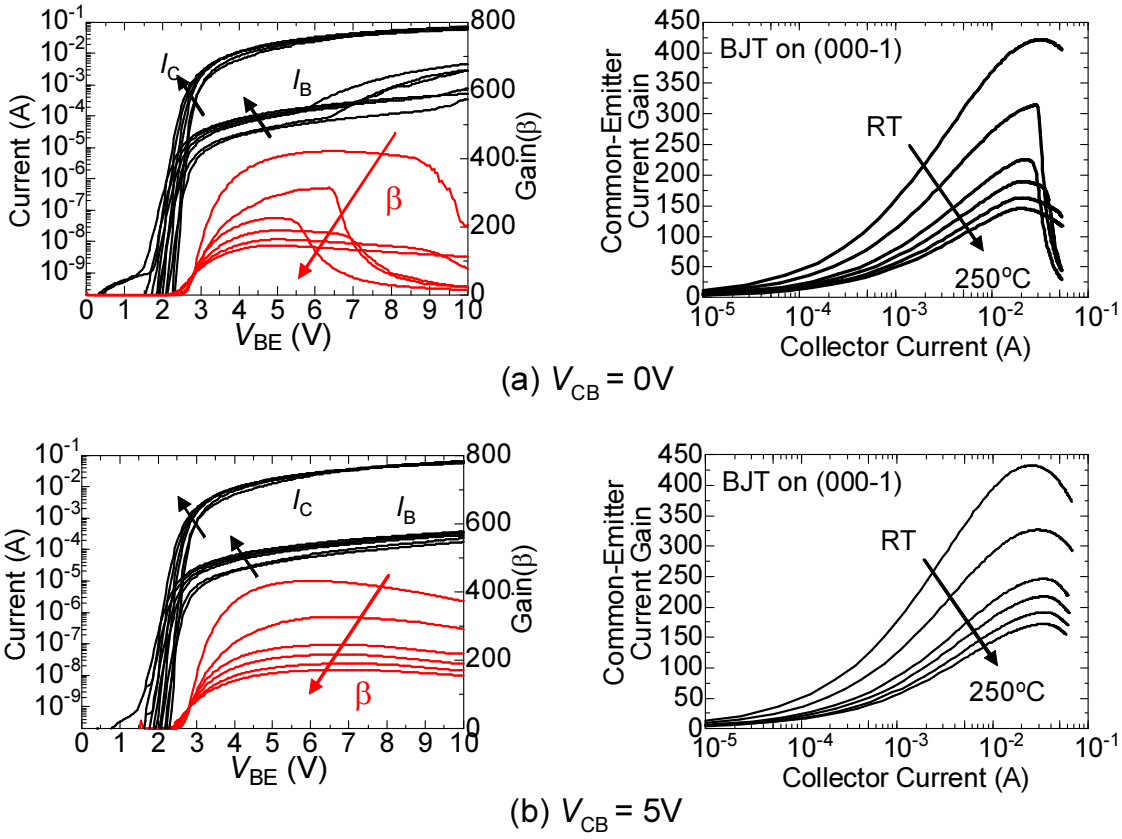

Figure 3.30: Gummel plots and current gains as a function of collector current for the BJTs at elevated temperature measured under (a) $V_{CB} = 0$ V (b) $V_{CB} = 5$ V. Current gain gradually decreased with temperature due to the activation of base acceptors. Current gain drop at lower collector current was observed due to a voltage drop across the collector.

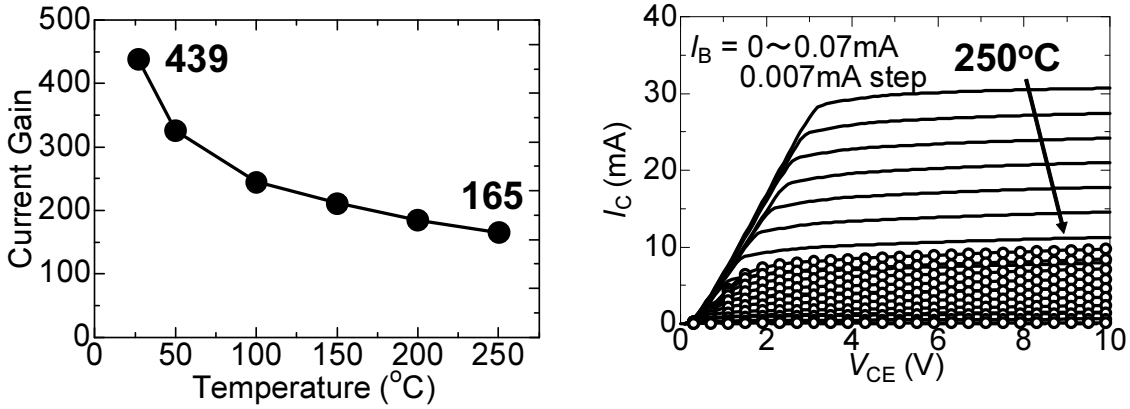

Figure 3.31: High temperature characteristics of SiC BJTs. The current gain of 439 and R_{sp_on} of 4.2 mΩcm^2 were obtained at RT, whereas the current gain of 165 and R_{sp_on} of 7.9 mΩcm^2 were achieved at 250°C.

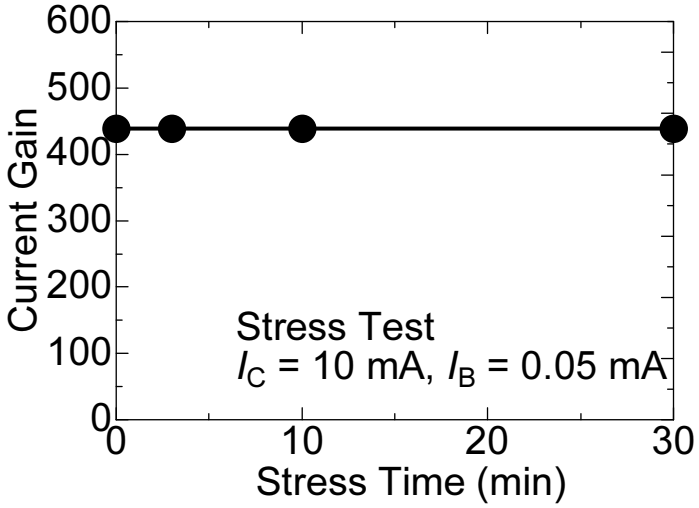

Figure 3.32: Common-emitter current gain as a function of stress time of SiC BJT on $(000\bar{1})$. Current stress of $I_C = 10$ mA and $I_B = 0.05$ mA was applied to the BJT.

3.8 17 kV 4H-SiC BJTs with Low On-Resistance

3.8.1 Motivation

Unlike Si power BJTs, SiC BJTs are free from 2nd breakdown; (1) they show a negative temperature coefficient of current gain so that they are free of forward-biased 2nd breakdown associated with thermal runway, (2) thanks to the high electric field and high electron saturation velocity in SiC, they show no reverse-biased 2nd breakdown during turn-off process and thus square safe operating area can be obtained [38]. The SiC BJTs have currently been reported in 1 kV – 10 kV range with low on-resistance close to SiC unipolar limit. Although the low current gain was one of the remaining issues, we reported a high current gain of 257 at room temperature and 127 at 250°C [31], making the BJTs more attractive as power switches.

To expand BJT applications to high voltage (∼10 kV) range, it is important to establish the proper edge termination technique to reduce the electric field crowding at the mesa edge. Currently, only a few reports on such high voltage (∼10 kV) BJTs are available [39, 40], and focused research on edge termination technique for such high voltage is necessary. Recently, we reported in PiN diodes a novel edge termination technique referred to as space-modulated junction termination extension (SM-JTE) featuring 2 zone-JTE and guard rings, which allowed us to achieve a high breakdown capability with an improved JTE dose window [41]. However, there has been no experimental study on such edge termination applied to SiC BJTs.

In this section, we report 20 kV-class SiC BJTs with SM-JTE. We investigated the impacts of the SM-JTE on the performance of SiC BJTs. In ON-state characteristics, they showed a maximum current gain of 60 and minimum specific on resistance of 242 $m\Omega cm^2$ assuming current spreading, which is below the SiC unipolar limit. In OFF-state characteristics, we achieved the open-base blocking voltage of > 17 kV (measurement system limit), which is a highest blocking voltage among SiC switching devices.

3.8.2 Design and Fabrication

Fig. 3.33 shows the schematic structure of a fabricated circular BJT. The BJT structure was grown on n-type 4H-SiC (0001) 8° off-axis substrates with a 186-μm-thick N-doped n-SiC collector ($N_d = 2.3\times10^{14}$ cm^{-3}). The theoretical breakdown voltage for this drift layer is 26.8 kV. A 0.35-μm-thick Al-doped ($N_a = 1\times10^{18}$ cm^{-3}) p^+-SiC base and a 1.2-μm-thick N-doped n^+-SiC emitter ($N_d = 2\times10^{19}$ cm^{-3}) were grown continuously in the same reactor by chemical vapor deposition. Vertical emitter mesa was formed by RIE, whereas improved bevel mesa was applied to the base to reduce the electric field crowding at the mesa edge under reverse bias [42].

Multiple Al^+ ion implantations at 500°C with an impurity concentration of 2×10^{20} cm^{-3} were carried out to form p^{++} base contact regions (depth ∼ 70 nm), whereas multiple Al^+ ion

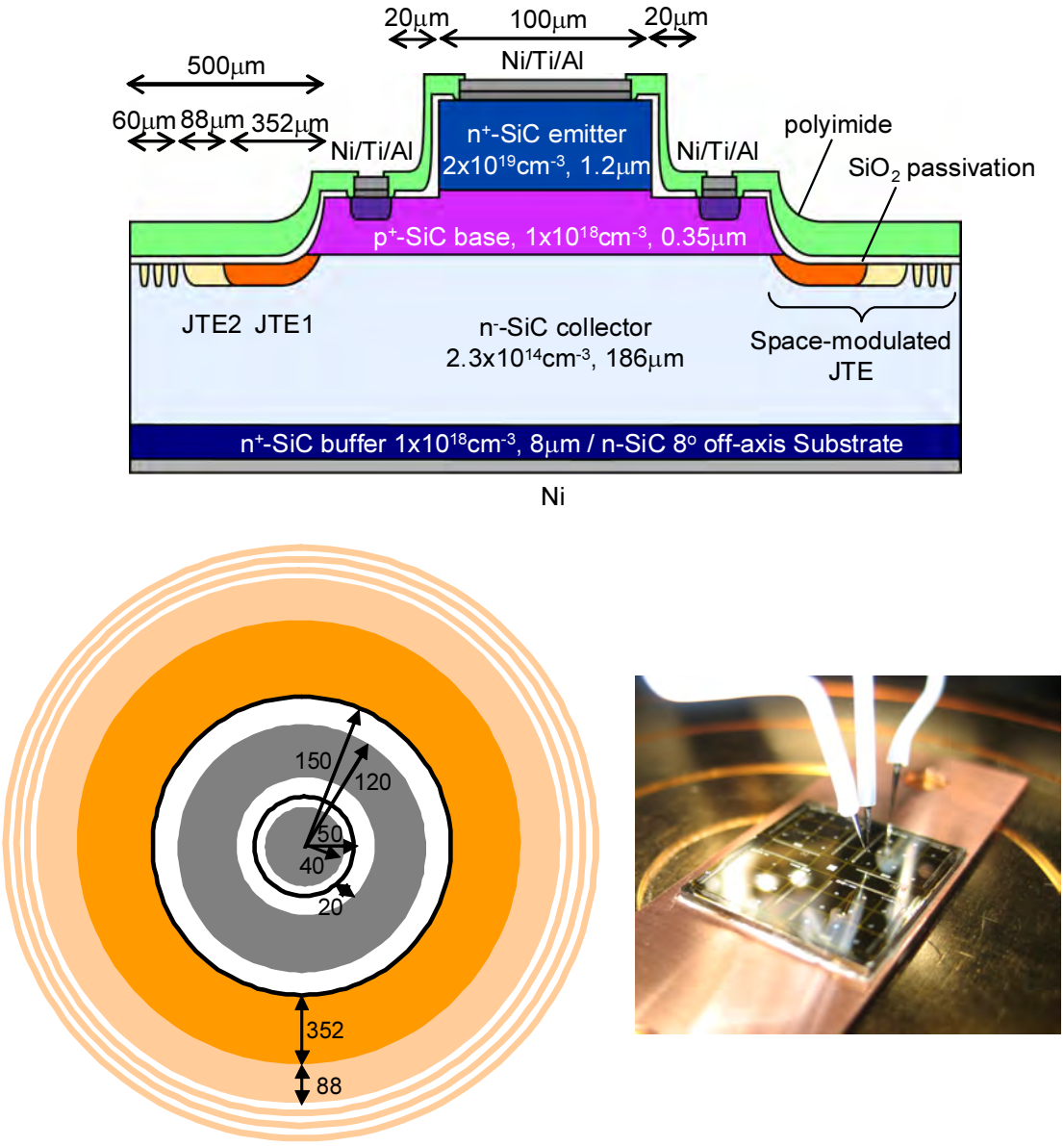

Figure 3.33: Schematic illustration and photo of fabricated ultrahigh-voltage 4H-SiC BJTs.

implantations at room temperature were performed to form JTE (depth ~ 1 μm). We employed SM-JTE (total length 500 μm) consisting of 440 μm JTE + 3 rings (10 μm-wide and 10 μm-space). The JTE dose (D_{JTE}) and JTE length (L_{JTE}) were $D_{\mathrm{JTE1}} : D_{\mathrm{JTE2}} = 3 : 2$ and $L_{\mathrm{JTE1}} : L_{\mathrm{JTE2}} = 4 : 1$, and D_{ring} was equal to D_{JTE2}. The D_{JTE1} ranged from 1.2×10^{13} cm^{-2} to 1.8×10^{13} cm^{-2}.

Subsequently, oxidation (1150°C, 5 h × 2), activation annealing of all the implants at 1700°C for 20 min in Ar, and oxidation (1150°C, 5 h × 2), which referred to as *deep-level-reduction process* [31], were performed to maximize the lifetime of p-SiC base. In addition, to achieve further reduction of deep levels, Ar annealing at 1550°C for 30 min were carried out, which is reported to be effective to eliminate the deep levels formed after the oxidation [32].

For the passivation, 30 nm-thick thermal oxides grown in 10%-diluted N_2O at 1300°C for 5 h and 80 nm-thick deposited oxides nitrided in 10%-diluted NO at 1300°C for 30 min were used in this study. Ni was deposited onto the emitter, base, and collector, and they were sintered in Ar at 800°C for 3 min followed by 950°C for 2 min. After the metallization, thick Ti/Al was deposited onto the emitter and base to reduce the voltage drop across the contact area. Finally, the surface was passivated by a polyimide to insulate the device.

3.8.3 Forward Characteristics

Fig. 3.34 shows the current gains as a function of collector current for the BJTs passivated with N_2O-grown oxide and deposited oxide nitrided in NO. The BJT passivated with N_2O-grown oxide showed a current gain of 21, whereas BJT passivated with deposited oxide nitrided in NO showed a current gain of 63. The improvement of current gain by deposited oxide + NO anneal process is attributed to the reduction of the surface recombination by utilizing improved surface passivation process [7]. Compared with [31], where the gain of 257 was obtained, the gain of 60 in this study is lower. This may be associated with the quality of very thick epilayer, which may have more number of structural defects that limits the current gain. It is worth noting that current gain drop at lower collector current was observed even at room temperature. As discussed in Section 3.6.2, this is attributed to the high resistance in collector region (N_{d} is as low as 2.3×10^{14} cm^{-3}), which gives rise to a voltage drop across the collector region and causes forward biasing of base-collector junction. By applying V_{CB}, current gain drop was suppressed, and improved characteristics were obtained.

Fig. 3.35 shows forward common-emitter current-voltage I-V characteristics of the fabricated BJT passivated with N_2O-grown oxide. The characteristics showed two different slope at low collector voltage, which corresponds to the saturation region and quasi-saturation region. The on-resistance $R_{\mathrm{sp\_on}}$ measured at 2 mA is calculated to be 55 mΩcm^2 without considering current spreading effect and 242 mΩcm^2 assuming current spreading. The $R_{\mathrm{sp\_on}}$ is below the drift resistance ($\sim$ 420 mΩcm^2) so that the conductivity modulation

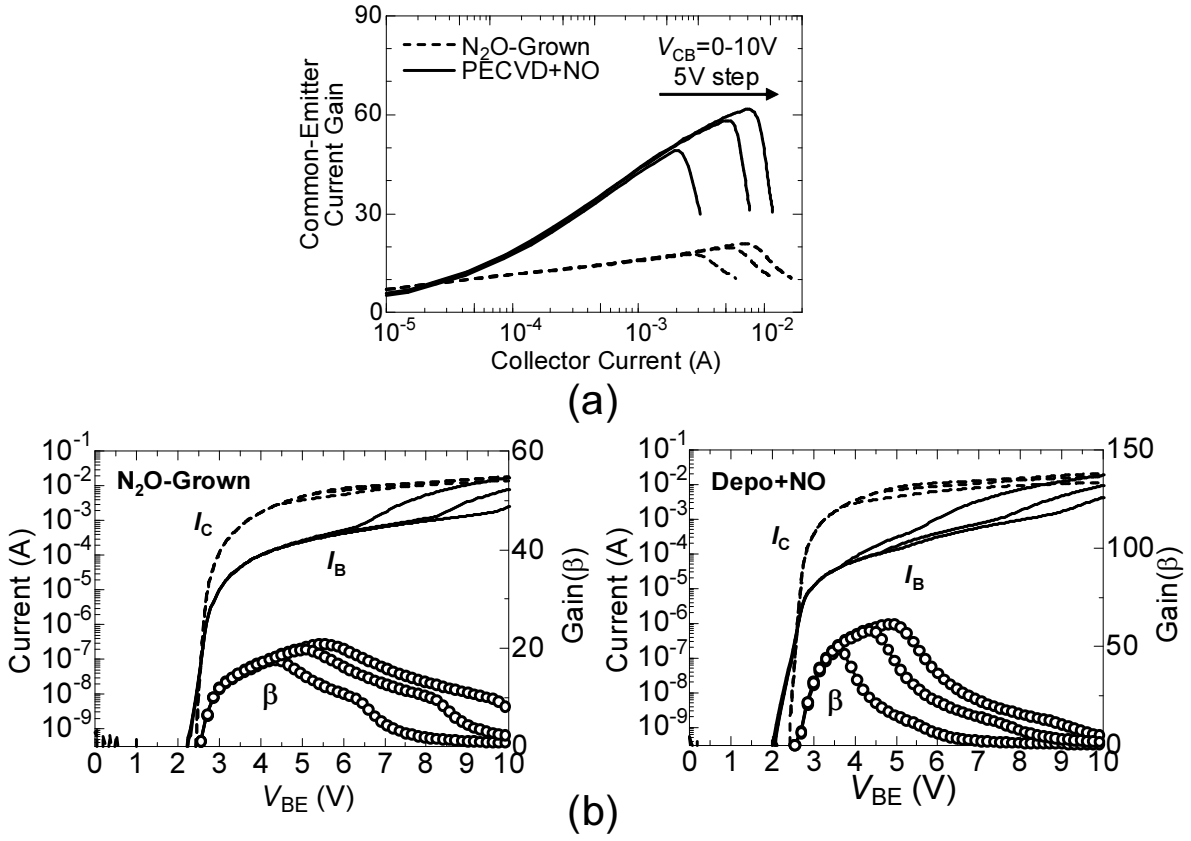

Figure 3.34: (a) Current gains as a function of collector current and (b) Gummel plots for the BJTs passivated with N_2O-grown oxide and deposited oxide nitrided in NO.

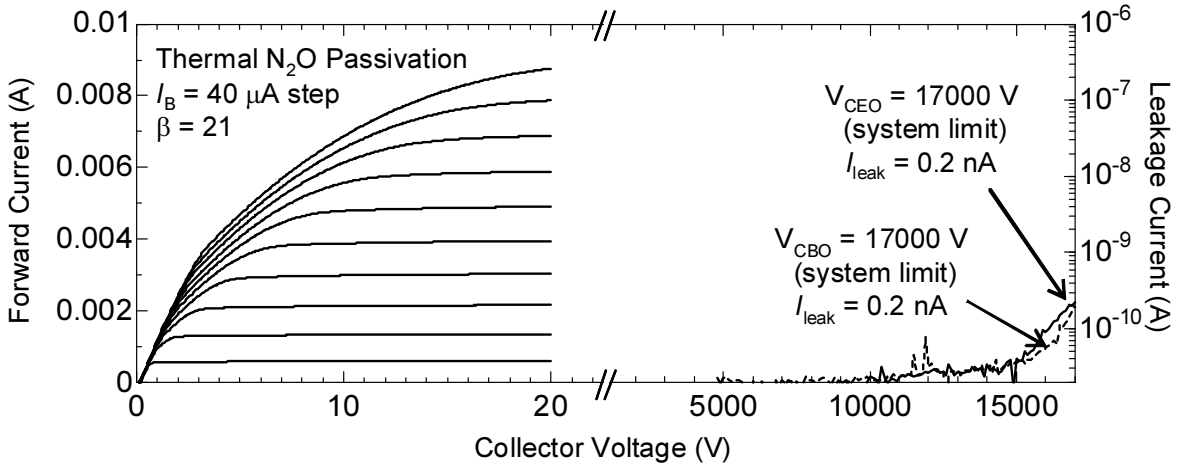

Figure 3.35: Common-emitter I_C-V_{CE} characteristics and open-base, open-emitter blocking characteristics of SiC BJT passivated by N_2O-grown oxide.

may be present, although it was not clearly seen in the saturation region since the curves with different base current overlapped each other. Likely explanation of the presence of conductivity modulation is due to the low carrier concentration in n-SiC collector while relatively high carrier concentration in p-SiC base are used to provide minority carriers to the collector. Quasi-saturation region observed only when the base current (I_B) is large can be explained by high series resistance of p-SiC base (R_B). When R_B and I_B is large, high V_{BE} is required since there is a voltage drop across the base region (emitter-base spacing used in this study is 20 μm). As a result, base-collector junction underneath the base contact region is forward biased and produces the parasitic current (Fig. 3.36), which contributes to the base current and reduces the effective current gain.

Fig. 3.37 shows forward common-emitter *I-V* characteristics of the fabricated BJT passivated with deposited oxide nitrided in NO. As shown in Fig. 3.37, the characteristics also showed saturation region and quasi-saturation region. The on-resistance R_{sp_on} measured at 2 mA is calculated to be 73 mΩcm^2 without considering current spreading effect and 321 mΩcm^2 assuming current spreading. The R_{sp_on} is below the drift resistance ($\sim$ 420 mΩcm^2) so that the conductivity modulation may be present, although it was not clearly seen in the saturation region since the curves with different base current overlapped each other.

3.8.4 Reverse Characteristics

The blocking voltage as a function of D_{JTE1} simulated with DESSIS by Synopsis^{TM} TCAD is plotted in Fig. 3.38. From the simulation, 20 kV blocking can be achieved in wide range of $D_{JTE1} = 0.8-1.6\times10^{13}$ cm^{-2} with SM-JTE. Experimental data of both open-base (V_{CEO}) and open-emitter (V_{CBO}) blocking voltage are also shown in Fig. 3.38. It is known that if a current gain is very high, the generated holes are injected into the base that triggers an emitter current multiplied by a factor of current gain. Such *transistor action* ends up with low V_{CEO}. In our BJTs investigated in this study, there is a little difference in V_{CEO} and V_{CBO}, so that such *transistor action* did not occur. This fact is favorable when the BJTs are integrated for converter or inverter applications, where base-collector diode is used as freewheeling PiN diodes [43]. Experimental data suggested the different tendency of blocking voltage with D_{JTE1} in two types of BJTs. This is attributed to the presence of interface charge at SiO_2/SiC [23]. It was reported that the positive charge at the SiO_2/SiC interface act as a space charge, which causes a effective dose shift in experimental breakdown voltage compared with the simulation.

The blocking characteristics of the BJTs with D_{JTE1} of 1.2×10^{13} cm^{-2} are shown in Fig. 3.35 and Fig. 3.37. We achieved high blocking voltage of $>$ 17 kV in both BJTs, which is, to the authors' knowledge, highest blocking voltage among SiC switching devices. It should be noted that the measurement was limited to 17 kV due to our measurement system. Since the leakage current was as low as 1 nA, we expect even high blocking voltage,

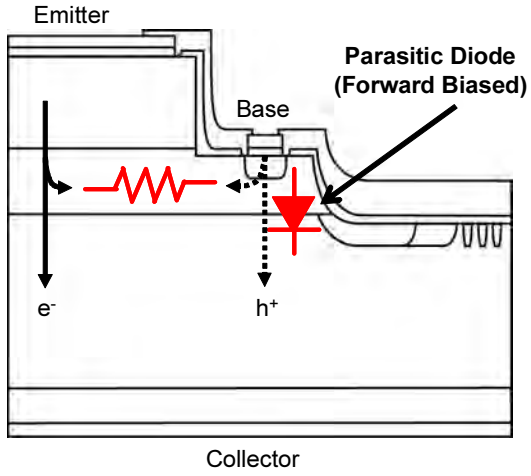

Figure 3.36: Schematic illustration of parasitic current, which contributes to the base current and reduces the effective current gain.

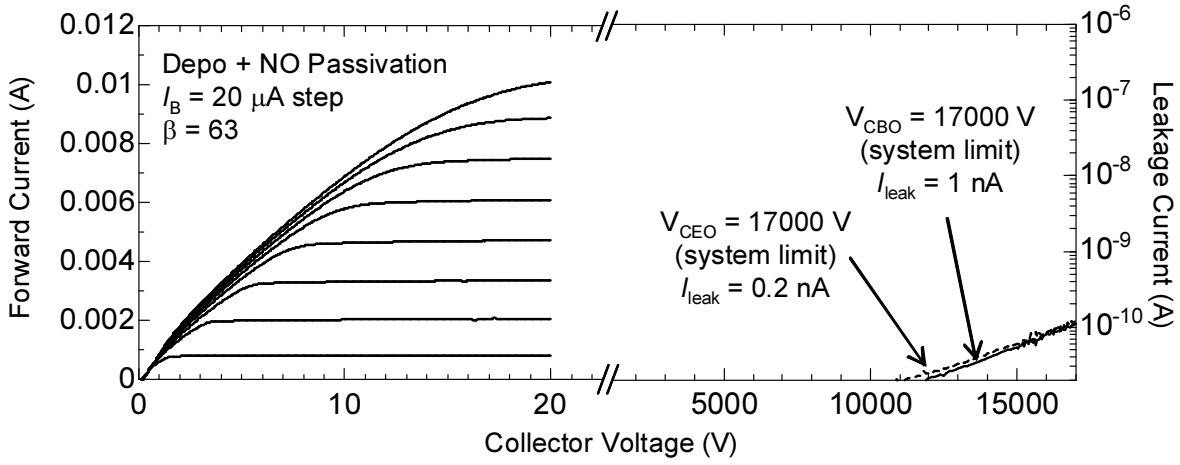

Figure 3.37: Common-emitter I_C-V_{CE} characteristics and open-base, open-emitter blocking characteristics of SiC BJT passivated by by deposited oxide annealed in NO.

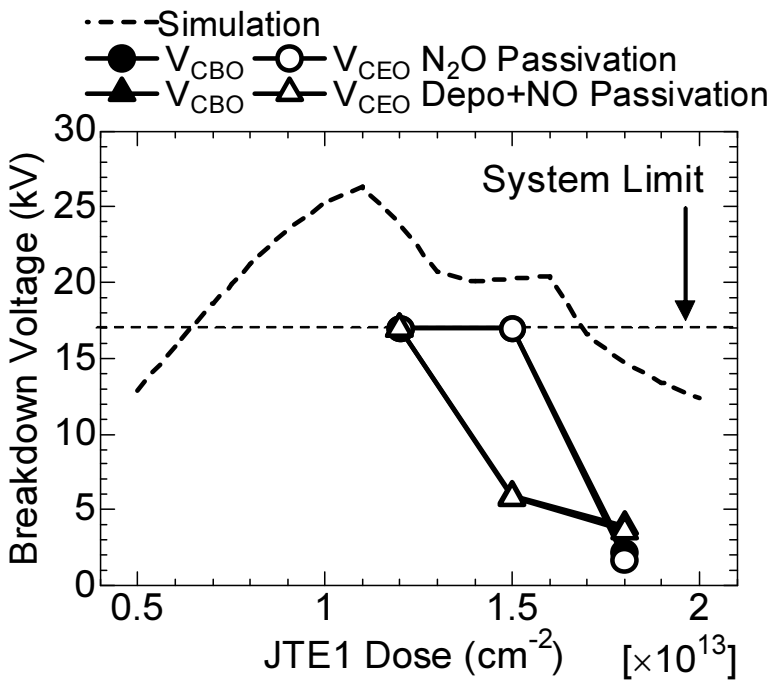

Figure 3.38: Simulated and experimental blocking voltage of 4H-SiC BJTs. Experimental data was limited to 17 kV due to our measurement setup.

which is suggested by simulation. From these results, SM-JTE can be used as an effective technology for SiC BJTs.

3.9 Comparison with Reported BJTs

The fabricated BJTs on Si-face and C-face showed current gain of 257 and 439 at room temperature. Fig. 3.39 shows the benchmark of current gain of SiC BJTs reported in literature and this study. Our results mark 2–3 times higher current gain than conventional record. This record current gain is attributed to the ultimate reduction of surface, interface, and bulk recombination as well as proper design of SiC BJTs, as investigated in this chapter. We hope that these technology investigated in this chapter will acceralate the commercial production of SiC BJTs.

3.10 Summary

In this chapter, we have investigated the suppression of surface, interface, and bulk recombination as well as proper design of SiC BJTs to improve the current gain.

We proposed the concept of deep-level-reduction process to enhance the lifetime of p-SiC base and thus suppress the bulk recombination. Then we investigated 4H-SiC BJTs passivated by deposited oxides with various post-deposition annealing processes to suppress the surface recombination. Using deposited oxides annealed in N_2O and NO, and $\{1\bar{1}00\}$ sidewall, we successfully demonstrated SiC BJTs with high current gains of 73 and 102 due to the reduced surface recombination, respectively, whereas BJTs having conventional thermally-grown oxides showed a current gain of 50.

Toward further reduction of surface recombination, we investigated effect of n-SiC surface passivation combined with high temperature HCl treatment on the current gain of 4H-SiC BJTs. With n-SiC passivation, the current gain was unexpectedly reduced from 102 to 43 due to the presence of undepleted portion of n-SiC surface passivation layer. On the other hand, following high temperature HCl treatment at 1500°C improved current gain to 82 (base thickness of 350 nm) and 115 (base thickness of 250 nm). These BJTs showed 1.0-1.5 kV blocking performance with newly developed 11-μm-deep mesa edge termination technique based on Cl_2 ICP and SiO_2 mask.

Moreover, we investigated the effect of continuous epitaxy on the current gain of SiC BJTs to reduce the interface recombination. We successfully demonstrated 4H-SiC BJTs with a record current gain of 257 at room temperature and 127 at 250°C on the (0001)Si-face, which is twice as large as the previous record gain. We assume that not only continuous growth but also well-optimized surface passivation combined with an intentional DLR-process described in this thesis contributed to such high current gains. In other

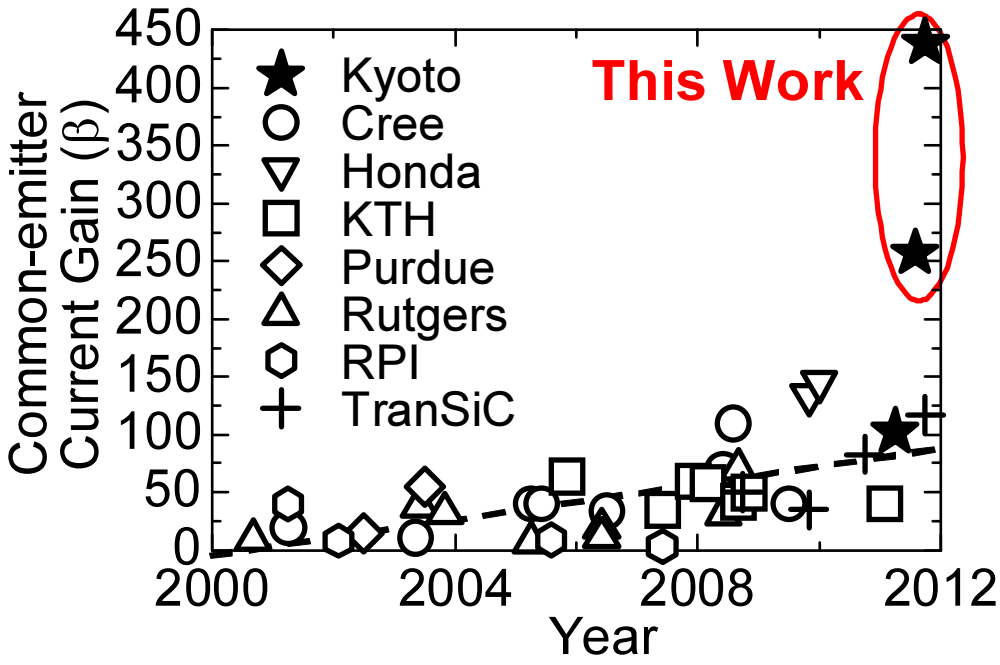

Figure 3.39: Benchmark of current gain of 4H-SiC BJTs in the past 10 years. Our results mark 2–3 times higher current gain than conventional record.

Table 3.4: Evolution of SiC BJTs investigated in this study.

Generation	1st	2nd	3rd
Emitter	2×10^{19}cm^{-3}, 1.2 μm	2×10^{19}cm^{-3}, 1.2 μm	2×10^{19}cm^{-3}, 1.2 μm
Base	1×10^{18}cm^{-3}, 0.35 μm	1×10^{18}cm^{-3}, 0.35 μm	1×10^{18}cm^{-3}, 0.25 – 0.35 μm
Collector	5×10^{15}cm^{-3}, 10 μm	5×10^{15}cm^{-3}, 10 μm	5×10^{15}cm^{-3}, 10 μm
Current Gain	35 – 73	86 – 102	51 – 140
$R_{\text{sp\_on}}$	–	–	–
V_{CEO}	600 V	600 V	1 kV – 1.5 kV
DLR-Process	Oxidation	Oxidation	Oxidation + HCl 1300–1500°C
Passivation	Depo. + N_2 Depo. + N_2O Anneal	Depo. + NO Anneal	Depo. + NO Anneal Low-Doped n-SiC
Continuous Epi	No	No	No
Edge Termination	None	None	Deep-Mesa Edge Termination
Emitter Metal	Ni	Ni	Ni
Base Metal	Ti/Al/Ni	Ni	Ni
RTA	950°C	950°C	950°C
Note			

Table 3.5: Evolution of SiC BJTs investigated in this study.

4th	5th
2×10^{19}cm^{-3}, 1.2 μm	2×10^{19}cm^{-3}, 1.2 μm
1×10^{18}cm^{-3} (Si-face), 2×10^{17}cm^{-3} (C-face), 0.35 μm	1×10^{18}cm^{-3}, 0.35 μm
1×10^{16}cm^{-3}, 10 μm	2.3×10^{14}cm^{-3}, 186 μm
257 (Si-face) – 439 (C-face)	20 – 60
3.4 mΩcm^2 (Si-face) – 4.2 mΩcm^2 (C-face)	242 – 321 mΩcm^2
600 V	17 kV (System Limit)
Oxidation	Oxidation + Ar 1550°C
Depo. + NO Anneal	N_2O-Grown Depo. + NO Anneal
Yes	Yes
None	Space-Modulated JTE
Ni	Ni + Ti/Al Overlayer
Ni	Ni + Ti/Al Overlayer
950°C	800°C → 950°C (2 step)
Record Current Gain **First Operation of C-face BJTs**	**Record Blocking Voltage**

words, surface passivation with deposited oxides annealed in NO, usage of $\{1\bar{1}00\}$ sidewalls, and continuous epitaxial growth of the emitter-base junction, combined with deep-level-reduction process based on thermal oxidation dramatically improved the current gain.

We also utilized SiC $(000\bar{1})$C-face because lower interface state density can be obtained for $SiO_2/SiC(000\bar{1})$ structures adequately processed, which may reduce the surface recombination on the p-SiC base and therefore enhance the current gains. We demonstrate degradation-free C-face BJTs showing the highest β of 439 among the SiC BJTs ever reported.

Finally, we reported 20 kV-class 4H-SiC BJTs with novel edge termination techniques referred to as space-modulated junction termination extension (SM-JTE) featuring 2 zone-JTE and guard rings. ON-state characteristics showed a current gain of 60 and $R_{\mathrm{sp\_on}}$ of 242 $\mathrm{m\Omega cm^2}$ assuming current spreading, which is below the SiC unipolar limit. We achieved BJTs with the open-base blocking voltage of > 17 kV (measurement system limit), which is highest blocking voltage among SiC switching devices.

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Chapter 4

Growth of GaN on SiC Off-Axis Surface and Fabrication of GaN/SiC Heterojunction Bipolar Transistors

4.1 Introduction

Power bipolar junction transistors (BJTs) based on SiC are very attractive candidates for high-power switching devices due to their high breakdown voltage, low ON-resistance, and high temperature operation with high current density [1]. SiC BJTs with low specific ON-resistance close to the SiC unipolar limit in a wide range of voltages have been reported in addition to attractive characteristics such as fast switching, low forward voltage drop [2, 3]. However, their low current gain remains one of the concerns, which produce large power dissipation at the base drive circuit. For practical application, the requirement for the current gain is 100 at operation temperature. Thus far a few groups have demonstrated a current gain over 100 at room temperature [4–6]. However, it falls off to about 50 at 250°C since BJTs show negative temperature coefficient of current gain. Thus, a current gain of 200 at room temperature that gives rise to a current gain of 100 at 250°C is desired.

To achieve higher current gain in SiC BJTs, utilization of heterojunction bipolar transistor (HBT) structure is one of the possible solutions for obtaining high electron injection efficiency from the n-emitter to p-base. Because it is impossible to grow Si_xC_{1-x} solid solutions with x near 0.5, bandgap engineering cannot be applied to SiC devices. Heteroepitaxial growth of wider bandgap semiconductor GaN on SiC makes it possible to utilize bandgap engineering in SiC-based devices, i.e., a higher current gain and superior high-frequency performance are expected for GaN/SiC HBTs. It is expected that the large valence band offset at the heterojunction can block hole injection from the p-SiC base to the n-GaN emitter, resulting in very high emitter injection efficiency. Fabrication of GaN/SiC HBTs was first reported by Pankove *et al.* [7] followed by several other groups [8, 9]. However, none of these HBTs offered common-emitter-mode operation due to large leakage at the

emitter junction, and focused research on n-GaN/p-SiC emitter junctions is necessary to achieve common-emitter-mode operation in the HBTs.

We have previously studied GaN/SiC HBTs [10–12]. Although common-base characteristics were obtained, the current gain was very low (1×10^{-4}). The current-voltage (I-V) characteristics revealed that the n^+-GaN/p^+-SiC emitter junction in the HBT ($N_d \sim 1\times10^{19}$ cm^{-3} for GaN, $N_a \sim 5\times10^{19}$ cm^{-3} for SiC) exhibited very leaky I-V characteristics, which is responsible for low emitter injection efficiency and low current gain in the HBTs. Therefore, control of electronic properties of n-GaN/p-SiC heterojunction is the most important factor in creating high-performance HBTs. Our previous results showed that an n^+-GaN/p^--SiC heterojunction with low acceptor doping ($N_a \sim 1\times10^{16}$ cm^{-3}) exhibited good I-V (low reverse leakage) and capacitance-voltage (C-V) characteristics [10, 11], indicating that the base doping concentration played an important role in the leakage current and emitter injection efficiency. In this paper, we have investigated the impact of base doping concentration and polytype of SiC (4H and 6H) on electronic properties of GaN/SiC heterojunction and HBTs. The GaN/4H-SiC and GaN/6H-SiC heterojunction diodes with two different base doping concentrations of 1×10^{19}cm^{-3} and 1×10^{18} cm^{-3} are fabricated and characterized. The current conduction mechanism and the band lineup of n-GaN/p-SiC heterojunction are discussed by means of current-voltage (I-V) characteristics, capacitance-voltage (C-V) characteristics, and electroluminescence (EL). Then, GaN/SiC HBTs are fabricated and characterized to clarify the impact of base doping concentration and different polytype on the current gain of GaN/SiC HBTs. We demonstrate the superior characteristics of GaN/6H-SiC HBTs with base doping of 1×10^{18} cm^{-3}. In addition to these investigations, crystal quality of MBE-grown GaN on off-axis SiC is also covered.

4.2 Device Fabrication

Fig. 4.1 illustrates the structures of fabricated heterojunction diodes as well as HBTs. The SiC substrates used in this study are commercially available 4H- or 6H-SiC (0001) wafers with off-cut angles of 8° or 3.5° toward [11$\bar{2}$0]. The p-SiC substrates with 5-μm-thick p-type homoepitaxial layers with two different acceptor concentrations (1×10^{19} cm^{-3} and 1×10^{18} cm^{-3}) were prepared for GaN/SiC heterojunction diodes, whereas the n-SiC substrates with an n-SiC collector layer (10 μm, $N_d = 8\times10^{15}$ cm^{-3}) and a p-SiC base layer (0.5 μm, $N_a = 5\times10^{19}$ cm^{-3} or $N_a = 1\times10^{18}$ cm^{-3}) were prepared for GaN/SiC HBT. Prior to GaN growth, the SiC surface was treated with high temperature HCl gas etching to obtain the smooth surface [13]. Then the air-exposed SiC surface was treated with HF solution followed by an *in-situ* Ga deposition and desorption process to remove residual oxygen from the SiC surface [14]. Subsequently, the Si-doped n^+-GaN films were directly grown on the 4H- and 6H-SiC homoepitaxial layers at 600°C by molecular beam epitaxy (MBE) using elemental Ga, Si, and rf-plasma excited active nitrogen (N*). The thickness

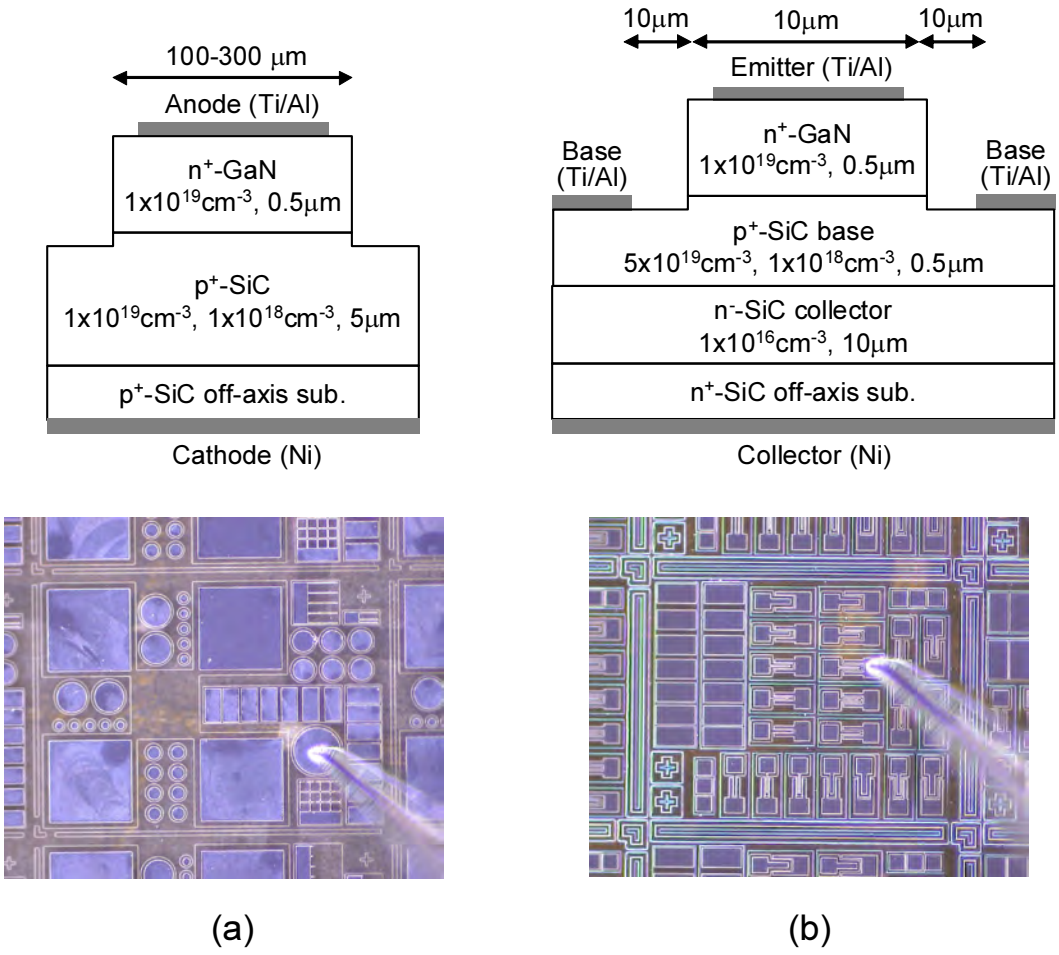

Figure 4.1: Schematic cross section and optical images of fabricated (a) GaN/SiC heterojunction diodes and (b) GaN/SiC HBTs.

of the GaN layers is 0.5 μm, and the Si donor concentration is 1×10^{19} cm^{-3}. Note that low-temperature GaN or AlN buffer layers were not used to ensure that we characterize the electronic properties of GaN/SiC heterojunction. The mesa diodes and double mesa HBTs were fabricated by using reactive ion etching (RIE). No passivation was applied to the mesa sidewalls. For heterojunction diodes, Ti/Al and Ni were deposited onto the n-GaN anode and p-SiC cathode (backside), and they were sintered in Ar at as low as 600°C to form the ohmic contacts. Here the annealing temperature was carefully chosen since a high-temperature annealing step exceeding growth temperature may increase the leakage. For HBTs, Ti/Al were deposited on the n-GaN emitter and p-SiC base, and Ni was used for n-SiC collector (backside). To achieve low base contact resistivity, metallization annealing was performed in Ar at 900°C for 10 min.

4.3 MBE Growth of GaN on Off-Axis SiC

Prior to the electrical characteristics of GaN/SiC heterojunction and HBTs, growth and characterization of MBE-grown GaN on off-axis SiC substrates are discussed. Currently, SiC homoepitaxy has been developed for (0001) off-axis SiC substrates instead of on-axis substrates because the step-controlled growth mechanism is essential to prevent formation of cubic-phase (3C-SiC) inclusions during homoepitaxy [15]. Therefore, to make the best use of the established SiC epitaxy process in GaN/SiC HBTs, growth of GaN on off-axis SiC substrates should be investigated. Although there have been a few reports of GaN growth on off-axis sapphire, notably [16], the investigation is limited to relatively low off-angle of up to 2°, whereas a large off angle of 8° for 4H-SiC or 3.5° for 6H-SiC toward the [11$\bar{2}$0] direction is generally used in SiC technology. In this section, MBE growth of GaN on SiC off-axis substrates is investigated by means of atomic forced microscopy (AFM), X-ray diffraction (XRD), transmission electron microscopy (TEM), and photoluminescence (PL).

4.3.1 Surface Morphology

Fig. 4.2 shows the surface morphologies of GaN grown on 6H-SiC on-axis surface. The surface morphology of 6H-SiC on-axis substrate treated with high temperature HCl gas etching before the GaN growth is also shown as a reference. As shown in Fig. 4.2, 6H-SiC on-axis substrate treated with HCl gas etching showed a step-and-terrace structure corresponding to a unit height of 6 bilayers (6BL) of 6H-SiC, and root mean square (RMS) roughness was 0.56 nm. When we grow GaN on this surface, we get a surface morphology showing a lot of spiral hillocks that are associated with screw dislocations [17]. The number of spiral hillocks is about 10^9-10^{10}cm^{-2}.

Fig. 4.3 shows the surface morphologies of GaN grown on 6H-SiC 3.5° off-axis surface and 4H-SiC 8° off-axis surface. The growth condition is the same as that of on-axis epitaxy. SiC surface treated with high temperature gas etching before the GaN growth is also shown

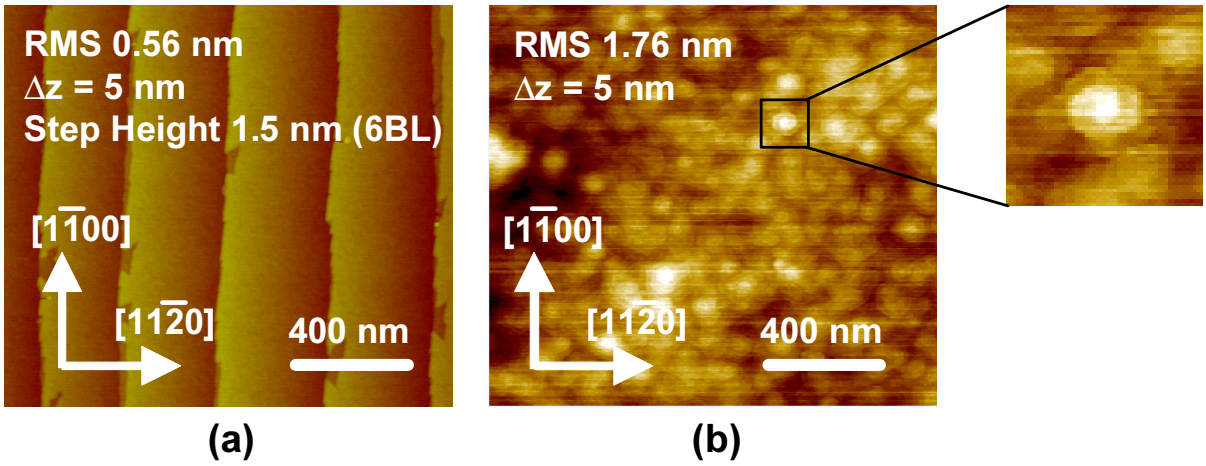

Figure 4.2: Surface morphologies of (a) 6H-SiC on-axis substrate treated with high temperature gas etching before the GaN growth and (b) GaN grown on 6H-SiC on-axis surface.

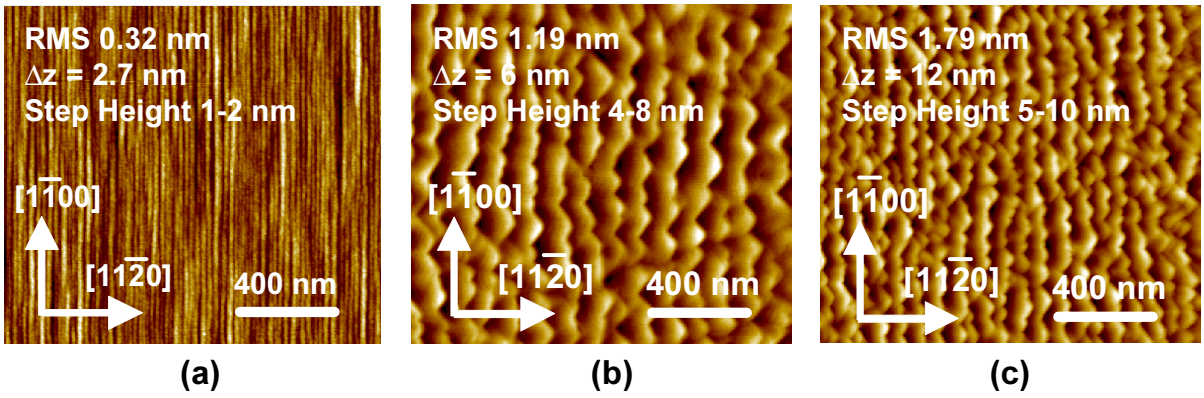

Figure 4.3: Surface morphologies of (a) 4H-SiC off-axis substrate treated with high temperature gas etching before the GaN growth, (b) GaN grown on 6H-SiC 3.5° off-axis surface, and (c) GaN grown on 4H-SiC 8° off-axis surface.

as a reference. As shown in Fig. 4.3 (a), 4H-SiC off-axis substrate treated with HCl gas etching showed steps with step height of 1–2 nm, corresponding to one or two unit height (4 or 8BL) of 4H-SiC, although there is a possibility of underestimation of step height since the terrace width is as small as 20 nm. RMS roughness of the surface was 0.32 nm, indicating a smooth surface was obtained, although the HCl gas etching was previously developed for SiC on-axis surface. When we grow GaN on this surface, we get a rough surface morphology showing step bunching (RMS roughness of 1.19 nm and 1.79 nm for GaN on 6H-SiC 3.5° off-axis and on 4H-SiC 8° off-axis surface, respectively). The step height was 4–8 nm for GaN on 6H-SiC 3.5° off-axis surface and 5–10 nm for GaN on 4H-SiC 8° off-axis surface. The number of bunched steps was larger in GaN on the 4H-SiC 8° off-axis sample due to the large off-angle of the substrates. In addition, GaN on 4H-SiC 8° off-axis substrate showed rougher morphology and larger step height than those on 6H-SiC 3.5° off-axis substrates, indicating that large off-angle is responsible for the origin of the step bunching and thereby rougher surface morphology.

4.3.2 XRD and TEM analysis

To further investigate the quality of MBE-grown GaN on off-axis SiC, XRD, and TEM analyses were conducted. Table 4.1 shows the full width at half maximum (FWHM) of (0002) and $(1\bar{1}02)$ reflection peaks in the ω scan of XRD measurements. FWHM of 742 arcsec for (0002) and 1397 arcsec for $(1\bar{1}02)$ were obtained for GaN grown on 6H-SiC on-axis substrates, whereas much reduced (0002), $(1\bar{1}02)$ FWHM of 43, 770 arcsec for GaN on 6H-SiC off-axis and 97, 936 arcsec for GaN on 4H-SiC off-axis substrates were obtained. Judging from the fact that the FWHM of (0002) and $(1\bar{1}02)$ reflection peaks indicate the number of screw and edge dislocations, respectively [18], the reduction of FWHM value indicates that the use of off-angle is effective for reducing both screw and edge dislocations. To clarify what mechanism reduced the dislocations, TEM observation was conducted. Fig. 4.4 shows a cross-sectional TEM image of GaN grown on 4H-SiC off-axis surface. The TEM image was taken from $[1\bar{1}00]$ direction (zone-axis). It was observed that large number of dislocations generated at the initial stage of growth due to the lattice mismatch between GaN and SiC ($\sim$ 3%), and they vended toward step bunched surface due to the step-flow growth. We found that annihilation of dislocations occurred mostly at the initial growth stage due to the dislocation vending toward step bunched surface. At the surface, most edge dislocations disappear thanks to this step-bunching-induced annihilation. It is reported that GaN grown on vicinal sapphire showed reduced FWHM in $(1\bar{1}02)$ ω scan by introducing off-angle of up to 2°, and TEM observation revealed the reduced FWHM was obtained because the step-bunching-induced annihilation of edge dislocations occurred [16]. We assume that the similar phenomena occurred in our GaN grown on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis surface. From both XRD and TEM analysis, we conclude that the quality of GaN is improved by using off-axis substrates, although further improvement of

Table 4.1: FWHM of (0002) and $(1\bar{1}02)$ reflection peak in ω scan of XRD measurement.

Substrate	FWHM in ω scan of XRD measurement.	
	(0002) reflection	$(1\bar{1}02)$ reflection
6H-SiC on-axis	742 arcsec	1397 arcsec
6H-SiC 3.5° off-axis	43 arcsec	770 arcsec
4H-SiC 8° off-axis	97 arcsec	936 arcsec

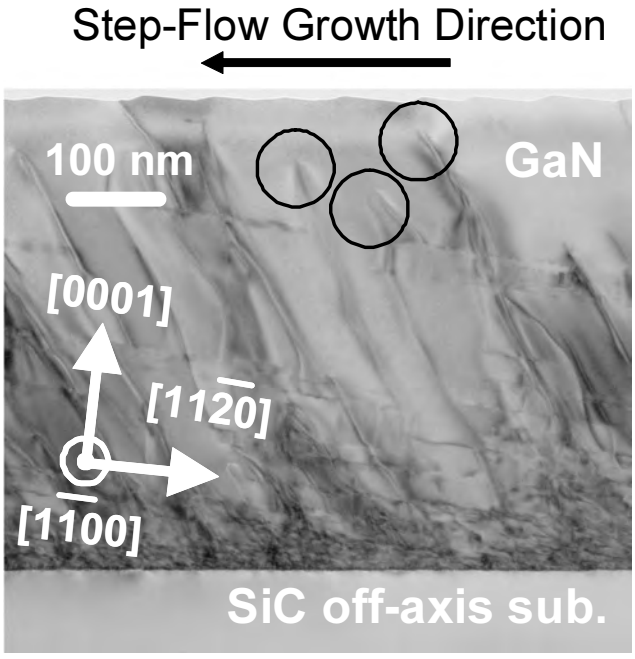

Figure 4.4: Cross-sectional TEM image of GaN grown on 4H-SiC off-axis surface (zone-axis). Dislocations generated at initial stage of growth vended toward step-bunched surface due to the step-flow growth and were annihilated thanks to the step-bunching-induced annihilation.

crystal quality is necessary especially near the GaN/SiC heterointerface since it affects the electronic properties of GaN/SiC heterojunction diodes and HBTs.

4.3.3 Photoluminescence

To further investigate the quality of GaN grown on off-axis SiC, PL measurement was conducted. Fig. 4.5 shows PL spectra of undoped GaN grown on 6H-SiC on-axis, 6H-SiC 3.5° off-axis, and 4H-SiC 8° off-axis substrates. The PL spectra were recorded at 4.2 K. The PL spectra taken at RT were also shown as a reference. In the case of GaN grown on 6H-SiC on-axis substrates, we observed one major peak labeled as D°X (3.46 eV) and three minor centers labeled as Y_2 (3.42 eV), Y_7 (3.21 eV), and Y_8 (3.08 eV), according to the literature [19, 20]. According to [19, 20], these centers are associated with donor bound exciton (DBE), exciton bound to structural defect at the surface, exciton bound to structural defect, and strongly localized exciton, respectively. In the case of GaN grown on off-axis SiC substrates, the peak intensity of D°X was unchanged, but we observed the increase of peak intensity of Y_7 center, indicating that the GaN on off-axis SiC includes larger number of structural defects. Also, we observed a new center, namely, Y_6 (3.32 eV), which is reported to be donor-acceptor pair (DAP) emission. We found the tendency that the peak intensity of the Y_6 center increased when the GaN is doped by Si. In other words, Y_6 center reflects the incorporation of Si. Although the GaN samples investigated in this study were undoped, the donor concentrations were as high as 6×10^{17} cm^{-3} and 2×10^{18} cm^{-3} on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates, respectively. So we assume the background doping of Si contributed to the advent of Y_6 peak, and lower peak intensity of Y_6 in GaN on 6H-SiC 3.5° off-axis substrates may be attributed to the lower background doping.

4.3.4 Hall Effect Measurement

Electronic properties of GaN grown on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates are characterized by Hall-effect measurements. Built-in, mesa-isolated van der Pauw geometry pattern in n-GaN/p-SiC heterojunction diode structure ($N_a = 1\times10^{18}$ cm^{-3}) are used for Hall-effect measurements. Fig. 4.6 (a) shows temperature dependence of carrier concentrations of undoped- and Si-doped GaN grown on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates. The Si-doping was performed at the same cell temperature of 1300°C for both GaN on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates. In the case of undoped-GaN, the carrier concentrations at 300 K were 3×10^{17} cm^{-3} and 1×10^{18} cm^{-3} on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates, respectively. From the temperature dependence, the ionization energy (ΔE_d) and concentration (N_d) are calculated to be 28 meV and 6×10^{17} cm^{-3} on off-axis 6H-SiC, and 0.2 meV and 2×10^{18} cm^{-3} on off-axis 4H-SiC. On the other hand, in the case of Si-doped GaN, the carrier concentrations at 300 K

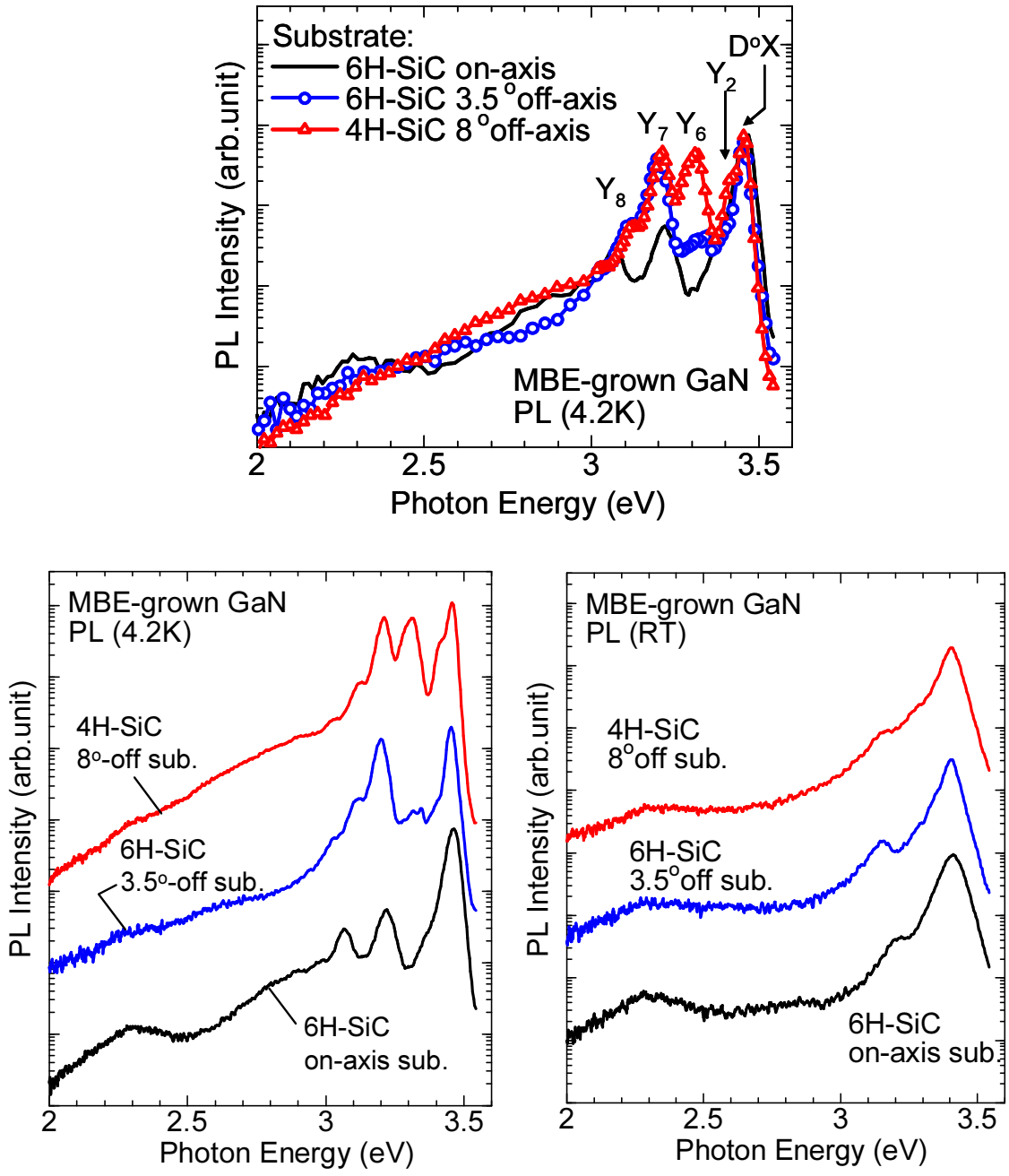

Figure 4.5: PL spectra of GaN grown on 6H-SiC on-axis, 6H-SiC 3.5° off-axis, and 4H-SiC 8° off-axis substrates taken at 4.2 K and RT.

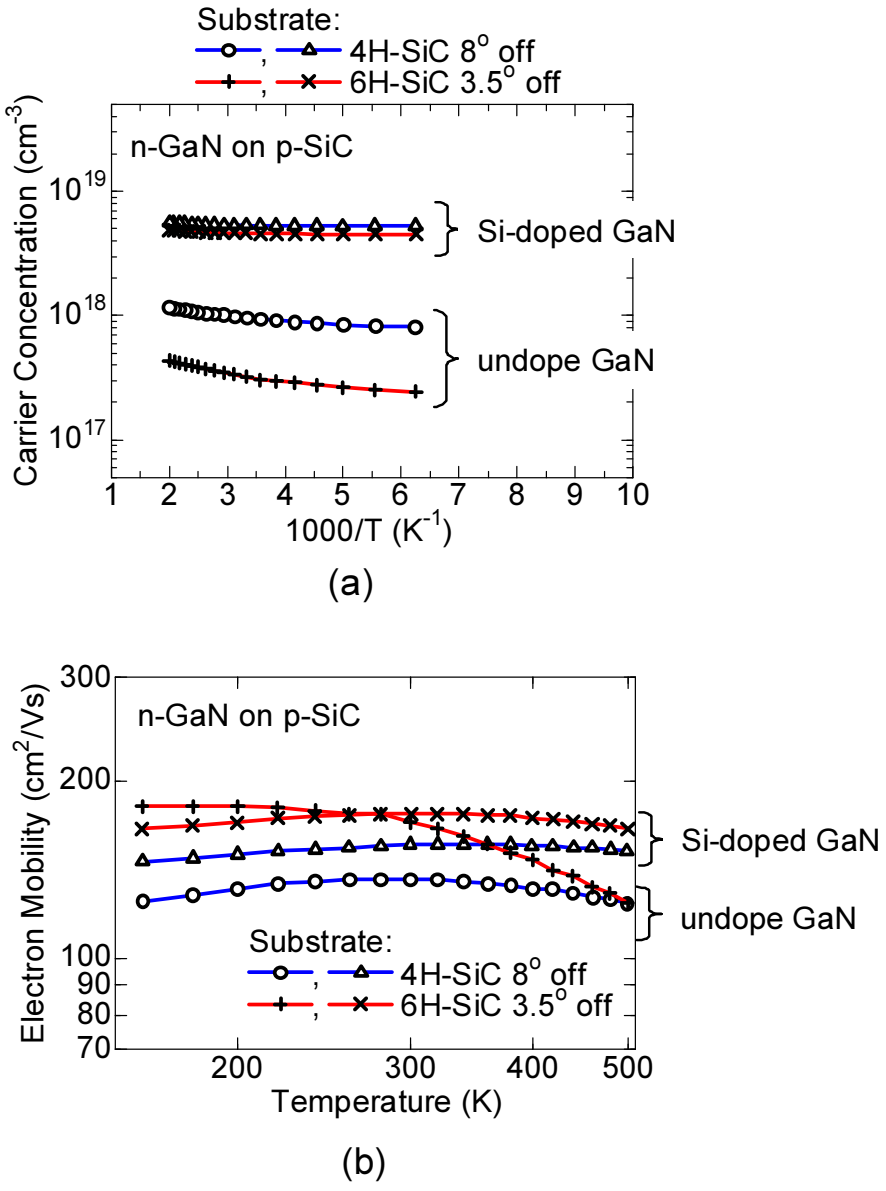

Figure 4.6: Temperature dependence of (a) carrier concentrations and (b) electron mobility of undoped- and Si-doped GaN grown on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates.

were 5×10^{18} cm^{-3} on both 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates, and they did not show temperature dependence so that Si-doped GaN are degenerated.

Fig. 4.6 (b) shows temperature dependence of electron mobility of undoped- and Si-doped GaN grown on 6H-SiC 3.5° off-axis and 4H-SiC 8° off-axis substrates. In the case of undoped-GaN, the electron mobility at 300 K was 172 cm^2/Vs on off-axis 6H-SiC and 136 cm^2/Vs on off-axis 4H-SiC, respectively. The electron mobility showed slight temperature dependence at high temperature over 300 K, indicating that impurity scattering is one of the dominant factor limiting the electron mobility. In contrast, in the case of Si-doped GaN, the electron mobility at 300 K was 176 cm^2/Vs on off-axis 6H-SiC and 156 cm^2/Vs on off-axis 4H-SiC, respectively, and they did not show temperature dependence because Si-doped GaN are degenerated. When comparing the mobility in GaN on off-axis 6H-SiC and off-axis 4H-SiC, GaN on off-axis 4H-SiC showed lower mobility. It is reported that the mobility in GaN can be limited by impurity scattering as well as dislocations that have an edge component [21]. This is because edge dislocations introduce acceptor centers along the dislocation lines that capture electrons (negatively charged) and form a space-charge, which scatters electrons crossing them. In our GaN, XRD measurement showed that FWHM of $(1\bar{1}02)$ reflection peak, which reflects the number of dislocations that have edge components [18], was larger in GaN on off-axis 4H-SiC compared with that on off-axis 6H-SiC. So we assume the larger number of edge dislocations contributed to the reduced mobility in the case of GaN on off-axis 4H-SiC. However, the GaN layer still shows adequate mobility as well as carrier concentration, so we conclude that GaN on off-axis SiC substrate is applicable for the emitter of GaN/SiC HBTs.

4.4 GaN/SiC Heterojunction Diodes

4.4.1 Band Offset at GaN/SiC Heterojunction

To reveal band diagram at the GaN/SiC heterojunction, capacitance-voltage (C-V) measurements were performed. Fig. 4.7 shows typical C-V characteristics of GaN/4H-SiC and GaN/6H-SiC diodes with $N_\mathrm{a} = 1\times10^{18}$ cm^{-3}. The slopes of the $1/C^2$-V plot agreed well with the acceptor concentration of p-SiC layers. Built-in voltages (V_d) were extracted from the $1/C^2$–V plots, and they were 2.33 V for n$^+$-GaN/p-4H-SiC and 2.15 V for n$^+$-GaN/p-6H-SiC. From this V_d value, the energy-band diagrams of the SiC/GaN pn heterostructure were estimated as shown in Fig. 4.8. Here, the valence and conduction band offsets are calculated from V_d using a simple model:

$$\Delta E_\mathrm{v} = E_\mathrm{g,GaN} - qV_\mathrm{d} - \delta_\mathrm{SiC} - \delta_\mathrm{GaN} \tag{4.1}$$

$$\Delta E_\mathrm{c} = qV_\mathrm{d} - E_\mathrm{g,SiC} + \delta_\mathrm{SiC} + \delta_\mathrm{GaN} \tag{4.2}$$

where E_g is the bandgap energy, and δ_SiC and δ_GaN are the differences between the

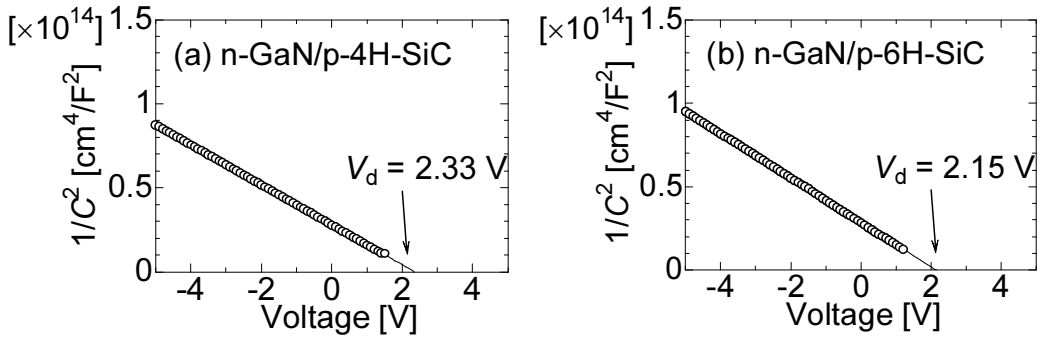

Figure 4.7: Room temperature C-V characteristics of (a) n^+-GaN/p-4H-SiC and (b) n^+-GaN/p-6H-SiC diode ($N_d = 1\times10^{19}cm^{-3}$ and $N_a = 1\times10^{18}cm^{-3}$).

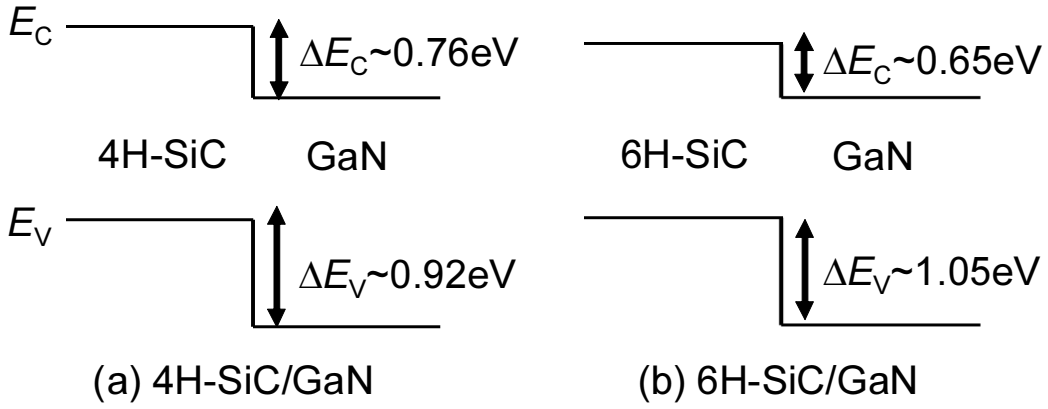

Figure 4.8: Energy-band diagrams of (a) 4H-SiC/GaN, (b) 6H-SiC/GaN heterojunctions as calculated on the basis of the built-in voltages in C–V measurements.

Fermi level and the valence-band maximum of SiC and conduction-band minimum of GaN, respectively. We used the values of $\delta_{\mathrm{GaN}} = -0.02$ eV ($n \sim 5{\times}10^{18}$ cm^{-3}) and $\delta_{\mathrm{SiC}} = 0.16$ eV ($p \sim 5{\times}10^{16}$ cm^{-3}), respectively.

The C-V analysis revealed that there is a large valence band offset (0.92 eV for 4H-SiC/GaN and 1.05 eV for 6H-SiC/GaN) that sufficiently blocks hole back injection from p-SiC to n-GaN. However, there is also a large conduction band offset (0.76 eV for 4H-SiC/GaN and 0.65 eV for 6H-SiC/GaN), which works as a potential barrier to electron and hinders electron injection from p-SiC to n-GaN. Since this band diagram (so called type-Ⅱ) is not suitable for HBTs, this indicates that the band offset control of the heterojunction will be required for high electron injection efficiency. When comparing these two heterojunctions (4H-SiC/GaN and 6H-SiC/GaN), the conduction band offset of the 6H-SiC/GaN heterojunction is smaller than that of 4H-SiC/GaN, so the 6H-SiC/GaN heterojunction may be better for the emitter of the HBTs.

4.4.2 Current Transport Properties of GaN/SiC Heterojunction

The GaN/4H-SiC and GaN/6H-SiC heterojunction diodes with two different base doping concentrations of $1{\times}10^{19}$ cm^{-3} and $1{\times}10^{18}$ cm^{-3} are fabricated and characterized. The temperature dependencies of the I-V characteristics of n$^+$-GaN/p$^+$-4H-SiC and n$^+$-GaN/p$^+$-6H-SiC with $N_{\mathrm{a}} = 1{\times}10^{19}$ cm^{-3} are shown in Fig. 4.9. The measurement temperature ranged from 200 K to 500 K. Large leakage current was observed in both diodes, which is consistent with an emitter junction of a GaN/SiC HBT with $N_{\mathrm{a}} = 5{\times}10^{19}$ cm^{-3} reported earlier [2]. Large leakage current is observed even close to zero-bias voltage at various temperatures. Under forward bias, I-V characteristics show weak temperature dependence, and the ideality factor (n) at 300 K is larger than 2 ($n \sim 2.8$ for 4H and $n \sim 2.1$ for 6H), suggesting that the dominant current transport is associated with tunneling. Fig. 4.10 shows the temperature dependencies of the I-V characteristics of n$^+$-GaN/p-4H-SiC and n$^+$-GaN/p-6H-SiC with $N_{\mathrm{a}} = 1{\times}10^{18}$ cm^{-3}. In contrast to the diodes with $N_{\mathrm{a}} = 1{\times}10^{19}$ cm^{-3}, leakage current was significantly suppressed in the measured voltage range, and it was almost negligible at the measured voltage range even at 500 K. Under forward bias, I-V characteristics show stronger temperature dependence and the ideality factors at 300 K are smaller than 2 ($n \sim 1.6$ for 4H and $n \sim 1.4$ for 6H), indicating that the dominant current transport mechanism is not related to tunneling but to the diffusion process. By utilizing reduced doping of $N_{\mathrm{a}} = 1{\times}10^{18}$ cm^{-3}, we successfully demonstrate heterojunction diodes with low leakage and smaller ideality factor so that these diodes seem to be promising for the emitter junction of the HBTs.

To explain why the doping concentration affected electronic properties of GaN/SiC heterojunction diodes, the current transport mechanism is investigated from the viewpoint of band diagram. Fig. 4.11 shows schematic illustrations of the n-GaN/p-SiC heterojunction with two different doping concentrations and the calculated width of depletion layers under

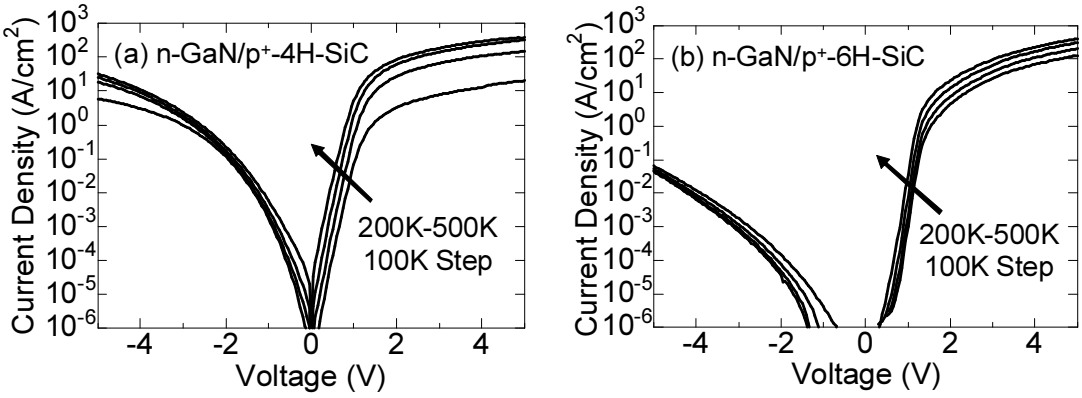

Figure 4.9: *I-V* characteristics of (a) n^+-GaN/p^+-4H-SiC and (b) n^+-GaN/p^+-6H-SiC heterojunction diodes ($N_d = 2\times10^{19}$ cm^{-3} , $N_a = 1\times10^{19}$ cm^{-3}) measured at 200 K–500 K.

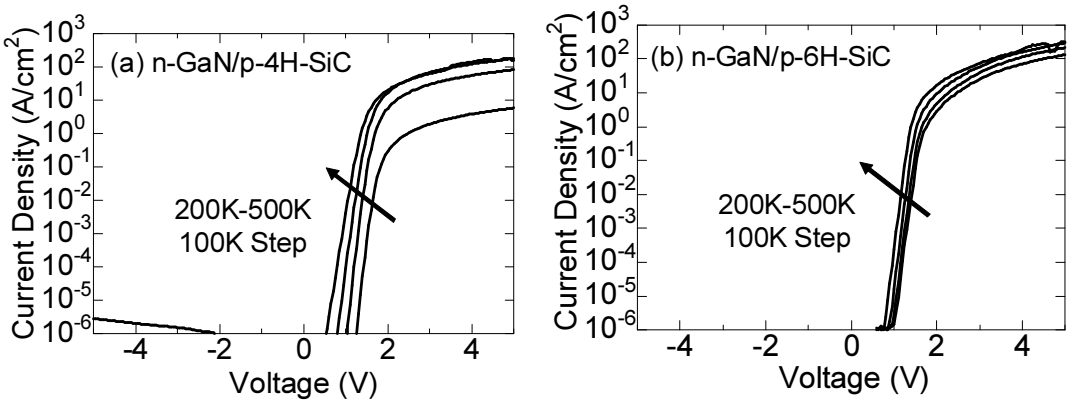

Figure 4.10: *I-V* characteristics of (a) n^+-GaN/p-4H-SiC and (b) n^+-GaN/p-6H-SiC heterojunction diodes ($N_d = 1\times10^{19}$ cm^{-3}, $N_a = 1\times10^{18}$ cm^{-3}) measured at 200 K–500 K.

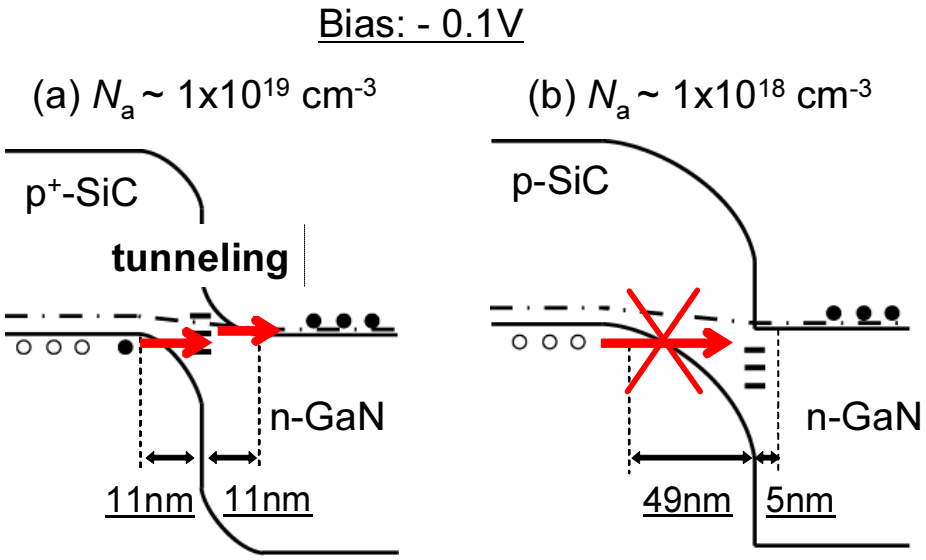

Figure 4.11: Schematic band diagrams of n$^+$-GaN/p-SiC with (a) $N_a = 1\times10^{19}$ cm^{-3} and (b) $N_a = 1\times10^{18}$ cm^{-3} under reverse bias of 0.1 V.

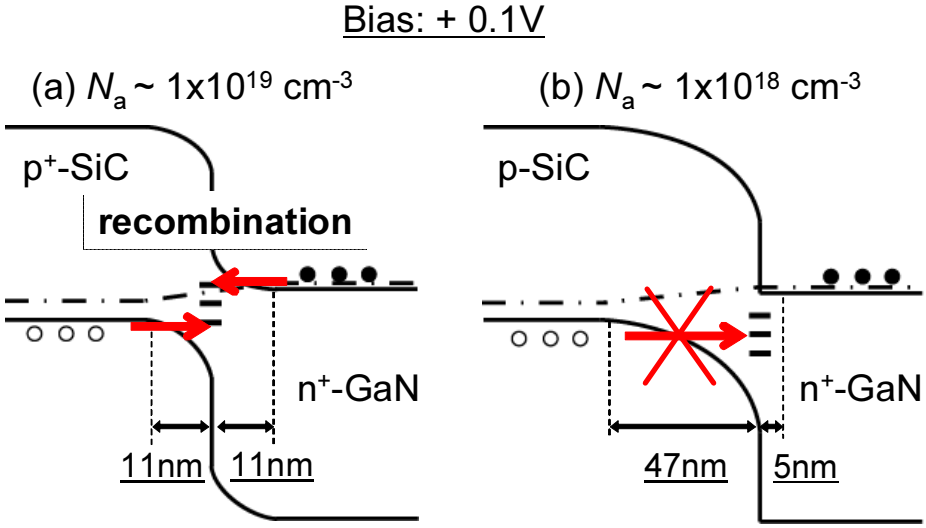

Figure 4.12: Schematic band diagrams of n$^+$-GaN/p-SiC with (a) $N_a = 1\times10^{19}$ cm^{-3} and (b) $N_a = 1\times10^{18}$ cm^{-3} under forward bias of 0.1 V.

reverse bias of 0.1 V. In the case of $N_a = 1\times10^{19}$ cm^{-3}, the calculated depletion layer is as thin as 11 nm so that it is thin enough for carriers to tunnel from p-SiC to n-GaN via interface traps under reverse-bias condition. Thus, we observed large leakage current under reverse bias. This model is consistent with weak temperature dependence of the diode with $N_a = 1\times10^{19}$ cm^{-3}, which suggested that the dominant current transport mechanism is related to tunneling current. In the case of $N_a = 1\times10^{18}$ cm^{-3}, however, the calculated depletion layer is 49 nm for p-SiC, so it is thick enough for carriers not to tunnel from p-SiC to n-GaN via interface traps under reverse-bias condition. Therefore, we did not observe leakage current under reverse bias.

Similarly, Fig. 4.12 shows schematic illustrations of the n-GaN/p-SiC heterojunction with two different doping concentrations and the calculated width of depletion layers under forward bias of 0.1 V. In the case of $N_a = 1\times10^{19}$ cm^{-3}, the calculated depletion layer is as thin as 11 nm so that it is thin enough for carriers to recombine via interface-trap-assisted tunneling under forward bias condition. Thus, we observed current even at zero-bias voltage. This model is consistent with weak temperature dependence of the diode with $N_a = 1\times10^{19}$ cm^{-3}, which suggests that the dominant current transport mechanism is related to tunneling current. In the case of $N_a = 1\times10^{18}$ cm^{-3}, however, the calculated depletion layer is 47 nm for p-SiC, so it is thick enough for carriers not to recombine via interface-trap-assisted tunneling. Therefore, we did not observe current near zero-bias voltage. This model is consistent with stronger temperature dependence of the diode with $N_a = 1\times10^{18}$ cm^{-3}, which suggests that the dominant current transport mechanism is not related to tunneling but to the diffusion process.

It can be concluded that by utilizing reduced doping of $N_a = 1\times10^{18}$ cm^{-3}, the current transport associated with the tunneling process through the thin depletion layer was suppressed, so that the diodes with $N_a = 1\times10^{18}$ cm^{-3} showed reduced leakage and thus improved rectifying behavior in I-V characteristics.

4.4.3 Carrier Injection Investigated by Electroluminescence

To further discuss the current transport mechanism in the GaN/SiC heterojunction, electroluminescence (EL) combined with PL were investigated. Fig. 4.13 (a) shows EL from the n$^+$-GaN/p-SiC heterojunction under forward bias. Dark red EL was observed from n$^+$-GaN/p-4H-SiC and n$^+$-GaN/p-6H-SiC with $N_a = 1\times10^{18}$ cm^{-3}. In PL measurement taken on the same region (Fig. 4.13 (b)), we observed bright whitish-yellow luminescence from the GaN layer, whereas dark red luminescence was observed from p-4H-SiC and p-6H-SiC (each PL spectra is also shown in Fig. 4.14). Judging from these two facts, the origin of the red EL is attributed to the luminescence from p-SiC. This means that the electron injection from n$^+$-GaN to p-SiC occurred while the hole injection from p-SiC to n$^+$-GaN was blocked, which is an important function in HBT structure. In addition, the diode on 6H-SiC showed brighter EL than that on 4H-SiC under the same current density. This fact suggests that

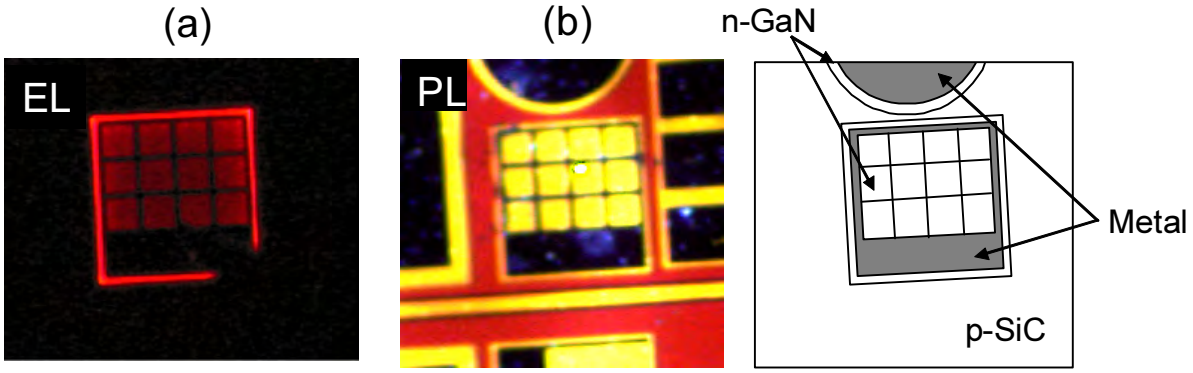

Figure 4.13: (a) EL from n^+-GaN/p-SiC heterojunction under forward bias. Dark red EL was observed from n^+-GaN/p-4H-SiC and n^+-GaN/6H-SiC with $N_a \sim 1\times10^{18}$ cm^{-3}. (b) PL taken on the same region. We observed bright whitish-yellow luminescence from GaN layer whereas dark red luminescence was observed from p-4H-SiC and p-6H-SiC.

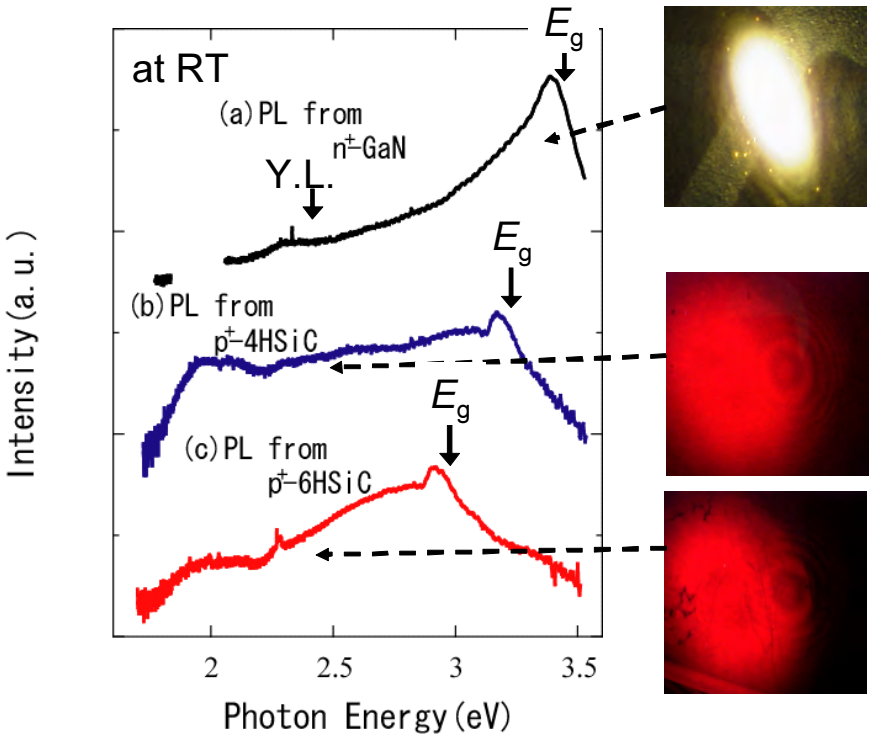

Figure 4.14: PL spectra of (a) n^+-GaN, (b) p-4H-SiC, and (c) p-6H-SiC, showing whitish-yellow luminescence for n^+-GaN and dark red for p-SiC.

6H-SiC is more efficient in terms of electron injection from n^+-GaN to p-SiC compared with 4H-SiC, which may be related to the lower barrier for electron injection according to the band diagram obtained from the C-V measurement.

4.5 GaN/SiC HBTs

4.5.1 Impact of Base Doping Concentration on GaN/SiC HBT Performance

The GaN/4H-SiC and GaN/6H-SiC HBTs with two different base doping concentrations of 5×10^{19} cm^{-3} and 1×10^{18} cm^{-3} are fabricated and characterized. HBTs with an emitter finger width of $W_{\mathrm{E}} = 10$ μm and the distance between emitter and base of $L_{\mathrm{EB}} = 10$ μm (total area: 140 μm $\times$ 320 μm) were used in this study.

The common-base I_{C}-V_{CB} characteristics of GaN/SiC HBTs with base doping of 5×10^{19}cm^{-3} and 1×10^{18} cm^{-3} are shown in Fig. 4.15 and Fig. 4.16. For HBT fabrication, metallization annealing of as high as 900°C was used to achieve low base contact resistance. Thus, although common-base I_{C}-V_{CB} characteristics were obtained, leakage current, which may originate from SiC surface since we did not utilize surface passivation in this study, was observed in collector-base diodes and thereby in common-base characteristics as shown in Fig. 4.15 and Fig. 4.16.

The common-base current gain of the HBTs with base doping of 5×10^{19} cm^{-3} was very low in both GaN/4H-SiC and GaN/6H-SiC HBTs ($\alpha < 1\times10^{-4}$). The low current gain is attributed to the low emitter injection efficiency from n-GaN to p-SiC since the dominant current transport mechanism is associated with tunneling as discussed before. On the other hand, we observed improved current gain of $\alpha \sim 0.01$ in GaN/4H-SiC HBTs and $\alpha \sim 0.03$ in GaN/6H-SiC HBTs with base doping of 1×10^{18} cm^{-3}. The improvement of current gain is due to the reduced doping of the p-SiC base layer. This resulted in a thicker depletion layer, which reduces the interface-trap-assisted tunneling and improves electron injection efficiency, as is suggested in the characteristics of GaN/SiC heterojunction diodes. In other words, optimization of the doping profile of the heterojunction contributes to a significant improvement in the current gain of GaN/SiC HBTs.

4.5.2 Impact of SiC Polytype on GaN/SiC HBT Performance

When comparing GaN/4H-SiC HBTs and GaN/6H-SiC HBTs, GaN/6H-SiC HBTs showed three times higher current gain of $\alpha \sim 0.03$. This implies that GaN/6H-SiC HBT structure has higher emitter injection efficiency probably due to its smaller conduction band offset as mentioned above. However, the current gain is still very low; thus further reduction of recombination at the interface, e.g. the band offset control of GaN/SiC heterojunction with AlGaN emitter, is necessary to achieve high performance HBTs.

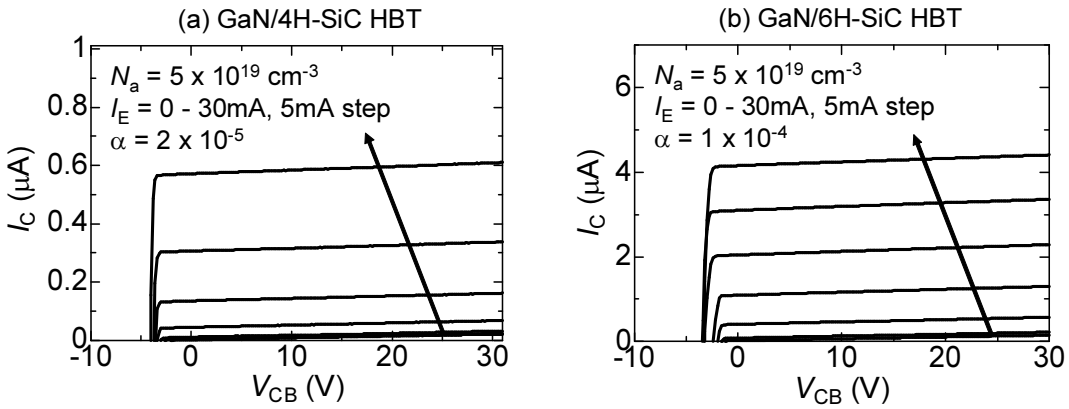

Figure 4.15: Common-base I_C-V_{CB} characteristics of (a) GaN/4H-SiC HBTs and (b) GaN/6H-SiC HBTs with base doping of 5×10^{19} cm^{-3}.

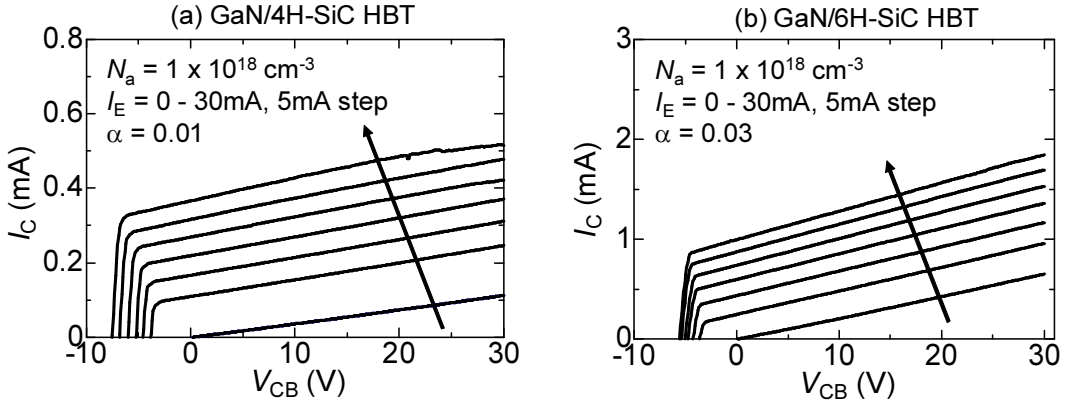

Figure 4.16: Common-base I_C-V_{CB} characteristics of (a) GaN/4H-SiC HBTs and (b) GaN/6H-SiC HBTs with base doping of 1×10^{18} cm^{-3}.

4.6 Effect of Ultrathin AlN Spacer on Electronic Properties of GaN/SiC Heterojunction Bipolar Transistors

4.6.1 Motivation

Bipolar junction transistors (BJTs) based on 4H-SiC are attractive candidates for high-power switching devices due to their high breakdown voltage, low ON-resistance, and high-current density [1]. In comparison with metal-oxide-semiconductor field effect transistors (MOSFETs), BJTs are free of oxide-related problems such as channel mobility and oxide reliability. However, SiC BJTs have so far suffered from the limited current gain. An alternative device structure would be heterojunction bipolar transistors (HBTs). Because it is impossible to grow Si_xC_{1-x} solid solutions with x near 0.5, bandgap engineering cannot be applied to SiC devices. Heteroepitaxial growth of wider bandgap semiconductor GaN ($E_g \sim 3.42$ eV) on SiC ($E_g \sim 3.26$ eV) makes it possible to utilize bandgap engineering in SiC-based devices, i.e., a higher current gain and superior high-frequency performance are expected for GaN/SiC HBTs [7].

In the previous section, impact of base doping concentration on electronic properties of GaN/SiC HBTs were studied. We suppressed the reverse leakage as well as recombination current at n-GaN/p-SiC heterojunction by reducing the base doping concentration from 1×10^{19} cm^{-3} to 1×10^{18} cm^{-3} [12]. Although common-base characteristics were obtained, the current gain was still very low ($\alpha \sim 0.01$). Since the low current gain must be attributed to low emitter injection efficiency, it is very important to control electronic properties of the n-GaN/p-SiC emitter junction.

In this section, GaN/SiC HBTs with ultrathin AlN spacer layer at the n-GaN/p-SiC emitter junction (GaN/AlN/SiC HBTs) are investigated. Considering that AlN has smaller lattice mismatch ($\sim 0.9\%$) with SiC than GaN ($\sim 3.0\%$), insertion of AlN spacer would be a promising approach to reducing the defect formation at the emitter junction and improving the electronic properties. On the other hand, AlN itself work as an insulator without any doping, and even with Si doping, it is not always easy to obtain highly conductive n-AlN since the donor ionization energy is about 250 meV [22]. Therefore, we utilize ultrathin AlN ($1-4.5$ nm) spacer between GaN and SiC so that the electrons can pass through the AlN layer via tunneling. In addition to the insertion of AlN layer, pre-irradiation of active nitrogen atoms (N*) is investigated to control the electronic properties of GaN/AlN/SiC heterojunction. We demonstrate improved electronic properties of GaN/SiC heterojunction and HBTs by the AlN spacer and N* pre-irradiation, and the correlation between the diode and transistor characteristics are discussed. In addition to electronic properties of the GaN/AlN/SiC heterostructures, newly developed process featuring ion implantation and Pd ohmic contact to obtain low resistivity to p-SiC base at low temperature is also presented.

4.6.2 Device Fabrication

A. Fabrication Process for GaN/AlN/SiC Heterojunction Diodes

The SiC substrates used in this study are commercially available 4H-SiC (0001) wafers with off-cut angles of 8° toward [11$\bar{2}$0]. The p-SiC substrates with 5-μm-thick p-type homoepitaxial layers with acceptor concentration of 1×10^{18} cm^{-3} were prepared for heterojunction diodes. Prior to the Ⅲ-nitride growth, SiC surface was treated with high temperature HCl gas etching to obtain the smooth surface [13]. Then the air-exposed SiC surface was treated with HF solution followed by an *in-situ* Ga deposition and desorption process to remove residual oxygen from the SiC surface [14]. The 1 – 4.5 nm-thick AlN films followed by 300 nm-thick Si-doped n-GaN films ($N_{\rm d} = 1\times10^{19}$ cm^{-3}) were grown on the 4H-SiC homoepitaxial layers at 600°C by molecular beam epitaxy (MBE) using elemental Al, Ga, Si and rf-plasma excited active nitrogen (N*). Two growth procedures were investigated: (1) supplying Al and N* simultaneously and (2) 1-min initial pre-irradiation of N* before AlN growth. The mesa diodes were fabricated by using reactive ion etching (RIE). No passivation was applied to the mesa sidewalls. Ti/Al/Ni and Ni were deposited onto the n-GaN and p-SiC, respectively, and they were sintered in Ar at as low as 600°C to form the ohmic contacts. Here the annealing temperature was carefully chosen since high temperature annealing step exceeding growth temperature may degrade the characteristics of the heterojunction.

B. Fabrication Process for GaN/AlN/SiC HBTs

For the GaN/AlN/SiC HBT fabrication, the n-SiC substrates with an n-SiC collector layer (10 μm, $N_{\rm d} = 8\times10^{15}$ cm^{-3}) and a p-SiC base layer (0.5 μm, $N_{\rm a} = 1\times10^{18}$ cm^{-3}) were prepared. Fig. 4.17 illustrates the structures of fabricated HBTs as well as heterojunction diodes. One of the considerations for the HBTs is how to form low resistivity ohmic contact to p-SiC. Generally speaking, when the doping concentration of p-SiC is $1\times10^{18} - 1\times10^{19}$ cm^{-3}, deposition of Ti/Al and high temperature annealing of over 900°C is required to form low resistivity ohmic contacts to p-SiC base. However, such high temperature annealing process exceeding MBE growth temperature (600°C) may degrade the GaN/AlN/SiC heterojunction. Therefore, ion implantation to p-SiC base contact region was employed to reduce the metallization temperature. In this study, multiple implantations of Al^+ were carried out at 500°C to form the p^{++} base contact regions ($N_{\rm a} = 5\times10^{20}$ cm^{-3}) with a 0.1 μm-deep box profile. The implants were activated by annealing at 1800°C for 10 min in Ar ambient. Note that these high temperature processes were all carried out before the MBE growth.

After the HCl gas etching followed by an *ex-situ* HF treatment and an *in-situ* Ga deposition and desorption process, the 1–4.5 nm-thick AlN films followed by Si-doped n^+-GaN films (0.3–0.5 μm, $N_{\rm d} = 2\times10^{19}$ cm^{-3}) were directly grown on the 4H-SiC surface at 600°C by MBE. Double mesa HBTs were fabricated by RIE, and no passivation was applied to

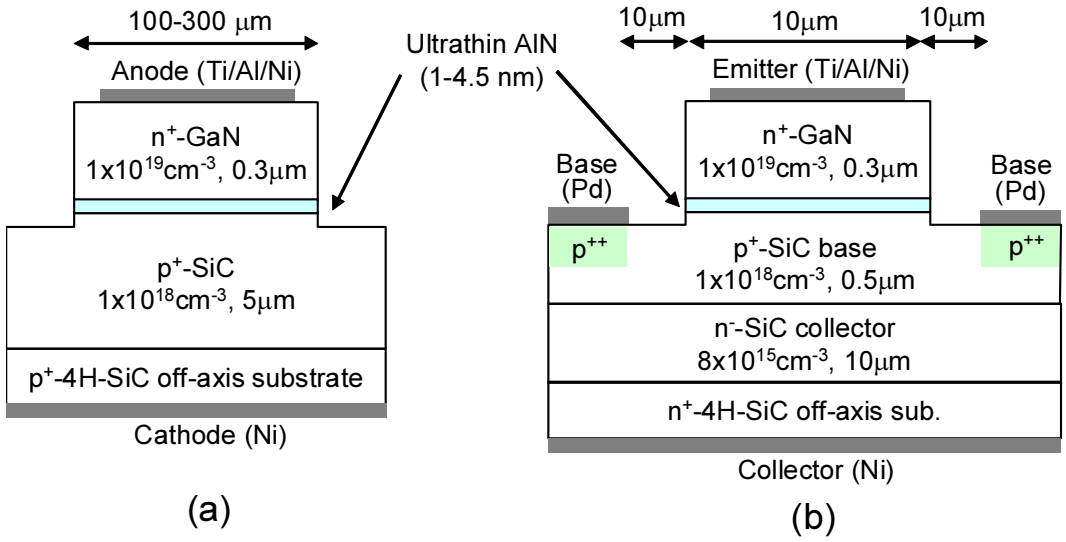

Figure 4.17: Schematic cross section of the fabricated GaN/SiC HBTs and GaN/SiC heterojunction diodes.

the mesa sidewalls in this study. Multilayer Ti/Al/Ni, Pd/Au, and Ni were deposited on the n-GaN emitter, p-SiC base, n-SiC collector (backside) surface, respectively, and they were sintered at 600°C for 10 min. Note that Pd was chosen to form low resistivity ohmic contacts to p^{++}-SiC, which is known as a good candidate for p^{++}-SiC ohmic contacts since it forms Pd-Si alloys at as low temperature as 500°C [23]. Fig. 4.18 shows I-V characteristics obtained from on-chip transmission line model (TLM) patterns. Pd and Ti/Al/Ni were investigated as ohmic contact materials. Although Pd did not show ohmic behavior without annealing, it showed linear I-V curves with annealing at 600°C, whereas common ohmic contact material Ti/Al/Ni did not show ohmic behavior even after the annealing at 600°C. This implies that Ti-Al system is not suitable to form p-SiC ohmic contacts at low annealing temperature. The contact resistance calculated using TLM structures after contact annealing were measured to 4.7×10^{-5} Ωcm^2 for the n-GaN emitter contact and 5.0×10^{-4} Ωcm^2 for the p-SiC base contact.

4.6.3 Impact of AlN Spacer Layer on Electronic Properties of GaN/SiC Heterojunction

To characterize the band diagram of GaN/AlN/SiC heterojunction, capacitance-voltage (C-V) measurements were conducted. Fig. 4.19 shows the C-V characteristics of GaN/SiC and GaN/AlN/SiC heterojunction without N* pre-irradiation. Here the thickness of AlN spacer is 1 nm. The slopes of $1/C^2$-V plots agreed well with the acceptor concentration of p-SiC layers. From the $1/C^2$-V plots, the built-in voltages (V_d) were extracted, and they were 2.35 V for GaN/SiC and 2.55 V for GaN/AlN/SiC. From these V_d values, the energy band diagrams of the GaN/AlN/SiC heterostructures are estimated as shown in Fig. 4.20. The C-V analyses revealed that the band diagram of both GaN/SiC and GaN/AlN/SiC heterojunction is type-Ⅱ, where there is a potential barrier to electrons from the emitter to base (0.90 eV for GaN/SiC and 0.70 eV for GaN/AlN/SiC) and a barrier to holes from the base to the emitter (0.74 eV for GaN/SiC and 0.54 eV for GaN/AlN/SiC). Note that the conduction band offset of 0.74 eV is almost the same as previously reported value. By utilizing AlN spacer, the barrier height to electron has been reduced from 0.74 eV to 0.54 eV, indicating that the GaN/AlN/SiC heterojunction may have better electron injection efficiency. It should be noted that the AlN layer is so thin that electrons can pass through via tunneling.

The current-voltage (I-V) characteristics of GaN/SiC and GaN/AlN/SiC heterojunction without N* pre-irradiation are shown in Fig. 4.21. GaN/SiC heterojunction diodes showed very small reverse leakage and good rectification. The turn-on voltage (V_T) defined by the current density of 10^{-2} A/cm^2 was 1.00 V. It should be noted that if the electron transport process is dominated by carrier injection, the turn-on voltage is nearly equal to the diffusion voltage. However, the measured turn-on voltage of the present n-GaN/p-SiC heterojunction diodes is as small as 1.00 V, which is much lower than the diffusion voltage (2.35 V) extracted

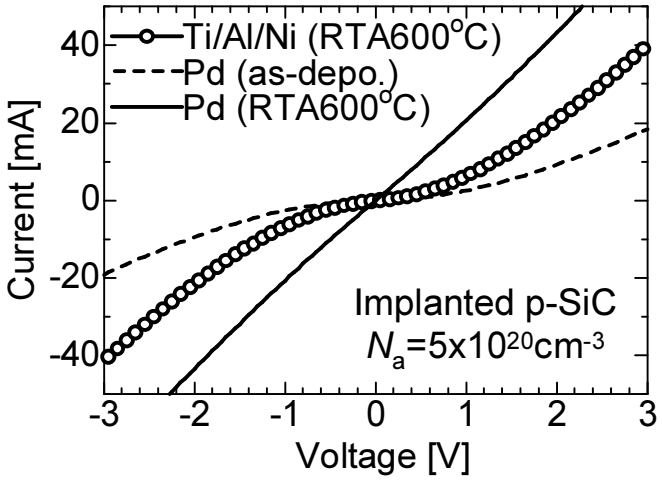

Figure 4.18: *I-V* characteristics obtained from on-chip transmission length method (TLM) patterns. Pd and Ti/Al/Ni were investigated as ohmic contact materials.

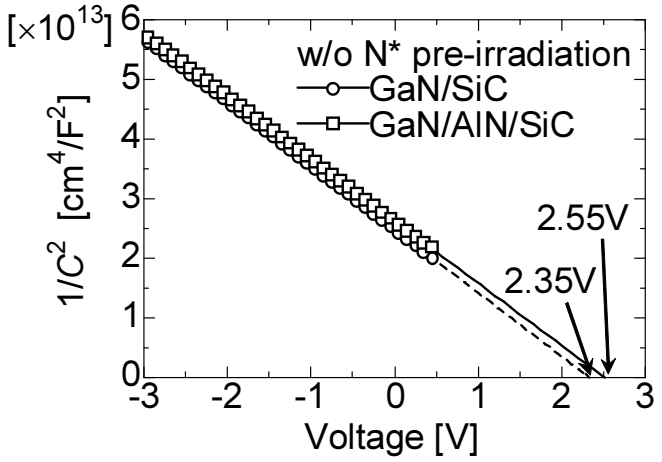

Figure 4.19: Capacitance-voltage (*C-V*) characteristics of GaN/SiC and GaN/AlN(1nm)/SiC heterojunction without N* pre-irradiation. Built-in potential ($V_{\rm d}$) is calculated to be 2.35 V for GaN/SiC and 2.55 V for GaN/AlN/SiC.

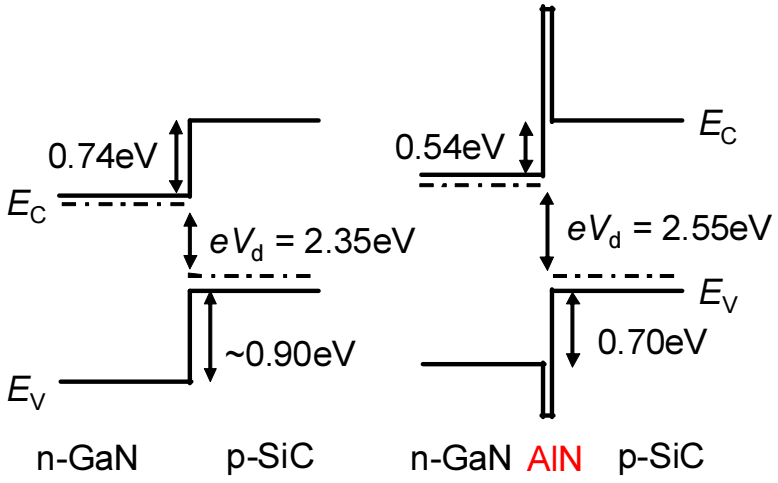

Figure 4.20: Energy band diagrams of (a) GaN/SiC and (b) GaN/AlN/SiC heterostructures.

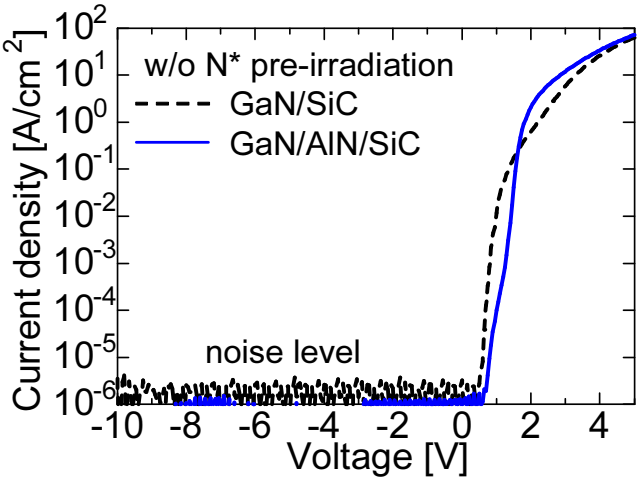

Figure 4.21: *I-V* characteristics of GaN/SiC and GaN/AlN/SiC heterojunction diodes without N* pre-irradiation. Turn-on voltages (V_T) defined by the current density of 10^{-2} A/cm^2 were 1.00 V for GaN/SiC and 1.45 V for GaN/AlN/SiC.

from *C-V* measurement (see Table 4.2). This phenomenon can be explained using Fig. 4.22 where the band diagram of GaN/SiC heterojunction under forward bias of V_{T} are shown. As revealed by *C-V* measurement, there is a large potential barrier to electron at GaN/SiC junction. This barrier blocks the electron injection from GaN to SiC. The accumulated electrons near the GaN/SiC heterointerface are forced to recombine via interface states with holes that are also accumulated at the heterojunction due to the potential barrier. As a result, recombination current is observed at low-bias voltage.

In the case of GaN/AlN/SiC heterojunction diodes, they also showed very small reverse leakage and good rectification, i.e. there is no significant degradation in diode characteristics by utilizing AlN spacer. The turn-on voltage (V_{T}) defined by the current density of 10^{-2} A/cm^2 was 1.45 V, which is smaller than the diffusion voltage (2.55 V) extracted from *C-V* measurement. The low turn-on voltage is attributed to the similar current transport mechanism as discussed above. However, by utilizing AlN spacer, the difference between V_{T} and V_{d} was reduced from 1.35 V to 1.10 V, suggesting that the smaller interface recombination is achieved in GaN/AlN/SiC heterojunction diodes.

To further investigate the impact of AlN spacer layer, GaN/AlN/SiC heterojunction with different AlN spacer thickness of 1, 2, 3, and 4.5 nm are investigated. Fig. 4.23 shows *I-V* characteristics of the heterojunction diodes with different AlN spacer thickness. From this section, emitter-base diodes in HBT structure are used for the characterization, and the turn-on voltage was defined at the forward current of 10^{-5}A. As shown in Fig. 4.23, *I-V* characteristics significantly changed with AlN spacer thickness. Although the diodes with AlN thickness of 1 nm did not show leakage, diodes with AlN thickness of 2, 3, and 4.5 nm showed significant leakage. Similarly, the diodes with AlN thickness of 1 nm showed relatively high turn-on voltage whereas diodes with AlN thickness of 2, 3, and 4.5 nm showed low turn-on voltage. The turn-on voltage and leakage current (defined at -10V) are plotted in Fig. 4.24. As shown in Fig. 4.24, we observed the tendency that the turn-on voltage was reduced as the leakage current increased, implying that the large leakage current and low V_{T} values may be related to the same origins. As already discussed, the low V_{T} is associated with large recombination at the heterojunction, which may suggest the presence of large number of interface states. So we assume that the presence of larger number of the interface states contributed to the recombination current, which reduced V_{T}, under forward bias as well as generation current, which produced leakage, under reverse bias. One possible reason for the larger number of interface states (larger recombination/generation current) with increased AlN thickness may be related to the formation of defects at GaN/AlN/SiC interface. However, the reason is still unclear and further investigation is required to figure it out. Judging from the *I-V* characteristics, the insertion of 1 nm-thick AlN seems to be promising for the emitter junction of the HBTs.

Table 4.2: Relationship of turn-on and built-in voltage of GaN/SiC and GaN/AlN/SiC heterojunction.

Structure	Turn-on voltage (V_T)	Built-in voltage (V_d)	$V_d - V_T$
GaN/SiC	1.00 V	2.35 V	1.35 V
GaN/AlN(1 nm)/SiC	1.45 V	2.55 V	1.10 V

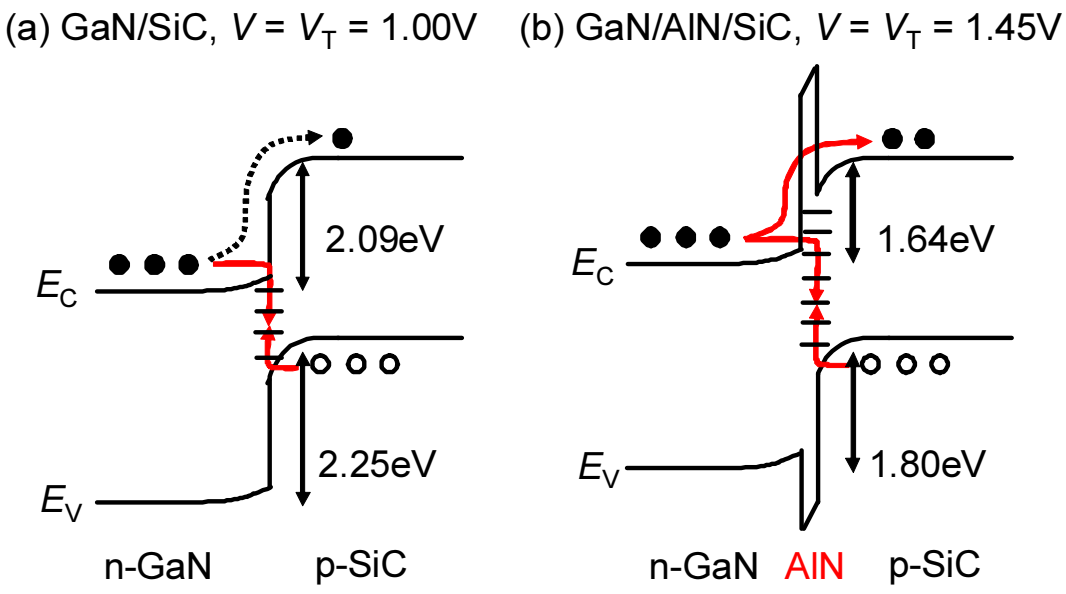

Figure 4.22: Band diagram of GaN/SiC heterostructure at forward bias of V_T.

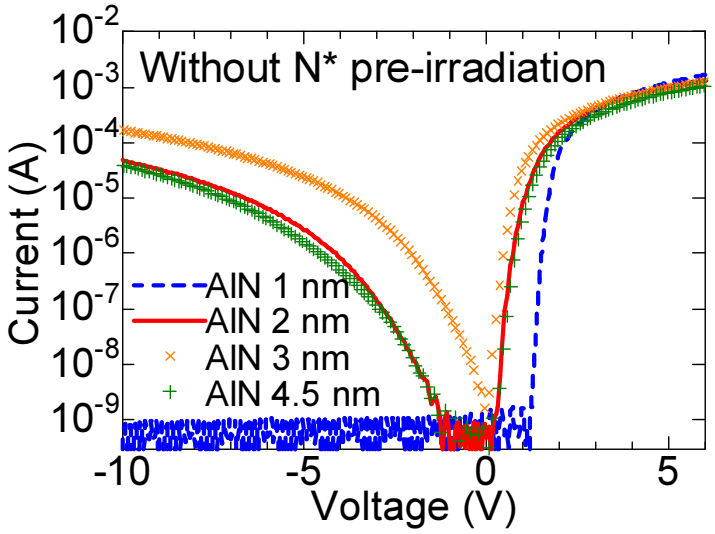

Figure 4.23: *I-V* characteristics of GaN/AlN/SiC heterojunction with different AlN spacer thickness of 1, 2, 3, and 4.5 nm.

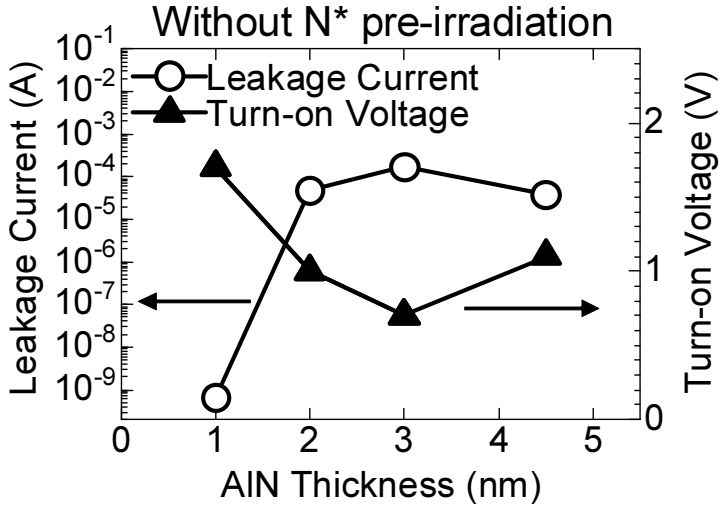

Figure 4.24: Relationship between leakage current and turn-on voltage in GaN/AlN/SiC heterojunction diodes. Turn-on voltage was defined at the forward current of 10^{-5} A and leakage current was defined at -10 V.

4.6.4 Impact of N* Pre-Irradiation on Electronic Properties of GaN/AlN/SiC Heterojunction

To control the electronic properties of GaN/AlN/SiC heterojunction, N* irradiation prior to the growth is investigated. Fig. 4.25 (a) shows the C-V characteristics of GaN/AlN/SiC heterojunction with N* pre-irradiation. Here the thickness of AlN spacer is 1 nm. $1/C^2$-V plots showed a linear curve and the built-in voltage (V_d) was extracted to 2.63 V. From this V_d value, the energy band diagram of the GaN/AlN/SiC heterostructures treated with N* pre-irradiation is estimated as shown in Fig. 4.25 (b). The band diagram of GaN/AlN/SiC heterojunction is type-Ⅱ, where there is a potential barrier to electrons from the emitter to base (0.46 eV) and a barrier to holes from the base to the emitter (0.62 eV). By utilizing N* pre-irradiation, the barrier height to electron has been reduced from 0.54 eV to 0.46 eV, indicating that N* pre-irradiation is effective to reduce the electron barrier. It should be noted that in the case of isovalent heterojunction such as AlGaAs/GaAs, the band offset is basically constant for a given heterostructure. However, the band offset can be varied by the different growth sequence in the case of heterojunction such as AlGaN/SiC, where the materials with different valency form the heterojunction. In fact, the large variation of band offset is theoretically predicted in ZnSe/GaAs [24, 25], GaAs/Ge [26, 27]and GaP/Si [26], and it was experimentally shown in ZnSe/GaAs heterovalent heterojunction that the band offset is tunable by manipulating interface compositions with Zn or Se treatment [28]. This is because heterovalent heterojunction has electron-excess and electron-deficient bonds at the interface, e.g. Si-N or Al-C in the case of AlN/SiC, which form donor and acceptor states and make the electronic dipoles affecting the band offset that are sensitive to the surface preparation prior to the growth. We assume that the N* pre-irradiation prior to the GaN/AlN growth contributed to the formation of different interface composition at the heterojunction due to the N termination of SiC surface, resulting in the different band offset.

Fig. 4.26 shows I-V characteristics of the GaN/AlN/SiC heterojunction diodes treated with N* pre-irradiation prior to the growth. Here the thickness of the AlN insertion layer has been varied from 1 nm to 4.5 nm. As shown in Fig. 4.26, I-V characteristics of GaN/AlN/SiC heterojunction diodes treated with N* pre-irradiation also changed with AlN spacer thickness. Although the diodes with AlN thickness of 2 nm did not show leakage, diodes with AlN thickness of 1, 3, and 4.5 nm showed significant leakage. Similarly, the diodes with AlN thickness of 2 nm showed relatively high turn-on voltage, whereas diodes with AlN thickness of 1, 3, and 4.5 nm showed low turn-on voltage. These I-V characteristics show a tendency that low V_T values are observed for diodes with large leakage current (Fig. 4.27). This implies that the large leakage current and low V_T values may be related to the same origins, which we assume generation/recombination at the GaN/AlN/SiC interface due to the presence of larger number of the interface states as already discussed above. In GaN/AlN/SiC heterojunction with N* pre-irradiation, we observed improved turn-on voltage when the AlN thickness is 2 nm, whereas improved characteristics were obtained when

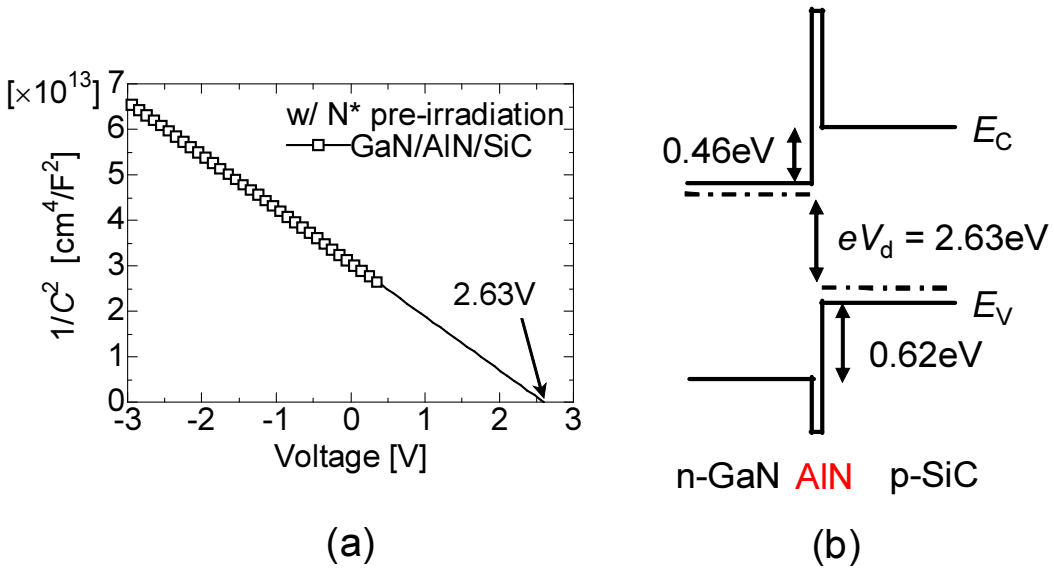

Figure 4.25: (a) C-V characteristics of GaN/AlN(1nm)/SiC heterojunction with N* pre-irradiation. $1/C^2$-V plots showed a linear curve and the built-in voltage (V_d) was extracted to 2.63 V. (b) Estimated energy band diagram of the GaN/AlN/SiC heterostructures treated with N* pre-irradiation using the V_d value.

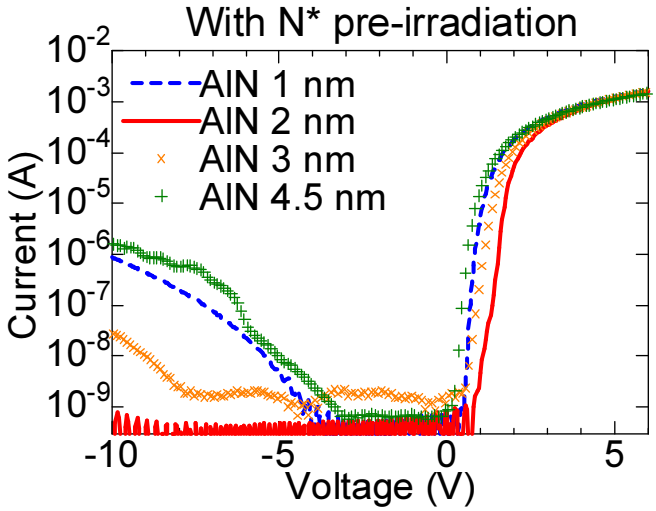

Figure 4.26: I-V characteristics of GaN/AlN/SiC heterojunction with N* pre-irradiation. The thickness of AlN spacer was varied from 1 nm to 4.5 nm.

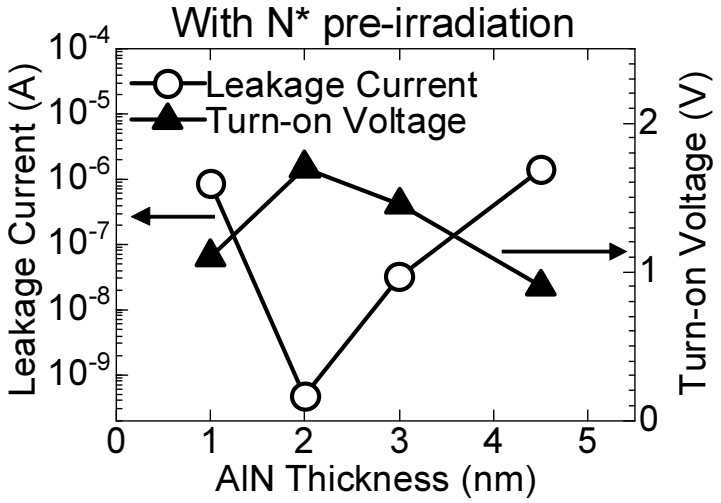

Figure 4.27: Relationship between leakage current and turn-on voltage in Gan/AlN/SiC heterojunction diodes. Turn-on voltage was defined at the forward current of 10^{-5} A and leakage current was defined at -10 V.

the AlN thickness is 1 nm in GaN/AlN/SiC heterojunction without N* pre-irradiation. One possible explanation for the different optimized AlN thickness may be attributed to the change of initial growth mode by N* pre-irradiation since it forms the Si-N bonds at the SiC surface. Judging from the *I-V* characteristics, the insertion of 2 nm-thick AlN with N* pre-irradiation seems to be promising for the emitter junction of the HBTs.

4.6.5 Performance of GaN/AlN/SiC HBTs

The 140 μm × 320 μm HBT structures with an emitter finger width of $W_{\mathrm{E}} = 10$ μm, and the distance between the emitter and base contact region of $L_{\mathrm{EB}} = 10$ μm were fabricated. Fig. 4.28 shows the characteristics of the emitter-base and collector-base diodes in GaN/SiC HBTs. Collector-base diodes in GaN/SiC HBTs did not show leakage under reverse bias, indicating that the mesa structure was successfully formed. The ideality factor of the diode under forward bias was calculated to be 2.0, suggesting the presence of recombination current. We assume the high ideality factor is attributed to surface recombination due to the lack of passivation layer in the present HBTs. Emitter-base diodes in the HBTs showed similar *I-V* characteristics to GaN/SiC heterojunction diodes without any degradation, indicating successful fabrication of HBT structures. Note that our previously reported GaN/SiC HBTs showed significant leakage in both emitter-base and collector-base diodes due to high temperature metallization annealing of 900°C. The suppression of the leakage is attributed to our newly developed process featuring ion implantation and Pd ohmic contact to obtain low resistivity to p-SiC base at as low as 600°C as discussed before.

Subsequently, the HBTs are characterized. Fig. 4.29 summarizes the current gain of fabricated HBTs. Open circles in Fig. 4.29 show the current gains of the HBTs without N* pre-irradiation. The common-base current gain of the HBTs without AlN spacer was very low ($\alpha \sim 0.001$). On the other hand, a significantly improved current gain ($\alpha \sim 0.1$) is observed in GaN/AlN/SiC HBTs by insertion of the 1 nm-thick AlN spacer (the common-base I_{C}-V_{CB} characteristics are shown in Fig. 4.30 (a)). The improvement of current gain is attributed to the better electron injection efficiency due to the reduced potential barrier to electron and smaller recombination at the heterojunction revealed by *C-V* and *I-V* measurements. In the case of AlN thickness of 2, 3, and 4.5 nm, diodes showed significant leakage and reduced turn-on voltage associated with generation/recombination at the GaN/AlN/SiC interface via interface traps, and therefore low current gain was predicted. In fact, HBTs with these heterojunction showed low current gain ($\alpha < 1\times10^{-3}$), and there is a strong tendency that low current gain was observed in the HBTs with large leakage current. Closed circles in Fig. 4.29 show the current gains of the HBTs with N* pre-irradiation. The gain showed strong dependence on the AlN thickness. From the diode characteristics, the low current gain was indicated due to their large leakage current and low V_{T} associated with generation/recombination at the GaN/AlN/SiC interface in the case of AlN thickness of 1, 3 and 4.5 nm. In fact, the HBTs with AlN thickness of 1, 3 and 4.5 nm showed the

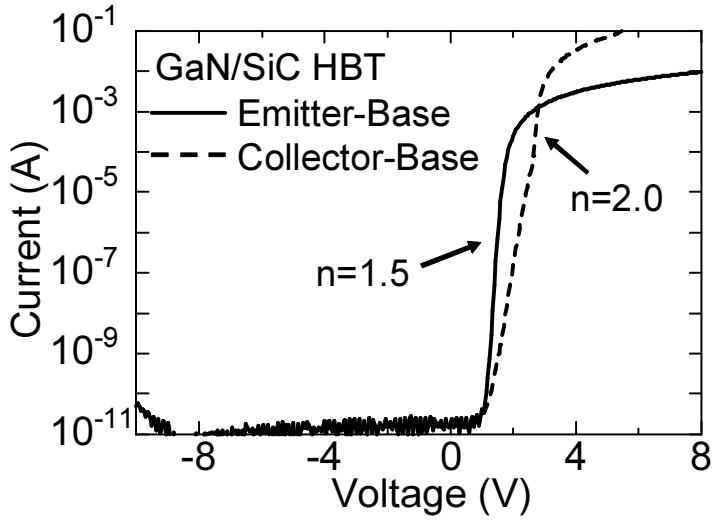

Figure 4.28: *I-V* characteristics of emitter-base and collector-base diodes in GaN/SiC HBTs. *I-V* characteristics similar to GaN/SiC heterojunction diodes were obtained, indicating successful fabrication of HBT structures.

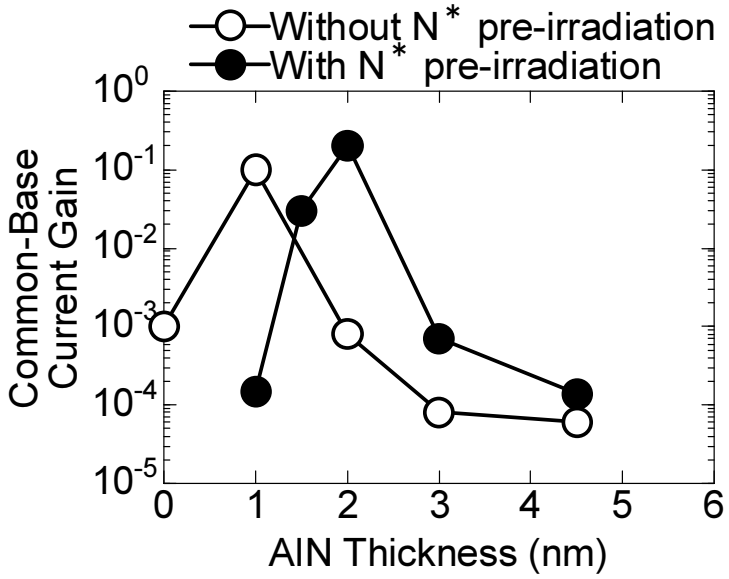

Figure 4.29: Summary of common-base current gain of the investigated GaN/AlN/SiC HBTs.

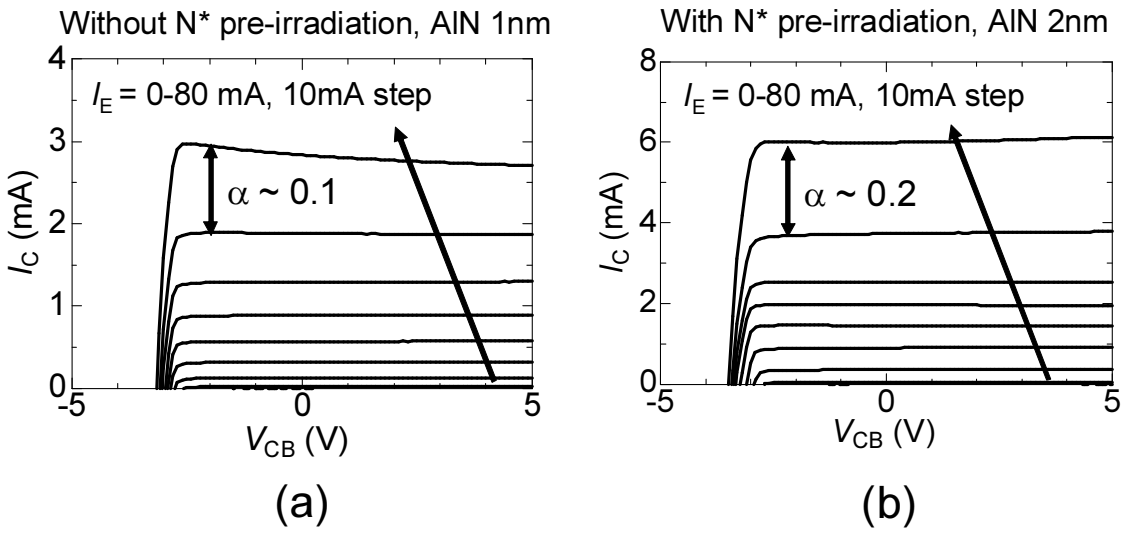

Figure 4.30: Common-base I_C-V_{CB} characteristics of the GaN/AlN/SiC HBT with (a) 1 nm-thick AlN layer without N* pre-irradiation and (b) 2 nm-thick AlN layer with N* pre-irradiation, where incremental current gains of 0.1 and 0.2 were obtained, respectively.

common-base current gain below 1×10^{-3}. In contrast, the HBT with AlN thickness of 2 nm, which is expected to show the improved current gain, exhibited a maximum incremental current gain of $\alpha \sim 0.2$ (The common-base I_C-V_{CB} characteristics are shown in Fig. 4.30 (b)). Compared with HBTs without N* pre-irradiation, further improvement of current gain was achieved, and one possible explanation of this may be due to the further reduction of potential barrier to electron injection by N* pre-irradiation revealed by C-V and I-V measurements. From these results, insertion of ultrathin AlN spacer at the GaN/SiC emitter junction as well as N* pre-irradiation would be a promising approach to obtaining high electron injection efficiency.

4.7 Summary

Growth, electrical characterization, and electroluminescence (EL) of GaN/SiC heterojunction bipolar transistors (HBTs) fabricated on SiC off-axis substrates are presented. We have started by investigating the crystal quality of MBE-grown GaN on off-axis SiC. The GaN layer grown on off-axis SiC showed step bunching due to the large off-angle of the substrates. It contributed to the annihilation of edge dislocations revealed by XRD and TEM analysis. Also, Hall-effect measurement showed the GaN layer has adequate electron mobility as well as carrier concentration, suggesting that the GaN on off-axis SiC substrate is applicable for the emitter of GaN/SiC HBTs. Subsequently, we investigated the impact of base doping concentration and polytype of SiC (4H and 6H) on electronic properties of the GaN/SiC heterojunction and HBTs. By utilizing reduced doping of 1×10^{18} cm^{-3} instead of 1×10^{19} cm^{-3}, we successfully suppressed the tunneling current via interface traps, resulting in significantly improved rectifying behavior in both the GaN/4H-SiC and GaN/6H-SiC heterojunction diodes. C-V characteristics revealed that the band lineup of GaN/SiC is type-Ⅱ, and 6H-SiC is better for electron injection, which is supported by EL. In accordance with diode characteristics, GaN/SiC HBTs showed improved current gain by employing reduced base doping concentration and by utilizing 6H-SiC. A maximum common-base current gain of 0.01 and 0.03 was obtained on GaN/4H-SiC HBTs and GaN/6H-SiC HBTs, respectively, with base doping of 1×10^{18} cm^{-3}.

Next, GaN/SiC HBTs with ultrathin AlN spacer layers at the n-GaN/p-SiC emitter junction were proposed in attempt to improve the electronic properties of GaN/SiC heterojunction. The insertion of AlN spacer is found to be promising in terms of electron injection efficiency due to the reduced potential barrier (0.54 eV) to electron injection and smaller recombination via interface traps. We also investigated N* pre-irradiation prior to AlN growth to control the electronic properties of GaN/AlN/SiC heterojunction. We found that the potential barrier was further reduced to 0.46 eV by N* pre-irradiation. The HBT structure was successfully fabricated with newly developed process featuring ion implantation and Pd ohmic contact to obtain low resistivity to p-SiC base at as low as 600°C. With

these efforts, we achieved a maximum common-base current gain of 0.1 in the GaN/AlN/SiC HBT with 1 nm-thick AlN layer without N* pre-irradiation and 0.2 in 2 nm-thick AlN layer with N* pre-irradiation.

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Chapter 5

AlGaN/SiC Heterojunction Bipolar Transistors featuring AlN/GaN Superlattice Emitter

5.1 Introduction

SiC-based power bipolar junction transistors (BJTs) are recognized as very attractive candidates for high-power switching devices due to the superior properties such as high breakdown voltage, low ON-resistance, and high temperature operation with high current density [1]. SiC BJTs close to the SiC unipolar limit in a wide range of voltages have been reported in addition to attractive characteristics such as fast switching, low forward voltage drop [2, 3]. However, their low current gain remains areas of the concerns since it results in the large power dissipation at the drive circuit. A few groups have demonstrated a current gain over 100 at room temperature [4–6]. However, it falls off to about 50 at 250°C since BJTs show negative temperature coefficient of current gain. In Chapter 3, we demonstrated 4H-SiC BJTs with record-high current gain of 257 on (0001), and it exhibited a high current gain of 127 even at 250°C [7]. However, to compensate the disadvantages of BJTs, namely, expensive and big drive circuit derived from the low current gain, even higher current gain especially at elevated temperature is desired for practical application. For improved current gain in SiC BJTs, we have studied AlGaN/SiC heterojunction bipolar transistors (HBTs) as next-generation high-current-gain power transistors. In the HBTs, AlGaN is employed as a wide bandgap emitter, which forms the valence band offset and hinders hole back injection from p-base to n-emitter. This band offset allows us to achieve extremely high electron injection efficiency equal to unity and therefore temperature-independent current gain if there were no interface states at AlGaN/SiC heterojunction.

Fabrication of GaN/SiC HBTs was first reported by Pankove *et al.* in 1994 [8]. They showed a current gain of $\alpha \sim 0.99999$ at room temperature and $\alpha \sim 0.99$ at high temperature of 535°C in common-base configuration so that the results seemed promising [9].

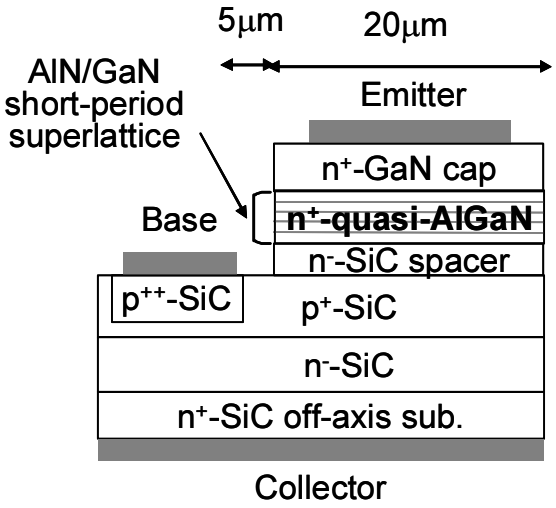
However, no groups reported such common-base results, and so far only a few reports are available on GaN/SiC HBTs in common-base configuration [10, 11]. In addition, it turned out that the promising results could not be easily reproduced [12]. After all, although there are large number of reports on GaN/SiC heterojunction diodes [13–18] in response to the first demonstration of GaN/SiC HBTs, common-emitter operation has not been reported in the HBTs and focused research on n-GaN/p-SiC emitter junctions is necessary to achieve common-emitter-mode operation in the HBTs.

In Chapter 4, GaN/SiC HBTs were studied and the electronic properties of GaN/SiC heterojunctions were improved by optimizing base doping concentrations to reduce the interface-trap-assisted tunneling [19] and inserting an ultrathin AlN spacer layer between the GaN and SiC to suppress interface recombination [20]. Although leakage current at emitter junctions was successfully suppressed, common-emitter current gain (β) in the HBTs was still much smaller than 1 ($\beta < 0.1$). Capacitance-voltage (C-V) measurements revealed that there was a large potential barrier (of about 0.5 eV) to electron injection (type-Ⅱ band alignment) [20]. This barrier blocked electron flow from n-GaN to p-SiC and produced high electron concentrations near the interface that resulted in interface-trap-assisted recombination. We assume this to be the one possible reason for the low current gain in GaN/SiC HBTs. Theoretically, utilization of a wider bandgap AlGaN emitter instead of a GaN emitter would seem to be a promising approach to controlling conduction band offset, but Danielsson *et al.* have reported that conduction band offset at the AlGaN/SiC heterointerface was nearly independent of the Al composition, due to the presence of a strong interface charge at the junction [21]. We have found that growth of ternary AlGaN on SiC is very difficult with the conventional growth techniques due to initial three-dimensional growth, which obstructed the control of band offset.

In this section, we propose SiC HBTs which employ AlN/GaN short-period superlattice (quasi-AlGaN) as widegap emitter [22]. With this device structure, growth can be started with AlN that has smaller lattice mismatch and better wetting (smaller interface energy) with SiC than does AlGaN. This results in a high-quality Ⅲ-N/SiC interface. We demonstrate band offset control in (quasi-)AlGaN/SiC and common-emitter mode operation ($\beta \sim 2.7$) in Ⅲ-N/SiC HBTs. Toward further improvement of current gain, impacts of n-SiC spacer and p-SiC base width are also presented in attempt to reduce the interface and bulk recombination. A maximum current gain of 13 is reported in the HBTs.

5.2 Device Fabrication

Fig. 5.1 shows a schematic cross section of fabricated HBTs. SiC substrates used in this study are commercially available 4H-SiC (0001) wafers with off-cut angles of 8° toward [11$\bar{2}$0]. N^+-SiC substrates with a N-doped n^--SiC collector layer (10 μm, $N_d = 5\times10^{15}$ cm^{-3}), an Al-doped p^+-SiC base layer (250 – 500 nm, $N_a = 1\times10^{18}$ cm^{-3}), and



Layer	Material	Concentration (cm^{-3})	Thickness (μm)
Contact	n^+-GaN	2×10^{19}	0.2
Emitter	n^+-(AlN/GaN)	$\sim 10^{19}$	0.1
Spacer	n^--SiC	1×10^{16}	0.05
Base	p^+-SiC	1×10^{18}	0.5
Collector	n^--SiC	5×10^{15}	10
Buffer	n^+-SiC	1×10^{18}	0.5

Figure 5.1: Structures of fabricated AlGaN/SiC HBTs.

an n^--SiC spacer layer (50 – 200 nm, $N_d = 1\times10^{16}$ cm^{-3}) were prepared by chemical vapor deposition. Before Group-Ⅲ nitride (Ⅲ-N) growth, selective Al^+ ion implantation to base contact region was carried out for low resistivity ohmic contacts. The Al^+ ion implantation was performed at 500°C with a 0.1 μm-deep box profile ($N_a = 5\times10^{20}$ cm^{-3}). The implants were activated by annealing at 1800°C for 10 min in Ar ambient with a carbon cap. The cap was removed by following sacrificial oxidation at 1150°C for 5 h, and surface was treated by high temperature HCl gas etching to form the step-controlled surface.

Ⅲ-N layers were then grown by means of plasma-assisted molecular beam epitaxy (MBE) using elemental Al, Ga, and rf-plasma-excited active nitrogen (N*). A Si-doped AlN (0.6 nm)/GaN (0.4 – 1.8 nm) short-period superlattice (total thickness: 0.1 μm, $N_d \sim 10^{19}$ cm^{-3}), followed by a Si-doped n^+-GaN contact layer (0.2 μm, $N_d = 2\times10^{19}$ cm^{-3}) were grown on the 4H-SiC homoepitaxial layers at 600°C. HBTs of various average Al compositions (0 – 0.6) were fabricated by changing the ratio of GaN layer thicknesses. For comparison, a GaN/SiC HBT with an ultra-thin AlN insertion layer (1.0 nm) was also fabricated [20].

Double-mesa HBTs were fabricated using reactive ion etching (RIE) with a deposited SiO_2 mask. Multilayer Ti/Al/Ni ohmic contacts were formed on the n-GaN and p-SiC surface using a standard lift-off technique and a rapid thermal annealing (RTA) at 600°C in Ar. Heterojunction mesa diodes with a diameter of 100 μm were also fabricated on p-SiC substrates with 5 μm-thick p-type homoepitaxial layers with an acceptor concentration of 1×10^{18} cm^{-3} for detailed electrical characterization of the AlGaN/SiC interface.

5.3 MBE Growth of AlN/GaN Short-Period Superlattice on Off-axis SiC

Prior to the characterizations of AlGaN/SiC heterojunction and HBTs, structural and electronic properties of MBE-grown AlGaN on off-axis SiC substrates are discussed in this section. As previously noted, AlN/GaN short-period superlattice (SPSL) was used as an emitter of the HBTs. The advantage beyond conventional AlGaN growth method is that we can start the growth with AlN layer that has smaller lattice mismatch and better wetting with SiC than AlGaN, resulting in a high-quality Ⅲ-N/SiC interface. We already reported in GaN/SiC HBTs that the insertion of an ultrathin AlN layer contributed to the smaller interface recombination due to the lower defect formation at the heterojunction. Another advantage is that it is easier to control the Al composition since it is defined by the thickness ratio of AlN/GaN superlattice. It should be noted that the AlGaN layer is grown on SiC 8° off-axis substrates since SiC homoepitaxy has been developed for (0001) off-axis SiC substrates instead of on-axis substrates because the step-controlled growth mechanism is essential to prevent formation of cubic-phase (3C-SiC) inclusions during homoepitaxy [23]. Although there have been a few reports of growth of AlN/GaN superlattice on off-axis

sapphire [24], the investigation is limited to relatively low off-angle of up to 2°, whereas a large off angle of 8° for 4H-SiC toward the [11$\bar{2}$0] direction is generally used in SiC technology. The MBE grown AlGaN layers on such SiC off-axis substrates are characterized by reflection high energy electron diffraction (RHEED), atomic forced microscopy (AFM), X-ray diffraction (XRD), transmission electron microscopy (TEM), and cathodoluminescence (CL). Electronic properties of the AlGaN layer are also characterized by Hall-effect measurement.

5.3.1 Surface Morphology

Fig. 5.2 shows the typical surface morphology of AlN/GaN superlattice grown on SiC off-axis surface. Surface morphologies of SiC before the AlN/GaN superlattice growth and GaN grown on SiC are also shown as a reference. As shown in Fig. 5.2 (a), 4H-SiC off-axis surface showed steps with a step height of 1 – 2 nm corresponding to one or two unit height (4 or 8BL) of 4H-SiC, although there is a possibility of underestimation of step height since the terrace width is as small as 20 nm. The RMS roughness of SiC surface before the growth was 0.32 nm, indicating a smooth surface was obtained. When the superlattice was grown on the SiC surface, a surface morphology with a RMS roughness of 0.63 nm was obtained, as shown in Fig. 5.2 (c). Although the surface morphology showed a step-and-terrace structure along [11$\bar{2}$0] off-cut direction, the terrace width was about 40 nm, which is larger than that of SiC surface before the growth (20 nm). In addition, the step height was 2 – 3 nm, which is also larger than that of SiC surface before the growth (1 – 2 nm), indicating that step bunching along [11$\bar{2}$0] off-cut direction occurred due to the large off-angle of the SiC substrates. It should be noted that in the case of GaN grown on SiC off-axis substrates at the same growth temperature by MBE (Fig. 5.2 (b)), we observed large step-bunching with a step height of 5-10 nm. The relatively smooth surface morphology in AlN/GaN superlattice on off-axis SiC compared with GaN is attributed to the presence of AlN layer. We reported that the AlN grown at the same growth temperature of 600°C showed very smooth surface morphology with RMS roughness of 0.3 nm, and the step height was measured to be 0.5 nm [25]. This indicated that no step bunching occurred in growth of AlN at 600°C, suggesting smaller migration length of Al compared with Ga on 4H-SiC surface. So we assume that although GaN likely grow in a step-flow mode, the AlN layer, which grows in layer-by-layer growth mode on SiC terraces due to the smaller migration length of Al, contributed to the suppression of surface roughening, resulting in the smooth surface morphology. This feature is indicated by TEM observation of GaN and AlN on SiC off-axis substrates, where step-bunching-induced annihilation of dislocation occurred only in the case of GaN (Fig. 5.3). This is also indicated by the RHEED intensity profile during MBE-growth of AlGaN on SiC shown in Fig. 5.4, where the intensity decreased during the AlN growth and it recovered during the GaN growth, suggesting that the AlN growth on GaN is likely 3-dimensional (3-D), whereas GaN growth on AlN is likely 2-D.

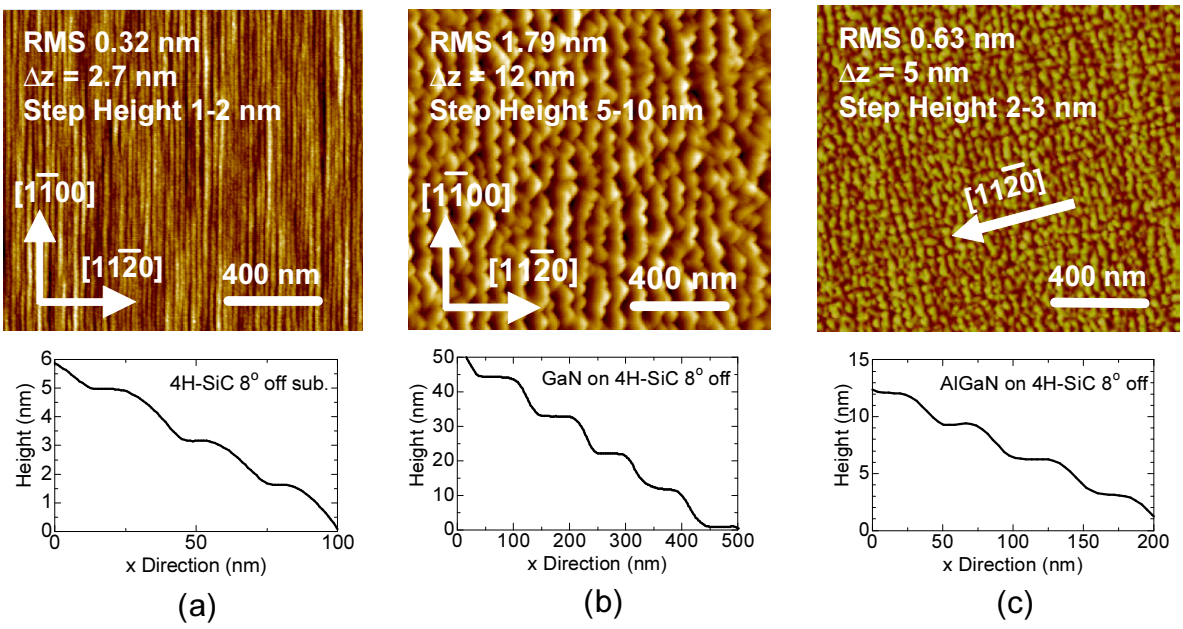


Figure 5.2: (a) Surface morphologies of SiC before the AlN/GaN superlattice growth, (b) GaN grown on SiC, and (c) AlN/GaN superlattice grown on SiC off-axis surface.

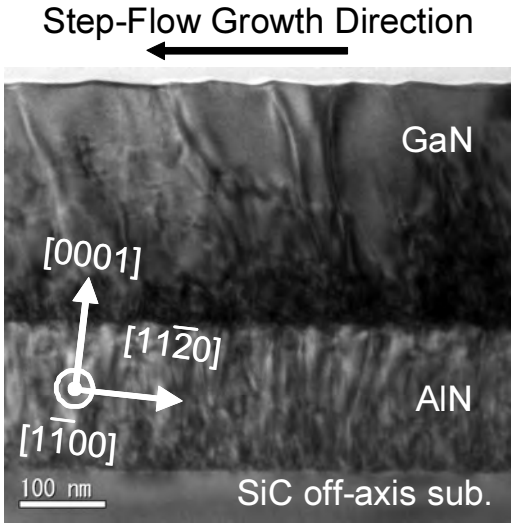


Figure 5.3: Cross-sectional TEM image (zone-axis) of GaN/AlN on SiC off-axis substrates, where step-bunching-induced annihilation of dislocation occurred only in the case of GaN.

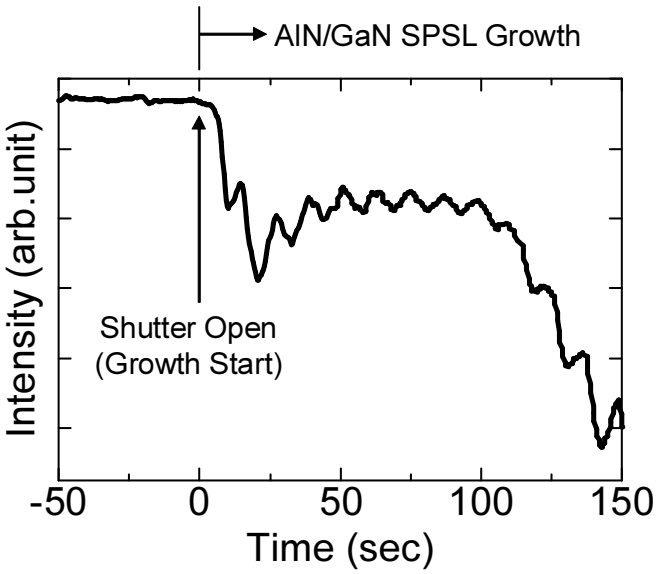


Figure 5.4: RHEED intensity profile during MBE-growth of AlGaN on SiC. Intensity decreased during the AlN growth and it recovered during the GaN growth.

5.3.2 XRD and TEM analysis

XRD and TEM analyses were conducted to characterize the quality of MBE-grown AlGaN on off-axis SiC. Table 5.1 shows the full width at half maximum (FWHM) in the (0002) reflection peak in XRD measurements. From the $2\theta/\omega$ scan, average Al composition was calculated. The calculated Al compositions were almost the same as those defined by the ratio of AlN/GaN layer thickness. FWHM of about 440 arcsec for $2\theta/\omega$ scan and 200 arcsec for ω scan were obtained independent of Al compositions, whereas FWHM of 124 arcsec for $2\theta/\omega$ scan and 97 arcsec for ω scan were obtained in reference GaN. Relatively high FWHM in $2\theta/\omega$ scan may be attributed to the 3-D growth of the thin AlN layer in the superlattice as discussed in the previous section. This assumption is also supported by the fact that we did not observe any satellite peaks derived from the presence of abrupt superlattice structure. The FWHM of the ω scan in $(1\bar{1}02)$ reflection peak was 2423 arcsec, which is higher than that of GaN grown at the same growth condition (936 arcsec), suggesting that the superlattice has large number of edge and/or mixed dislocations. In the case of GaN, we reported that although edge dislocations are generated at the initial growth stage due to the lattice mismatch between GaN and SiC, step-flow growth of GaN contributed to the dislocation vending along off-cut direction, resulting in the annihilation of edge dislocations as the thickness increased. In contrast, such step-flow growth mode does not always occur in AlN/GaN superlattice growth since AlN growth mode is likely three-dimensional, so the reduction of edge dislocations in growth on SiC off-axis substrates was not expected in AlN/GaN superlattice epitaxy. Thus, high FWHM value and thereby large number of edge dislocations were indicated. Fig. 5.5 shows a high-resolution cross-sectional TEM image of AlGaN grown on 4H-SiC off-axis surface. The TEM image was taken from $[2\bar{1}\bar{1}0]$ direction to observe the superstructure of the epilayer. We confirmed the presence of superlattice structure by HRTEM. However, we observed disorders in superlattice structure in some areas so that the control of growth sequence will be implemented in the future work.

5.3.3 Cathodoluminescence

To investigate the optical properties of AlGaN grown on off-axis SiC, CL measurements were conducted. Fig. 5.6 shows CL spectra of AlGaN grown on 4H-SiC off-axis substrates taken at RT. As shown in Fig. 5.6, one single peak was observed. The peak energies were extracted from CL spectra, which were summarized in Table 5.2. In Table 5.2, bandgap energies of AlGaN calculated by Vegard's law or Kronig-Penny model are also shown, where the bandgap energy of 3.42 eV for GaN and 6.00 eV for AlN, bowing parameter b of 0.82, and the conduction/valance band offset of 1.7 eV/0.8 eV at AlGaN/SiC are used. As shown in Table 5.2, the peak energy of CL spectra is far below the bandgap energy of AlGaN (0.36 – 0.72 eV deeper than E_g). This difference indicates that no band-emission related peaks are observed in the present quasi-AlGaN. One possible explanation of the emission from deep states is the presence of a large amount of such impurities as oxygen (O) or carbon (C).

Table 5.1: FWHM in the (0002) reflection of XRD measurement.

AlGaN on 4H-SiC 8° off-axis	XRD FWHM in (0002) reflection	
	$2\theta/\omega$ scan	ω scan
GaN	124 arcsec	97 arcsec
$Al_{0.25}Ga_{0.75}N$	428 arcsec	188 arcsec
$Al_{0.33}Ga_{0.67}N$	440 arcsec	202 arcsec
$Al_{0.40}Ga_{0.60}N$	446 arcsec	200 arcsec

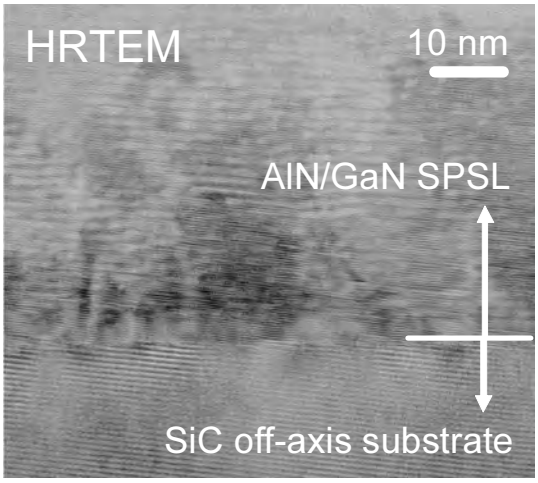


Figure 5.5: A high-resolution cross-sectional TEM image of AlGaN grown on 4H-SiC off-axis surface. The TEM image was taken from $[2\bar{1}\bar{1}0]$ direction.

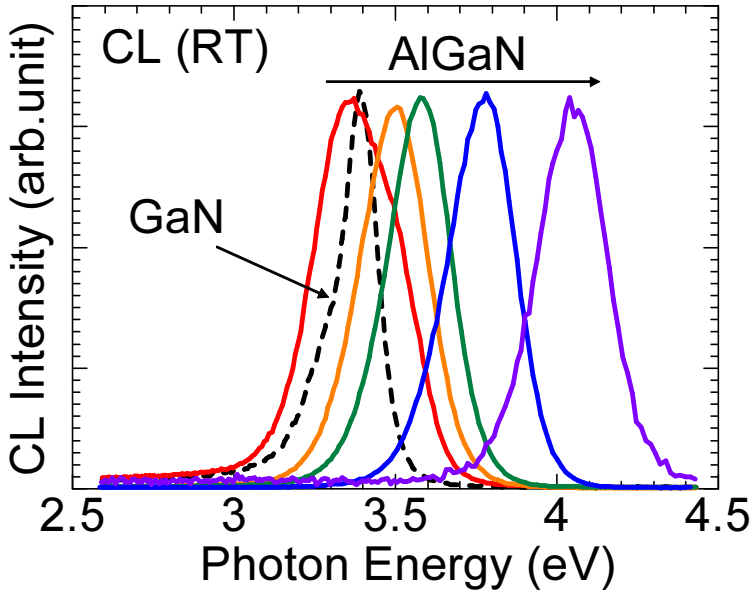


Figure 5.6: CL spectra of AlGaN grown on 4H-SiC off-axis substrates taken at RT.

Table 5.2: Calculated bandgap energy and measured CL peak energy.

Quasi-AlGaN on 4H-SiC 8° off-axis	Calculated Bandgap (eV)		CL peak energy (eV)
	Vegard's law	Kronig-Penny model	
GaN	3.42	3.42	3.39
$Al_{0.25}Ga_{0.75}N$	3.91	3.73	3.37
$Al_{0.33}Ga_{0.67}N$	4.09	3.94	3.50
$Al_{0.40}Ga_{0.60}N$	4.26	4.13	3.58
$Al_{0.50}Ga_{0.50}N$	4.51	4.44	3.78
$Al_{0.60}Ga_{0.40}N$	4.77	4.76	4.04

SIMS measurement revealed that the typical incorporation of C in GaN or AlN films was below $5\times10^{15}-5\times10^{16}$ cm^{-3}, whereas O in GaN or AlN films are $3\times10^{17}-7\times10^{17}$ cm^{-3}, so that oxygen may be responsible for the deep emission. However, the reason of the low-energy emission is currently under investigation.

5.3.4 Hall Effect Measurement

To examine the electronic properties of AlGaN layer, Hall-effect measurements were performed. For Hall-effect measurements, AlGaN/SiC heterojunction diodes that have mesa-isolated van der Pauw geometry pattern were used. The Si-doping was performed at the same cell temperature of 1300°C for all layers in this section. Fig. 5.7 (a) shows the carrier concentrations of AlGaN with various Al compositions on off-axis SiC as a function of temperature. In the case of GaN, high carrier concentrations of 1.5×10^{19} cm^{-3} at 300 K were obtained. Although it becomes more difficult to obtain high carrier concentrations when the Al composition increases because the donor ionization energy becomes large [26], reasonably high carrier concentrations of 9.7×10^{18} cm^{-3} for $Al_{0.33}Ga_{0.67}N$, 7.6×10^{18} cm^{-3} for $Al_{0.4}Ga_{0.6}N$, and 5.5×10^{18} cm^{-3} for $Al_{0.5}Ga_{0.5}N$ were obtained at 300 K. It should be noted that all AlGaN layers showed almost no temperature dependence on carrier concentrations, indicating that the AlGaN layers on off-axis SiC investigated in this study may be degenerated, so that the donor concentration is equal to carrier concentration. Assuming this, the donor concentrations are replotted in Fig. 5.7 (c). For comparison, donor concentration of AlN grown under the same condition was evaluated using *C-V* characteristics of n-AlN/p-SiC heterojunction diodes, and the calculated result is also plotted in Fig. 5.7 (c). From Hall effect measurements, MBE-grown AlGaN on off-axis SiC has adequate electronic property for the emitter of SiC HBTs. Fig. 5.7 (b) shows temperature dependence of electron mobility of AlGaN with various Al compositions on off-axis SiC. In the case of GaN, the electron mobility at 300 K was 145 cm^2/Vs. The electron mobility did not show temperature dependence because the GaN layer was degenerated. In contrast to GaN, we observed low electron mobility of 8.5 cm^2/Vs for $Al_{0.33}Ga_{0.67}N$, 3.1 cm^2/Vs for $Al_{0.4}Ga_{0.6}N$, and 1.4 cm^2/Vs for $Al_{0.5}Ga_{0.5}N$ were obtained at 300 K. The mobility showed a slight temperature dependence, where they increased with the temperature. The very low electron mobility in AlGaN is attributed to the presence of large number of edge dislocations [27–29]. It is reported that the edge dislocations introduce acceptor centers along the dislocation lines that capture electrons (negatively charged) and form a space-charge, which scatters electrons crossing them [28]. Reduced electron mobility with large number of edge dislocations was experimentally confirmed in GaN [29]. In our AlGaN, XRD measurement showed that FWHM of $(1\bar{1}02)$ reflection peak, which reflects the number of dislocations that have edge components [30], was as high as 2423 arcsec, while that of GaN grown on the same condition was 936 arcsec. So we assume the larger number of edge dislocations contributed to the reduced mobility in the case of AlGaN, which should be taken into account for the

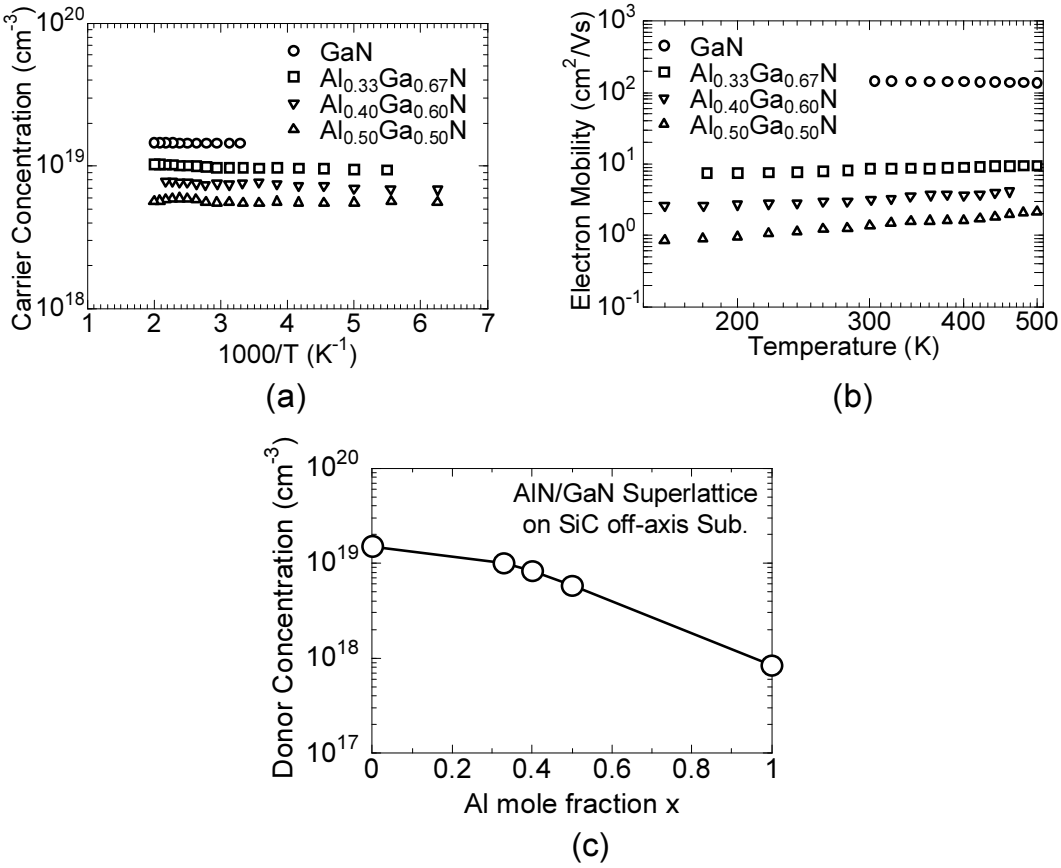


Figure 5.7: (a) Carrier concentrations and (b) electron mobility as a function of temperature of AlGaN with Al compositions of 0, 0.33, 0.40, and 0.50. (c) Donor concentration of AlGaN as a function of Al composition. For comparison, donor concentration of AlN grown under the same condition is also shown.

characterization of AlGaN/SiC HBTs.

5.4 AlGaN/SiC Heterojunction Diodes

5.4.1 Band Offset Control of AlGaN/SiC Heterojunction

To characterize the band diagram at AlGaN/SiC heterojunction, capacitance-voltage (C-V) measurements at 1 MHz were performed. Fig. 5.8 shows typical C-V characteristics of AlGaN/SiC heterojunction diodes. We obtained linear curves in $1/C^2$-V plots. The slopes in the $1/C^2$-V plot of GaN/SiC heterojunction diodes agreed well with the acceptor concentration of p-SiC layers ($N_a = 1\times10^{18}$ cm^{-3}). In the case of $Al_{0.4}Ga_{0.6}N$ and $Al_{0.5}Ga_{0.5}N$, we obtained the different slope in $1/C^2$-V plots, which are attributed to the different doping concentrations in GaN, $Al_{0.4}Ga_{0.6}N$, $Al_{0.5}Ga_{0.5}N$ films revealed by Hall effect measurements. Intercept voltages (V_d) were extracted from the $1/C^2$–V plots and they were summarized in Table 5.3. As previously reported, the intercept voltage of GaN/SiC heterojunction is 2.55 V. For $Al_{0.25}Ga_{0.75}N$/SiC and $Al_{0.33}Ga_{0.67}N$/SiC heterojunction, the intercept voltages were nearly equal to that of GaN, and we observed their monotonic increase when the Al composition exceeded 0.4. From this V_{int} value, the energy-band diagrams of the AlGaN/SiC heterojunction are calculated using equation shown below:

$$\Delta E_v = E_{g,GaN} - qV_d - \delta_{SiC} - \delta_{GaN} \tag{5.1}$$

$$\Delta E_c = qV_d - E_{g,SiC} + \delta_{SiC} + \delta_{GaN} \tag{5.2}$$

where E_g is the bandgap energy, and δ_{SiC} and δ_{GaN} are the differences between the Fermi level and the valence-band maximum of SiC and conduction-band minimum of GaN, respectively. We used the bandgap of AlGaN calculated using Kronig-Penny model shown in Table 5.2 in this study.

The C-V analysis revealed that there is a large valence band offset (ΔE_V) of about 0.4 - 1.0 eV in AlGaN/SiC heterojunction which sufficiently blocks hole back injection from p-SiC to n-AlGaN. As for conduction band offset (ΔE_C), there is also a large ΔE_C in the case of GaN/SiC heterojunction which works as a potential barrier to electron as previously reported (type-Ⅱ band alignment). The ΔE_C value remained almost constant in the case of $Al_{0.25}Ga_{0.75}N$/SiC and $Al_{0.33}Ga_{0.67}N$/SiC heterojunction. And we observed their monotonic increase when the Al composition exceeded 0.4. With Al composition of over 0.5, we achieved Type-I band alignment, which is suitable for HBTs (see Fig. 5.9). It should be noted that although there are a few reports on trial of the band offset control, no groups achieved type-I band alignment in AlGaN/SiC heterojunction. Danielsson *et al.* reported that the conduction band offset values were almost unchanged with increasing Al compositions up to 0.5, although ΔE_C was expected to decrease toward zero since ΔE_C will finally approach the value of the AlN/SiC heterojunction. They assumed it to be due

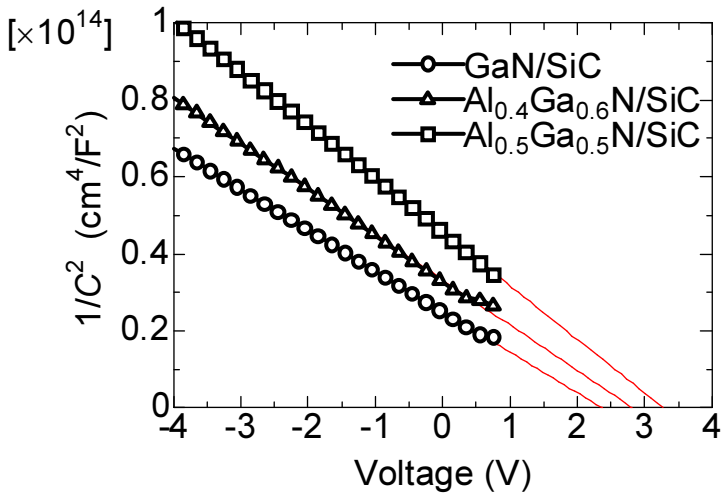


Figure 5.8: Room temperature C-V characteristics of AlGaN/SiC heterojunction diodes..

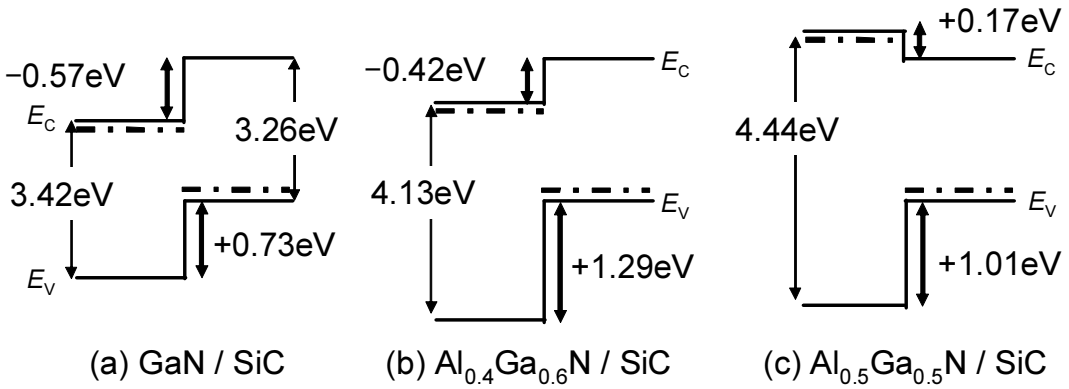


Figure 5.9: Flat band diagram of (a) GaN/SiC, (b) $Al_{0.4}Ga_{0.6}N$/SiC, and (c) $Al_{0.5}Ga_{0.5}N$/SiC heterojunctions, as calculated on the basis of the intercept voltages in C-V measurements.

Table 5.3: Built-in voltage and calculated conduction and valance band offset at AlGaN/SiC heterojunction.

Emitter	Intercept Voltage (V)	ΔE_C (eV)	ΔE_V (eV)
GaN/AlN(1nm)	2.55	-0.57	0.73
$Al_{0.25}Ga_{0.75}N$	2.51	-0.58	1.06
$Al_{0.33}Ga_{0.67}N$	2.54	-0.59	1.27
$Al_{0.40}Ga_{0.60}N$	2.70	-0.42	1.29
$Al_{0.50}Ga_{0.50}N$	3.28	0.17	1.01
$Al_{0.60}Ga_{0.40}N$	4.17	1.07	0.42

to the presence of strong interface charge influencing *C-V* measurement. Johnson *et al.* reported the the band alignment of $Al_{0.3}Ga_{0.7}N$/SiC and $Al_{0.5}Ga_{0.5}N$/SiC were type-Ⅱ with $|\Delta E_C|$ of 0.30 eV and 0.56 eV, respectively [31]. Note that in these two reports they did not employ superlattice structure but used conventional AlGaN growth method either by HVPE [21] or CVD [31]. In contrast to these reports, we achieved type-I band alignment with Al compositions of over 0.5, indicating that our method to form the heterojunction, i.e. growth method featuring AlN/GaN superlattice, is applicable to control the band offset.

5.4.2 Current Transport Properties of AlGaN/SiC Heterojunction

The AlGaN/SiC heterojunction diodes with various Al compositions are fabricated and characterized. *I-V* characteristics of the n-AlGaN/p-SiC heterojunction diodes are shown in Fig. 5.10. Under reverse bias, all diodes showed very small reverse leakage current. Under forward bias, *I-V* characteristics showed different thresholds. In particular, GaN/SiC diodes showed the lowest threshold whereas AlGaN/SiC diodes with Al composition of 0.25 and 0.33 showed higher thresholds, and highest thresholds were obtained in the diodes with Al composition of 0.5 and 0.6. The different thresholds may be attributed to the reduction of recombination current via interface traps by using high Al-content AlGaN, which is explained using Fig. 5.11. For GaN/SiC heterojunction, potential barrier to electron due to the type-Ⅱ band alignment blocked the carrier injection and produces high electron concentrations near the interface. The accumulated electrons recombine via interface traps with holes that are also accumulated near the heterojunction due to the potential barrier. Thus, we observed the recombination current at small bias. Similar discussions are found in other reports [15–18], where the electrical characteristics are intensively investigated. For AlGaN/SiC heterojunction with Al composition of over 0.5, similar current transport mechanism can occur. However, we did not observe the leakage current at small bias, suggesting the reduction of recombination current via interface traps by using high Al-content AlGaN. Since the major difference was the elimination of potential barrier to electron with high Al-content AlGaN, one possible explanation of the different threshold in *I-V* characteristics is associated with the eliminated potential barrier to electron injection.

5.5 AlGaN/SiC HBTs

5.5.1 Common-Base Mode Operation

The AlGaN/SiC HBTs with different Al compositions are fabricated and characterized. HBTs with an emitter finger width of $W_E = 10$ μm and the distance between emitter and base of $L_{EB} = 10$ μm (total area: 140 μm × 320 μm) were used in this study.

Fig. 5.12 shows the common-base I_C-V_{CB} characteristics of GaN/SiC HBTs,

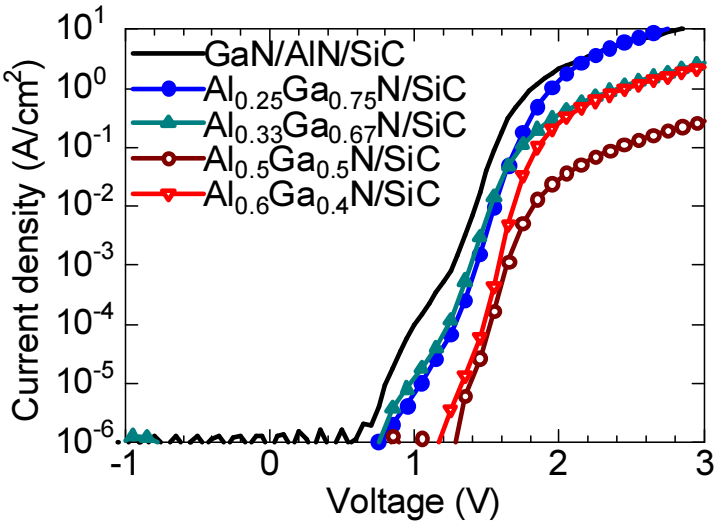


Figure 5.10: *I-V* characteristics of the n-AlGaN/p-SiC heterojunction diodes.

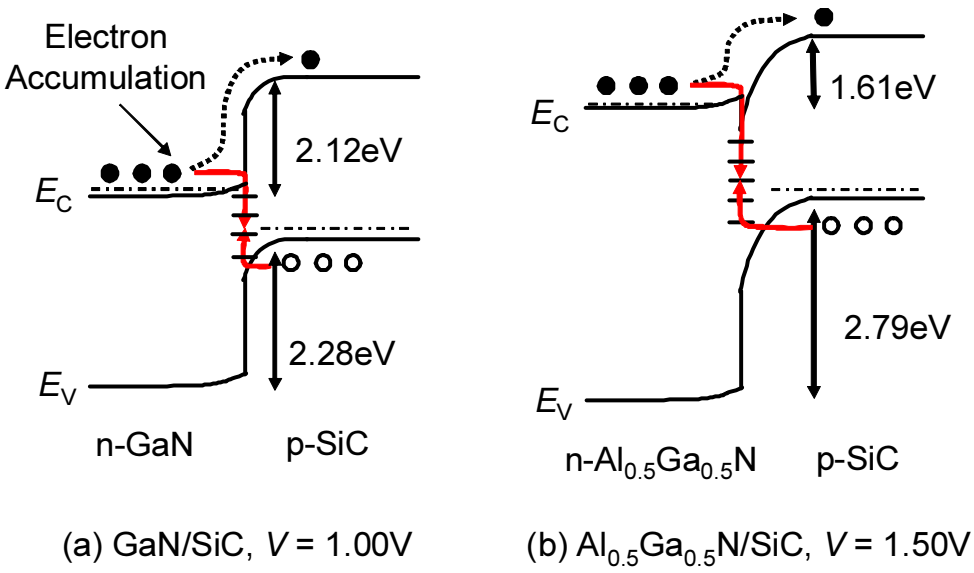


Figure 5.11: Schematic band diagrams of n-GaN/p-SiC and n-$Al_{0.5}Ga_{0.5}N$/p-SiC under the forward bias near turn-on voltage.

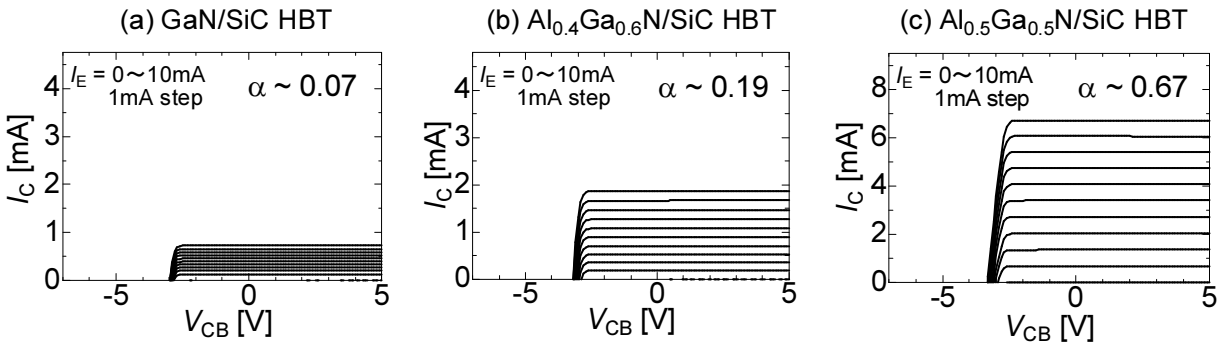


Figure 5.12: Common-base I_C-V_{CB} characteristics of (a) GaN/SiC HBTs, (b) $Al_{0.4}Ga_{0.6}N$/SiC HBTs, and (c) $Al_{0.5}Ga_{0.5}N$/SiC HBTs.

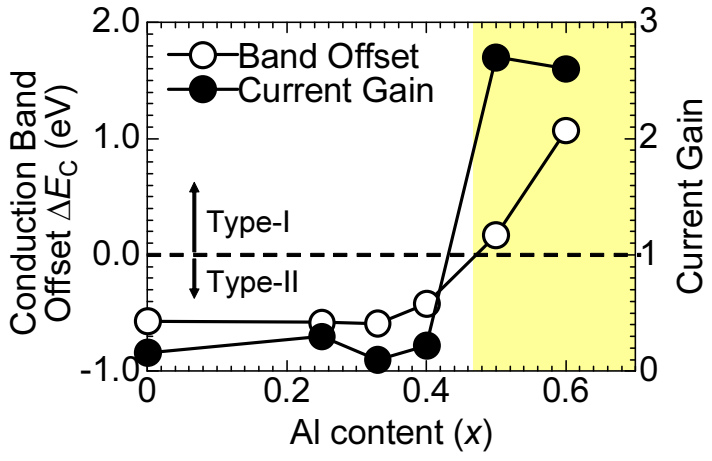


Figure 5.13: Correlation between band offset at AlGaN/SiC heterojunction and current gain of AlGaN/SiC HBTs..

$Al_{0.4}Ga_{0.6}N$/SiC HBTs, and $Al_{0.5}Ga_{0.5}N$/SiC HBTs. A summary of current gain of the HBTs are also shown in Table 5.4. All HBTs showed common-base characteristics, with no significant leakage. The GaN/SiC HBTs showed a common-base current gain of $\alpha \sim 0.07$. AlGaN/SiC HBTs with Al content below 0.5 exhibited a low current gain of $\alpha \sim 0.2$, whereas HBTs with Al content over 0.5 exhibited significantly improved current gain, up to $\alpha \sim 0.67$.

The improvement of current gain is associated with the band alignment of AlGaN/SiC heterojunction, which is illustrated in Fig. 5.13. As revealed by *C-V* measurement, AlGaN/SiC heterojunction with Al composition below 0.4 showed type-II band alignment. This band alignment forms the large potential barrier to electron injection from n-AlGaN to p-SiC, resulting in low emitter injection efficiency. On the other hand, with AlGaN emitter with Al content over 0.5, type-I band alignment that is free from such potential barrier was realized, so that the higher electron injection efficiency and thus improved current gain were achieved. *I-V* measurements also suggested reduced recombination current when the quasi-AlGaN emitter was used with Al content over 0.5.

5.5.2 Common-Emitter Mode Operation

It should be noted that $\alpha > 0.5$ indicates a common-emitter current gain $\beta > 1$. The common-emitter I_C-V_{CE} characteristics and the Gummel plot of the $Al_{0.5}Ga_{0.5}N$/SiC HBT are shown in Fig. 5.14. It should be noted that the open-base blocking voltage V_{CEO} of the HBT was larger than 1 kV, even though any passivation or junction termination extension was not employed in the HBTs. Current gain was observed above V_{BE} of 2.8 V, indicating electron injection from AlGaN to SiC becomes dominant above the voltage. A maximum common-emitter current gain of $\beta \sim 2.7$ was demonstrated in the HBTs.

5.5.3 High Temperature Characteristics

To further discuss the characteristics of AlGaN/SiC HBTs, we investigated the high temperature characteristics. The high temperature characteristics of the $Al_{0.5}Ga_{0.5}N$/SiC HBT are shown in Fig. 5.15. In Fig. 5.15, characteristics at RT and 550 K are shown. The HBT showed the operation at up to 550 K, and it did not show any degradation after the cooling off. We observed the increase of ON-resistance at 550 K, which is attributed to the increase of mobility of drift region at elevated temperature. The current gain was reduced from 2.7 at RT to 0.6 at 550 K. It is well known that the current gain decreases with the temperature in SiC BJTs because ionized acceptors in p-SiC base are injected to the emitter that reduce the emitter injection efficiency. In the ideal HBTs, such hole back injection is suppressed due to the presence of potential barrier to hole at the heterojunction, so that the electron injection efficiency is not affected by the increase of carrier concentrations. However, the HBT showed significant reduction of current gain. The reduction of the current gain indi-

Table 5.4: Common-base and common-emitter current gain of fabricated HBTs.

HBT	Common-Base Gain α	Common-Emitter Gain β
GaN/SiC	0.07	0.16
$Al_{0.25}Ga_{0.75}N$/SiC	0.15	0.3
$Al_{0.33}Ga_{0.67}N$/SiC	0.1	0.1
$Al_{0.40}Ga_{0.60}N$/SiC	0.19	0.22
$Al_{0.50}Ga_{0.50}N$/SiC	0.67	2.7
$Al_{0.60}Ga_{0.40}N$/SiC	0.66	2.6

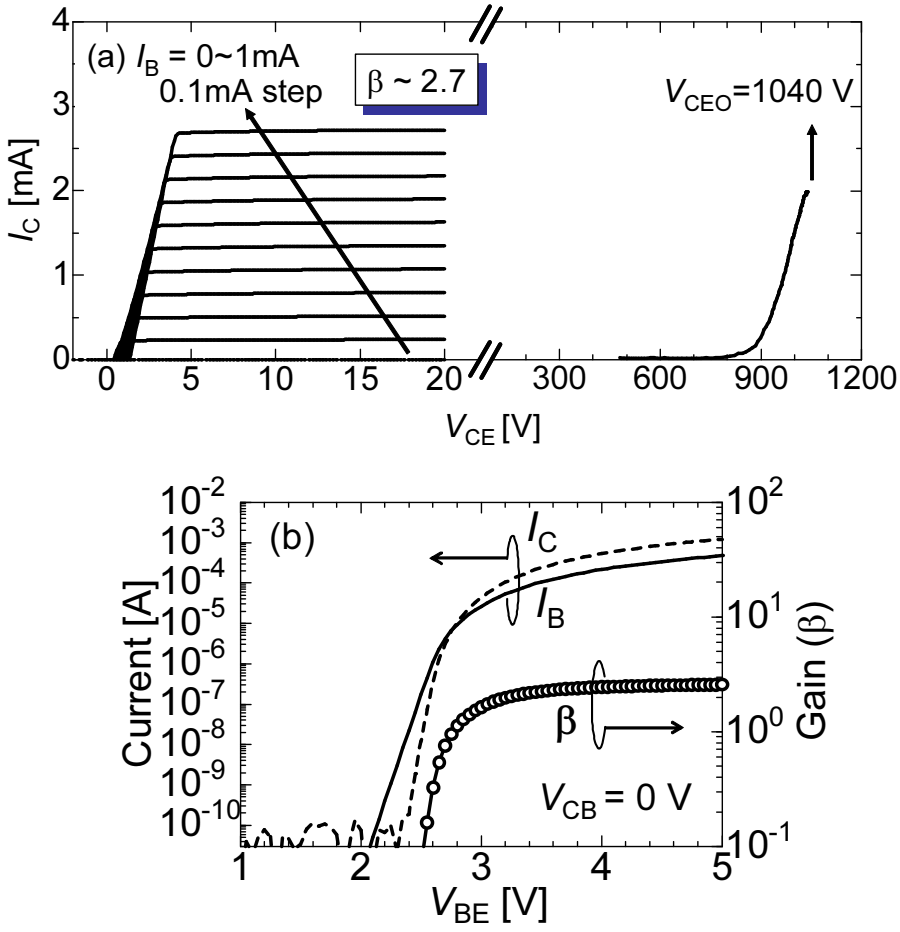


Figure 5.14: (a) Common-emitter I_C-V_{CE} characteristics and open-base breakdown voltages in $Al_{0.5}Ga_{0.5}N$/SiC HBTs. (b) A Gummel plot of an $Al_{0.5}Ga_{0.5}N$/SiC HBT.

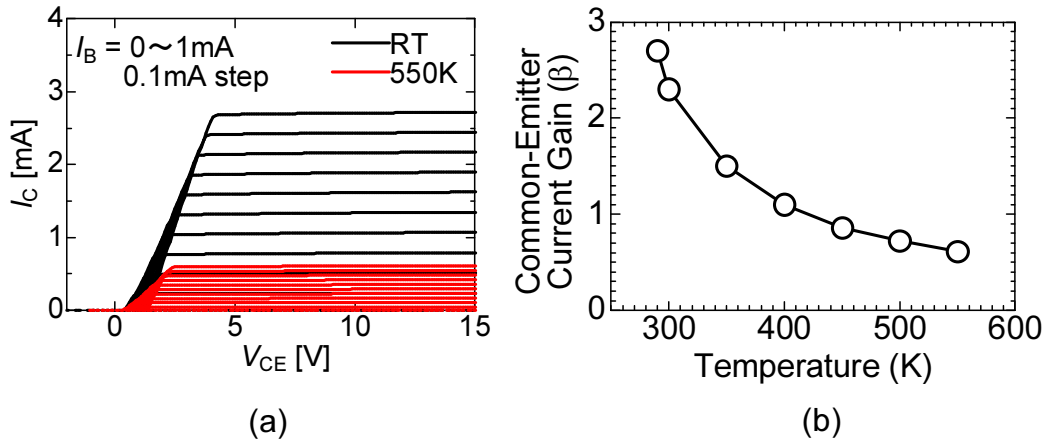


Figure 5.15: High temperature characteristics of the $Al_{0.5}Ga_{0.5}N$/SiC HBT.

cates the evidence that the increased carrier concentrations in p-SiC base contributed to the reduced emitter injection efficiency, i.e., recombination at the heterojunction via interface states, suggesting that further reduction of interface states at AlGaN/SiC heterojunction is necessary to improve the current gain.

5.5.4 Carrier Injection Investigated by Electroluminescence

To discuss the current transport mechanism in GaN/SiC heterojunction, electroluminescence (EL) of the HBTs was investigated. EL from $Al_{0.4}Ga_{0.6}N$/SiC HBTs and $Al_{0.5}Ga_{0.5}N$/SiC HBTs during the operation in active region at the base current of 1 mA are shown in Fig. 5.16 (a) and (b). Yellow EL was observed from $Al_{0.4}Ga_{0.6}N$/SiC HBTs, whereas blue EL was observed from $Al_{0.5}Ga_{0.5}N$/SiC HBTs. This indicates a different current transport mechanism is dominant in the heterojunction.

In $Al_{0.4}Ga_{0.6}N$/SiC HBTs that have type-Ⅱ band alignment, there is a potential barrier to electron injection from n-AlGaN to p-SiC so that most electrons are forced to recombine at n-AlGaN/n-SiC interface. Thus, the yellow EL from $Al_{0.4}Ga_{0.6}N$/SiC HBTs may be associated with the recombination at n-AlGaN/n-SiC (see Fig. 5.17). On the other hand, $Al_{0.5}Ga_{0.5}N$/SiC HBTs, which have type-I band alignment, have no potential barrier to electron injection so that most electrons pass through n-AlGaN/n-SiC interface and they may recombine in n-SiC spacer or p-SiC base. It was reported that the luminescence associated with p^+-SiC is dark red [19], whereas the luminescence associated with n^--SiC is typically blue. Thus, the blue EL from $Al_{0.5}Ga_{0.5}N$/SiC HBTs indicates the recombination in n^--SiC spacer region.

5.5.5 Effect of n-SiC Spacer Layer and p-SiC Base Width

In high temperature characteristics, it was suggested that main bottleneck in limiting the current gain is interface recombination at AlGaN/SiC heterojunction. To solve this issue, we investigated the impact of n-SiC spacer width. The function of the n-SiC spacer layer is illustrated in Fig. 5.18. Without n-SiC spacer, some of the injected carriers from n-AlGaN to p-SiC can be trapped at the interface states in AlGaN/SiC heterojunction. These trapped carriers can recombine with the holes supplied from p-SiC, resulting in the large recombination. With n^--SiC spacer between n-AlGaN and p-SiC, although some injected electrons can be trapped at the AlGaN/SiC interface, the number of holes that contribute to the recombination can be reduced since the energy gap between valence band maximum and quasi-Fermi level E_{fP} becomes larger, resulting in lower recombination and thereby higher current gain. In this study, we investigated the spacer thickness of 50, 100, and 200 nm. For the 200 nm-thick n-SiC spacer, HBTs with the base thickness of 500 nm and 250 nm are fabricated. Fig. 5.19 shows the Gummel plot and common-emitter I_{C}-V_{CE} characteristics of AlGaN/SiC HBTs with 50 nm- and 200 nm-thick n-SiC spacer. Although the current gain

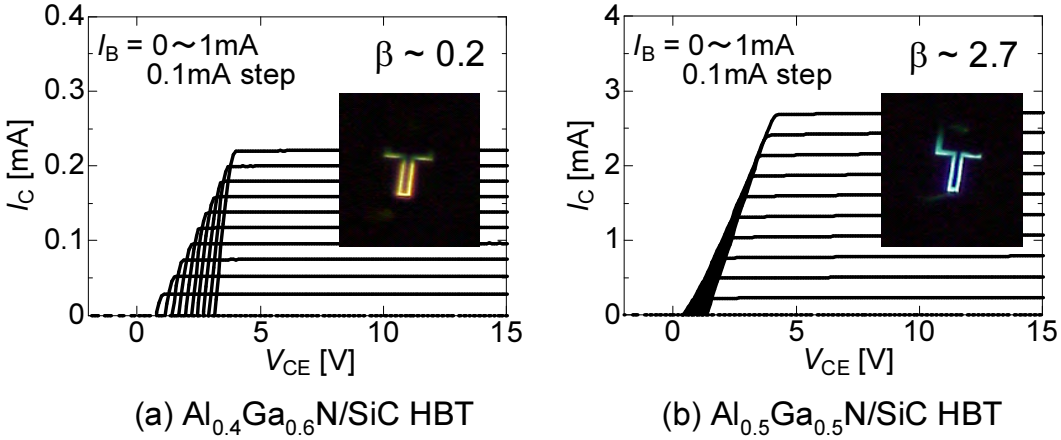


Figure 5.16: Common-emitter I_C-V_{CE} characteristics of (a) $Al_{0.4}Ga_{0.6}N$/SiC HBTs and (b) $Al_{0.5}Ga_{0.5}N$/SiC HBTs. The inset shows EL during the operation at the base current of 1 mA.

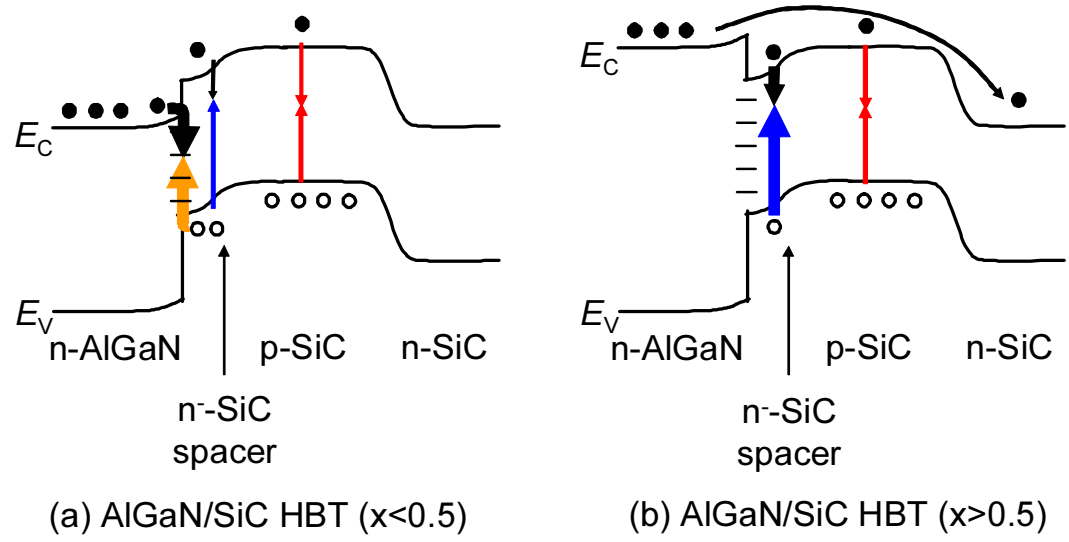


Figure 5.17: Schematic band diagrams and corresponding EL of n-GaN/p-SiC and n-$Al_{0.5}Ga_{0.5}N$/p-SiC.

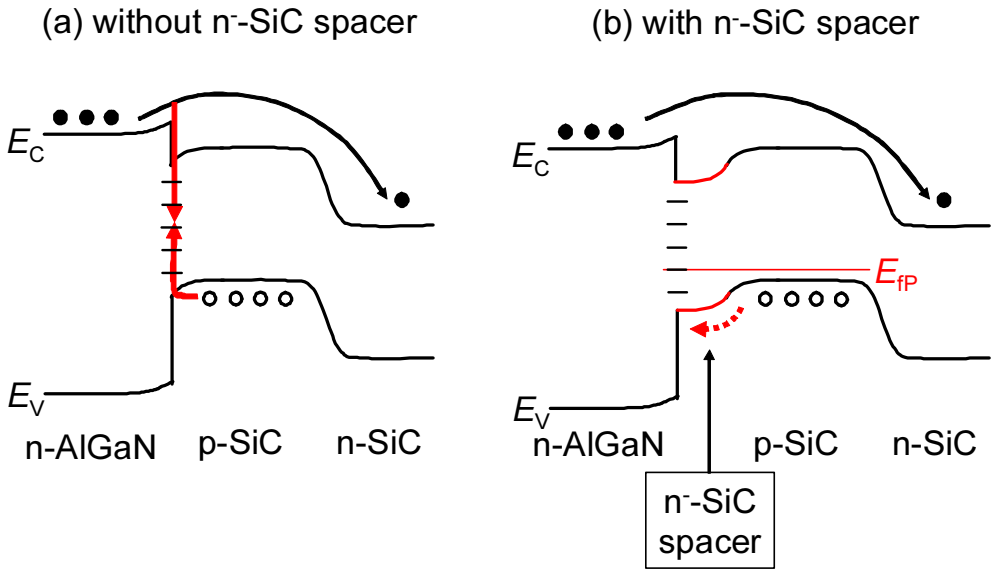


Figure 5.18: Function of the n-SiC spacer layer in AlGaN/SiC HBTs. With n-SiC spacer between n-AlGaN and p-SiC, although some injected electrons can be trapped at the AlGaN/SiC interface, the number of holes that contribute to the recombination can be reduced since the energy gap between valence band maximum and quasi-Fermi level E_{fP} becomes larger.

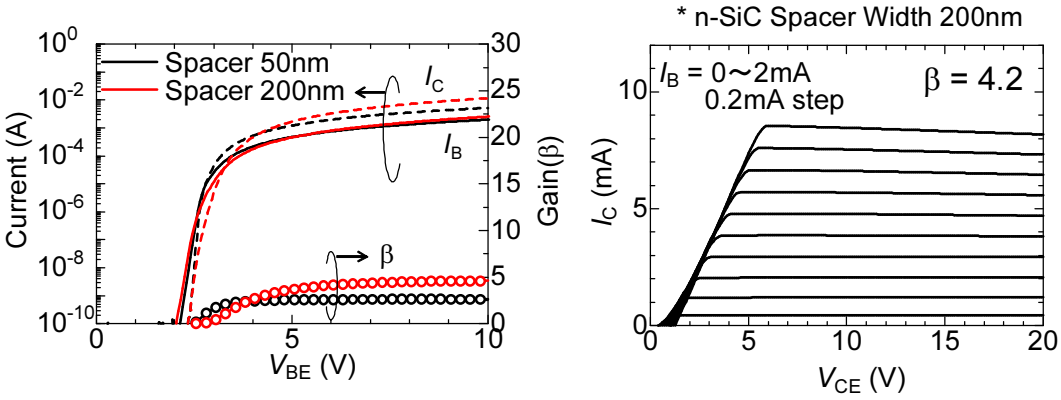


Figure 5.19: Gummel plot and common-emitter I_C-V_{CE} characteristics of AlGaN/SiC HBTs with 50 nm- and 200 nm-thick n-SiC spacer. Although the current gain was 2.7 with 50 nm-thick n-SiC spacer, the current gain was improved to 4.2 by utilizing 200 nm-thick n-SiC spacer.

was 2.7 with 50 nm-thick n-SiC spacer, the current gain was improved to 4.2 by utilizing 200 nm-thick n-SiC spacer. It should be noted that the current gain showed a tendency that it increased with n-SiC spacer thickness, indicating that the implementing of n-SiC spacer is effective to suppress the interface recombination at the AlGaN/SiC heterojunction.

We also note that in the case of HBTs with 200 nm-thick n-SiC spacer, the current gain was significantly improved by utilizing 250 nm-thick p-SiC base. Fig. 5.20 shows the Gummel plot and common-emitter I_{C}-V_{CE} characteristics of AlGaN/SiC HBTs with 500nm- and 250 nm-thick p-SiC base. As shown in Fig. 5.20, the base current in Gummel plot was suppressed due to the reduced bulk recombination by a short base, resulting in a maximum current gain of 13, which is 3 times higher current gain compared with the case of base thickness of 500 nm. In other words, it turned out that the suppression of recombination current in p-SiC base also plays an important role limiting current gain in the HBTs, although we have focused on the reduction of interface recombination.

5.5.6 Discussion

Here, common-emitter current gain β is expressed as:

$$\beta = \frac{\alpha}{1-\alpha} \tag{5.3}$$

and common-base current gain α is expressed as the product of emitter injection efficiency γ and base transport factor α_T:

$$\alpha = \gamma \times \alpha_{\mathrm{T}} \tag{5.4}$$

$$\gamma = 1 - \frac{D_{\mathrm{pE}} W_{\mathrm{B}} p_{\mathrm{E}}}{D_{\mathrm{nB}} L_{\mathrm{pE}} n_{\mathrm{B}}} \cdot \exp\left(\frac{-\Delta E_{\mathrm{g}}}{kT}\right) \tag{5.5}$$

$$\alpha_{\mathrm{T}} = \frac{1}{\cosh\left(\frac{W_{\mathrm{B}}}{L_{\mathrm{nB}}}\right)} \sim 1 - \frac{1}{2}\left(\frac{W_{\mathrm{B}}}{L_{\mathrm{nB}}}\right)^2 \left(\because \cosh\left(\frac{W_{\mathrm{B}}}{L_{\mathrm{nB}}}\right) = 1 + \frac{1}{2}\left(\frac{W_{\mathrm{B}}}{L_{\mathrm{nB}}}\right)^2 \text{when } \frac{W_{\mathrm{B}}}{L_{\mathrm{nB}}} \ll 1 \right) \tag{5.6}$$

where D_{pE} diffusion coefficient of holes in n-emitter, D_{nB} diffusion coefficient of electron in p-base, W_{B} base width, L_{pE} diffusion length of hole, p_{E} minority carrier concentration in equilibrium within the n-emitter, n_{B} minority carrier concentration in equilibrium within the p-base.

Using these equations and the results $\beta = 4.2$ ($\alpha \sim 0.808$) for 500 nm-base HBTs and $\beta = 13$ ($\alpha \sim 0.929$) for 250 nm-base HBTs and, γ and α_{T} are estimated to be 0.907 and 0.901 for 500 nm-base HBTs and 0.953 and 0.975 for 250 nm-base HBTs, respectively.

As shown in Table 5.5, base transport factor was significantly improved by utilizing 250 nm-thick base. Emitter injection efficiency was also improved as well, so that the

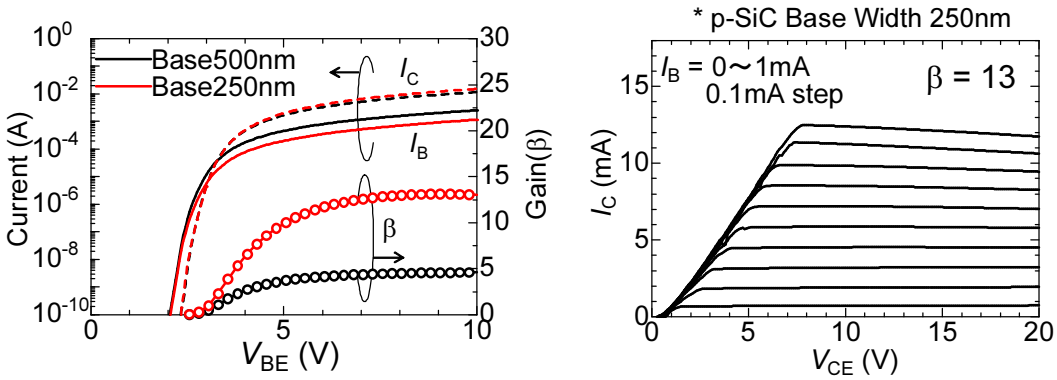


Figure 5.20: Gummel plot and common-emitter I_C-V_{CE} characteristics of AlGaN/SiC HBTs with 500nm- and 250 nm-thick p-SiC base. A maximum current gain of 13 was obtained.

Table 5.5: Common-emitter current gain (β), common-base current gain (α), and calculated emitter injection efficiency (γ) and base transport factor (α_T) of AlGaN/SiC HBTs with base thickness of 500 nm and 250 nm.

Base Width	β	α	γ	α_T
500 nm	4.2	0.808	0.907	0.901
250 nm	13	0.929	0.953	0.975

base width significantly affected the current gain of the HBTs. It should be noted that the emitter injection efficiency over 0.9 was realized by utilizing AlGaN emitter since our previous 500 nm-base GaN/SiC HBTs showed low current gain of $\alpha \sim 0.2$ where the emitter injection efficiency γ was ~ 0.22 assuming $\alpha_{\mathrm{T}} \sim 0.901$. So it can now be concluded that the dominant factor limiting the current gain is not only the emitter injection efficiency but also the base transport factor. Thus, continuous work on the control of AlGaN/SiC heterojunction as well as the control of the carrier lifetime of p-SiC base will be necessary to achieve high current gain in AlGaN/SiC HBTs.

5.6 Atomic Control of AlGaN/SiC Heterojunction and Its Impact on HBT Performance

5.6.1 Motivation

In the previous section, we investigated the utilization of AlGaN emitter featuring AlN/GaN superlattice and optimization of n-SiC spacer and p-SiC base width. With these efforts, we have successfully demonstrated the band offset control of AlGaN/SiC and operation with common-emitter current gain of $\beta \sim 13$. However, the further improvement of current gain is necessary to meet practical requirements.

One of the factors limiting the current gain is the chemical valence mismatch at AlGaN/SiC. This heterojunction, where the materials with different valency (SiC: Ⅳ-Ⅳ, Ⅲ-N: Ⅲ-Ⅳ) form the heterojunction, is referred to as *heterovalent heterojunction* and there are electron-excess or electron-deficient bonds at the interface [32], e.g. Si-N bonds and Al-C bonds can be formed at AlN/SiC [33]. In AlGaN/SiC$(0001)_{\mathrm{Si}}$ heterojunction, Si-N bonds are preferentially formed. Each Si-N bond has an excess electron so that there is a donor-like charge accumulation at the interface, affecting the electronic properties. Since no charge states would be preferable from the viewpoint of electron injection efficiency in AlGaN/SiC HBTs, it is important to compensate the charge balance and realize neutralized interface by introducing electron-deficient bonds, e.g. Al-C. However, there have been no experimental reports concerning such atomic control of the interface.

In this study, we conduct the atomic control of AlGaN/SiC heterointerface toward high-current-gain AlGaN/SiC HBTs. To compensate the charge states at the AlGaN/SiC, we investigate C pre-irradiation prior to the growth. This aims at the formation of the mixed interface with Si-N and Al-C, which is reported to be most favorable atomic arrangements with no charge states [32], as illustrated in Fig. 5.22. For comparison, Si pre-irradiation is also investigated. The correlation between various pre-irradiation and HBT performance is presented in this paper.

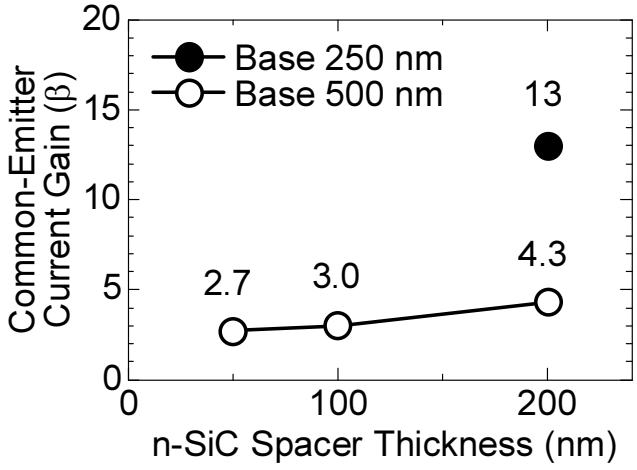


Figure 5.21: Summary of fabricated HBT with different n-SiC spacer and p-SiC base thickness.

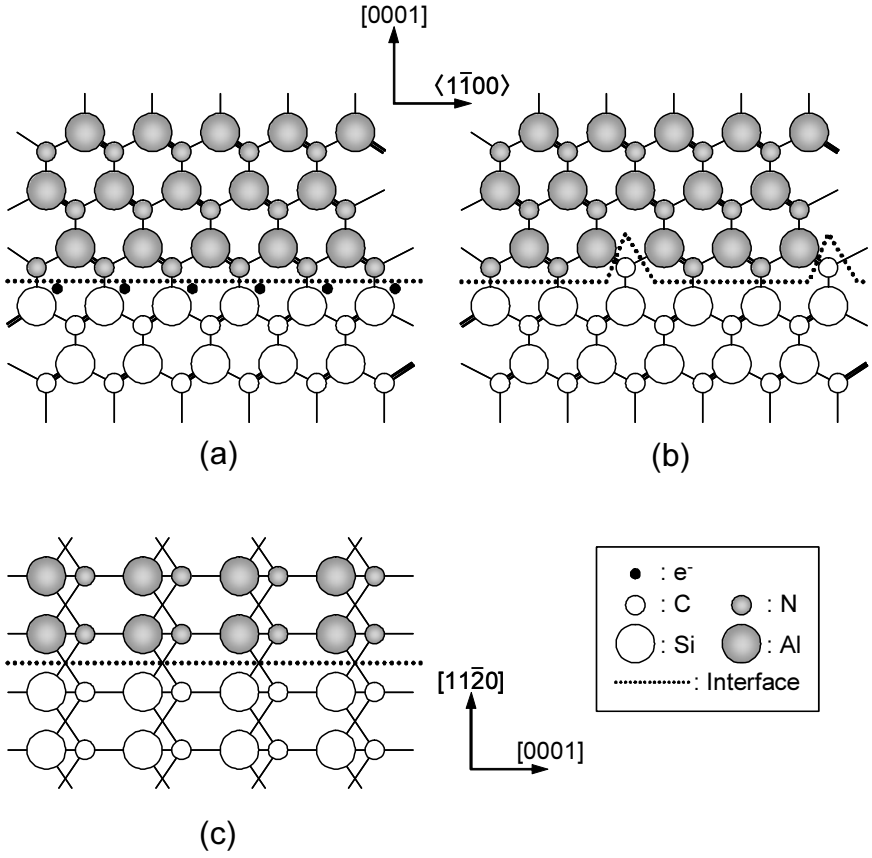


Figure 5.22: Schematic illustration of bond configuration of Al(Ga)N/SiC heterojunction grown on (a) SiC(0001)Si-face (b) SiC(0001)Si-face with C-adsorbed layer.

5.6.2 Device Fabrication

Fig. 5.23 shows a schematic cross section of a fabricated AlGaN/SiC HBT and AlN/SiC HBT (will be discussed in the next section). We used n-type 4H-SiC (0001) 8° off-axis Si-face substrates. N^+-SiC substrates with a N-doped n^--SiC collector layer (10 μm, $N_d = 5\times10^{15}$ cm^{-3}), an Al-doped p^+-SiC base layer (0.5 μm, $N_a = 1\times10^{18}$ cm^{-3}), and an n^--SiC spacer layer (0.05 μm, $N_d = 1\times10^{16}$ cm^{-3}) were prepared by chemical vapor deposition. Ⅲ nitride (Ⅲ-N) layers were then grown by plasma-assisted molecular beam epitaxy (MBE). Prior to the growth, C or Si pre-irradiation was performed using current-controlled sublimation cell. Deposition of these atoms was monitored by *in-situ* RHEED system. Before pre-irradiation, SiC surface showed $\sqrt{3}\times\sqrt{3}$ R30° pattern which suggests O-contamination free. Deposition of 1 ML of C or Si atoms are determined when the $\sqrt{3}\times\sqrt{3}$ R30° pattern changed to 1×1 pattern (see Fig. 5.24). Using the deposition rate calibrated above, 1/3, 2/3, or 1 ML C- or Si-deposited surface are prepared. Then a Si-doped n-quasi-AlGaN (100 nm, $N_d \sim 5\times10^{18}$ cm^{-3}, stack of AlN(0.6 nm)/GaN (0.6 nm) short-period superlattice), followed by a Si-doped n^+-GaN contact layer (200 nm, $N_d = 2\times10^{19}$ cm^{-3}) were grown for AlGaN/SiC HBTs, whereas a Si-doped n-AlN (80 nm, [Si] = 2×10^{19} cm^{-3}) followed by n^+-GaN contact layer were grown for AlN/SiC HBTs. AlGaN/SiC HBT without any pre-irradiation and with initial Al, Ga pre-irradiation are fabricated as a reference.

Double-mesa HBTs were fabricated using reactive ion etching (RIE) with a deposited SiO_2 mask. Multilayer Ti/Al/Ni were deposited onto the n-GaN and p-SiC surface and they were sintered in Ar at 600°C.

5.6.3 Impact of Al, Ga Pre-Irradiation on AlGaN/SiC HBT Performance

Fig. 5.25 (a) shows common-emitter current gains of reference HBTs as a function of collector current. Reference HBTs shown in Fig. 5.25 (a) showed a peak current gain of 5.1. HBTs grown by Ga or Al pre-irradiation showed slightly higher current gain of 5.4 and 5.5, respectively. The improvement of current gain may be attributed to the change of initial growth mode of AlGaN on SiC. It is reported that reduced-defect-density AlN can be grown in the presence of Ga since it works as a surfactant during AlN growth [34]. Since we started the quasi-AlGaN growth with AlN, such growth mode change can contribute to the improvement of current gain. As for Al pre-irradiation, we speculate that it contributed to the different interface compositions (i.e. Al-rich), which affected the growth mode and current gain.

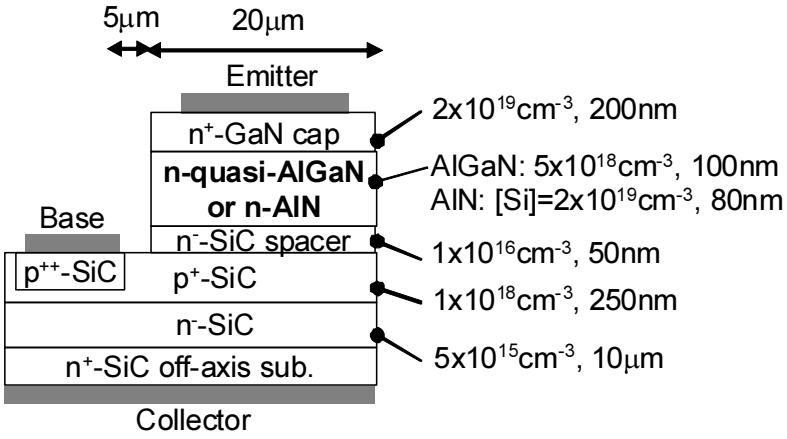


Figure 5.23: Schematic cross section of a fabricated AlGaN/SiC and AlN/SiC HBT.

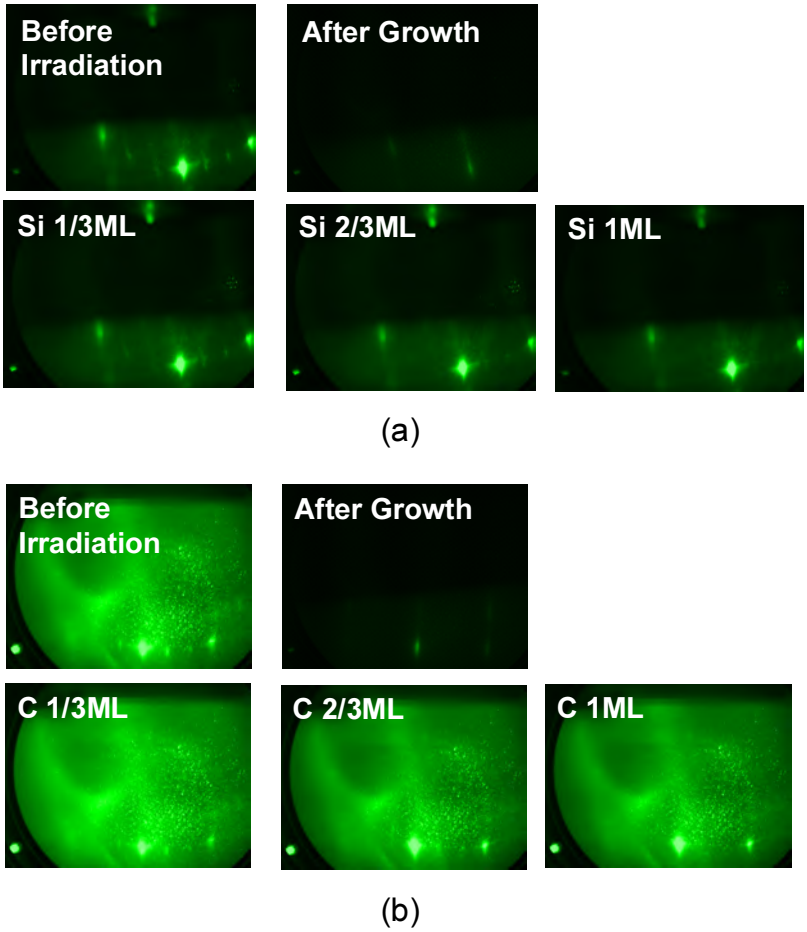


Figure 5.24: RHEED pattern during Si or C sublimation. Before pre-irradiation, SiC surface showed $\sqrt{3} \times \sqrt{3}$ R30° pattern. Deposition of 1 ML of C or Si atoms are determined when the $\sqrt{3} \times \sqrt{3}$ R30° pattern changed to 1×1 pattern.

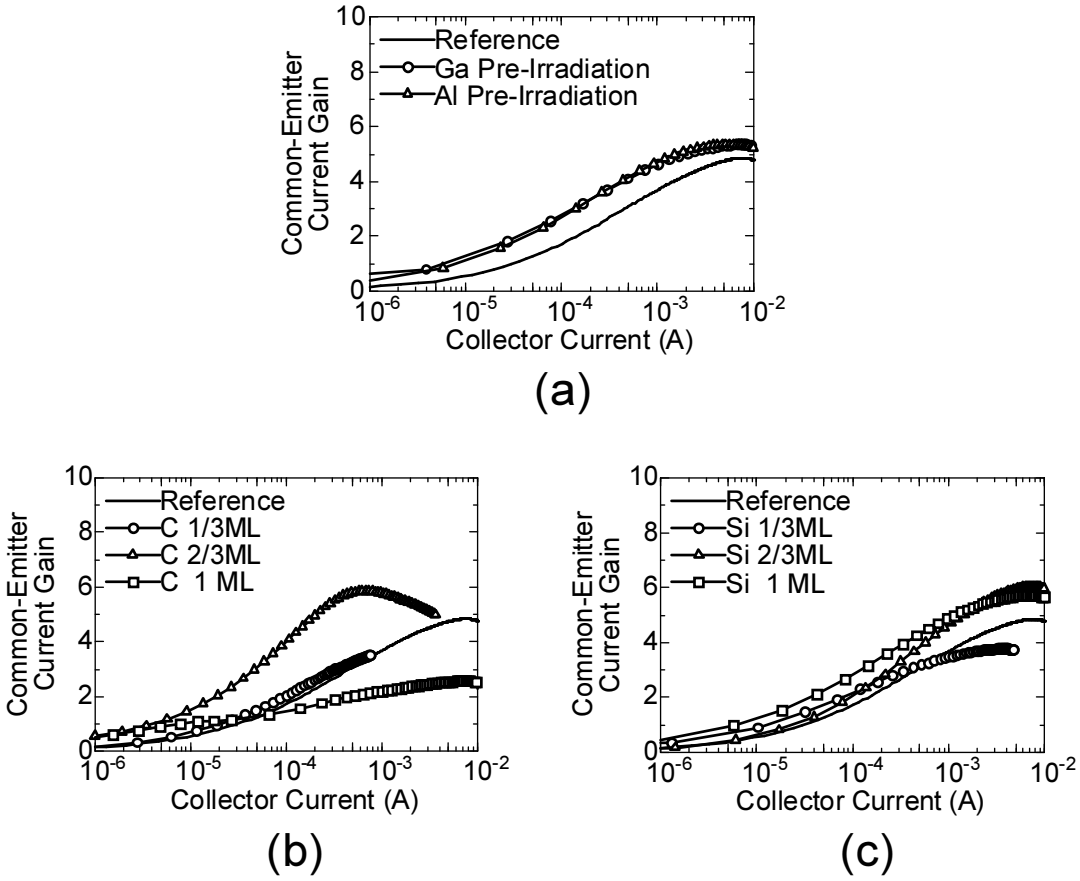


Figure 5.25: Common-emitter current gains of HBTs as a function of collector current grown by various pre-irradiation (a) Ga and Al (b) C (c) Si.

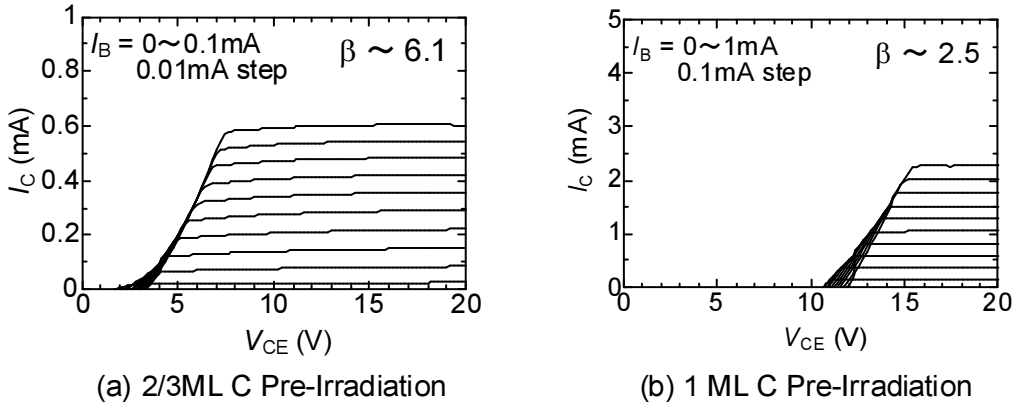


Figure 5.26: Common-emitter I_C-V_{CE} characteristics of $Al_{0.5}Ga_{0.5}N$/SiC HBTs grown by (a) 2/3 ML C pre-irradiation (b) 1 ML C pre-irradiation.

5.6.4 Impact of Si, C Pre-Irradiation on AlGaN/SiC HBT Performance

Fig. 5.25 (b) shows common-emitter current gains of HBTs as a function of collector current grown by C pre-irradiation. HBTs grown by 1/3 ML C pre-irradiation did not show any significant difference with reference HBTs in the measured range, whereas HBTs grown by 2/3 ML C pre-irradiation showed improved current gain of 6.1, as shown in Fig. 5.26 (a). This result indicates that C pre-irradiation may form Al-C bonds (mixed interface with Si-N and Al-C) and compensate the charge states in AlGaN/SiC, resulting in an improved current gain. On the other hand, HBTs grown by 1 ML C pre-irradiation showed reduced current gain of 2.5, and common-emitter characteristics showed large forward voltage drop of 10V (Fig. 5.26 (b)). It is known that C can work as a deep acceptor in AlN so that this result suggests the deposition of 1 ML C contributed to the formation of highly resistive region associated with deep levels [35].

We have also conducted Si pre-irradiation prior to the growth. Fig. 5.25 (c) shows common-emitter current gains of HBTs as a function of collector current grown by Si pre-irradiation. HBTs grown by 1/3 ML Si pre-irradiation showed reduced current gain of 4.0, whereas HBTs grown by 2/3 ML and 1 ML Si pre-irradiation showed improved current gain of 6.3 and 6.2, respectively. This improvement may be associated with Si incorporation in epilayers during MBE growth. It is known that when the AlN layer is grown on SiC under the metal-rich condition, out-diffusion of Si from SiC surface occur and large amount of Si are incorporated in the epilayer [36]. It is also known that when the GaN/AlN stack layer is grown, accumulation of the Si is observed at the GaN/AlN interface since the Si out-diffusion may not occur in GaN [36]. In fact, we observed similar phenomena in our GaN/AlN stack grown under metal-rich condition (Si pre-irradiation was not used) (Fig. 5.27). Since the AlGaN/SiC heterojunction investigated in this study includes AlN/GaN superlattice structure, we assume that the 2/3 ML or 1 ML Si pre-irradiation contributed to more accumulation of Si near interface, resulting in the enhanced emitter injection efficiency. A summary of the current gain of the HBTs is shown in Fig. 5.28. Although significant improvement of current gain was not achieved, our initial results on atomic control of AlGaN/SiC heterojunction suggest the possibility of further improvement of current gain by optimizing deposition condition.

5.7 Operation of AlN/SiC HBTs

We also note that AlN/SiC HBTs are successfully fabricated and characterized. The use of AlN instead of AlGaN provides smaller lattice mismatch with SiC and larger conduction and valance band offset. Therefore higher current gain is expected due to the reduced defect

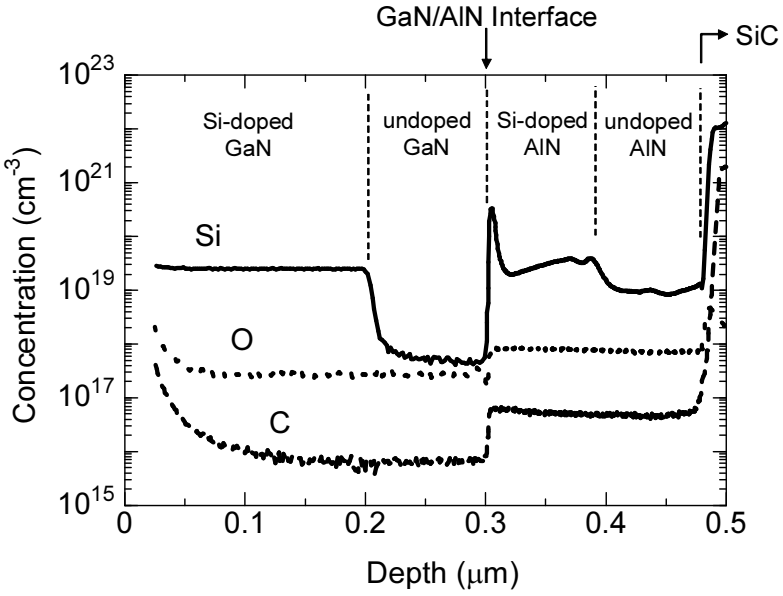


Figure 5.27: SIMS depth profile of Si in GaN/AlN stack structure grown under metal-rich condition (Si pre-irradiation was not used). Incorpolation of large amount of Si in undoped-AlN and accumulation of Si at the GaN/AlN interface were observed.

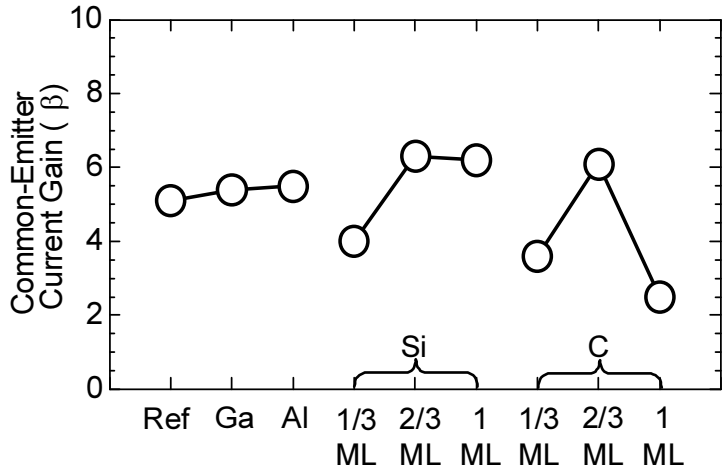


Figure 5.28: A summary of the current gain of the HBTs grown by various pre-irradiation investigated in this study.

density at the interface and stronger confinement of holes.[1]

Fig. 5.29 shows the common-emitter I_C–V_{CE} characteristics of the AlN/SiC HBT grown by 1/3 ML C pre-irradiation. A common-emitter mode operation without leakage was obtained, although large forward voltage drop was observed perhaps due to the low carrier concentration in AlN. A current gain of $\beta \sim 2.4$ was obtained whereas reference AlGaN/SiC HBT grown by 1/3 ML C pre-irradiation showed $\beta \sim 3.6$. Although the higher current gain was not obtained probably due to the high series resistance of AlN emitter, which was indicated in a Gummel plot shown in Fig. 5.29, the operation of AlN/SiC HBT indicates their future possibility, taking account such potential advantage as smaller lattice mismatch with SiC and sufficient valence band offsets.

5.8 Summary

We proposed here AlGaN/SiC HBTs with AlN/GaN short-period superlattice widegap emitter. We have started by investigating the crystal quality of MBE-grown quasi-AlGaN on off-axis SiC. Although quasi-AlGaN layer grown on off-axis SiC showed step bunching due to the large off-angle of the substrates, it showed adequate structural and electronic properties as the emitter of the HBTs revealed by XRD, TEM, CL analysis and Hall effect measurement.

Then we investigated the impact of Al composition on the electronic properties of AlGaN/SiC heterojunction and HBTs. By utilizing Al composition of over 0.5, we successfully demonstrated bandgap engineering in AlGaN/SiC and suppressed the tunneling current via interface traps in AlGaN/SiC heterojunction, resulting in the first common-emitter mode operation ($\beta \sim 2.7$) in the HBTs. The improvement of electron injection efficiency was also indicated by the change of electroluminescence (EL), where yellow EL was observed in $Al_xGa_{1-x}N$/SiC HBTs with $x > 0.5$ and blue EL was observed in HBTs with $x > 0.5$.

Toward further improvement of current gain, we also investigated the effect of n^--SiC spacer between n-AlGaN and p-SiC, and p-SiC base width. By utilizing 200 nm-thick n-SiC spacer and 250 nm-thick p-SiC base layer, we achieved improved current gain of 13 due to the reduced interface and bulk recombination.

Toward high-current-gain AlGaN/SiC HBTs, atomic control of AlGaN/SiC heterointerface is conducted. We conducted C pre-irradiation prior to the AlGaN growth on SiC to

[1] one may think that large conduction band offset gives the potential spike at the interface and reduces the electron injection efficiency. However, our HBTs are designed as "power" transistor where high emitter/base doping ratio of 20 is employed, whereas "high-frequency" AlGaAs/GaAs HBT usually employs high base doping to reduce base resistance and thus low emitter/base doping ratio of < 0.1. Thus, depletion width in the AlN emitter is very small so that such potential spike becomes almost negligible.

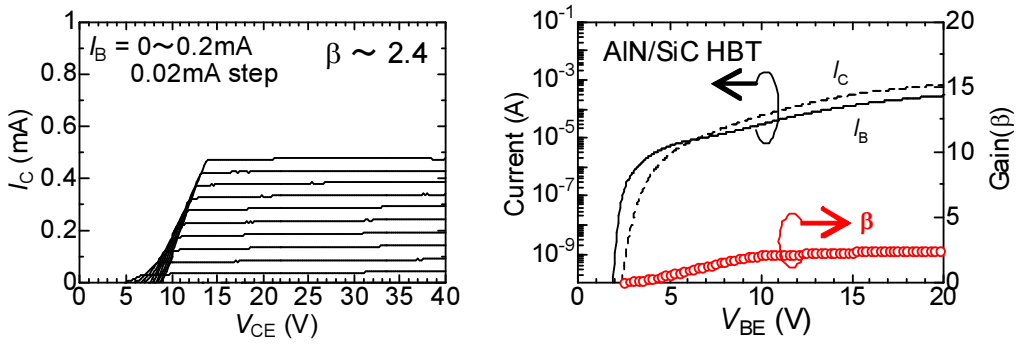


Figure 5.29: Common-emitter I_C-V_{CE} characteristics and a Gummel plot of AlN/SiC HBTs grown by 1/3 ML C pre-irradiation.

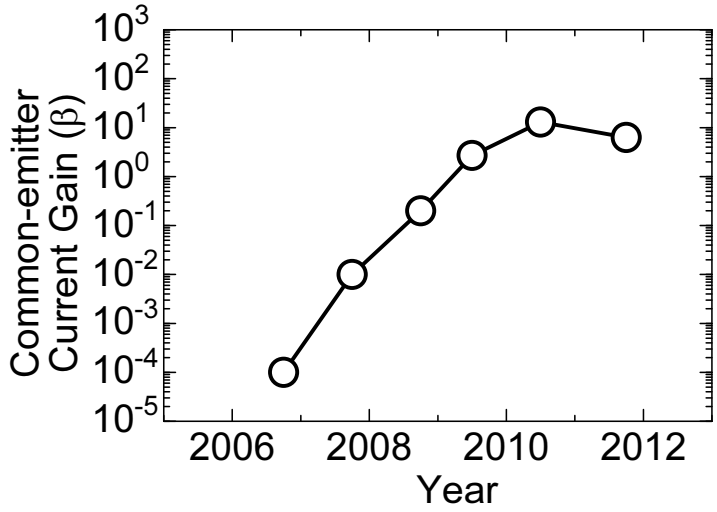


Figure 5.30: Evolution of Ⅲ-N/SiC HBTs investigated in this study. In 2006, a current gain was as low as 0.0001. With the techniques described in this thesis, a maximum current gain of 13 was achieved.

Table 5.6: Evolution of Ⅲ-N/SiC HBTs investigated in this study.

Generation	1st	2nd
Emitter 1	GaN 500 nm 2×10^{19}cm^{-3}	GaN 300 nm 2×10^{19}cm^{-3}
Emitter 2	— —	AlN 1–4.5 nm —
Emitter 3	— —	— —
Base	SiC 500 nm 5×10^{19}cm^{-3}, 1×10^{18}cm^{-3}	SiC 500 nm 1×10^{18}cm^{-3}
Collector	SiC 10 μm 5×10^{15}cm^{-3}	SiC 10 μm 5×10^{15}cm^{-3}
Current Gain	0.0001 – 0.03	0.1 – 0.2
$R_{\text{sp\_on}}$	–	–
V_{CEO}	–	1020 V
Emitter Metal	Ti/Al/Ni	Ti/Al/Ni
Base Metal	Ti/Al/Ni	Pd
RTA Temperature	900°C	600°C
Ion Implantation	None	Yes
Note	Base Doping, Polytype	AlN Spacer, N* Pre-Irradiation

Table 5.7: Evolution of III-N/SiC HBTs investigated in this study.

3rd	4th	5th
GaN 200 nm 2×10^{19}cm^{-3} Quasi-AlGaN 100 nm 1×10^{19}cm^{-3} SiC 50 nm 1×10^{16}cm^{-3}	GaN 200 nm 2×10^{19}cm^{-3} Quasi-AlGaN 100nm 1×10^{19}cm^{-3} SiC 50–200 nm 1×10^{16}cm^{-3}	GaN 200 nm 2×10^{19}cm^{-3} Quasi-AlGaN 100 nm or AlN 80 nm 1×10^{19}cm^{-3} SiC 50 nm 1×10^{16}cm^{-3}
SiC 500 nm 1×10^{18}cm^{-3}	SiC 250–500 nm 1×10^{18}cm^{-3}	SiC 250 nm 1×10^{18}cm^{-3}
SiC 10 μm 5×10^{15}cm^{-3}	SiC 10 μm 5×10^{15}cm^{-3}	SiC 10 μm 5×10^{15}cm^{-3}
0.2 – 2.7	4.2 – 13	5.0 – 6.3
20 – 30 mΩcm^2	–	–
1040 V	–	–
Ti/Al/Ni	Ti/Al/Ni	Ti/Al/Ni
Ti/Al/Ni	Ti/Al/Ni	Ti/Al/Ni
600°C	600°C	600°C
Yes	Yes	Yes
AlN/GaN Superlattice Emitter **First Common-Emitter Operation**	Spacer & Base Width	Si, C Pre-Irradiation, AlN Emitter

replace Si-N bonds (having excess electrons) at the interface with Al-C bonds (having excess holes), which may contribute to compensation of the charge states at the AlGaN/SiC. A maximum current gain obtained in this study was $\beta \sim 6.1$ in the HBTs with 2/3ML C pre-irradiation. We also conducted Si pre-irradiation for comparison. A maximum current gain β of 6.2 – 6.3 was obtained in the HBTs with 2/3 – 1ML Si pre-irradiation due to the Si incorporation. Finally, we also demonstrated the operation of AlN/SiC HBTs with a current gain of $\beta \sim 2.4$.

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Chapter 6

Conclusions

6.1 Conclusions

In this thesis, SiC-based bipolar junction transistors (BJTs) were intensively investigated toward advanced high-power and low-loss switching applications. To realize high performance BJTs, the author concentrated on the improvement of current gain that is one of the critical parameters determining the power loss in bipolar transistors. Design, growth, processing and characterization of SiC BJTs are investigated. Record-breaking current gain ($\beta > 250$) as well as record-high blocking voltage ($V_{\mathrm{CEO}} > 17$ kV) were demonstrated in SiC BJTs. In addition, toward further improvement of current gain, an alternative device structure, Ⅲ-N/SiC HBTs, were proposed as next-generation power switches. To develop high-current-gain HBTs, growth of Ⅲ-N on SiC as well as control of electronic properties of Ⅲ-N/SiC heterojunction were investigated. Fabrication process optimized for Ⅲ-N/SiC HBTs was also established. With these efforts, the author demonstrated the first common-emitter-mode operation ($\beta > 10$) in AlGaN/SiC HBTs. The main conclusions obtained in the present study are summarized as follows.

In Chapter 2, utilization of cold-wall CVD was proposed to achieve relatively thin layer of $0.35-1.2$ μm or very thin layer of $0.05-0.20$ μm required for BJTs and HBTs. Its system configuration, high-temperature HCl gas etching prior to the growth, and growth procedure for SiC epitaxy were discussed. In addition, plasma-assisted molecular-beam epitaxy (MBE) was described to achieve low-temperature Ⅲ-N heteroepitaxy with *in-situ* monitoring. Such features as ultra-high vacuum system, *in-situ* RHEED systems as well as *in-situ* Ga deposition and desorption treatment prior to the growth, and growth procedure for Ⅲ-N epitaxy were presented.

In Chapter 3, development of high-current-gain SiC BJTs was presented. To improve the current gain, the suppression of surface, interface, and bulk recombination as well as proper design of SiC BJTs were intensively investigated. The author proposed the concept of deep-level-reduction process to enhance the lifetime of p-SiC base and thus suppress the bulk recombination. Then 4H-SiC BJTs passivated by deposited oxides with various

post-deposition annealing processes were investigated to suppress the surface recombination. Using deposited oxides annealed in N_2O and NO, and $\{1\bar{1}00\}$ sidewalls, the BJTs demonstrated a high current gain of 73 – 102 due to the reduced surface recombination, whereas BJTs having conventional thermally-grown oxides showed a current gain of 50. Toward further reduction of surface recombination, the effect of n-SiC surface passivation combined with high temperature HCl treatment on the current gain of 4H-SiC BJTs were also investigated. The BJTs with 1.0 – 1.5 kV blocking performance were realized by newly developed 11 μm-deep mesa edge termination technique based on Cl_2-based ICP etching with a deposited SiO_2 mask.

Moreover, the effect of continuous epitaxy on the current gain of SiC BJTs was investigated to reduce the interface recombination. A record current gain of 257 at room temperature and 127 at 250°C were demonstrated in 4H-SiC BJTs on the (0001)Si-face, which is twice as large as the previous record gain. The results suggested that the surface passivation with deposited oxides annealed in NO, usage of $\{1\bar{1}00\}$ sidewalls, and continuous epitaxial growth of the emitter-base junction, combined with deep-level-reduction process based on thermal oxidation dramatically improved the current gain. Toward further reduction of the surface recombination on the p-SiC base, the SiC $(000\bar{1})$C-face was utilized. The author demonstrated C-face BJTs showing the highest current gain of 439 among the SiC BJTs ever reported.

Finally, ultrahigh-voltage 4H-SiC BJTs with novel edge termination techniques referred to as space-modulated junction termination extension (SM-JTE) featuring two-zone-JTE and guard rings are reported. ON-state characteristics showed a current gain of 60 and $R_{\mathrm{sp\_on}}$ of 242 mΩcm^2 assuming current spreading, which is below the SiC unipolar limit. The author achieved an open-base blocking voltage of > 17 kV (measurement-system limit), which is the highest blocking voltage among any semiconductor switching devices.

In Chapter 4, growth, electrical characterization, and electroluminescence (EL) of GaN/SiC HBTs fabricated on SiC off-axis substrates were presented. The GaN layers grown on off-axis SiC showed step bunching due to the large off-angle of the substrates. It contributed to the annihilation of edge dislocations as revealed by XRD and TEM analysis. Hall-effect measurement showed the GaN layer has adequate electron mobility as well as carrier concentration, suggesting that the GaN on off-axis SiC substrate is applicable for the emitter of GaN/SiC HBTs.

Subsequently, the impact of base doping concentration and polytype of SiC (4H and 6H) on electronic properties of the GaN/SiC heterojunction and HBTs were investigated. By utilizing reduced doping of 1×10^{18} cm^{-3} instead of 1×10^{19} cm^{-3}, tunneling current via interface traps was suppressed, resulting in significantly improved rectifying behavior in both the GaN/4H-SiC and GaN/6H-SiC heterojunction diodes. C-V characteristics revealed that the band lineup of GaN/SiC is type-II with a potential barrier of 0.76 eV for GaN/4H-SiC and 0.65 eV for GaN/6H-SiC, suggesting that GaN/6H-SiC is better for electron injection. The electron injection form the emitter to the base was confirmed by EL. In accordance

with diode characteristics, GaN/SiC HBTs showed an improved current gain by employing reduced base doping concentration and by utilizing 6H-SiC. A maximum common-base current gain of 0.01 and 0.03 was obtained on GaN/4H-SiC HBTs and GaN/6H-SiC HBTs, respectively, with base doping of $1\times10^{18}\mathrm{cm}^{-3}$.

Next, GaN/SiC HBTs with ultrathin ($1-4.5$ nm) AlN spacer layers at the n-GaN/p-SiC emitter junction were proposed in attempt to improve the electronic properties of GaN/SiC heterojunction. The insertion of AlN spacer is found to be promising in terms of electron injection efficiency due to the reduced potential barrier (0.54 eV) to electron injection and smaller recombination via interface traps. N* pre-irradiation prior to AlN growth was also investigated to control the electronic properties of GaN/AlN/SiC heterojunction. It was found that the potential barrier was further reduced to 0.46 eV by N* pre-irradiation. The HBT structure was fabricated with newly developed process featuring ion implantation and Pd ohmic contact to obtain low resistivity to the p-SiC base at as low as 600°C. With these efforts, a maximum common-base current gain of 0.1 was achieved in the GaN/AlN/SiC HBT with 1 nm-thick AlN layer without N* pre-irradiation and 0.2 in 2 nm-thick AlN layer with N* pre-irradiation.

In Chapter 5, the author proposed AlGaN/SiC HBTs with an AlN/GaN short-period superlattice widegap emitter to obtain better electronic properties in Ⅲ-N/SiC heterojunction. Although quasi-AlGaN layers grown on off-axis SiC showed step bunching due to the large off-angle of the substrates, it showed adequate structural and electronic properties as the emitter of the HBTs as revealed by XRD, TEM analysis and Hall effect measurement.

Then, the impact of Al composition on the electronic properties of AlGaN/SiC heterojunction and HBTs was investigated. By utilizing Al composition of over 0.5, the band offset control and suppression of tunneling current via interface traps in AlGaN/SiC heterojunction were realized, resulting in the first common-emitter mode operation ($\beta \sim 2.7$) in the HBTs. The improved electron injection efficiency was also indicated by EL. Toward further improvement of current gain, the effects of n^--SiC spacer between n-AlGaN and p-SiC, and p-SiC base width were also investigated. By utilizing 200 nm-thick n-SiC spacer and 250 nm-thick p-SiC base layer, a maximum current gain of 13 was achieved due to the reduced interface and bulk recombination.

Finally, trials of atomic control of AlGaN/SiC heterointerface was conducted toward high-current-gain AlGaN/SiC HBTs. The results suggested that the interface states can be controlled by Si and C pre-irradiation prior to the AlGaN growth.

6.2 Future Outlook

Through this study, approaches for high-current-gain SiC BJTs and AlGaN/SiC HBTs were established. However, there are still remaining issues to be solved to improve the performance of SiC BJTs.

- **Improvement of Current Gain in SiC BJTs:**

  In this work, high current gain was demonstrated in SiC BJTs. However, at low collector current, the current gain was lower than the peak gain, and collector current range which gave high current gain was limited. This indicates that the recombination currents derived from surface, interface, and bulk recombination are still present. Thus, further suppression of these recombination currents is necessary to provide higher current gain in a wide range of collector current. From the insights obtained through this work, optimization of surface passivation by low-doped n-SiC or utilization of C-face may be one of the solutions to reduce the surface recombination. For the bulk recombination, utilization of thinner base or modified deep-level-reduction process may be promising. Regarding the interface recombination, development of AlGaN/SiC HBT is a possible solution. Issues on the AlGaN/SiC HBT are addressed below.

- **Improvement of Current Gain in AlGaN/SiC BJTs:**

  One of the bottlenecks limiting the current gain in AlGaN/SiC HBTs is interface recombination, so that further control of electronic properties of AlGaN/SiC interface is necessary. Possible components of the interface recombination includes (1) defects formed by lattice mismatch, (2) polytype mismatch, and (3) chemical valence mismatch. On non-polar faces such as $(1\bar{1}00)$ and $(11\bar{2}0)$, it is known that isopolytype 4H-AlN is coherently grown on 4H-SiC [1]. In addition, it is expected that there are no charge states at non-polar AlN/SiC since there is the same number of Si and C on the SiC surface, contributing to the formation of the same number of Si-N and Al-C bonds. Thus, lattice-matched, isopolytype, non-polar 4H-AlN/4H-SiC interface, where there is no defects caused by lattice and polytype mismatch, and no charge accumulation caused by chemical valence mismatch, can be achieved. With integrating the technologies developed for SiC BJTs, i.e. surface passivation technique and deep-level-reduction process proposed in this study, a much higher current gain beyond SiC BJTs is expected in the AlGaN/SiC HBTs.

- **Reduction of ON-Resistance by Conductivity Modulation:**

  Conductivity modulation is promising to reduce the ON-resistance below the SiC unipolar limit. In 17 kV BJTs investigated in this study, the presence of conductivity modulation was confirmed. This may be attributed to the relatively high base doping and low collector doping. However, the origin is still unclear, so that further study to maximize the effect of conductivity modulation should be conducted.

Finally, the author sincerely hopes the production of high-current-gain SiC BJTs based on the technology developed in this study, which contribute to the ultra-low loss power switching and thus, high energy efficiency in the world.

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List of Publications

A. Full Length Papers and Letters

BJT

1. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Improvement of Current Gain in 4H-SiC BJTs by Surface Passivation With Deposited Oxides Nitrided in N_2O or NO,"
IEEE Electron Device Lett., **32**, 285 (2011).

2. **(IEEE Kansai Section Student Paper Award)**
Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"4H-SiC BJTs with Record Current Gains of 257 on (0001) and 335 on $(000\bar{1})$,"
IEEE Electron Device Lett., **32**, 841 (2011).

3. Hiroki Miyake, Takafumi Okuda, Hiroki Niwa, Tsunenobu Kimoto, and Jun Suda,
"17 kV 4H-SiC BJTs with Space-Modulated Junction Termination Extension,"
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HBT

4. Jun Suda, Hiroki Miyake, Koichi Amari, Yuki Nakano, and Tsunenobu Kimoto,
"Systematic Investigation of c-Axis Tilt in GaN and AlGaN Grown on Vicinal SiC(0001) Substrates,"
Jpn. J. Appl. Phys., **48**, 020202 (2009).

5. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Demonstration of Common-Emitter Operation in AlGaN/SiC Heterojunction Bipolar Transistors,"
IEEE Electron Device Lett., **31**, 942 (2010).

6. Takafumi Okuda, Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Current Transport Properties of Quasi-$Al_xGa_{1-x}N$/SiC Heterojunction Bipolar Transistors with Various Band Discontinuities,"
Jpn. J. Appl. Phys., in press

7. Hiroki Miyake, Koichi Amari, Tsunenobu Kimoto, and Jun Suda,
"Growth, Electrical Characterization, and Electroluminescence of GaN/SiC Heterojunction Bipolar Transistors Fabricated on SiC Off-Axis Substrates,"
to be submitted to J. Appl. Phys.

8. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Effect of Ultrathin AlN Spacer on Electronic Properties of GaN/SiC Heterojunction Bipolar Transistors,"
to be submitted to IEEE Trans. Electron Devices.

9. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"SiC Heterojunction Bipolar Transistors featuring AlN/GaN Short-Period Superlattice Emitter,"
to be submitted to IEEE Trans. Electron Devices.

10. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Investigation of Various Pre-Irradiation on Growth and Performance of AlGaN/SiC Heterojunction Bipolar Transistors,"
to be submitted to Jpn. J. Appl. Phys.

B. Conference Proceedings

1. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Improved Current Gain in GaN/SiC Heterojunction Bipolar Transistors by Insertion of Ultra-thin AlN Layer at Emitter-junction,"
Mater. Sci. Forum, **615-617**, 979 (2009).

2. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"SiC Heterojunction Bipolar Transistors with AlN/GaN Short-Period Superlattice Widegap Emitter,"
Mater. Sci. Forum **645-648**, 1029 (2010).

3. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Improved Current Gain in 4H-SiC BJTs Passivated with Deposited Oxides Followed by Nitridation,"
Mater. Sci. Forum, **679-680**, 698 (2011).

4. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"4H-SiC Bipolar Junction Transistors with Record Current Gains of 257 on (0001) and 335 on (000-1),"
Proceedings of the 23rd IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD), p. 292 (2011).

5. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Enhanced Current Gain (> 250) in 4H-SiC Bipolar Junction Transistors by A Deep-Level-Reduction Process,"
to be published in Mater. Sci. Forum (2012).

C. Papers Presented at International Conferences

1. Hiroki Miyake, Koichi Amari, Tsunenobu Kimoto and Jun Suda,
" Impact of Base Doping Concentration on Characteristics of n-GaN/p-SiC/n-SiC Heterojunction Bipolar Transistors, "
9th International Conference on Atomically Controlled Surfaces, Interfaces and Nanostructures (ACSIN-9), Tokyo, Japan, Nov. 2007.

2. Hiroki Miyake, Tsunenobu Kimoto and Jun Suda,
"Improved Current Gain in GaN/SiC Heterojunction Bipolar Transistors by Insertion of Ultra-thin AlN Layer at Emitter-junction, "
7th European Conference on Silicon Carbide and Related Materials (ECSCRM), Barcelona, Spain, Sept. 2008.

3. **(Student Paper Award)** Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
" Demonstration of Common-Emitter Mode Operation in AlGaN/SiC Heterojunction Bipolar Transistors, "
2009 IEEE International Meeting for Future of Electron Devices Kansai (IMFEDK), Osaka, Japan, May 2009.

4. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
" Demonstration of SiC Heterojunction Bipolar Transistors with AlN/GaN Short-Period Superlattice Widegap Emitter, "
67th IEEE Device Research Conference (DRC), University Park, Pennsylvania, USA, June 2009.

5. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
" SiC Heterojunction Bipolar Transistors with AlN/GaN Short-Period Superlattice Widegap Emitter, "
13th International Conference on Silicon Carbide and Related Materials (ICSCRM), Nürnberg, Germany, Oct. 2009.

6. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Improved Current Gain in 4H-SiC BJTs Passivated with Deposited Oxides Followed by Nitridation, "
8th European Conference on Silicon Carbide and Related Materials (ECSCRM), Oslo, Norway, Aug. 2010.

7. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Ⅲ-N/SiC Heterojunction Bipolar Transistors with the AlN/GaN Superlattice Emitter Grown by Plasma-Assisted Molecular Beam Epitaxy,"
2010 International Workshop on Nitride Semiconductors (IWN), Tampa, Florida, USA, Sept. 2010.

8. Hiroki Miyake,
"Can we realize high-current-gain transistors using Ⅲ-N/SiC heterovalent heterojunctions ?"
3rd HOPE Meeting, Tokyo, Japan, Mar. 2011.

9. **(Charitat Award)** Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"4H-SiC Bipolar Junction Transistors with Record Current Gains of 257 on (0001) and 335 on (000-1),"
23rd IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD), San Diego, California, USA, May 2011.

10. **(Invited)** Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Enhanced Current Gain (>250) in 4H-SiC Bipolar Junction Transistors by A Deep-Level-Reduction Process,"
2011 International Conference on Silicon Carbide and Related Materials (ICSCRM), Cleveland, Ohio, USA, Sept. 2011.

11. Takafumi Okuda, Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Current Transport Characteristics of Quasi-$Al_xGa_{1-x}N$/SiC Heterojunction Bipolar Transistors with Various Band Discontinuities,"
2011 International Conference on Solid State Devices and Materials (SSDM), Aichi Industry & Labor Center, Nagoya, Japan, Sept. 2011.

12. **(Keynote Lecture)** Jun Suda, Hiroki Miyake, and Tsunenobu Kimoto,
"Improvement of Current Gain in 4H-SiC Bipolar Junction Transistors,"
2011 International Symposium on Materials Science and Innovation for Sustainable Society (ECO-MATES), Osaka, Japan, Nov. 2011.

D. Papers Presented at Domestic Conferences (Selected)

1. **(JSAP Paper Award)** Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda,
"Demonstration of Common-Emitter Mode Operation in AlGaN/SiC Heterojunction Bipolar Transistors",
26th Japan Society of Applied Physics (JSAP) Spring Meeting, Tsukuba Univ., Japan, Mar. 2009.

2. **(JSAP Paper Award Presentation)** Hiroki Miyake, Tsunenobu Kimoto, Jun Suda, “SiC Heterojunction Bipolar Transistors with AlN/GaN Short-Period Superlattice Widegap Emitter”,
70th Japan Society of Applied Physics (JSAP) Fall Meeting, Toyama Univ., Japan, Sept. 2009.

3. **(EMS Award)** Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda, “High Temperature Characterization and Electroluminescence of Quasi-AlGaN/SiC Heterojunction Bipolar Transistors”,
29th Electronic Materials Symposium (EMS), Laforet Shuzenji, Shizuoka, Japan, July 2010.

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71th Japan Society of Applied Physics (JSAP) Fall Meeting, Nagasaki Univ., Japan, Sept. 2010.

5. Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda, “4H-SiC BJTs with Record Current Gain by a Deep-Level-Reduction Process”,
72th Japan Society of Applied Physics (JSAP) Fall Meeting, Yamagata Univ., Japan, Aug. 2011.

6. **(Invited)** Hiroki Miyake, Tsunenobu Kimoto, and Jun Suda, “Development of High-Current-Gain SiC Bipolar Junction Transistors”,
20th Meeting on SiC and Related Wide Bandgap Semiconductors, Winc Aichi, Japan, Dec. 2011

E. Related Articles

1. Jun Suda, Hiroki Miyake, and Tsunenobu Kimoto,
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Hyomen Kagaku, **31**, 651 (2010) (in Japanese).