STUDIES ON BIPOLAR RANDOM ACCESS MEMORY INTEGRATED CIRCUITS

by
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November 1982

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CHAPTER I

INTRODUCTION

Since integrated circuit (IC) memories started to expel ferrite cores from computers in late 1960s, they have been continuing to develop in speed and capacity, contributing greatly to the progress of computers' hardware performance. In view of functions, IC memories are divided into two major types: random access memories (RAMs) and read only memories (ROMs). A RAM allows to be written information into, to store it, and to be read it from. On the contrary, a ROM can only be read it from as the nomenclature designates. The word "random" means that a RAM has about equal access times no matter in what address the accessed information is stored, unlike sequentially addressed memories such as shift registers. RAMs have wider applications than ROMs, and are used in various kinds of computers in large volumes.

The other classification of IC memories is based on device types: bipolar or metal-oxide-semiconductor (MOS). Both types of memories are used in different applications according to their features. MOS memories are characterized by large bits per chip (which means low cost per bit) and slow or medium speed. On the other hand, bipolar ones boast of their high-speed, but their integration level is comparatively small (higher cost per bit than MOS memories'). One of good examples showing proper use of both RAMs can be found in a general purpose mainframe computer of today. It usually uses MOS RAMs as main storage whose main requirements are large capacity and low cost per bit, and bipolar ones as buffer or cache storage which requires high-speed but small volume (see Chap. IV). This hierarchical organization of different memory devices gives the best

cost/performance to the system. To sum up, MOS RAMs provide the system with capacity and bipolar with speed.

This thesis will study circuit and device innovations in bipolar RAM ICs. The background for this research will be described in Chapter II, which will give a historical overview of bipolar RAM ICs, at first. Then, requirements of memory cell circuits, which are the most important circuit among RAM circuitries, will be discussed. At last, a novel high-performance memory cell with alterable load impedance between at standby and at selection will be proposed and discussed. Appendix I will describe the configuration and function of a typical bipolar RAM.

Chapter III will describe the development of a high-speed low-power 4096 X 1-bit bipolar RAM. One of the problems encountered in increasing integrated bit count on a chip from 1024 to 4096 without increasing the total power dissipation and the access time is to choose or devise a cell circuit fitted for low-power operation, high-speed, and small silicon area. A novel cell circuit which satisfies the above requirements at the same time will be proposed. High-speed and low-power are also the requirements for the peripheral circuits which perform buffering, decoding, driving, sensing, etc. Several circuit techniques satisfying the above conditions have been chosen and applied together with the proposed cell to develop the 4K-bit RAM with a typical address access time of 25 ns and power dissipation of 350 mW.

At first, the proposed cell's function and device structure will be analyzed, followed by the description of the peripheral circuitries. Then, the process and device technologies will briefly be described. At last, the performance will be given.

In Chapter IV, a pair of bipolar RAMs developed for use in a mainframe computer will be described. A typical mainframe computer with buffer storage and virtual memory system requires several kinds of ultra-high speed RAMs. The pair has been designed so as to cover the main roles of the above RAMs. Required

performance is so high that a new approach of integrating both RAMs and logics on the same chip has been adopted. A 3072-bit RAM with its peripheral circuits and 470 logic gates have been integrated on the same chip, which is one of the pair. The other chip of the pair is a 1024-bit RAM with a typical access time of as fast as 5.5 ns, which is the fastest access time ever reported for a 1K-bit RAM (at least until 1980).

At first, design considerations leading to the new approach will be presented, followed by description of configuration, functions, and major electrical characteristics of the new chip consisting of the RAM and the logic gates. Then, circuit design of the 1K-bit RAM will be given. Taking the RAM as an example, circuit design method of a RAM IC will be discussed.

Accurate and precise measurement of such a fast access time as 5.5 ns is quite difficult, because a conventional memory tester has access time measurement accuracy of about $\pm(1\text{-}2)$ ns. An adapter circuit board interfacing signals between a memory tester and a RAM to be measured had to be devised to perform the accurate and precise measurement of the access time of the 1K-bit RAM. The method and results will also be presented in this chapter.

Both go/no-go production testing and characterization/failure analysis of ultra high-speed RAMs require a high-performance memory tester and techniques to utilize it. Testing requirements and methods of high-speed bipolar RAMs with an access time of under 10 ns will be discussed in Chapter V.

Overall conclusions and suggestions for further study will be presented in Chapter VI.

CHAPTER II

HIGH SPEED AND LOW POWER MEMORY CELL CIRCUITS

1. Introduction

The most important circuit among various kinds of circuits used for a RAM is a memory cell. Because its number is the largest and its array occupies the most of the RAM silicon area, its performance greatly affects the overall RAM performance. Therefore, many efforts have been made to devise a high speed and low power memory cell since the beginning of the bipolar RAM history. This chapter will study a high-performance memory cell circuit. At first, a quick historical overview on bipolar RAM ICs will be made. How have they been developed? What parts have they been playing in today's mainframe computers? Then, memory cell circuit requirements will be discussed. This requirements analysis has lead to the proposition of a novel high-performance cell named a switched collector impedance cell which will be discussed in the last section.

2. Historical Overview on Bipolar RAM ICs

Ever since International Business Machines Corp. (IBM) introduced IC memories to the System/360 model 85 in 1968[1,2] and to the System/370 model 145 in 1971[3,4,5], many computers, especially mainframe computers, started to adopt them, instead of core memories which had been the primary storage elements in computers for a long time. This tendency has accelerated the development of IC memories with high-performance and large capacity. As a result, every mainframe computer of today is equipped with

them, and boasts of its high-performance owing to their contribution.

Advantages of IC memories over core storage are their high-speed and compatibility with logic elements which are usually ICs. On the other hand, their disadvantages consisted in their relatively high cost per bit and volatality of the stored information. But, outstanding progress of IC technologies has decreased cost of IC memories year by year, which is now well below that of core memories. The problem of volatality is solved by sheltering the stored information into a disc memory when the external power supply is interrupted.

The IC memory used in the System/360 model 85 in 1968 was a bipolar 64-bit memory cell array chip. Afterwards, IBM endeavored to increase the integration level, resulting in a 128-bit chip including peripheral circuits in 1971 [5], and a 1024-bit chip in 1973 [6,7].

Although all the above three memories introduced by IBM were bipolar, the progress of MOS technology has made MOS memory ICs in wide use, especially for low cost and large volume applications. Today, bipolar memories are used where high-performance is necessary, and MOS memories where large storage capacity is needed. One good example is a nowadays general-purpose mainframe computer which uses bipolar memories for its buffer and control storage, and MOS memories for its main storage.

Because of strong demand for more bits on a chip, it has always been a memory IC whose integration level is the largest among various types of ICs of the time. Therefore, to realize a faster and larger memory IC, the most advanced technologies have been applied to it, and many innovative circuit, device, and process technologies have been invented.

One of such technologies is oxide isolation, which is able to cause 40% saving in device area by substituting silicon dioxide for isolating regions of silicon. This approach allows a

transistor base to contact directly with the isolating silicon dioxide, eliminatig space between isolation and the base necessary to support breakdown voltages[8,9,10,11]. Advent of oxide isolation gave impetus to development of larger-integrated memory.

In 1972, Fairchild Camera & Instrument Corp. developed the first bipolar 1024-bit RAM by applying oxide isolation. Their commercial name for oxide isolation process is " Isoplanar " [11]. From 1972 to 1973, different types of insulator isolation processes were developed. Some of them were Motorola Corp.'s Vee-Isolation with Polysilicon backfill (VIP)[12], Raytheon Semiconductor Corp.'s Vertical Anisotropic Etch (V-ATE)[13], and Harris-Intertype Corp.'s Polyplanar[14].

In 1976, the first 4K-bit bipolar RAM was announced[15]. However, it was not a static RAM, but a dynamic one with a novel cell circuit, challenging "the common sense" that low impedance of bipolar devices restricts a bipolar RAM to a static type. This dynamic RAM was increased in degree of integration to 16K-bit RAM in 1978[16].

The first 4K-bit static bipolar memory was developed in 1977, whose access time and power dissipation were 35 ns typ. and 930 mW typ., respectively[17]. The RAM adopted the "walled emitter " oxide isolation process to obtain small memory cell size. "Walled emitter" means that a transistor's emitter contacts directly with the isolating oxide, eliminating the spacing between the emitter and base areas.

The performance of a 4K-bit static bipolar RAM was improved in 1978, when a 4K-bit RAM with a typical access time of 25 ns and a typical power dissipation of 350 mW was presented[18,19]. Details of the RAM will be described in Chapter III. In the same year, another 4K-bit RAM with a typical access time of 35 ns and a typical power dissipation of 500 mW was announced. It adopted characteristic bipolar process which did not need epitaxial growth[20].

In 1979, three new bipolar 4K-bit RAMs were announced. One was an ECL compatible 1024 words by 4-bit RAM with a typical access time of 15 ns[21]. The second was also an ECL 4K-bit RAM with ultra high-performance, whose typical access time was 6 ns[22]. It adopted very advanced processes such as selective growth of epitaxial layer on a transistor emitter and lift-off metallization in addition to a sophisticated cell circuit. The last was an ECL compatible RAM with a cell circuit of IIL type[23]. Its typical access time and power dissipation were 20 ns and 300 mW, respectively.

High-performance of bipolar devices is best demonstrated in comparatively small-integrated RAMs. One of the good examples is an ECL compatible 1024-bit RAM. Its typical access time was 45 ns when it was first introduced in 1972[11]. Four years later, a 1K- bit RAM with a typical access time of 15 ns was presented[24], followed by a RAM with an access time of 7.5 ns typ. in 1977[25], and by a RAM with 5.5 ns typ. in 1979[26,27].

Pursuit of high speed in bipolar memories brought forth a new type of memories in which both logics and memories were integrated. It was usual that a RAM included a cell array and the necessary peripheral circuits interfacing input and output signals for the cell array. The new memories, however, include not only the peripheral circuits for the cell array, but also additional logics to realize higher performance by eliminating off-chip propagation delay between the memory and the logics. Two such examples were presented in 1979[26,27,28]. This new approach shows one of the ways which bipolar memories should follow in future.

Most recent advancements in bipolar memories were announced in 1980. They were a 64K-bit dynamic bipolar RAM[29] and a 16K-bit IIL memory[30]. Because both of them are experimental ones, correct evaluation will be done in future.

The historical overview is summarized in Table 2.1. The access time and cell size evolutios are shown in Fig. 2.1 and Fig. 2.2,

TABLE 2.1

Development of Bipolar Static RAMs

Year	Source	Bits per chip	Access time (ns)	Power per chip (mW)	Chip size (mm^2)	Cell size (mm^2)
'69	1,2	64	[a]7	112	8.1	-
'70	36	64	-	-	1.94	19,400
'70	31,32	256	70	500	11.4	-
'71	37,38	288	[a]4	-	-	16,500
'71	3,4,5	128	40	150	8.89	23,900
'72	11	1024	45(ECL)	500	12.6	6,450
'72	13	1024	35(ECL)	400	7.34	2,774
'74	b	1024	50(TTL)	500	15.1	6,450
'74	54	1024	25(TTL)	500	8.37	3,880
'76	24	1024	15(ECL)	400	10	4,200
'77	c	1024	22(TTL)	400	6.74	3,030
'77	25	1024	7.5(ECL)	832	8.68	2,756
'77	17	4096	35(TTL)	925	15.3	1,935
'78	18,19	4096	25(TTL)	350	21.4	2,480
'78	20	4096	35(TTL)	500	17.2	2,280
'79	26,27	1024	5.5(ECL)	800	7.6	2,896
'79	21	4096	15(ECL)	900	18.3	2,500
'79	22	4096	6(ECL)	650	-	1,640

a: Without peripheral circuits.

b: F. Tsang, "A 1024-bit bipolar RAM," ISSCC Dig. Tech. Papers, Feb. 1974, pp. 200-201.

c: M. N. Phan et al., "A fast 1024-bit bipolar RAM using JFET load devices," ISSCC Dig. Tech. Papers, Feb. 1977, pp. 70-71.

ECL: Emitter coupled logic. TTL: Transistor transistor logic.

TABLE 2.1 - Continued

Metal layers		Cell type	Notable device technologies
Min. width (μm)	Min. spacing (μm)		
-	-	-	
7.6	-	DCC	epitaxial resistors
-	-	MEC	epitaxial resistors
-	-	SCI	washed emitter, double metal layer
-	-	-	
-	-	PDC	oxide isolation (Isoplaner)
-	5	-	oxide isolation(V-ATE), double metal layer
-	-	d	
4	4	MEC	double metal layer by aluminum anodization
-	-	PDC	oxide isolation
-	-	[e]DCC	washed emitter, PtSi Schottky diode
-	-	[f]PDC	self-aligned emitter, oxide isolation
-	-	PDC	walled emitter oxide isolation
6	3	VIC	oxide isolation, double metal layer
-	-	PDC	non-epi., polisilicon self-aligned method
6	3	[f]PDC	oxide isolation, double metal layer
5	5	PDC	walled emitter oxide isolation
-	-	SLR	lift-off metal layer, selective epi. growth

d: A special cell circuit with inverted transistors.
e: With J-FET loads.
f: With Schottky barrier diodes.
DCC: Diode-coupled cell. MEC: Multi-emitter cell. SCI: Switched collector impedance cell. PDC: Parallel diode cell.
VIC: Variable impedance cell. SLR: Switched load resistor cell.

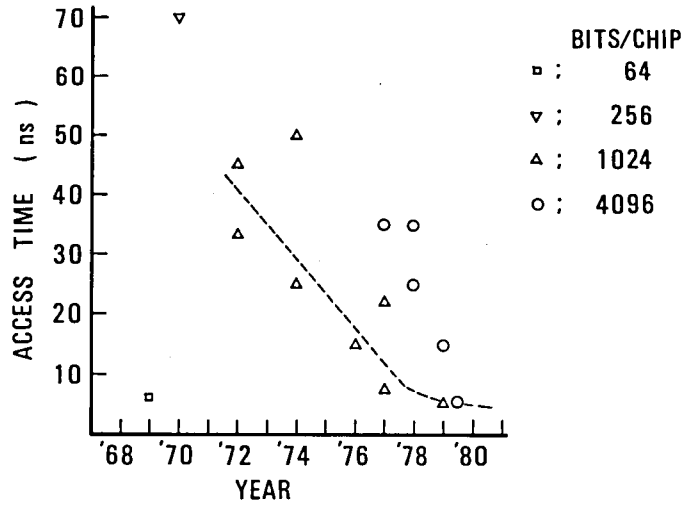


Fig. 2.1. Access time evolution.

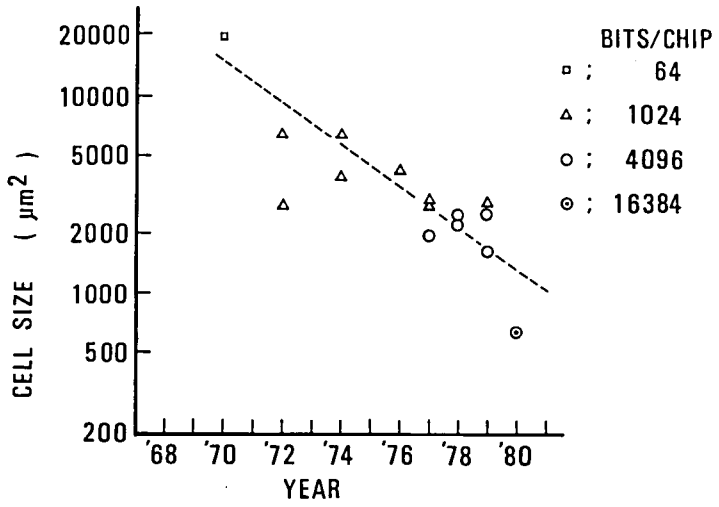


Fig. 2.2. Cell size evolution.

respectively. The access times shown in Fig. 2.1 are typical ones.

3. Memory Cell Circuit Requirements

As explained in Appendix I, circuitries in a RAM are roughly classified into two types: memory cells and the peripheral circuitries. Many types of a memory cell circuit have been proposed and studied because it is the most important circuitry which affects the speed, total power dissipation, and chip area of a RAM.

For example, a 4096-bit RAM described in Chapter III contains 4096 cells, 64 word drivers, 64 sense amplifiers, 12 address buffers, and several control circuits. The cell array occupies 60 % of the active chip area. The active area means the area obtained by subtracting the area for bonding and scribing from the total chip area. As N, the number of bits on a chip, is increased, the cell count increases proportionally to N, but the number of the peripheral circuitries is proportional to $N^{1/2}$. Therefore, the relative importance of a cell circuit increases as the integrated bits on a chip increases.

To be used in an integrated memory, a cell circuit must satisfy a few conditions which are summarized as follows:

(1) First of all, a cell must be a storing circuit which is capable of taking the two distinctive electrically stable (bistable) states corresponding to either "1" or "0" logical state.

(2) It is desirable that a cell can operate at low power dissipation to realize small total power dissipation.

(3) It is desirable that a cell has fast switching characteristics to realize as fast an access time as possible.

(4) To realize as small chip size as possible, a cell must be feasible with small silicon area. For that purpose, a cell had better be consisted of a small number of circuit ele-

ments. What's more, the elements should occupy small area.

(5) The other condition for area reduction is that a cell should allow to be organized into a matrix in which the cells in the same row should share the same word lines, and the cells in the same column should share the same digit lines. Sharing of the lines reduces area for wiring.

Some of the important cell circuits which have been proposed will be reviewed and studied below. The discussion will be restricted mainly to "static" cells. "Static" means that a cell circuit is bistable, and that it can retain its state at standby so long as the current is supplied to it. On the other hand, "dynamic" memory cells store data on a small capacitance. Because of leak current of the capacitance, stored information (charge) disappears as time goes. Therefore, the cell's charge must be reinforced periodically. This reinforcement is called "refreshing".

Although some bipolar dynamic cells were proposed[15,16,29], the common bipolar RAMs in wide use for practical applications are static ones. This is because the high performance, which is expected for bipolar memories, requires static types of cells. Static cells usually have faster switching speed than dynamic ones.

Two memory cell circuits which were often used in the earliest stage in the evolution of bipolar memories are shown in Fig. 2.3. One is a multi-emitter cell[31,32,33,34], and the other is a diode-coupled cell[35,36].

The basic storing element of both cells is two cross-coupled transistors with a collector load, which is shown in Fig. 2.4. Because a positive feed back loop is formed in that circuit, the element functions as a bistable storing circuit satisfying the above condition (1). It is one of the simplest bistable circuits that are feasible with a small number of integrated circuit elements such as transistors, diodes, resistors, and

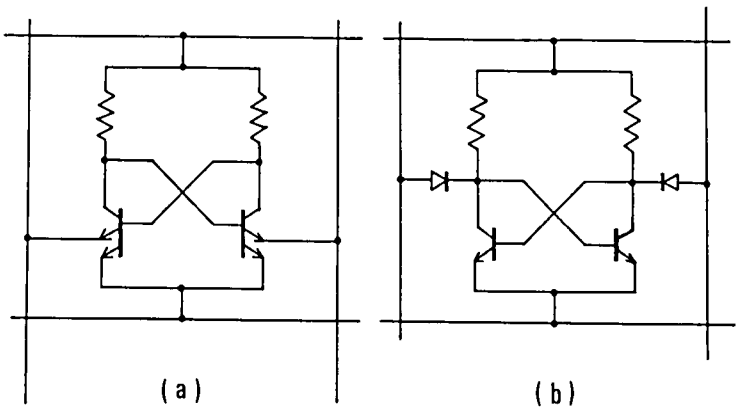


Fig. 2.3. Typical memory cell circuits used in the earliest stage of the bipolar RAM history. (a) Multi-emitter cell. (b) Diode-coupled cell.

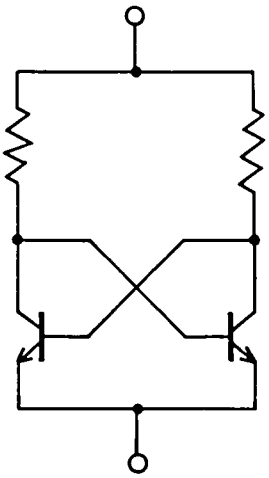


Fig. 2.4. Basic cell circuit.

capacitors. Therefore, it satisfies the condition (4). It also satisfies the condition (2) because its standby current can be designed to be small by choosing a high value collector resistor.

The basic cell must be transformed to allow to be organized into a cell array (the condition (5)). One of the transformations is the multi-emitter cell which is formed by addition of two other transistors to the basic cell. The added transistors are combined with the storing transistors into a pair of multi-emitter transistors. Because two emitters can be fabricated within the same base region (see Chap. III, Fig. 3.5.), a multi-emitter transistor occupies a small area. The emitters of added transistors are connected to a pair of digit lines through which reading and writing of stored information is performed.

A multi-emitter cell in the same row of a cell array share a pair of word lines (upper and lower), and cells in the same column share a pair of digit lines. An individual cell can be accessed by selecting the row and column which include the cell. Selection of a row is performed by raising the potential level of either the upper or lower word line of the row. Selection of a column is performed by lowering the potential levels of digit lines. Raising of word line level and lowering of digit line level makes one of the added transistors of the selected cell active while the added transistors of other cells remain in off-state. Therefore, only the selected cell is capable of either transmitting the stored information to the digit lines or receiving the datum to be written from the digit lines. In this way, the added transistors of the multi-emitter cell work so as to connect/cut-off a cell to/from digit lines. This function of the added transistors enables the cells to be configured into a matrix.

One measure for cell performance is a ratio of the readout current to the standby current: I_R/I_{ST}[36,37,38]. Larger readout current means fast charging and discharging of stray capacitances connected to digit lines (the condition (3)), and smaller standby current means the lower power dissipation of a memory.

If N bits are integrated on a chip, the standby current's contribution to the total power dissipation is N-fold. On the other hand, the read current's contribution is $N^{1/2}$-fold, or less (see Chap. III). The ratio of the multi-emitter cell is small[36,38]. It is estimated from 0.8 to 8 according to the reference (38).

A diode-coupled cell is also derived from the basic cell shown in Fig. 2.4. The cell is coupled with digit lines through two added diodes as the nomenclature signifies. By making both diodes inactive, a cell is deselected. The selected cell sinks the readout current from one of the digit lines through either of the diodes depending on which storing transistor is on.

Because the diode is formed by addition of a contact hole in the collector region of the storing transistor, cell area increase by addition of the diode is kept minimum. A diode-coupled cell can have a high ratio of I_R/I_{ST}[36].

A Switched Collector Impedance (SCI) memory cell introduced in 1971 can have a very high ratio of I_R/I_{ST} (=40-200) because switched collector impedance integrated into a multi-emitter cell can define the standby and readout current values independently [37,38]. A 288-bit SCI memory cell array LSI was fabricated and evaluated[39,40,41,42,43]. Afterwards, a fully decoded 128-bit RAM was developed using SCI memory cells and sophisticated peripheral circuitries such as a pulsed current source, sharing of read current sources, a charge sweeper, and collector-dot type sense amplifiers[44]. A variation of the cell was used to realize a very fast (address access time = 6 ns typ.) prototype 4K-bit RAM in 1979[45].

One of the major drawbacks of bipolar devices is that they need isolation. One of the approaches to reduce cell area is to devise a new cell which does not require isolating region between the neighboring cells. Even if conventional bipolar devices requiring isolation were used in the peripheral circuits of a RAM, elimination of isolation region from the cell array greatly reduces the chip area. Such an example is a super-integrated

memory cell, or an Integrated Injection Logic (IIL) memory cell introduced in 1971[46,47,48]. The cell circuits are shown in Fig. 2.5.

The basic cell shown in Fig. 2.4 is transformed into the new IIL cell by fabricating the n-p-n transistors upside down and by replacing the load resistors with p-n-p transistors in the common n-type epitaxial layer. The cell realizes low power operation as well as reduced area. Therefore, many attemps have been made to fabricate a large capacity memory ranging from 1K to 16K-bit with this type of cells[49,50,23,30].

The cell is famous as the origin of IIL or MTL (Merged Transistor Logic) which can realize digital logic integrated circuits with low-power and high packing density[51,52].

One of the shortcomings of the IIL cell is that it requires a long write pulse width to change its state[49]. One of the causes for small occupying area of the IIL cell is that it can use n^+ buried layer for the lower word line instead of a metallization layer. The series resistance of the n^+ buried layer, however, yields a fairly large amount of voltage drop across the layer. Therefore, care must be taken to afford the drop in designing[23].

The most widely used bipolar cell circuit seems a parallel diode cell shown in Fig. 2.6[11,24,25,27], which is made by addition of diodes across load resistors of the multi-emitter cell. Because the added diodes clamp the collector potential levels of the cell transistors to prevent them to saturate deeply, more readout current can be drawn from the cell than from the multi-emitter cell. A half cell circuit, which consists of a multi-emitter transistor, a resistor, and a diode, can be integrated in the same isolated island. Because the diode can be formed by a parasitic p-n junction between the p-type resistor and the n-type transistor collector (see Fig. 3.5 (a)), the cell area is no larger than that of the multi-emitter cell in spite of addition of the diodes.

A Variable Impedance Cell (VIC) shown in Fig. 2.7 is an

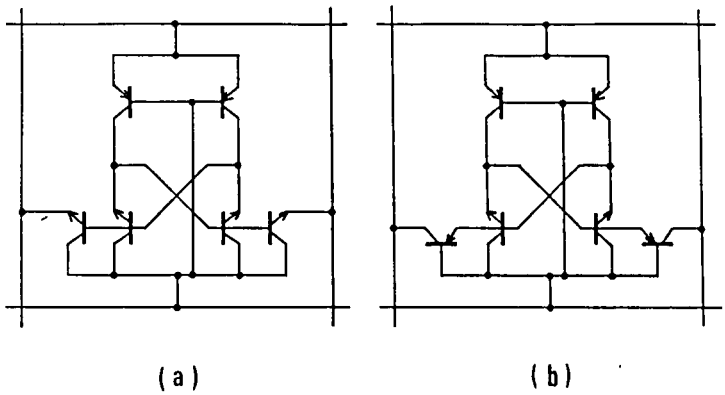


Fig. 2.5. IIL memory cells. (a) n-p-n coupled. (b) p-n-p coupled. See references (46) and (47).

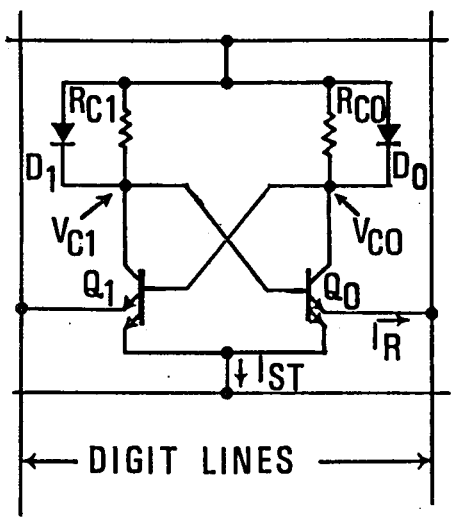


Fig. 2.6. Parallel diode cell.

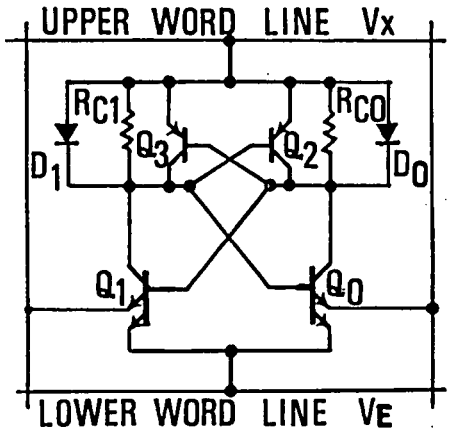


Fig. 2.7. Variable impedance cell.

improved variation of a parallel diode cell for a memory with large capacity[18,19]. The cell will be discussed in more details in Chapter III. The variation of VIC for smaller standby power can be formed by eliminating load resistors[24,53], which is the ultimate form of the VIC when its load resistance are brought to be infinitive for lower standby power operation.

Many efforts have been made to develop a memory LSI with larger capacity and higher speed. Such efforts include not only circuit technology, but also device and process technologies. A short overview on the development of device and process technologies applied for bipolar RAMs will be made below.

Development of bits per chip, access times, chip sizes, and cell sizes as well as the major device technologies is summarized in Table 2.1. Cost reduction is one of the most important and permanent purpose of memory LSIs. It can be realized by integrating more bits on the same silicon area. Therefore, cell size is one of the measures for how the device and process technologies for memories have been advanced. It was reduced from about 20,000 μm^2 in 1970 to about 2,000 μm^2 in 1979 as shown in Table 2.1 and Fig. 2.2.

Device technologies which served much to reduce cell size are concerned with isolation, metallization, fine patterning, shallowing and thinning of devices, and so on. As described earlier, introduction of oxide isolation was a significant step to increase the integration level. A novel approach to eliminate device isolation produced an IIL memory[46,47].

Development of fine pattern technology was another significant contribution of realization of denser memories. Cell area is determined primarily by the area required for metallization lines, the spacings between them, and the area associated with contacts between metallization and silicon. Therefore, finer metallization patterns and smaller contacts produce a smaller cell.

Various other device technologies have been adopted to

minimize cell area. Some of them are two layer metallization[38,54], washed emitters to minimize emitter contact area[38], epitaxial resistors[31], poly-silicon resistors[20], and lift-off metallization[22].

Because smaller devices have smaller capacitances, area reduction of devices serves not only to decrease cell area, but also to achieve high speed. Although the integration level of bipolar memories has been increasing year by year, their access times have been getting faster and faster, owing to the improvement of high-frequency parameters of transistors and other circuit elements. Shallowing and thinning of devices have also contributed to improve the transistor performance.

4. Switched Collector Impedance Memory Cell

A switched collector impedance (SCI) memory cell has been devised to realize a very high ratio of I_R/I_{ST}. Its circuit configuration allows its standby and readout current values to be defined independently.

The SCI cell circuit is shown in Fig. 2.8. It has a multi-emitter transistor (Q_2) and three resistors (R_{RO}, R_{R1} and R_{CC}) additionally compared with the multi-emitter cell in Fig. 2.3 (a). It also has an additional resistor (R_{EE}) which is not necessarily peculiar to the SCI memory cell. The resistor can reduce current hogging effect found among memory cells on the same word line, and may be adopted by other cell circuits including a multi-emitter cell. It was often used in the earlier age of bipolar memory LSIs when IC process technologies were not so fully developed as to limit transistors' current gain (h_{FE}) and base-emitter forward voltage (V_{BE}) variation within a chip to a small value.

At its standby, the transistor Q_2 is made to be in off-state. Therefore, its standby current I_{ST} flows through the

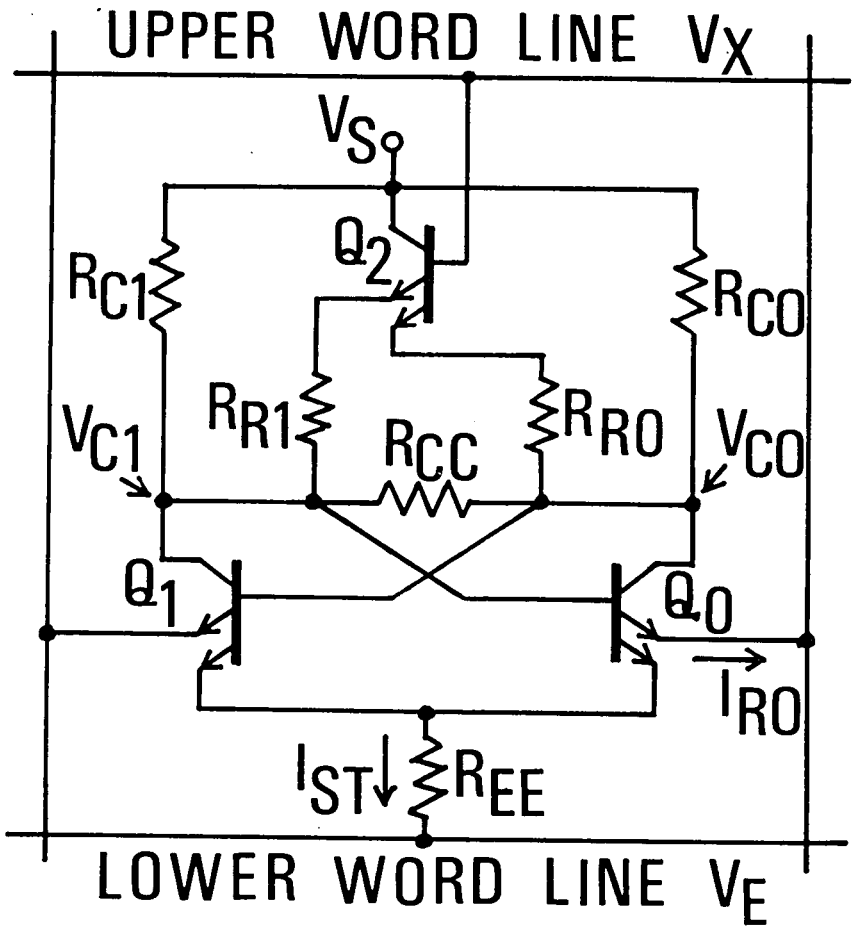


Fig. 2.8. Switched collector impedance cell circuit.

resistors R_{CO}, R_{C1}, R_{CC} and R_{EE}, and the transistors Q_0 or Q_1. When the cell is selected, Q_2 is forced to be in on-state by raising the word line voltage. The readout current I_R is supplied mainly by Q_2, and flows through R_{RO} and R_{R1}, and Q_0 or Q_1. Because the resistance values of R_{RO} and R_{R1} can be designed to be smaller by an order of magnitude than those of R_{CO}, R_{C1} and R_{CC}, the readout current defined by R_{RO} and R_{R1} is made larger than the standby current defined by R_{CO}, R_{C1} and R_{CC}.

The resistor R_{CC} serves to set the cell collector voltages (V_{CO} and V_{C1}) in standby at desired values. Without R_{CC}, the higher cell collector voltage V_{CNH} must be equal to the power supply voltage V_S. But, V_{CNH} has to be lower than V_S which is the transistor Q_2's collector, to prevent Q_2 from saturation at its selected state when the word line voltage V_X, that is, Q_2's base voltage, is raised.

The ratios of readout curret to standby current (I_R/I_{ST}) of SCI and multi-emitter cells are expressed as follows (see Appendix II):

$$\frac{I_R}{I_{ST}} = \frac{V_{CSH}-V_{CSL}}{V_{CNH}-V_{CNL}} * \frac{R_{CO}}{R_{RO}} * \frac{R_{CC}+2R_{RO}}{R_{CC}+2R_{CO}} \qquad \text{(SCI)} \qquad (1.1)$$

$$\frac{I_R}{I_{ST}} = \frac{V_{CSH}-V_{CSL}}{V_{CNH}-V_{CNL}} \qquad \text{(multi-emitter)} \qquad (1.2)$$

where V_{CSH} and V_{CSL} are the upper and lower cell collector voltages at selection, respectively, V_{CNH} and V_{CNL} are the upper and lower cell collector voltages at standby, respectively. In above equations, the cells are assumed to be symmetric, that is, $R_{CO}=R_{C1}$, and $R_{RO}=R_{R1}$.

The voltage difference ($V_{CNH}-V_{CNL}$) must be defined by cell stability at standby. The larger the difference is, the more resistive the cell is against inversion induced by noises.

Therefore, (V_{CNH}-V_{CNL}) cannot be designed to be a extremely small value. It is usually set to be about 100 mV. On the other hand, (V_{CSH}-V_{CSL}) cannot be set to be larger than about 800 mV to prevent the cell transistors (Q_0 and Q_1) from deep saturation which causes slow cell flip-flop inversion during a write cycle. From the above discussion, it is clear that the ratio (V_{CSH} -V_{CSL}) /(V_{CNH}-V_{CNL}) cannot be designed to be larger than 10 at most for both SCI and multi-emitter memory cells. Therefore, the ratio I_R/I_{ST} for a multi-emitter cell is 10 at most. On the other hand, the ratio for the SCI memory cell can be set to any large value because the ratio R_{CO}/R_{RO} can be chosen to be as large as necessary.

The term $(R_{CC}+2R_{RO})/(R_{CC}+2R_{CO})$ is approximated to $R_{CC}/(R_{CC}+2R_{CO})$ because R_{CO} and R_{CC} are usually designed to be larger orders of magnitude than R_{RO}. The values of R_{CC} and R_{CO} cannotbe chosen independently because the cell collector voltages at standby (V_{CNH} and V_{CNL}) are dependent on both values, and because they also cannot be defined independently owing to the design constraints with regard to cell function. The more detailed analysis of cell function (see Appendix II) reveals that the ratio cannot be larger than about 1/9. Even if the ratio, $R_{CC}/(R_{CC}+2R_{CO})$, is chosen to be 1/10, the I_R/I_{ST} ratio for a SCI cell can be made larger tenfold than that for a multi-emitter cell by choosing R_{CO}/R_{RO} to be 100.

Although a SCI cell shows better performance than a multi-emitter cell, it requires more circuit elements and higher value resistors which usually consumes more silicon area than transistors. To make area increase as small as possible, pinched epitaxial layer has been used to implement high value resistors R_{CO}, R_{C1} and R_{CC}. Cell cross-section and layout adopted for the 288-bit SCI memory cell matrix[38] are shown in Figs. 2.9 and 2.10.

P^+ buried layer "pinches" the thickness of the N^- epitaxial layer to realize high sheet-resistivity as shown in Fig. 2.9. Moreover, the epitaxial layer used for R_{CO}, R_{C1} and R_{CC} can

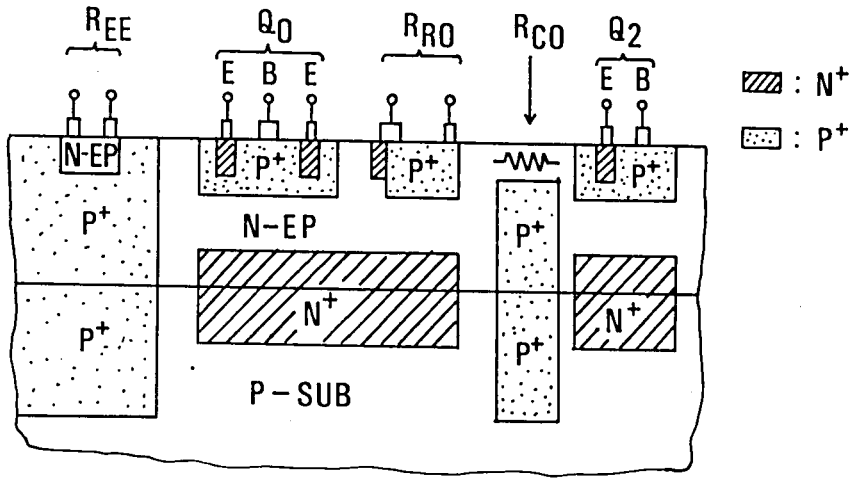


Fig. 2.9. Switched collector impedance cell cross section.

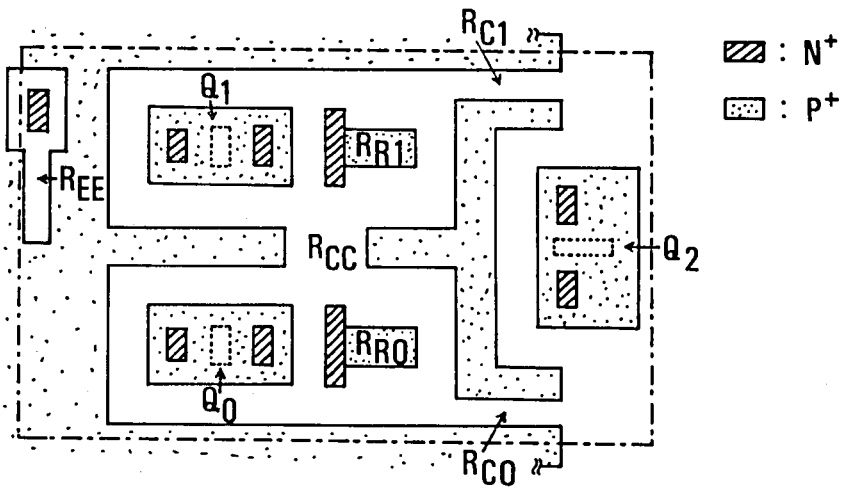


Fig. 2.10. Switched collector impedance cell layout for a 288-bit cell array LSI.

be formed within the same silicon island as the transistors Q_0, Q_1 and Q_2 avoiding adoption of additional isolated islands and contact holes required if metallization wiring is used to connect the resistors and transistors.

With SCI memory cells, a 288-bit cell array LSI to evaluate the cell performance[38] and a 128-bit RAM LSI with full decoding circuitry[44] have been developed. The 128-bit RAM has showed access times ranging from 13 to 19 ns with its stanby and operating power of 0.9 and 3.1 mW/bit, respectively. Its chip and cell sizes are 3.2X3.2 mm^2 and 100X150 μm^2, respectively. In the RAM, a high I_R/I_{ST} ratio of 100 has been achieved by designing the values of I_R and I_{ST} as 2 mA and 20 μA, respectively.

In spite of its high-performance, a SCI cell was not adopted for commercial bipolar RAM LSIs, because a later-introduced parallel diode cell having simpler device structure and a moderate number of I_R/I_{ST} ratio began to be in wide use. The added transistor of a SCI cell made its cell area larger, and the pinched epitaxial layer demanded preciser process control compared to a parallel diode cell, although it had a higher I_R/I_{ST} ratio.

However, a variation of a SCI memory cell was used to realize a very fast (address access time = 6 ns typ.) 4K-bit RAM afterwards in 1979[45]. In its design, ion implantation which was a more controllable process than pinching of epitaxial layer was adopted to implement high value resistance, and a circuit analysis program was fully used to analyze complex function of the cell. Both technologies, ion implantation and circuit analysis program, were not available when a SCI memory cell was first introduced in 1971.

CHAPTER III

A HIGH-SPEED LOW-POWER 4096X1 BIT BIPOLAR RAM

1. Introduction

One of bipolar RAM's strong points is its high speed. The fastest versions of ECL compatible 1024-bit bipolar RAM boast of their fast address access times from around 5.5 ns to 15 ns[24,25,26].

In the field of 4K-bit RAMs, a newly developed NMOS static RAMs challenged bipolar RAMs in high performance[55,56,57]. However, the inherent high speed of bipolar devices combined with optimized circuit techniques still gives bipolar devices an advantage in the field of high-performance RAMs[17,18,19,20,21,22,23]. Such an example is given in this chapter, which describes a 4096-word by 1-bit TTL compatible static RAM with a fast address access time of 25 ns typically while retaining its power dissipation at 350 mW typically.

Increasing memory chip density from 1K bits to 4K bits while retaining the power dissipation and access time at the same values requires circuits which perform high-speed switching with low power dissipation. Four such circuit techniques applied to this new 4K-bit RAM will be presented. In Section 2, a new cell fitted for a largely integrated RAM will be proposed and analyzed. In Section 3 and 4, the other three circuit techniques will be discussed. A brief description of processes and devices will be presented in Section 5, followed by description of the RAM's performance in Section 6.

2. Variable Impedance Cell (VIC)

Design of a memory LSI usually starts from a cell circuit because a cell is the most important circuit which affects the performance. Cell function defines necessary specifications for the peripheral circuits.

The parallel diode cell shown in Fig. 2.6 was investigated as a candidate for the high-speed, low-power 4K-bit RAM. The reasons are as follows:

1) It is able to cause fast switching of digit lines for the reason mentioned in Chapter II, Section 3. That is that it has a high ratio of read current to standby current owing to the clamping diodes.
2) It is coupled to digit lines with its emitters, which allows one to design a sense amplifier of the ECL type. ECL sensing is the fastest means of sensing in bipolar memories.
3) It has already been successfully applied to 256- and 1024-bit RAMs, which have been produced in great quantities for practical applications, by the author and his colleagues. Therefore, much knowledge and know-how about the cell, which are based not only on a small number of experimental devices, but also on mass production and field use, have been accumulated. Consequently, it was easier and reliable approach to develop a 4K-bit RAM by using the same type of a cell as a parallel diode cell. In other words, the cell was applied to the 4K-bit RAM not because it had been proved to be the most appropriate cell to realize a high-speed, low-power 4K-bit RAM, but because it was the design aim to realize a high-performance 4K-bit RAM using the similar type of a cell as the parallel diode cell.

To realize a 4K-bit chip with both high-speed and low power dissipation using parallel diode cells, standby current I_{ST} of the cell should be decreased to about a quarter of that of a 1K-bit chip, requiring its collector resistors R_{C0} and R_{C1} to be

quadrupled correspondingly. The read current I_R should also be increased to about twice that for a 1K-bit chip, because a 4K-bit chip has about twice as much parasitic capacitance connected to the digit lines as a 1K-bit chip. Therefore, voltage drop (R_C*I_R/h_{FE}) across a collector resistor due to base current of a 4K-bit cell is about eight times larger than that of a 1K-bit cell, reducing chip operating range substantially.

This mechanism will be explained using a circuit diagram and equations below. Fig. 3.1 shows a portion of a RAM circuit diagram which adopts parallel diode cells as storing elements. In the figure, transistors Q_0,Q_1; diodes D_0,D_1; and resistors R_{C0},R_{C1} form a parallel diode cell (see Fig. 2.6). Transistors Q_4-Q_8; resistors R_{L0},R_{L1}; and current sources I_{R0}, I_{R1} form a sense amplifier.

Data-readout from a selected cell is performed by current switching between a cell transistor and a sense transistor. Two such current switches exist. One is formed by the transistors Q_0 and Q_4, and the other by Q_1 and Q_5. It is assumed that cell "X" is selected and that its collector voltage V_{C1} shows a higher value ($=V_{CSH}$) than V_{C0} ($=V_{CSL}$). Because node voltages V_{W0} and V_{W1} are set about midway between V_{CSH} and V_{CSL} (the midway value is named $V_{refcell}$), the transistors Q_0 and Q_5 become active , while Q_1 and Q_4 inactive in the above two current switches. Therefore, the read current I_{R0} flows from the cell transistor Q_0, and I_{R1} from the sense transistor Q_5, causing voltage drop across R_{L1} and not across R_{L0}. Thus, Q_6's emitter node SO_0 shows a higher voltage level than Q_7's emitter node SO_1 does. If the cell "X" stores the inverse data (that is, $V_{C1}=V_{CSL} < V_{C0}=V_{CSH}$), SO_0 becomes low, and SO_1 high. Readout is completed by transferring the voltages on SO_0 and SO_1 to an output amplifier.

Selected cell's collector voltages V_{CSH} and V_{CSL} are given by the following equations:

$$V_{CSH} = V_{XH}-R_{C1}*I_{R0}/(h_{FE}+1) \qquad (3.1)$$

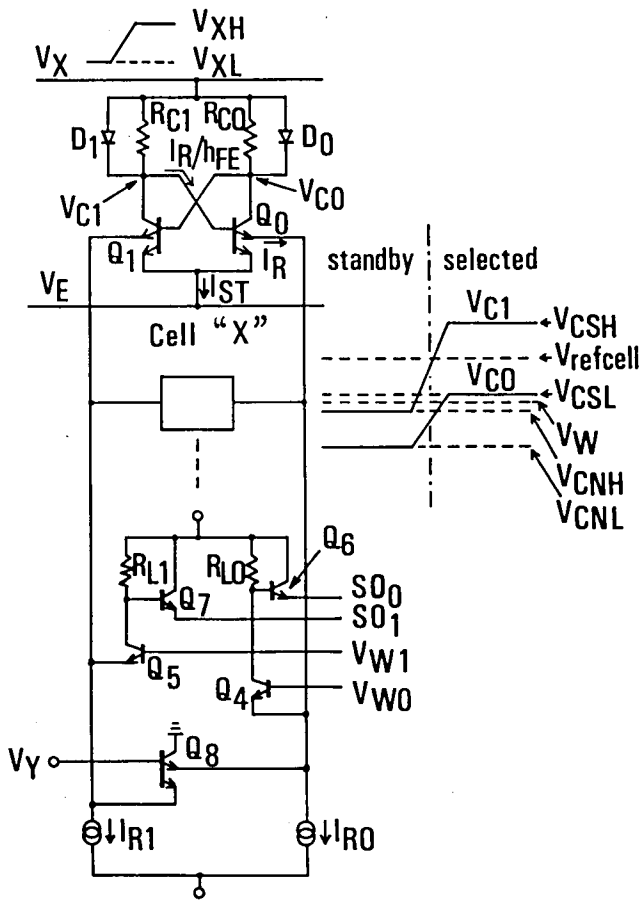


Fig. 3.1. A portion of a RAM circuit with parallel diode cells.

$$V_{CSL} = V_{XH} - V_{DO} \qquad (3.2)$$

where V_{XH} is the upper word line voltage of the cell when the line is at high voltage level of selection, h_{FE} is a common emitter current gain of the cell transistor Q_0, and V_{DO} is forward voltage drop of the cell diode D_0 while it is conducting a current which equals to $I_{RO}*h_{FE}/(h_{FE}+1)$. In Eq. (3.1), a current flowing through the cell diode D_1 is neglected because forward bias for D_1 is so small that an equivalent impedance of D_1 is assumed to be infinite. A current flowing through R_{CO} is also neglected in Eq. (3.2), because R_{CO} is too large compared with the impedance of fully forward-biased D_0.

The value $(V_{CSH}-V_{refcell})$ stands for a noise margin for the current switch of Q_0 and Q_4, and the value $(V_{refcell}-V_{CSL})$ defines a noise margin for the current switch of Q_1 and Q_5. Both values must be large enough for stable operation of a cell. Therefore, a sum of both values also must be large, but it has the upper limit of about 0.8 V as shown below. The sum is given by

$$(V_{CSH}-V_{refcell})+(V_{refcell}-V_{CSL})$$

$$=V_{CSH}-V_{CSL}=V_{DO} - R_{C1}*I_{RO}/(h_{FE}+1) \qquad (3.3)$$

(3.3)

Because the first term in Eq. (3.3) has a fixed value of about 0.8 V, the second term is required to be as small as possible.

In case of a typical 1K-bit RAM with total power dissipation of about 500 mW, I_{RO} is about 0.3 mA and R_{C1} is chosen to be about 10 KΩ. If V_{DO} and h_{FE} are assumed to be 0.8 V and 50, respectively, Eq. (3.3) is caluculated as follows:

$$V_{CSH}-V_{CSL} \text{ (for 1K)} = 0.8-0.06=0.74 \quad \text{(V)} \qquad (3.4)$$

For a 4K-bit RAM whose I_{RO} should be doubled and whose R_{C1} should be quadrupled, the above value becomes

$$V_{CSH}-V_{CSL} \text{ (for 4K)} = 0.8-0.3mA*2*10K\Omega*4/51$$

$$=0.8-0.47=0.33 \quad (V) \qquad (3.5)$$

The above value must be divided by the two current switches of the cell and sense transistors. Because a noise margin of at least about 0.3 V is required for each current switch considering parameter variation of circuit elements forming a current switch, the above value cannot afford a 4K-bit RAM with stable operating margin. On the other hand , if the same values as those of a 1K-bit RAM were chosen for I_{RO} and R_{C1} of a 4K-bit RAM to achieve high operating margin, the RAM performance would be greatly degraded.

To overcome the foregoing difficulty, the parallel diode cell was modified, while retaining its ability to supply a large amount of read current. The new cell, called variable impedance cell (VIC), is shown in Fig. 2.7. A variable impedance cell can supply as much read current as a parallel diode cell because of diodes D_0 and D_1. In addition, because its newly added p-n-p transistors Q_2 and Q_3 bypass the cell collector resistors, the voltage drop due to base current is greatly reduced. The effect of the added p-n-p transistors will be explained using equations below.

Fig. 3.2 shows a VIC when it is selected to supply a read current to a digit line. If the transistor Q_0 is on, its collector current flows through the colleltor resistor R_{CO}, the clamp diode D_0, and the base-emitter diode of the p-n-p transistor Q_3. Conduction of current through Q_3's emitter-base diode makes Q_3 active to supply its collector current I_{CQ3} to Q_0's base. Therefore, the expression (3.1) for V_{CSH} will be modified as follows:

$$V_{CSH}=V_{XH}-R_{C1}*(I_{RO}/(h_{FE}+1)-I_{CQ3})$$

$$=V_{XH}-R_{C1}*(I_{RO}/(h_{FE}+1)-I_{BQ3}*h_{FEpnp}) \quad \text{(for VIC)} \quad (3.6)$$

where I_{BQ3} and h_{FEpnp} are Q_3's base current and common emitter current gain, respectively.

The above equation shows that the value of the second term in Eq. (3.1) is decreased by an amount of $I_{BQ3}*h_{FEpnp}$. Because D_0 and Q_3's emitter-base diode clamp the lower collector level V_{CO}, Eq. (3.2) expresses V_{CSL} also for the VIC. Therefore, the cell operating range expressed in Eq. (3.3) is rewritten for the VIC as follows:

$$V_{CSH}-V_{CSL}=V_{BEQ3}-R_{C1}*(I_{RO}/(h_{FE}+1)-I_{BQ3}*h_{FEpnp}) \quad (3.7)$$

$$=0.8-R_{C1}*(I_{RO}/(h_{FE}+1)-I_{BQ3}*h_{FEpnp}) \quad (V) \quad (3.8)$$

where V_{BQ3} is Q_3's emitter-base forward bias voltage.

In the above equation, a current flowing through D_0 is supposed to be a portion of I_{BQ3} because the diode D_0 really forms a portion of Q_3's emitter diode in the device structure, which will be described afterwards (see Fig. 3.5.).

The current flowing through R_{CO} can be neglected compared with I_{BQ3}, because R_{CO} is much larger than an equivalent impedance of fully forward-biased emitter-base diode of Q_3. Provided that R_{CO}= 60 KΩ and a voltage across R_{CO} is 0.8 V, the current through R_{CO} is 13 μA, which is small enough compared with I_{BQ3}. It is nearly equal to 420 μA in the RAM design. Therefore,

$$I_{BQ3}\doteqdot I_{RO}*h_{FE}/(h_{FE}+1) \quad (3.9)$$

Eq. (3.8) is transformed using Eq. (3.9) into the following equation:

$$V_{CSH}-V_{CSL}\doteqdot 0.8-R_{C1}*I_{RO}*\frac{h_{FE}}{(h_{FE}+1)}*(1/h_{FE}-h_{FEpnp}) \quad (3.10)$$

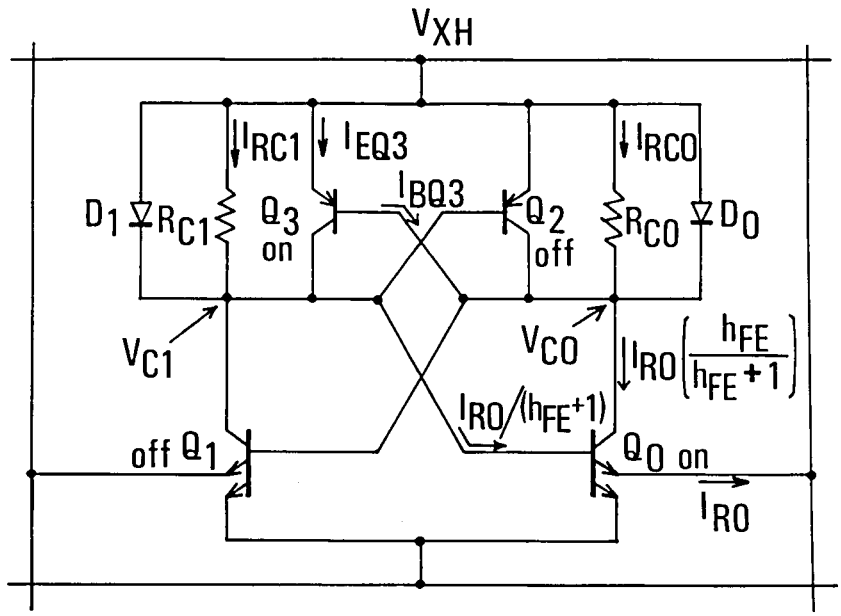


Fig. 3.2. Node voltages and branch currents of a selected variable impedance cell.

The above equation shows that cell operating range (V_{CSH}-V_{CSL}) is greatly increased only if h_{FEpnp} is nearly equal to $1/h_{FE}$, which is a very small value (=0.020 if h_{FE}=50). This means that a p-n-p transistor with a low common-emitter current gain would greatly increase cell operating range. This is desirable because realization of high-performance n-p-n and p-n-p transistors, both of which have high-performance, on the same silicon chip is difficult. This is one of the advantages of the VIC.

Both transistors Q_0 and Q_3 in Fig. 3.2 are saturated because the collector-base junctions of both transistors are forward-biased. In a saturated transistor, its equivalent common-emitter current gain (h_{FE} or h_{FEpnp}) decreases, because the net collector current is the difference of the two injected currents at both junctions (base-emitter and base-collector). As degree of saturation becomes deeper, h_{FE} or h_{FEpnp} becomes smaller.

If h_{FEpnp} is greater than $1/h_{FE}$ in Eq. (3.10), degree of saturation of Q_0 and Q_3 will automatically be increased, resulting in reduced equivalent h_{FE} or h_{FEpnp}. Therefore, the value ($1/h_{FE}$-h_{FEpnp}) in Eq. (3.10) is always a certain positive value.

The above mentioned effect of the added p-n-p transistors will best be illustrated in Fig. 3.3, which shows how the cell collector voltages vary as the read current is increased in a selected cell. V_{C1} and V_{C0} are the higher and lower collector voltages of the cell, respectively. The same 50 KΩ collector resistors are used for the VIC and the parallel diode cell. The curve for the VIC was obtained from measurement of a test cell integrated on the edge of the 4K-bit RAM chip. The curve for the parallel diode cell was calculated. The difference of both curves is clear. In case of a parallel diode cell, the higher collector voltage V_{C1} drops as the read current increases. The gradient of this slope is 50 kΩ divided by current gain h_{FE} of the cell transistor. In case of the VIC, however, V_{C1} remains at a high poten-

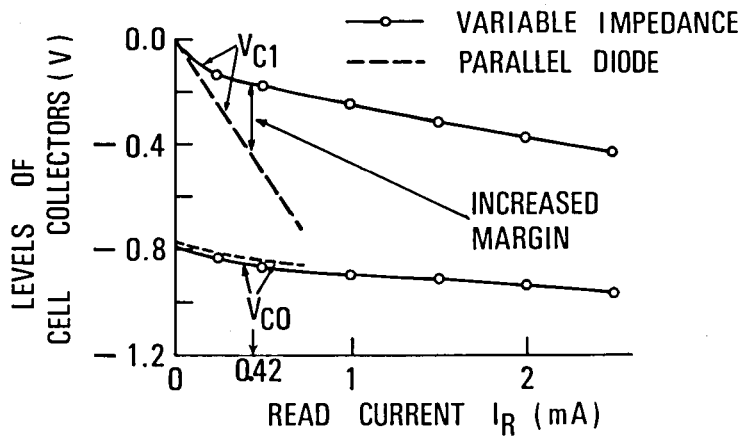


Fig. 3.3. Cell collectors' potential levels versus read currnt.

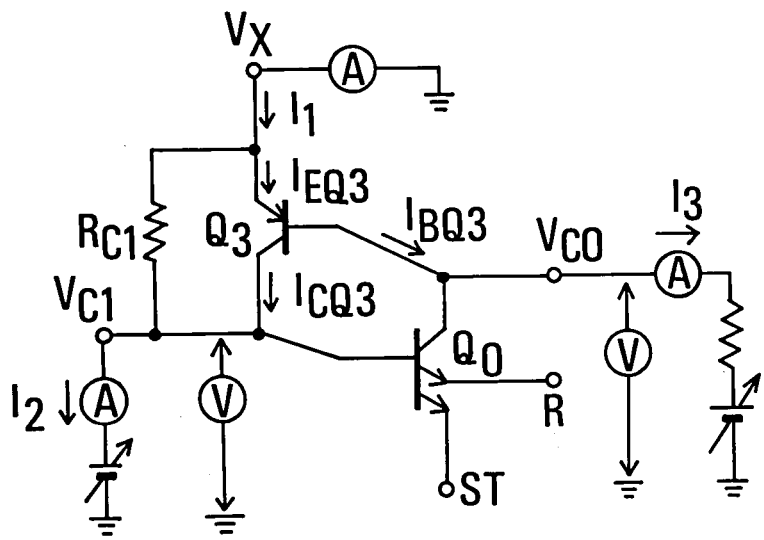


Fig. 3.4. A test cell circuit.

tial level even if the read current is increased. This effect results from the previously mentioned function of the p-n-p transistors.

The 4K-bit RAM has a read current of 0.42 mA. Thus, using the VIC, the operating range was increased by the amount as shown in Fig. 3.3. This figure also shows that the value of the read current can be increased further to obtain a faster access time.

The h_{FEpnp} is one of the design parameters of the VIC. If the h_{FEpnp} becomes large, the more base current is fed to the transistor Q_0, compelling Q_0 to saturate more deeply. The deeply saturated cell needs a long write pulse width to be toggled into the other state, because it takes more time to extract the stored charge from the saturated Q_0.

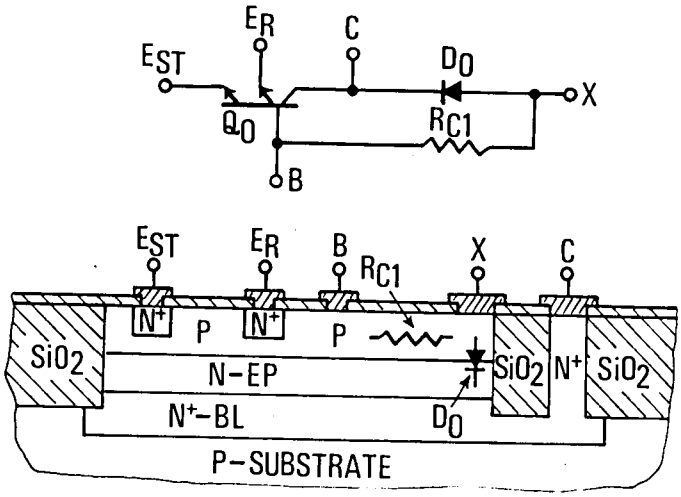
On the contrary, if the h_{FEpnp} is too small, the cell will be reduced to the conventional parallel diode cell which has too narrow operating range to be used for a 4K-bit RAM.

The above discussion implies that the optimum value of the h_{FEpnp} exists. The value of the h_{FEpnp} was decided experimentally. Because only a small value is required for the h_{FEpnp}, the p-n-p transistor structure shown in Fig. 3.5 has given h_{FEpnp} enough to realize the 4K-bit RAM with wide operating range. The actual value of the h_{FEpnp} was measured using a test cell shown in Fig. 3.4. The test cell was made by a half cell circuit of the VIC. In Fig. 3.4, nodal currents and voltages were measured to estimate h_{FEpnp}, which is given by the following equation:

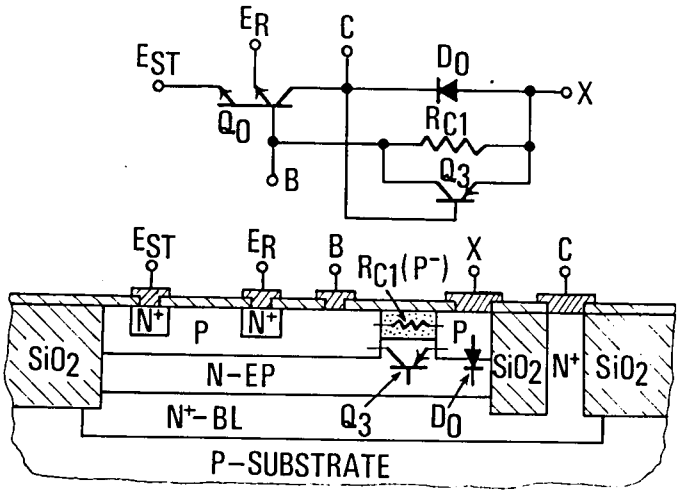
$$h_{FEpnp}=I_{CQ3}/I_{BQ3}=(I_2-(V_X-V_{C1})/R_{C1})/I_3 \qquad (3.11)$$

The righthand side of the above equation was evaluated for some value of (V_X-V_{CO}) and (V_X-V_{C1}). As a result, the h_{FEpnp} was estimated to be around 0.2-0.4 when the p-n-p transistor was not saturated deeply.

Fig. 3.5 shows half of a cell circuit and its cross section for a VIC and a parallel diode cell. The only difference between



(a)



(b)

Fig. 3.5. Half of a cell circuit and its cross section. (a) Parallel diode cell. (b) Variable impedance cell.

both cells exists in the device structure of the collector resistor R_{C1}. In the case of a parallel diode cell, the same p-region is used for both the transistor Q_0 base and the collector resistor R_{C1}. In the case of a VIC, however, the two p-regions are separated by a p^--region which forms a collector resistor of high value. Because the depth of the p^--region is shallower than that of the two p-regions, these p-regions, together with an n-epitaxial layer, act as a p-n-p transistor which bypasses the p^- high value collector resistor. All other configurations are the same as for a parallel diode cell. Therefore, it is possible to add the p-n-p transistors without increasing silicon area.

Fig. 3.5 (b) shows that the diode D_0 can be regarded as a portion of the emitter-base diode of the transistor Q_3. Therefore, the diodes D_0 and D_1 can be omitted from the cell circuit diagram shown in Fig. 2.7.

The device structure of the p-n-p transistor Q_3 as shown in Fig. 3.5 (b) makes the value of the h_{FEpnp} smaller because the existence of the p^--layer limits carrier injection area of the Q_3 emitter. Moreover, this effect of the reduced h_{FEpnp} is aggravated by the fact that the p^--layer exists in the narrowest region between the two opposing p-layers. That region would function to increase the value of the h_{FEpnp} greatly if it were not for the p^--layer. This structure, however, is quite acceptable for a VIC which would have a long write pulse width if the h_{FEpnp} were large. The other advantage of this structure is realization of a " buried " p-n-p transistor whose base region is buried into the silicon. Therefore, its h_{FEpnp} can be liberated from the surface effect which is often one of the causes for anomalous h_{FEpnp}.

3. Cell Margin Increasing Circuitry

The second technique used to realize a RAM with a wide operating range is the cell margin increasing circuitry shown in Fig. 3.6 which depicts an outline of the 4K-bit RAM circuit

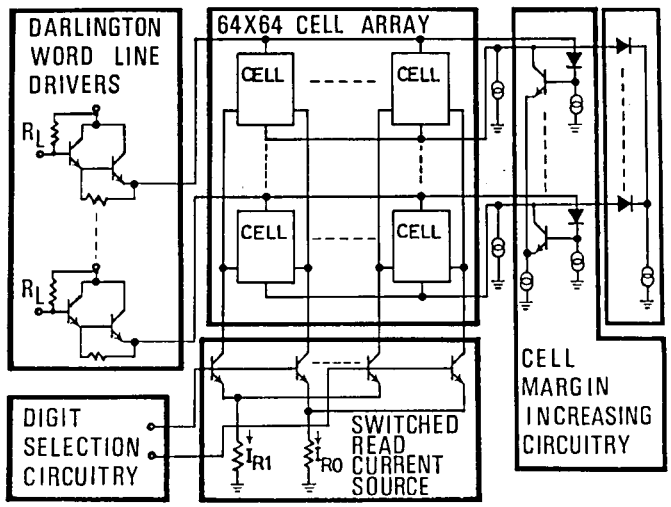


Fig. 3.6. Outline of circuit diagram of the 4K-bit RAM.

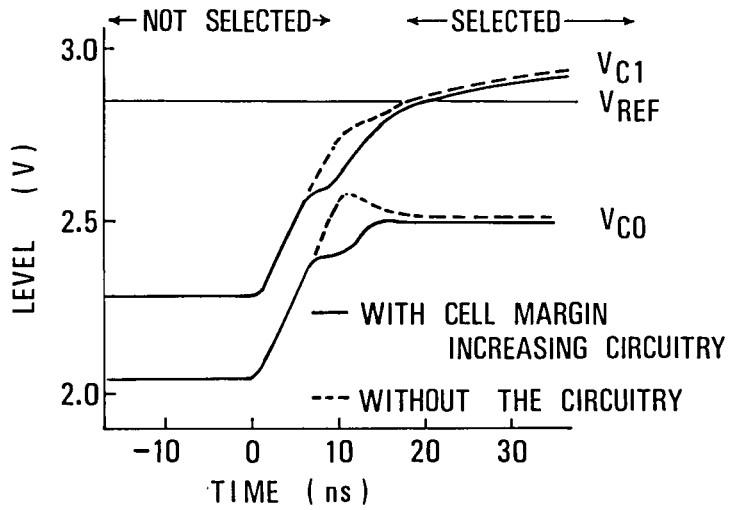


Fig. 3.7. Simulated waveforms of cell collector voltages during the transition from not selected to selected.

diagram.

To reduce power, the stanby current of a cell is decreased to 4 μA, and its collector resistors are increased correspondingly to 60 kΩ. The risk of malfunction of the cell flip-flop caused by low standby current was avoided by the circuitry described below.

The circuitry consists of one current source and 64 transistors, which forms a current switch. This configuration allows cells on a selected word line to have more standby current than they have when not selected. This standby current increase occurs at the instant when a cell is going from not selected to selected.

The circuitry, shown on the right side in Fig. 3.6, consisting of 64 diodes and one current source, also increases the standby current of cells on a selected word line. But, because diode-gating is performed through the lower word lines, the increase of standby current occurs after the cells have been selected. Consequently, it cannot help increase the operating margin of a cell which is going to be selected, but it does accelerate discharging of word lines when they change from selected to not selected. Therefore, it is properly called word line discharge circuitry because of its function[17,24].

On the contrary, since the cell margin increasing circuitry gates through the upper word lines, it can help increase the cell standby current at the instant when it is being selected.

Fig. 3.7 shows the simulated waveforms of cell collector levels with and without the cell margin increasing circuitry. V_{REF} is the reference voltage for sensing stored data in a cell. Without the circuitry, the cell lower collector level V_{CO} peaks when a cell is being selected. If the potential difference between this peak and the reference voltage decreases, the possibility of cell flip-flop malfunction increases. Using cell margin increasing circuitry, this peak diminishes to the level of the solid line. Disappearance of this dotted peak proves that at this moment the cell standby current is increased because the standby

current increase causes a decrease in the potential level of the lower collector level V_{CO}. The standby current increase gives the cell more energy to resist against noise-induced inversion.

The purpose of the cell margin increasing circuitry is to increase the standby current of a cell which is about to be selected. For that, it is desirable that the standby current increase should begin a little time before the cell starts to be selected. This requirement, however, is difficult to realize because both the cell selection and its standby current increase are simultaneously initiated by the potential rise of the upper word line. The above discussion suggests that the effectiveness of the cell margin increasing circuitry depends greatly on the time differerence between the standby current increase and the cell selection.

To verify the actual effectiveness of the circuitry would require to compare the operating ranges of a RAM with the circuitry and a one without it. This comparison, however, has not been carried out. Therefore, the effect of the circuitry has not yet been proved except for the simulation shown in Fig. 3.7. In spite of the lack of the actual proof, the cell margin increasing circuitry was integrated to the 4K-bit RAM because its adoption causes small expenses. About 64 additional transistors and diodes required for the circuitry caused negligible increase of the chip area, and only small amount of current of about 7 mA was added to the total power supply current. Moreover, addition of the circuitry would not injure the RAM function even if it does not serve to increase the RAM operating range.

4. Other Circuit Techniques

Third way to decrease the power dissipation of the RAM is to arrange the circuit so that one pair of read current sources is shared by 64 pairs of digit lines (see Fig. 3.6)[24,17,25,18,

[22]. This technique made it possible to increase the read current in order to cope with the increased parasitic capacitance connected to the digit lines without greatly increasing the total power dissipation. Because the value of 0.42 mA was adopted for the read current, total of 53 mA (=0.42*63*2) was saved. This value is comparable to the total power supply current of the RAM (see Table 3.1).

The last innovation applied to the RAM circuit was Darlington word drivers. With this circuit, fast switching of the word line is achieved at low power because the source impedance of a Darlington word driver is reduced by a factor of h_{FE} compared to a conventional emitter follower driver.

A Darlington connection of transistors also helps reduce the fluctuation of potential levels of the word lines caused by device parameter variation. Because the equivalent current gain h_{FE} of the transistors is very large (the equivalent gain is the product of both transistors' current gains.), a potential drop across a load resistor R_L due to base current is greatly reduced. (The load resistor R_L is connected to the collectors of transistors in a word driver current switch which is not shown in Fig. 3.6.) Therefore, the levels of the word lines remain approximately constant against variations of h_{FE} and resistance. This feature was very effective when a high value load resistor was used to decrease the power dissipation of the word drivers.

A major drawback of the Darlington word driver is that it introduces an additional voltage drop of about 0.8 V (= one V_{BE}). This penalty was alleviated by optimized allotment of the power supply voltage (=5 V) to those circuits which were connected each other in series between the power supply voltage V_{CC} and the V_{EE} (ground). A requirement in power supply voltage allotment was to prevent every transistor in the circuits from being deeply saturated even in the worst-case conditions. In spite of the adoption of Darlington word drivers, the operating range of the RAM was wide enough as shown in Section 6 (see Fig. 3.12).

Power allocation of the RAM was optimized to obtain as fast an access time as possible with proper attention to operating margin of the cell array. Table 3.1 shows the resultant power allocation of the RAM.

5. Processes and Devices

An outline of the process and device technology is shown in Table 3.2. Oxide isolation and fine pattern technology were employed to realize high performance and a small chip size. Although the values of the line width and spacings for the 1st and 2nd layer metallizations were those of the finest ones for that age, the chip and cell sizes are larger than those of the 4K-bit RAMs in the literatures (17) and (20). The performance of the RAM, however, are superior to the above 4K-bit RAMs. The superiority in performance may owe to the circuit techniques described above.

Figs. 3.8 and 3.9 show photomicrographs of the chip and the cell, respectively.

6. Performance

Major electrical characteristics of the fabricated RAM are summarized in Table 3.3. The RAM is fully compatible with standard TTL. Fig. 3.10 shows an example of switching waveforms. The temperature and power supply voltage dependence of the address access time are illustrated in Fig. 3.11, which show that the maximum address access time of 45 ns can be guaranteed over the operating range of T_a=0-75°C, and V_{CC} =4.5-5.5 V. Fig. 3.12 shows the operating range for the power supply voltage and temperature in which the RAM can function properly. The use of Darlington word drivers introduced an additional voltage drop, which reduced

TABLE 3.1

Power Allocation of the RAM

Memory cell array	18.4
X address decoder	3.7
Word drivers	8.3
Y address decoder	5.0
Digit drivers	13.4
Sense amplifiers	3.0
Output amplifiers	10.7
Control circuit	2.4
Others	3.1
Total	68.0 (mA)

TABLE 3.2

Outline of Process and Device Technology

- OXIDE ISOLATION
- DOUBLE LAYER METALLIZATION
  LINE WIDTH PLUS SPACINGS { 1ST 9 μm; 2ND 15 μm }
- CHIP SIZE 3.4 mm X 6.3 mm
- CELL SIZE 2475 μm^2
- EMITTER SIZE 3 μm X 3 μm MIN.
- $C_{TS} = 0.13$, $C_{TC} = 0.041$, $C_{TE} = 0.034$ (pF)

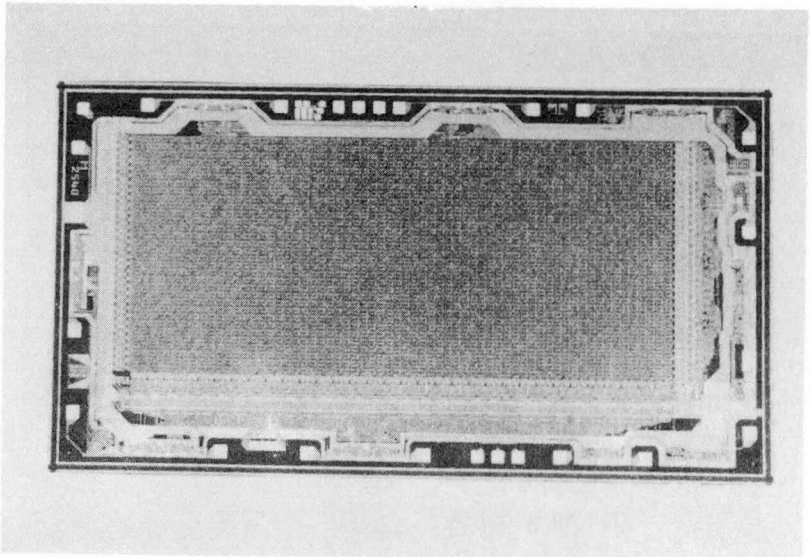


Fig. 3.8. Photomicrograph of the 4K-bit RAM chip.

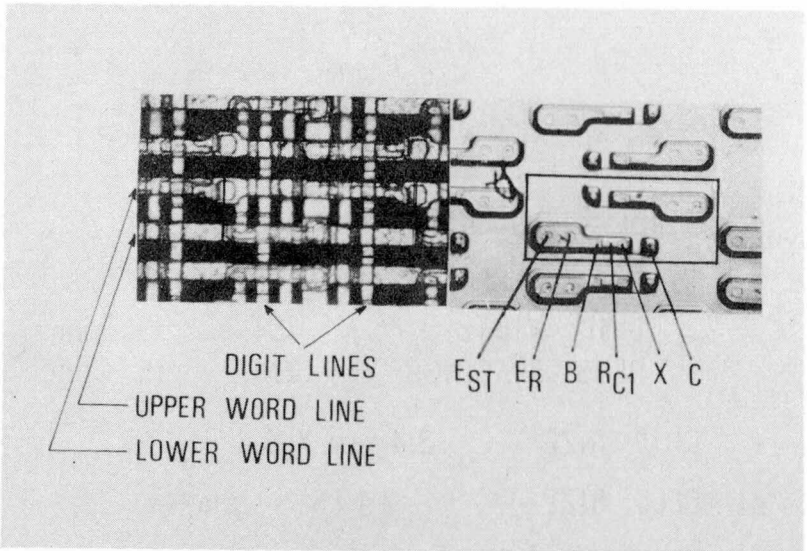


Fig. 3.9. Photomicrograph of the memory cell. Its size is 77 X 33 μm^2.

TABLE 3.3

Major Electrical Characteristics of the RAM

Address Access time	25 ns typ.
Chip Select Access Time	17 ns typ.
Minimum Write Pulse Width	20 ns typ.
Power Dissipation (V_{CC}=5V)	350 mW typ.

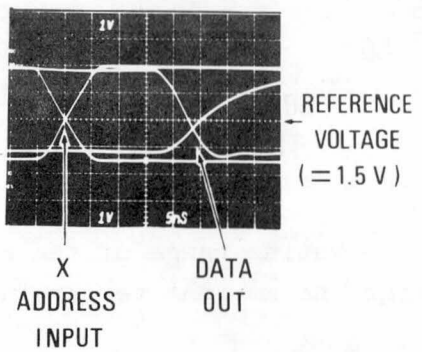


Fig. 3.10. Switching waveforms showing an access time of 25 ns (I_{CC}=70 mA).

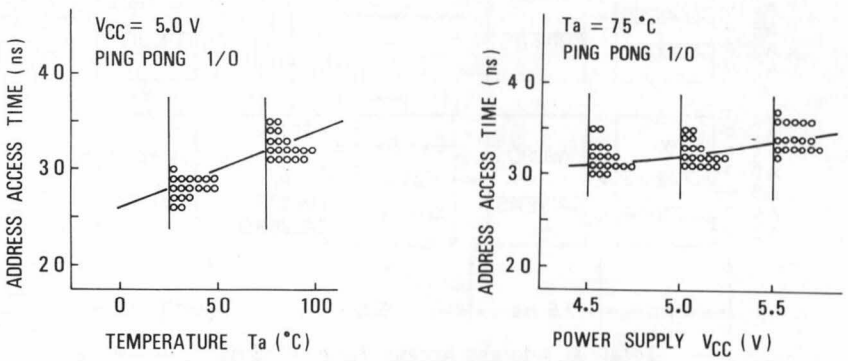


Fig. 3.11. Address access times of the RAM when all the cells are scanned with a ping-pong 1/0 pattern (see Sec. 7 in Chap. IV and Sec. 2 in Chap. V). (a) Temperature dependence. (b) Power supply voltage dependence.

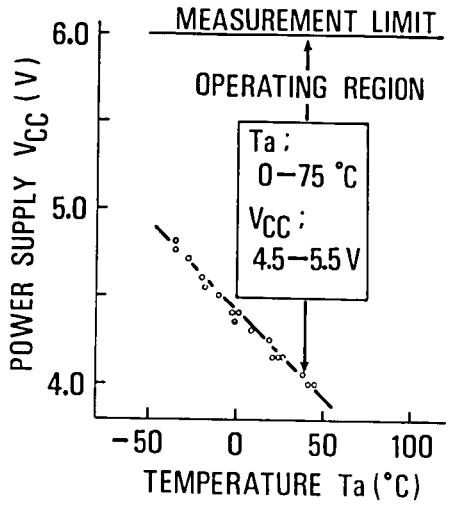


Fig. 3.12. Operating range of the RAM with regard to its power supply voltage and ambient temperature.

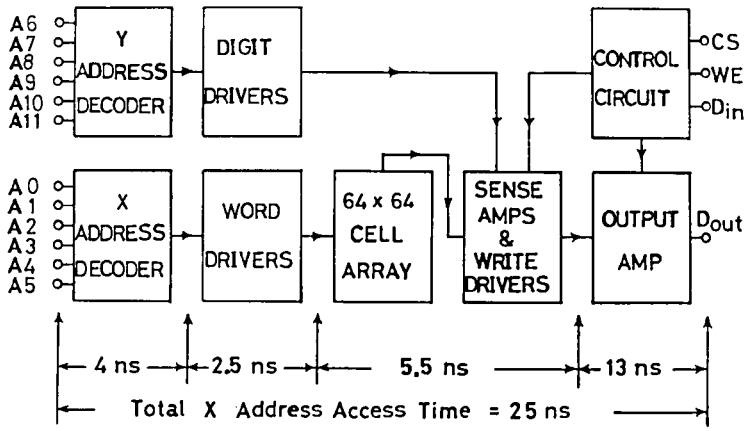


Fig. 3.13. Block diagram of the RAM and a breakdown of an X address access time.

the lower operating limit of V_{CC}, making the RAM operation critical at low ambient temperatures. But the RAM can operate over the wide operating range of T_a=0-75 °C and V_{CC}= 4.5-5.5 V as shown in the figure.

Fig. 3.13 shows a block diagram of the RAM and a breakdown of an X address access time. The block diagram is typical of a conventional static bipolar RAM. A critical path for access is an X address access time, which was divided into four partial delays as shown in the figure. These data were obtained by probing the chip. Investigation of the breakdown revealed that the delay of the output amplifier is very long (~13 ns).

The RAM was designed to be compatible with TTL ICs because it was planned to be used with them, and because bipolar 4K-bit RAMs were supposed to find their application in the TTL environment at first, and later in the ECL one. A combination of ECL internal circuitries and processes intended for non-saturating devices, which had been successfully applied to produce commercial 256- and 1024-bit RAMs, was also adopted for the RAM. However, it necessitated the output amplifier which converts the ECL sense amplifier output to TTL voltage levels. And, the amplifier's delay cannot help bocoming very long because it has to be composed of non-saturating devices.

Therefore, it is expected that an ECL version of the RAM, which does not require the voltage level conversion from ECL to TTL, will show an address access time of around 10 ns while retaining power dissipation of 350 mW without any significant modification of circuit and processes[17].

7. Conclusion

The development of a 4K-word by 1-bit TTL compatible static RAM has been described in this chapter. Its typical and worst-maximum address access times were found to be as fast as 25 and 45 ns, respectively, while its power dissipation was as low as

350 mW. The product of typical operating power and address access time was 2.1 pJ/bit. The above high speed and low power was realized by use of variable impedance cells, other sophisticated circuit techniques, and oxide isolation with double layer metallization. The newly proposed variable impedance cell can supply a larger amount of read current to digit lines than a conventional parallel diode cell when the cell standby current is reduced to about several micro-amperes. Comparison of the both cells was also presented.

The RAM presented will allow the board density of buffer and control memories of large computers to be increased by a factor of four without a significant loss in speed or increse in power.

CHAPTER IV

A PAIR OF BIPOLAR MEMORY LSI CHIPS FOR A MAINFRAME COMPUTER

1. Introduction

High-speed bipolar memories continue to play important roles in high-performance mainframe computers. This is because they are used in the storage control unit as well as in the buffer storage, and greatly affect the speed of processor execution[58,59].

This chapter describes a new pair of bipolar memory LSI chips brought forth by endless pursuit of improving memory access cycles in mainframe computers. The pair consists of a newly devised index array (IA) chip and a standard buffer storage (BS) chip. The IA chip includes not only a 3072-bit RAM with its peripheral circuits, but also additional 470 logic gates on the same chip. The BS chip is a standard 1024-bit RAM with an ultra-high speed access time of 5.5 ns typical. The new pair of chips is used in Hitachi's newest mainframe computer, the M200H. They contribute greatly to the more than 8 million instructions per second (MIPS) performance which the M200H typically realizes.

At first, Section 2 will describe design considerations leading to the development of the two chips fairly different each other in functions and integration level. And, the major chip characteristics will also presented there. In Section 3, the block diagram and the functions of the IA chip will be explained. The BS chip design will be discussed in Section 4. Almost every RAM design of today is performed by use of circuit simulation programs. Circuit design steps using a simulation program will briefly be presented. How the optimum power allocation of a RAM

is made will also be described.

Processes and devices of the pair will be summarized in Section 5. How the BS chip's access time is dependent on various device parameters has been analyzed to achieve the high speed. And, based on the analysis, a special effort has been made to improve transistor cut-off frequency f_T which has been found to be the most influential parameter on the access time.

Section 6 will describe the performance of the both chips. Section 7 will present how the BS chip's access times have been measured. Usually, a commercial memory tester of today has an accuracy of $\pm$ 1 to $\pm$ 3 ns in access time measurement. This accuracy is not enough to measure as fast an access time as 5.5 ns of the BS chip. Therefore, a special adapter circuit had to be attached to a memory tester to perform accurate and precise evaluation. Testing of ultra-high speed bipolar RAMs will be studied in more detail in Chap. V.

2. Design Cosiderations and Major Chip Characteristics

The outline of a conventional memory access mechanism in a mainframe computer which adopts buffer memory as well as virtual memory system is shown in Fig. 4.1. Categorically, the buffer storage is sometimes included in the storage control unit. But, in the figure, they are indicated separately for better understanding of their functions.

An instruction or an operand address in a logical address register of the instruction unit is sent to the storage control unit, where the address is translated from virtual value to real one. Then, it is checked whether the data for that address are in the buffer storage or not. If the data are in the buffer storage, they are read out, and sent to the instruction unit. On the contrary, if the data are not in the buffer storage, they are sent from the main storage, through the buffer, to the instruction

unit. It is evident that the former case, that the requested data exist in the buffer storage, has a much faster access cycle than the latter case that they are not in the buffer, because the latter cycle includes a slow read cycle of the main storage.

It is usual that a small number of fast-but-high-cost-per-bit bipolar memories are used for the buffer storage, and that a large number of slow-but-low-cost-per-bit MOS memories are used for the main storage. The buffer is used to store the data of those portions of the main storage that are currently used. Therefore, most instruction fetches can be performed by referring to the buffer, resulting in a short memory access time most of the time. This hierarchical organization of memory devices with different cost and performance is a cost effective approach found in most general-purpose mainframe computers[58,59].

The above functions of the storage control unit are called dynamic address translation and buffer storage control, or cache control. There are two major storage areas in the storage control unit. One is the translation lookaside buffer (TLB) which contains the tables required to translate virtual addresses to real ones. The other is the buffer address array (BAA) which contains the addresses of data stored in the buffer storage. The speeds of TLB and BAA, as well as the access time of the buffer storage itself, are key parameters for improving processor performance.

A pair of very high-speed bipolar memory LSIs has been developed to speed up the memory cycles in the M200H. The major characteristics of the pair are depicted in Table 4.1 and are compared to the bipolar memory ICs used for an existing Hitachi mainframe computer, the M180. The M180 was announced in 1974 and is now in production, while the M200H was announced recently (late in 1978). The performance of the M200H is 2.5 to 3 times better than that of the M180 in terms of MIPS. One major reason for this performance improvement is this bipolar pair.

One is an index array (IA) chip designed for use in the TLB as well as in the BAA. The degree of integration for the IA chip

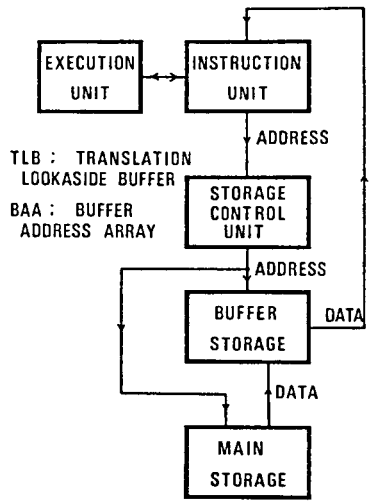


Fig. 4.1. Outline of memory access mechanism in a main-frame computer.

TABLE 4.1

Comparison of Bipolar Memory ICs
Used in the M200H and M180

COMPUTER		M 200H	M 180
RELATIVE PERFORMANCE		2.5 — 3.0	1
BIPOLAR MEMORY	TLB	IA CHIP : $3072^{b}+470^{gate}$ 6.7ns typ , 8.0ns max	$128^{w} \times 1^{b}$ 12 ns max
	BAA		$256^{w} \times 1^{b}$ 15 ns max
	BS	BS CHIP : $1K^{w} \times 1^{b}$ 5.5ns typ , 7.0ns max	$1K^{w} \times 1^{b}$ 35 ns max

is greatly increased compared to the small storage bipolar memories used in the M180. This new chip consists of a 3072-bit RAM and 470 logic gates. The chip includes not only peripheral circuits for cell array, but also additional logic for compare functions. Therefore, off-chip propagation delays between the memory and compare-logic have been eliminated. This leads to the realization of fast dynamic address translation and buffer storage control. This is a novel bipolar memory approach to mainframe computers.

The performance of the two chips is optimized and cooperatively function to improve computer performance. This performance optimization has led to a comparatively large difference in degree of chip integration. Integration for the BS chip was chosen to be 1K bits to realize a fast access time. It might be increased to 4K bits with the same performance in the future with further progress in bipolar technology[22].

Another consideration concerning specification optimization was cost. It is desirable to reduce cost for semiconductor devices by producing them in large volumes. For this purpose devices should be standardized for various kinds of user application. The BS chip has been designed as a standard 1K-bit RAM compatible with the 10K logic family, and housed in a conventional 300 mil wide, 16 pin dual-in-line cerdip. The IA chip, however, could not help being a customized LSI intended solely for in-house use because of performance requirements.

3. IA Chip

A block diagram of the new IA chip is shown in Fig. 4.2. It consists of eight 64 X 6-bit RAMs divided into two sections, the a- and b-planes. Two CA inputs (CA0 and CA1) select one 64 X 6-bit RAM block from the four blocks in each plane and six address inputs (A0-A5) select one set of six bits from the

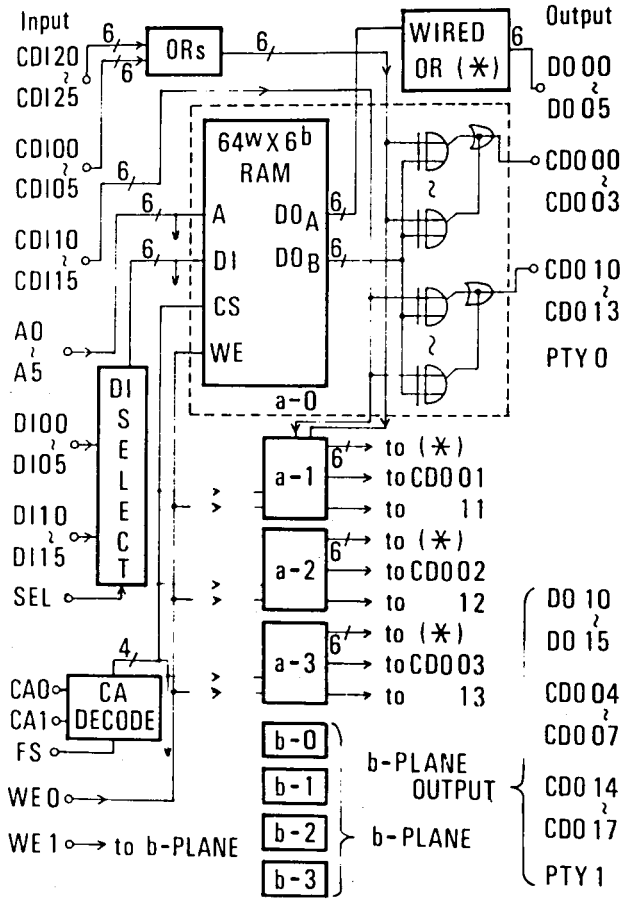


Fig. 4.2. Block diagram of the index array (IA) chip.

selected block.

The block diagram of the IA chip represents functions which eight memory ICs and a plural number of logic ICs would have co-operatively realized so far. Therefore, the concept of eight memory chips is preserved in the IA block diagram although those memory and logic ICs have been merged into the single LSI chip. From this point of view, CAs may be considered to stand for an address of one of the eight memory "chips", by which one "chip" is selected out of the eight ones. One should note that decoded signals of CAs go to CS (chip select) inputs of the memory blocks. In the actual IA chip, CA inputs are used to select several columns in the memory matrix. Therefore, they may also regarded as column addresses.

The SEL input decides whether either of two sets of data inputs (DI00-DI05, DI10-DI15) should be written into a block. WE0 and WE1 control writing in the a- and b-planes, respectively.

Three types of data outputs are available. The first consists of two set of six DO outputs (DO00-DO05, DO10-DO15) which represent the stored data in each block on both planes. From this standpoint, the IA chip is looked upon as two 256-word-by-6-bit RAMs because CA0 and CA1 are regarded as part of the address inputs.

The second consists of CDO outputs. The 6-bit read-out data from each block are compared with 6-bit CDI inputs using the exclusive OR gates shown in the figure. A low voltage level signal appears at the CDO terminal when all CDI bits coincide with those of the stored data, and a high level is obtained when they do not coincide. This compare function is necessary to organize BS and IA chips as a set associative memory[59].

Two CDO outputs are obtained for each block by comparing the stored data with three sets of CDI inputs (CDI20-CDI25/CDI00-CDI05 and CDI10-CDI15),two of which are OR-ed. When FS is low, two CA inputs are enabled to select one block for each plane, giving CDO outputs solely for the selected block. However, when

FS input is high, CA inputs are disabled and all eight blocks are selected, giving CDO outputs for all blocks.

The third type of output is PTYO and PTY1 for parity checks.

The actual circuit configuration is that two 64-row by 24-column cell matrices are driven by 64-word (row) drivers placed between the two cell matices (refer to Fig. 4.12). Selection of one word driver from the 64 is performed by the information from AO to A5. The 24 columns are divided into four groups, each of which consists of six columns representing a set of 6-bit data. Selection of one group of 6 bits is decided by the information from CAO and CA1.

Some special pins (not shown in Fig. 4.2) were added to control the power supply to the CDO output current switches. This power reduction mode is useful when CDO outputs are not in use.

4. BS Chip

4.1 Basic Principles of Cicuit Design

The main objective of the BS chip was to achieve an access time as fast as 7 ns worst-maximum. For that purpose, comparatively small bit density of 1K bits per chip was chosen although a 4K-bit RAM was desirable for the system performance. An ECL version of the 4K-bit RAM described in Chapter III would show an access time of around 10 ns as mentioned in Section 6 of the chapter. But it was not supposed to satisfy the worst-maximum access time of 7 ns. Moreover, an ultra-high speed 4K-bit RAM with a typical access time of 6 ns described in the literature (22) was considered to require a long time until it would be transferred from pilot run to volume production. Therefore, the ultra-high speed 4K-bit RAM was scheduled to replace the 1K-bit BS chip afterwards when the system performance would be upgraded.

The important measures applied to the BS chip to achieve the above high speed are as follows:

(1) Adoption of a conventional parallel diode cell with Schottky barrier diodes as parallel diodes.

(2) Adoption of advanced oxide isolation technology. Great efforts have been made to achieve high performance device parameters which are shown in Table 4.2.

(3) The total power dissipation was increased to 800 mW typ., which was the upper limit allowed by cooling requirement of printed circuit boards on which the BS LSIs were mounted.

(4) Optimized allotment of the above power of 800 mW to each circuit of the RAM. This was done with the help of a computer program for transient analysis of circuits.

In case of a 1K-bit RAM, the voltage drop across a collector resistor caused by base current of a cell transistor feeding read current is too small to necessitate such a cell suitable for large capacity memories as a variable impedance cell. The voltage drop is fatal to the 4K-bit RAM described in Chapter III. The finally-defined values for a collector resistor and read current of the BS chip cell were 11 KΩ and 0.65 mA, respectively. The voltage drop due to base current was then estimated to be about 140 mV if h_{FE} of the cell transistor was assumed to be 50. This value was not a catastrophic one for the 1K-bit RAM design. Therefore, a parallel diode cell shown in Fig. 4.3 was chosen.

The Schottky barrier diode was adopted for the following reasons:

(1) Because the RAM is operated at very short cycles, its write pulse width must be small. The SBD can reduce the write pulse by preventing a cell transistor to saturate deeply. Degree of saturation of the transistor can be controlled by the forward voltage drop of the SBD. Therefore, by controlling the forward voltage drop, the write pulse width was fixed for a specified value.

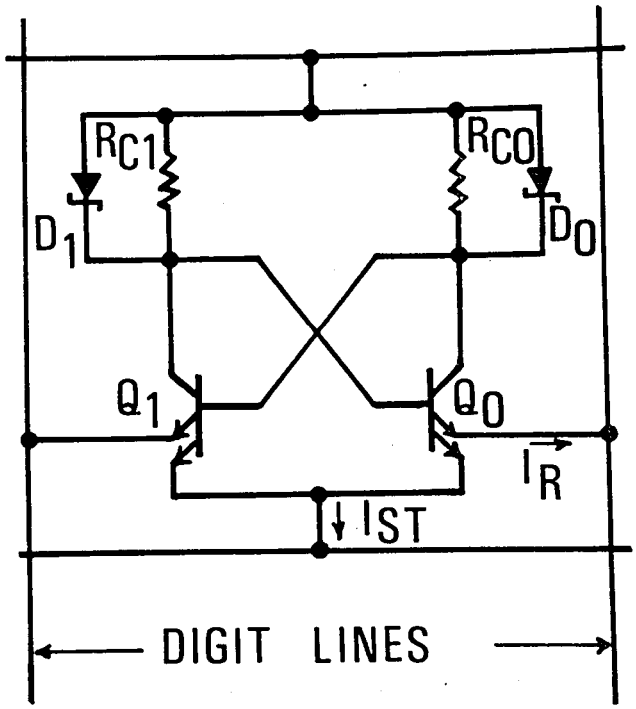


Fig. 4.3. Memory cell circuit.

(2) The forward voltage drop V_F of a SBD is about 0.5-0.6 V, which is smaller than that (=0.8 V) of a P-N diode. A parallel diode cell with SBDs then has a smaller value of (V_{CSH}-V_{CSL}) because (V_{CSH}-V_{CSL}) is about the same as the forward voltage drop V_F of the cell clamp diode (see Eqs. (3.3) and (3.4)). Because cell's read/write operation requires a voltage swing of an upper word line to be about 0.2 V larger than the value of (V_{CSH}-V_{CSL}), the voltage swing of an upper word line of a cell with SBDs can be designed to be as small as about 0.7-0.8 V, compared with about 1 V of a cell with P-N diodes. A faster access time is expected for a cell with SBDs because the smaller voltage swing leads to the faster switching time of the word line.

(3) One of the ways to make a parallel diode cell respond more quickly to the upper word line's switching is addition of a capacitance across a cell collector load. Because the added capacitance reduces equivalent high-frequency impedance between the upper word line and the base of the cell's on-transistor, the switching signal of the upper word line is quickly transferred to the on-transistor base through the reduced impedance.

In Fig. 4.3, on-transistor Q_O's response to fast potential rise of the upper word line is delayed because of high impedance of R_{C1}. But, the series capacitance of the SBD D_1 acts as the above mentioned bypassing capacitance, resulting in apparently reduced high-frequency impedance of R_{C1}.

Bypassing resistance between an input and a transistor base by use of capacitance is one of the well known techniques to speed up transistor switching [60].

The design of the 1K-bit BS chip didn't adopt those circuit techniques applied to the 4K-bit RAM as cell margin increasing circuitry, sharing of read current sources, and Darlington word drivers. As described earlier, the cell margin increasing circuitry

requires as shortest a delay as possible between the beginning of cell current increase and the upper word line's potential rise to achieve its purpose. However, because the BS chip's access time was too fast to afford such a short delay, the cell margin increasing circuitry was not used.

The sharing of read current sources was not adopted for the following reasons. An Y address access time of the BS chip had to be made one nanosecond faster than its X address access time because of the system requirement. Because the read current source sharing requires an additional delay to switch read current sources, the sharing makes it difficult to satisfy the above difference in the X and Y address access times. Furthermore, because an 1K-bit RAM requires only half a number of read current sources which a 4K-bit RAM would require, the sharing is isn't so imperative as in case of a 4K-bit RAM.

But, it is true that a large portion (27%) of the total power dissipation of 800 mW is spared to the read current sources. To achieve high speed, the value of the read current of the BS chip was designed to be as large as 0.65 mA, compared with 0.42 mA of the 4K-bit RAM described in Chapter III.

The Darlington word drivers also were not used because their effectiveness was decreased in a 1K-bit RAM which were able to have a low source impedance for a word driver. The source impedance of the 1K-bit RAM is about 1 KΩ. On the other hand, it is about 10 KΩ in the 4K-bit RAM.

4.2 Circuitries and Their Design

A block diagram of the BS chip is shown in Fig. 4.4. A 32-by-32 cell matrix is driven by 32 word drivers, which receive decoced X address signals from the X address decoder. One of the 32 rows in the cell array is selected by the word driver which has been designated by the applied X address. Then, stored data in the selected row are transferred to the 32 sense amplifiers. One of the 32 digit drivers designated by the applied Y address

drives one of the sense amplifiers to make its datum transferred further to the output amplifier. Thus, only one of the 1024 stored data is read out at the output terminal.

Writing is performed by write drivers which receive signals to be written into a cell from the control circuit, which also functions to make the output (D_{out}) at low potential level during writing.

A circuit diagram of the X address decoder and the word drivers of the BS chip is shown in Fig. 4.5. Fig. 4.6 shows a circuit diagram of the Y address decoder, digit drivers and sense amplifiers which include the write drivers. The X and Y address decoders and the word drivers consist of conventional current switches. Outputs from the 32 sense amplifiers are collector-dotted[44] in the amplifier shown on the right in Fig. 4.6, and are transferred to the output current switch.

Circuit design of a RAM LSI is difficult because:

(1) To reduce area for wiring, cells should share digit and word lines. Therefore, care must be taken not to cause malfunction of a RAM due to interaction of cells sharing the lines.

(2) Various circuitries such as storing cell, decoders, drivers and sense amplifiers are used. Therefore, their matching each other in functions, voltage levels, signal timings, and power allotment is important.

(3) Device parameters such as transistor current gains, cut-off frequencies, forward bias voltages, resistances, and capacitances unnecessarily vary according to uncontrollable changes of wafer processing conditions. For example, a value of a diffused resistor usually spreads within about $\pm$ 20 % deviation from the nominal value. Furthermore, because every device parameter has its inherent temperature coefficient, its value changes as its temperature changes. Some device parameter values vary correlatively each other. All the above device parameter varia-

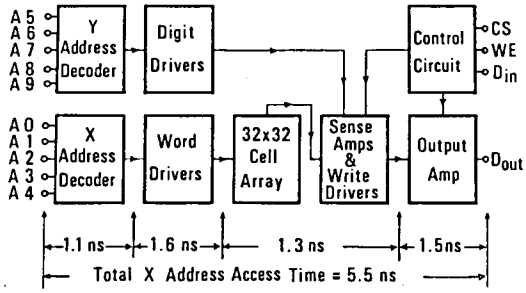


Fig. 4.4. Block diagram of the buffer storage (BS) chip.

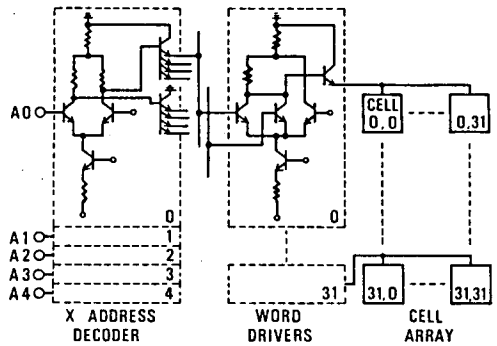


Fig. 4.5. Circuit diagram of the buffer storage (BS) chip: the X address decoder, word drivers, and cell array.

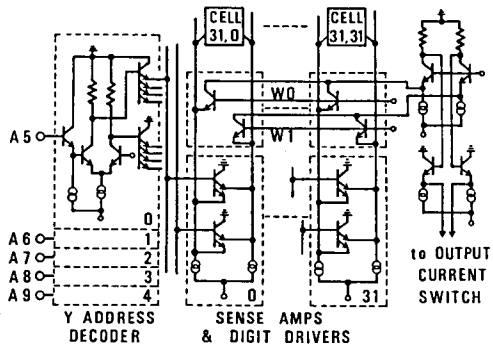


Fig. 4.6. Cirduit diagram of the buffer storage (BS) chip: the Y address decoder, digit drivers, and sense amplifiers.

tions must be taken into account in RAM LSI design.

(4) Precise evaluation of the switching characteristics of a RAM sometimes requires exact values of such parasitic capacitances as accompany aluminum metallizations and device isolation. Because their values depend on how they are layed out, it is sometimes necessary to make a trial layout of the circuit to correctly estimate the parasitic capacitances.

Practrical circuit design of a RAM is divided into two groups, DC design and AC (switching time) design. The latter is much more difficult than the former, because accurate and precise measurement of internal switching waveforms on a RAM chip is almost impossible. Integrated circuit elements are too small to be probed, and even if they are probed, parasitic capacitance and inductance accompanying the probe distort the internal waveforms. Therefore, RAM AC design can hardly be verified in direct ways.

There are three ways of RAM AC design, which will briefly be discussed in the following:

(1) Theoretical Analysis

At first, analytical equations expressing circuits' propagation delays in terms of device parameters (f_T, h_{FE}, $r_{bb'}$, C_{TC}, C_{TE}, etc.) and circuit parameters such as logic swings, current values and resistance values are derived. Then, optimum circuit parameters for best performance are obtained by manipulating the derived equations.

Because device characteristics inherently involve non-linear effects, it is difficult to derive a theoretical equation for a circuit propagation delay. Therefore, the equation cannot help being an approximate one which has limited extent of application dependent on the approximation conditions. There are few circuits whose analytical equations for propagation delays are

known. Propagation delays for some typical integrated logic circuits were analyzed in the literature (61).

It takes many hours to derive analytical equations for various circuits used for a RAM such as storing cells, decoders, drivers and sense amplifiers. Therefore, this approach is not commonly used for RAM LSI design, which usually requires a short time to compete in today's hard developmental race of LSIs.

This approach's good point is to give an insight into switching mechanism of a circuit. Investigation of an analytical equation allows one to quickly understand which parameters should be improved to speed up the RAM.

(2) Breadboarding (Hardware Simulation)

A circuit to be designed is constructed on a board using discrete transistors, resistors, and capacitors. The circuit is operated by applying necessary signals and power supplies. Its electrical characteristics are evaluated using measuring instruments such as an oscilloscope.

A circuit on a "breadboard" usually shows slower switching speeds than its integrated version on a silicon chip has, because large parasitic capacitance and inductance cannot help accompanying discrete components used, whose sizes are far larger than integrated elements. Breadboarding was often used in the early years of memory IC development when circuit simulation programs were not yet available.

(3) Computer Simulation

Today's outstanding development of circuit analysis programs allows one to simulate switching waveforms of a nonlinear circuit including about one thousand transistors[62]. Because its timing accuracy is about 10 % of actual values, computer simulation is quite acceptable and widely used for integrated circuit design. The BS chip design was not an exception.

When a CAD (Computer Aided Design) program is used, good understanding of device models and their limitations is necessary. Usually, a simulation model does not include second-order

effects.

RAM circuit design by a simulation program (a transient analysis program) will be explained in the following taking the BS chip design as an examle.

(1) Fundamental Design

In this stage of design, three basic policies should be investigated and defined. One is target specifications of the RAM. Its electrical characteristics, integration level, compatibility, package type, pin configuration, etc. are fixed considering system requirements as well as its feasibility by available IC technologies. The BS chip's major electrical specifications and compatibility are tabulated in Table 4.3.
Although the BS chip's performance specifications were determined by the system (M200H) requirements, its compatibility with 10K logic IC family, package type, and pin configuration were decided to coincide with the standard 10K ECL compatible 1K-bit RAM for the purpose of finding wider application area for the RAM.

The second is choice of circuit types. Which kind of a cell should be used, a variable impedance cell or a parallel diode cell ? (The variable impedance cell was chosen for the 4K-bit RAM described in Chapter III, while the parallel diode cell was used for the BS chip.) Which type of a sense circuitry should be better, wired-ORed emitter follower type or collector-dot type? These alternatives are evaluated to select one of them. In some cases, final decision cannot be made until computer simulation or trial fabrication and evaluation will discriminate candidate circuits in performance. An example is shown in Fig. 4.8, which compares collector-dot type sense circuitry with wired-ORed emitter follower type by computer simulation. The former gives a faster access time than the latter by 0.35 ns. Therefore, the former was adopted as a sense circuitry in the BS chip.

The third is process choice, which is important because not

only RAM performance but also its productivity, yield and cost are greatly dependent on the processes with which the RAM is produced. A series of processes which is already used for volume production of RAMs may give the shortest development time. But, it will probably produce a RAM with deteriorated cost/performance because progress of process technologies is so rapid at present that processes prevailing today may have a great possibility to become obsolete at the time when the development will be completed and volume production will start. Therefore, targeting of process technology improvement at the time of volume production is usually made at the beginning of the development.

After process choice is made, device parameters will then be estimated by either calculation or measurement of experimentally fabricated devices in order to be used for computer simulations.

Processes for the BS chip were derived by improving those applied to the older types of bipolar RAMs which have been in volume production since about 1976. Recently developed advanced technologies such as projection aligning, ion implantation, high-pressure oxidation, and dry etchig [63] were introduced to obtain better device parameters, the major ones of which are tabulated in Table 4.2.

Because the above three policy investigations are entangled each other, they cannot be performed independently. RAM performance specifications should be decided by paying careful attention to availability and feasibility of circuits and processes to be used.

(2) Functional Design

Once circuit types to be used are fixed, the next step is to construct a skelton of the whole RAM circuitry using selected circuits. At this stage of design, nominal node voltages of each circuit should be investigated and fixed so as to match neigh-

boring circuits' node voltages for realization of complete DC functions of the RAM as a whole. Starting point is cell functions. After cell functions are fully analyzed, voltage levels of word drivers, digit drivers, sense amplifiers, and write drivers are decided to be compatible with the cell functions. The voltage levels of X address decoder are then fixed to match word drivers' function. The X address decoder should also be compatible with input voltage levels (10K ECL). The same condition apply to Y address decoder, output amplifier, and control circuit, which have to be compatible with both the neighboring internal circuits and external input/output voltage levels.

Various reference voltages are used for internal circuits of the RAM. They also should be fixed. Although node voltages and voltage swings of each internal circuit are fixed, its current values (or its impedance level) are not yet fixed at this stage.

(3) AC Design

This stage includes evaluation and analysis of AC (switching) characteristics and optimum power allocation by use of computer simulation. Hitachi's program for circuit transient analysis was used for the BS chip AC design. The Ebers-Moll model of a bipolar transistor[64] shown in Fig. 4.7 was used. The simulation procedure is usually as follows:

(i) Current values should be assigned to each current source in the RAM. Assigned current values are arbitrary, at first. How to obtain optimum values will be described afterwards. Because voltage swings of each circuit have already been fixed in the functional design, load resistance values can be calculated simply by dividing a voltage swing by its correspondent assigned current value. All node voltages and current values (as a matter of course, resistor values) are fixed at this step.

(ii) The size of each transistor or diode is chosen to fit

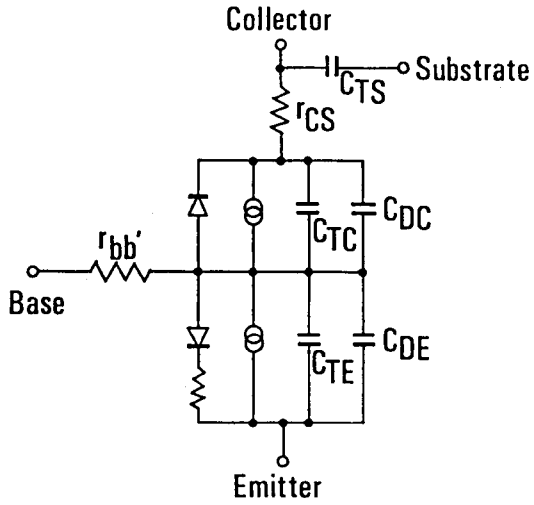


Fig. 4.7. The transistor model for simulation.

the current value which it conducts. Because a transistor or a diode of smaller size has smaller parasitic capacitances, it may be desirable for fast switching. However, if too small a transistor were chosen for the current value, undesirable nonlinear effects such as fall-off of transistor current gain (h_{FE}) or cut-off frequency (f_T) or else would deteriorate the circuit performance.

Once the size of each transistor or diode is fixed, all its device parameters such as V_{BE}, h_{FE}, f_T, $r_{bb'}$, C_{TS}, C_{TC}, C_{TE} can be calculated for its computer simulation model. The size of each resistor is also fixed to calculate its parasitic capacitance (isolation capacitance). Then, parasitic capacitances accompanying metallization layers are estimated, if necessary, by trial layout of the circuits.

(iii) Rewriting of all the circuitry in terms of device models for the simulation program is performed. Then, the program is run several times, and the results are analyzed.

As an example, simulated waveforms from X address input to the output (D_{out}) and from Y address input to the ouptput are shown in Figs. 4.8 and 4.9, respectively. These were obtained by use of the final designed values for the circuit elements.

Switching times of a circuit usually become faster if more power is allowed to the circuit, and vice versa. Because the allowable total power supply to a RAM is limited, how to allocate it to individual circuit in the RAM for best performance is an optimization problem to be solved. This optimization may be performed mechanically as follows if all the circuits related to the switching time to be analyzed can be simulated as a whole.

If a group of circuts are connected each other and transmit a signal successively to the neighboring circuit as shown in Fig. 4.10, the switching time from the input to the output is expressed as follows:

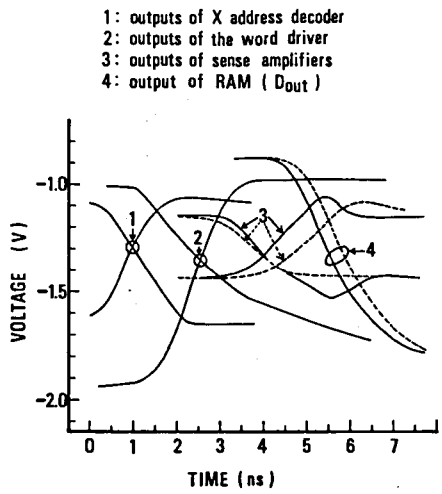


Fig. 4.8. Simulated waveforms in X address access. X address inputs are applied at the time of 0 ns. (Solid line: collector-dot type sense amplifiers. Dotted line: wired-ORed emitter follower type ones.)

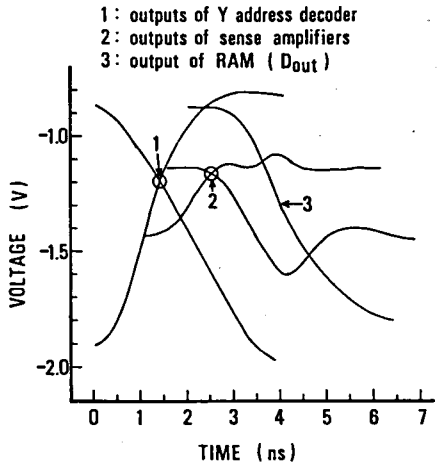


Fig. 4.9. Simulated waveforms in Y address access. Y address inputs are applied at the time of 0 ns.

$$t_{pd}=f(I_1, I_2, I_3, - - -, I_n) \tag{4.1}$$

where t_{pd} is the overall switching time of the circuit group, and I_1, I_2, I_3, - - -,I_n are supply current values of the individual circuits. The above equation means that t_{pd} is a function of I_1, I_2, I_3, - - -, and I_n.

If the X address access time of the BS chip is expressed using Eq. (4.1), I_1 will be the sum of currents flowing through the current switches of the X address decoder, I_2 will be the sum of currents flowing through the emitter followers of the X address decoder, I_3 will be the sum of currents of the word drivers' current switches, and I_n will be the current of the output amplifier.

The t_{pd} should be minimized under the following condition:

$$I_T(=\text{constant})=I_1+I_2+I_3+ - - - +I_n \tag{4.2}$$

Lagrange's unknown coefficient method gives the minimization condition, which follows.

$$\frac{\partial f}{\partial I_1} = \frac{\partial f}{\partial I_2} = \frac{\partial f}{\partial I_3} = - - - = \frac{\partial f}{\partial I_n} \tag{4.3}$$

The above condition of optimum power allocation can be derived by computer simulations. Its procedure will be shown in Fig. 4.11 and be explained in the following:

(i) $\frac{\partial f}{\partial I_1}$, $\frac{\partial f}{\partial I_2}$, $\frac{\partial f}{\partial I_3}$, - - -, $\frac{\partial f}{\partial I_n}$ are calculated repeating t_{pd} simulations by changing the current values in each circuit individually.

(ii) Graphs of $\frac{\partial f}{\partial I_1}$ versus I_1, $\frac{\partial f}{\partial I_2}$ versus I_2, $\frac{\partial f}{\partial I_3}$ versus I_3, - - -, $\frac{\partial f}{\partial I_n}$ versus I_n are plotted.

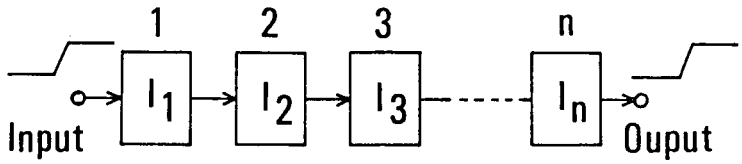


Fig. 4.10. A group of circuits transmitting a signal successively to the neighboring circuits.

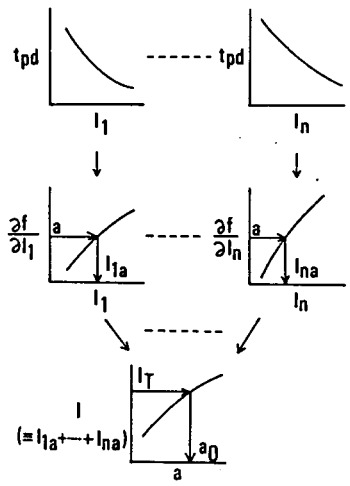


Fig. 4.11. Procedure to achieve optimum power allocation.

(iii) From the above graphs, I_{1a}, I_{2a}, I_{3a}, - - -, I_{na} are derived for the same value of a ($=\partial f/\partial I_1=\partial f/\partial I_2=\partial f/\partial I_3=$ - - - $=\partial f/\partial I_n$). These I_{1a}, I_{2a}, I_{3a}, - - -, I_{na} are then added to give I ($=I_{1a}+I_{2a}+I_{3a}+$ - - - $+I_{na}$). This Is are plotted against various values of a.

(iv) From the above plot of I vs. a, find a_0 at the point that $I=I_T$. Then, from the graphs of $\partial f/\partial I_i$ vs. I_i , find I_{ia_0} at $\partial f/\partial I_i=a_0$. This I_{ia_0} is the optimum allocated current value for the circuit i.

(4) Detailed DC design

After AC design is completed, all the nominal values of circuit elements except reference voltage generators are assigned. Next step is to investigate whether stable operation of the RAM is secured against device parameter variations due to uncontrollable change of wafer-processing conditions or due to their temperature coefficients. For example, a resistor value may vary from lot to lot, wafer to wafer, chip to chip, or even depending upon its location on the chip. Furthermore, it will change as its temperature changes.

All the above variations have to be considered when noise margins of a circuit are calculated. Each noise margin of all the circuits in the RAM must be secured against the worst case device parameter deviations from the nominal values. Node voltages and reference voltages are calibrated according to the worst case investigation. Then, details of the reference generators are fixed.

Detailed DC design may be performed by either computer simulations for DC analysis or manual calculations.

5. Processes and Devices

Photomicrographs of the IA and BS chips are shown in Figs. 4.12 and 4.13, respectively. Process and device parameters for both chips are summarized in Table 4.2. The primary fabrication process is oxide isolation with double layer metallization.

To achieve high speed, each parameter's contribution to the X address access time was analyzed. The relations between the access time and each device parameter were estimated by computer simulations. The results are plotted in Fig. 4.14. It shows that the largest dependence of the access time on percentage change of a device parameter occurs with transistor cut-off frequency f_T, and the next largest does with transistor base resistance $r_{bb'}$. Based on this analysis, special efforts were made to simultaneously obtain both high cut-off frequency and low base resistance. For this, shallow emitter junction of 0.4 μm and low base sheet resistivity of 400 $\Omega/\square$ were employed. Furthermore, three types of boron implantation were used. One for transistor bases, another for low value resistors, and the third for high value resistors in the memory cell circuits.

A half cell circuit and its cross section are shown in Fig. 4.15. The base of the transistor and a high value resistor R_{C1} are formed by different boron implantation processes. The Schottky barrier diode is formed using an aluminum metallization layer and a phosphorous-implanted N^+ layer. In addition, accurate control of forward voltage drop for the diode was achieved by varying the impurity densisity of the N^+ layer.

6. Performance of Both Chips

The major electrical characteristics provided by the new chips are summarized in Table 4.3. For the IA chip, the address access time from A to DO is 6.7 ns, and from CA to DO is 5.5 ns.

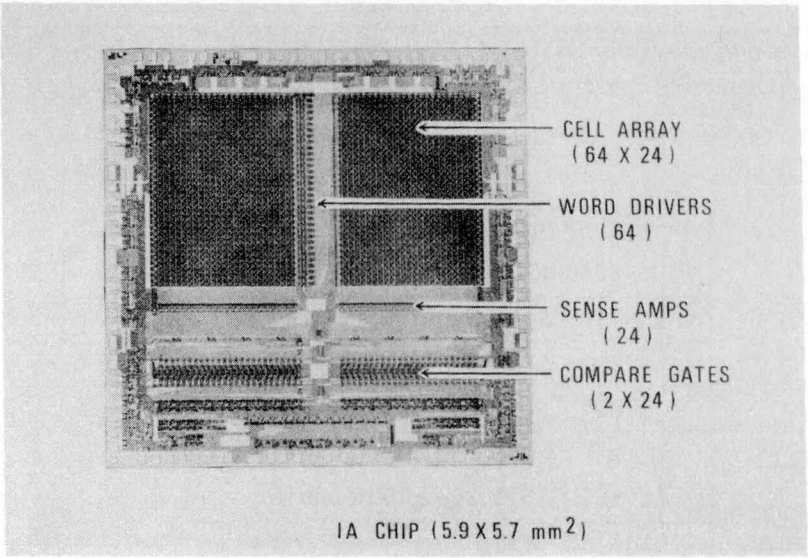


Fig. 4.12. Photomicrograph of the index array (IA) chip.

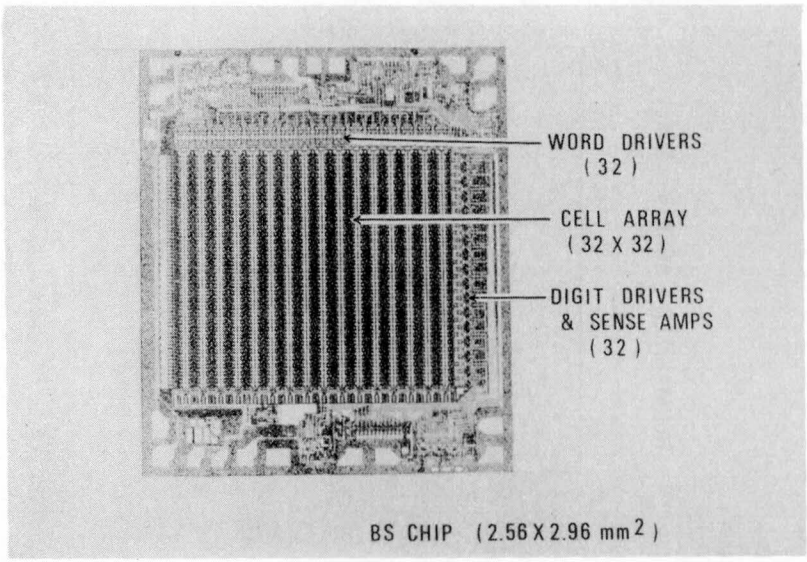


Fig. 4.13. Photomicrograph of the buffer storage (BS) chip.

TABLE 4.2

Process and Device Parameters

		IA	BS
LINE WIDTH PLUS SPACING	1ST	8 μm	9 μm
	2ND	14 μm	15 μm
EMITTER SIZE		3 μm X 3 μm	
CELL SIZE		3200 μm^2	2896 μm^2
CHIP SIZE		33.6 mm^2	7.6 mm^2
$C_{TS} = 0.13$ pf $C_{TC} = 0.041$ pf $C_{TE} = 0.034$ pf $f_T = 2.7$ GHz $r_{BB'} = 500$ ohms			
EMITTER DEPTH		0.4 μm	
SHEET RESISTIVITY OF IMPLANTED P-LAYERS		400, 700, 4K $\Omega/\square$	

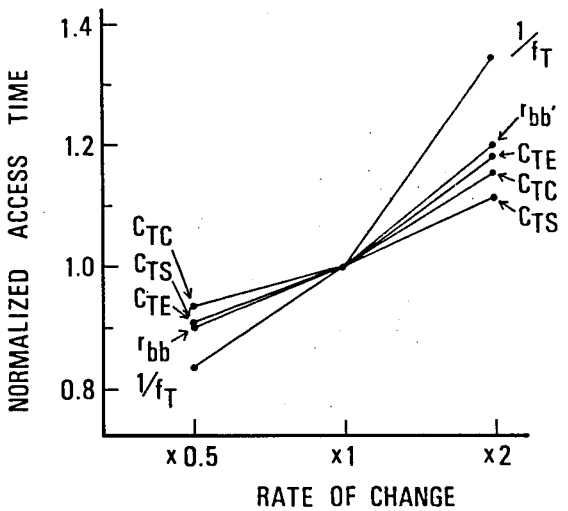


Fig. 4.14. An X address access time's dependence on each device parameter.

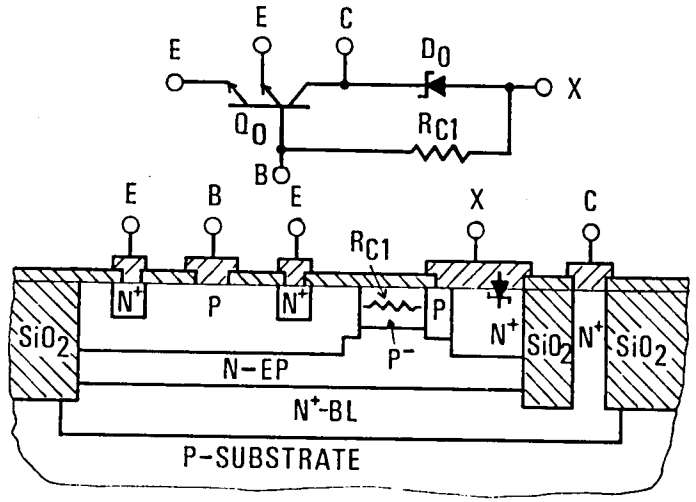


Fig. 4.15. Half cell circuit and its cross section.

TABLE 4.3

Major Electrical Characteristics of the Chips
(Values are typical ones.)

	UNIT	I A	B S
ADDRESS ACCESS TIME (A-DO)	ns	6.7	—
ADDRESS ACCESS TIME (CA-DO)	ns	5.5	—
COMPARE ACCESS TIME (CDI-CDO)	ns	3.1	—
X ADDRESS ACCESS TIME	ns	—	5.5
Y ADDRESS ACCESS TIME	ns	—	4.5
WRITE PULSE WIDTH	ns	6	3.5
POWER DISSIPATION	W	3.9	0.8
POWER SUPPLY VOLTAGE	V	− 4.5	− 5.2
LEVEL		ECL	10K ECL

The compare access time is 3.1 ns. With regard to the BS chip, the X address access time is 5.5 ns, and the Y address access time is 4.5 ns. All these values are typical ones.

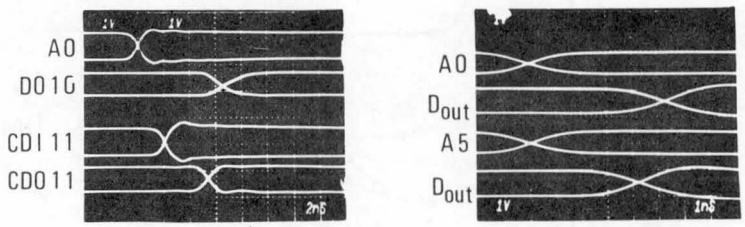
The power supply voltage for the IA chip was chosen to be -4.5 V in order to reduce power dissipation and to provide power supply compatibility with the logic LSIs(550 gates maximum) used in the M200H. However, the power supply voltage for the BS chip was made compatible with existing standard 10K compatible 1K-bit RAMs currently available.

The Y address access time of the BS chip was intentionally designed to be faster than that of the X address access time. This feature is very useful when X address signals are first determined and then Y address signals are sent to the chip. This usually occurs when the IA chip sends signals to the BS chip. Examples of the switching waveforms are shown in Fig. 4.16.

The write pulse width of the BS chip was optimized by controlling SBD's forward bias voltage V_F which decides how deeply the cell transistor saturates. This was done by varying impurity density of the N^+ layer beneath the Schottky contact. Three levels of impurity dosage were chosen to vary the V_F. The V_F's dependency on the dosage is tabulated in Table 4.4 and the write pulse width versus the address setup time of the BS chip for the three dosage levels is shown in Fig. 4.17. In the figure, the address setup time t_{WSA} is a time between the address signal transition and the leading edge of the write pulse as illustrated in Fig. 4.18.

The t_W represents the minimum write pulse width which is required to achieve writing in any cell in any condition. That is, writing into any cell can be performed with a longer pulse than t_W no matter what bit pattern the cell array is in, and irrespective of the sequence in which the cell is accessed.

The t_{NW} represents the not-write pulse width. Writing into any cell cannot be performed with a shorter pulse than t_{NW}. That is, a longer pulse than t_{NW}, which is induced on the write enable



(a) IA (b) BS

Fig. 4.16. Switching waveforms of (a) the index array (IA) chip and (b) the buffer storage (BS) chip.

TABLE 4.4

Forward Voltage's Dependence on Dosage Level
(Dosage level: A < B < C.)

Dosage	V_F(at I_D=0.6 mA)
A	0.80 V
B	0.75 V
C	0.64 V

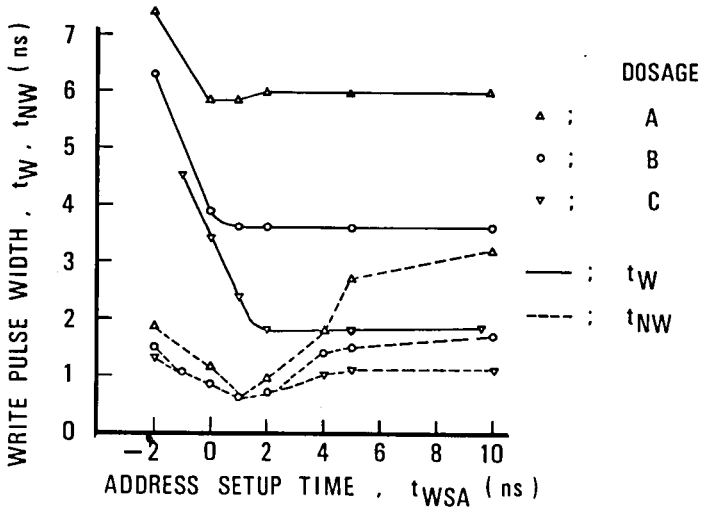


Fig. 4.17. BS chip's write pulse width versus address setup time. (Dosage lvel: A < B < C.)

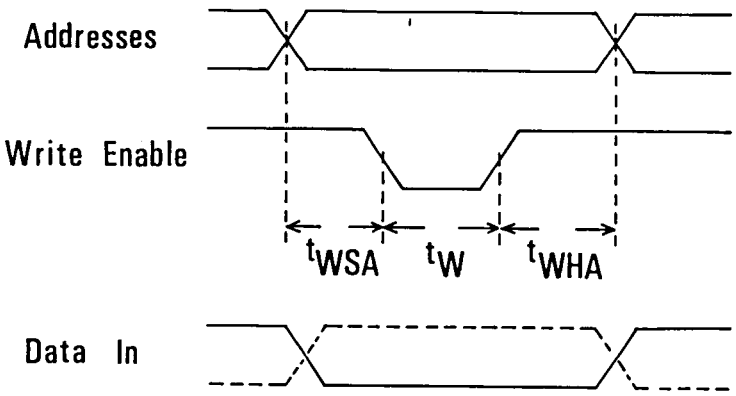


Fig. 4.18. Definition of write pulse width and address setup time. (t_W: write pulse width. t_{WSA}: address setup time. t_{WHA}: address hold time.)

terminal, may write data incorrectly into the RAM under some conditions.

To sum up, if writing is intended, the write pulse longer than t_W has to be applied to the RAM. But, if it is not intended, any noise signal whose pulse width is longer than t_{NW} should not be applied to the write enable terminal of the RAM to avoide malwriting. Because the level A gave too long write pulse widths to satisfy the BS chip's specification and the level C gave too short write pulse widths for the RAM to be immune from noises, the level B was chosen for the BS chip.

7. Accurate and Precise Measurements of the BS Chip Access Times

It is difficult to accurately measure the BS chip access times. This is because existing memory testers have too much address skew and jitter. Consequently, overall accuracy for access time measurement is estimated to be no better than $\pm$ 1 to 3 ns depending on the tester and how it is calibrated.

An effort was made to verify that the address access times of the BS chip are really under 7 ns, even for the worst case function mode. The configuration used for measurements and the results are shown in Figs. 4.19 and 4.20, respectively.

The skew for each address signal from a conventional memory tester was adjusted to within $\pm$ 300 ps using subnano-second gate delay IC flip-flops(F100131) and skew adjusters placed in front of the flip-flop clock inputs. Another purpose of the flip-flops was to apply signals with fast rise and fall times(=0.7ns/0.8V) to the memory under test(M.U.T.).

An output signal from the M.U.T. was detected by a hybrid IC comparator whose equivalent transition time including jig response was as fast as 0.6 ns[65]. A strobe pulse was produced by a variable delay circuit and the same clock signal as was applied to the flip-flops. The output from the hybrid comparator was

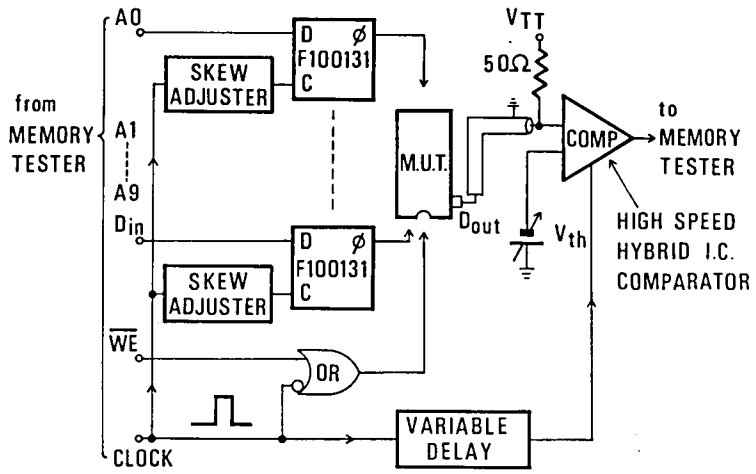


Fig. 4.19. Schematic for accurate address access time measurements of the BS chip.

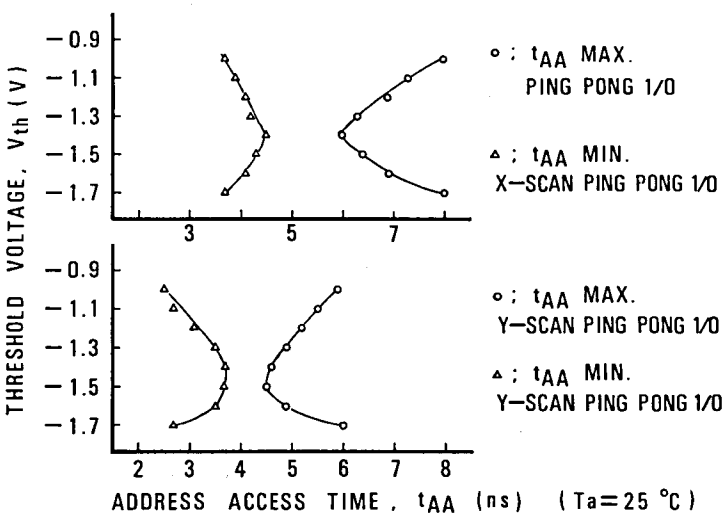


Fig. 4.20. Results of accurate address access time measurements of the BS chip.

sent to the memory tester, where a decision on pass/fail of the memory function was made.

Access time measurements were performed by manually changing the variable delay. This was carried out to find the threshold time under which the memory failed, and above which the memory functioned properly. The measured threshold time was an access time.

The fact that address skew was within ± 300 ps was verified as follows. First, a known and calibrated delay line, instead of a memory, was inserted between the socket pin for the address signal A0 and the socket pin for the RAM output(Dout). Then " the access(delay) time " from the A0 pin to the Dout pin was measured by changing the variable delay. At the same time, the memory tester tested whether or not the proper function pattern for A0 appeared at the Dout pin. This procedure was repeated for all address signals(pins). It was found that every signal transition for all the address signals fell within ± 300 ps of the calibrated delay.

Measurements were made for several samples. One of the results is shown in Fig. 4.20. To perform a ping-pong 1/0 pattern, the memory is initially set to the state in which all cells are in the "0" state. At the beginning of the test the first cell (which is called a reference cell) is set to the "1" state. All the remaining(N-1) field cells are now read to verify that they are in the "0" state. Between reading each "0" cell(field cell), the "1" cell(the reference cell) is read to verify that it is in the "1" state. This process continues until every cell has been set to the reference cell ("1" state), and this whole process is repeated after all the cells of the memory are initially set to the "1" state, and a refernce cell is set to the "0" state.

In the process of performing a ping-pong pattern, every combination of address changes in the memory occurs, as well as with a galloping 1/0 pattern. Consequently, this is considered the worst pattern for an address access time.

X-scan ping-pong means limited transitions between the reference bit and the field bits in a ping-pong 1/0 pattern. These transitions accompany any change in X address signals(A0-A4)(see Fig. 4.4). However, they do not accompany some changes in Y address signals(A5-A9). Y-scan ping-pong stands for the opposite situation.

The threshold voltages in the figure are the voltage levels which discriminate between the "1" and "0" levels.

The worst maximum address access time for the BS chip at T_a=25°C is about 6.0 ns, as seen in Fig. 4.20. Other experiments revealed that the temperature coefficient for the address access time is about 10 ps/°C. Therefore, a worst maximum access time of 7 ns can be guaranteed in the temperature range of 0°C-75°C.

Recent advent of a new high-performance memory tester with overall time measurement accuracy of $\pm$ 0.5 ns[66] has improved efficiency and reliability of access time measurement of ultra high-speed bipolar RAMs. Now, the BS chip's access times can easily be measured with a commercially available new tester without such an adapter as shown in Fig. 4.19. The BS chip's performance evaluation with a new high performance memory tester will be discussed in Chapter V, which also includes an overview on testing of ultra high-speed bipolar RAMs.

8. Conclusion

A pair of bipolar memory LSI chips for use in Hitachi's new mainframe computer, M200H, has been described. One is a new index array chip consisting of a 3072-bit random access memory and 470 logic gates. It has a typical access time of 6.7 ns and a typical power dissipation of 3.9 W. The chip is applied as the tranlation lookaside buffer and buffer storage control. This is a novel bipolar memory approach to mainframe computers.

The other chip is a standard 1K word by 1-bit 10K compati-

ble RAM. It has typical and maximum access times of 5.5 and 7 ns, respectively.

The primary fabrication process is oxide isolation with double layer metalliztion. Here, the minimum line width-plus-spacing is 8 μm. This pair of new chips should serve as a key to new bipolar memory concepts for future mainframe computers.

CHAPTER V

TESTING OF ULTRA HIGH SPEED BIPOLAR RAMS

1. Introduction

Most bipolar RAMs find their application in high-performance fields, such as buffer (or cache) storage in mainframe computers. Some ultra high-speed bipolar 1K- and 4K- bit RAMs with an access time of under 10 ns were recently developed to improve mainframe computers' performance[1,2,3]. Both go/no-go production testing and characterization/failure analysis of these RAMs require a high-performance memory tester and techniques to utilize it. If such a tester is not available, special adapter boards have to be attached to a conventional memory tester to improve its performance.

At first, testing requirements of high-speed bipolar RAMs will be described. Then, the old and new testing methods will be compared. At last, test results will be presented.

2. Testing Requirements

Table 1 tabulates the major electrical characteristics of a 1K-bit ECL RAM whose typical access time is as fast as 5.5 ns[2]. The RAM's access times vs. the logic threshold voltage are shown in Fig. 1. To evaluate an access time of a RAM, it is desirable that overall time measurement accuracy of a memory tester should be under $\pm$ 10% of the access time to be measured. The accuracy of $\pm$ 0.3 ns was achieved to obtain the curves shown in Fig. 1[4].

The RAM's write pulse widths vs. address setup time are shown in Fig. 2, which tells that the write pulse widths vary as

Table 1. Major electrical characteristics of the 1K-bit ECL RAM

X address access time	5.5 ns typ.
Y address access time	4.5 ns typ.
write pulse width	3.5 ns typ.
power dissipation	800 mw typ.
V_{EE}	-5.2 V
level	10K ECL
package	16 Pin Dual-In-Line
pin configuration	compatible with standard 1K-bit ECL RAMs

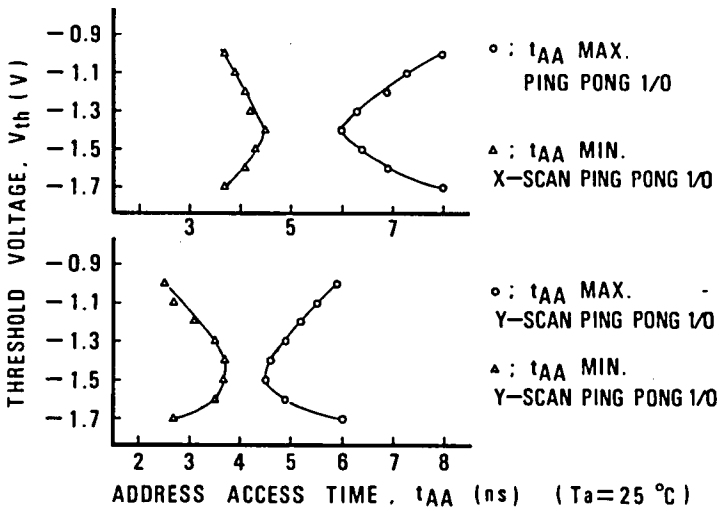


Fig. 1. The 1K-bit ECL RAM's access times vs. threshold voltages.

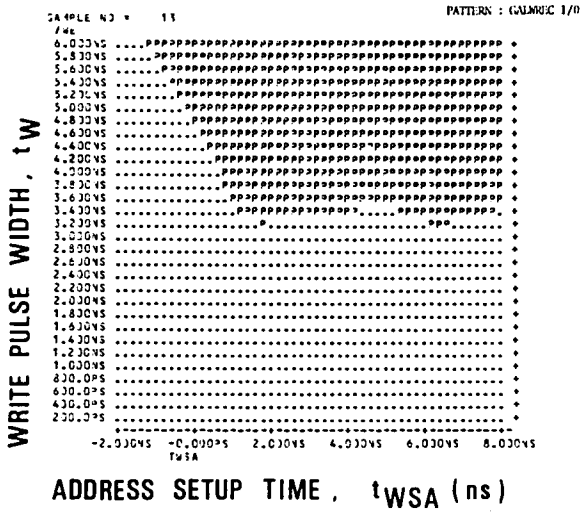


Fig. 2. (a) The 1K-bit RAM's write pulse width t_W vs. address setup time. (t_W: Writing into any cell can be performed with a longer pulse than t_W.)

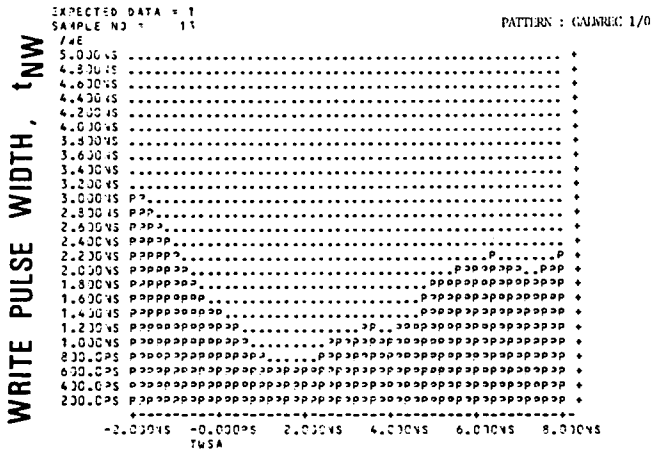


Fig. 2. (b) The 1K-bit RAM's write pulse width t_{NW} vs. address setup time. (t_{NW}: Writing into any cell cannot be performed with a shorter pulse than t_{NW}.)

the address setup time changes. To plot the figure, not only small jitter (under ± 0.1 ns is desirable) between the address and write enable signals, but also about 0 ns-wide write enable pulse was necessary (0 ns-wide pulse is a triangular pulse whose peak just reaches the logic threshold voltage. See Fig. 4.).

Desirable performance of a memory tester as well as realized performances of a new and an old memory testers are tabulated in Table 2. Not only overall time measurement accuracy of under ± 0.5 ns, but also its automatic calibration and other capabilities shown in the table are necessary. Testing requirements of ultra high-speed RAMs will be discussed item by item in the following.

(1) Drivers

Because the RAM are driven by high-speed ECL ICs such as F100K, rise/fall times of a driver output have to be comparable with those of F100K ICs(=0.7ns/V).

Skew of drivers greatly affects the accuracy of access time measurement. To guarantee a RAM's maximum address access time, a delay from the first address change to the last output change should be tested. On the contrary, the minimum address access time should be tested from the last address change to the first output change. This is illustrated in Fig. 3.

The minimum pulse width should be about 0 ns, and jitter between address and write enable signals should be less than ± 0.1 ns, as described before. Driver output waveforms of the new memory tester are shown in Fig. 4. One should note triangular-shaped pulse in the figure.

(2) Comparators

A compartor's propagation delay changes according to rise/fall times and the input overdrive. The smaller the above change is, the more accurate the comparator's time measurement accuracy is. The values shown in Table 2 were obtained by inputting signals with various rise/fall times and overdrives and measuring the signal delays by use of the comparator. Although tester

Table 2. Desirable and realized performances of memory testers

Item	Unit	Desirable performance	The new performance	The old performance
Drivers				
Rise/fall times	ns/V	0.5-0.7	0.7	2
Skew	ns	± 0.2	±0.2	± 1-2
Minimum pulse width	ns	*0	2	10
Comparator				
Time measurement accuracy	ns	± 0.3	±0.3	±0.5-1
Overall time measurement accuracy	ns	± 0.5	±0.5	±1.5-3
Automatic skew adjust		○	○	×
Pattern generator				
Pattern		arbitrary	arbitrary	arbitrary
Rate	MHz	above 20	20	10
Fail memory		○	○	○
Shmoo plot		○	○	○
Interrupt shmoo		○	○	×
Address skewing		○	○	×
Address scramble		○	○	×
Address mask		○	○	○
Bit/wafer map		○	○	○

*) 0 ns pulse is a triangular shaped one whose peak reaches the logic threshold level.

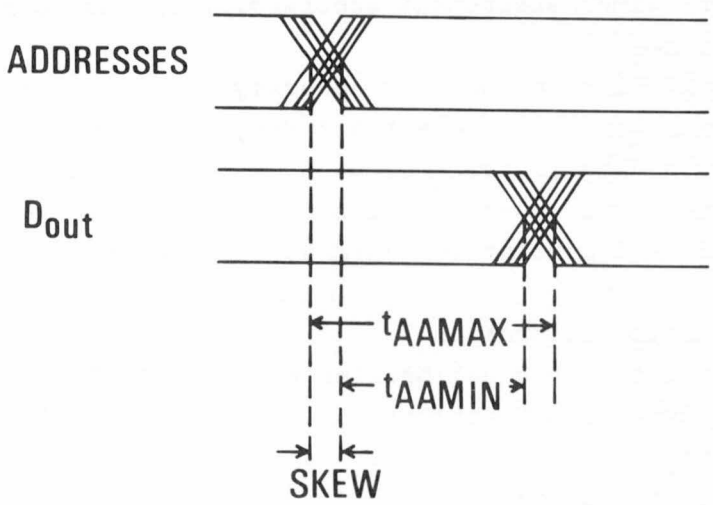


Fig. 3. Address skew's effect on address access time measurement.

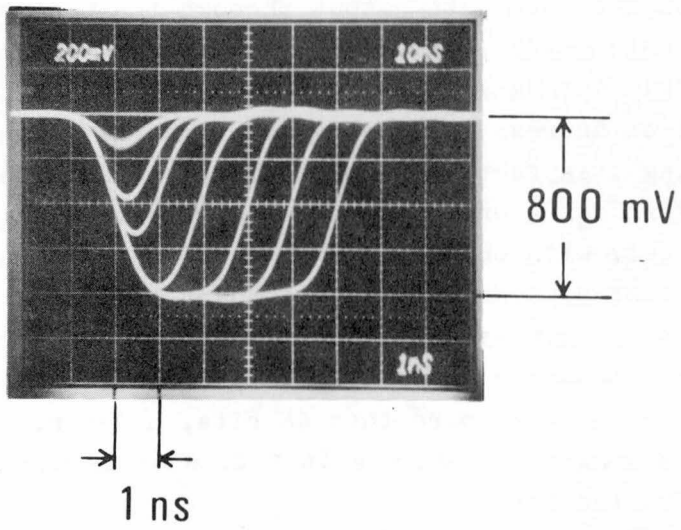


Fig. 4. Waveforms of a driver's output.

makers' data sheets usually do not include clear definition of comparators' time measurement accuracy, they should specify it for users' sake.

(3) Overall Time Measurement Accuracy

Overall time measurement accuracy shown in Table 2 was obtained by adding drivers' skew and comparator's time measurement accuracy. This specification is not found in testers' data sheets, but is important for characterization of high-performance testers.

(4) Automatic Calibration

The old tester's calibration requires tedious and lengthy adjustment by a highly skilled man. To reduce maintenance time and to increase reliability, automatic calibration scheme should be included in a tester.

(5) Pattern Generator

Compared to MOS RAMs, bipolar RAMs' performance is less sensitive to a data map of the cell matrix and sequence of access to a cell.Because PING PONG pattern scans every signal path from address inputs to a data output through the peripheral circuitries and cell matrix, it usually gives the maximum address access time for bipolar RAMs. A write pulse width of bipolar RAMs is dependent on address setup and hold times as shown in Fig. 2. Considering this fact, GALWREC pattern seems to be the worst-case pattern for a write pulse width, because it involves writing of every cell with transitions to and from every other cell.

Because bipolar RAMs have comparatively small integrated bits and their high-speed allows them to be tested at as fast cycles as a tester can operate, they are usually tested with N^2 patterns. A RAM with more than 4K bits, however, requires $N^{3/2}$ patterns to achieve as short a test time as is necessary for low-cost production test.

Fig. 5 shows a calculated functional test time versus a test cycle time when a RAM is driven four times with the pattern of PING PONG plus GALWREC. PING PONG and GALWREC are N^2 patterns

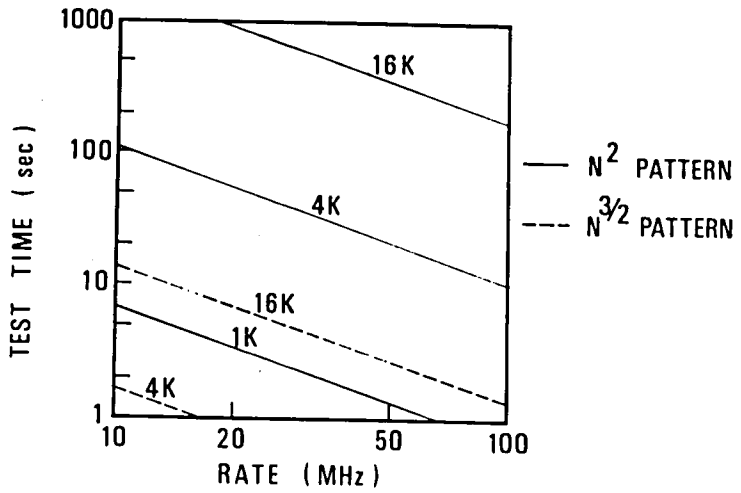


Fig. 5. Test time vs. pattern rate.

requiring ($4N^2+2N$) and ($12N^2-10N$) test cycles, respectively. Test times for $N^{3/2}$ patterns are also plotted in the figure assuming that a RAM is driven four times with DIAGONAL PING PONG ($4N^{3/2}+2N$) plus DIAGONAL GALWREC ($12N^{3/2}-22N$). From the figure, it is clear that adoption of $N^{3/2}$ patterns should be inevitable to test a RAM with more than 4K bits even if a tester's cycle time is improved to 100 MHz.

An ultra high-speed bipolar RAM may operate in a system at cycles of about 100 MHz. To evaluate a RAM's performance dependence on a cycle time of operation requires a memory tester with a pattern rate of above 100 MHz. Such a high-speed memory tester was not available in the past and was only recently reported to have been developed[5,6]. Fortunately, lack of tests at a cycle at which a bipolar RAM should operate practically in a system seems to have caused no field failure in the past, and to be going to do so in near future. But, for characterization and analysis of bipolar RAMs, designers want to do tests at practical cycles.

Once tests at practical cycles are neglected, a pattern rate of a test should be specified from the other point of view, "test time". The faster the pattern rate is, the smaller the functional test time is. Relation between a rate and a test time is also shown in Fig. 5.

(6) Software

For an engineer to master the usage of a tester within a short time, an English-like language is indispensable. A macro-assembler is also necessary to improve program efficiency. In production tests, it is often necessary to reduce a test time by writing a test program with assembly language.

(7) Failure Analysis Function

Analysis capabilities such as shown in Table 2 are necessary to increase efficiencies of failure analysis and device characterization.

(8) Device Fixtures

Device fixtures, which are often neglected, are important

to exchange signals with minimum reflections and distortions between leads of a device under test(DUT) and pin electronics cards of a tester. The importance is enhanced especially for ECL devices with sub-nanosecond rise/fall times. One of the most important solutions to high-fidelity pulse transmission is that impedance matching should be maintained all the way between the DUT and the pin electronics cards.

Impedance matching is also important when a test station is connected to a prober. Although only DC functional and parametric tests are usually made in probing of bipolar RAMs, reflection-free pulse transmission between pin electronics cards and probing needles is desirable.

Auto-handling of a DUT is necessary to reduce test cost. It will be difficult that impedance matching, good contact to the ground, and reduction of crosstalk between DUT leads are achieved by an auto-handler, considering physical and mechanical constraints imposed on it. But, development of such an auto-handler is expected.

3. Comparison of the New and Old Testing Methods

How the testing methods have been improved with the advent of the new tester is shown in Table 3. To perform accurate AC parametric and AC functional characterization with the old tester requires special adapter circuits which receive signals from the tester, send them to a DUT after skew-adjusting, and are able to generate a narrow write pulse. Fig. 6 shows the schematic of the adapter which has been used to obtain the data shown in Fig. 1. Usually, an adapter cannot help outputting fixed voltage levels to a DUT, disabling output voltage level programmability of the drivers. Furthermore, design, maintenance and calibration of an adapter board are time-consuming work.

Table 3. Comparison of the new and old testing methods

Item	New	Old
Detailed AC parametric & AC functional characterization	The new tester	The old tester with a special adapter (V_{IH} & V_{IL} are fixed)
Rough AC parametric, DC parametric & DC functional characterization	The new tester	The old tester.
Production test	The new tester	The old tester (Some items cannot be tested)

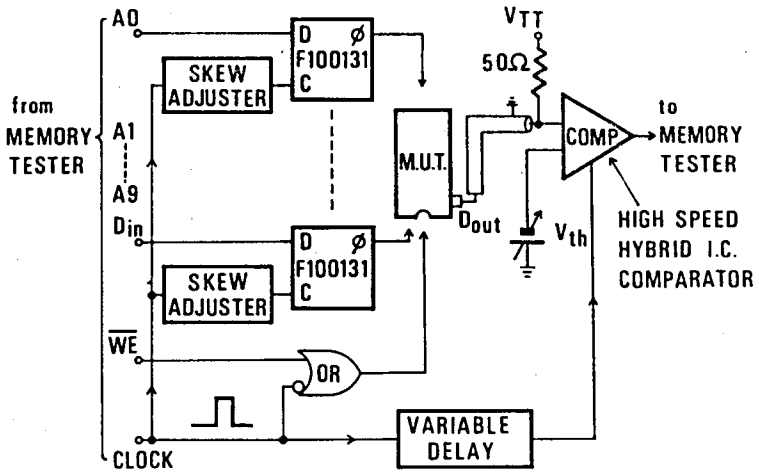


Fig. 6. Schematic of the adapter.

4. Test Results

(1) Access Time Measurements

Fig. 7 compares the 1K-bit RAM's access time dependence on the logic threshold voltage measured by the old tester without an adapter and the new tester. Delays of the strobe pulse of each tester are measured from the same reference time for both the maximum and minimum address access time measurements. Therefore, the difference between the measured maximum and minimum access times is given by the following equation:

$$t_{AAMAX}(\text{measured}) - t_{AAMIN}(\text{measured})$$

$$= t_{AAMAX}(\text{real}) - t_{AAMIN}(\text{real}) + t_{ACCURACY}$$

where $t_{ACCURACY}$ is an overall time measurement accuracy of an tester. (If it is expressed as $\pm$ 0.5 ns, $t_{ACCURACY}$=0.5X2=1.0 ns.) Fig. 7 shows that the above difference is reduced from 5.0 ns of the old tester to 1.8 ns of the new one at the threshold voltage of -1.3 V. The difference (3.2 ns) between the 5.0 and 1.8 ns means the difference in overall time measurement accuracy of both testers.

(2) Write Pulse Width Measurement

Fig. 2 is an example of write pulse width measurements performed by the new tester. The minute evaluation of t_{NW} vs. t_{WSA} in the figure was possible by the new tester's ability to generate 0 ns-wide pulse.

(3) Effect of Socket

A socket for a DUT is important for high speed ECL RAM testing. An output emitter follower driving a 50 Ω load produces the output current change of about 16 mA (=0.8 V/50Ω) within few nanosecond transition time. This current change induces noise voltages on the V_{CC} and A_0 leads. The A_0 lead is adjacent to the D_{out} lead (see Fig. 8 for the pin configuration of a

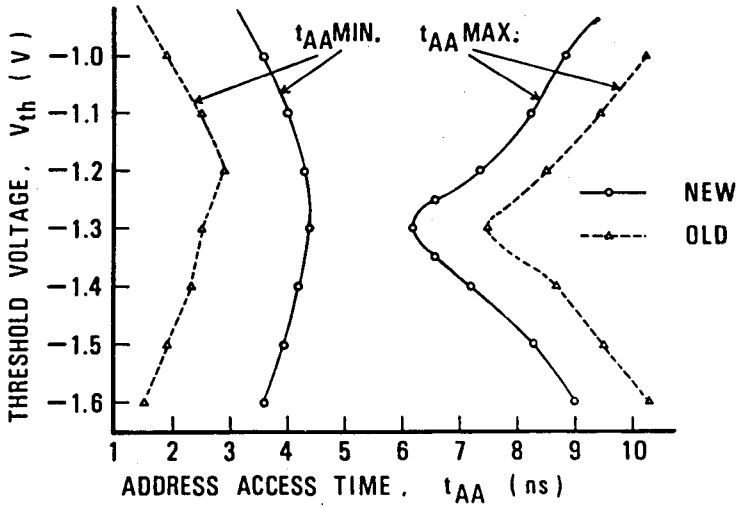


Fig. 7. The 1K-bit RAM's access times vs. threshold voltage measured by the new and old testers without an adapter.

standard ECL 1K-bit RAM). The noise on the V_{CC} lead results from the inductance of the socket lead, while the noise on the A_0 lead comes from the signal crosstalk between the D_{out} and A_0 socket's and DUT's leads. The noises are shown in Fig. 9. Noise generation mechanism is illustrated in Fig. 10.

To reduce the noises, lead sockets were adopted instead of a conventional IC socket. The V_{CC} lead socket was embedded in a printed circuit board to make as shortest contact to the broad ground plane as possible (see Fig. 11).

The noise voltage V_{NC} on the V_{CC} lead is given by the following equation:

$$V_{NC} = L\frac{\Delta i}{\Delta t} \tag{1}$$

where L is the inductance of the socket lead, Δi is the amount of current change on the V_{CC} lead, and Δt is the transition time for the current change. Because the RAM's output, whose waveforms are shown in Fig. 9, drives the load capacitance of 30 pF and the 50 Ω transmission line, Δi is divided into two terms, i.e. the two currents flowing into the 50 Ω load and capacitance.

$$\Delta i_R = \frac{\Delta V}{R} \tag{2}$$

$$\Delta i_C = C\frac{\Delta V}{\Delta t} \tag{3}$$

$$\Delta i = \Delta i_R + \Delta i_C \tag{4}$$

Because C=30 pF, R=50 Ω, and ΔV and Δt are estimated to be 0.8 V and 2.4 ns, respectively, from Fig. 9, Δi is,

$$\Delta i = \Delta i_R + \Delta i_C = 16 + 10 = 26 \quad \text{(mA)} \tag{5}$$

The above value, 12 nH (measured value) for L, and 2.4 ns for Δt are given into Eq. (1) to calculate the V_{NC}.

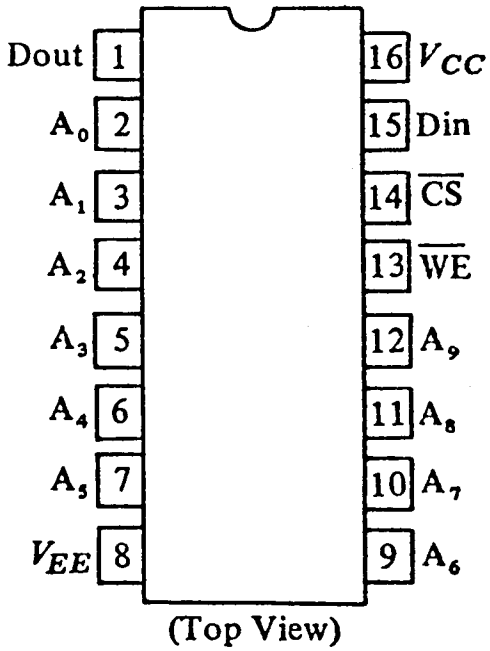
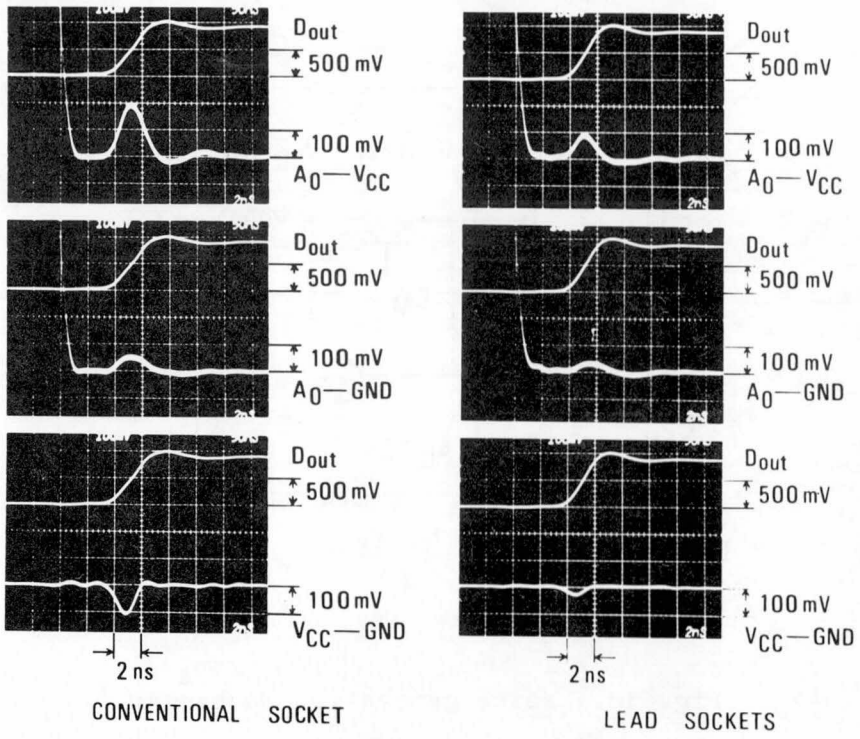


Fig. 8. Pin configuration of a standard ECL 1K-bit RAM.



(a) (b)

Fig. 9. Noises caused by output current switching. (a) Conventional socket. (b) Lead sockets.

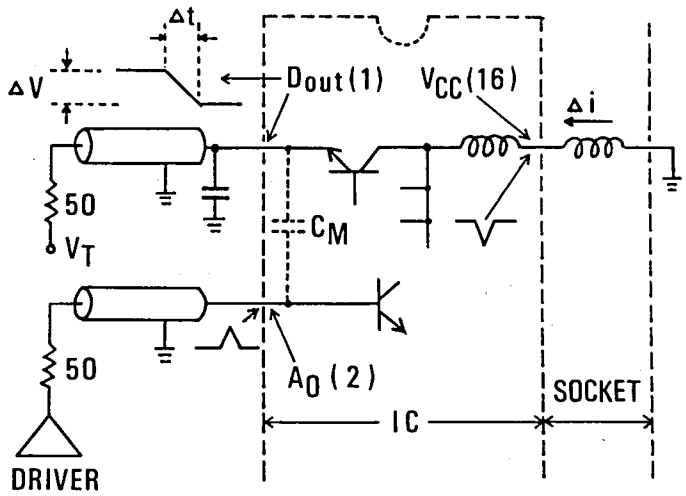
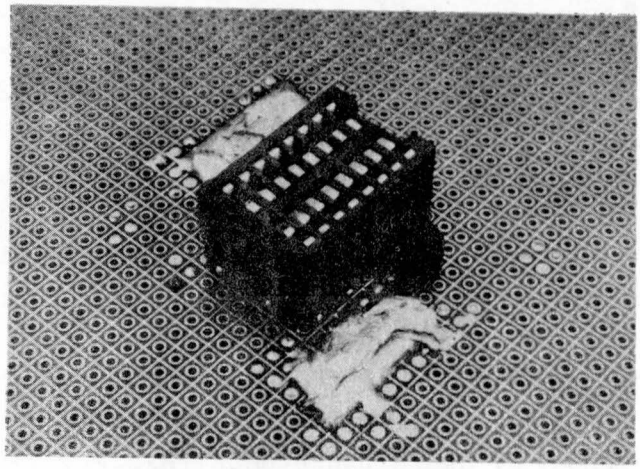
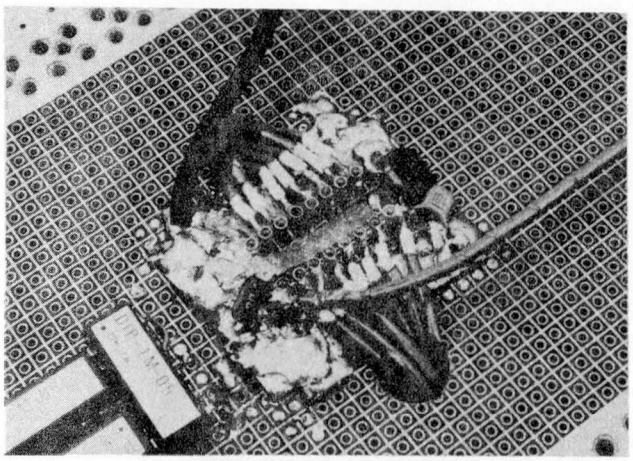


Fig. 10. Noise generation mechanism.



CONVENTIONAL SOCKET

Fig. 11. (a) Photograph of the conventional socket.



LEAD SOCKETS

Fig. 11. (b) Photograph of the lead sockets.

$$V_{NC} = 130 \quad (mV) \tag{6}$$

The above value is about the same as the measured V_{CC} noise, 110 mV for the conventional socket. Because the lead socket contacts with the ground plane near at its mouth, the inductance of the socket is decreased resulting in the reduced V_{NC} of 30 mV as shown in Fig. 9. One should note that there exists larger noise on the V_{CC} line on the chip because of the inductance of the IC's inner lead and bonding wire.

The noise on the A_0 lead results mainly from the crosstalk through stray capacitance between adjacent leads of the device. The noise caused by capacitance-coupling, V_{NA} is expressed as follows:

$$V_{NA} = z_o C_m \frac{\Delta V}{\Delta t} \tag{7}$$

where z_o is the characteristic impedance of the cable, C_m is the capacitance between the D_{out} and A_0 leads. The V_{NA} is estimated by giving 50 Ω for z_o, 1.8 pF(measured value) for C_m, 0.8 V for ΔV, and 2.4 ns for Δt.

$$V_{NA} = 30 \quad (mV) \tag{8}$$

The above value is about the same as the observed noise of 30 mV for the lead sockets. The value is increased to 50 mV for the conventional socket because of additional capacitance of the socket.

The noise voltage measured between the A_0 and V_{CC} leads (which is the sum of V_{NC} and V_{NA}) was reduced from about 200mV to about 90 mV by adoption of the lead sockets.

The drawback of lead sockets is that they do not allow easy insertion/withdrawal of a DUT.

5. Summary

With the advent of the newly developed high performance tester, efficiency and reliability of ultra high-speed bipolar RAM testing have been greatly improved. In future, however, it will be desirable that overall time measurement accuracy is further improved. Development of an IC socket with good high-frequency characteristics and easy insertion/withdral of DUTs, and an auto-handler dealing with high-speed ECL devices is also desirable.

CHAPTER VI

CONCLUSIONS AND SUGGESTIONS FOR FURTHER STUDY

Bipolar RAM integrated circuits have been studied throughout the thesis.

To increase integrated bits on a RAM chip without increasing (preferably, with decreasing) its access time and power dissipation is one of the most important and everlasting targets of IC memories. For that, memory circuitries with high speed and low power are necessary. Among other things, a cell circuit is the most important one for the RAM performance.

Cell circuit requirements were discussed and summarized as the following three items: stable operation at low standby current, ability to supply a large amount of readout current to digit lines, and occupying small silicon area. The former two are put together into a ratio of readout current to standby current (I_R/I_{ST} ratio). This ratio is the most important performance of a memory cell.

A novel cell circuit named a switched collector impedance cell which can have any high I_R/I_{ST} ratio owing to its circuit configuration was proposed. The cell was used to develop a 288-bit cell array and a 128-bit full decoding RAM, and its high performance was verified in them. The 128-bit RAM showed access times of 13 to 19 ns, standby and operating power of 0.9 and 3.1 mW/bit, respectively. A high I_R/I_{ST} ratio of 100 was achieved in the RAM by designing the read and standby current to be 2 mA and 20 uA, respectively.

In spite of its high-performance, a switched collector impedance (SCI) cell was not adopted for commercial bipolar RAM LSIs, because a later introduced parallel diode cell having simpler device structure and a moderate number of I_R/I_{ST} ratio

began to be in wide use. The added transistor of a SCI cell made its cell area larger, and the pinched epitaxial layer demanded preciser process control compared to a parallel diode cell.

However, a variation of a SCI memory cell was adopted to realize a very fast (address access time = 6 ns typ.) 4K-bit RAM afterwards when ion implantation which was a more controllable process to implement high value resistance than pinching of epitaxial layer had become available.

A parallel diode cell has most widely been used for commercially available 256 and 1024-bit RAMs. But, if it is used to develop a 4K-bit RAM which has the same fast access time and the same total power dissipation as a 1K-bit RAM, a difficulty arises. To realize a 4K-bit RAM with the same performance as that of a 1K-bit RAM requires the memory cell to have about eight times larger I_R/I_{ST} ratio than in a 1K-bit RAM. A parallel diode cell's I_R/I_{ST} ratio cannot be made so large because increased voltage drop across the cell load resistor caused by cell transistor base current flowing through it cannot be neglected when its I_R/I_{ST} ratio is increased.

To correct the above defect of a parallel diode cell, a new memory cell was proposed and named a variable impedance cell. This improved version of a parallel diode cell is formed by addition of a pair of p-n-p transistors to a parallel diode cell.

Because the added p-n-p transistor bypasses the increased load resistor, a variable impedance cell can supply a larger amount of read current than a parallel diode cell even if the load resistor is increased more than four times larger than that of a 1K-bit RAM to achieve more than four times lower standby current than that of a 1K-bit RAM.

The added p-n-p transistor is integrated beneath the load resistor without increasing silicon area. Therefore, the area of a variable impedance cell is no larger than that of a parallel diode cell. Moreover, because only small valued current gain of the p-n-p transistor is enough for its purpose, its introduction

does not require any additional strict processing control.

The 4K-bit RAM by use of variable impedance cells, other sophisticated circuit techniques, and oxide isolation showed typical and worst-maximum address access times of 25 and 45 ns, respectively, and the total power dissipation of as low as 350 mW.

Bipolar RAMs' greatest advantage consists in its high speed. Their most important application is found in high-performance mainframe computers, where they are used in the storage control unit as well as in the buffer storage, and greatly affect the speed of processor execution.

A new pair of bipolar memory LSI chips was introduced for improving memory access cycles in Hitachi's newest mainframe computer, the M200H, which typically realizes the more than 8 million instructions per second performance. One is an index array (IA) chip consisting of a 3072-bit RAM and 470 logic gates on the same chip. It has a typical address access time of 6.7 ns and a typical power dissipation of 3.9 W. It is used in the translation lookaside buffer and in the buffer address array to speed up dynamic address translation and buffer storage control. The other chip is a standard 1024 words by one-bit RAM with a typical address access time of 5.5 ns and a typical power dissipation of 800 mW. It is used for the buffer storage in the M200H.

Design considerations leading to the development of the new pair were presented. Very fast access cycles required in the M200H made it necessary to eliminate off-chip propagation delays by integrating both the RAM and the logic gates on the same IA chip. Integration level for the 1K-bit RAM was decided also in order to achieve a fast access time. The other consideration concerning specification optimizatin for the pair was cost. It is desirable to reduce cost of LSIs producing them in large volumes. For this purpose, LSIs should be standard ones that can be used for a variety of applications. The IA chip had to be a customized LSI solely for in-house use because of performance

requirements. The BS chip (the 1K-bit RAM), however, was designed as a standard 1K-bit RAM compatible with the 10K logic family, and housed in a conventional 300 mil wide, 16 pin dual-in-line package.

The fast access time of the BS chip was achieved with a combination of circuit, device, and process technologies. Circuit selection and optimum power allocation for the RAM were performed by full use of a computer simulation program. General approach for optimum power allocation with a transient analysis program was proposed.

The primary fabrication process was oxide isolation with double layer metallization. The minimum line width-plus-spacing was 9 μm. To achieve high speed, the access time's dependence on device parameters was analyzed with the simulation program. Based on this analysis, a special effort was made to simultaneously obtain both high cut-off frequency and low base resistance of transistors. To achieve fast writing, Schottky barrier diodes were introduced into the BS chip's cell circuit. And, their forward bias voltage was controlled to obtain optimum writing performance.

Basically, the same circuit and process technologies were applied to the IA chip.

To accurately evaluate such a high-speed RAM as the BS chip requires a high-performance memory tester and testing techniques to utilize it. Testing requirements of a high-speed RAM were analyzed. Based on the analysis, the BS chip's performance was evaluated with the accuracy of within ±300 ps.

In future, bipolar memories will continue to develop in integration level and performance considering the importance of their roles played in computers. The new concepts discussed in this thesis will serve to the future development of bipolar RAMs. Some 4K-bit ECL RAMs with typical access times of around 10 ns are already being developed using variable impedance cells in combination with advanced lithography and processes.

It is a matter of common knowledge that development of customized high-performance LSIs or VLSIs is the most important factor for future computing and communicating systems. Therefore, it is no doubt that custom LSIs including both memories and logic gates will find wider application in near future. And, technologies and tools to design and fabiricate such LSIs will be developed with great efforts.

APPENDIX I

CONFIGURATION AND FUNCTIONS OF A TYPICAL BIPOLAR RAM

1. Introduction

This appendix will describe how a typical bipolar RAM IC will function as "a black box", taking an ECL compatible 1K-bit RAM as an example. Therefore, little explanation regarding the internal circuits of the RAM will be made.

Most bipolar RAMs are designed, fabricated and sold to satisfy various users' needs. For that purpose, a RAM must be compatible with a standard one on electrical specifications, pin arrangement and package. Most users purchase standard type RAMs from multi-vendors because they are afraid of supply shortage and high cost due to depending on one specific vendor. The 1K-bit RAM used as an example is also a standard one. It was developed in 1976, and are now produced by Hitachi Ltd. Its commercial name is HM2110. Figures and tables which will be used afterwards to explain the configuration and functions of a typical 1K-bit RAM are borrowed from the Hitachi's memory data book.

2. Block Diagram and Functions

The block diagram of the 1K-bit RAM is shown in Fig. 1. The main portion of the diagram is the cell array consisting of 1024 storing circuits arranged as a 32 by 32 matrix. Adoption of matrix configuration for cells results from minimization of necessary word/digit driver circuits and word/digit lines to reduce element count and to achieve high performance. For example, a 1024-by-one cell matrix requires 1024 word or digit drivers,

while the 32-by-32 arrangement needs only a total of 64 drivers. Because a cell usually requires two word lines (upper and lower. see Figs. 2.5 and 2.6) and two digit lines, 1024-by-one arrangement requires a total of 2050(=1024X2+2) lines. On the contrary, 128(=32X2+32X2) lines are enough for the 32-by-32 array.

RAMs can be either bit-organized (n-words by one-bit) or word organized (n-words by m-bits. m may be 4, 8, 9 or else)[1]. Because a bit-organized memory has an advantage of requiring fewer input/output pins compared with a word-organized one, it is more popular than the latter.

A cell lying on both the selected word line (row) and the selected digit line (column) is to be accessed. The word line selection is made by the word drivers and the X address decoder, while the digit line selection is performed by the digit drivers and the Y address decoder. Anyone of the 1024 cells can be accessed by providing the necessary logic levels (the address of the cell to be accessed) to the address inputs from A_0 to A_9. The selected cell's stored information is read through the sense amplifiers to the output terminal designated by D_{out}.

Logic functions made by the input/output signals are tabulated in Table 1.

While writing is performed, a cell to be written into is selected in the same way as in reading. Then, the information to be written is provided by giving the required logic level to the D_{in} terminal and enabling the WE terminal (giving low logic level to the WE). It is transferred to the cell through the write drivers and the sense amplifiers. In Fig. 1, sense amplifiers include digit drivers which are shown separately in Figs. 3.13 and 4.4.

Chip select, CS, terminal is used to select the RAM (chip) as the term designates. When this signal is not activated, both reading and writing of the RAM cannot be performed, giving low logic level at the D_{out} terminal regardless of the accessed cell's stored information or logic levels given to the D_{in} and WE terminals. This CS's function enables the RAM's output to be

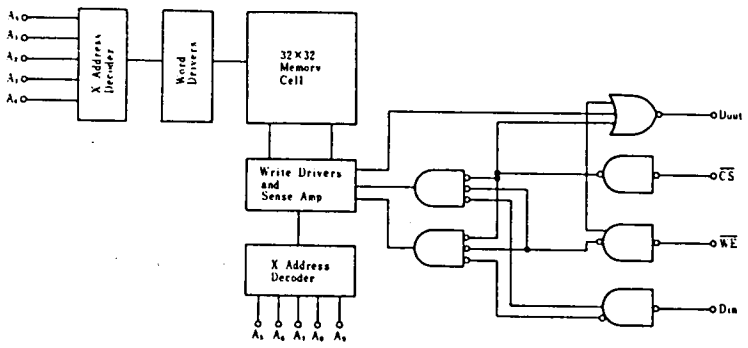


Fig. 1. Block diagram of a 1K-bit ECL RAM.

TABLE 1

Truth Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

× : irrelevant
* : Read out noninverted

wired-ORed with other RAM outputs.

3. Major Electrical Specification

Electrical specification is divided into two groups. One is the DC characteristics which specify the RAM's input/output voltage levels, input/output current, input/output leak current, power supply current and so on. Input/output voltage levels should be compatible with those of logic ICs which exchange signals with the RAM. Therefore, most RAMs are compatible with the standard logic IC families such as 10K ECL, F100K ECL and TTL. (ECL: Emitter Coupled Logic. TTL: Transistor Transistor Logic.) HM2110's DC characteristics are shown in Table 2.

Power supply current defines RAM's power dissipation which is one of the most important parameters governing packing density of the RAMs on printed circuit boards and cooling means of the memory boards. To achieve high packing density, RAMs are usually loaded on a printed circuit board as densely as possible.

AC characteristics are divided into two mode, read and write modes, as shown in Table 3. Fig. 2 shows loading condition, input pulse waveform at test, and definitions of various delays related to the AC characteristics. There are three versions in HM2110 according to difference in their maximum address access times, HM2110, -1, and -2.

The address access time, t_{AA}, is a delay time from application of address input signals to appearance of the accessed information at the D_{out} terminal. The address access time varies according to not only its power supply voltage and junction temperature, but also accessed cell's location in the cell array and sequence of access. The variation due to the last two causes is called pattern sensitivity of an address access time. Ping Pong 1/0 pattern is estimated to give the maximum address access time to the most bipolar RAMs. (see Chap. IV, Sec. 7 and

TABLE 2

DC Characteristics

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min. (B)	typ.	max. (A)	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{INA}$ or V_{ILB}	0°C	−1000		−840	mV
			+25°C	−960		−810	
			+75°C	−900		−720	
	V_{OL}		0°C	−1870		−1665	
			+25°C	−1850		−1650	
			+75°C	−1830		−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{INB}$ or V_{ILA}	0°C	−1020			mV
			+25°C	−980			
			+75°C	−920			
	V_{OLC}		0°C			−1645	
			+25°C			−1630	
			+75°C			−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145		−840	mV
			+25°C	−1105		−810	
			+75°C	−1045		−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870		−1490	
			+25°C	−1850		−1475	
			+75°C	−1830		−1450	
Input Current	I_{IH}	$V_{IN} = V_{INA}$	0 to +75°C			220	μA
	I_{IL}	$\overline{CS}$ $V_{IN} = V_{ILB}$	0 to +75°C		0.5	170	
		Other			−50		
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	0≦ Ta <25°C	150	−100		mA
			Ta ≧25°C	125	90		

TABLE 3

AC Characteristics

●AC CHARACTERISTICS (V_{EE} = −5.2V ± 5%, Ta = 0 to +75°C, air flow exceeding 2m sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			HM2110-2			Unit
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	—	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			HM2110-2			Unit
			min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
Write Pulse Width	t_W	t_{WSA} = 8ns	25	—	—	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}	t_W = 25ns	8	—	—	8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	5	—	—	5	—	—	ns
Write Disable Time	t_{WD}		—	—	10	—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	10	—	—	10	ns

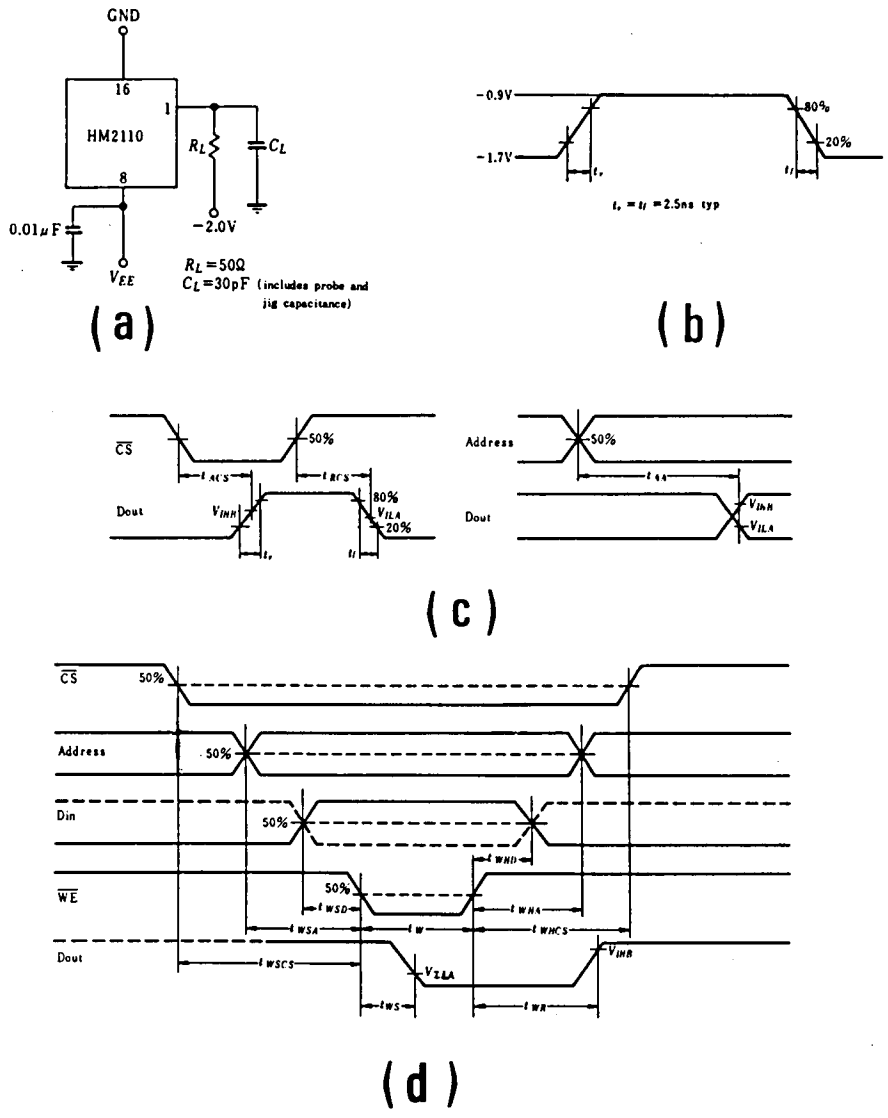


Fig. 2. Conditions for AC characteristics measurements. (a) Loading condition. (b) Input pulse waveform. (c) Definition of delays in read-mode. (d) Definition of delays in write-mode.

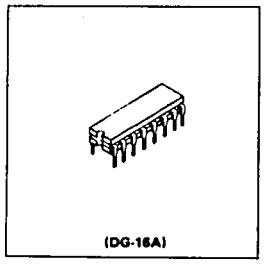
dix II.) The maximum value of address access times is important to users because their memory board design should afford a time, longer than the maximum value, between address change and triggering of a latch which detects the RAM's output.

Writing requires a complex timetable of the chip select (CS), addresses (A_i), data input (D_{in}), and write enable ($\overline{WE}$) signals shown in Fig. 2 (d). To write into an address without writing incorrectly into the different addresses, low state of the $\overline{WE}$ should remain well inside the duration of the aimed address with longer setup time (t_{WSA}) and hold time (t_{WHA}) than the specified minimum values. Moreover, the write enable pulse width (t_W) must be greater than the specified minimum value. To write an intended datum requires low state of the $\overline{WE}$ signal inside the duration of the intended state of D_{in} with enough data setup and hold times (t_{WSD} and t_{WHD}). The same condition applies to the timing between $\overline{CS}$ and $\overline{WE}$. Enough t_{WSCS} and t_{WHCS} have to be given for proper writing.

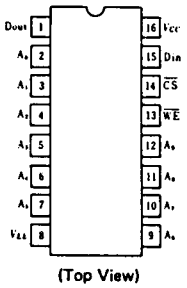
A write pulse width has pattern sensitivity as an address access time does. It also depends on various setup and hold times.

3. Package and Pin Arrangement

The RAM's package and pin arrangement are shown in Fig. 3. The package is a standard dual-in-line cerdip with 16 pins. The pin arrangement is also standard one for an 1K-bit ECL RAM.



(a)



(b)

Fig. 3. Package and pin arrangement. (a) 16-pin dual-in-line cerdip package. (b) Pin arrangement.

APPENDIX II

COMPARISON OF I_R/I_{ST} RATIOS OF SWITCHED COLLECTOR IMPEDANCE AND MULTI-EMITTER MEMORY CELLS

1. Introduction

This appendix will analyze and compare the I_R/I_{ST} ratios of switched collector impedance (SCI) and multi-emitter memory cells to show how high SCI cell's I_R/I_{ST} ratio is.

2. Analysis and Comparison of the I_R/I_{ST} Ratios

A SCI memory cell with a sensing circuit is shown in Fig.1. The voltage levels of the cell flip-flop are also shown in the figure. Fig. 2 shows a multi-emitter cell circuit.

The SCI cell is turned from its standby state to the selected one by raising the word line voltage V_X from V_{XL} to V_{XH}. Correspondingly, cell colector voltages V_{C0} and V_{C1} change their values from V_{CNH} and V_{CNL} to V_{CSH} and V_{CSL}, respectively. In this case, that the cell transistor Q_0 is on and Q_1 is off is assumed. That means that the cell collector voltage V_{C1} is higher than the other voltage V_{C0}. The voltages V_{W0} and V_{W1} are set at the midway voltage $V_{refcell}$ between V_{CSH} and V_{CSL} during reading in order to sense the cell voltages by currnt-switching action of between Q_0 and Q_4, and Q_1 and Q_5. Writing is performed by changing V_{W0} and/or V_{W1} from $V_{refcell}$.

The same symbols are used for the multi-emitter cell in Fig. 2. In this case, V_{XL} and V_{XH} are nearly equal to V_{CNH} and V_{CSH}, respectively because only a small amount of current (Q_0's base current) flows through R_{C1} causing only a small voltage

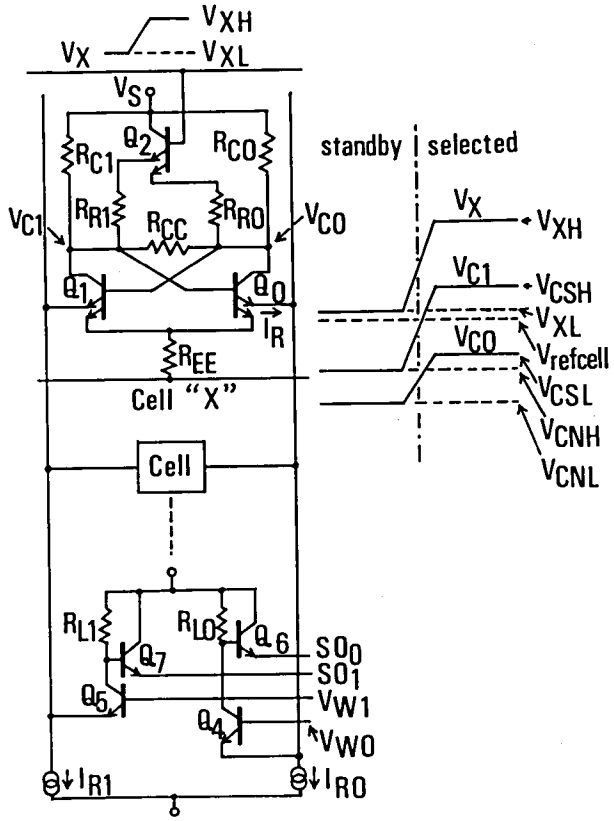


Fig. 1. Switched collector cell circuit with a sensing circuit and the related node voltages.

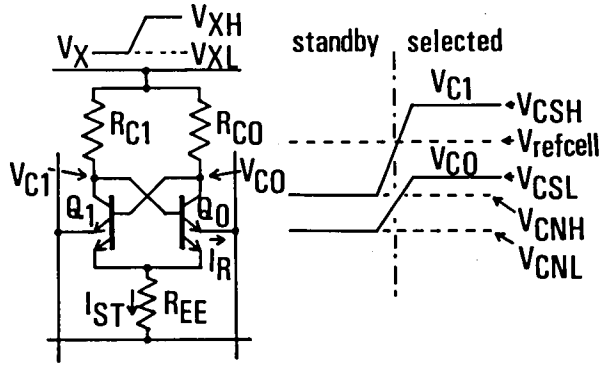


Fig. 2. Multi-emitter cell circuit with its related node voltages.

across it.

At standby, Q_2 is in off-state. Therefore, the standby current I_{ST} of the SCI cell is given as follows assuming that the current gain h_{FE} of Q_O is infinite and that $R_{CO}=R_{C1}$:

$$I_{ST}=\frac{V_{CNH}-V_{CNL}}{R_{CO}}*\frac{2R_{CO}+R_{CC}}{R_{CC}} \quad \text{(SCI)} \qquad (1)$$

At selected state, the read current I_{RO} ($=I_{R1}$) is given as follows:

$$I_{RO}=\frac{V_{CSH}-V_{CSL}}{R_{RO}}*\frac{R_{CC}+2R_{R1}}{R_{CC}} \quad \text{(SCI)} \qquad (2)$$

In the above equation, that $R_{CO}=R_{C1}\gg R_{RO}=R_{R1}$, that Q_O's $h_{FE}=\infty$, and that Q_2's two emitter voltages are equal to each other are assumed.

I_{ST} and I_{RO} of the multi-emitter cell are given as follows:

$$I_{ST}=\frac{V_{CNH}-V_{CNL}}{R_{CO}} \quad \text{(multi-emitter)} \qquad (3)$$

$$I_{RO}=\frac{V_{CSH}-V_{CSL}}{R_{CO}} \quad \text{(multi-emitter)} \qquad (4)$$

From Eq. (1) to (4), the ratios of the readout current to standby current are calculated:

$$\frac{I_{RO}}{I_{ST}}=\frac{V_{CSH}-V_{CSL}}{V_{CNH}-V_{CNL}}*\frac{R_{CO}}{R_{RO}}*\frac{R_{CC}+2R_{RO}}{2R_{CO}+R_{CC}} \quad \text{(SCI)} \qquad (5)$$

$$\frac{I_{RO}}{I_{ST}}=\frac{V_{CSH}-V_{CSL}}{V_{CNH}-V_{CNL}} \quad \text{(multi-emitter)} \qquad (6)$$

As seen from the above equations, the multi-emitter cell's I_R/I_{ST} ratio is given solely by the collector node voltages of the cell flipflop, and cannot be designed to be larger than 10,

because (V_{CSH}-V_{CSL}) cannot be larger than 800 mV to prevent the cell transistors from saturation, and because (V_{CNH}-V_{CNL}) cannot be set to be smaller than 80 mV for fear that the cell flipflop should toggle by noises at standby.

On the other hand, the SCI cell's I_R/I_{ST} ratio can be set at any value by manipulating the ratio of R_{CO} to R_{RO}. The ratio of (R_{CC}+2R_{RO}) to (2R_{CO}+R_{CC}) works to reduce the I_R/I_{ST} ratio as shown afterwards. But, because its value can be designed to be about 1/10, the SCI cell's I_R/I_{ST} ratio can be set to be larger an order of magnitude than the multi-emitter cell's by choosing 100 as the R_{CO}/R_{RO} ratio.

The value of R_{CC} cannot be chosen independently from that of R_{CO} because both values affect the value of V_{CNH} which must be set to be lower by about 0.4 V than the supply voltage to the cell, V_S. V_S is expressed as follows:

$$V_S=(V_S-V_{XH})+(V_{XH}-V_{CSH})+(V_{CSH}-V_{refcell})$$
$$+(V_{refcell}-V_{CNH})+V_{CNH} \qquad (7)$$

The first term of the right-hand side of the above equation stands for the voltage applied between the collector and base nodes of Q_2, and it should be greater than about -0.8 V to prevent Q_2 from saturation. The second term is nearly equal to Q_2's forward bias voltage between its base and emitter nodes when Q_2 is in on-state. It is about 0.8 V. The third term represents the noise margin for the current switching between Q_0 and Q_4, and Q_1 and Q_5 at selection. It is hardly designed to be smaller than 0.2 V. The fourth term stands for the noise margin that the cell transistor Q_0 or Q_1 is definitely in its off-state at its standby. and it is usually designed to be greater than 0.2 V. These values will be put into Eq. (7) to derive the following inequality:

$$V_S - V_{CNH} \geq 0.4 \quad (V) \tag{8}$$

The above inequation implies that V_S should be greater than V_{CNH}. This condition requires that R_{CC} should have some definite value because V_S would be equal to V_{CNH} if R_{CC} were infinite.

The lefthand term of Eq. (8) will be rewritten in terms of I_{ST}, R_{CC} and R_{CO} as follows:

$$V_S - V_{CNH} = \frac{I_{ST} * R_{CO}}{2 + R_{CC}/R_{CO}} \geq 0.4 \quad (V) \tag{9}$$

I_{ST} will be expressed using V_{CNH}, V_{CNL}, R_{CC} and R_{CO} as follows:

$$I_{ST} = \frac{(V_{CNH} - V_{CNL})}{R_{CO}} * \frac{2R_{CO} + R_{CC}}{R_{CC}} \tag{10}$$

Eqs. (9) and (10) will give the following condition for the ratio of R_{CC} to R_{CO}:

$$\frac{R_{CC}}{R_{CO}} \leq \frac{0.4}{(V_{CNH} - V_{CNL})} \tag{11}$$

The third factor $(R_{CC}+2R_{RO})/(2R_{CO}+R_{CC})$ of SCI's I_R/I_{ST} ratio in Eq. (6) will have the maximum value defined by Eq. (11):

$$\frac{R_{CC}+2R_{RO}}{2R_{CO}+R_{CC}} \doteqdot \frac{R_{CC}}{2R_{CO}+R_{CC}} \leq 1/\left(\frac{2*0.4}{(V_{CNH}-V_{CNL})}+1\right) \tag{12}$$

In the above inequation, $R_{RO} \ll R_{CC}$ is assumed. Because $(V_{CNH}-V_{CNL})$ is required to be greater than 0.1 V owing to cell flipflop stability at standby, the above inequation will be evaluated as follows:

$$\frac{R_{CC}+2R_{RO}}{2R_{CO}+R_{CC}} \leq 1/9 < 0.1 \tag{13}$$

Therefore, the $(R_{CC}+2R_{RO})/(2R_{CO}+R_{CC})$ factor will decrease SCI's I_R/I_{ST} ratio by an order.

In the 128-bit RAM with SCI cells described in Chap. II, the I_R/I_{ST} ratio as high as 100 has been achieved by designing that I_R=2 mA and I_{ST}=20 μA. In this design, $(V_{CSH}-V_{CSL})$=0.15 V, R_{CO}=110 KΩ, R_{RO}=150 Ω, and R_{CC}=17.7 KΩ. These values will be put into Eq. (5) to evaluate its righthand term:

$$\frac{(V_{CSH}-V_{CSL})}{(V_{CNH}-V_{CNL})}*\frac{R_{CO}}{R_{RO}}*\frac{(R_{CC}+2R_{RO})}{(2R_{CO}+R_{CC})}$$

$$=2.67*714*0.0756=144 \qquad (14)$$

That the above value is greater than the real value of I_R/I_{ST} (=100), is due to the assumption that Q_2's two emitter voltages at selection are equal, and that the h_{FE}s of Q_0 and Q_2 are infinite.

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