Power Packet Dispatching Based on Synchronization with Features on Safety

Yanzi Zhou

2015

Dedicated to my beloved family

Abstract

In the context of liberalized power market, the environment of power systems at present is more decentralized than that of conventional ones. Accordingly, the power distribution and power control become more complicated. For the purpose of introducing large-scale of renewable power sources into the power grid and optimizing power supply between power sources and consumers, a modernized power distribution network integrated with information and communications technology (ICT) is highly expected.

The main topics that are going to be discussed in this dissertation are simply introduced in Chapter 1, those are power packet dispatching system, clock synchronization, and safety of power packet dispatching. The power packet dispatching system is proposed to manage low direct current (DC) power sources, including renewable power sources, together with commercial power sources for adjusting to demands. In this system, the clock synchronization between a mixer and a router is required to achieve the exchange of information attached in a power packet. Furthermore, the concept of safety of power packet dispatching is proposed for protecting the information of power packets as well as keeping the loads safe regarding supplied power from power packets. As a potential approach to achieve the information safety and the power safety, modulation of power packets is proposed.

In the following Chapter 2, the operating principles of CPPLL are summarized in the beginning. According to the principles of CPPLL, a model of a digital clock synchronization method is derived, which is referred to as the primitive model. Next, applying a first-order control to the primitive model, we aim to achieve the clock synchronization between two clock signals: REF (reference clock signal) and NCO (output clock signal of a numerically-controlled oscillator). Moreover, the settling time is defined as the time needed to achieve the clock synchronization. Through experiments,

it is found that the setting time of the first-order controlled clock synchronization is around 10 reference clock cycles and further it is independent on the initial relationships between REF and NCO.

As a key factor of a clock synchronization method, the settling time is expected to be as short as possible. For the purpose of achieving clock synchronization in a shorter time, we are motivated to apply a second-order control to the primitive model in Chapter 3. Also, given the future application to the power packet dispatching system, the stability of the second-order controlled model is discussed. After that, the clock synchronization between two clock signals is achieved based on the second-order controlled model. In the end, embedding the model into a router, the power packet dispatching under autonomous clock synchronization is verified. The novelty lies on the application of the second-order controlled clock synchronization to the power packet dispatching system.

Chapter 4 investigates the power packet dispatching in a modified power packet dispatching system, where two mixers and one router are included. The attempt is to demonstrate the feasibility of system expansion based on autonomous clock synchronization. Power packet dispatching under different scenarios are discussed in experiments. Particularly, we focuses on the congestion of packets and the corresponding regulation. It is confirmed that power packets are dispatched as expected or as regulated. Therefore, one may conclude that based on autonomous clock synchronization achieved by second-order controlled model, it is feasible to expand the power packet dispatching system into a network system for power distribution in future.

The feature on safety of power packet dispatching is focused in Chapter 5, which can be considered from two aspects: protecting the information of packets from attackers (information safety) and keeping the loads safe regrading power (power safety). The novelty lies on proposing the concept of safety related to power packets, especially the concept of power safety. For the purpose of achieving information safety and power safety, we introduce a simple modulation of power packets before sending them. At first, we propose to modulate the preamble and the header of packets using the differential chaos shift keying (DCSK) scheme, a typical non-coherent chaos-based communication scheme, so that the information safety can be achieved. Then, we propose whole packet modulation aiming to achieve the information safety and the power safety simultaneously. In whole packet

modulation, pulse width modulation (PWM) is applied to the payload first for managing the amount of transferred power of packets. After that, the whole packet is further modulated using the DCSK scheme. By this means, the information of packets is protected and the spectrum of noise existing in the modulated packets is spread as well. The realization of the power packet modulation in real circuits is left for future research since the scope of this chapter is to present possible ways to achieve the safety of power packet dispatching under limited assumptions.

Chapter 6 summarizes the major points as well as the achievements. In addition, the future work is pointed out from two main aspects. One is to improve the performance of clock synchronization for power packet dispatching. The other is to improve the safety of power packet dispatching including the realization of the packet modulation. The potential obstacles are also mentioned.

Acknowledgments

I would like to extend my sincere thanks to all those patient souls who helped me accomplish my doctoral studies. It wouldn't have been possible for me to make it to the end without the support in various forms from many people around me. The three years in Kyoto University as a Ph.D. student is valuable to me in several ways. For me, it is a cyclic process of feeling confused, tough, desperate, promising, inspiring and joyful. In the meantime, I experienced many first times during these three years: I stayed in a foreign country for the first time, used English as the daily language, and lived alone outside of campus. The most important thing is that I learned a lot from Hikihara-laboratory and made a progress in doing research.

I would like to begin with expressing my deepest gratitude to Professor Takashi Hikihara, who is kind, wise, hard working, responsible, supportive and modest. He gave me the chance to join the Hikihara-laboratory as a Ph.D. student in Kyoto University, accepting my ignorance and my weakness. He led me through the difficulties in research activities by not only giving patient guidance but also encouraging me to trust myself and to trust him when I was depressed. Without his selfless concern and support, I would have given up in the very beginning. What's more, he also showed his concern to my families which I appreciated a lot. As an ancient Chinese saying, "He who teaches me for one day is my father for life.", I respect Professor Takashi Hikihara as my father. He has set a model of an excellent researcher for the young people. I am impressed by his sense of responsibility for both work and students. I would never have grown up so much without his selfless devotion to education, his wise guidance and his continuous encouragement. Therefore, I would like to extend my most sincere appreciation to Professor Takashi Hikihara.

Cordial gratitude is extended to my sub-supervisors, Professor Tomo-

hiko Mitani, Professor Ken Umeno and Professor Yasuo Okabe, who supported me with their valuable comments and constructive suggestions on my research every semester. This study went more smoothly under their supervision.

I would also like to thank Dr. Ryo Takahashi, Dr. Tsuguhiro Takuno, Mr. Keiji Tashiro, Mr. Takuya Kajiyama, Mr. Shinya Nawata, Mr. Naoaki Fujii, Mr. Daichi Nishihara and Mr. Shiu Mochiyama, who also did or are now doing researches about power packet dispatching system. I am very grateful to them for giving me help in the study. In particular, Mr. Keiji Tashiro helped me to be familiar with the system and Mr. Naoaki Fujii helped me install the experimental device and also gave me some good advice which inspired me a lot.

Thanks are also extended to all other members of Hikihara-laboratory. Ms. Yoshiko Deguchi gave me lots of help in my application for the Ph.D. course, and continued to help me in many stuffs during the whole Ph.D. period. I also want to give my thanks to Dr. Yoshihiko Susuki for his kind support. Ms. Madoka Kubota, my tutor in the beginning, is always hard working and responsible. She is more like a friend to me because she would point out my shortcomings and also give some advice to overcome them. I am also deeply impressed by Mr. Atsushi Yao because of his dedication to research. Mr. Hikari Hoshino always shows his smile to everyone, just like the sunshine which makes the lab more colorful. Mr. Yohei Nakamura is always kind to talk to me. I would like to express my special gratitude to the foreigner students in Hikihara-laboratory, who helped me adapt the life in Japan more easily. Ms. Eileen Lu was also a girl from China, and I learned a lot of things from her in the beginning, such as the culture difference and the lab atmosphere. Mr. Fredrik Raak, joined the lab at the same time as I did, showed his concern as a good friend and liked to share his experiences also, such as jujitsu. I also learned passion and independence from Ms. Rutvika Manohar. All of them helped me when I had difficulties in research and life. I had a great time with all of them and I will remember them forever.

I would also like to show my appreciation to the Global CEO program of Kyoto University (GCOE), the Monbukagakusho scholarship of Ministry of Education, Culture, Science and Technology of Japan (MEXT) for the financial support of three years. Furthermore, the Super Cluster Program

supported by JST and the Cross-ministerial Strategic Innovation Promotion Program supported by NEDO are aslo appreciated for their supported in this research.

My friends, old ones in China and new ones in Japan, made my Ph.D. life more colorful. Ms. Minghua Li was a graduate from Hikihara-laboratory, who helped me reduce the worries about life in Japan and explained the research environment before I came to Japan. I appreciated her help a lot because she gave me more confidence. I would also like to give special thanks to my dear friend Renee Wang, who was always there listening to my problems patiently and encouraged me.

Finally, special recognition goes out to my family for their support and encouragement. To my beloved husband, he is the person who believed me and encouraged me to take the challenge of becoming a Ph.D. student in the first place. He shared my joys and sorrows, as well as providing constant support during the entire process. He listened to all my complaint patiently and comforted me unconditionally. I would not have survived in a foreign country without his unconditional love, let alone completing this study. All the success I have achieved, I owe to my angel husband. To my dear parents and my parents-in-law, who supported my decision to pursue the Doctorate in Electrical Engineering. To my dear brothers, brother-in-law, and their wives, who took good care of my parents which allowed me to feel at ease studying abroad.

Sincerely yours,
Yanzi Zhou

List of Figures

Nomenclature

b_l:	transmitted information bit in DCSK
A, B, C, D (A', B', C', D'):	switches in the router
b'_l:	recovered information bit in DCSK
CLKIN, CLKIN1(2):	router clock signal: for packet1 (2)
DN:	negative phase difference
E[x_j], E[x_j^2]:	mean value of chaotic signal x_j, x_j^2
f_{REF}:	reference clock frequency
F_{s}:	sampling frequency of numerically-controlled oscillator
$fset, fset_{1(2)}$:	parameter to determine the mixer frequency: mixer1 (2)
f_{VCO}:	output clock frequency of voltage-controlled oscillator
H, H1(2):	header of packet: packet1 (2)
IN1(2):	router input port 1 (2)
$Inc^{(k)}$:	phase increment of numerically-controlled oscillator
j:	serial number of sample points in DCSK
k:	serial number of the reference clock cycle
l:	serial number of bits
m:	serial number of points of chaotic sample in each bit period
N_{b}:	bit number of packet signal in one packet
NCO:	output clock signal of numerically-controlled oscillator
OUT1(2):	router output port 1 (2)
packet1(2):	packet generated in mixer1 (2)
packet1s(2s):	signal generated in mixer1 (2) for clock synchronization
P_{modout}:	transfered power of a modulated packet
REF:	reference clock signal
r_j:	input signal of a DCSK demodulator
$R(x, x)$:	auto-correlation of chaotic signal
$R_{1(2)}$:	resistive load 1 (2)
s_j:	output signal of the DCSK modulator

T_{b}:	bit period of transmitted signal
T_{CLKIN}:	clock period of the router clock signal
t_k:	start time of the k-th reference clock cycle
T_{mixer}:	mixer clock period
T_{NCO}:	output clock period of numerically-controlled oscillator
T_{REF}:	reference clock period
T_{router}:	router clock period
T_{sam}:	sampling time of packet modulation in simulation
T_{sint}:	sampling interval in sampling theory
T_{supply}:	time duration of power packets transmission
T_{VCO}:	output clock period of voltage-controlled oscillator
T_{x}:	time interval between two sample points of chaotic signal
UP:	positive phase difference
VCO:	output clock signal of voltage-controlled oscillator
V_{ctrl}:	output voltage of loop filter in CPPLL
x_j:	chaotic signal in DCSK
x_{lm}:	m-th sample point of chaotic signal in the l-th bit period
z:	absolute voltage amplitude of packet
α:	partial spreading factor of modified DCSK
2β:	spreading factor of DCSK
Δf:	resolution of numerically-controlled oscillator
$\Delta(k)$:	phase difference between REF and NCO

Abbreviations

ADPLL:	all-digital phase-locked loop
AWGN:	additive white Gaussian noise
BER:	bit error rate
CDMA:	code division multiple access
CDR:	clock and data recovery
CP:	charge pump
CPPLL:	charge-pump phase locked loop
CSK:	chaos shift keying
DC:	direct current
DCSK:	differential chaos shift keying
FPGA:	field programmable gate array
ICT:	information and communication technology
LPF:	loop filter
NCO:	numerically-controlled oscillator
OEEN:	open electric energy network
PDM:	pulse density modulation
PFD:	phase frequency detector
PWM:	pulse width modulation
QoI:	quality of information
TDM:	time-division multiplexing
VCO:	voltage-controlled oscillator
VHDL:	VHSIC hardware description language
VHSIC:	very high speed integrated circuit

Contents

Chapter 1

Introduction

1.1 Power packet dispatching system

In recent years, the total energy consumption has been steadily increasing in the world. Of all energy consumption, the demand for electrical energy has been greatly increased because of the widespread use of electrical appliances, such as central air conditioner, oven, microwave, heater, etc. On the other hand, renewable energy sources such as solar energy, wind energy, hydroelectric energy, geothermal energy, and wave energy [1,2] are gaining more and more attention as environmental concerns and energy consumption continue to increase. In [3], statistical results of the growth and potential of renewable energies were presented. The statistics showed a generalized increase in all the fields of renewable energies. For example, the average annual growth rate of grid-connected solar panels, wind power and biodiesel were 60%, 28% and 25%, respectively. In particular, more and more renewable power sources are introduced in electricity generation and power delivery on demand. In this context, compared to the conventional power systems, in which power is mainly generated by fuel and coal in power generation companies, the environment of power systems nowadays has become more distributed. For instance, entities in different places generate solar electricity making use of their own photo voltaic cells and related devices. Consequently, the management of power flow becomes more complicated due to the coexistence of multiple entities, different quality criteria, different operation policies, and so on [4,5]. Also, it is readily apparent that the power generated from renewable power sources is fluctuating. Taking the solar power as an example, it is dependent on the weather and time, etc.

The instability of power makes power systems more complicated from the viewpoint of balance control of power supply and demand [6]. Therefore, in order to improve the efficiency, reliability, economics, and sustainability of the distribution of power, a modernized power distribution network is highly expected. Furthermore, in the modernized power distribution network, power is distributed based upon information exchange between power sources and loads.

The concept of power flow control based on information exchange can be traced back to as early as 1990s. In the context of liberalized power market, the concepts of energy packet and open electric energy network (OEEN) were proposed by Saitoh et al. in [4,5]. In their proposal, the electric energy produced by distributed power sources was packaged into energy packets, which were provided with information related to power producer and consumer. The power flow control system was referred to as a "power router". The basic configuration of small-size power router was presented. However, the power router and the OEEN in the proposal has not yet been realized physically due to the technology limitation at that time, such as limitation of information and communication technology (ICT). After that, researches related to energy packets have been continued. A digital approach to the power grid for a data center was presented in [7]. Moreover, quality of information (QoI) was evaluated using energy packet networks in [8] and a controlled-delivery power grid was studied in [9]. In particular, a power packet dispatching system was proposed for the purpose of managing low direct current (DC) power sources, including renewable power sources, together with commercial power sources for adjusting to demands [10–13]. The work in this dissertation is based on the power packet dispatching system.

In the power packet dispatching system, the management of power is supposed to be realized through bidirectional information exchange between power sources and loads. At present, however, only one-direction information exchange, i.e., information transmitted from the power sources side to the loads side, is considered. Figure 1.1 illustrates the fundamental configuration of a power packet dispatching system, which consists of DC power sources, a mixer, power line, a router, and loads. In the system, the power source is selected in the mixer at first so that power can be supplied to satisfy the demand of loads. Subsequently, power packets are produced in the mixer by switching on and off the selected power source based on the

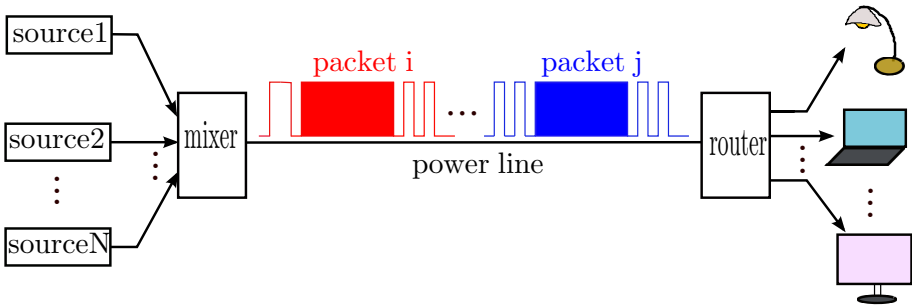


Figure 1.1: Fundamental configuration of a power packet dispatching system.

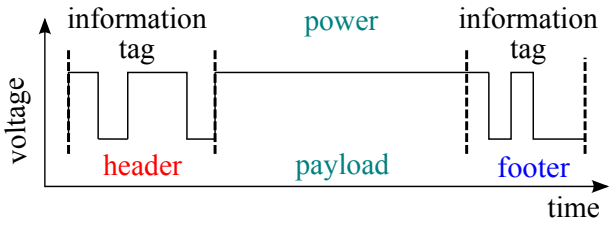


Figure 1.2: Basic composition of a power packet.

mixer clock frequency. The power packets are then transmitted from the mixer to the router through the power line in the time-division multiplexing (TDM) fashion. The router is a power control device through which power packets are dispatched according to the attached information of each packet. The basic composition of a power packet is presented in Fig. 1.2. As seen from the figure, a power packet is composed of a header, a payload, and a footer. The header and the footer are information tags which contain dispatching information of the packet, such as information on power sources and power destinations. The payload carries electric power to be transferred. In the router, the dispatching information of a packet is obtained by recognizing the packet signal in information tags. According to the attached information, the power packet is dispatched to the designated load. In this sense, the mixer, the router, and the power packet can be considered as the counterparts of the transmitter, the receiver, and the data packet in a communication system, respectively. In other words, the power packet dispatching system is analogous to the communication system.

1.2 Clock synchronization

From the above discussion, we learn that the power packet dispatching in a power packet dispatching system is determined by the attached information of packets. Thus the recognition of information tags in the receiver (router) is essential to correct packet dispatching. On the other hand, incorrect recognition of information tags may lead to two kinds of unwanted results. One is to discard the packet. The other is wrong dispatching of the packet. In order to analyze the impact of the results on the system, it is worth noting the difference between a power packet and a data packet which mainly depends on the physical meaning of the payload. The payload of a power packet carries electric power while the payload of a data packet carries data. As a consequence, in a communication system, if a data packet is discarded in the receiver, it can be reproduced because the data can be memorized in the transmitter. However, when a power packet is discarded in the router, it cannot be reproduced since the power cannot be memorized in the mixer, i.e., the power of the packet has been lost physically. Next, in the case of wrong packet dispatching, no damage will be caused to the communication system if a data packet is dispatched to a wrong destination. Whereas, in the power packet dispatching system, wrong dispatching of a power packet may result in damage to loads and further to the running system. For example, instead of the designated load, another load is supplied with the power of the packet. In such a case, the load may be damaged if the supplied power is higher than its rated power. Given the above reasons, the handshake between sources and loads in the power packet dispatching system is more rigid and must be optimized.

Figure 1.3 shows an illustrative setting of a power packet. As illustrated in the figure, the header includes a start signal, a source signal and an address signal. Besides, an end signal is included in the footer. Among all the signals, the start signal and the end signal indicate the beginning and the end of the packet, respectively. The source signal and the address signal contain information on origin of the power (power source) and destination of the power (load). On one hand, it has been mentioned in the previous section that power packets are produced in the mixer based on the mixer clock frequency. In more detail, the packet signal is generated at each rising edge of the mixer clock signal and the bit length of the packet signal is equal

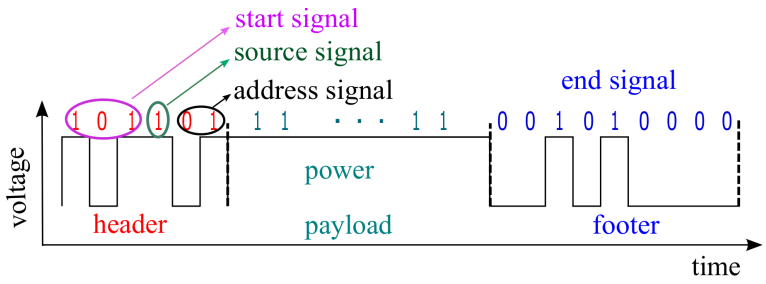


Figure 1.3: Illustrative setting of a power packet.

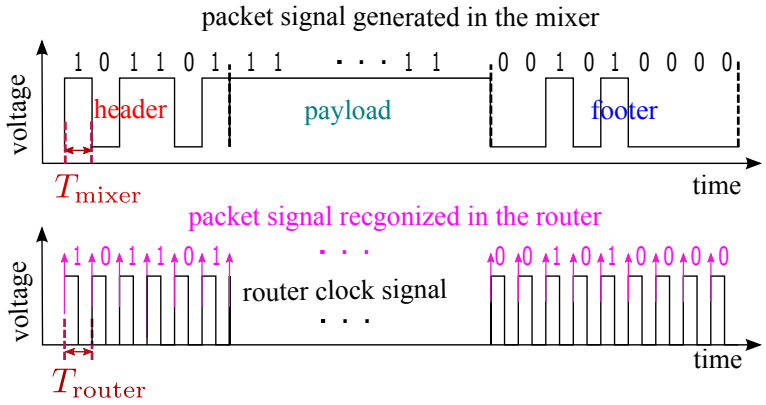


Figure 1.4: Recognition of packet signal in the router under clock synchronization ($T_{\text{mixer}} = T_{\text{router}}$).

to the mixer clock period (T_{mixer}) as shown in Fig. 1.4. On the other hand, in the router, the packet signal is read at every rising edge of the router clock signal to obtain the dispatching information. From Fig. 1.4, it is easily to understand that the router clock period (T_{router}) should be equal to T_{mixer} in the whole packet duration, for correct recognition of whole packet signal. We refer to $T_{\text{router}} = T_{\text{mixer}}$ as the clock synchronization between the mixer and the router in the power packet dispatching system. Additionally, Fig. 1.5 illustrates the recognition of packet signal in the case that the two clock signals are asynchronous, i.e., $T_{\text{router}} \neq T_{\text{mixer}}$. In such a case, the time difference between the corresponding rising edges of the two clock signals, namely the phase difference, is accumulated. Once the phase difference exceeds one mixer clock period, the following bit of packet signal may be recognized incorrectly. As can be seen from Fig. 1.5, the packet signal is still read at every rising edge of the router clock signal but error appears in signal recognition.

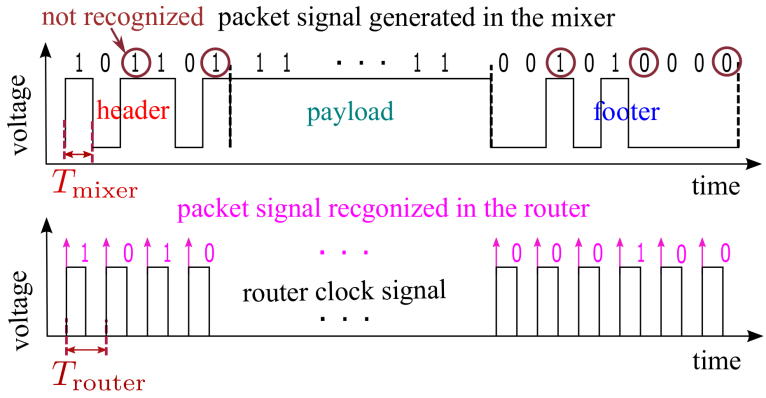


Figure 1.5: Recognition of packet signal in the router under clock asynchronism ($T_{\text{mixer}} \neq T_{\text{router}}$).

The clock synchronization in the power packet dispatching system was achieved using an external clock line in [14, 15]. An additional signal line, named as the clock line, is connected between the mixer and the router for achieving the clock synchronization while the power line is for transmitting power packets. Nevertheless, this approach suffers from some disadvantages. First of all, the additional line will lead to increase in the cost of the introduction of the power packet dispatching system undoubtedly. Secondly, the clock synchronization is weak for disturbances in the additional line. Moreover, the external clock line is not reasonable to establish a network system in future. Worse still, unexpected dispatching of packets to multiple destinations has been observed in experiments. As analyzed before, the unexpected dispatching of packets is due to incorrect recognition of the packet signal at the router side. Moreover, the reason for incorrect recognition, the failure in clock synchronization, is explained theoretically in [16].

Given the deficiency of the external clock line in achieving the clock synchronization, we are motivated to propose a clock synchronization method specified for power packet dispatching. It is worth mentioning that in future, the power packet dispatching system needs to be expanded from the standpoint of network design for power distribution. As a consequence, several mixers may be included in the system and it is possible that their clock signals are of different clock frequencies. This implies power packets may be produced based on different clock frequencies in the system. For this reason, the clock synchronization should be achieved for each power packet independently so that all packets generated from different mixers can be

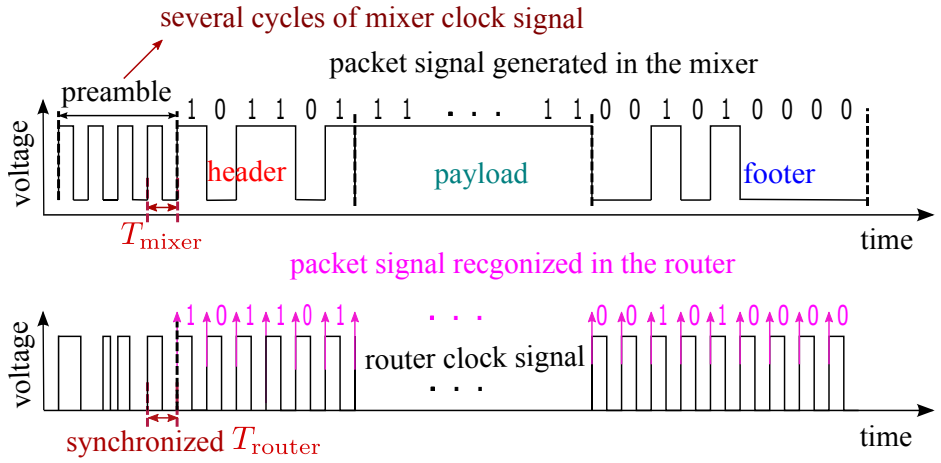


Figure 1.6: Proposal of achieving independent clock synchronization via preamble.

dispatched correctly. For the purpose of achieving the clock synchronization independently for each power packet, a preamble is added in front of each packet, as shown in Fig. 1.6. The preamble here is several cycles of the mixer clock signal and we aim to achieve the clock synchronization during the preamble in an automated fashion. The process of clock synchronization for one packet is executed in the router. It starts as soon as the preamble is received and ends at the end of the preamble. That is the clock synchronization between the mixer and the router has been achieved before the packet signal is read in the router. Thereafter, the synchronized router clock signal is locked until the end of the packet. By this way, all the signal in this packet duration can be read correctly. When the following packet is received in the router, the clock synchronization process will be restarted automatically.

As for the approach to achieve the clock synchronization, charge-pump phase locked loop (CPPLL) is widely adopted in analog systems [17–19]. However, if CPPLL is adopted to achieve clock synchronization for a wide range of reference frequencies, tuning parameters is required because of the analog charging and the filtering part in CPPLL. As a result, CPPLL is inappropriate to achieve the clock synchronization in the power packet dispatching system. Instead, digital clock synchronization methods which do not require parameter tuning contribute to develop a network system. In this dissertation, a model of a common digital clock synchronization method is derived, based on which the clock synchronization between the mixer and

the router is achieved.

1.3 Safety of power packet dispatching

A concept of safety of power packet dispatching is proposed which covers information safety and power safety. The information safety refers to protecting the information of power packets from attackers and the power safety is considered from the perspective of keeping the loads safe regarding supplied power of packets.

At first, for the system in Fig. 1.1, when an attacker existing between the mixer and the router receives a power packet, he or she may deduce the packet signal and accordingly obtain some useful information. For instance, by recognizing the address signal, the attacker may learn the time and the amount of power consumption of the corresponding load. In this sense, the safety of information is very weak. We can easily imagine that the attacker may even change the packet signal purposely, send the tampered packet to the router, and give rise to wrong packet dispatching. Such kind of cyber-attacks in power systems was studied in [20] and it was mentioned that contingencies could be created as a consequence. Here, the attacker may lead to damage to the running system by sending the tampered packet. Considering the consumers' privacy and the system stability, the information needs to be protected from attackers. Next, on the loads side the supplied power should be lower than their rated power. Therefore, rescaling of the transferred power of packets is desired.

In order to achieve the information safety and the power safety, we introduce simple modulations of power packets before sending them. In particular, partial packet modulation, i.e., modulating the preamble and the header of packets is proposed to protect the information of packets. Modulation scheme based on chaotic signal is one possibility for packet modulation and the differential chaos shift keying (DCSK) scheme is adopted in this dissertation. With respect to the power safety, it can be achieved by applying pulse width modulation (PWM) to the payload of packets. Furthermore, it is expected that the information safety and the power safety are achieved simultaneously. For this purpose, whole packet modulation is proposed. In whole packet modulation, two steps of modulation are included. At first, PWM is applied to the payload for adjusting the transferred power. Then,

the whole packet is further modulated using the DCSK scheme for achieving the information safety. Besides, using the whole packet modulation, the spectrum of the noise existing in the packet can be spread because of the broadband property of the chaotic signal used in the DCSK scheme.

1.4 Purpose and outline

In the context of liberalized power market, the environment of power systems at present is more decentralized than that of conventional ones. Accordingly, the power distribution and power control become more complicated. For the purpose of introducing large-scale of renewable power sources into the power grid and optimizing power supply between power sources and consumers, a modernized power distribution network integrated with information and communications technology (ICT) is highly expected.

The main topics that are going to be discussed in this dissertation were simply introduced in Chapter 1, those are power packet dispatching system, clock synchronization, and safety of power packet dispatching. The power packet dispatching system is proposed to manage low direct current (DC) power sources, including renewable power sources, together with commercial power sources for adjusting to demands. In this system, the clock synchronization between a mixer and a router is required to achieve the exchange of information attached in a power packet. Furthermore, the concept of safety of power packet dispatching is proposed for protecting the information of power packets as well as keeping the loads safe regarding supplied power from power packets. As a potential approach to achieve the information safety and the power safety, modulation of power packets is proposed.

In the following Chapter 2, the operating principles of CPPLL are summarized in the beginning. According to the principles of CPPLL, a model of a digital clock synchronization method is derived, which is referred to as the primitive model. Next, applying a first-order control to the primitive model, we aim to achieve the clock synchronization between two clock signals: REF (reference clock signal) and NCO (output clock signal of a numerically-controlled oscillator). Moreover, the settling time is defined as the time needed to achieve the clock synchronization. Through experiments, it is found that the setting time of the first-order controlled clock synchronization is around 10 reference clock cycles and further it is independent on

the initial relationships between REF and NCO.

As a key factor of a clock synchronization method, the settling time is expected to be as short as possible. For the purpose of achieving clock synchronization in a shorter time, we are motivated to apply a second-order control to the primitive model in Chapter 3. Also, given the future application to the power packet dispatching system, the stability of the second-order controlled model is discussed. After that, the clock synchronization between two clock signals is achieved based on the second-order controlled model. In the end, embedding the model into a router, the power packet dispatching under autonomous clock synchronization is verified. The novelty lies on the application of the second-order controlled clock synchronization to the power packet dispatching system.

Chapter 4 investigates the power packet dispatching in a modified power packet dispatching system, where two mixers and one router are included. The attempt is to demonstrate the feasibility of system expansion based on autonomous clock synchronization. Power packet dispatching under different scenarios are discussed in experiments. Particularly, we focuses on the congestion of packets and the corresponding regulation. It is confirmed that power packets are dispatched as expected or as regulated. Therefore, one may conclude that based on autonomous clock synchronization achieved by second-order controlled model, it is feasible to expand the power packet dispatching system into a network system for power distribution in future.

The feature on safety of power packet dispatching is focused in Chapter 5, which can be considered from two aspects: protecting the information of packets from attackers (information safety) and keeping the loads safe regrading power (power safety). The novelty lies on proposing the concept of safety related to power packets, especially the concept of power safety. For the purpose of achieving information safety and power safety, we introduce a simple modulation of power packets before sending them. At first, we propose to modulate the preamble and the header of packets using the differential chaos shift keying (DCSK) scheme, a typical non-coherent chaos-based communication scheme, so that the information safety can be achieved. Then, we propose whole packet modulation aiming to achieve the information safety and the power safety simultaneously. In whole packet modulation, pulse width modulation (PWM) is applied to the payload first for managing the amount of transferred power of packets. After that, the

whole packet is further modulated using the DCSK scheme. By this means, the information of packets is protected and the spectrum of noise existing in the modulated packets is spread as well. The realization of the power packet modulation in real circuits is left for future research since the scope of this chapter is to present possible ways to achieve the safety of power packet dispatching under limited assumptions.

Chapter 6 summarizes the major points as well as the achievements. In addition, the future work is pointed out from two main aspects. One is to improve the performance of clock synchronization for power packet dispatching. The other is to improve the safety of power packet dispatching including the realization of the packet modulation. The potential obstacles are also mentioned.

Chapter 2

First-Order Controlled Clock Synchronization

2.1 Prologue

The operating principles of charge pump phase locked loop (CPPLL) will give us the primary knowledge of the mechanism of achieving the clock synchronization between two clock signals. Referring to this mechanism, the model of a digital clock synchronization method will be derived. Then a first-order control will be applied to the derived model for achieving the clock synchronization between two clock signals. The process of the model derivation will be given in detail. Thereafter, the performance of the controlled model in achieving the clock synchronization will be evaluated by analyzing the simulation and experimental results. In the end of this chapter, a simple summary will be given.

2.2 Operating principles of CPPLL

As it was previously mentioned in Sect. 1.2, CPPLL is widely employed to achieve the clock synchronization in analog systems. A lot of research literatures studying CPPLL have been reported [21–30]. For example, in [21] various non-ideal phenomena in the charge pump circuits were discussed and a novel adaptive-bandwidth CPPLL with an improved passive filter was presented in [23]. Besides, a digital clock and data recovery (CDR) circuit was proposed in [24] and a second-order all-digital phase-locked loop

(ADPLL) was designed in [29], both were based on the analogy between a second-order CPPLL and an ADPLL.

The block diagram of CPPLL [31] is illustrated in Fig. 2.1, which consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LPF), and a voltage-controlled oscillator (VCO). Here, the signal REF stands for a reference clock signal whose frequency is fixed and the signal VCO represents the output clock signal of a voltage-controlled oscillator. Henceforth without specification, we use the phrase of "block VCO" and the letters of "VCO" to represent the voltage-controlled oscillator and its output clock signal, respectively. The operating principles of CPPLL can be simply described as follows: At first, the PFD compares the phases of the two input clock signals (REF and VCO) and outputs the phase difference between them (the time difference between corresponding rising edges of the two clock signals). The phase difference is represented by a pair of voltage pulses UP or DN [32]. Next, the charge pump converts the phase difference into an analog current, which is converted to a voltage (V_{ctrl}) later via the loop filter. The resulting V_{ctrl} is applied to drive the block VCO so that VCO is adjusted moving towards synchronization with REF, i.e., the frequency of VCO (f_{VCO}) is adjusted to be equal to the frequency of REF (f_{REF}) gradually.

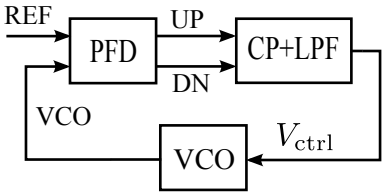


Figure 2.1: Block diagram of charge-pump phase locked loop (CPPLL).

To be more specific, in CPPLL, the synchronization between REF and VCO is equivalent to that the corresponding rising edges of them arrive at PFD simultaneously. The phenomena of two clock signals are asynchronous can be divided into two categories: the rising edge of REF leads and the rising edge of REF lags. In the case that the rising edge of REF arrives first, the voltage pulse UP is output by the PFD with the pulse width same as the phase difference. After that, positive V_{ctrl} is generated at the output of LPF which increases f_{VCO}. By this means, the phase difference between REF and VCO in the next reference clock cycle will be reduced. Otherwise,

if the rising edge of REF lags is the case, the voltage pulse DN is output by the PFD and negative V_{ctrl} is generated correspondingly. As a result, f_{VCO} decreases. Likewise, the phase difference will also be reduced in the next reference clock cycle. The adjusting process continues until REF and VCO are synchronized. In this manner, the negative feedback loop in CPPLL automatically adjusts the phase difference moving towards zero. In short, the primary mechanism of CPPLL in achieving the clock synchronization relies on the feedback control.

2.3 First-order controlled model

In the power packet dispatching system, it is required that the router clock signal is synchronous with the mixer clock signal as explained in Sect. 1.2. Generally speaking, analog clock synchronization methods can be used to achieve the clock synchronization in the system. However, in order to achieve clock synchronization for different levels of frequency, the parameters in analog circuits need to be tuned. The parameter tuning, unfortunately, will restrict the development of the system into a network system in future.This kind of issue does not exist in digital clock synchronization methods. Furthermore, digital clock synchronization methods can be realized easily in an field programmable gate array (FPGA) board. In experiments, the controllers of the mixer and the router are also implemented in FPGA boards in [13–15]. Therefore, digital clock synchronization methods are superior to analog ones regarding system compatibility, too.

Instead of adopting ADPLL, such as the ADPLL-based clock recovery circuit proposed in [33], we want to achieve the clock synchronization by applying our own control to a model of a digital clock synchronization method. The block diagram of a digital clock synchronization method is illustrated in Fig. 2.2, where $\Delta(k)$ denotes the phase difference between the two clock signals. Compared to CPPLL in Fig. 2.1, the VCO in CPPLL is replaced by a numerically-controlled oscillator (NCO) in the digital clock synchronization method. At the same time, both CP and LPF are deleted. Henceforth without specification, we use the phrase of "block NCO" and the letters of "NCO" to represent the numerically-controlled oscillator and its output clock signal, respectively.

A model of the above digital clock synchronization method can be de-

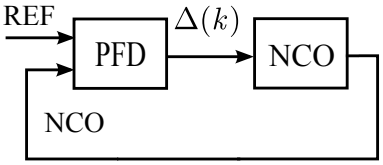


Figure 2.2: Block diagram of a digital clock synchronization method.

rived in accordance with the mechanism of CPPLL in achieving the clock synchronization. As shown in Fig. 2.3, before the clock synchronization is achieved, there exist four kinds of relationship between REF and NCO. Here, $k \in N^*$ indicates the serial number of the reference clock cycle, t_k represents the start time of the k-th reference clock cycle, and $\Delta(k)$ denotes the phase difference between the two clock signals. Besides, T_{REF} and $T_{\mathrm{NCO}}^{(k)}$ indicate the clock period of REF and the clock period of NCO at t_k, respectively. In Fig. 2.3(a), the rising edge of REF comes first at time t_k and continues leading at t_{k+1}. In Fig. 2.3(b), REF leads at t_k but becomes lagging at t_{k+1}. The case that NCO leads at t_k and keeps leading at t_{k+1} is shown in Fig. 2.3(c), while Fig. 2.3(d) presents the case that NCO leads at t_k but becomes lagging at t_{k+1}. We define $\Delta(k)$ is positive when the rising edge of REF comes first and $\Delta(k)$ is negative when REF lags. Under this definition, the signs of $\Delta(k)$ and $\Delta(k+1)$ in Fig. 2.3 can be summarized as follows,

(a) $\Delta(k) > 0$ and $\Delta(k+1) > 0$,

(b) $\Delta(k) > 0$ and $\Delta(k+1) < 0$,

(c) $\Delta(k) < 0$ and $\Delta(k+1) < 0$,

(d) $\Delta(k) < 0$ and $\Delta(k+1) > 0$.

Consequently, the model of the digital clock synchronization method can be derived as in Eq. (2.1), which is defined as the primitive model.

$$T_{\mathrm{NCO}}^{(k)} = T_{\mathrm{REF}} + \Delta(k+1) - \Delta(k), \;\; k = 1, 2, \cdots . \tag{2.1}$$

In the power packet dispatching system, it is only required that $T_{\mathrm{mixer}} = T_{\mathrm{router}}$ for correct power packet dispatching. Accordingly, in the next step, we apply some control to the primitive model for achieving $T_{\mathrm{NCO}} = T_{\mathrm{REF}}$. We refer to $T_{\mathrm{NCO}} = T_{\mathrm{REF}}$ as the achievement of clock synchronization using the digital clock synchronization method. From Eq. (2.1), it is readily apparent that the achievement of clock synchronization ($T_{\mathrm{NCO}}^{(k)} = T_{\mathrm{REF}}$) is equivalent to that the series of $\Delta(k)$ is convergent ($\Delta(k+1) = \Delta(k)$). As

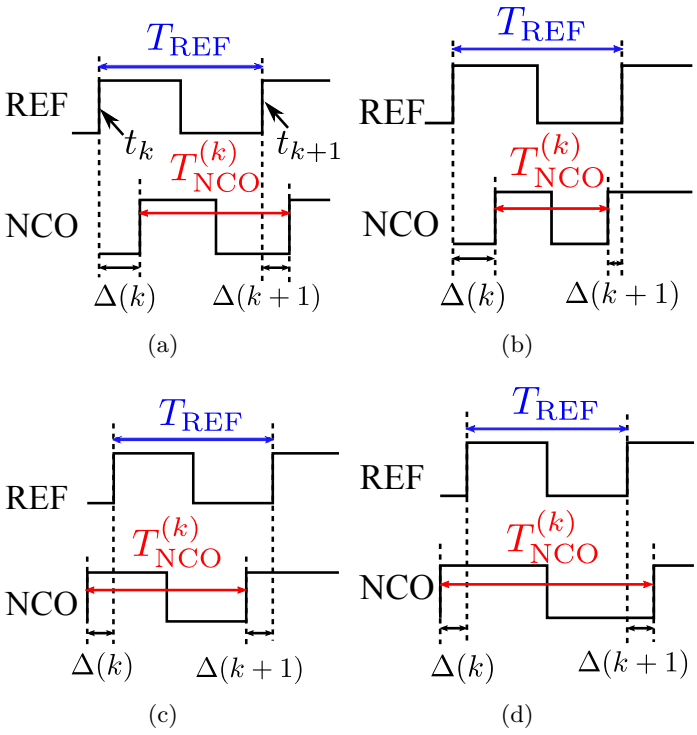


Figure 2.3: Relationship between REF and NCO before synchronization.

thus, we take some control algorithms which ensure the convergence of $\Delta(k)$ into consideration. One satisfying control algorithm can be proposed referring to the condition of a variable to be convergent in an analog system. Let the output of an analog system be '$x(t)$'. It is well known that if $x(t)$ is of the form as $x(t) = e^{-at}$ (a is a constant parameter), then $x(t)$ is asymptotically stable (convergent) on the condition that a is positive. The derivative of $x(t)$ can be obtained as $\mathrm{d}x(t)/\mathrm{d}t = -ax(t)$. Analogously, when it comes to a digital system, the series of $\Delta(k)$ is convergent when the first-order control algorithm below is applied to the primitive model, where a and c are constant parameters.

$$\Delta(k+1) - \Delta(k) = -a\Delta(k) + c. \qquad (a > 0) \tag{2.2}$$

As a consequence, the model of the first-order controlled clock synchronization is initially established as in Eq. (2.3) by substituting Eq. (2.2) into

Eq. (2.1).

$$T_{\mathrm{NCO}}^{(k)} = T_{\mathrm{REF}} - a\Delta(k) + c, \;\; k = 2, 3, \cdots . \tag{2.3}$$

Furthermore, in order to realize the model in Eq. (2.3) practically, the following approximation will be necessary,

$$\Delta(k) \approx \Delta(k-1), \;\; k = 2, 3, \cdots . \tag{2.4}$$

The model of first-order controlled clock synchronization is finally established as in Eq. (2.5).

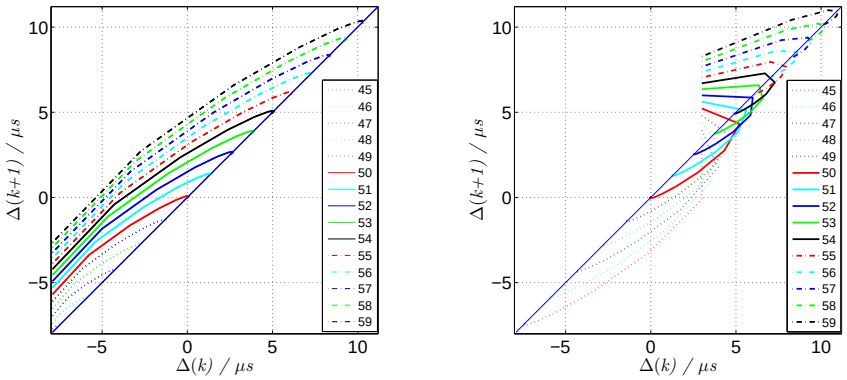
$$T_{\mathrm{NCO}}^{(k)} = T_{\mathrm{REF}} - a\Delta(k-1) + c. \;\; k = 2, 3, \cdots . \tag{2.5}$$

2.4 Simulation results

Simulations of the first-order controlled model in Eq. (2.5) are performed in MATLAB. The values of $\Delta(k+1)$ can be calculated by transforming Eq. (2.1) into Eq. (2.6). Then, according to Eqs. (2.5) and (2.6), all the values of $\Delta(k)$ in simulations can be obtained at the condition that $T_{\mathrm{NCO}}^{(1)}$, $\Delta(1)$, T_{REF}, a and c are given.

$$\Delta(k+1) = T_{\mathrm{NCO}}^{(k)} - T_{\mathrm{REF}} + \Delta(k). \;\; k = 1, 2, \cdots . \tag{2.6}$$

Referring to Eq. (2.2), it can be figured out that the convergence speed of the series of $\Delta(k)$ depends on the value of a. We define the time it takes for two clock signals to be synchronized as the settling time and generally, short settling time is desired in a clock synchronization method. Based on the fact that the clock synchronization is equivalent to the convergence of the series of $\Delta(k)$, the settling time in the first-order controlled clock synchronization is equivalent to the time it takes for the series of $\Delta(k)$ to be convergent. Therefore, in the first step, we aim to find out an ideal value of a, which enables the series of $\Delta(k)$ to be convergent quickly. For this purpose, we fix other parameters as $f_{\mathrm{NCO}}^{(1)} = 49\,\mathrm{kHz}$, $f_{\mathrm{REF}} = 50\,\mathrm{kHz}$, $\Delta(1) = 5\,\mu s$ and $c = 0$ in simulations and observe the convergence speed under different values of a. After many times of simulation, $a = 0.3$ is found to be an ideal choice in terms of convergence speed. Henceforth we will fix $a = 0.3$ in the first-order controlled model. As for c, let it satisfy the equation below for simplicity in



(a) (b)

Figure 2.4: Time evolution of $\Delta(k)$ in simulations for (a) $\Delta(1) = -8\,\mu s$. (b) $\Delta(1) = 3\,\mu s$. The numbers in legend represent the value of f_{REF}, which ranges from 45 kHz to 59 kHz. The diagonal line: $\Delta(k+1)$=$\Delta(k)$.

the program.

$$c + T_{\mathrm{REF}} = 20\,\mu s. \tag{2.7}$$

Given the above settings of a and c, the values of $\Delta(k)$ under different initial conditions, T_{REF} and $\Delta(1)$, can be obtained in simulations. The time evolution of $\Delta(k)$ in simulations are plotted in Fig. 2.4, where $\Delta(1) = -8\,\mu s$ stands for REF lags by $8\,\mu s$ in the beginning and $\Delta(1) = 3\,\mu s$ means REF leads by $3\,\mu s$ initially. In addition, f_{REF}, the reference frequency ranges from 45 kHz to 59 kHz with 1 kHz interval. In both figures, we can see that all trajectories of $\Delta(k)$ for different f_{REF} approach the line: $\Delta(k+1) = \Delta(k)$, which suggests all the series of $\Delta(k)$ converge. Therefore, the simulation results allow us to say that, for different values of f_{REF}, the clock synchronization between REF and NCO has been achieved based on the first-order controlled model. It can also be observed that the two trajectories for the same f_{REF} in Figs. 2.4(a) and 2.4(b) converge to the same value. Thus it is confirmed that the clock synchronization is independent to $\Delta(1)$. Substituting $f_{\mathrm{REF}} = f_{\mathrm{NCO}}$ and Eq. (2.7) into Eq. (2.5), the convergence value of $\Delta(k)$ for each f_{REF} can be calculated as in Eq. (2.8). The convergence value correspond to the final phase differences between REF and NCO for each f_{REF}. Here, due to the setting of c, the convergence values for different

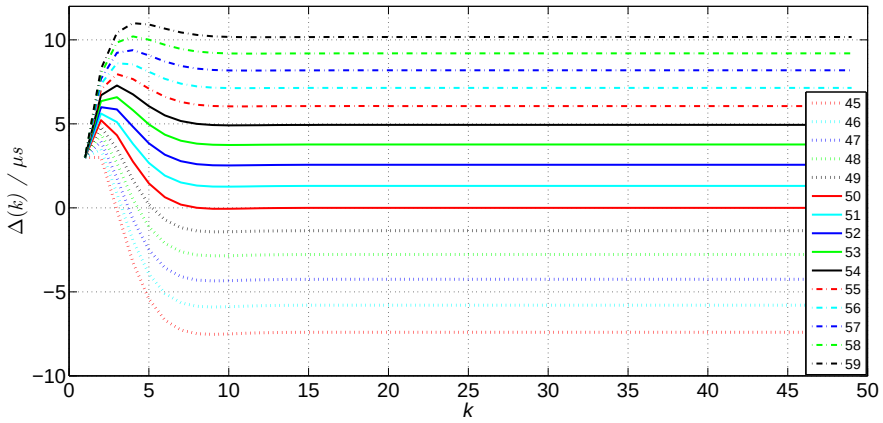


Figure 2.5: Values of $\Delta(k)$ in simulations. $\Delta(1) = 3\,\mu$s. $f_{\mathrm{REF}} \in [45, 59]\,$kHz.

f_{REF} are different as exhibited in Figs. 2.4(a) and 2.4(b).

$$\Delta(k-1) = \frac{20\mu s - T_{\mathrm{REF}}}{a}. \tag{2.8}$$

Next, the settling time of the first-order controlled clock synchronization is of concern. As previously mentioned, the settling time here is identical to the time it takes for the series of $\Delta(k)$ to be convergent. In Fig. 2.5, the values of $\Delta(k)$ for each f_{REF} in simulations are presented. It is readily apparent that for each f_{REF}, the values of $\Delta(k)$ remain the same after $k = 10$. It implies the series of $\Delta(k)$ is convergent. Therefore, it can be concluded that the settling time of the first-order controlled clock synchronization is nine reference clock cycles in simulations.

2.5 Experimental results

In order to verify the first-order controlled clock synchronization in experiments, we implement the first-order controlled model in Eq. (2.5) in a Xilinx Spartan®-6 FPGA (XC6LX16-CS324) board. From Eq. (2.5), we see that the controlled model can be realized by two functional modules: the PFD and the block NCO. The function of both modules can be described in VHSIC hardware description language (VHDL). In particular, the VHDL code for the block NCO is generated by the toolbox of HDL

Coder in MATLAB R2013b. It should be noted that the frequency of NCO (f_{NCO}) is adjustable as in Eq. (2.9), where $f_{\mathrm{NCO}}^{(k)}$ denotes the frequency of NCO at t_k and $Inc^{(k)}$ is the input argument (phase increment) used to adjust $f_{\mathrm{NCO}}^{(k)}$. Moreover, N in Eq. (2.9) is determined by the resolution (Δf) and the sampling frequency (F_{s}) of the block NCO. The values of Δf and F_{s} in experiments are set as in Eqs. (2.10) and (2.11). Accordingly, $N = 27$ is obtained and $f_{\mathrm{NCO}}^{(k)}$ in experiments can be calculated as in Eq. (2.12).

$$f_{\mathrm{NCO}}^{(k)} = F_{\mathrm{s}} \times \frac{Inc^{(k)}}{2^N} \text{ Hz}, \tag{2.9}$$

$$F_{\mathrm{s}} = 100\,\mathrm{MHz}. \tag{2.10}$$

$$\Delta f = \frac{F_{\mathrm{s}}}{2^N} \approx 1\,\mathrm{Hz}. \tag{2.11}$$

$$f_{\mathrm{NCO}}^{(k)} = 1e^8 \times \frac{Inc^{(k)}}{2^{27}} \text{ Hz}. \tag{2.12}$$

For the sake of comparing the experimental results with simulation results, the parameters and initial conditions in experiments are set the same as those in simulations, i.e., $f_{\mathrm{NCO}}^{(1)} = 45$ kHz, $a = 0.3$, and $c = 20\,\mu\mathrm{s} - \mathrm{T_{REF}}$. Subsequently, according to Eqs. (2.5), (2.7), and (2.12), the value of $Inc^{(k)}$ can be calculated by Eq. (2.13), where $\Delta(k-1)$ is in nanosecond order.

$$Inc^{(k)} = \begin{cases} \frac{10\times 2^{27}}{20000-3\Delta(k-1)}, & \Delta(k-1) \geq 0, \\ \\ \frac{10\times 2^{27}}{20000+3\Delta(k-1)}, & \Delta(k-1) < 0. \end{cases} \tag{2.13}$$

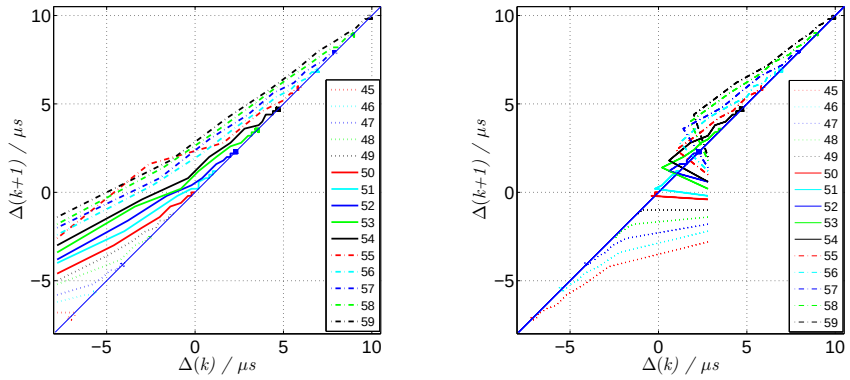
Based on Eqs. (2.12) and (2.13), it can be figured out that $f_{\mathrm{NCO}}^{(k)}$ is directly controlled by $\Delta(k-1)$. In addition, it is worth mentioning that in experiments, the value of $\Delta(k-1)$ is restricted in the program to the range in Eq. (2.14) for simplicity.

$$0 \leq \Delta(k-1) \leq 1000, \text{ or } -1000 \leq \Delta(\mathrm{k}-1) \leq 0. \tag{2.14}$$

Along with the restriction of $\Delta(k-1)$, the value of $f_{\mathrm{NCO}}^{(k)}$ is restricted as $f_{\mathrm{NCO}}^{(k)} \in [43.4, 59]$ kHz according to Eqs. (2.12), (2.13) and (2.14). This implies f_{REF} should also be within this range so that the clock synchronization

between REF and NCO can be achieved. This is also the reason why f_{REF} in simulations is selected from 45 kHz to 59 kHz.

Provided with the above formulas and the settings of the parameters, the values of $\Delta(k)$ yielded by the first-order controlled model in experiments can be obtained. The time evolution of $\Delta(k)$ for different reference frequencies under conditions of $\Delta(1) = -8\,\mu$s and $\Delta(1) = 3\,\mu$s are plotted in Figs. 2.6(a) and 2.6(b), respectively. In experiments, REF is a reference clock signal generated by an FPGA board. We can see that all trajectories in Figs. 2.6(a) and 2.6(b) approach the line $\Delta(k+1) = \Delta(k)$ as in simulations. Thus the convergence of $\Delta(k)$ is confirmed which further implies the achievement of clock synchronization. Comparing Figs. 2.6(a) and 2.6(b) to Figs. 2.4(a) and 2.4(b), it can be found that the convergence values of $\Delta(k)$ for different f_{REF} in experiments have a good agreement with those in simulations. Besides, the values of $\Delta(k)$ in experiments are shown in Fig. 2.7. It can be observed that the values of $\Delta(k)$ remain the same approximately after $k = 11$. That is the settling time of the first-order controlled clock synchronization is around 10 T_{REF} in experiments.



(a) (b)

Figure 2.6: Time evolution of $\Delta(k)$ in experiments for (a) $\Delta(1) = -8\,\mu s$. (b) $\Delta(1) = 3\,\mu s$. The numbers in legend represent the value of f_{REF}, which ranges from 45 kHz to 59 kHz. $f_{\mathrm{REF}} \in [45, 59]$ kHz. The diagonal line: $\Delta(k+1)$=$\Delta(k)$.

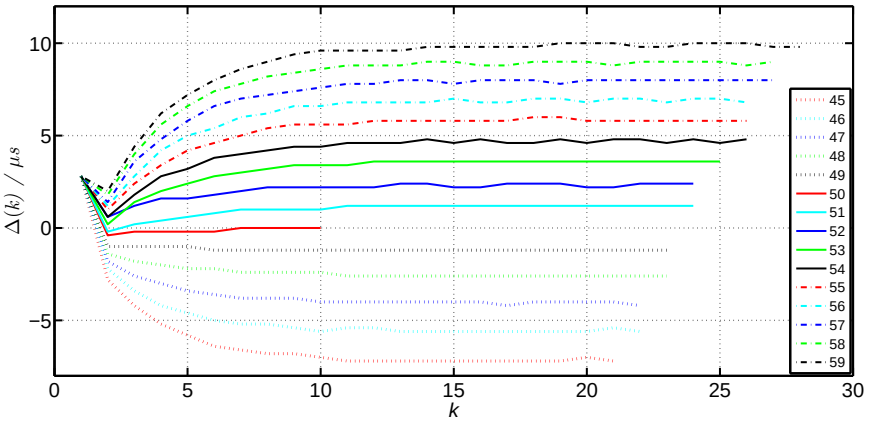


Figure 2.7: Values of $\Delta(k)$ in experiment, $\Delta(1) = 3\,\mu$s. $f_{\mathrm{REF}} \in [45, 59]$ kHz.

2.6 Summary

In this chapter the first-order controlled clock synchronization was covered. At first, based on the mechanism of CPPLL in achieving the clock synchronization, a first-order controlled model of the digital clock synchronization method was established. The model was an attempt to address the potential deficiencies existing in current available clock synchronization method applied to the power packet dispatching system. Then the effectiveness of the established model in achieving the clock synchronization between two clock signals was verified. It was also confirmed that the achievement of the clock synchronization was independent on the initial conditions. In addition, it was found that the settling time was around 10 reference clock cycles in experiments. The work done in this chapter can be considered as the preparation for achieving clock synchronization in the power packet dispatching system.

Generally speaking, frequency synthesizers with fast settling time are considered to be essential blocks of modern communication systems [34]. Likewise, a shorter settling time is also desired in the clock synchronization method specified for power packet dispatching. This is the motivation for us to proceed to a second-order controlled clock synchronization. The derivation of the second-order controlled model will be given in detail in the following chapter. Furthermore, the stability of the second-order con-

trolled model is under discussion considering the application of the model to the power packet dispatching system in practical. After verifying the availability of the model in achieving autonomous clock synchronization, power packet dispatching based on the autonomous clock synchronization will also be discussed.

Chapter 3

Second-Order Controlled Clock Synchronization

3.1 Prologue

In this chapter, a second-order controlled model of the digital clock synchronization method will be derived for shortening the settling time of the clock synchronization. The stability of the controlled model will be analyzed for its practical applications to a power packet dispatching system. Under the condition of stability, the controlled model will be carried out in both simulations and experiments so as to verify the achievement of clock synchronization between two clock signals. Thereafter, in order to validate power packet dispatching based on autonomous clock synchronization, the controlled model will be embedded into a router in a basic power packet dispatching system. Finally, the contents of this chapter will be summarized in the end.

3.2 Second-order controlled model

The settling time is a key factor in evaluating the performance of a clock synchronization method and generally short settling time is required. Short settling time is also desired in a clock synchronization method applied to the power packet dispatching system. On one hand, from the standpoint of loads, continuous power supply is expected when the loads request power. On the other hand, power is supplied via power packets and only the payload

of packets carries power as introduced in Sect. 1.1. Additionally, we assume that there is no interval between two power packets during the power supply. Therefore, it is clear that higher duty ratio of the payload in a power packet corresponds to more continuous power supply. Let us recall that a preamble is added in front of each packet for achieving the clock synchronization. Thus we can consider the preamble as an additional part of a power packet which does not carry power either as the information tags. In this sense, short preamble is desired for continuous power supply. Furthermore, the length of the preamble depends on the settling time of the clock synchronization, .i.e., the shorter the settling time, the shorter the preamble. Hence, we are motivated to further establish a second-order controlled model of the digital clock synchronization method aiming for shorter settling time.

The second-order controlled model of the digital clock synchronization method is derived as in Eq. (3.1), where a_1 and a_2 are constant parameters within the range of $a_1 \neq 1, a_2 > 0$.

$$T_{\mathrm{NCO}}^{(k)} = a_1 T_{\mathrm{NCO}}^{(k-1)} - a_2\Delta(k) + a_1 a_2 \Delta(k-1) + (1-a_1)T_{\mathrm{REF}}. k = 2, 3, \cdots . \quad (3.1)$$

The derivation of the model is given in detail in Appendix A. From Eq. (3.1), we can tell that in the second-order controlled clock synchronization, the achievement of the clock synchronization ($T_{\mathrm{NCO}}^{(k)} = T_{\mathrm{NCO}}^{(k-1)} = T_{\mathrm{REF}}$) is equivalent to the series of $\Delta(k)$ converges to 0, i.e., $\Delta(k) = \Delta(k-1) = 0$.

3.2.1 System stability

Like any other feedback control systems such as CPPLL, the model derived above has to be designed with a proper consideration for stability. When the second-order controlled clock synchronization is applied to the power packet dispatching system, the stability is indispensable for power packet dispatching. Referring to Eq. (3.1), we can find that the stability of the model relies on the parameters a_1 and a_2. For this reason, in the next step, the range of the parameters (a_1 and a_2) which guarantees the model be stable is under discussion.

There are several ways to analyze the stability of a model or a system. For instance, the root locus technique is applied to analyze the effects of the digital loop filter parameters on the stability of an ADPLL in [35]. In [36], the stability analysis of a CPPLL is performed using the discrete-time state

equations while the phase margin is utilized to discuss the stability of an ADPLL in [24]. For the model given in Eq. (3.1), it can be considered as a second-order digital system, and thus the characteristic equation can be employed to analyze its stability. The detail of the stability analysis of the model is given in Appendix B. As a result, the range of the parameters (a_1 and a_2) which ensures the stability of the model is obtained as in Eq. (3.2).

$$-1 < a_1 < 1,\ 0 < a_2 < 2. \tag{3.2}$$

3.3 Simulation results

Under the condition of stability, it is further necessary to determine the ideal values of a_1 and a_2 for achieving clock synchronization in a short time. Similar to the way of determining the ideal value of a in the first-order controlled model, the ideal values of a_1 and a_2 can also be determined through many times of simulations. In simulations, we compare the settling time by observing the values of $\Delta(k)$ for different parameters. The formula of calculating the value of $\Delta(k)$ is derived through the deformation of Eq. (A.1) as follows,

$$\Delta(k) = T_{\mathrm{NCO}}^{(k-1)} - T_{\mathrm{REF}} + \Delta(k-1), \quad k = 2, 3, \cdots . \tag{3.3}$$

According to Eqs. (3.1) and (3.3), the values of $\Delta(k)$ can be obtained at the condition that $T_{\mathrm{NCO}}^{(1)}$, $\Delta(1)$, and T_{REF} are given. As a result, it is found that $a_1 = 0.0001$ and $a_2 = 1.01$ is one of the combinations that ensure short settling time. Henceforth, we fix $a_1 = 0.0001$ and $a_2 = 1.01$ in simulations and experiments related to the second-order controlled model.

Under the above setting of parameters, we continue to confirm the settling time of the second-order controlled clock synchronization. Figure 3.1 displays the values of $\Delta(k)$ for different reference frequencies (f_{REF}) in simulations, where f_{REF} ranges from 10 Hz to 1000 kHz. The simulation results are obtained under the condition of $T_{\mathrm{NCO}}^{(1)} = 0.1\,\mathrm{s}$ and $\Delta(1) = T_{\mathrm{REF}}/4$. k, as mentioned before, indicates the serial number of the reference clock cycle. $\Delta(1) = T_{\mathrm{REF}}/4$ means REF leads NCO by $T_{\mathrm{REF}}/4$ in the beginning. Special attention should be paid to the different units of the points on different lines, which are listed in corresponding labels in Fig. 3.1. For example, for $f_{\mathrm{REF}} = 10$ Hz and $f_{\mathrm{REF}} = 1000$ kHz, the units of $\Delta(k)$ are 10 ns, whereas

$\Delta(k)$ for $f_{\mathrm{REF}} = 100\,\mathrm{Hz}$ is in units of 1000 ns. As seen from Fig. 3.1, all the series of $\Delta(k)$ have a peak value at k=2, except for $f_{\mathrm{REF}} = 10\,\mathrm{Hz}$. Moreover, $\Delta(2)$ is far greater than other $\Delta(k)$ for each f_{REF}. This phenomenon is attributed to the setting of the initial value of T_{NCO} ($T_{\mathrm{NCO}}^{(1)} = 0.1\,\mathrm{s}$). Apart from $T_{\mathrm{REF}} = 0.1\,\mathrm{s}$ for $f_{\mathrm{REF}} = 10\,\mathrm{Hz}$, $T_{\mathrm{NCO}}^{(1)}$ is far greater than all the other T_{REF} ranging from 1 μs to 0.01 s. Take $f_{\mathrm{REF}} = 100\,\mathrm{Hz}$ as an example, we can obtain $\Delta(1) = T_{\mathrm{REF}}/4 = 0.0025\,\mathrm{s}$. Then $\Delta(2)$ can be calculated from Eq. (3.3) as 0.0925 s, and thus $\Delta(2)$ is far greater than $\Delta(1)$. However, due to the second-order control to T_{NCO}, the following $\Delta(3)$ becomes small. From Fig. 3.1, it can be observed that all the series of $\Delta(k)$ remain at 0 after $k = 4$. This implies the clock synchronization has been achieved within three reference clock cycles. That is the settling time of the second-order controlled clock synchronization is three T_{REF} in simulations.

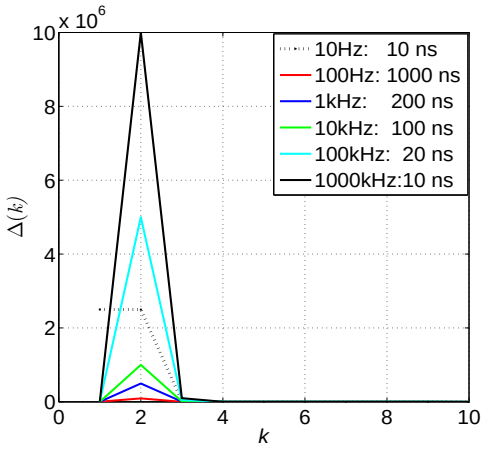


Figure 3.1: Values of $\Delta(k)$ in simulations for different f_{REF}; f_{REF} ranges from 10 Hz to 1000 kHz. $\Delta(k)$ in different lines are of different units as listed in the legend of the figure.

3.4 Experimental results

Next, the second-order controlled model in Eq. (3.1) will be implemented in a Xilinx Spartan®-6 FPGA (XC6LX16-CS324) board in experiments to verify the achievement of clock synchronization between tao clock signals. The parameters in experiments are set the same as in simulations, i.e., $T_{\mathrm{NCO}}^{(1)} = 0.1\,\mathrm{s}$ and $\Delta(1) = T_{\mathrm{REF}}/4$. For realizing the model in exper-

iments, Eq. (3.1) is deformed as in Eq. (3.4) by replacing $\Delta(k-1)$ with $\Delta(k)/(1-a_2)$. The deformation is based on Eq. (A.3) in Appendix A.

$$T_{\mathrm{NCO}}^{(k)} = a_1 T_{\mathrm{NCO}}^{(k-1)} - a_2(1 - \frac{a_1}{1-a_2})\Delta(k) + (1-a_1)T_{\mathrm{REF}}. \tag{3.4}$$

Given $a_1 = 0.0001$ and $a_2 = 1.01$, the following approximation can be made,

$$1 - \frac{a_1}{1-a_2} \approx 1. \tag{3.5}$$

Subsequently, the model in Eq. (3.4) can be simplified as

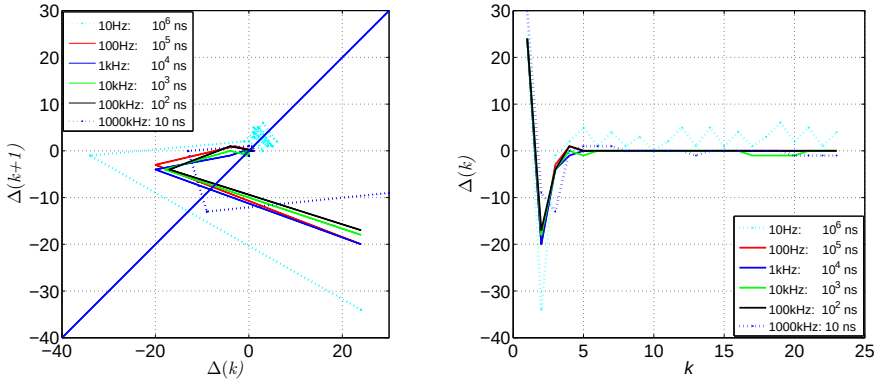
$$T_{\mathrm{NCO}}^{(k)} = a_1 T_{\mathrm{NCO}}^{(k-1)} - a_2\Delta(k) + (1-a_1)T_{\mathrm{REF}}. \tag{3.6}$$

Then according to Eqs. (2.12) and (3.6), the second-order controlled model can be eventually described in VHDL as below.

$$Inc^{(k)} = \frac{2^{27}}{a_1 \frac{2^{27}}{Inc^{(k-1)}} - [a_2\Delta(k) - (1-a_1)T_{\mathrm{REF}}] \times 10^8}, \tag{3.7}$$

where $\Delta(k)$ and T_{REF} are in units of seconds. From Eqs. (2.12)) and (3.7)), we can tell that $f_{\mathrm{NCO}}^{(k)}$ is adjusted by both $f_{\mathrm{NCO}}^{(k-1)}$ and $\Delta(k)$.

The time evolution of $\Delta(k)$ in experiments are shown in Figs. 3.2(a) and 3.3(a), where f_{REF} ranges from 10 Hz to 1000 kHz. The results in Fig. 3.2(a) are obtained under the condition of $\Delta(1) = T_{\mathrm{REF}}/4$ while the results in Fig. 3.2(a) correspond to $\Delta(1) = -T_{\mathrm{REF}}/4$. Also, it should be noted that the points on different lines in these figures are of different units as annotated in the legends. We can see that all trajectories in both figures approach the origin, except for $f_{\mathrm{REF}} = 10$ Hz. This means all the series of $\Delta(k)$ are convergent to 0 for different reference frequencies except for $f_{\mathrm{REF}} = 10$ Hz. Furthermore, the values of $\Delta(k)$ are exhibited in Figs. 3.2(b) and 3.3(b). It can be seen that $\Delta(k)$ for different f_{REF}, except for $f_{\mathrm{REF}} = 10$ Hz, remain at 0 approximately after $k = 6$, which implies it takes around five reference clock cycles for $\Delta(k)$ to be convergent. That is the settling time of the second-order controlled clock synchronization is around five T_{REF}. Therefore, it is verified that the settling time has been greatly shortened by the second-order controlled model compared to the first-order controlled clock synchronization. In addition, the failure in convergence of $\Delta(k)$ for $f_{\mathrm{REF}} = 10$ Hz can be observed in both figures. Consequently, one



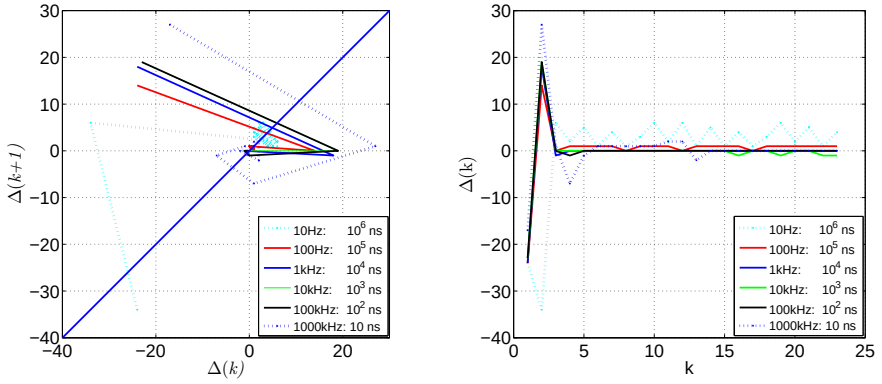
(a) (b)

Figure 3.2: Experimental results of $\Delta(k)$ for $\Delta(1) = T_{\mathrm{REF}}/4$. (a) time evolution of $\Delta(k)$. (b) values of $\Delta(k)$. f_{REF} ranges from 10 Hz to 1000 kHz. $\Delta(k)$ on different lines have different units as listed in the legends.

may conclude that based on the second-order controlled model, the clock synchronization between two clock signals is achieved for f_{REF} ranging from 100 Hz to 1000 kHz.

3.5 Implementation into power packet dispatching system

As discussed above, the clock synchronization between two clock signals can be achieved based on the second-order controlled model. In the next step, we aim to realize power packet dispatching based on autonomous clock synchronization. Here, "autonomous" means that the clock synchronization between the mixer and the router is achieved through power packets themselves without using any external clock line. For this purpose, the second-order controlled model is embedded into a router. Shown in Fig. 3.4 is the experimental power packet dispatching system, which contains one direct current (DC) source (9.34 V), one mixer, one router and two resistive loads ($R_{1,2} = 100\,\Omega$). We refer to a system which includes one mixer and one router as a basic power packet dispatching system. As introduced before, a preamble (several cycles of reference clock signal) is added in front of each packet for achieving autonomous clock synchronization. It has been con-



(a) (b)

Figure 3.3: Experimental results of $\Delta(k)$ for $\Delta(1) = -T_{\text{REF}}/4$. (a) time evolution of $\Delta(k)$. (b) values of $\Delta(k)$. f_{REF} ranges from 10 Hz to 1000 kHz. $\Delta(k)$ on different lines have different units as listed in the legends.

firmed in Sect. 3.4 that based on the second-order controlled model, the clock synchronization can be achieved within five T_{REF}. Thus, for insurance purpose, six cycles of reference clock signal are included in the preamble. A setting of a power packet employed in experiments is illustrated in Fig. 3.5. The preamble is designed as "101010101010" with every two bits of "10" representing one reference clock cycle, i.e., "101010101010" stands for six cycles of reference clock signal. Also, it is worth mentioning that the bit length of the preamble is equal to that of the packet signal, which is also identical with the mixer clock period (T_{mixer}). Hence, $T_{\text{REF}} = 2T_{\text{mixer}}$ in the setup. Furthermore, as shown in Fig. 3.5 the header of the packet is of six bits, a start signal "101" followed by a source signal '0' or '1' and two more bits defined as an address signal. The payload takes up 85 bits and the end signal in the footer is designed as "001010000". Among these signals, the start signal and the end signal indicate the beginning and the end of the packet, respectively. The source signal specifies the storages in the router [15,37], which will be explained later. The address signal is for determining the router output ports. Power packets are dispatched to the loads connected to the selected ports. In experiments, two types of address signal, "11" and "01", are employed so as to dispatch power packets to two different loads. In more specific terms, the address signal "11" indicates the packet is dispatched to the load connected to router output port 1 (OUT1) and "01"

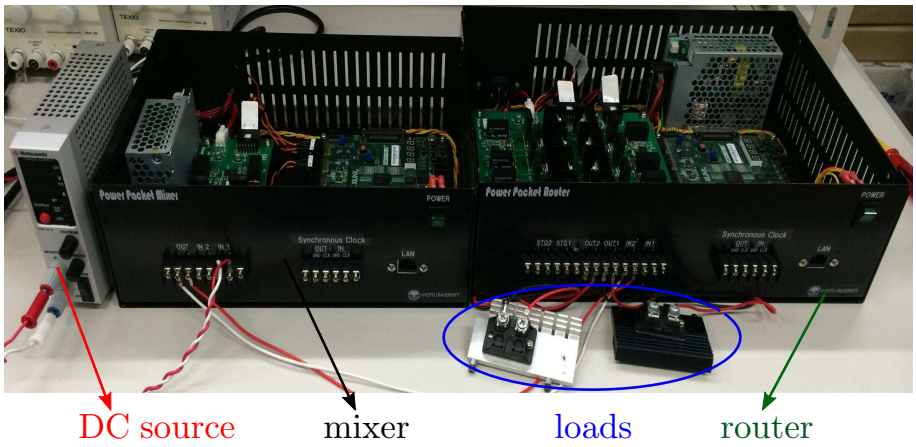


Figure 3.4: Experimental power packet dispatching system with a second-order controlled model embedded.

corresponds to the load attached to the router output port 2 (OUT2). In what follows, R_1 and R_2 are connected to OUT1 and OUT2, respectively.

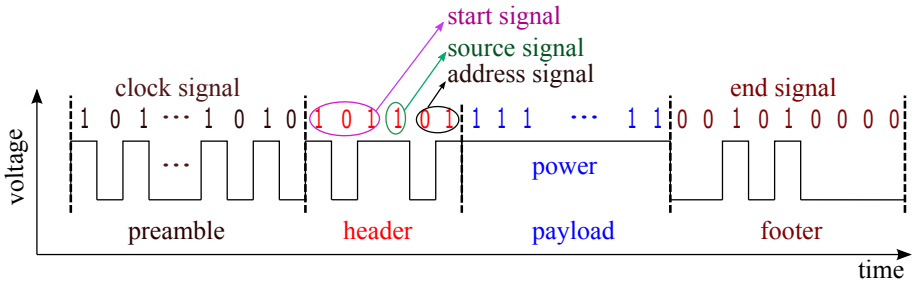


Figure 3.5: Setting of a power packet with preamble ahead in experiment. The preamble is added in front of each packet to achieve the clock synchronization.

3.5.1 Router clock signal

Let us bear in mind that the preamble is added in front of each packet to achieve the clock synchronization, and thus it should not be recognized as the packet signal. In addition, the packet signal received in the router is read at every rising edge of the router clock signal. Based on the above two points, the router clock signal should not exist in the preamble duration of each packet. Given the fact that the signal NCO is needed in the process of clock synchronization, i.e., NCO exists during the preamble, it is inappropriate to treat the signal NCO as the router clock signal directly. As a solution,

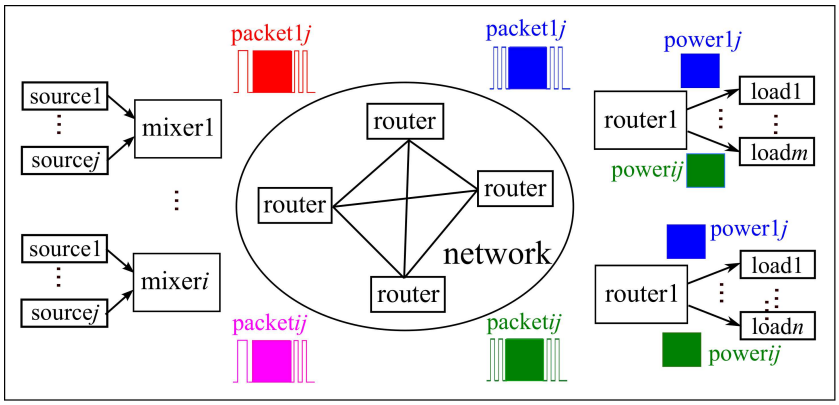


Figure 3.6: Conceptual diagram of a power packet dispatching system with network design.

another signal named as CLKIN is generated and is adopted as the router clock signal. To be more specific, CLKIN is identical to NCO in each packet duration starting from the header. As explained in Sect. 3.5, T_{REF} is equal to $2T_{\mathrm{mixer}}$ because of the setting of power packets. Accordingly, $T_{\mathrm{NCO}} = T_{\mathrm{REF}} = 2T_{\mathrm{mixer}}$ is obtained at the end of the preamble due to the clock synchronization achieved by the embedded model. Hence, T_{NCO} needs to be halved and kept for achieving T_{CLKIN}=$T_{\mathrm{NCO}} = T_{\mathrm{mixer}}$ in the packet duration. That is the clock synchronization between the mixer clock signal and the router clock signal is achieved. Furthermore, in order to avoid affecting the signal recognition of the following packet, the synchronized router clock signal, CLKIN, is set to be '0' before the next packet being received. By this means, signal in each packet can be recognized correctly.

In addition to the above setting, there is more requirement of CLKIN considering the expansion of the power packet dispatching system into a network system for power distribution in future. Figure 3.6 illustrates a conceptual diagram of a power packet dispatching system with network design [15, 37]. In the system, two kinds of routers are included: routers in the network and routers connected to loads. The routers in the network are in charge of forwarding power packets while the other kind of routers are for transferring power of packets to loads. In view of the function of the routers in the network, power packets should not be changed at output ports of these routers. However, a power packet will not be dispatched until its header is completely read in the router. As a result, the header will not appear at the output port. To solve this issue, repacketization of packets is

proposed, which is defined as recovering the received packet at the output ports including the preamble. At present, however, we focus on recovering packets starting from the header only. Moreover, six extra router clock cycles (T_{CLKIN}) are needed after the footer in order to realize the repacketization [15, 37]. In our experiments, 10 more router clock cycles are retained for each power packet. Thereafter, CLKIN is set to be '0' and NCO is continuously output with $T_{\mathrm{NCO}} = 0.1$ ms which is pre-assigned in the program. Therefore, CLKIN lasts for one packet duration plus 10 more router clock cycles. Once the next preamble is received, the clock synchronization for the next power packet will be started automatically.

3.5.2 Verification of power packet dispatching

Based on the determination of the router clock signal CLKIN, the experiment of power packet dispatching in the basic system is carried out. The results are shown in Fig. 3.7, where the signal "OUT2" represents the voltage across R_2 and the signal "packet" denotes the received packet at the router input port. Moreover, the signals are plotted in Fig. 3.7 based on different reference voltages, i.e., the reference voltages for packet, OUT2, NCO, and CLKIN are set at 0V, 2V, 2V, and 0V, respectively. At first, the signals NCO and CLKIN in one packet duration is confirmed. As shown in Fig. 3.7, NCO is always in existence, whereas CLKIN only exists in the packet duration and further for a while after the footer. Figure 3.8 gives more detail about the signals, from which it is confirmed that after the footer, 10 cycles of synchronized router clock signal are retained in both CLKIN and NCO. Thereafter, T_{NCO} is kept at 0.1ms as pre-assigned in the program. Additionally, in Fig. 3.8, the synchronization process for the following packet during the following preamble can also be observed. Then, the power packet dispatching needs to be confirmed. The header of the packet in Fig. 3.7 is given as "101101". As explained earlier in Sect. 3.5, the address signal "01" indicates the packet should be dispatched to OUT2 and this can be observed in Fig. 3.7. As thus, the power packet dispatching based on autonomous clock synchronization is verified in experiments.

After the verification of power packet dispatching, the range of the mixer clock frequency (f_{mixer}) within which the power packet dispatching can be successful is of concern. In experiments, f_{mixer} is set by a parameter $fset$

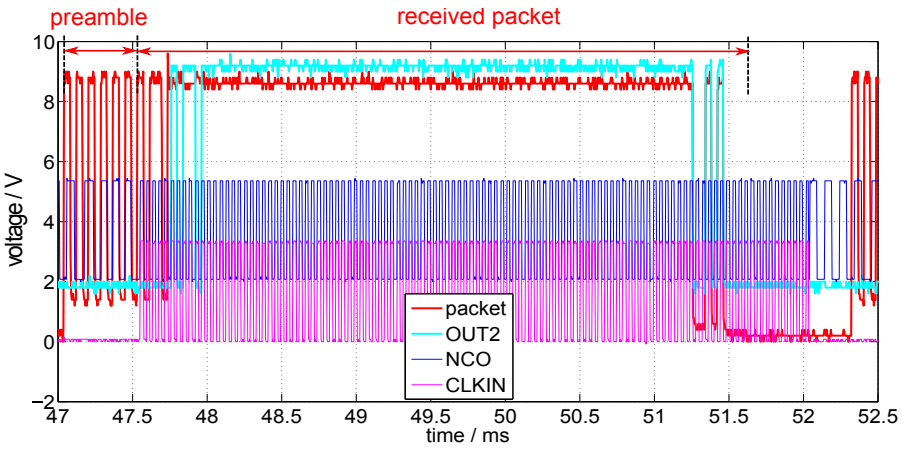


Figure 3.7: Experimental results of power packet dispatching in one packet duration. T_{mixer}=41 μs. Reference voltages for OUT2 and NCO are 2V.

satisfying the following relationship given in Eq. (3.8).

$$f_{\text{mixer}i} = \frac{10^8}{2^{(fset_i+1)}} \text{ Hz}. \tag{3.8}$$

Through experiments, it is found that under the above setting of the preamble (the bit length of the preamble equals to T_{mixer}), power packets can be dispatched correctly for $fset$ ranging from 8 to 11. It means that the power packet dispatching succeeds for $f_{\text{mixer}} \in [24.4\,\text{kHz}, 195\,\text{kHz}]$. However, in Sect. 3.4, it has been confirmed that based on the second-order controlled model, the clock synchronization between two clock signals can be achieved for f_{REF} ranging from 100 Hz to 1000 kHz. The different ranges suggest that the clock synchronization fails for some f_{REF} when REF becomes the preamble of a power packet. It is possible that the failure is caused by the noise in the preamble, which can be introduced by switching operation in the generation process of the preamble. Next, we change the setting of the preamble to investigate whether the setting of the preamble will affect the range of f_{mixer}. The bit length of the preamble is changed to half of T_{mixer}. Accordingly, it is unnecessary to halve T_{NCO} after the preamble for achieving T_{CLKIN}=T_{NCO} = T_{mixer}. In this case, it is confirmed in experiments that power packet dispatching succeeds for $f_{\text{mixer}} \in [763\,\text{Hz}, 195\,\text{kHz}]$, i.e., $fset \in [8, 16]$. Compared to the previous setting of the preamble, the range of f_{mixer} under this setting of the preamble (the bit length of the preamble

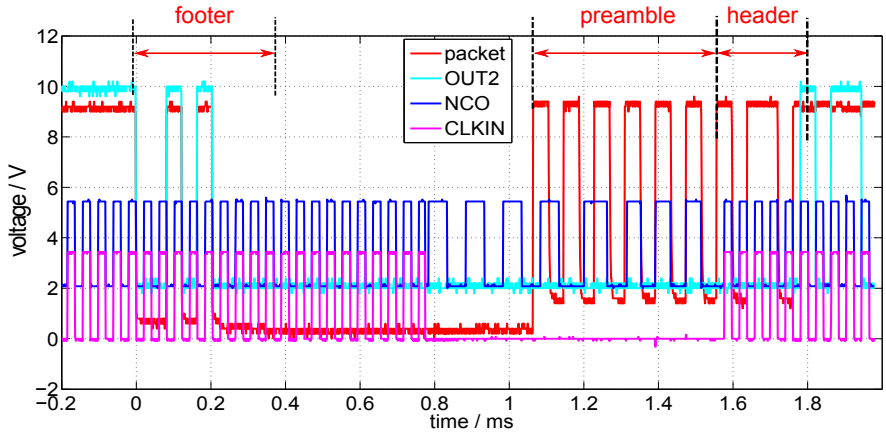


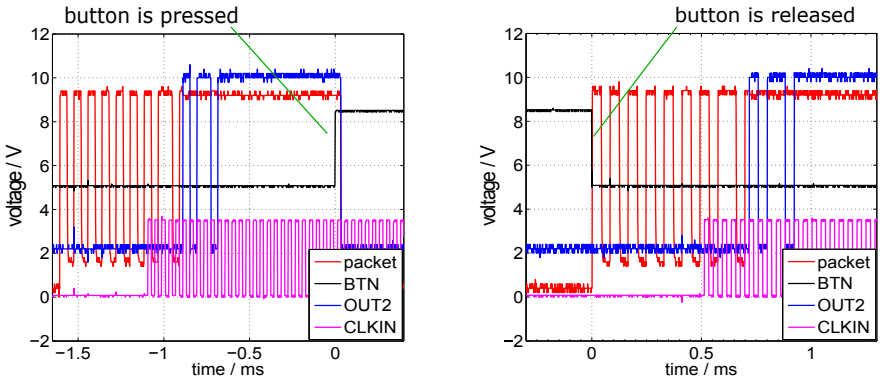
Figure 3.8: NCO and CLKIN in part of one packet period. T_{mixer}=41 μs. Reference voltages for OUT2 and NCO are 2V.

equals to half of T_{mixer}) is widely expanded. As thus, it is speculated that with the setting of the preamble in Fig. 3.5, the operation of dividing the synchronized T_{NCO} by 2 in the program introduces calculation error to the router clock signal T_{CLKIN}. Consequently, the clock synchronization between the mixer clock signal and the router clock signal becomes loose and further incorrect signal recognition is caused. The exact reason of the difference in the ranges of f_{mixer} will be left for future research.

3.5.3 Button operation

In the mixer, some parameters such as T_{mixer} and the time interval between packets can be regulated via the buttons on the FPGA board. In addition, the parameters can be changed at any time. For keeping the system safe, the mixer should output signal '0' during the time when buttons are pressed. Correspondingly, the router output becomes '0' too. On the other hand, after the button is released, new power packets are generated based on the new parameters. These two operations are confirmed in experiments as shown in Figs. 3.9(a) and 3.9(b), where "BTN" represents the button signal. Figure 3.9(a) illustrates the case that the button is pressed (BTN changes from low to high) during the payload of the received packet. Both the input and output of the router, represented by packet and OUT2, become '0' once the button is pressed and remain at '0' during the press (BTN keeps high). In Fig. 3.9(b), the button is released with BTN chang-

ing from high to low, after which a new packet with preamble ahead is generated.



(a) (b)

Figure 3.9: Input and output of the router when (a) BTN is pressed. (b) BTN is released. $T_{\text{mixer}} = 41\,\mu$s. Reference voltages for BTN and OUT2 are 5V and 2V, respectively.

3.5.4 Repacketization

As explained earlier, repacketization of power packets are expected at the output ports of the routers in the network. The repacketization can be achieved through an algorithm [14,15,38], where a shift register is designed. This is because on one hand power is needed to recover the packet and the power is supplied from the received packet. On the other hand, the power is transferred after the header of the packet is completely recognized. In the algorithm of repacketization, the shift register leads to six bits delay (the bit number of the header) between the repacketized packet and the received packet. As shown in Fig. 3.7, the output at OUT2 is a repacketized packet. However, the results clearly show that the repacketized packet becomes six bits shorter than the received packet (the header is six bits delayed while the footer is not delayed). This phenomenon can be explained from two aspects. One is that the power can not be delayed and thus no power is supplied to repacketize the signals after the payload of the received packet. The other is related to the switches in the router. The structure of the switches in the router will be explained later in more detail. The switches are turned on once the header of the received packet is completely recognized

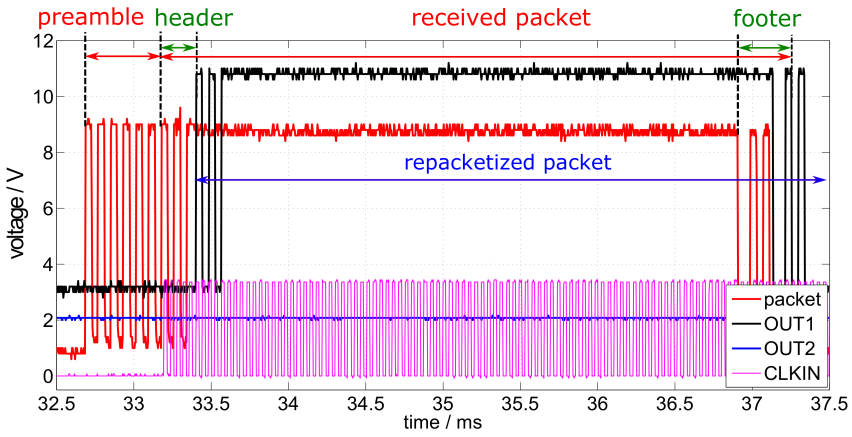


Figure 3.10: Input and output of the router with installed storages. Header is "101011". Reference voltages for OUT1 and OUT2 are 3V and 2V, respectively.

and are turned off after the footer is completely recognized. Moreover, when the switches are turned on and there is no power for repacketization, the packet signal will be directly transmitted to the router output port. As a consequence, the packet signal between the payload and the footer will be directly transmitted to the router output port.

The above incomplete repacketization issue can be solved by installing storages, namely capacitors, in the router [15, 38]. By means of installing storages, the transferred power of packet can be stored. Consequently, the signal after the payload of the received packet can also be repacketized correctly, i.e., the footer is also delayed. The router output with installed storages are illustrated in Figs. 3.10 and 3.11, where the signal OUT1 represents the voltage across the load R_1. The header of the packet in Fig. 3.10 is "101011", and thus the packet is dispatched to the port OUT1 according to the address signal "11". Compared to Fig. 3.7, it is found that the footer is indeed delayed by six bits in Fig. 3.10. Thus, we say that complete repacketization is realized. The header of the packet in Fig. 3.11 is "101101" and the repacketization is achieved at OUT2 as expected. Based on the above results, it can be concluded that packets are dispatched correctly to different output ports and are repacketized completely at the same time by means of installing storages. It is worth mentioning again that the power packet dis-

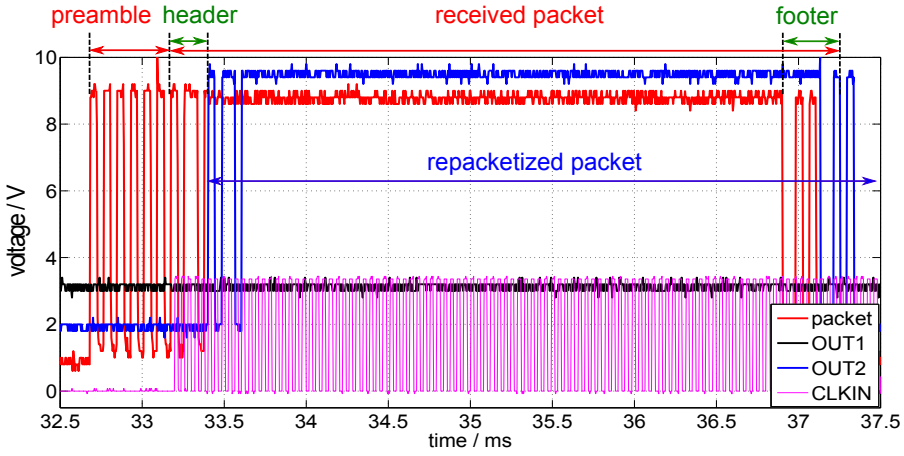


Figure 3.11: Input and output of the router with installed storages. Header is "101101". Reference voltages for OUT1 and OUT2 are 3V and 2V, respectively.

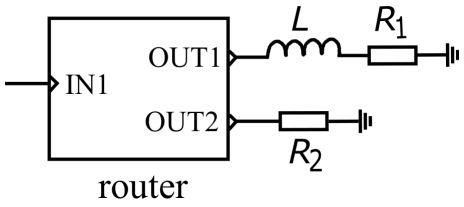


Figure 3.12: Loads connected to a router which has one input port IN1 and two output ports OUT1 and OUT2.

patching and the repacketization in experiments relies on autonomous clock synchronization achieved by the embedded second-order controlled model.

3.5.5 Ohmic-inductive loads

In what follows, we place an inductor (L) in series with R_1 in order to investigate the router output with inductive loads. As illustrated in Fig. 3.12, ohmic-inductive loads (R_1 and L) are connected to OUT1 and a resistive load (R_2) is connected to OUT2. Also, storages are installed in the router for complete repacketization of packets. In experiments, 1000 μF capacitors are deployed and the mixer frequency is set at 48.82 kHz. In addition, different values of inductance are given as 0 μH, 10 μH, 47 μH, and 100 μH. The experimental results are exhibited in Fig. 3.13, where CLKIN is not shown for brevity. In Figs. 3.13(b), 3.13(c), and 3.13(d), impulses are observed on some falling edges of OUT1. From the detailed waveforms of OUT1 in

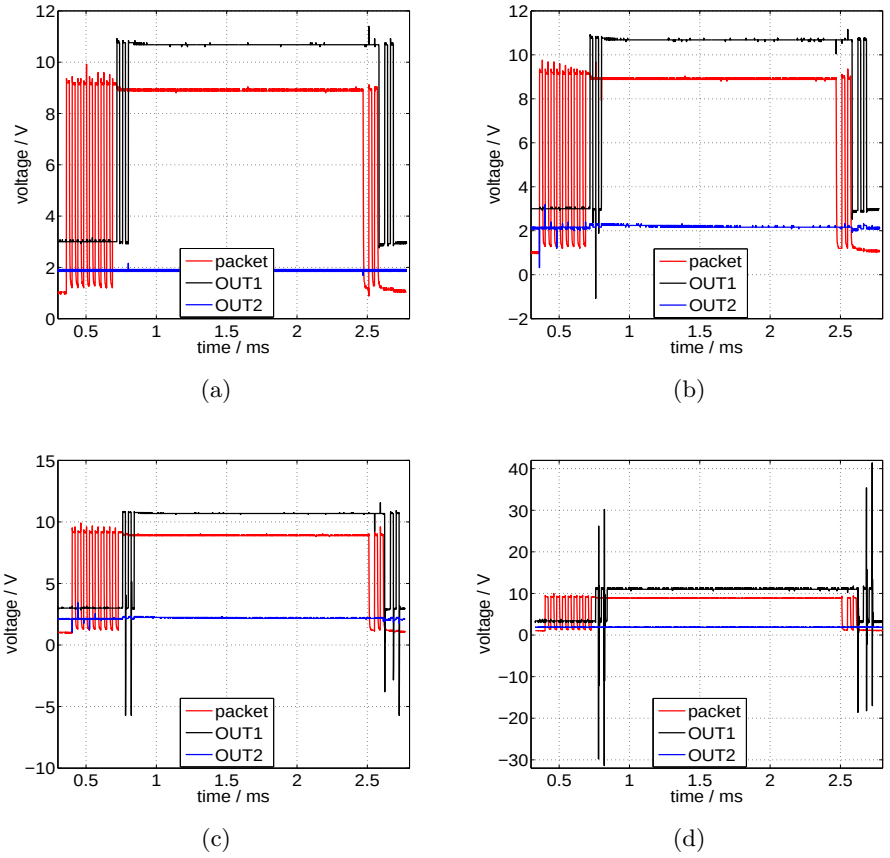


Figure 3.13: Input and output of the router with ohmic-inductive loads. Header is "101011". Reference voltages for OUT1 and OUT2 are 3V and 2V, respectively.(a) $L = 0$ μH; (b)$L = 10$ μH; (c) $L = 47$ μH; (d)$L = 100$ μH.

Fig. 3.14, the impulses are confirmed as oscillations. In addition, the results in Fig. 3.14 suggest that the larger the value of inductance, the greater the peak value of the oscillation. The oscillations are caused by the inductor in the loads and the capacitors as storages. Given the oscillations, we take only resistive loads into account in the current work for concentrating on the verification of power packet dispatching. In future, the power factor correction of inductive loads are reasonable in the application of power packet dispatching.

In the next step, whether the inductive loads at one port will affect the router output at other ports is of concern. For this reason, we change the

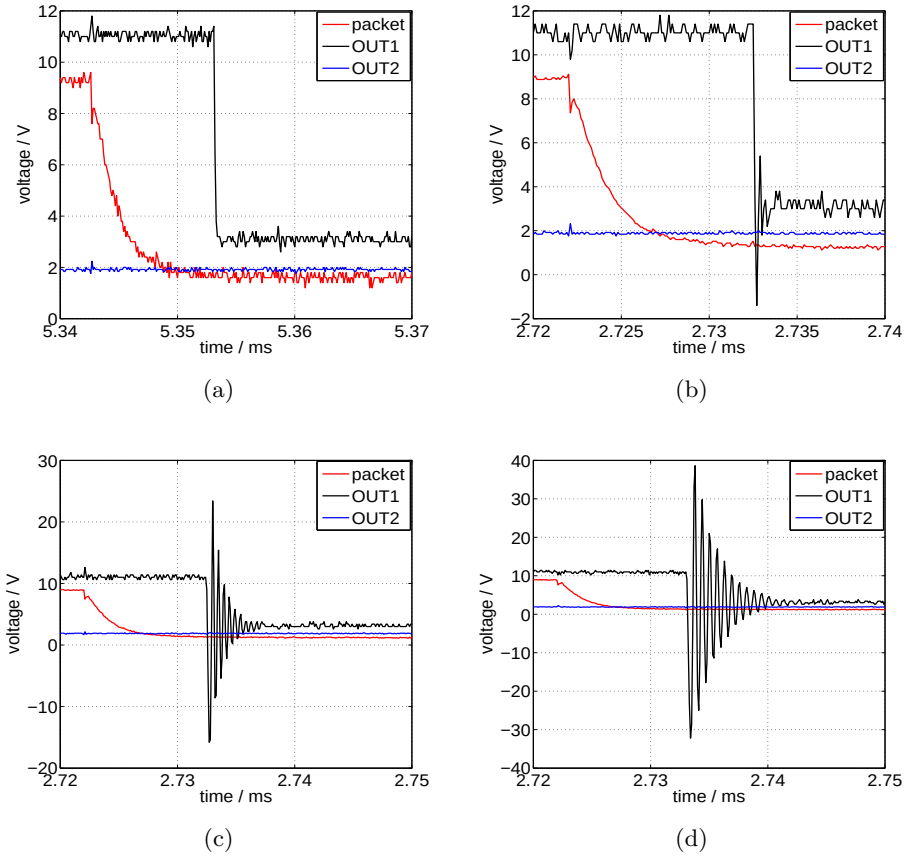


Figure 3.14: Part of the input and output of the router with ohmic-inductive loads. The results are focused on the falling edge of the end of the payload. (a) $L = 0$ μH; (b)$L = 10$ μH; (c) $L = 47$ μH; (d)$L = 100$ μH.

header of a packet to "101101" and observe the router output at OUT2. The results for $L = 47$ μH are shown in Fig. 3.15. It is clear that no oscillation appears at OUT2. Thus, one may conclude that inductive loads at one router output port will not affect the router output at other ports.

3.6 Summary

A second-order controlled model of a digital clock synchronization method was established in this chapter. The settling time of the second-order controlled clock synchronization was confirmed to be five reference clock cycles which is relatively shorter than the settling time of the first-order controlled

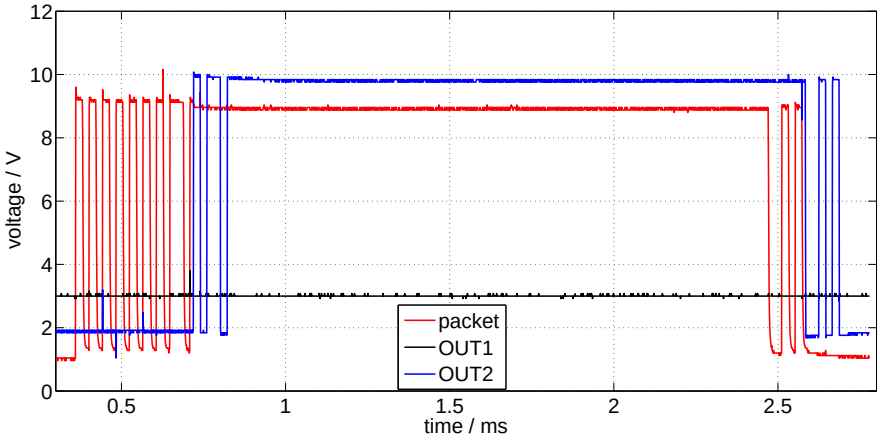


Figure 3.15: Input and output of the router with ohmic-inductive load 2. Header is "101101". $L = 47$ μH. Reference voltages for OUT1 and OUT2 are 3V and 2V, respectively.

clock synchronization. Then the stability of the second-order controlled model was analyzed considering the application of the model in the power packet dispatching system. Embedding the model into a router, autonomous clock synchronization between the mixer and the router was achieved. Then correct power packet dispatching and complete repacketization based on autonomous clock synchronization were demonstrated. The novelty lies on the fact that the clock synchronization between the mixer and the router in a power packet dispatching system is achieved based on the second-order controlled model. The clock synchronization is achieved using the preamble which is generated from power sources, i.e., power is included in the carrier of information. In addition, power packet dispatching under the condition of ohmic-inductive loads was also discussed in this chapter. Besides the success in power packet dispatching and repacketization, oscillations were observed in the corresponding router output.

Considering the future application of the power packet dispatching system, expansion of the system into a network system is desired. Accordingly, more than one mixer and one router may be included in an expanded system. In such a system, power packets may be generated based on different clock frequencies. Also, power packets transmitted from different mixers may exist in one router simultaneously. Moreover, it is possible that these packets

have same attached dispatching information. As a consequence, the power packet dispatching will become more complicated and adequate regulations will be required. In this context, the following chapter will investigate power packet dispatching under different scenarios in a simple expanded system.

Chapter 4

Power Packet Dispatching Under Congestion

4.1 Prologue

This chapter is devoted to investigating the feasibility of system expansion based on autonomous clock synchronization. For this purpose, we will introduce a simple expanded system which includes two mixers and one router. Besides, the second-order controlled model is embedded in the router for achieving autonomous clock synchronization. In this system, power packet dispatching will become more complicated and congestion of packets may exist. For example, it is possible that power packets generated in two mixers exist in the router simultaneously and they have same destination or same demand of storages. Power packet dispatching under different scenarios in the simple expanded system will be discussed. At last, a simple conclusion will be made in the end of this chapter.

4.2 Expanded power packet dispatching system

It has been mentioned previously that expanding the power packet dispatching system from the standpoint of network design is desired for power distribution in future. In order to validate the feasibility of system expansion, power packet dispatching in an expanded system is investigated. In the previous chapter, power packet dispatching in a basic system has been verified, which is based on autonomous clock synchronization, i.e., second-

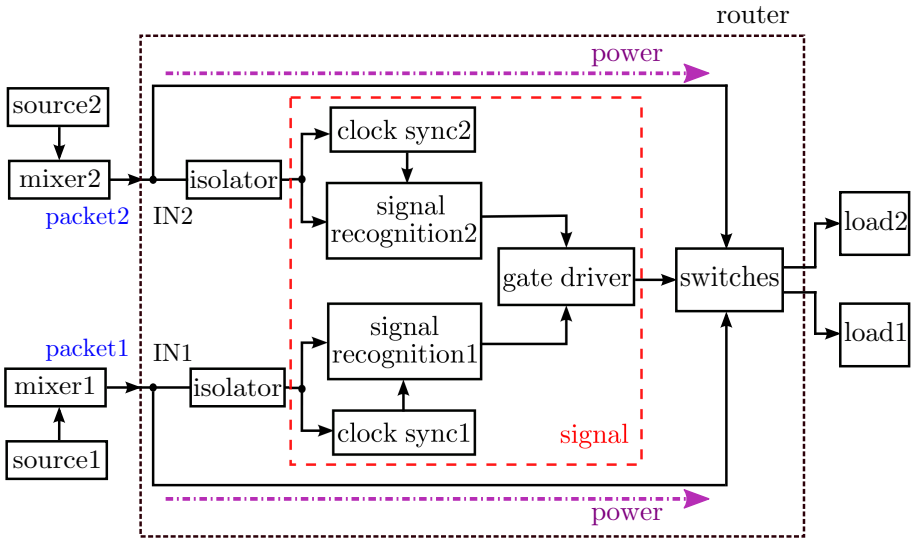


Figure 4.1: Block diagram of original power packet dispatching system in experiments.

order controlled clock synchronization. Likewise, power packet dispatching based on autonomous clock synchronization in an expanded system will be discussed here. For this purpose, the system block illustrated in Fig. 4.1 is introduced, in which two DC power sources, two mixers, one router, and two resistive loads are included. In the system, each mixer is connected with the router through a power line. The generation and transmission of power packets are independent in two mixers. Moreover, the packets generated in mixer1 and mixer2, named as packet1 and packet2, are transmitted to input port 1 and input port 2 of the routers (IN1 and IN2), respectively. In the router, two groups of clock synchronization block and signal recognition block, namely clock sync1 (2) and signal recognition1 (2) are realized in two FPGA boards (Nexys^{TM}4 Artix-7 FPGA board) separately. They are specified for processing the received packets from IN1 and IN2, respectively. In the setup, the loads are fixed at 10 kΩ to confirm the router operation.

When a power packet is received in the router, the clock synchronization between the mixer and the router is achieved autonomously by the corresponding clock sync block. Thereafter, the packet signal is read in the signal recognition block. Then the recognized signal is processed to control the gate driver of power devices for switching circuit. Once the specified switch is turned on, the power of payload will be transferred to the des-

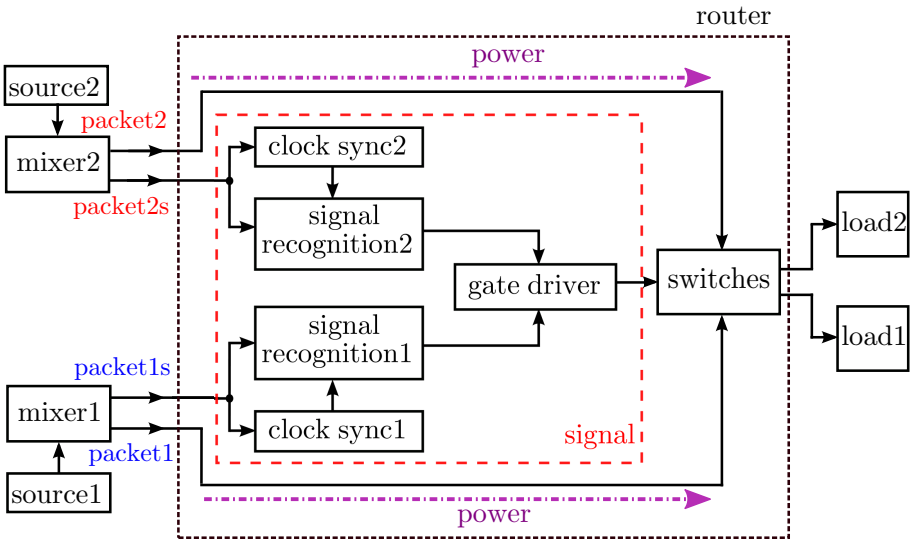


Figure 4.2: Block diagram of modified system.

ignated load. In this manner, the power packet dispatching is completed through the router.

An experiment of power packet dispatching is carried out in the original system. It is found that jitter exists in the voltage of power packets when the packets from two mixers exist in the router simultaneously. The jitter may lead to failure in autonomous clock synchronization. Thus, given the feasibility of the clock synchronization algorithm, the original system needs to be modified as in Fig. 4.2. In the modified system, another set of signal, named as packet1s (2s) are produced directly from FPGA boards in mixers for achieving the clock synchronization. Packet1s (2s) and packet1 (2) are generated simultaneously with same shape of signal waveform. The difference between them is that packet1s (2s) do not carry power from power sources while packet1 (2) do. In this way, the clock synchronization is independent to packet1 (2). Furthermore, as shown in Fig. 4.3, each combination of a mixer and a source in Fig. 4.1 is replaced by an FPGA board (Nexys3 Spartan-6 FPGA board) named as FPGA1 and FPGA2, for concentrating on the confirmation of algorithm and process in experiments. In the following experiments, we consider the FPGA boards as the mixers. At the setting, packet1 (2) and packet1s (2s) become exactly the same and the power of packet1 (2) is not exactly sent by power sources, but by FPGA boards. Moreover, the voltage of signals can be set by the FPGA boards and it is

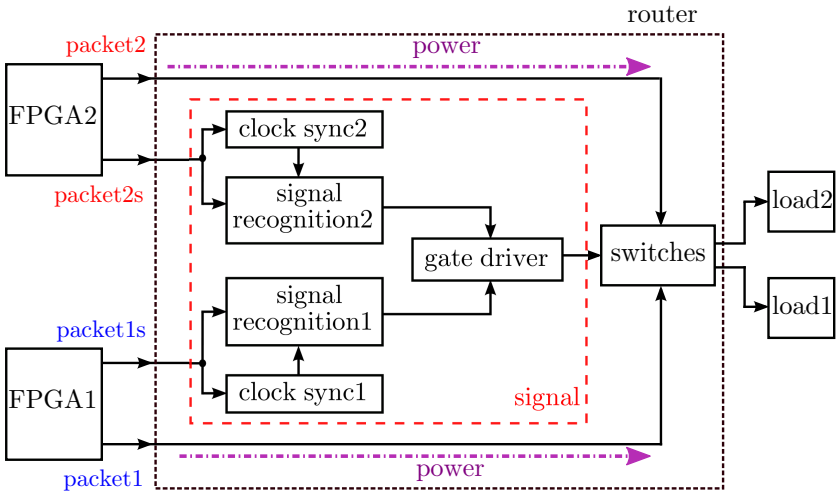


Figure 4.3: Block diagram of modified system in experiments.

set at 3.3V in experiments. In addition, the modified system can remove the isolators in Fig. 4.1 because packet1s (2s) transmitted to FPGA boards (NexysTM4 Artix-7 FPGA board) in the router are generated in FPGA boards (Nexys3 Spartan-6 FPGA board). However, these modifications do not loose the generality of the confirmation of algorithm in hardware.

4.3 Verification of power packet dispatching

The packet dispatching is investigated under different scenarios which can be divided into four main categories: (1) packets generated in one mixer; (2) packets generated in two mixers based on same and different frequencies; (3) packets generated in two mixers with same address signal; (4) packets generated in two mixers with same source signal. Figure 3.5 shows the setting of a power packet adopted in experiments. Two kinds of address signal, "11" and "01", are employed in experiments, which indicate that the packets are dispatched to output port 1 and output port 2 of the router (OUT1 and OUT2), respectively. In addition, the mixer clock frequency ($f_{\text{mixer}i}$, i=1 or 2) is determined by a parameter "$fset_i$" (i=1 or 2) as in Eq. (3.8).

4.3.1 Packets generated in one mixer

Power packet dispatching in the case that packets are generated in one mixer is considered first. Without loss of generality, it can be assumed that packet1 is generated with header (H1) as "101011". The results in Fig. 4.4 demonstrate that packet1 is dispatched to OUT1 as expected. It should be noted that signals are plotted in Fig. 4.4 based on different reference voltages, i.e., the reference voltages for packet1s, packet1, OUT1, and CLKIN1 are 1V, 0.5V, 1V, and 0V, respectively. The signal "CLKIN1" is considered as the router clock signal in this packet duration. In addition, it is worth mentioning that no storages are installed in experiments in this chapter. As a result, the repacketized packet is around six bits shorter than the received packet as can be observed in Fig. 4.4. The reason why the bit number is reduced has been explained in Sect. 3.5.4.

As shown in Fig. 4.4, the bit length of the preamble is equal to the bit length of the packet signal in the modified system. Similar to the power packet dispatching in Sect. 3.5.2, there also exists a range of f_{mixer} within which power packets can be dispatched correctly. Through experiments, it is found that power packet dispatching succeeds in the modified system for $fset \in [8, 16]$, i.e., $f_{\text{mixer}} \in [763\text{ Hz}, 195\text{ kHz}]$. Compared to the range of f_{mixer} under same condition in Sect. 3.5.2 ($f_{\text{mixer}} \in [24.4\text{ kHz}, 195\text{ kHz}]$), the range here is widely expanded. We speculate the reason is that the preamble used for clock synchronization here is generated directly from an FPGA board, i.e., no noise is introduced by switching operation. However, the reason is not our concern at the moment.

4.3.2 Packets generated independently in mixers

Dispatching of two packets generated in different mixers are considered next. That is the packets received at IN1 and IN2 exist simultaneously in the router. Before analyzing the experimental results, it is necessary to introduce the switches in the router. As presented in Fig. 4.5, there are two sets of switches in the router. The left set (switches A to D) is designed to select the storages for each received packet according to the source signal in the header ('0' and '1' correspond to storage1 and storage2, respectively). While the right set (switches A' to D') is for selecting the router output ports (OUT1 and OUT2) based on the address signal ('11' corresponds to OUT1 and '01' to OUT2). Each packet is dispatched to the selected port.

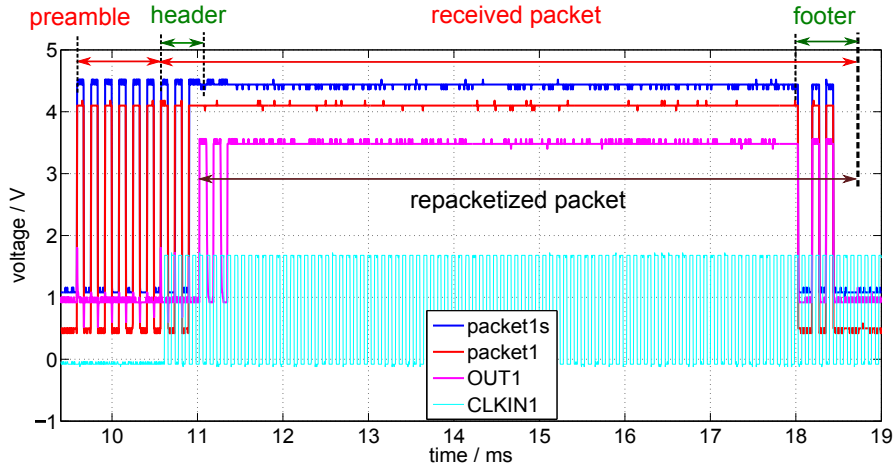


Figure 4.4: Dispatching of packet1 with H1: "101011". $f_{\text{mixer1}} = 12.2$ kHz.

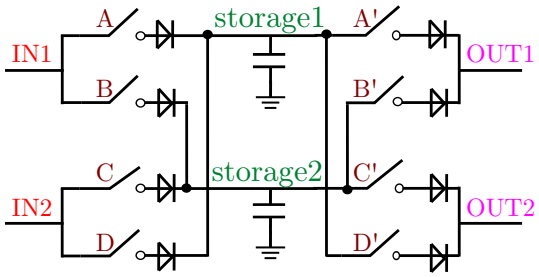
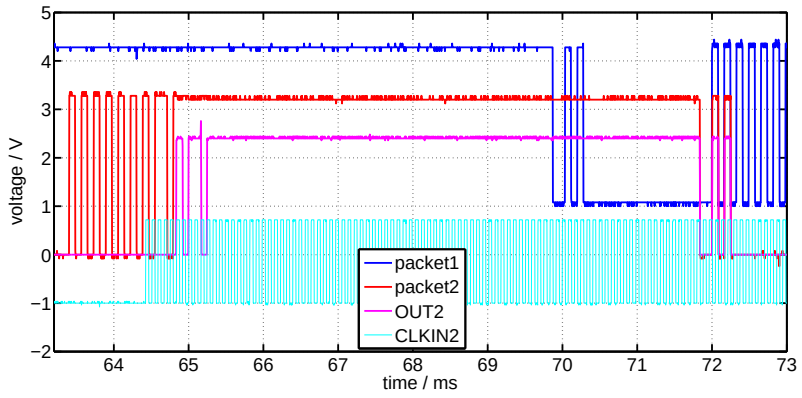
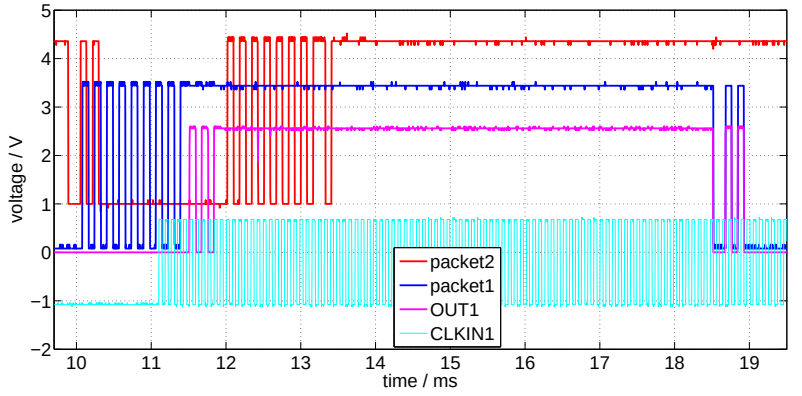


Figure 4.5: Block diagram of switches and storages in the router.

To begin with, $fset_1 = fset_2 = 12$ are set to discuss the dispatching of packets generated based on same frequency. The corresponding experimental results are displayed in Fig. 4.6, where the reference voltages for packet1, packet2, OUT1 (2), and CLKIN1 (2) are 0V, 1V, 0V, and -1V, respectively. This setting of reference voltages also applies to the following figures in this chapter. As seen from the figure, the two packets are of same bit length since the bit length of packet signal equals to the mixer clock period. The headers of the two packets are annotated in the caption as H1="101011" and H2="101101". Hence, packet1 is supposed to be dispatched to OUT1 and packet2 to OUT2. The dispatching of packet2 is confirmed at OUT2 in Fig. 4.6(a) while the results in Fig. 4.6(b) illustrates packet1 is dispatched to OUT1 correctly as well. In addition, it can be observed that the high voltage of packet1 is 3.44V and that of OUT1 is 2.56V. The voltage differ-



(a)

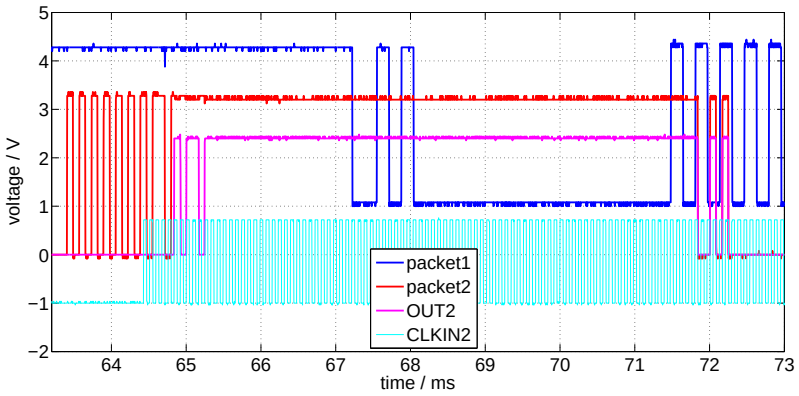


(b)

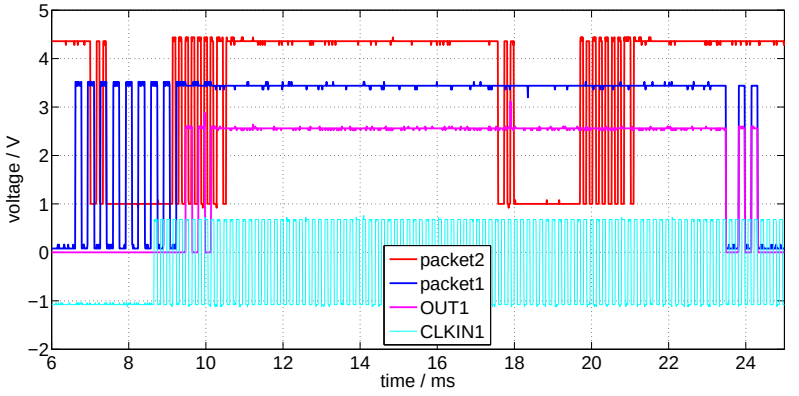
Figure 4.6: Dispatching of two packets generated based on same mixer clock frequency. H1: "101011", H2: "101101", $fset_1 = fset_2 = 12$.

ence is caused by the switches. As shown in Fig. 4.5. a diode is installed behind each individual switch in order to avoid the reverse current when the switches are turned on. As a consequence, the voltage difference between the input and output of the router depends on the threshold voltage of the diodes.

We continue to discuss the dispatching of packets generated in two mixers with independent frequencies. The headers of packets are kept the same butthe mixer frequencies are changed by setting $fset_1 = 13$ and $fset_2 = 12$. In Fig. 4.7(a), it can be observed that packet2 is dispatched to OUT2. Meanwhile, the dispatching of packet1 to OUT1 is confirmed in Fig. 4.7(b).



(a)



(b)

Figure 4.7: Dispatching of two packets generated based on different mixer clock frequencies. H1: "101011", H2: "101101", $fset_1 = 13$, $fset_2 = 12$.

Additionally, it is obvious that the bit length of packet1 is longer than that of packet2, which can be explained by substituting $fset_1 = 13$ and $fset_2 = 12$ into Eq. (3.8). Given the above analysis, one may conclude that no matter the two mixer clock frequencies are same or not, the packets generated in two mixers can be dispatched correctly when they exist simultaneously in the router. However, it should be noted that the packet dispatching here is discussed under the condition that the packets from different mixers have different source signal and address signal.

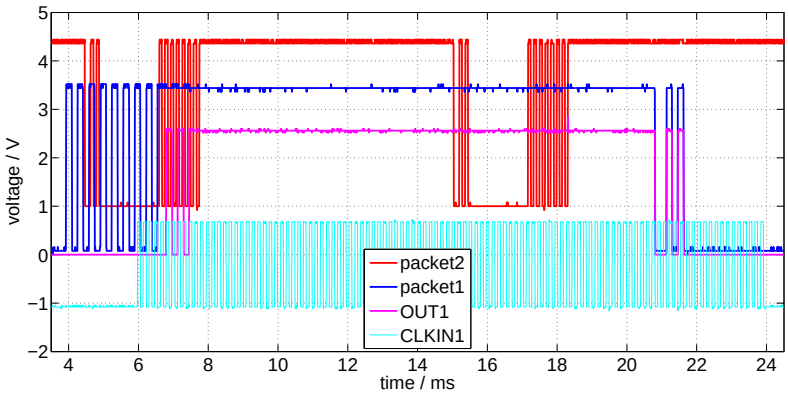


Figure 4.8: Dispatching of two packets attached with same address signal. H1: "101011", H2: "101111", $fset_1 = 13$, $fset_2 = 12$.

4.3.3 Packets generated in mixers with same destination

When packets generated in different mixers exist simultaneously at the router and are of same address signal, congestion of packets may appear at the router output ports. In this case, a rule "first come, first serve" should be complied with for packet dispatching. By the rule, the packet, whose header is first recognized completely, will be dispatched while other packets received in this packet duration will be discarded. For example, we set the address signal of packet1 and packet2 same as "11" and the experimental results are shown in Fig. 4.8. It is obvious that the header of packet1 is recognized earlier than the header of packet2 and the bit length of the signal at OUT2 is same as the bit length of signal in packet1. Therefore the dispatching of packet1 to OUT1 is confirmed. When the packet1 is completely dispatched, the following packet whose header is recognized will be dispatched. In this manner, the congestion caused by same address signal is solved.

4.3.4 Packets generated in mixers toward same storage

At last, we focus on the case when packets generated in two mixers exist simultaneously in the router and have same source signal. As previously mentioned, storages in the router are selected by the source signal. Thus, congestion of packets may arise at storages in this case. When it happens, the power of packets from different mixers are stored in the same storage (capacitor). This will generally cause safety issue in the power packet dis-

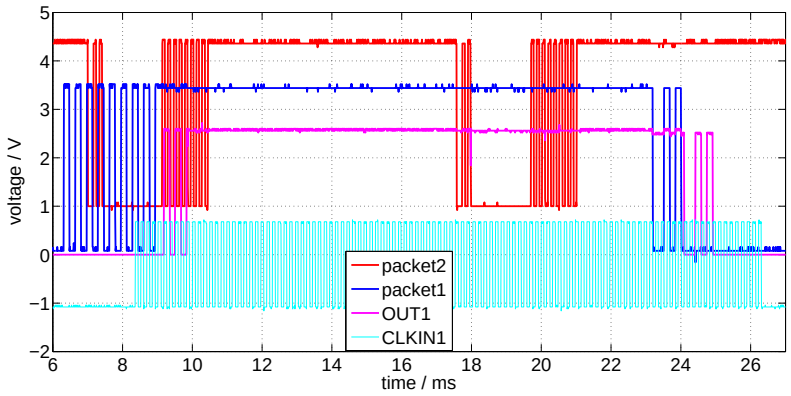


Figure 4.9: Dispatching of two packets attached with same source signal. H1: “101011”, H2: “101011”, $fset_1 = 13$, $fset_2 = 12$.

patching system. For instance, if the two input packets are of different voltages, the capacitor will be charged at high voltage and thus the low voltage packet can not be stored simultaneously.

In our experiments, the packets are generated by FPGA boards, and thus the voltages of packets are same at around 3.3V. Correspondingly, the unsafe issue mentioned above does not exist here. However, the effect of same source signal on the packet dispatching can still be observed in Fig. 4.9, where the header of packets from different mixers are set the same as H1=H2=“101011”. Compared to Fig. 4.8, still, only packet1 is dispatched to OUT1 in Fig. 4.9 because of the same address signal. Whereas, it can be observed in Fig. 4.9 that the packet is completely repacketized. Let us recall that complete repacketization requires installed storages in the router. Referring to the reasons of incomplete repacketization in Sect. 4.3.1, the correct repacketization of the footer here can be explained. That is the power of packet2 is supplied to repacketize bits ‘1’ during the footer of packet1 since power of both packets are stored in storage1.

4.4 Summary

This chapter dealt with the feasibility of system expansion based on autonomous clock synchronization. Power packet dispatching in a modified system were discussed under four typical scenarios. It was demonstrated

that the power packet dispatching system is possible to be extended to transfer multi packets in the network without loosing the concept of power packet dispatching.

The basic function of a power packet dispatching system as dispatching power packets was verified in experiments and the feasibility of system expansion based on autonomous clock synchronization was also validated. In the next step, one advantageous function of the power packet dispatching system will be considered. The concept of safety of power packet dispatching will be proposed in the next and final main chapter.

Chapter 5

Safety of Power Packet Dispatching

5.1 Prologue

In this chapter, the question under discussion is one advantageous function of a power packet dispatching system, i.e., the safety of power packet dispatching. In the beginning, the motivation of proposing the concept of safety will be explained and modulation of power packets will be proposed for achieving the safety. Then the principles of the differential chaos shift keying (DCSK) scheme will be summarized as preparation for the introduction of packet modulation. After that, packet modulation will be explained in detail, which covers partial packet modulation and whole packet modulation. The power transferred after modulation will also be discussed. In the end of the chapter, a brief conclusion will be given.

5.2 Concept of safety

The concept of safety of power packet dispatching is proposed covering information safety and power safety. The concept has not been figured out before for dispatching electric energy, until the power packet dispatching was introduced. To be more specific, the information safety refers to protecting the information of packets from attackers while the power safety is considered from the perspective of keeping the loads safe regarding power. At first, for the system in Fig. 1.1, when an attacker existing between the

mixer and the router receives a power packet, he or she may deduce the packet signal and accordingly obtain some useful information. For instance, by recognizing the address signal, the attacker may learn the time and the amount of power consumption of the corresponding load. In this sense, the safety of information with power packet is very weak. We can easily imagine that the attacker may even change the packet signal purposely, send the tampered packet to the router, and give rise to wrong power distribution. In this way, the attacker may lead to damage to the running system. Considering the consumers' privacy and the system stability, the information needs to be protected from attackers and modulating information tags of power packets before sending them is a possible solution. Next, on the loads side the supplied power should be lower than their rated power. For this reason, the rescaling of the transferred power of packets is desired, which can be realized by modulating the payload since the payload carries the power of packets. In other words, modulation of payload in packets can keep the loads safe regarding power.

The similarity between a power packet dispatching system and a communication system has been mentioned in Sect. 1.1. Therefore, we can refer to the modulation schemes used in communication systems for protecting the information of packets. Moreover, in the power packet dispatching system, power packets are generated in digital form and thus digital modulation schemes are required. The use of chaos in communication systems is appealing due to several intrinsic properties of chaotic signals, such as aperiodic and broadband. Hence, many chaos-based communication systems have been proposed and analyzed [39–51], among which the chaos shift keying (CSK) scheme with coherent detection was firstly proposed in [40, 42] to encode digital symbols with chaotic signals. However, the sensitive dependence of chaotic signals upon initial condition makes it very difficult to replica signal in the receiver [46]. As thus, non-coherent detection of received signal is advantageous over coherent detection. The differential chaos shift keying (DCSK) scheme is a typical non-coherent chaos-based communication scheme [44], which also solves the problem of threshold shift in non-coherent CSK system [46]. In addition, the DCSK scheme is much easier compared to some advanced schemes such as the code division multiple access (CDMA) scheme [52]. As a result, the DCSK scheme is adopted to modulate the information tags for the purpose of protecting the information

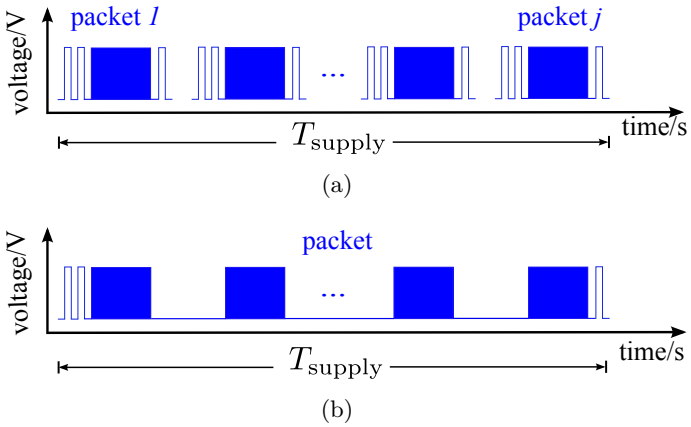


Figure 5.1: Adjusting the amount of transferred power by (a) pulse density modulation of a train of power packets; (b) pulse width modulation of the payload in a equivalent big packet. T_{supply} is the determined time duration when the power packets are transferred.

from attackers,

With respect to power, a train of power packets are generated in a determined time duration T_{supply} as illustrated in Fig. 5.1(a) so that demanded power can be supplied to loads. In the case that the packets are exactly the same, we can manage the total transferred power by applying pulse density modulation (PDM) to the train of packets. In this sense, the power safety can be achieved through the pulse density modulation. Furthermore, given the fact that the information tags of packets do not carry power, the pulse density modulation of the train of packets is equivalent to applying pulse width modulation (PWM) of the payload in a big packet as shown in Fig. 5.1(b). Here, we refer to the modulation of the payload using PWM as the premodulation and the resulting packet as the premodulated packet. From now on, we take the equivalent big packet as the packet we will discuss about. As previously mentioned, the power packet is produced by switching on and off the selected source in the mixer and noise may arise in the packet signal due to the switching operation. It is clear that more switching operation will be performed when the premodulation is introduced. Consequently, more noise may arise in packet signal during the payload. Worse still, the noise existing in the packet may result in incorrect signal recognition in the router and further wrong or failed packet dispatching. As a solution of reducing the influence of such kind of noise on power packet

dispatching, we further modulate the payload of the premodulated packet using the DCSK scheme because the chaos-based modulation can spread the spectrum of noise. Based on the above discussion, we finally propose the whole packet modulation, in which premodulation of a packet is carried out first for achieving the power safety. Then the whole premodulated packet is modulated using the DCSK scheme in order to achieve the information safety and reduce the effect of the noise.

5.3 Differential chaos shift keying

The operating principles of the differential chaos shift keying (DCSK) scheme were reported in [44, 46]. The block diagram of a DCSK system is presented in Fig. 5.2 which includes a DCSK modulator and a DCSK demodulator. In the DCSK modulator, every bit period (T_b) is divided into two equal time slots so that every information bit b_l ($l \in \mathbb{N}_1$ denotes the serial number of bits) is represented by two consecutive chaotic signal samples: reference sample and data sample. As an example, Fig 5.3 shows the representation of one bit b_1='0' using the DCSK scheme. As seen from the plot, T_b=2×βT_x, where T_x is the time interval between two consecutive points of the chaotic sample. 2β ($\beta \in \mathbb{N}_1$) is the spreading factor in DCSK. In the first time slot (0 to βT_x), the reference sample ($\{x_j\}$, $j \in \mathbb{N}_1$ indicates the serial number of sample points) is transmitted and in the second time slot (βT_x to $2\beta T_x$), the data sample ($\{-x_{j-\beta}\}$) is sent. Here, we can see that for bit '0', the data sample is inverted to the half bit period delayed reference sample. Whereas, in the case of b_l='1', the data sample will be identical to the delayed reference sample. In this manner, the data sample carries information in the DCSK scheme. In the DCSK demodulator, r_j is the received signal and y_l stands for the correlation of r_j and $r_{j-\beta}$ at the end of the l-th bit duration. Comparing y_l with the threshold value in the threshold detector, the transmitted bit can be recovered as b'_l. It is worth noting that according to the principle of the DCSK demodulator [46], the spreading factor (2β) is essential to recover the transmitted bit correctly.

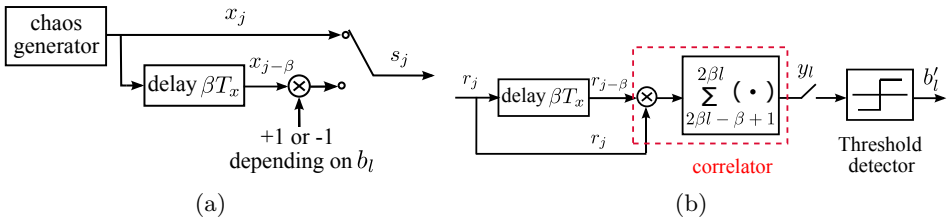


Figure 5.2: Block diagram of a non-coherent single-user DCSK system. (a) modulator. x_j is the chaotic signal sample generated in the chaos generator. b_l is the bit to be transmitted and s_j is the modulator output. (b) demodulator. r_j is the received signal and b'_l is the recovered l-th bit.

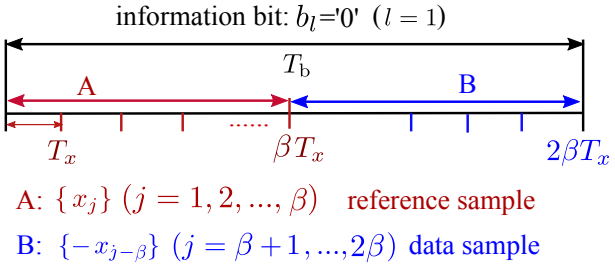


Figure 5.3: Representation of one bit b_1 (b_1='0') in the DCSK scheme.

5.4 Partial packet modulation

In order to protect the information of power packets from attackers, we propose to modulate the preamble and the header in packets, namely, partial packet modulation. As introduced in Sect. 1.2, the preamble is designed to achieve the clock synchronization for power packet dispatching. It is thus important to modulate the preamble during packet transmission so that the clock information can be protected. The header should also be modulated because it includes some useful information. In this sense, the information safety is possibly established, provided that the preamble and the header are protected.

The schematic diagram of a power packet dispatching system with partial packet modulation is illustrated in Fig. 5.4, where a DCSK modulator and demodulator are embedded in the mixer and the router, respectively. As illustrated in Fig. 5.4, the power packet generated in the mixer is partially modulated by the DCSK modulator. Later, the modulated packet signal is recovered through the DCSK demodulator. As such, the whole packet

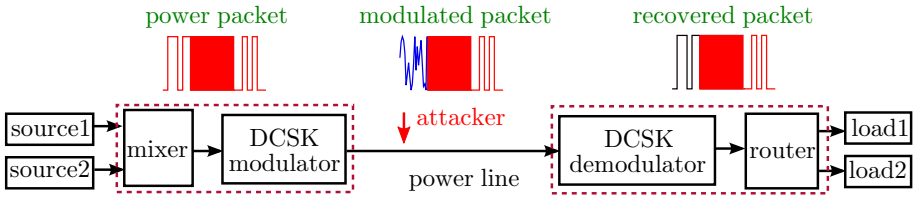


Figure 5.4: Schematic diagram of a power packet dispatching system with partial packet modulation.

can be recovered in the partial packet modulation, not only because the recovered preamble and header suffice to determine the packet dispatching, but also because no modulation of the payload keeps the power of packet unchanged. Additionally, we define the spreading factor (2β) as the key in the partial packet modulation since 2β is critical for correct signal recovery in the DCSK demodulator.

For the purpose of demonstrating the effect of the key on the signal recovery, we build the DCSK modulator and demodulator in Simulink and perform simulation of partial packet modulation. Noise performances of the DCSK scheme over additive white Gaussian noise (AWGN) channels have been discussed in [50, 51, 53–55]. Whereas, at present we assume the channel between the modulator and the demodulator is ideal, i.e., no noise is considered during the packet transmission in simulation. Moreover, in real applications, the limitation of spectrum suitable for communication may be caused by the components of power grid, e.g. the power transformers. This kind of limitation is beyond the scope of discussion because our aim here is to confirm potential ways of protecting the information of power packets. Power packets with the composition as in Fig. 3.5 are adopted in simulation. As mentioned, there are 112 bits of signal in one packet duration including 12 bits of preamble and six bits of header. We also set one bit of '0' as the guard interval between two consecutive packets. Furthermore, the parameters in the DCSK scheme are given as $T_\mathrm{b} = 0.1$ s and $T_x = 0.001$ s, which implies $2\beta = 100$.

Given the above assumptions and settings, simulations of partial packet modulation are performed with different keys in the demodulator. Figure 5.5 shows the modulation and demodulation in partial packet modulation, assuming that the key is given correctly in the demodulator. First, we can see that only the preamble and the header (18 bits of packet signal in total) in

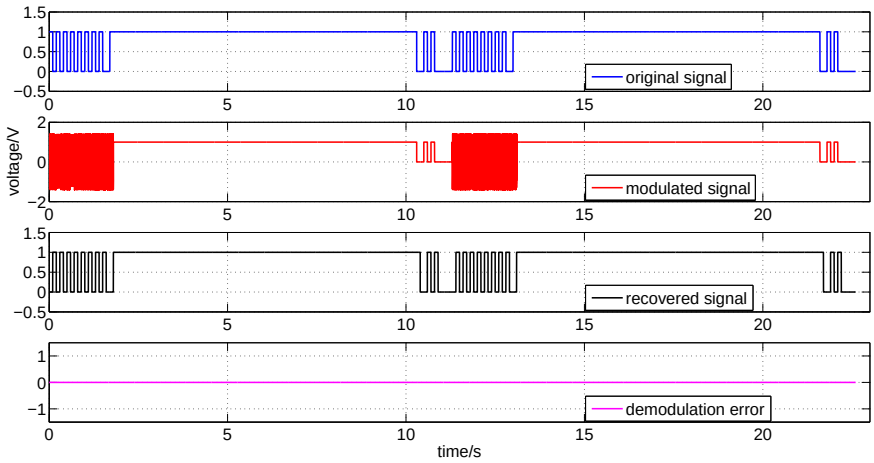


Figure 5.5: Partial packet modulation in simulation with correct key in the demodulator.

one packet are modulated. Then, Fig. 5.6 shows the detail about the modulation, from which it can be confirmed that the data sample is inverted to the reference sample for bit '0' and is identical to the reference sample for bit '1'. Moreover, from Fig. 5.5, it can be observed that the modulated packet signal is recovered without error. However, if an incorrect key such as 98 is given in the demodulator, then as seen from Fig. 5.7, error appears in the demodulation. Based on the above results, one may conclude that if the attacker receives a modulated packet, he can not deduce the packet signal correctly without the key. That is the information safety is achieved by modulating the preamble and the header using the DCSK scheme.

5.5 Whole packet modulation

After achieving the information safety in partial packet modulation, we continue to discuss about the power safety. In particular, we aim to achieve the information safety and the power safety simultaneously. To begin with, the payload of a power packet is modulated using PWM so that the amount of transferred power can be adjusted. The modulation of the payload using PWM is defined as the premodulation of packets. Then, the whole premodulated packet is modulated using the DCSK scheme which contributes

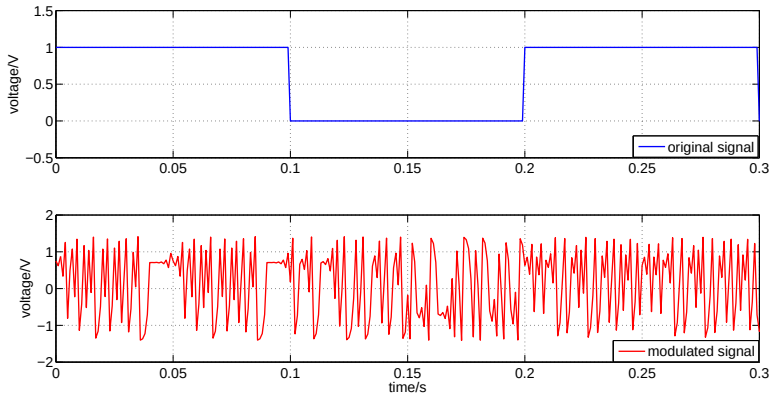


Figure 5.6: Detailed DCSK modulation in partial packet modulation in simulation. Each bit period ($T_\mathrm{b} = 0.1\,\mathrm{s}$) is divided into two equal time slots (0.05 s). The data sample (chaotic signal sample in the second time slot) is identical or inverted to the reference sample (chaotic signal sample in the first time slot) depending on the bit '1' or '0'.

to protection of the information of packets and to reduction of the effect of noise on the power packet dispatching. Accordingly, Fig. 5.8 shows the block diagram of the power packet dispatching system with whole packet modulation.

5.5.1 Information safety

In whole packet modulation, we still try to achieve the information safety by modulating the information tags of the premodulated packet using the DCSK scheme. In addition, the payload of the premodulated packet is also modulated using the DCSK scheme for reducing the influence caused by noise. In this method, it is necessary to check the information safety first. It should be stressed that the payload carries electric power as physical quantity, and thus the DCSK modulator needs to be modified as in Fig. 5.9 for transferring power in whole packet modulation. In the modified DCSK modulator, after the conventional DCSK modulation, the modulated signal is multiplied by the absolute voltage amplitude of the power packet. Here, we assume the voltage of the packet signal is '$+z$' or '$-z$' in volts. The packet signal of amplitude $+z$V or $-z$V are recognized as bit '1' or '0', respectively.

Adopting the modified DCSK modulator, we carry out simulations of

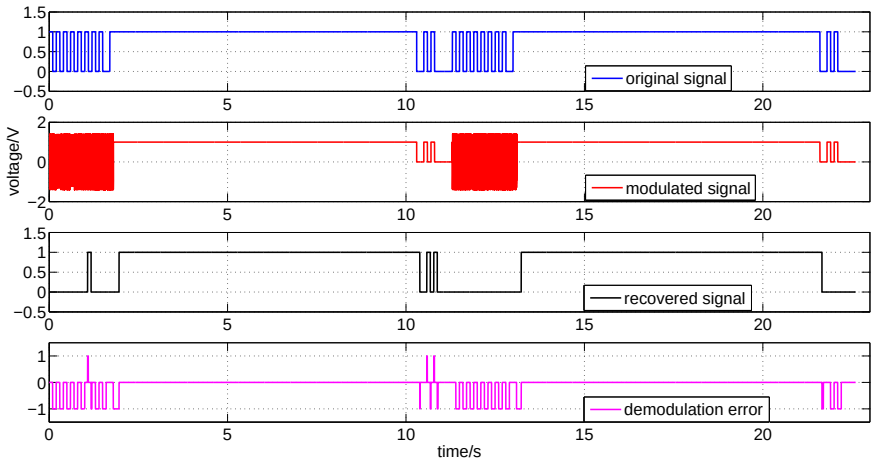


Figure 5.7: Partial packet modulation in simulation with wrong key in the demodulator.

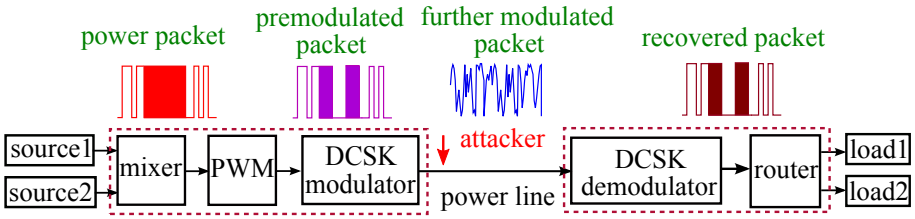


Figure 5.8: Block diagram of the power packet dispatching system with whole packet modulation.

whole packet modulation to discuss about the information safety. The parameters are set as $T_{\mathrm{b}} = 0.1\,\mathrm{s}$, $T_{\mathrm{sam}} = T_x = 0.001\,\mathrm{s}$, $N_{\mathrm{b}} = 200$, and $2\beta = 100$. T_{sam} is the system sampling period and N_{b} represents the bit number of the payload. Also, the duty ratio of PWM in the premodulation is defined as D ($D \in [0, 1]$). In these conditions, the amplitude spectra of the DCSK modulator output signal (s_j) with different values of D in premodulation are plotted in Fig. 5.10. In this figure, for some values of D, especially for those which are far away from 0.5, rough periodization can be observed in the shape (envelope) of the amplitude spectrum. It is well known that in the field of sampling theory [56], sampling in the time domain gives rise to periodization in the associated frequency domain, where sampling interval T_{sint} corresponds to a periodization with period of $f_{\mathrm{period}} = 1/T_{\mathrm{sint}}$. Here,

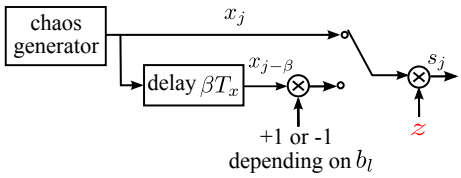


Figure 5.9: Block diagram of a modified DCSK modulator in whole packet modulation.

we can consider whole packet modulation as a special sampling process: the premodulated packet signal is sampled first with $T_{\text{sint}} = \beta T_x$ and then each signal sample is represented by β points of chaotic sample. According to $T_x = 0.001\,\text{s}$ and $\beta = 50$, it can be deduced that a periodization with period of $f_{\text{period}} = 1/\beta T_x = 20$ Hz exists in the frequency domain, as can be found in Figs. 5.10(a) or 5.10(e). In this sense, the key 2β may be estimated by the attacker directly from the amplitude spectrum of the modulated packet signal. This may eventually lead to unsafety of information in whole packet modulation.

From the above analysis, it is found that the periodization in frequency domain should be hidden for achieving the information safety. Referring to the sampling theorem, we can change the sampling interval T_{sint} to overlap the adjacent envelopes so that the periodization is hidden. Correspondingly, the DCSK scheme needs to be modified. By contrast with the conventional DCSK scheme in which each transmitted bit is mapped to two chaotic samples with equal length, in the modified DCSK scheme each bit is mapped to two chaotic samples with different lengths. The spreading factor 2β remains to denote the number of points of chaotic sample representing one bit. In addition, a new parameter is defined as partial spreading factor α ($\alpha \in \mathbb{N}_1$ and $\alpha < 2\beta$) which indicates the first part of each bit is represented by α points of chaotic sample. Given the relationship between α and β, the DCSK scheme can be modified in two ways.

In the beginning, we set $\alpha > \beta$ and take the $2\beta - \alpha$ points of chaotic sample in the second time slot as the data sample. The representation of one bit (b_1='0') in this modified DCSK scheme is exemplified in Fig. 5.11. We can see that the data sample is inverted to the first $2\beta - \alpha$ points of the reference sample because of b_1='0'. More generally, the modulator output signal s_j can be described as in Eqs. (5.1) and (5.2). It should be noticed that b_l here represents the l-th bit of the premodulated packet signal. The

DCSK demodulator needs to be modified correpondingly as in Fig. 5.12(b). For b_l= '1',

$$s_j = \begin{cases} zx_j, & (l-1)2\beta+1 \le j \le (l-1)2\beta+\alpha, \\ zx_{j-\alpha}, & (l-1)2\beta+\alpha+1 \le j \le (l-1)2\beta+2\beta. \end{cases} \tag{5.1}$$

For b_l='0',

$$s_j = \begin{cases} zx_j, & (l-1)2\beta+1 \le j \le (l-1)\beta+\alpha, \\ -zx_{j-\alpha}, & (l-1)2\beta+\alpha+1 \le j \le (l-1)\beta+2\beta. \end{cases} \tag{5.2}$$

A simulation of whole packet modulation using the modified DCSK scheme with $\alpha = 70$ is performed. At first, the modified DCSK modulation is shown in detail in Fig. 5.13. From the figure, it is confirmed that the data sample in each bit period, i.e., the last 30 points ($2\beta - \alpha = 30$), is identical to or inverted to part of the reference sample (the first $2\beta - \alpha = 30$ points in each bit period) depending on the transmitted bit. Figure 5.14 illustrates the modulation and demodulation of the whole premodulated packet, where D is fixed at 0.2 in the premodulation. It can be seen in Fig. 5.14 that the premodulated packet signal is recovered correctly when both α and 2β are known in advance in the demodulator. We refer to α and 2β as two keys in the whole packet modulation. Next, the information safety based on the modified DCSK scheme is considered. Part of the amplitude spectra of s_j with different α are plotted in Fig. 5.15 so as to analyze the effect of α on the information safety. Comparing Figs. 5.15(a) and 5.15(b) to Fig. 5.10(a), it can be found that within the range of $\beta < \alpha < 2\beta$, the greater the α, the more overlapped the envelopes of the amplitude spectrum. In other words, it becomes more difficult to estimate keys from the spectrum directly. Additionally, in the conventional DCSK demodulator, the bit error rate (BER) can be improved by increasing the spreading factor [53]. Here, the BER can be improved by increasing the length of the data sample ($2\beta - \alpha$) in this modified DCSK scheme. As a consequence, a trade off between the BER and the degree of overlap in envelopes of the amplitude spectrum should be made to determine the value of α. It is worth mentioning again that more overlapped envelopes of spectrum corresponds to more difficulty in estimating the keys. Besides, the amplitude spectrum of s_j for $D = 0.4$ with different α are exhibited in Fig. 5.16. Still, no obvious periodization is observed in the spectra. As a result, one may conclude that adopting the

modified DCSK scheme, the information safety is achieved in whole packet modulation for different values of D in premodulation.

In the case of $\alpha < \beta$, the representation of one bit is exemplified in Fig 5.17. As shown in the plot, the second part of each bit (B) is represented by α points of chaotic sample and it is the opposite of the reference sample 1 (A1) for b_1='0'. Hence, B is treated as the data sample. The remaining $2\beta - 2\alpha$ points are defined as reference sample 2 (A2). Correspondingly, s_j during the l-th bit period can be described as follows.
For b_l= '1',

$$s_j = \begin{cases} zx_j, & (l-1)2\beta + 1 \le j \le (l-1)2\beta + \alpha, \\ zx_{j-\alpha}, & (l-1)2\beta + \alpha + 1 \le j \le (l-1)2\beta + 2\alpha, \\ zx_j, & (l-1)2\beta + 2\alpha + 1 \le j \le (l-1)2\beta + 2\beta. \end{cases} \tag{5.3}$$

For b_l= '0',

$$s_j = \begin{cases} zx_j, & (l-1)2\beta + 1 \le j \le (l-1)2\beta + \alpha, \\ -zx_{j-\alpha}, & (l-1)2\beta + \alpha + 1 \le j \le (l-1)2\beta + 2\alpha, \\ zx_j, & (l-1)2\beta + 2\alpha + 1 \le j \le (l-1)2\beta + 2\beta. \end{cases} \tag{5.4}$$

Figure 5.18 presents the simulation results of whole packet modulation in the case of $\alpha = 30$. The other parameters are set the same as those for $\alpha > \beta$. It can be seen that the data sample (31th to 60th points in each bit period) is identical to or inverted to the reference sample 1 (the first 30 points in each bit period). Particularly, it should be pointed out that the DCSK demodulators for $\alpha > \beta$ and $\alpha < \beta$ are different due to the difference in modulations. Shown in Fig. 5.19 is the modified demodulator for $\alpha < \beta$. Furthermore, the amplitude spectra of s_j with different α ($\alpha < \beta$) are plotted in Fig. 5.20. Comparing Figs. 5.20(a) and 5.20(b) to Fig. 5.10(a), it is obvious that the smaller the α, the more overlapped the envelopes of the amplitude spectrum. Whereas the BER can be improved by increasing α in this case and thus the trade off between the BER and the degree of overlap appears in determining the value of α.

Based on the above discussion, one may conclude that the two keys (2β and α) in the modified DCSK scheme facilitate keeping the information safety in whole packet modulation. Moreover, the farther the α is away from β, the more difficult it is for attackers to estimate keys directly from the amplitude spectrum of the modulated packet signal. As for determining the value of α, the trade off between the BER and the degree of overlap in

envelopes of amplitude spectrum should be considered.

5.5.2 Power transfer

The power transferred after whole packet modulation is analyzed in this section. Since the power of packet is carried by the payload, we focus on the average output power of the modulator in payload duration named as P_{modout}. Here, we assume that the chaotic signal generated from the chaos generator carries power for modulation. Referring to Eqs. (5.3) and (5.4), P_{modout} in the case of $\beta < \alpha < 2\beta$ can be calculated by Eq. (5.5), where P_{modout} is in watts (W) and x_{lm} denotes the m-th point of chaotic sample in the l-th bit period. Likewise, P_{modout} for $0 < \alpha < \beta$ can be calculated from Eq. (5.6).

$$P_{\text{modout}} = \frac{D \sum_{l=1}^{N_{\text{b}}} (\sum_{m=1}^{\alpha} z^2 x_{lm}^2 T_x + \sum_{m=1}^{2\beta-\alpha} z^2 x_{lm}^2 T_x)}{N_{\text{b}} T_b}. \tag{5.5}$$

$$P_{\text{modout}} = \frac{D \sum_{l=1}^{N_{\text{b}}} (\sum_{m=1}^{\alpha} z^2 x_{lm}^2 T_x + \sum_{m=1}^{\alpha} z^2 x_{lm}^2 T_x + \sum_{m=2\alpha+1}^{2\beta} z^2 x_{lm}^2 T_x)}{N_{\text{b}} T_b}. \tag{5.6}$$

Thus, the chaotic sample needs to be determined first to obtain P_{modout}. Without loss of generality, we generate chaotic sample x_j in simulation by the normalized improved logistic map [46] as in Eq. (5.7). The initial value is set at $x_1 = 0.75$. x_j is thus limited in the range of $[-1.4142, +1.4142]$.

$$x_{j+1} = \sqrt{2}(1 - x_j^2). \tag{5.7}$$

Moreover, the time interval between two points of chaotic sample is $T_{\text{x}} = 0.001$ s and the generated sample is of finite length 1000 ($N_{\text{x}} = 1000$). Accordingly, the numerical approximation of auto-correlation function of x_j is shown in Fig. 5.21(a). It can be seen that $R(x, x) \approx \delta[n]$ which demonstrates that x_j is random-like. Meanwhile, the power spectral density of x_j is exhibited in Fig. 5.21(b), from which the wide-band property of x_j is confirmed. According to the above characteristics of x_j, Eqs. (5.5) and (5.6) can be approximately simplified as Eqs. (5.8) and (5.9), respectively. The equations suggest that the power of the modulated packet is eventually de-

termined by the duty ration of premodulation (D), the characteristic chaotic sample ($\mathrm{E}[x_j^2]$) and the voltage of the original power packet (z). For example, under the settings of $T_x = T_{\mathrm{sam}} = 0.001$ s, $T_b = 0.1$ s, and $2\beta = 100$, the mean values of x_j and x_j^2 in the payload duration (200 bits) can be obtained as $\mathrm{E}[x_j] = -0.0012$ and $\mathrm{E}[x_j^2] = 1.0007$. Thus the transferred power is determined by D and z^2 approximately in the whole packet modulation.

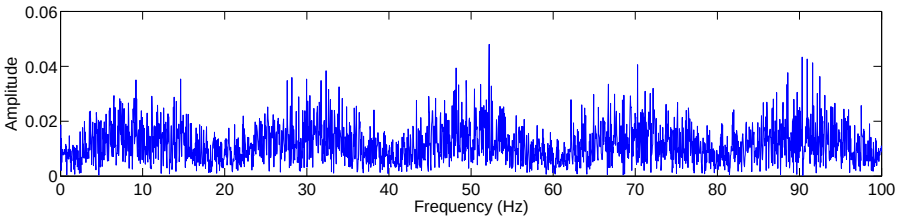
$$\begin{aligned} P_{\mathrm{modout}} &\approx \frac{Dz^2T_x}{T_b}\{\alpha\mathrm{E}[x_j^2] + (2\beta - \alpha)\mathrm{E}[x_j^2]\} \\ &= D\mathrm{E}[x_j^2]z^2. \end{aligned} \tag{5.8}$$

$$\begin{aligned} P_{\mathrm{modout}} &\approx \frac{Dz^2T_x}{T_b}\{\alpha\mathrm{E}[x_j^2] + \alpha\mathrm{E}[x_j^2] + (2\beta - 2\alpha)\mathrm{E}[x_j^2]\} \\ &= D\mathrm{E}[x_j^2]z^2. \end{aligned} \tag{5.9}$$

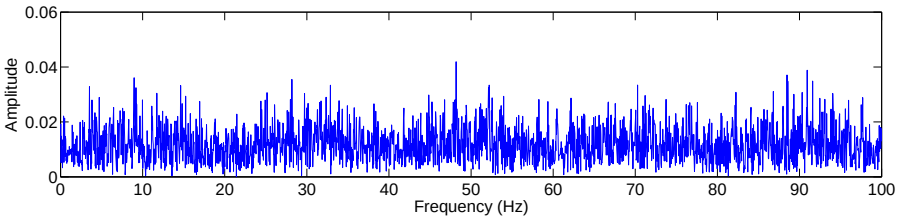
Next, we will consider how to transfer the power of the modulated packet correctly. In the basic power packet dispatching system, once the header is recognized in the router, the inside switches will be turned on and the power of packet is transferred. This is based on the fact that electric current appears when the positive voltage of the packet signal is applied to loads. As explained in Sect. 3.5.5, loads are restricted to be resistors in the system currently. However, using the DCSK scheme, the modulated signal is of both positive and negative voltages, It should be noticed that no power is transferred when the voltage of the modulated signal is negative. For this reason, it is necessary to shift the voltage of the modulated signal to be positive for transferring full power of the modulated packet. On the other hand, the preamble and the header do not carry power and they are supposed to be recovered for determining the packet dispatching through the DCSK demodulator. According to the principles of the DCSK demodulator, the positive and negative voltages of the modulated signal are essential for the correct demodulation. As a result, we first shift the voltage of the modulated signal in the whole modulated packet at the output of the modulator for transferring power. Then, the voltage of the modulated signal in preamble and header duration is shifted back to the original values in the demodulator before demodulation starts. In this manner, the information contained in the preamble and the header can be obtained correctly and the power of modulated packet is transferred completely to the designated load.

5.6 Summary

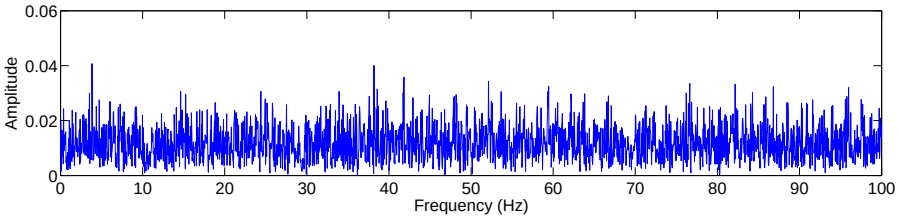
The concept of safety of power packet dispatching was firstly proposed in this chapter, for the purpose of protecting the information of packets from attackers and keeping the loads safe regarding power. The concept has not been figured out before for dispatching electric energy, until the power packet dispatching was introduced. As a possible way to achieve the safety, modulation of power packets was proposed. At first, partial packet modulation using the DCSK scheme was examined in simulation, through which the information safety based on the partial packet modulation was confirmed. Next, we proposed to modulate the whole power packet, in which premodulation using PWM was applied to the payload in the first step. Due to the premodulation, the amount of transferred power could be adjusted. Thereafter, the whole premodulated packet was further modulated using a modified DCSK scheme. Adopting the modified DCSK scheme, two advantages exist in the further modulation: one is to achieve the information safety and the other is to spread the spectrum of noise. Additionally, the rescaling of power by premodulation in whole packet modulation might be a potential advantage from the viewpoint of expanding the range of power sources to meet the demand of loads. Besides, it should be pointed out that the power packet modulation method is very preliminary and is proposed primarily to suggest a possible way to improve the function of power packet dispatching.



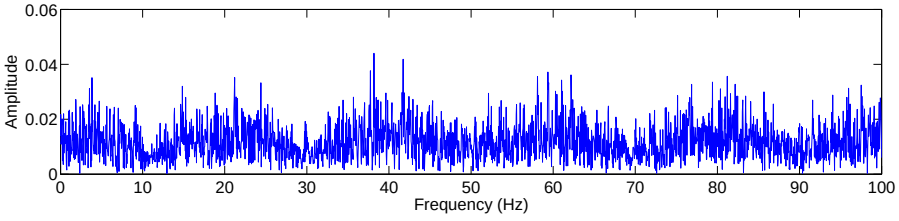
(a)



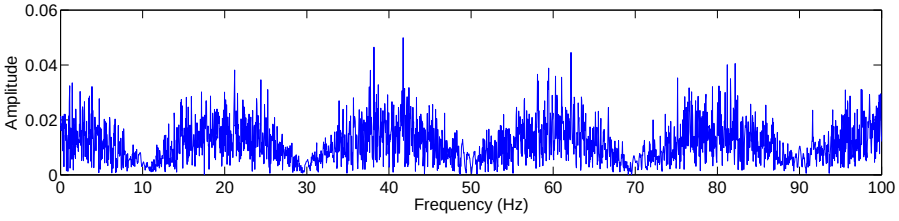
(b)



(c)



(d)



(e)

Figure 5.10: Amplitude spectrum of the modulated signal in the whole packet modulation with different values of D in premodulation. (a) $D = 0.2$; (b) $D = 0.4$; (c) $D = 0.6$; (d) $D = 0.8$; (e) $D = 1$;

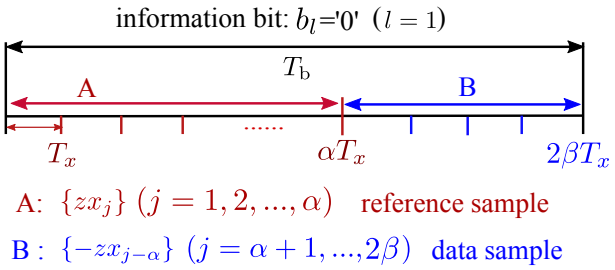


Figure 5.11: Representation of one bit b_1 (b_1='0') using the modified DCSK scheme with $\alpha > \beta$.

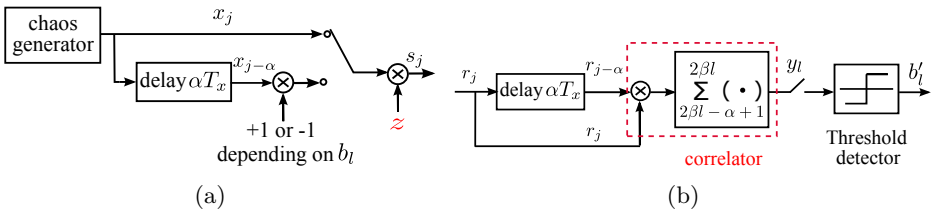


Figure 5.12: Block diagram of the modified DCSK system. (a) modulator; (b) demodulator.

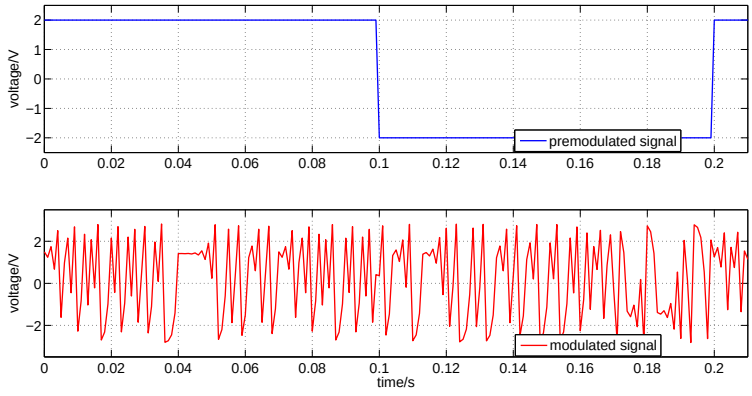


Figure 5.13: Modified DCSK modulation in simulation with $\alpha = 70$.

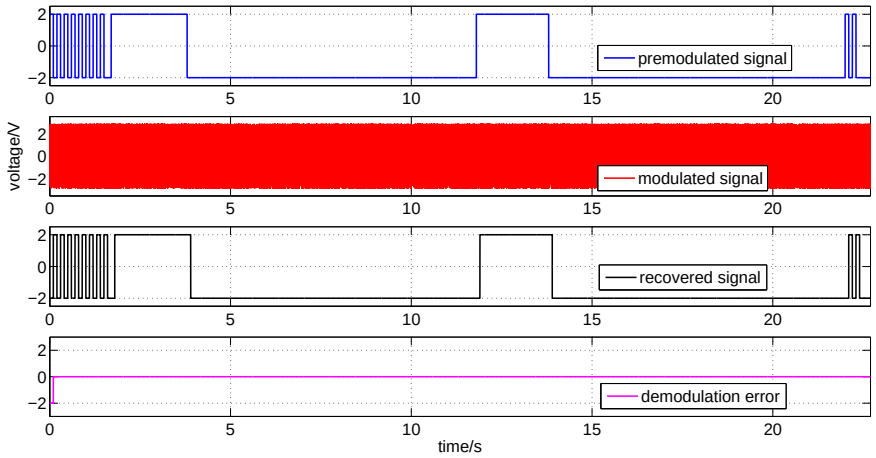
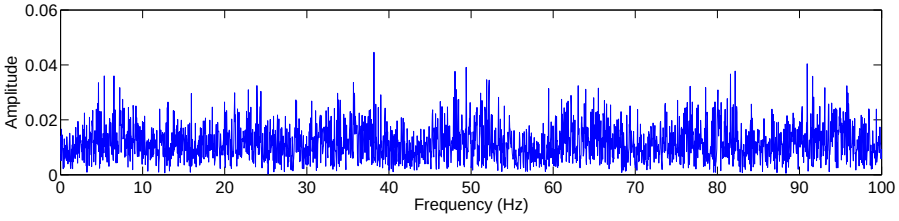
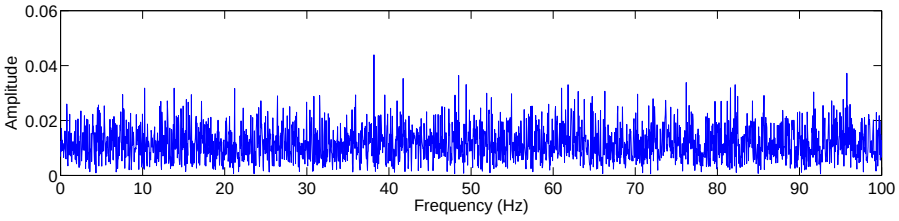


Figure 5.14: Modulation and demodulation of whole premodulated packet in simulation with correct keys in demodulator. The premodulated packet is recovered without error. $T_{\mathrm{b}} = 0.1$s, $T_x = 0.001$s, $2\beta = 100$, and $\alpha = 70$.

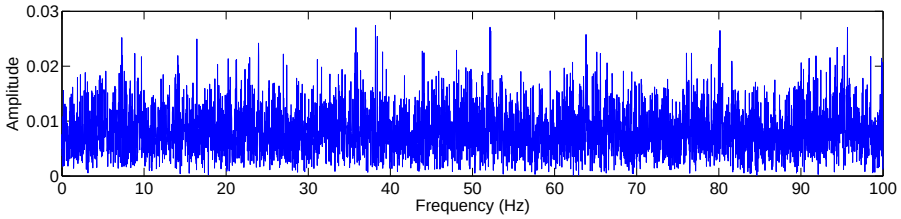


(a)

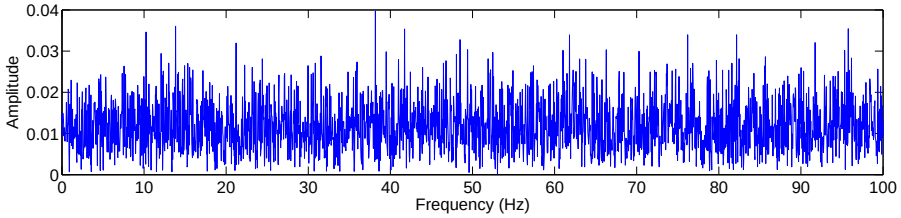


(b)

Figure 5.15: Amplitude spectrum of the modulated signal s_j in one packet duration with $\alpha > \beta$. (a) $\alpha = 70$; (b) $\alpha = 90$.



(a)



(b)

Figure 5.16: Amplitude spectrum of the modulated signal s_j in one packet duration for $D = 0.4$. (a) $\alpha = 70$; (b) $\alpha = 90$.

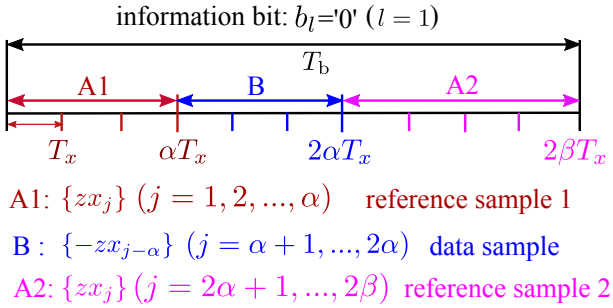


Figure 5.17: Representation of one information bit b_1 (b_1='0') using modified DCSK scheme with $\alpha < \beta$.

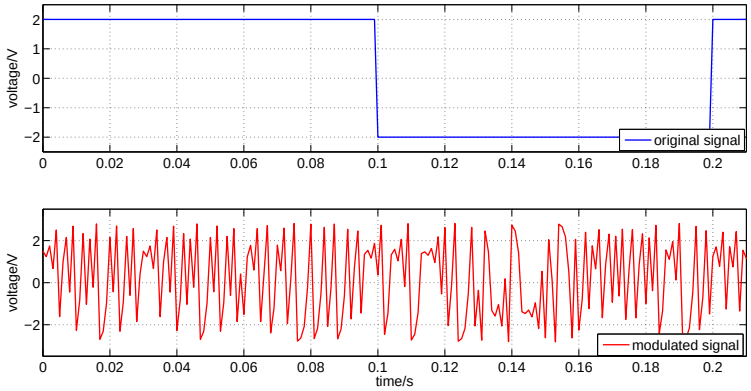


Figure 5.18: Modified whole packet modulation in simulation with $\alpha = 30$.

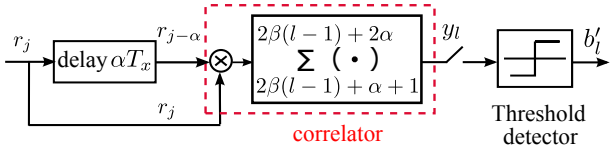


Figure 5.19: Block diagram of the demodulator in the modified DCSK system with $\alpha < \beta$.

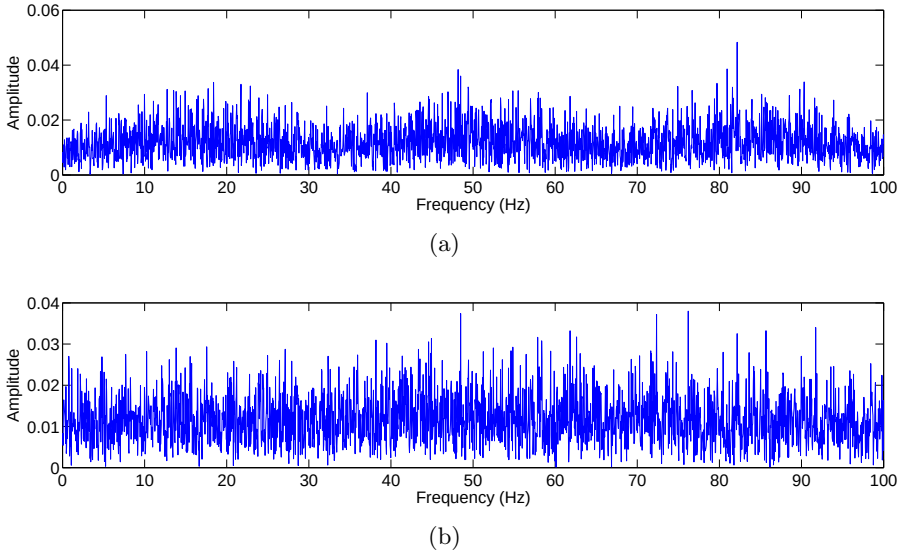
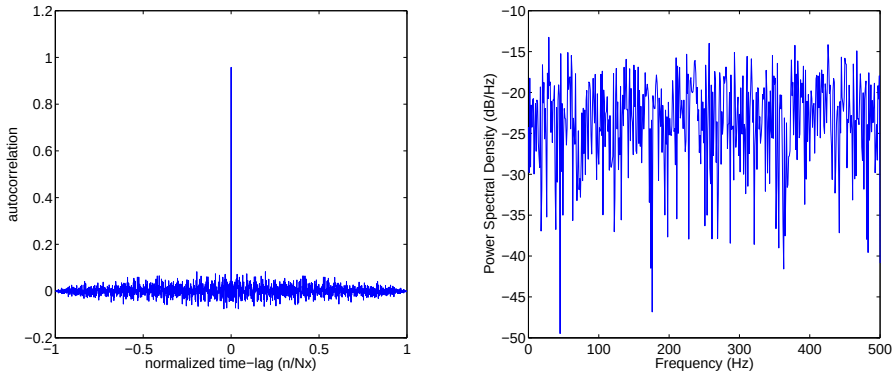


Figure 5.20: Amplitude spectrum of the modulated signal s_j in one packet duration with $\alpha < \beta$. (a) $\alpha = 30$; (b) $\alpha = 10$.



(a) (b)

Figure 5.21: Characteristics of the chaotic sample in simulation. (a) Normalized approximated auto-correlation; (b) Approximated power spectral density.

Chapter 6

Conclusions

6.1 Attainments

In this dissertation, the discussion centers on power packet dispatching in a power packet dispatching system. In the beginning, the system was introduced and the necessity of clock synchronization between a mixer and a router was analyzed. In order to overcome the deficiencies of the current wired clock synchronization in the system, a first-order controlled clock synchronization was derived. For the quick convergence for every arriving packet, a second-order controlled clock synchronization was proposed, based on which the power packet dispatching in a basic system succeeded. The power packet dispatching under different scenarios was also investigated in a modified system and the feasibility of system expansion based on autonomous clock synchronization was validated. Besides the basic function of the system as dispatching power packets, an advantageous function was also proposed, i.e., the safety of power packet dispatching.

Chapter 2 focused on the first-order controlled clock synchronization. At first, the mechanism of CPPLL in achieving the clock synchronization between two clock signals was introduced. Referring to the mechanism of CPPLL, the first-order controlled model of a digital clock synchronization method was established. Then the achievement of the clock synchronization based on the first-order controlled model was confirmed in both simulations and experiments. Moreover, the settling time was found to be around 10 reference clock cycles in experiments.

Chapter 3 realized the power packet dispatching based on autonomous clock synchronization in a basic power packet dispatching system. A second-

order controlled model of the digital clock synchronization method was firstly established, which improved the settling time of clock synchronization significantly by shortening it from 10 reference cycles in first-order controlled clock synchronization to five reference clock cycles. Before applying the second-order controlled model to a power packet dispatching system practically, its stability was analyzed. Using the second-order controlled clock synchronization and the preamble in power packets, autonomous clock synchronization between the mixer clock signal and the router clock signal was achieved. Based on the success of autonomous clock synchronization, correct power packet dispatching and complete repacketization were realized experimentally. In addition, power packet dispatching was also confirmed under the condition of ohmic-inductive loads.

Chapter 4 dealt with the feasibility of system expansion based on autonomous clock synchronization. Power packet dispatching in a modified system under four typical scenarios were discussed in experiments. Based on the results, the possibility of extending the power packet dispatching system to transfer multi packets in the network was demonstrated without loosing the concept of power packet dispatching.

Chapter 5 proposed the concept of safety of power packet dispatching, for the purpose of protecting the information of packets from attackers and keeping the loads safe regarding power. After introducing the principles of the DCSK scheme, the preamble and the header of a power packet were modulated using this scheme to achieve the information safety in simulations, which is called as partial packet modulation. Next, the payload of packets was modulated using the modulation scheme of PWM, i.e., premodulation, due to which the transferred power of packets became adjustable. Then, the whole premodulated packet was further modulated using the modified DCSK scheme. By these two steps of modulation to the whole power packet, the information safety and the power safety were achieved simultaneously.

One primary achievement of this dissertation is the achievement of autonomous clock synchronization for power packet dispatching. The clock synchronization was achieved via the preamble and the preamble was generated from power sources, i.e., power was included in the carrier of information. Another achievement of this work relies on the proposal of safety of power packet dispatching. The concept of safety was firstly defined and figured out for dispatching electric energy. In particular, the DCSK scheme

was modified for achieving the information safety and the power safety simultaneously.

6.2 Future work

Further research in the area of power packet dispatching based on autonomous clock synchronization mainly include three aspects. At first, considering different applications of the power packet dispatching system, extension of the range of the mixer clock frequency, which can be synchronized with using the second-order controlled model, is desired. Next, the system expansion based on autonomous clock synchronization calls for further study. In particular, the failure in autonomous clock synchronization caused by jitter in a power packet dispatching system should be paid attention to. In addition, when congestion of packets occurs at storages, regulation schemes are required to avoid potential safety issues. At last, realization of system expansion in real circuits needs to be investigated.

With respect to the safety of power packet dispatching, deeper study will be indispensable. Most importantly, the usefulness of adopted modulation schemes in improving the information safety needs to be discussed. For example, power packets might be modulated using other advanced modulation schemes such as CDMA. Thus, comparison of the information safety based on different modulation schemes will be necessary. Next, there may exist a lot of difficulties in realizing modulation and demodulation of packets in a real circuit. For instance, it will be challenging to generate and deal with both positive and negative voltages in a real circuit. Besides, it is important to discuss a practical way to transfer full power of modulated packets in the whole packet modulation. At last, the bit-error rate of the demodulation will be another topic needs to be considered in future.

Appendix A

Second-order controlled model

The second-order controlled model of a digital clock synchronization method is derived based on the primitive model in Eq. (2.1). In order to apply a second-order control algorithm, a second-order digital clock synchronization system needs to be built first. Thus, $T_{\mathrm{NCO}}^{(k-1)}$ is introduced as in Eq. (A.1) referring to Eq. (2.1).

$$T_{\mathrm{NCO}}^{(k-1)} = T_{\mathrm{REF}} + \Delta(k) - \Delta(k-1). \quad k = 2, 3, \cdots \tag{A.1}$$

Based on Eqs. (2.1) and (A.1), the second-order clock synchronization system is built as described in Eq. (A.2) by combining $T_{\mathrm{NCO}}^{(k)}$ with $T_{\mathrm{NCO}}^{(k-1)}$ in a certain proportion a_1 ($a_1 \neq 1$ is a constant parameter).

$$T_{\mathrm{NCO}}^{(k)} - a_1 T_{\mathrm{NCO}}^{(k-1)} = [\Delta(k+1) - \Delta(k)] - a_1[\Delta(k) - \Delta(k-1)] + (1-a_1)T_{\mathrm{REF}}. \tag{A.2}$$

It has been explained in Sect. 2.3 that the achievement of clock synchronization using the digital clock synchronization method is equivalent to the convergence of the series of $\Delta(k)$. Therefore, in the next step, the control algorithm in Eq. (A.3) is applied to the second-order system in order that the series of $\Delta(k)$ in the system converges. Here, a_2 is a constant parameter which is taken to be positive. Likewise, Eq. (A.4) can also be obtained.

$$\Delta(k) - \Delta(k-1) = -a_2\Delta(k-1). \quad k = 2, 3, \cdots. \tag{A.3}$$

$$\Delta(k+1) - \Delta(k) = -a_2\Delta(k). \tag{A.4}$$

The reason for using such kind of control algorithm has also been explained in Sect. 2.3. At last, substituting Eqs. (A.3) and (A.4) into Eq. (A.2), the second-order controlled model of a digital clock synchronization method can be obtained as in (A.5).

$$T_{\mathrm{NCO}}^{(k)} = a_1 T_{\mathrm{NCO}}^{(k-1)} - a_2\Delta(k) + a_1 a_2 \Delta(k-1) + (1-a_1)T_{\mathrm{REF}}. \quad (a_1 \neq 1, a_2 > 0) \tag{A.5}$$

Appendix B

Stability of the model

As stated in the beginning of Sect. 3.2.1, the stability of the second-order controlled model in Eq. (3.1) will be analyzed using characteristic equations here. To begin with, we replace $T_{\mathrm{NCO}}^{(k)}$ and $T_{\mathrm{NCO}}^{(k-1)}$ in Eq. (3.1) with T_{REF}, $\Delta(k+1)$, $\Delta(k)$ and $\Delta(k-1)$ so that the characteristic equation of the model can be obtained. Correspondingly, Eq. (B.1) is obtained. It is readily apparent that Eq. (B.1) can be simplified to Eq. (B.2).

$$\begin{aligned} T_{\mathrm{REF}} + \Delta(k+1) - \Delta(k) = a_1[T_{\mathrm{REF}} + \Delta(k) - \Delta(k-1)] - a_2\Delta(k) \\ + a_1 a_2 \Delta(k-1) + (1-a_1)T_{\mathrm{REF}}. \end{aligned} \tag{B.1}$$

$$\Delta(k+1) - (1 + a_1 - a_2)\Delta(k) + a_1(1-a_2)\Delta(k-1) = 0. \tag{B.2}$$

From Eq. (B.2), it is clear that the characteristic of the model is determined by the constant parameters a_1 and a_2. In addition, the characteristic equation of the model can be derived from Eq. (B.2) as in Eq. (B.3). Subsequently, the characteristic values are obtained as in Eq. (B.4).

$$r^2 - (1 + a_1 - a_2)r + a_1(1-a_2) = 0. \tag{B.3}$$

$$r = \frac{(1 + a_1 - a_2) \pm \sqrt{(1 + a_1 - a_2)^2 - 4a_1(1-a_2)}}{2}. \tag{B.4}$$

It is obvious that $(1 + a_1 - a_2)^2 - 4a_1(1-a_2)$ in Eq. (B.4) can be simplified to Eq. (B.5). Accordingly, Eq. (B.4) can be rewritten as in Eq. (B.6).

$$(1 + a_1 - a_2)^2 - 4a_1(1-a_2) = (a_1 + a_2 - 1)^2. \tag{B.5}$$

$$r = \frac{(1 + a_1 - a_2) \pm |a_1 + a_2 - 1|}{2}. \tag{B.6}$$

Moreover, the characteristic values given in Eq. (B.6) can be further simplified, if the sign of $a_1 + a_2 - 1$ is determined in advance. Therefore, we categorize $a_1 + a_2 - 1$ into two cases by its sign and analyze the corresponding result of r: (1) $a_1 + a_2 - 1 \geq 0$. (2) $a_1 + a_2 - 1 < 0$. It can be figured out that the characteristic values, represented by r_1 and r_2, for both cases are the same as in Eq. (B.7).

$$r_1 = a_1,\ r_2 = 1 - a_2. \tag{B.7}$$

For a second-order digital system, it is well known that the absolute value of all characteristic values is required to be less than 1 so that the system is guaranteed to be stable. As a consequence, the range of a_1 and a_2 which ensures the stability of the second-order controlled model is obtained as in Eq. (B.8), which is equivalent to Eq. (B.9)

$$|a_1| < 1,\ |1 - a_2| < 1. \tag{B.8}$$

$$-1 < a_1 < 1,\ 0 < a_2 < 2. \tag{B.9}$$

Bibliography

[1] S. Gadelovits, A. Kuperman, M. Sitbon, I. Aharon, and S. Singer, "Interfacing renewable energy sources for maximum power transfer part i: Statics," *Renewable and Sustainable Energy Reviews*, vol. 31, pp. 501–508, 2014.

[2] M. Lenzen, "Current state of development of electricity-generating technologies: A literature review," *Energies*, vol. 3, no. 3, pp. 462–591, 2010.

[3] N. Armaroli and V. Balzani, "The future of energy supply: Challenges and opportunities," *Angewandte Chemie International Edition*, vol. 46, pp. 52–66, 2007.

[4] H. Saitoh, S. Miyamori, T. Shimada, and J. Toyoda, "An autonomous decentralized control mechanism for power flow in an open electric energy network," *Electrical engineering in Japan*, vol. 121, no. 4, pp. 28–37, 1997.

[5] J. Toyoda and H. Saitoh, "Proposal of an open-electric-energy-network (oeen) to realize cooperative operations of iou and ipp," in *Energy Management and Power Delivery, 1998. Proceedings of EMPD'98. 1998 International Conference on*, vol. 1. IEEE, 1998, pp. 218–222.

[6] T. Takebayashi, T. Sonoda, and W.-P. Chen, "Power supply and demand control technologies for smart cities," *FUJITSU Sci. Tech. J*, vol. 50, no. 1, pp. 72–77, 2014.

[7] Y. Xu, R. Rojas-Cessa, and H. Grebel, "Allocation of discrete energy on a cloud-computing datacenter using a digital power grid," in *Green Computing and Communications (GreenCom), 2012 IEEE International Conference on*, Nov 2012, pp. 615–618.

[8] E. Gelenbe, "Quality of information and energy provisioning," in *Pervasive Computing and Communications Workshops (PERCOM Workshops), 2013 IEEE International Conference on*, March 2013, pp. 453–457.

[9] R. Rojas-Cessa, Y. Xu, and H. Grebel, "Management of a smart grid with controlled-delivery of discrete levels of energy," in *Electrical Power Energy Conference (EPEC), 2013 IEEE*, Aug 2013, pp. 1–6.

[10] T. Hikihara, "Power router and packetization project for home electric energy management," *Santa Barbara Summit on Energy Efficiency, Santa Barbara, CA, USA*, pp. 12–13, 2010.

[11] T. Takuno, M. Koyama, and T. Hikihara, "In-home power distribution systems by circuit switching and power packet dispatching," in *Smart Grid Communications (SmartGridComm), 2010 First IEEE International Conference on*. IEEE, 2010, pp. 427–430.

[12] T. Takuno, Y. Kitamori, R. Takahashi, and T. Hikihara, "Ac power routing system in home based on demand and supply utilizing distributed power sources," *Energies*, vol. 4, no. 5, pp. 717–726, 2011.

[13] R. Takahashi, T. Takuno, and T. Hikihara, "Estimation of power packet transfer properties on indoor power line channel," *Energies*, vol. 5, no. 7, pp. 2141–2149, 2012.

[14] K. Tashiro, R. Takahashi, and T. Hikihara, "Feasibility of power packet dispatching at in-home dc distribution network," in *Smart Grid Communications (SmartGridComm), 2012 IEEE Third International Conference on*. IEEE, 2012, pp. 401–405.

[15] N. Fujii, R. Takahashi, and T. Hikihara, "Networked power packet dispatching system for multi-path routing," in *2014 IEEE/SICE International Symposium on System Integration (SII2014)*. IEEE, 2014.

[16] S. Nawata, N. Fujii, Y. Z. Zhou, R. Takahashi, and T. Hikihara, "A theretical examination of an unexpected transfer of power packets by synchronization failure," in *International Symposium on Nonlinear Theory and its Applications (NOLTA2014)*. IEICE, 2014, pp. 60–63.

[17] X. Wang and Z. B. Zeng, "A design for clock synchronization using cppll," *Applied Mechanics and Materials*, vol. 543, pp. 558–561, 2014.

[18] F. M. Gardner, "Charge-pump phase-lock loops," *Communications, IEEE Transactions on*, vol. 28, no. 11, pp. 1849–1858, Nov 1980.

[19] P. K. Hanumolu, M. Brownlee, K. Mayaram, and U.-K. Moon, "Analysis of charge-pump phase-locked loops," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, no. 9, pp. 1665–1674, 2004.

[20] S. Pan, T. Morris, and U. Adhikari, "Classification of disturbances and cyber-attacks in power systems using heterogeneous time-synchronized data," 2009.

[21] H. Yu, Y. Inoue, and Y. Han, "A new high-speed low-voltage charge pump for pll applications," in *ASIC, 2005. ASICON 2005. 6th International Conference On*, vol. 1, Oct 2005, pp. 387–390.

[22] J. Zou, D. Mueller, H. Graeb, and U. Schlichtmann, "A cppll hierarchical optimization methodology considering jitter, power and locking time," in *Proceedings of the 43rd annual Design Automation Conference*. ACM, 2006, pp. 19–24.

[23] S. Ying, W. Yuan, J. Song, Z. Baoying, and J. Lijiu, "Design of low jitter adaptive-bandwidth charge pump pll with passive filter," in *ASIC, 2007. ASICON'07. 7th International Conference on*. IEEE, 2007, pp. 319–322.

[24] V. Kratyuk, P. K. Hanumolu, U.-K. Moon, and K. Mayaram, "A design procedure for all-digital phase-locked loops based on a charge-pump phase-locked-loop analogy," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART 2 EXPRESS BRIEFS*, vol. 54, no. 3, p. 247, 2007.

[25] X. Y. TAN, X. W. LIU, and Y. JI, "A low-jitter cppll for clock of micro-accelerometer," *Journal of Harbin Institute of Technology*, vol. 5, p. 039, 2007.

[26] S. L. WANG, X. Z. LIU, and X. Q. LAI, "Application and architecture of a novel and self-balanced cppll circuit," *Chinese Journal of Electron Devices*, vol. 5, p. 104, 2007.

[27] J. Gupta, A. Sangal, and H. Verma, "High speed cmos charge pump circuit for pll applications using 90nm cmos technology," in *Information and Communication Technologies (WICT), 2011 World Congress on*. IEEE, 2011, pp. 346–349.

[28] V. S. Sadeghi and H. M. Naimi, "A fast synthesizer using a bang-bang frequency comparator and locking status indicator," in *Electrical Engineering and Informatics (ICEEI), 2011 International Conference on*. IEEE, 2011, pp. 1–4.

[29] N. Tall, N. Dehaese, S. Bourdel, and B. Bonat, "An all-digital clock and data recovery circuit for low-to-moderate data rate applications," in *Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on*, Dec 2011, pp. 37–40.

[30] V. S. Sadeghi, H. M. Naimi, and M. P. Kennedy, "A fast charge pump pll using a bang-bang frequency comparator with dead zone," in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*. IEEE, 2012, pp. 1379–1382.

[31] B. Mishra, S. Save, and S. Patil, "Design and analysis of second and third order pll at 450 mhz," *Int. J. VLSI Des. Commun. Syst*, vol. 2, pp. 97–114, 2011.

[32] K.-S. Lee, B.-H. Park, H.-i. Lee, and M. J. Yoh, "Phase frequency detectors for fast frequency acquisition in zero-dead-zone cpplls for mobile communication systems," in *Solid-State Circuits Conference, 2003. ESSCIRC'03. Proceedings of the 29th European*. IEEE, 2003, pp. 525–528.

[33] T.-Y. Hsu, B.-J. Shieh, and C.-Y. Lee, "An all-digital phase-locked loop (adpll)-based clock recovery circuit," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 8, pp. 1063–1073, Aug 1999.

[34] C. Vaucher, "An adaptive pll tuning system architecture combining high spectral purity and fast settling time," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 4, pp. 490–502, April 2000.

[35] A. Fahim, "A compact, low-power low-jitter digital pll," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, Sept 2003, pp. 101–104.

[36] Y. Chia-Yu, H. Chun-Te, and C.-J. Chien, "Stability analysis of fourth-order charge-pump plls using linearized discrete-time models," *IEICE transactions on electronics*, vol. 90, no. 3, pp. 628–633, 2007.

[37] R. Takahashi, K. Tashiro, and T. Hikihara, "Router for power packet distribution network: Design and experimental verification," *Smart Grid, IEEE Transactions on*, vol. 6, no. 2, pp. 618–626, 2015.

[38] ——, "Router for power packet distribution network: Design and experimental verification," *Smart Grid, IEEE Transactions on*, vol. 6, no. 2, pp. 618–626, 2015.

[39] R. Takahashi and K. Umeno, "Performance evaluation of cdma using chaotic spreading sequence with constant power in indoor power line fading channels," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 97, no. 7, pp. 1619–1622, 2014.

[40] U. Parlitz, L. O. Chua, L. Kocarev, K. Halle, and A. Shang, "Transmission of digital signals by chaotic synchronization," *International Journal of Bifurcation and Chaos*, vol. 2, no. 04, pp. 973–977, 1992.

[41] K. M. Cuomo and A. V. Oppenheim, "Circuit implementation of synchronized chaos with applications to communications," *Physical review letters*, vol. 71, no. 1, pp. 65–68, 1993.

[42] H. Dedieu, M. P. Kennedy, and M. Hasler, "Chaos shift keying: modulation and demodulation of a chaotic carrier using self-synchronizing chua's circuits," *Circuits and systems II: Analog and digital signal processing, IEEE Transactions on*, vol. 40, no. 10, pp. 634–642, 1993.

[43] T. Kohda and A. Tsuneda, "Pseudonoise sequences by chaotic nonlinear maps and their correlation properties," *IEICE Transactions on Communications*, vol. 76, no. 8, pp. 855–862, 1993.

[44] G. Kolumban, "Differential chaos shift keying: A robust coding for chaotic communication," in *Proc. 4th Int. Workshop on Nonlinear Dynamics of Electronic Systems*, 1996, pp. 87–92.

[45] G. Kolumban, M. P. Kennedy, Z. Jákó, and G. Kis, "Chaotic communications with correlator receivers: theory and performance limits," 2002.

[46] F. Lau and C. Tse, "Performance analysis methods for non-coherent differential chaos-shift-keying systems," in *Chaos-Based Digital Communication Systems*. Springer, 2003, pp. 63–96.

[47] T. Yang, "A survey of chaotic secure communication systems," *International Journal of Computational Cognition*, vol. 2, no. 2, pp. 81–130, 2004.

[48] H. Chen, J. Feng, and C. Tse, "A general noncoherent chaos-shift-keying communication system and its performance analysis," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*. IEEE, 2007, pp. 2466–2469.

[49] R. Takahashi and K. Umeno, "Performance analysis of complex cdma using complex chaotic spreading sequence with constant power," *IEICE transactions on fundamentals of electronics, communications and computer sciences*, vol. 92, no. 12, pp. 3394–3397, 2009.

[50] G. Kaddoum, F. Gagnon, P. Chargé, and D. Roviras, "A generalized ber prediction method for differential chaos shift keying system through different communication channels," *Wireless Personal Communications*, vol. 64, no. 2, pp. 425–437, 2012.

[51] G. Kaddoum, J. Olivain, G. Beaufort Samson, P. Giard, and F. Gagnon, "Implementation of a differential chaos shift keying communication system in gnu radio," in *Wireless Communication Systems (ISWCS), 2012 International Symposium on*. IEEE, 2012, pp. 934–938.

[52] Y. Nathan, J.-P. M. Linnartz, and G. Fettweis, "Multi-carrier cdma in indoor wireless radio networks," *IEICE Transactions on Communications*, vol. 77, no. 7, pp. 900–904, 1994.

[53] B. Farah, A. Kachouri, and M. Samet, "Design of secure digital communication systems using dcsk chaotic modulation," in *Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. International Conference on*. IEEE, 2006, pp. 200–204.

[54] W. Zhenchao and Z. Shibing, "An improved scheme for noise reduction to dcsk based on its retransmission characteristic," in *Computer Science & Education, 2009. ICCSE'09. 4th International Conference on*. IEEE, 2009, pp. 366–370.

[55] C. YiPing, S. Ying, and Z. Dianlun, "Performance of differential chaos-shift-keying digital communication systems over several common channels," in *Future Computer and Communication (ICFCC), 2010 2nd International Conference on*, vol. 2. IEEE, 2010, pp. V2–755.

[56] A. I. Zayed, *Advances in Shannon's sampling theory*. CRC press, 1993.

List of publications

This dissertation is partially fulfilling the requirements of Ph.D. diploma of the Department of Electrical Engineering of Kyoto University. Major divisions have been reproduced throughout this work from the following publication list. The author wishes no claim of copyrights from each and every one publication.

Journal articles

- Yanzi Zhou, Ryo Takahashi, and Takashi Hikihara. "Realization of Autonomous Clock Synchronization for Power Packet Dispatching." *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol.E98-A, No.2, pp.749-753, 2015.

- Yanzi Zhou, Ryo Takahashi, and Takashi Hikihara. "Power Packet Dispatching with Second-Order Clock Synchronization." *International Journal of Circuit Theory and Applications*, Wiley (published online), 2015.

- Yanzi Zhou, Ryo Takahashi, and Takashi Hikihara. "Security of Power Packet Dispatching Using Differential Chaos Shift Keying." *Special Section on Recent Progress in Nonlinear Theory and Its Applications*, NOLTA, IEICE (under resubmission), 2015.

- Yanzi Zhou, Ryo Takahashi, Naoki Fujii and Takashi Hikihara. "Power Packet Dispatching Under Congestion Based on Autonomous Clock Synchronization." *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, IEICE (submitted), 2015.

International conference proceedings

- Yanzi Zhou, Ryo Takahashi and Takashi Hikihara. "System Modeling of a Clock Synchronization Method for Power Packet Dispatching." *International Symposium on Nonlinear Theory and its Applications*, pp. 296-299. IEICE, Luzern, Switzerland, September 2014.

Unarchived proceedings or technical reports

- Yanzi Zhou, Ryo Takahashi and Takashi Hikihara. "A Method of Clock Synchronization for Power Packet Dispatching." *IEICE Society Conference*, A-1-6, IEICE, Fukuoka, Japan, September 2013.
- Yanzi Zhou, Ryo Takahashi, and Takashi Hikihara, "A Method of Clock Synchronization for Power Packet Dispatching – Parameters Optimization in Clock Synchronization." *Technical Committee on Circuits and Systems (CAS) / Nonlinear Problems (NLP)*, CAS2013-46, NLP2013-58, IEICE, Gifu, Japan, September 2013.
- Yanzi Zhou, Ryo Takahashi, Takashi Hikihara. "A Experimental Realization of Clock Synchronization for Power Packet Dispatching." *Proceedings of the IEICE General Conference*, A-1-21, IEICE, Niigata, Japan, March 2014.
- Yanzi Zhou, Ryo Takahashi, Takashi Hikihara. "Security of Power Packet Dispatching Using DCSK Encryption Scheme." *Technical Commitee on Complex Communication Sciences*, IEICE, Tokyo, Japan, March 2015.