Breakdown Characteristics in SiC and Improvement of PiN Diodes toward Ultrahigh-Voltage Applications

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Abstract

Silicon carbide (SiC) is attracting much attention as a material for the next-generation high-power and high-temperature semiconductor devices owing to its superior properties such as wide bandgap, high critical electric field strength, and high thermal conductivity, By years of research, 600–1200 V-class SiC devices such as Schottky barrier diodes or MOSFETs are commercially available from several vendors. For ultrahigh-voltage (UHV: >10 kV) devices, which are attractive for the advanced power distribution and transmission systems, intensive studies are ongoing and several UHV SiC diodes and switches have been demonstrated. However, these devices are still in the research stage and numerous issues are remaining to be solved. For the further improvement and optimization of UHV devices, fundamental studies targeting such high voltage are required.

In this thesis, fundamental studies focusing on improvement of both reverse and forward characteristics of UHV SiC bipolar devices are presented. For the reverse characteristics, a problem of the undetermined values of impact ionization coefficients is studied, followed by extensive studies of edge termination structure for achieving ultrahigh-breakdown voltage. For the forward characteristics, a problem of large built-in potential in SiC bipolar devices is challenged by introducing the concept of hybridization of unipolar and bipolar operations.

In Chapter 2, impact ionization coefficients in SiC are determined by photomultiplication measurement using SiC photodiodes. By using various multiplication layer structures, the impact ionization coefficients are determined in a wide range of electric field of 1.0–3.2 MV/cm. In particular, impact ionization coefficients at low electric field down to 1 MV/cm are determined for the first time in SiC, which is particularly important for designing UHV devices. In addition, the temperature dependence is accurately measured for the first time in SiC up to 150°C, where an unusual temperature dependence is observed in electron impact ionization coefficients. Then, by using the obtained impact ionization coefficients, the critical electric field strength and ideal breakdown voltage of SiC are calculated.

In Chapter 3, an edge termination structure, especially, junction termination extension (JTE) based termination is extensively studied using UHV SiC PiN diodes. First, breakdown characteristics of 10 kV-class SiC PiN diodes with various JTE structures are experimentally studied. The JTE-dose dependence of breakdown voltage for a conventional single-zone JTE applied to UHV PiN diodes is extensively investigated by both experiment

and numerical device simulation. The effect of interface charge on the JTE-dose dependence of breakdown voltage is especially discussed here, and the importance of optimum JTE-dose window is clarified. To overcome the negative effect of interface charge, space-modulated JTE (SM-JTE) is introduced in this study, and its effect is experimentally studied for the first time. By the optimization of SM-JTE structure, a 20 kV-class SiC PiN diode is demonstrated to show the superior potential of SiC as an UHV power device.

In Chapter 4, a hybrid operation device in SiC is demonstrated. As the first step of such a device, an UHV merged-PiN-Schottky (MPS) diode with epitaxial p^+-anode layer is proposed to reduce both the unipolar and bipolar on-resistance. First, each of the component structures of the mesa MPS diode, which are the voltage-blocking layer, junction barrier Schottky (JBS) region, edge termination, and mesa structure, has been investigated through analytical modeling and device simulation. In this study, a snapback phenomenon in MPS diode is especially investigated. To predict and explain the snapback phenomenon, an analytical model is proposed in this study, which is compared with the device simulation and experiment to investigate the validity. In addition, forward characteristics of MPS diodes without the snapback phenomenon are investigated and design guidelines of hybrid operating MPS diode are presented. Furthermore, using the SM-JTE studied in Chapter 3, a 10 kV-class SiC MPS diode is demonstrated.

In Chapter 5, a summary of the present work is given, together with the issues yet to be solved and suggestions for future work.

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Contents

Chapter 1

Introduction

1.1 Background

On 11 March 2011, a catastrophic earthquake and resulting tsunami hit the pacific coast of Tohoku region of this country, causing 15,893 deaths, 6,152 injured, and 2,572 missing in the region [1]. With the help of many people from all over the world, recovery and reconstruction have been going on up to now. However, damage caused by the great earthquake is still remaining, and many people are still suffering from an inconvenient life in the region. Among the numerous disasters caused by the earthquake and the tsunami, the largest tragedy is the accident at the Fukushima Daiichi nuclear power plant. Although the power plant endured the large earthquake, the cooling system of the reactor was destroyed by the tsunami, causing an explosion of chamber which spread a radioactive material. This nuclear power plant disaster has caused large effect to the energy politics of Japan: The qualification to use a nuclear power plant became tighten, making thermal power plant using fossil fuels to be the main generator of the electricity. Because burning of fossil fuels produces large amount of CO_2 which leads to a global warming, consumption of fossil fuels needs to be suppressed. Therefore, using of alternative energy sources such as photovoltaic energy or wind power, and the improvement of conversion efficiency in a power converter system are getting much more important to solve the problem. For the performance improvement of a power converter system, the key is to improve the performance of a semiconductor power device inside it.

A semiconductor power device is an application of semiconductor devices as rectifiers or switches, to control the electric power (voltage, current, frequencies, etc.) itself [2]. Nowadays, the semiconductor material commonly used to fabricate a power device is silicon (Si) from the availability of high-quality and large-area wafers. Furthermore, since the discovery of transistor effect by Bardeen and Brattain in 1947 [3], demand to the logic application has boosted the enormous amount of fundamental studies in both material physics and process technologies in Si. Application of Si as power devices has started in the mid-1950s using bipolar junction transistors (BJTs) [2, 4] in medium power systems, and

thyristors [5] or gate turn-off thyristors (GTOs) [6] developed in the 1960s in high power systems. In the 1970s, power metal-oxide-semiconductor field effect transistors (MOSFETs) were introduced to replace the low voltage BJTs from its high input impedance and fast switching speed [7, 8]. For the high power application, an insulated gate bipolar transistor (IGBT), which is the fusion of BJT and MOSFET, has been invented [9, 10]. Since the 1980s, numerous works have been performed on power MOSFETs and IGBTs to improve the device performances [11–14], and nowadays, it is used in high power systems such as motor control in railway or electric vehicles, and low power systems such as consumer electronics. Similar to the logic application, these power devices are supporting the comfortable life we are achieving these days.

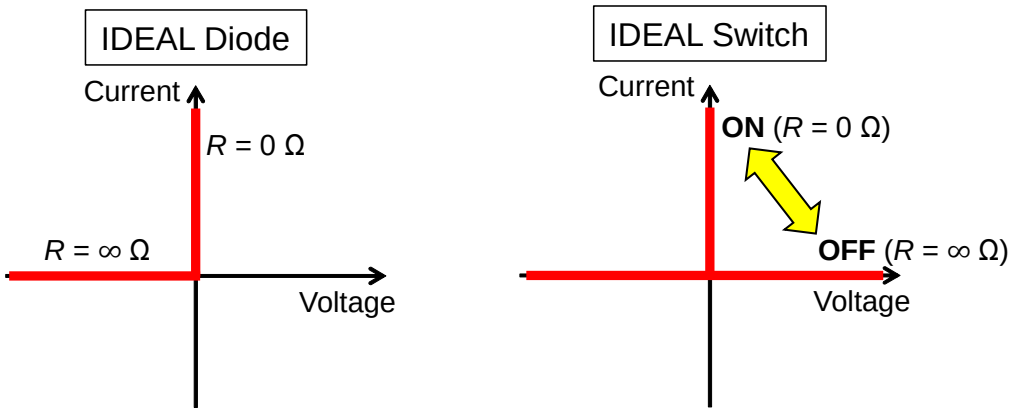
However, from more than 50 years of research in Si power devices, their performance is now approaching the physical limit of material itself. Although there have been attempts to overcome the classical-physical limit by introducing new device structures [15–17], significant performance improvement in Si power device is getting extremely difficult. Therefore, to overcome the physical limit of Si and realize high-performance power devices which Si cannot realize, new semiconductor materials with wide bandgap are getting much attention from its extreme potential when used in a power device [18]. In particular, from its superior physical properties, Silicon Carbide (SiC) has become a promising candidate for the next-generation power device materials [19–22].

1.2 SiC Power Devices

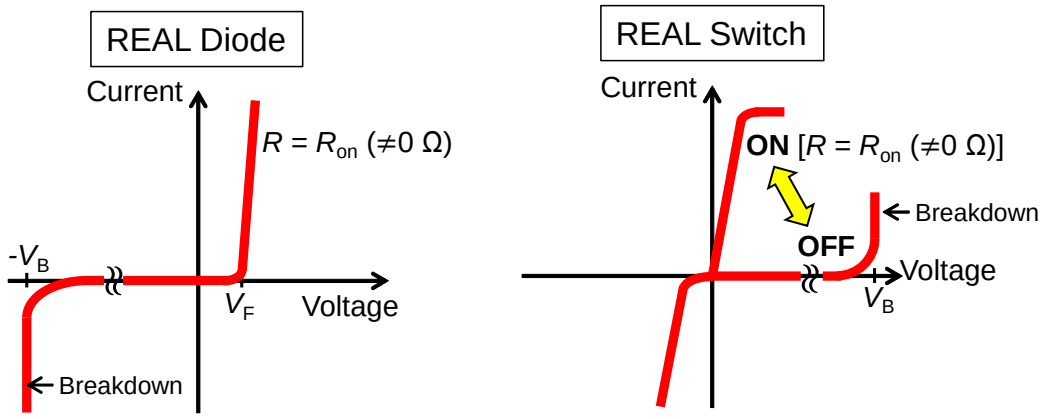
1.2.1 Ideal and Actual Power Device Characteristics

When using semiconductor device as a power device, it is usually used as a rectifier or switch working as "ON" or "OFF." Figure 1.1(a) shows the current–voltage (I-V) characteristics of an ideal rectifier and switch. When a forward bias voltage is applied to a rectifier, it works as a 0 Ω conductor, and at reverse bias, it works as an ∞ Ω insulator which cuts off the current. In an ideal switch, at the ON-state, it also works as a conductor with 0 Ω resistance, and at OFF-state, it works as an insulator with ∞ Ω resistance.

However, in a real semiconductor device, it does not work as an ideal device. Figure 1.1(b) shows the I-V characteristics in real semiconductor devices. For rectifiers, it has a finite on-resistance (R_{ON}) and a voltage drop (V_{F}) at forward bias, and leakage current at reverse bias. Moreover, at a specific reverse bias voltage (V_{B}), the resistance suddenly decreases and a large current starts to flow, where the phenomenon is often called as the breakdown of a device. For actual switches (in this case, MOSFET), it also has a finite on-resistance at ON-state, and a leakage current and breakdown voltage at OFF-state. Due to this R_{ON} and V_{F}, conduction loss occurs in the ON-state which will degrade the power converter efficiencies. Also, due to the existence of V_{B}, an upper limit of the voltage which can be used in the circuit rises. In addition, when transient characteristics are compared,



(a) *I-V* characteristics of ideal power devices



(b) *I-V* characteristics of real power devices

Figure 1.1: Schematic illustration of $I - V$ characteristics of (a) ideal and (b) real diode and switch.

an actual power device needs a transient time to change from ON-state to OFF-state which also causes power dissipation.

Thus, there are large differences between ideal and real power devices. When designing a power device, one will focus on reducing the power dissipation (i.e. R_{ON}) while increasing the breakdown voltage to approach the ideal power device. However, there is a trade-off relationship between R_{ON} and V_{B}, which will limit the maximum device performance which can be realized. Because this limit is determined by the physical properties of a semiconductor material used, this trade-off relationship is commonly employed to compare different semiconductor materials when used in a power device.

1.2.2 Physical Properties of SiC

To overcome the performance limitation of Si power devices, SiC is attracting much attention as an alternative material for the next-generation power devices. Assuming a non-punchthrough structure, the relationship between R_{ON} and V_{B} explained in the previous section can be expressed in the following equation [23],

$$R_{\mathrm{ON}} = \frac{4V_{\mathrm{B}}^2}{\varepsilon_{\mathrm{s}}\mu E_{\mathrm{B}}^3}. \tag{1.1}$$

Here, ε_{s} is the permittivity of the semiconductor, μ the carrier mobility, and E_{B} the critical electric field strength. Table 1.1 shows the physical properties of SiC, Si, and other semiconductor materials. When 4H-type SiC is assumed, the R_{ON}–V_{B} relationship for SiC and Si can be expressed as shown in Fig. 1.2. At a given breakdown voltage, the on-resistance of SiC devices can be reduced to 1/300 of Si devices especially by the difference of critical electric field. In addition, SiC has high thermal conductivity which contributes to the quick removal of heat produced by power losses. Also, the wide bandgap will result in a smaller intrinsic carrier density, which enables the high temperature operation of a power device.

From the superior physical properties SiC has, it was actually known in 1950s as an ideal semiconductor material for high-temperature electronics as predicted by William Shockley [24]. However, due to the difficulties in obtaining high-quality and large-area single crystals without any inclusions of other polytypes, research and development of SiC semiconductors slowed down in the late 1970s. After the dark era, in 1980s, large accomplishments were achieved in the crystal growth of 6H-SiC. First, by the modification of Lely method introduced in 1955 [25], Tairov and Tsvetkov have invented a reproducible method for large area bulk-growth called "seeded sublimation" or simply "modified Lely method" [26, 27]. Using this method, commercialization of high-quality SiC wafers have been realized in a large-diameter up to 150 mm (6 inch) nowadays. In a research stage, even a 200 mm (8 inch) diameter [28] or ultrahigh-quality SiC single crystals [29] have been demonstrated. Second accomplishment was made by Matsunami *et al.* in 1987, where a high-quality 6H-SiC was homoepitaxially grown by chemical vapor deposition (CVD) by using an off-oriented substrate [30]. This technique is called "step-controlled epitaxy," and

Table 1.1: Physical properties and technological status of various polytypes of SiC along with other common semiconductor materials (data given at room temperature).

Property	SiC			Si	GaAs	GaN
	3C	4H	6H			
Crystal Structure	ZB	4H	6H	Dia.	ZB	W
Lattice Constant (Å)	4.36	$a = 3.09$ $c = 10.08$	$a = 3.09$ $c = 15.12$	5.43	5.65	$a = 3.19$ $c = 5.19$
Band Structure	I.D.	I.D.	I.D.	I.D.	D.	D.
Bandgap (eV)	2.3	3.26	3.02	1.12	1.42	3.42
Electron Mobility (cm^2/Vs)	1000	1000 ($\perp$ c) 1200 (// c)	450 ($\perp$ c) 100 (// c)	1350	8500	1500
Hole Mobility (cm^2/Vs)	50	120	100	450	400	50
Electron Saturation Velocity (10^7 cm/s)	2.7	2.2	1.9	1	1	2.7
Breakdown Field (MV/cm)	1.5	2.8	3.0	0.3	0.4	3
Thermal Conductivity (W/cmK)	4.9	4.9	4.9	1.5	0.46	1.3
Relative Permittivity	10	9.7 ($\perp$ c) 10.2 (// c)	9.7 ($\perp$ c) 10.2 (// c)	11.9	12.8	10.4
Conductivity Control	△	◯	◯	◯	◯	△
Thermal Oxide	◯	◯	◯	◯	×	×
Conductive Wafer	△ (Si)	◯	◯	◯	◯	△
Insulating Wafer	×	◯	◯	△ (SOI)	◯	△ (Sapphire)

ZB: Zincblende Dia.: Diamond W: Wurtzite
I.D.: Indirect D.: Direct
◯: Good △: Fair ×: Difficult

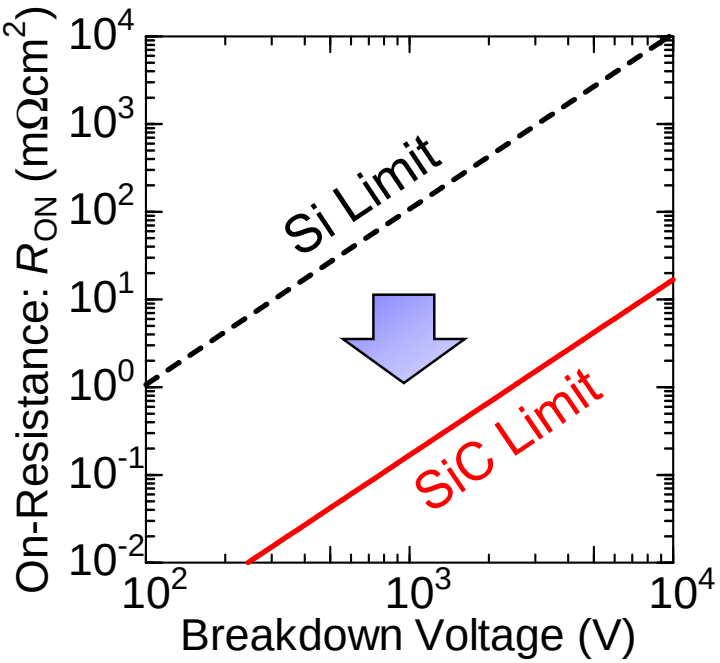


Figure 1.2: Relationship between on-resistance and breakdown voltage for Si and SiC unipolar devices.

by using this method, 4H- and 6H-SiC could be obtained without any inclusions of other polytypes at a low growth temperature of 1500°C, which is over 300°C lower than previous methods [20, 31].

After the realization of high-quality crystal growth, investigations on fundamental technologies toward the fabrication of SiC power devices have started. For the epitaxial growth, conductivity control of both n- and p-types in a wide range of doping concentration (10^{14}–10^{19} cm^{-3}) has been realized [32, 33]. In addition, a high growth rate over 100 μm/h has been achieved toward the thick epilayer used in ultrahigh-voltage (UHV) devices by reducing the growth pressure [34–36] or by using chloride-based chemistry [37, 38]. For the selective doping, ion implantation has been extensively studied because diffusion process cannot be used in SiC due to the extremely low diffusion constants of dopants [39]. By using nitrogen or phosphorus as an n-type dopant and aluminum as a p-type dopant, doping control in a wide range has been achieved [40–42]. In addition, several unique technologies such as hot implantation for the high-dose implantation [43, 44], and a carbon-cap technique for preventing surface degradation during the activation annealing [45] have been invented in SiC. For the electrode formation, ohmic contact with low contact resistivity ($<10^{-6}$ Ωcm^2) has been realized using Ni for n-type, and Ti/Al for p-type, both sintered at 900–1000°C [46–48]. For Schottky contact, extensive studies using various metals have been performed [49, 50]. By applying these component technologies, a number of high-performance SiC power devices have been demonstrated, where the details will be shown in the following sections. From these fundamental studies and the availability of large-area wafers up to 6 inch, SiC is the most promising material compared with the other wide bandgap materials such as gallium nitride (GaN), gallium oxide (Ga_2O_3), or diamond. Although other materials may obtain better R_{ON}–V_B relationship, SiC will be the material for the next-generation power devices.

1.2.3 Present Status of SiC Power Devices

Because SiC can realize lower on-resistance at a given breakdown voltage compared with Si, SiC is attractive for fabricating high-voltage power devices. Figure 1.3 shows the voltage rating of Si and SiC power devices. SiC unipolar devices such as Schottky barrier diodes (SBDs) and MOSFETs are expected to replace the Si bipolar devices such as IGBTs, because unipolar devices have extremely small transient loss. For SiC bipolar devices, they are promising for UHV region (>10 kV) where Si power devices are impossible to target. However, because Si can gain enough low on-resistance at low voltage region (<300 V), SiC is not attractive in this region if the device is used in a normal environment. If the power device is targeting a harsh environment such as high temperature or high radiation environment, SiC devices may be promising.

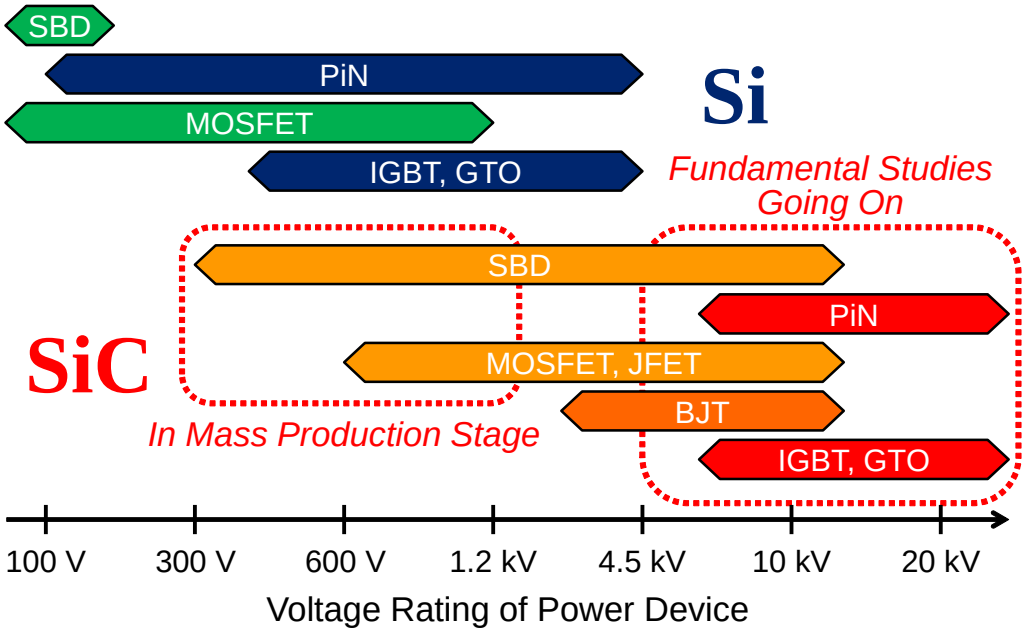


Figure 1.3: Voltage rating of Si and SiC power devices.

Rectifiers: Schottky Barrier Diodes and PiN Diodes

Since SBD and PiN diodes are the basic structures of power devices, intensive studies have been going on for further understanding of SiC device physics and toward the fabrication of switching devices. SBD has a very simple structure where a Schottky metal is formed on an epitaxial layer as shown in Fig. 1.4(a). It is particularly expected to be used in voltage rating over 300 V, where a Si PiN diode is used nowadays. Because a PiN diode is a bipolar device where minority carriers are injected in the lightly-doped layer, it causes a large switching loss during the transient time. However, because SiC SBD has negligibly small switching loss from the unipolar operation, a large reduction of power dissipation can be realized compared with the Si PiN diode. Moreover, the negligible switching loss can increase the switching frequency in the system, which will enable the downsizing of passive components leading to downsizing of the whole conversion system.

From its simple structure, SiC SBD has been demonstrated soon after the realization of crystal growth and investigation of basic technologies. The first 400 V-class 6H-SiC SBD was demonstrated at 1992 [51], followed by a breakdown voltage over 1 kV in 1993 [52]. In 1996, by changing the polytype of SiC to 4H-SiC, SBD with a breakdown voltage of 1.75 kV and an on-resistance of 5 $m\Omega cm^2$ was achieved, which is far below the Si unipolar limit [53]. Hereafter, investigations on SiC devices have accelerated, and in 2001, commercialization of 4H-SiC SBD has started for the first time by Infineon.

Although the commercialization of SiC SBD has started in 2001, numerous problems had to be solved to further improve its performance. For example, one of the largest problems a SiC SBD have faced was the large reverse leakage current. When reverse characteristics of SiC SBD were measured, the observed leakage current density was many orders of magnitude higher than the predicted value using the thermionic emission (TE) model and barrier height lowering, which is the standard model for Si SBD [54]. The origin was first assumed to be some effect by crystal defects, but Hatakeyama *et al.* have pointed out the effect of electron tunneling at the Schottky barrier interface [55]. Because SiC has 10 times larger critical electric field strength than Si at Schottky interface, the effect of electron tunneling has turned out to be the dominant factor of the leakage current. This current was modeled using a thermionic field emission (TFE) model, which is thought to be occurring in other wide bandgap materials. In addition to the TFE current, Fujiwara *et al.* have pointed out that the presence of threading dislocations at Schottky interface has also caused increase of leakage current [56, 57]. In this case, a threading dislocation itself is not the origin, but the shallow nano-pit ($\sim$45 nm-depth) observed directly above the dislocation has caused electric field crowding at reverse bias, which resulted in a large leakage current.

Due to these origins of leakage current, reduction method of electric field strength at the Schottky interface became the key for the improvement of SiC SBD performance. To reduce the electric field strength at Schottky interface, a junction barrier Schottky (JBS) structure shown in Fig. 1.4(b) has been introduced to SiC [58–63]. In this structure, p-type

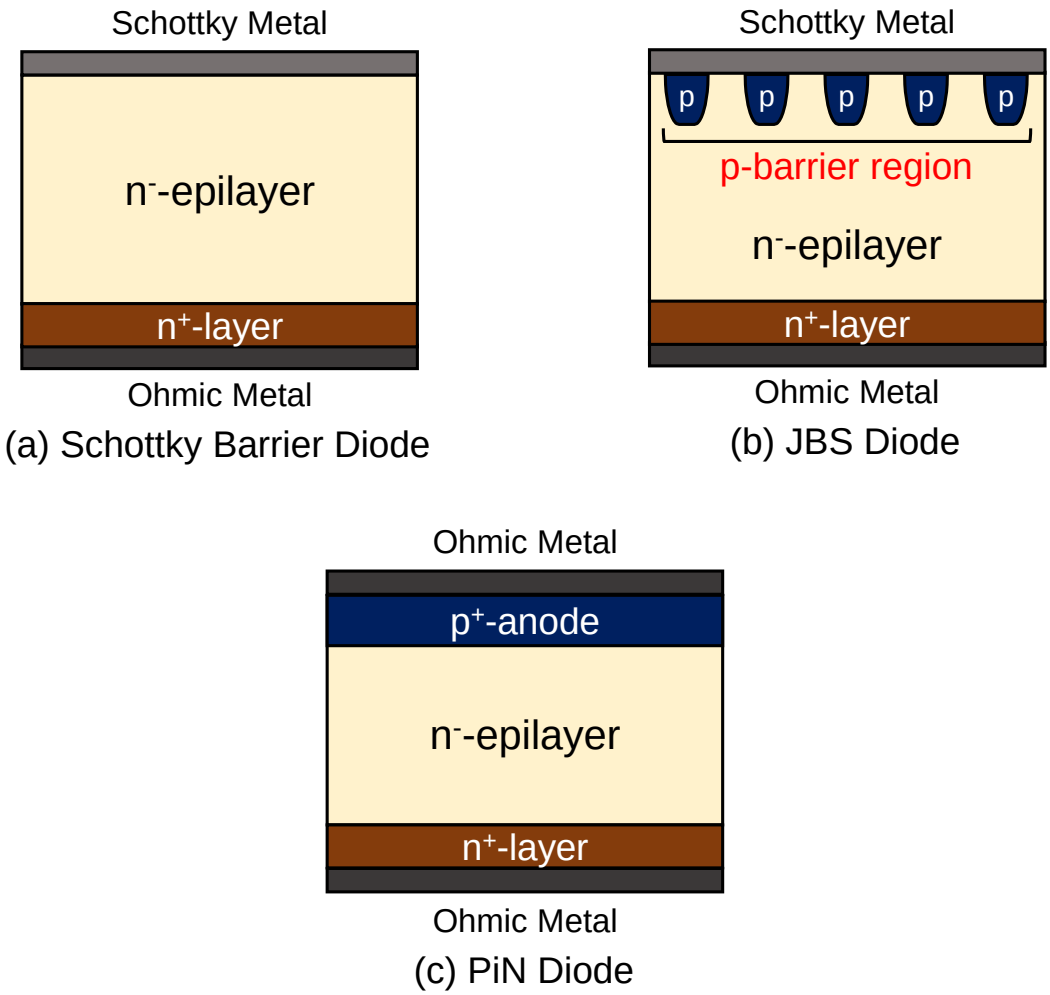


Figure 1.4: Schematic illustration of (a) SBD, (b) JBS, and (c) PiN diodes.

regions are locally formed on the surface of epilayer. When a reverse bias is applied, the depletion regions from the pn junction will merge under the Schottky region, which results in the reduction of electric field at the Schottky interface. By using a JBS structure, reverse leakage current can be drastically reduced to the level of PiN diodes. In recent years, a trench JBS structure has been proposed to further reduce the leakage current or maintain the low leakage current even for metals with low Schottky barrier height [64].

In addition, there have been numerous fundamental studies in SiC SBD to improve its device performance. Using technologies obtained in these studies, a SBD with breakdown voltage over 10 kV [62, 65], and a 600 V-class SBD with an extremely low on-resistance of 0.22 $m\Omega cm^2$ [66] have been demonstrated. Furthermore, inverters employing SiC SBDs have shown great improvement of efficiency while reducing its system size, although conventional Si IGBTs are still used [67, 68]. These impressive results will spread the use of SiC SBDs as a replacement of Si PiN diodes, and will help reduce the power dissipation of the electric converter systems.

From the superior performance of SiC SBD, adoption of 600–1200 V-class devices is widely spreading nowadays. However, in an UHV region where breakdown voltage over 10 kV is required, even a SiC SBD cannot escape from the high on-resistance causing a large conduction loss. Therefore, in such a high voltage application, a PiN diode is attractive owing to the low on-resistance by the conductivity modulation effect. Schematic structure of PiN diode is shown in Fig. 1.4(c), where a p^+-anode layer is formed on the voltage-blocking layer (n^--layer) with low doping concentration. During the forward operation, minority carriers are injected from the anode layer into the lightly doped voltage-blocking layer and exceeds the original carrier concentration of it (Fig. 1.5). Subsequently, to maintain the charge neutrality, majority carriers are also injected from the cathode side which results in carrier concentration larger than the doping concentration of voltage-blocking layer. The larger carrier concentration will mean lower on-resistance than the unipolar on-resistance. However, storage of the carrier in the voltage blocking layer will cause large tail current at reverse recovery, which results in a large switching loss. Therefore, PiN diodes are commonly used in the voltage region where conduction loss of SBD is severely large, or in a low frequency where switching loss can be neglected.

Investigations on SiC PiN diodes are still widely going on. In the early stage, SiC pn diodes were studied focusing on high-temperature operation and blue light-emitting diodes, but in the 1990s, studies focusing on power device have started [69]. At first, 6H-SiC was used and a high breakdown voltage of 2 kV in 1994 [70], and 4.5 kV in 1995 [71] was realized by increasing the voltage-blocking layer thickness. However, because catastrophic failure had occurred at mesa periphery for these devices, studies on edge terminations have started which focuses on achieving high breakdown voltage the SiC potentially has [72]. In 1997 and 1998, Mitlehner *et al.* have fabricated a 4H-SiC pn diode with implanted anode and edge termination [73, 74]. During the high temperature measurement of reverse characteristics, they observed a positive temperature coefficient of breakdown voltage, which indicates that

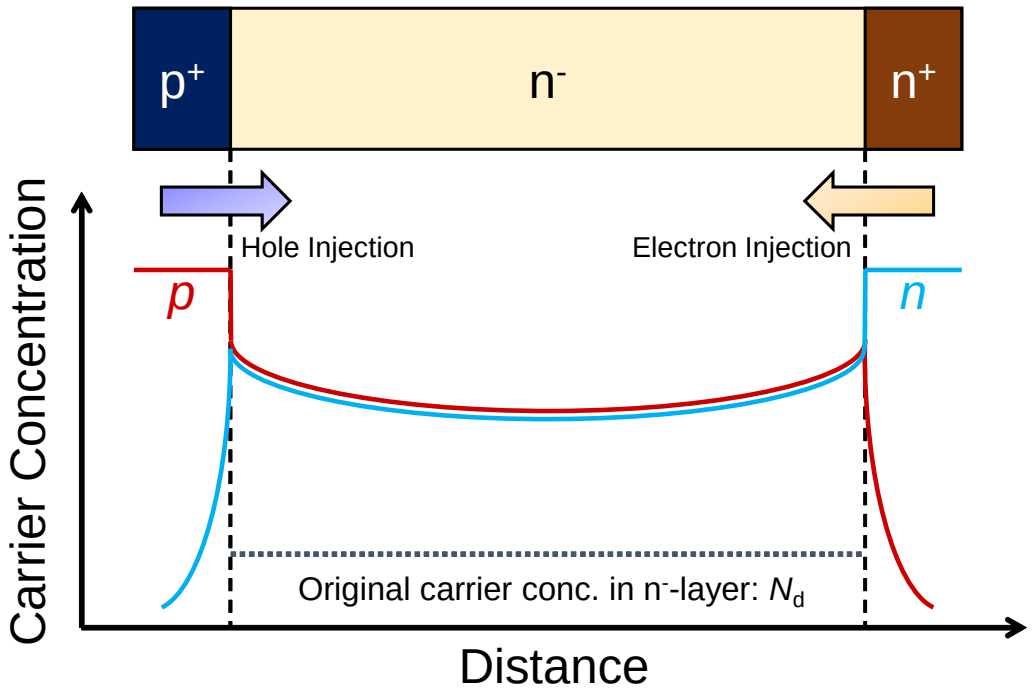


Figure 1.5: Schematic illustration of conductivity modulation effect in a PiN diode.

the breakdown mechanism of pn junction in SiC to be avalanche breakdown. Because the positive temperature coefficient of breakdown voltage is one of the most important requirements for a power device, it encouraged the application of SiC as a power device. Finally in 2001, a large breakthrough was done by Sugawara *et al.*, where they have demonstrated a 19.5 kV 4H-SiC PiN diodes with low on-resistance and fast switching [75]. This extremely high breakdown voltage of 19.5 kV is physically impossible to fabricate with Si, and it indicates the superior physical properties of SiC. Furthermore, this UHV device has enhanced the promise of UHV SiC devices to be used in future electrical power systems.

For the forward characteristics, many studies have been performed such as investigations for the p^+-anode formation process (Al, B implantation [76] or epitaxial growth [77]), but the largest problem has been the extremely short carrier lifetime (<1 μs) in SiC in spite of the indirect bandgap [78, 79]. When a carrier lifetime is too short, recombination of carriers will occur as soon as they are injected, causing smaller storage of carriers inside the voltage-blocking layer. Because the effect of conductivity modulation is weaker in this case, enough reduction of on-resistance does not occur. In 2007, Danno *et al.* clarified that the deep level which limits the carrier lifetime to be $Z_{1/2}$-center [80], which was found to be a carbon vacancy [81, 82]. Then in 2008, Storasta *et al.* have shown that the $Z_{1/2}$-center could be eliminated by carbon ion implantation followed by high temperature annealing [83]. In addition, Hiyoshi *et al.* have also discovered that high temperature oxidation can also eliminate the $Z_{1/2}$-center [84, 85], resulting in a long carrier lifetime of 20–30 μs [86]. Although PiN diodes using these methods showed extremely low on-resistance and forward voltage drop [87, 88], too long carrier lifetime caused large reverse recovery characteristics [89]. Therefore, in recent years, studies on controlling the $Z_{1/2}$-density is going on to control carrier lifetimes for the best trade-off between static and switching characteristics of PiN diodes [90–92].

In addition to the forward characteristics, another problem SiC PiN diodes face is the bipolar degradation [93–95]. When a PiN diode is forward biased, recombination of the injected carriers triggers expansion of a single Shockley stacking fault (SSF) at the location of a basal plane dislocation (BPD). The expanded SSF significantly increases the forward voltage drop and the leakage current, which degrades the long-term reliability of the device. To solve this problem, significant efforts have been made to reduce the BPD density inside the epilayer [96–98]. In recent studies, use of low off-angle substrates is becoming a promising method, where epitaxial growth with only 1 BPD in a quarter of 3 inch substrate has been demonstrated [98]. Although more studies may be needed, it should be completely solved as it was in $Z_{1/2}$-center.

By solving various problems occurring in PiN diodes, development of SiC PiN diodes is on the way. However, although *"demonstration"* of SiC PiN diodes can be realized, many fundamental studies are still required toward the further improvement of the performance and reliability.

Transistors: MOSFETs and IGBTs

Regarding switching transistors, the general trend is the MOS-gated power devices which can be controlled by applying voltage to the gate. Because SiC can produce silicon dioxide (SiO_2) by thermal oxidation as in Si, this is a large advantage compared with other wide-bandgap materials in terms of device fabrication. The development of SiC MOS-based devices has been going on for mainly unipolar switching devices such as MOSFETs targeting 600–3300 V-class. In recent years, for UHV (>10 kV) application, development of UHV MOSFETs or bipolar devices such as IGBTs have started in a research stage.

The development of SiC MOSFETs has been equivalent to the investigation of MOS interface for more than 20 years. Since the first inversion-mode 6H-SiC MOSFETs [99], the performances of SiC MOSFETs had been limited by its low inversion channel mobility of about several cm^2/Vs [21]. In the last decades, several successful developments to enhance the channel mobility have been proposed. The process most widely used is the post-oxidation annealing in NO or N_2O [100–103], and furthermore, annealing in $POCl_3$ is also effective for reducing the interface states [104, 105]. In contrast to the post-oxidation annealing, use of other crystal faces such as $(11\bar{2}0)$ and $\{03\bar{3}8\}$ has also improved the channel mobility [106–108].

Development of vertical SiC switching devices started in the early 1990s. The first power MOSFET was demonstrated by Palmour *et al.* in 1993 using a trench MOS structure, although the blocking voltage was about 50 V [109]. Since then, several innovative studies have been conducted to improve its performance [110, 111], but from the late 1990s, the planar double implanted MOSFETs (DMOSFETs) have become the mainstream. The first SiC DMOSFET was demonstrated by Shenoy *et al.* in 1997 with a breakdown voltage of 760 V [112]. Following that demonstration, a number of groups have shown unique methods to improve the performances such as original self-align process to realize a short channel [113], or utilizing an epitaxial layer for the channel layer [114, 115]. These studies have encouraged the commercialization of SiC MOSFETs in 2010 by Rohm and Cree (now Wolfspeed), followed by other companies such as STMicroelectronics. Furthermore, SiC DMOSFETs with breakdown voltage up to 15 kV have been demonstrated toward UHV applications requiring a high switching speed [116]. In recent years, development of trench MOSFET have started again, which mainly focuses on the oxide breakdown issues [117–120]. Particularly, Nakamura *et al.* have demonstrated a 600 V-class trench MOSFET with extremely low on-resistance of 0.79 $m\Omega cm^2$ by introducing the unique double-trench structure [117].

For UHV application, SiC IGBTs have been developed in recent years. The first SiC IGBT was demonstrated in 1996 using an UMOS structure [121]. However, the device improvement was rather slow compared with MOSFET. Because a p^+-substrate of SiC has high resistivity due to the relatively-low carrier concentration, development of IGBT was mainly p-channel IGBTs [122–124]. However, Wang *et al.* have developed a method of

fabricating n-channel device using a free standing epilayer [125]. From the comparison of p- and n-IGBTs, it was shown that n-IGBT can achieve better performances due to the higher channel mobility [126], and recently, 16.5 kV n-IGBT was demonstrated with low on-resistance of 14 mΩcm^2 [127].

Although high-performance MOS-based devices have been demonstrated, there are still issues that need to be solved. Absolutely, the low channel mobility is the largest problem, and at the same time, the physical origin of the interface states and the reason why mobility enhancement process such as nitridation actually works have to be clarified. In addition, oxide reliability issues particularly at elevated temperatures are a big challenge [128, 129]. Furthermore, bipolar degradation has to be solved for both IGBTs and MOSFETs, because bipolar operation of body diodes in MOSFET will cause SSF expansion, which will degrade the MOSFET performance, too [130].

Other switching devices such as junction FETs (JFETs) or BJTs which do not use MOS structure have been also investigated by many groups [131–137]. However, each of the devices possesses a unique problem, and much more fundamental studies are required.

1.3 Key Issues of Ultrahigh-Voltage SiC Power Devices and Aim of this Thesis

By years of research, 600–1200 V-class SiC unipolar devices such as SBD, MOSFET, and JFET are in the market, and is showing the excellent performance in reducing the power dissipation. On the other hand, although UHV devices with breakdown voltage over 10 kV have been demonstrated in the past, they are still in the research stage and numerous issues are remaining to be solved. Therefore, fundamental studies on UHV SiC devices are essential for improving their characteristics, which will contribute to the efficiency improvement of power converters especially for the future power distribution and transmission systems. Moreover, these studies will be indispensable for further understanding of device physics in SiC devices.

Among a number of issues which UHV SiC devices face, this thesis focuses on studies toward the improvement of both reverse and forward characteristics of SiC PiN diodes. For the reverse characteristic, a problem of the undetermined values of impact ionization coefficients is studied, followed by extensive studies of edge termination structure for achieving ultrahigh-breakdown voltage. For the forward characteristics, a problem of high built-in potential in bipolar devices is challenged by introducing the concept of hybridization of unipolar and bipolar devices.

1.3.1 Impact Ionization Coefficients in SiC

In a power device, one of the most important characteristics is the breakdown voltage. Two main mechanisms of breakdown in a semiconductor junction is the "avalanche multiplication" and the "tunneling" [54]. As explained in the previous section, the breakdown mechanism of pn-junction used in SiC power devices was found to be avalanche breakdown. Therefore, fundamental studies on avalanche breakdown mechanism are particularly important to accurately predict the breakdown voltage of a power device, such as in a device simulation.

In avalanche breakdown, the important physical property is the impact ionization coefficients. Impact ionization coefficients are defined as the number of electron-hole pairs generated by a carrier per unit distance, and it is a function of electric field and temperature [54]. Using impact ionization coefficients, the breakdown voltage of a device can be calculated by applying following equations to the depletion layer [54]:

$$\int_0^W \beta \cdot \exp\left[-\int_0^x (\beta - \alpha) dx'\right] dx = 1 \tag{1.2}$$

$$\int_0^W \alpha \cdot \exp\left[-\int_x^W (\alpha - \beta) dx'\right] dx = 1. \tag{1.3}$$

Here, W is the depletion layer width and α, β are electron and hole impact ionization coefficients, respectively. The left hand side of equation (1.2) and (1.3) are called the ionization integral, and when it becomes unity, avalanche breakdown occurs. In calculation of breakdown voltage, the ionization integral is calculated while the reverse bias voltage is increased to find the voltage where the integral becomes unity.[1]

The determination of impact ionization coefficients was first performed in Si by McKay *et al.* in 1953 [138]. Since then, studies based on both experiments and theory have been conducted in many semiconductor materials such as Si or GaAs [139–144]. For SiC, the first determination was performed by Glover in 1975, using an Au/6H-SiC Schottky junctions [145]. However, this study assumed the ionization coefficients for electrons and holes to be equal, which is actually not true. Furthermore, crystal quality in that age is not perfect enough to obtain accurate ionization coefficients by the measurement. The first reliable experiment was not conducted until 1997, where Konstantinov *et al.* [146] and Raghunathan *et al.* [147] have reported at the same time. Since then, there have been several experimental studies to determine the ionization coefficients in SiC [146, 148–150]. Figure 1.6 shows some of the reported ionization coefficients up to now in 4H-SiC. As can be seen, there are large variations between the reported results. Using the ionization coefficients shown in Fig. 1.6, doping concentration dependence of ideal breakdown voltage for p^+n non-punchthrough structure was calculated and is shown in Fig. 1.7. The large variation between

[1] Here, it should be noted that the critical electric field explained in Section 1.2 does not reflect physics of breakdown. As it will be explained precisely in Chapter 2, the critical electric field changes by the device structure employed. Toward the accurate calculation, the impact ionization coefficients are essential.

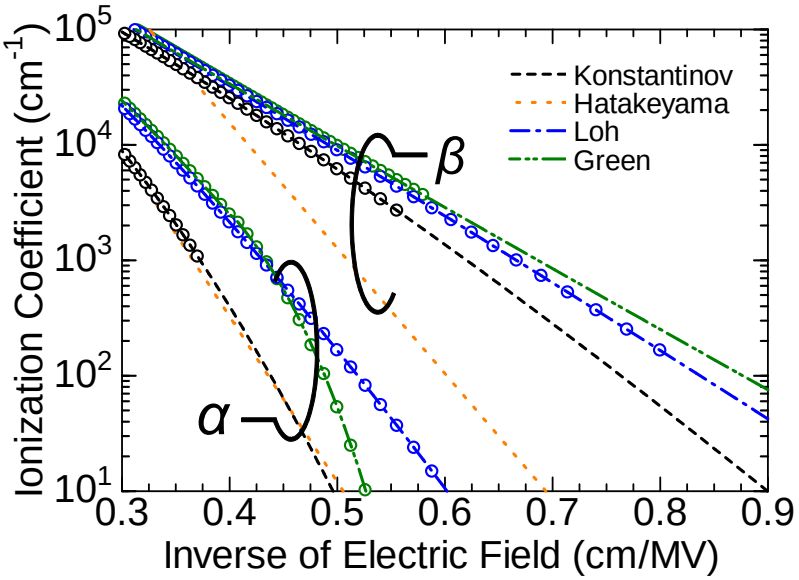


Figure 1.6: Some of the reported impact ionization coefficients in SiC [146, 148–150]. Here, α and β are electron and hole impact ionization coefficients, respectively. Symbols: measured ionization coefficients. Lines: calculation result of the fitting equations.

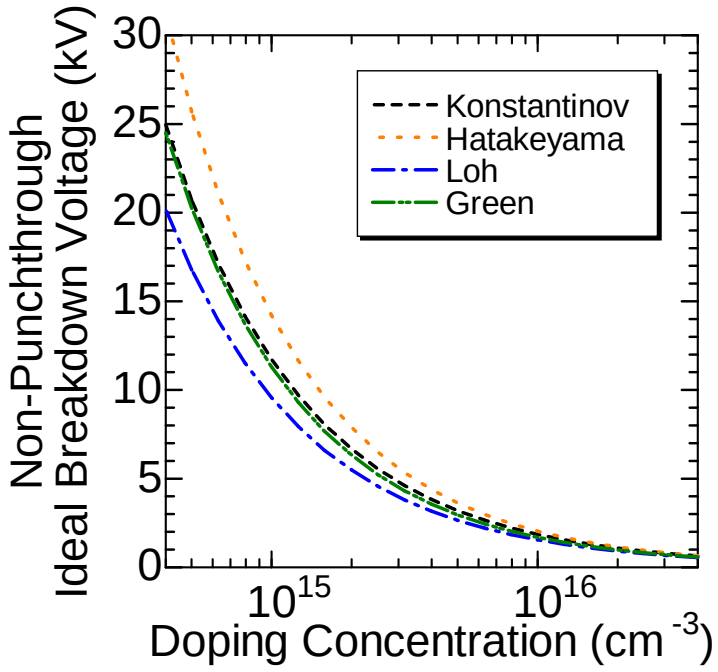


Figure 1.7: Doping concentration dependence of ideal breakdown voltage for non-punchthrough SiC p^+n structure, calculated by using impact ionization coefficients from [146, 148–150].

the reported ionization coefficients has caused large variation of calculated ideal breakdown voltage, especially for UHV devices.

As will be discussed in Chapter 2, there are problems in the measurement or analysis method for the reported ionization coefficients. In addition, experimental studies of ionization coefficients focusing on electric field range important for UHV devices have not been conducted yet. To realize the accurate calculation of breakdown voltage, especially in complicated structures of real power devices, the ionization coefficients must be accurately determined in a wide range of electric field. Moreover, toward further understanding of high-field physics of SiC, the accurate electric field dependence is essential.

1.3.2 Electric Field Crowding and Edge Termination Structures

In a real power device structure, it is not like the one-dimensional structure shown in Fig. 1.4, but is two- or three-dimensional structure which produces an "edge" at the end of the junction. For example, in a planar p^+n diode, the edge of the device does have a rounded corner as shown in Fig. 1.8. When such a curvature exists, the depletion region is narrower at the corner which result in a higher electric field strength in the region. This effect is often called as electric field crowding, which causes a premature breakdown of a power device [151]. Therefore, when designing a power device, the key technology for obtaining high breakdown voltage is the proper designing of edge termination structure.

Edge termination is an indispensable structure when fabricating a power device to alleviate the electric field crowding. Figure 1.9 shows some of the typical structures used for edge termination. Figure 1.9(a) is a field plate structure, where a contact metal is extended above the field oxide [152]. The reverse bias to the anode metal will expand the depletion layer at the outer edge of p^+-region, which reduces the electric field crowding. The variables for this structure are the length of the extended metal and the thickness and material of the field oxide. Figure 1.9(b) is a guard ring structure, where highly doped p^+-regions are formed around the p^+-anode region with a space between the neighboring p^+-regions [153, 154]. These p^+-rings will expand the depletion layer at the outer edge of p^+-anode region, which reduces the electric field crowding occurring at the p^+-anode edge. Here, the space and ring width needs be optimized to efficiently alleviate the electric field crowding. Figure 1.9 (c) is a junction termination extension (JTE) structure, where a moderately-doped p-layer is formed around the p^+-anode [155]. Because the JTE-region will deplete at reverse bias, a depletion layer will expand to the outer edge and electric field crowding occurring at the p^+-anode edge will be alleviated. At last, Fig. 1.9(d) is a positive bevel termination, where more material is removed from the edge of lightly doped side in the pn junction [154]. In this structure, the depletion layer width at the surface of the periphery is wider than that inside the diode. Because the same voltage is being supported across the depletion layer, the electric field at the periphery is reduced, in other words, electric field crowding does not occur.

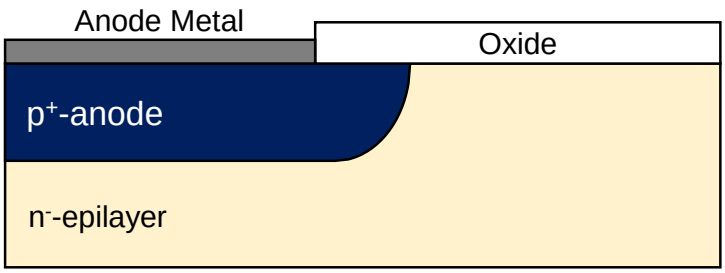


Figure 1.8: Schematic cross section near the edge of p^+n region in a real planar PiN diode structure.

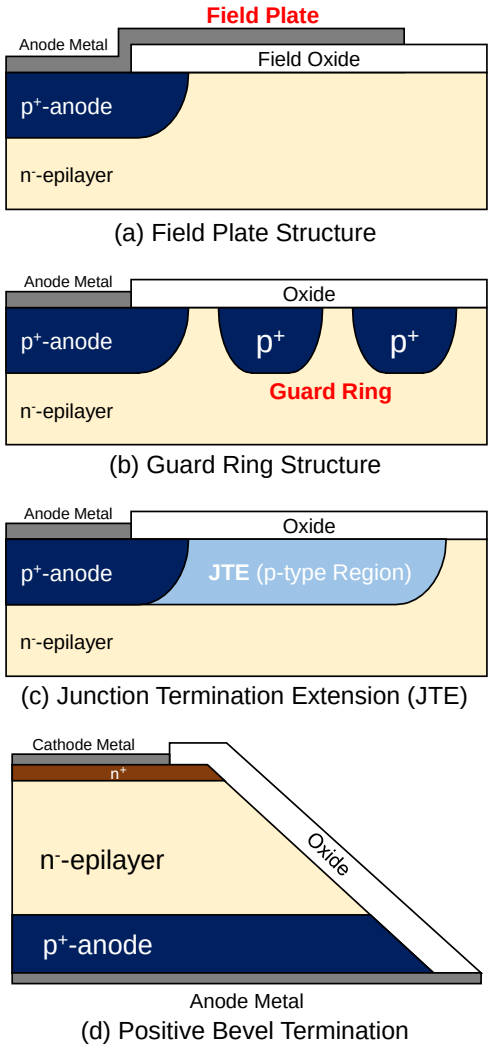


Figure 1.9: Schematic cross section near the edge of p^+n region for various edge termination structures used in PiN diodes.

Each of these structures has both advantages and disadvantages. For the field plate and guard ring, the advantage is the convenient fabrication process where it can be formed by simply changing the photolithography mask. However, disadvantage is the very few variable that can be changed in the structure. This makes difficulties during optimization of the structure to effectively alleviate the electric field crowding. In addition, because SiC handles 10 times higher electric field strength than Si, breakdown of field oxide can easily occur by the high electric field when a similar structure in Si was used in SiC. For JTE, advantage is the large number of variables that can be changed, such as its dose and design geometry. However, additional implantation is needed when fabricating a JTE, which is a disadvantage compared with the field plate and guard ring. For a positive bevel termination, although it can completely alleviate the electric field crowding, the device structure to which it can be applied is very few. Furthermore, it can only be used in a non-punchthrough structure, which is not the case for standard UHV devices where a punchthrough structure is usual. Among these edge termination structures, JTE-based structure is the most promising from its efficiency to the electric field crowding alleviation. Although it may require an additional step in the fabrication, the advantage will overcome the disadvantage.

From its effectiveness of JTE, a number of studies have been conducted in SiC [156–160]. However, these studies have been mainly based on a few kV-class devices, and fundamental studies targeting UHV devices are very scarce. Because UHV devices need larger area of JTE (will be shown in Chapter 3) and electric field strength is lower than a few kV-class devices, direct adoption of JTEs used in a few kV-class devices are not useful. Therefore, extensive studies on JTE using UHV devices are required.

1.3.3 Forward Conduction Loss of Bipolar Devices

In bipolar devices, forward conduction loss can be reduced by improving the on-resistance. For SiC PiN diodes, extremely low on-resistance can be realized through the lifetime-enhancement process as explained in the previous section. However, bipolar devices in a wide bandgap semiconductor have one critical disadvantage: The wide bandgap causes a large built-in potential leading to a relatively high forward voltage drop. In SiC, built-in potential of $\sim$3 V needs to be applied before it can flow the current with a low on-resistance. Therefore, if the operating current density is low, bipolar devices can have a larger conduction loss than unipolar devices, although enough conductivity modulation may be occurring.

One solution to solve this problem is the integration of unipolar and bipolar devices in a single chip, in other words, assuming a hybrid operation where unipolar operation is used at low current density and bipolar operation is used at high current density. This idea has been proposed in Si transistors, where MOSFET operation and IGBT operation have been integrated in a single chip [161–163]. One example of such a device is the Hybrid Unipolar Bipolar Field Effect Transistor (HUBFET) proposed by Donnellan *et al.* in 2012. Figure 1.10 shows the schematic structure and schematic figure of forward characteristics

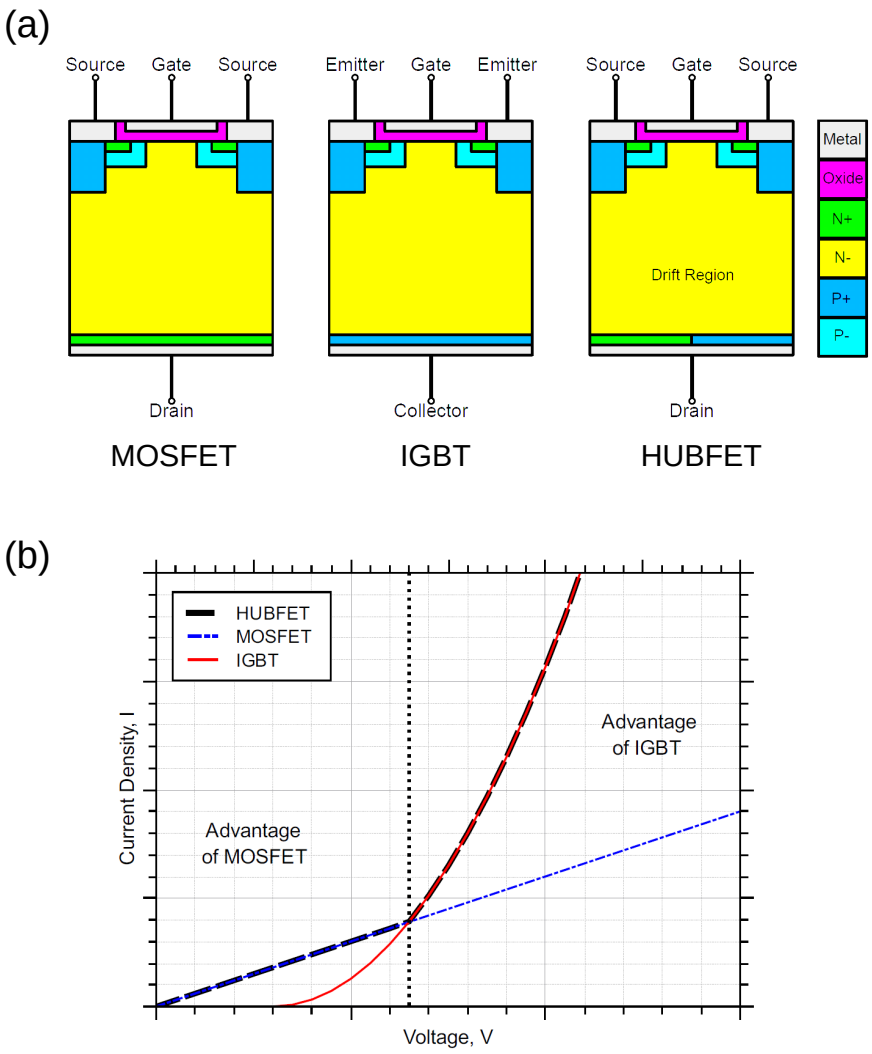


Figure 1.10: (a) Schematic cross section and (b) schematic illustration of forward $I-V$ characteristics of MOSFET, IGBT, and HUBFET taken from [163].

of MOSFET, IGBT, and HUBFET from [163]. In a HUBFET, the drain/collector region has a highly doped n^+-region as a MOSFET in one part, and p^+-region as an IGBT in another part. During the forward operation, the MOSFET part of the device will operate at low forward bias, and when the forward bias becomes sufficiently large, the IGBT part turns on and conductivity modulation starts. The fabricated HUBFET was compared to an IGBT in an inductive switching test, and showed reduction of turn-off loss at the low current because of the MOSFET operation.

The concept of hybrid operation may have large impacts in SiC because of the large built-in potential. Not only the switching loss, but also the conduction loss at low current density may be largely reduced compared with conventional bipolar devices. Although using a separate unipolar and bipolar devices in parallel may result in a similar result, it will increase the system cost dramatically because of the large epi-wafer cost of SiC. Therefore, combining them into a single chip will be effective in terms of both cost and efficiency. However, application of this concept in SiC will need fundamental studies before it can be actually used in real SiC power devices.

1.4 Outline of This Study

In this thesis, experimental studies are presented to solve the issues explained in the previous section, which are the undetermined values of impact ionization coefficients, extensive studies of edge termination structures for UHV devices, and fundamental studies on hybrid operating devices using a pn-diode for conduction loss reduction in bipolar devices. These investigations will serve as a basis for improvement of UHV SiC devices, and for further understanding of device physics in SiC devices. Because a pn-diode is the most fundamental structure of a power device, the obtained insight can be easily applied to the other complicated devices such as MOSFETs or IGBTs.

In Chapter 2, impact ionization coefficients in SiC are determined by photomultiplication measurement using SiC photodiodes. By using various multiplication layer structures, the impact ionization coefficients are determined in a wide range of electric field of 1.0–3.2 MV/cm. In particular, impact ionization coefficients at low electric field down to 1 MV/cm are determined for the first time in SiC. Values at this low electric field range is particularly important for designing UHV devices. In addition, the temperature dependence is accurately measured for the first time in SiC up to 150°C, where an unusual temperature dependence is observed in electron impact ionization coefficients. Then, by using the obtained impact ionization coefficients, the critical electric field strength and ideal breakdown voltage of SiC are calculated.

In Chapter 3, an edge termination structure, especially, JTE-based termination is extensively studied using UHV PiN diodes. First, breakdown characteristics of 10 kV-class SiC PiN diodes with various JTE structures are experimentally studied. The JTE-dose

dependence of breakdown voltage for a conventional single-zone JTE applied to UHV PiN diodes is extensively investigated by both experiment and numerical device simulation. The effect of interface charge on the JTE-dose dependence of breakdown voltage is especially discussed here, and the importance of optimum JTE-dose window is clarified. To overcome the negative effect of interface charge, space-modulated JTE (SM-JTE) is introduced in this study, and its effect is experimentally studied for the first time. By the optimization of SM-JTE structure, a 20 kV-class SiC PiN diode is demonstrated to show the superior potential of SiC as a UHV power device.

In Chapter 4, a hybrid operating device in SiC is demonstrated. As the first step of such a device, a UHV merged-PiN-Schottky (MPS) diode with epitaxial p^+-anode layer is proposed to reduce both the unipolar and bipolar on-resistance. First, each of the component structures of the mesa MPS diode, which are the voltage-blocking layer, JBS region, edge termination, and mesa structure, has been investigated through analytical modeling and device simulation. In this study, a snapback phenomenon in the MPS diode is especially investigated. To predict and explain the snapback phenomenon, an analytical model is proposed in this study, which is compared with the device simulation and experiment to investigate the validity. In addition, forward characteristics of MPS diodes without the snapback phenomenon are investigated and design guidelines of hybrid operating MPS diodes are presented. Furthermore, using the SM-JTE studied in Chapter 3, a 10 kV-class SiC MPS diode is demonstrated.

In Chapter 5, this thesis is summarized and suggestions for the future study are provided.

References

[1] National Police Agency of Japan, *Damage Situation and Police Countermeasures associated with 2011Tohoku district–off the Pacific Ocean Earthquake*, http://www.npa.go.jp/archive/keibi/biki/higaijokyo_e.pdf.

[2] M. S. Adler, K. W. Owyang, B. J. Baliga, and R. A. Kokosa, *IEEE Transactions on Electron Devices* **31**, 1570 (1984).

[3] J. Bardeen and W. H. Brattain, *Physical Review* **74**, 230 (1948).

[4] J. A. Hoerni, *Technical Digest on International Electron Devices Meeting* **6** (1960) p. 50.

[5] J. L. Moll, M. Tanenbaum, J. M. Goldey, and N. Holonyak, *Proceedings of the IRE* **44** (1956) p. 1174.

[6] J. M. Goldey, I. M. Mackintosh, and I. M. Ross, *Solid-State Electronics* **3**, 119 (1961).

[7] R. D. Josephy, *Philips Technical Review* **31**, 251 (1970).

[8] V. A. K. Temple and R. P. Love, *Technical Digest on International Electron Devices Meeting* **24** (1978) p. 664.

[9] B. J. Baliga, M. S. Adler, P. V. Gray, R. P. Love, and N. Zommer, *Technical Digest on International Electron Devices Meeting* **28** (1982) p. 264.

[10] A. Nakagawa, H. Ohashi, M. Kurata, H. Yamaguchi, and K. Watanabe, *Technical Digest on International Electron Devices Meeting* **30**, (1984) p. 860.

[11] D. Ueda, H. Takagi, and G. Kano, *IEEE Transactions on Electron Devices* **32**, 2 (1985).

[12] B. J. Baliga, *Technical Digest on International Electron Devices Meeting* **32** (1986) p. 102.

[13] M. Kitagawa, I. Omura, S. Hasegawa, T. Inoue, and A. Nakagawa, *Technical Digest on International Electron Devices Meeting* (1993) p. 679.

[14] H. Takahashi, H. Haruguchi, H. Hagino, and T. Yamada, *Proceeding of 8th International Symposium on Power Semiconductor Devices and ICs* (1996) p. 349.

[15] T. Fujihira, *Japanese Journal of Applied Physics* **36**, 6254 (1997).

[16] X.-B. Chen, X. Wang, and J. K. O. Sin, *IEEE Transactions on Electron Devices* **47**, 1280 (2000).

[17] Y. C. Liang, K. P. Gan, and G. S. Samudra, *IEEE Electron Device Letters* **22**, 407 (2001).

[18] S. Fujita, *Japanese Journal of Applied Physics* **54**, 030101 (2015).

[19] M. Bhatnagar and B. J. Baliga, *IEEE Transactions on Electron Devices* **40**, 645 (1993).

[20] H. Matsunami and T. Kimoto, *Material Science and Engineering* **R20**, 125 (1997).

[21] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, *IEEE Transactions on Electron Devices* **49**, 658 (2002).

[22] T. Kimoto, *Japanese Journal of Applied Physics* **54**, 040103 (2015).

[23] B. Baliga, *IEEE Electron Device Letters* **10**, 455 (1989).

[24] R. C. Marshall, J. W. Faust, Jr., and C. E. Ryan, *Silicon Carbide 1973*, University of South Carolina Press, 1974.

[25] J. A. Lely, *Berichte der Deutschen Keramischen Gesellschaft* **32**, 229 (1955).

[26] Y. M. Tairov and V. F. Tsvetkov, *Journal of Crystal Growth* **43**, 209 (1978).

[27] Y. M. Tairov and V. F. Tsvetkov, *Journal of Crystal Growth* **52**, 146 (1981).

[28] A. Powell, J. Sumakeris, Y. Khlebnikov, M. Paisley, R. Leonard, E. Deyneka, S. Gangwal, J. Ambati, V. Tsevtkov, J. Seaman, A. McClure, J. Guo, M. Dudly, E. Balkas, and V. Balakrishna, *Extended Abstract of 16 th International Conference on Silicon Carbide and Related Materials*, Mo–2B–1 (2015).

[29] D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori, *Nature* **430**, 1009 (2004).

[30] N. Kuroda, K. Shibahara, W. Yoo, S. Nishino, and H. Matsunami, *Extended Abstracts of the 19th Conference on Solid State Devices and Materials*, 227 (1987).

[31] T. Ueda, H. Nishino, and H. Matsunami, *Journal of Crystal Growth* **104**, 695 (1990).

[32] U. Forsberg, O. Danielsson, A. Henry, M. K. Linnarsson, and E. Janzén, *Journal of Crystal Growth* **236**, 101 (2002).

[33] U. Forsberg, O. Danielsson, A. Henry, M. K. Linnarsson, and E. Janzén, *Journal of Crystal Growth* **253**, 340 (2003).

[34] T. Hori, K. Danno, and T. Kimoto, *Journal of Crystal Growth* **306**, 297 (2007).

[35] M. Ito, L. Storasta, and H. Tsuchida, *Applied Physics Express* **1**, 015001 (2008).

[36] Y. Ishida, T. Takahashi, H. Okumura, K. Arai, and S. Yoshida, *Materials Science Forum* **600-603**, 119 (2009).

[37] F. La Via, G. Galvagno, G. Foti, M. Mauceri, S. Leone, G. Pistone, G. Abbondanza, A. Veneroni, M. Masi, G. L. Valente, and D. Crippa, *Chemical Vapor Deposition* **12**, 509 (2006).

[38] H. Pedersen, S. Leone, O. Kordina, A. Henry, S. Nishizawa, Y. Koshka, and E. Janzén, *Chemical Reviews* **112**, 2434 (2012).

[39] Y. A. Vodakov and E. N. Mokhov, *Silicon Carbide 1973*, University of South Carolina Press, 1974.

[40] S. Yaguchi, T. Kimoto, N. Ohyama, and H. Matsunami, *Japanese Journal of Applied Physics* **34**, 3036 (1995).

[41] M. A. Capano, R. Santhakumar, R. Venugopal, M. R. Melloch, and J. A. Cooper, Jr., *Journal of Electronic Materials* **29**, 210 (2000).

[42] T. Kimoto, A. Itoh, H. Matsunami, T. Nakata, and M. Watanabe, *Journal of Electronic Materials* **25**, 879 (1996).

[43] T. Kimoto and N. Inoue, *physica status solidi (a)* **162**, 263 (1997).

[44] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, J. Heindl, H. P. Strunk, and M. Maier, *physica status solidi (a)* **162**, 277 (1997).

[45] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, *Journal of Applied Physics* **96**, 224 (2004).

[46] L. M. Porter and R. F. Davis, *Materials Science and Engineering: B* **34**, 83 (1995).

[47] J. Crofton, L. M. Porter, and J. R. Williams, *physica status solidi (b)* **202**, 581 (1997).

[48] F. Roccaforte, F. La Via, and V. Raineri, *International Journal of High Speed Electronics and Systems* **15**, 781 (2005).

[49] J. R. Waldrop and R. W. Grant, *Applied Physics Letters* **62**, 2685 (1993).

[50] A. Itoh, T. Kimoto, and H. Matsunami, *IEEE Electron Device Letters* **16**, 280 (1995).

[51] M. Bhatnagar, P. McLarty, and B. Baliga, *IEEE Electron Device Letters* **13**, 501 (1992).

[52] T. Kimoto, T. Urushidani, S. Kobayashi, and H. Matsunami, *IEEE Electron Device Letters* **14**, 548 (1993).

[53] A. Itoh, T. Kimoto, and H. Matsunami, *Proceeding of 7th International Symposium on Power Semiconductor Devices and ICs* (1995) p. 101.

[54] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley, 2007.

[55] T. Hatakeyama and T. Shinohe, *Materials Science Forum* **389-393**, 1169 (2002).

[56] T. Katsuno, Y. Watanabe, H. Fujiwara, M. Konishi, H. Naruoka, J. Morimoto, T. Morino, and T. Endo, *Applied Physics Letters* **98**, 222111 (2011).

[57] H. Fujiwara, H. Naruoka, M. Konishi, K. Hamada, T. Katsuno, T. Ishikawa, Y. Watanabe, and T. Endo, *Applied Physics Letters* **100**, 242102 (2012).

[58] F. Dahlquist, C. Zetterling, M. Östling, and K. Rottner, *Materials Science Forum* **264-268**, 1061 (1998).

[59] R. Held, N. Kaminski, and E. Niemann, *Materials Science Forum* **264-268**, 1057 (1998).

[60] R. Singh, D. C. Capell, A. R. Hefner, J. Lai, and J. W. Palmour, *IEEE Transactions on Electron Devices* **49**, 2054 (2002).

[61] R. Rupp, M. Treu, S. Voss, F. Björk, and T. Reimann, *Proceeding of 18th International Symposium on Power Semiconductor Devices and ICs* (2006) p. 1.

[62] B. Hull, J. Sumakeris, M. O'Loughlin, Q. Zhang, J. Richmond, A. Powell, E. Imhoff, K. Hobart, A. Rivera-Lopez, and A. Hefner, *IEEE Transactions on Electron Devices* **55**, 1864 (2008).

[63] L. Zhu and T. P. Chow, *IEEE Transactions on Electron Devices* **55**, 1857 (2008).

[64] M. Aketa, Y. Yokotsuji, M. Miura, and T. Nakamura, *Materials Science Forum* **717-720**, 933 (2012).

[65] J. H. Zhao, P. Alexandrov, and X. Li, *IEEE Electron Device Letters* **24**, 402 (2003).

[66] T. Sakaguchi, M. Aketa, Y. Miura, H. Asahara, and T. Nakamura, *Extended Abstract of 15 th International Conference on Silicon Carbide and Related Materials*, Tu–P–59 (2013).

[67] Z. Liang, B. Lu, J. D. van Wyk, and F. C. Lee, *IEEE Transactions on Power Electronics* **20**, 679 (2005).

[68] T. Duong, A. Hefner, K. Hobart, S. Ryu, D. Grider, D. Berning, J. Ortiz-Rodriguez, E. Imhoff, and J. Sherbondy, *26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)* (2011) p. 1057.

[69] L. G. Matus, J. A. Powell, and C. S. Salupo, *Applied Physics Letters* **59**, 1770 (1991).

[70] P. G. Neudeck, D. J. Larkin, J. A. Powell, L. G. Matus, and C. S. Salupo, *Applied Physics Letters* **64**, 1386 (1994).

[71] O. Kordina, J. P. Bergman, A. Henry, E. Janzén, S. Savage, J. Andre, L. P. Ramberg, U. Lindefelt, W. Hermansson, and K. Bergman, *Applied Physics Letters* **67**, 1561 (1995).

[72] D. Peters, R. Schorner, K. H. Holzlein, and P. Friedrichs, *Applied Physics Letters* **71**, 2996 (1997).

[73] H. Mitlehner, W. Bartsch, M. Bruckmann, K. Dohnke, and U. Weinert, *Proceeding of 9th International Symposium on Power Semiconductor Devices and ICs* (1997) p. 165.

[74] H. Mitlehner, P. Friedrichs, D. Peters, R. Schorner, U. Weinert, B. Weis, and D. Stephani, *Proceedings of 10th International Symposium on Power Semiconductor Devices and ICs, 1998. ISPSD 98* (1998) p. 127.

[75] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, and T. Hayashi, *Proceedings of 13th International Symposium on Power Semiconductor Devices and ICs* (2001) p. 27.

[76] T. Kimoto, O. Takemura, H. Matsunami, T. Nakata, and M. Inoue, *Journal of Electronic Materials* **27**, 358 (1998).

[77] H. Lendenmann, A. Mukhitdinov, F. Dahlquist, H. Bleichner, M. Irwin, and R. Soderholm, *Proceedings of 13th International Symposium on Power Semiconductor Devices and ICs* (2001) p. 31.

[78] J. Zhang, L. Storasta, J. P. Bergman, N. T. Son, and E. Janzén, *Journal of Applied Physics* **93**, 4708 (2003).

[79] T. Tawara, H. Tsuchida, S. Izumi, I. Kamata, and K. Izumi, *Materials Science Forum* **457-460**, 565 (2004).

[80] K. Danno, D. Nakamura, and T. Kimoto, *Applied Physics Letters* **90**, 202109 (2007).

[81] N. T. Son, X. T. Trinh, L. S. Løvlie, B. G. Svensson, K. Kawahara, J. Suda, T. Kimoto, T. Umeda, J. Isoya, T. Makino, T. Ohshima, and E. Janzén, *Physical Review Letters* **109**, 187603 (2012).

[82] K. Kawahara, X. T. Trinh, N. T. Son, E. Janzén, J. Suda, and T. Kimoto, *Journal of Applied Physics* **115**, 143705 (2014).

[83] L. Storasta, H. Tsuchida, T. Miyazawa, and T. Ohshima, *Journal of Applied Physics* **103**, 013705 (2008).

[84] T. Hiyoshi and T. Kimoto, *Applied Physics Express* **2**, 041101 (2009).

[85] T. Hiyoshi and T. Kimoto, *Applied Physics Express* **2**, 091101 (2009).

[86] S. Ichikawa, K. Kawahara, J. Suda, and T. Kimoto, *Applied Physics Express* **5**, 101301 (2012).

[87] K. Nakayama, A. Tanaka, M. Nishimura, K. Asano, T. Miyazawa, M. Ito, and H. Tsuchida, *IEEE Transactions on Electron Devices* **59**, 895 (2012).

[88] L. Cheng, J. W. Palmour, A. K. Agarwal, S. T. Allen, E. Van Brunt, G. Y. Wang, V. Pala, W. Sung, A. Q. Huang, M. J. O'Loughlin, A. A. Burk, D. E. Grider, and C. Scozzie, *Materials Science Forum* **778-780**, 1089 (2014).

[89] K. Nakayama, S. Ogata, T. Hayashi, T. Hemmi, A. Tanaka, T. Izumi, K. Asano, D. Okamoto, Y. Tanaka, T. Mizushima, M. Yoshikawa, H. Fujisawa, K. Takenaka, M. Takei, Y. Yonezawa, K. Fukuda, and H. Okumura, *Materials Science Forum* **778-780**, 841 (2014).

[90] T. Kimoto, K. Danno, and J. Suda, *physica status solidi (b)* **245**, 1327 (2008).

[91] T. Hayashi, K. Asano, J. Suda, and T. Kimoto, *Journal of Applied Physics* **112**, 064503 (2012).

[92] B. Zippelius, J. Suda, and T. Kimoto, *Journal of Applied Physics* **111**, 033515 (2012).

[93] H. Lendenmann, F. Dahlquist, N. Johansson, R. Söderholm, P. A. Nilsson, J. P. Bergman, and P. Skytt, *Materials Science Forum* **353-356**, 727 (2001).

[94] J. P. Bergman, H. Lendenmann, P. A. Nilsson, U. Lindefelt, and P. Skytt, *Materials Science Forum* **353-356**, 299 (2001).

[95] H. Lendenmann, J. P. Bergman, F. Dahlquist, and C. Hallin, *Materials Science Forum* **433-436**, 901 (2003).

[96] H. Tsuchida, T. Miyanagi, I. Kamata, T. Nakamura, K. Izumi, K. Nakayama, R. Ishii, K. Asano, and Y. Sugawara, *Materials Science Forum* **483-485**, 97 (2005).

[97] R. L. Myers-Ward, B. L. VanMil, R. E. Stahlbush, S. Katz, J. McCrate, S. Kitt, C. R. Eddy Jr., and D. K. Gaskill, *Materials Science Forum* **615-617**, 105 (2009).

[98] S. Leone, A. Henry, E. Janzén, and S. Nishizawa, *Journal of Crystal Growth* **362**, 170 (2013).

[99] R. F. Davis, G. Kelner, M. Shur, J. W. Palmour, and J. A. Edmond, *Proceedings of the IEEE* **79**, 677 (1991).

[100] H.-F. Li, S. Dimitrijev, H. B. Harrison, and D. Sweatman, *Applied Physics Letters* **70**, 2028 (1997).

[101] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, *IEEE Electron Device Letters* **22**, 176 (2001).

[102] P. Jamet, S. Dimitrijev, and P. Tanner, *Journal of Applied Physics* **90**, 5058 (2001).

[103] L. A. Lipkin, M. K. Das, and J. W. Palmour, *Materials Science Forum* **389-393**, 985 (2002).

[104] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, *IEEE Electron Device Letters* **31**, 710 (2010).

[105] D. Okamoto, H. Yano, T. Hatayama, and T. Fuyuki, *Applied Physics Letters* **96**, 203508 (2010).

[106] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, K. Asano, and Y. Sugawara, *IEEE Electron Device Letters* **20**, 611 (1999).

[107] S. Nakazawa, T. Okuda, J. Suda, T. Nakamura, and T. Kimoto, *IEEE Transactions on Electron Devices* **62**, 309 (2015).

[108] T. Hirao, H. Yano, T. Kimoto, H. Matsunami, and H. Shiomi, *Materials Science Forum* **389-393**, 1065 (2002).

[109] J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr., *in Silicon Carbide and Related Materials*, 449 (1993).

[110] S. Onda, R. Kumar, and K. Hara, *physica status solidi (a)* **162**, 369 (1997).

[111] J. Tan, J. A. Cooper, Jr., and M. R. Melloch, *IEEE Electron Device Letters* **19**, 487 (1998).

[112] J. N. Shenoy, J. A. Cooper, Jr., and M. R. Melloch, *IEEE Electron Device Letters* **18**, 93 (1997).

[113] M. Matin, A. Saha, and J. A. Cooper, Jr., *IEEE Transactions on Electron Devices* **51**, 1721 (2004).

[114] S. Harada, M. Okamoto, T. Yatsuo, K. Adachi, K. Fukuda, and K. Arai, *IEEE Electron Device Letters* **25**, 292 (2004).

[115] S. Harada, M. Kato, K. Suzuki, M. Okamoto, T. Yatsuo, K. Fukuda, and K. Arai, *Technical Digest on International Electron Devices Meeting* (2006) p. 1.

[116] J. W. Palmour, L. Cheng, V. Pala, E. Van Brunt, D. J. Lichtenwalner, G.-Y. Wang, J. Richmond, M. O'Loughlin, S.-H. Ryu, S. T. Allen, A. A. Burk, and C. Scozzie, *Proceeding of 26th International Symposium on Power Semiconductor Devices and ICs* (2014) p 79.

[117] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, and Y. Yokotsuji, *Technical Digest on International Electron Devices Meeting* (2011) p. 26.

[118] Y. Kagawa, R. Tanaka, N. Fujiwara, K. Sugawara, Y. Fukui, N. Miura, M. Imaizumi, S. Nakata, and S. Yamakawa, *Materials Science Forum* **821-823**, 761 (2015).

[119] S. Harada, M. Kato, M. Shinozaki, Y. Kobayashi, K. Ariyoshi, T. Kojima, M. Sometani, J. Senzaki, Y. Tanaka, and H. Okumura, *Materials Science Forum* **821-823**, 769 (2015).

[120] Y. Mikamura, K. Hiratsuka, T. Tsuno, H. Michikoshi, S. Tanaka, T. Masuda, K. Wada, T. Horii, J. Genba, T. Hiyoshi, and T. Sekiguchi, *IEEE Transactions on Electron Devices* **62**, 382 (2015).

[121] N. Ramungul, T. P. Chow, M. Ghezzo, J. Kretchmer, and W. Hennessy, *Technical Digest of 54th Annual Device Research Conference* (1996) p. 56.

[122] Q. Zhang, C. Jonas, S.-H. Ryu, A. Agarwal, and J. Palmour, *Proceeding of 18th International Symposium on Power Semiconductor Devices and ICs* (2006) p. 1.

[123] Y. Sui, X. Wang, and J. A. Cooper, Jr., *IEEE Electron Device Letters* **28**, 728 (2007).

[124] Q. Zhang, M. Das, J. Sumakeris, R. Callanan, and A. Agarwal, *IEEE Electron Device Letters* **29**, 1027 (2008).

[125] X. Wang and J. A. Cooper, Jr., *IEEE Transactions on Electron Devices* **57**, 511 (2010).

[126] S.-H. Ryu, L. Cheng, S. Dhar, C. Capell, C. Jonas, J. Clayton, M. Donofrio, M. J. O'Loughlin, A. A. Burk, A. K. Agarwal, and J. W. Palmour, *Materials Science Forum* **717-720**, 1135 (2012).

[127] K. Fukuda, D. Okamoto, M. Okamoto, T. Deguchi, T. Mizushima, K. Takenaka, H. Fujisawa, S. Harada, Y. Tanaka, Y. Yonezawa, T. Kato, S. Katakami, M. Arai, M. Takei, S. Matsunaga, K. Takao, T. Shinohe, T. Izumi, T. Hayashi, S. Ogata, K. Asano, H. Okumura, and T. Kimoto, *IEEE Transactions on Electron Devices* **62**, 396 (2015).

[128] A. Agarwal, S. Seshadri, and L. B. Rowland, *IEEE Electron Device Letters* **18**, 592 (1997).

[129] J. Senzaki, K. Kojima, and K. Fukuda, *Applied Physics Letters* **85**, 6182 (2004).

[130] A. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, *IEEE Electron Device Letters* **28**, 587 (2007).

[131] J. H. Zhao, P. Alexandrov, J. Zhang, and X. Li, *IEEE Electron Device Letters* **25**, 474 (2004).

[132] V. Veliadis, *physica status solidi (a)* **206**, 2346 (2009).

[133] Y. Tanaka, A. Takatsuka, T. Yatsuo, K. Arai, and K. Yano, *Proceeding of 22nd International Symposium on Power Semiconductor Devices and ICs* (2010) p. 357.

[134] S. Krishnaswami, A. Agarwal, S.-H. Ryu, C. Capell, J. Richmond, J. Palmour, S. Balachandran, T. P. Chow, S. Bayne, B. Geil, K. Jones, and C. Scozzie, *IEEE Electron Device Letters* **26**, 175 (2005).

[135] K. Nonaka, A. Horiuchi, Y. Negoro, K. Iwanaga, S. Yokoyama, H. Hashimoto, M. Sato, Y. Maeyama, M. Shimizu, and H. Iwakuro, *physica status solidi (a)* **206**, 2457 (2009).

[136] H. Miyake, T. Kimoto, and J. Suda, *IEEE Electron Device Letters* **32**, 841 (2011).

[137] H. Miyake, T. Okuda, H. Niwa, T. Kimoto, and J. Suda, *IEEE Electron Device Letters* **33**, 1598 (2012).

[138] K. G. McKay and K. B. McAfee, *Physical Review* **91**, 1079 (1953).

[139] C. A. Lee, R. A. Logan, R. L. Batdorf, J. J. Kleimack, and W. Wiegmann, *Physical Review* **134**, A761 (1964).

[140] R. Van Overstraeten and H. De Man, *Solid-State Electronics* **13**, 583 (1970).

[141] T. P. Pearsall, F. Capasso, R. E. Nahory, M. A. Pollack, and J. R. Chelikowsky, *Solid-State Electronics* **21**, 297 (1978).

[142] G. E. Bulman, L. W. Cook, and G. E. Stillman, *Solid-State Electronics* **25**, 1189 (1982).

[143] P. A. Wolff, *Physical Review* **95**, 1415 (1954).

[144] Y. Okuto and C. R. Crowell, *Physical Review B* **6**, 3076 (1972).

[145] G. H. Glover, *Journal of Applied Physics* **46**, 4842 (1975).

[146] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, *Applied Physics Letters* **71**, 90 (1997).

[147] R. Raghunathan and B. J. Baliga, *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's* (1997) p. 173.

[148] T. Hatakeyama, T. Watanabe, T. Shinohe, K. Kojima, K. Arai, and N. Sano, *Applied Physics Letters* **85**, 1380 (2004).

[149] W. S. Loh, B. K. Ng, J. S. Ng, S. I. Soloviev, H.-Y. Cha, P. M. Sandvik, C. M. Johnson, and J. P. R. David, *IEEE Transactions on Electron Devices* **55**, 1984 (2008).

[150] J. E. Green, W. S. Loh, A. R. J. Marshall, B. K. Ng, R. C. Tozer, J. P. R. David, S. I. Soloviev, and P. M. Sandvik, *IEEE Transactions on Electron Devices* **59**, 1030 (2012).

[151] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer, 2008.

[152] A. S. Grove, O. Leistiko, Jr., and W. W. Hooper, *IEEE Transactions on Electron Devices* **14**, 157 (1967).

[153] Y. C. Kao and E. D. Wolley, *Proceedings of the IEEE* **55**, 1409 (1967).

[154] M. S. Adler, V. A. K. Temple, A. P. Ferro, and R. C. Rustay, *IEEE Transactions on Electron Devices* **ED-24**, 107 (1977).

[155] V. A. K. Temple and W. Tantraporn, *IEEE Transactions on Electron Devices* **33**, 1601 (1986).

[156] D. C. Sheridan, G. Niu, and J. D. Cressler, *Solid-State Electronics* **45**, 1659 (2001).

[157] J. N. Merrett, T. Isaacs-Smith, D. C. Sheridan, and J. R. Williams, *Journal of Electronic Materials* **31**, 635 (2002).

[158] P. A. Losee, S. K. Balachandran, L. Zhu, C. Li, J. Seiler, T. P. Chow, I. B. Bhat, and R. J. Gutmann, *Proceeding of 16th International Symposium on Power Semiconductor Devices and ICs* (2004) p. 301.

[159] R. Pérez, D. Tournier, A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán, *IEEE Transactions on Electron Devices* **52**, 2309 (2005).

[160] R. Ghandi, B. Buono, M. Domeij, G. Malm, C.-M. Zetterling, and M. Östling, *IEEE Electron Device Letters* **30**, 1170 (2009).

[161] F. Udrea, G. Amaratunga, and N. Udugampola, *Proceedings of 2004 International Semiconductor Conference (CAS2004)* **1** (2004) p. 17.

[162] M. Westmoreland, P. J. Ward, and P. A. Mawby, *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE 2011)* (2011) p. 1.

[163] B. T. Donnellan, P. A. Mawby, M. Rahimo, and L. Storasta, *27th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)* (2012) p. 152.

Chapter 2

Impact Ionization Coefficients in SiC toward Ultrahigh-Voltage Power Devices

2.1 Introduction

Impact ionization coefficients, defined as electron-hole pairs generated by a carrier per unit distance, is one of the most important physical properties in a semiconductor material. Because impact ionization coefficients determine the breakdown voltage and safe-operating area of power devices, its value needs to be determined toward the accurate designing and characterization of a power device.

In SiC, there have been several experimental studies to determine them [1–8]. The first reliable work was reported by Konstantinov *et al.* [1, 2], where photomultiplication characteristics were measured by using a He-Cd laser ($\lambda = 325$ nm) on p^+n diodes. At the same time, Raghunathan and Baliga [3] have also reported the impact ionization coefficient of holes (β) in 4H-SiC by Electron Beam Induced Current (EBIC) measurement on a Schottky barrier diode. In the work by Hatakeyama *et al.* [5, 6], photomultiplication characteristics were measured by using an Ar^+-laser ($\lambda = 350$ nm) on p^+n diodes on the Si-face and A-face of 4H-SiC, and showed the anisotropy of avalanche breakdown voltage and impact ionization coefficients. For these studies, however, Loh *et al.* [7] have pointed out a problem in the measurement procedures: the penetration depth of the illumination light (or electron beam) was too long and caused considerable carrier generation inside the depletion layer and in the substrate. This will cause an increase in mixed carrier injection and results in an error for the measured multiplication factors. Furthermore, Green *et al.* [8] has presented ionization coefficients derived from the photomultiplication and excess noise measurement using a frequency doubled Ar^+ laser ($\lambda = 244$ nm), and showed that electron ionization coefficient (α) exhibits strong electric field dependence at low electric field.

Although studies on impact ionization coefficients in SiC are both experimentally and

theoretically [9–11] in progress, accurate values of ionization coefficients which can be used for designing of power device have not been reported. For example, very few studies focusing on designing of UHV devices have been reported. Due to its low doping concentration and thick voltage-blocking layer used in UHV devices, breakdown occurs at lower maximum electric field than the conventional 1 kV-class devices, making ionization coefficients at low electric field (∼1 MV/cm) of much interest. Since most of the ionization coefficients reported to date relies on accurate measurement results only to ∼1.5 MV/cm, experimental studies are needed at lower electric field to accurately simulate UHV devices. Furthermore, since one of the main benefits of SiC devices is the capability of high-temperature operation, ionization coefficients at elevated temperatures will be especially important. However, reports on high-temperature measurement of ionization coefficients are also very limited in 4H-SiC [6, 12, 13].

In this chapter, impact ionization coefficients along nearly ⟨0001⟩ of 4H-SiC were determined in a wide range of electric field using various photodiodes (PDs) having different multiplication-layer structures up to 150°C. The obtained ionization coefficients were verified by comparing the calculated multiplication factors and ideal breakdown voltages with the measurement result. Furthermore, the doping concentration and temperature dependences of critical electric field strength and ideal breakdown voltage were calculated toward convenient estimation of breakdown voltage of SiC power devices.

2.2 Extraction of Impact Ionization Coefficients

Because direct measurement of impact ionization coefficients cannot be done, a photomultiplication measurement is commonly used to indirectly extract the ionization coefficients [14]. This measurement is a standard technique to extract impact ionization coefficients in many semiconductor materials including Si [15, 16], GaAs [17, 18], and SiC. In this measurement, a photodiode is used and its photocurrent is measured while applying a reverse bias. When the reverse bias voltage is high enough, the generated carriers by the illumination will initiate avalanche multiplication causing an increase of photocurrent. Then by calculating the ratio of the multiplied and unmultiplied photocurrent, we obtain a multiplication factor M, and using the obtained multiplication factor, ionization coefficients can be algebraically calculated.

In this section, photomultiplication measurement will be explained in details. Toward the high accuracy in the final ionization coefficients, important aspects that need to be solved during the measurement will be pointed out. While concerning these aspects, measurement setup used in this study will be explained.

2.2.1 Photomultiplication Measurement

The schematic illustration of generated photocurrent during the photomultiplication measurement is shown in Fig. 2.1. Here, a p^+-i-n^+ structure is assumed. When the photodiode

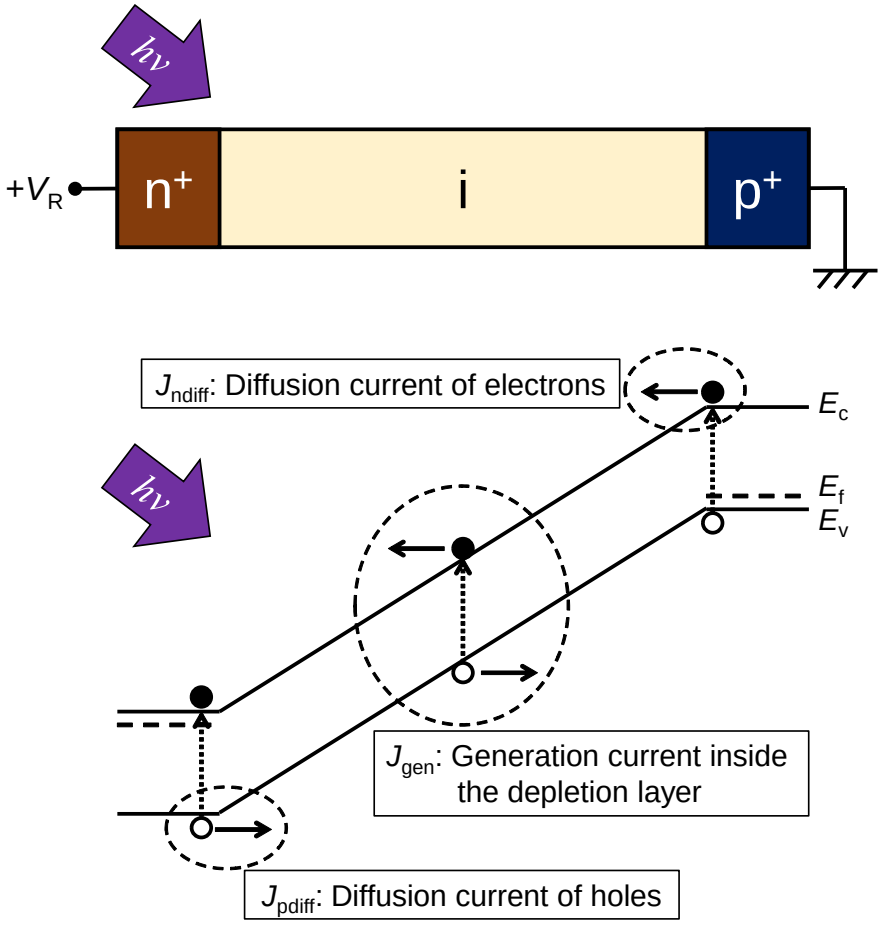


Figure 2.1: Schematic illustration of different current components of the measured photocurrent in a reverse biased photodiode.

is illuminated, the measured photocurrent will contain various current components. These are the drift current generated within the depletion region (J_{gen}), hole diffusion current from the undepleted n-region (J_{pdiff}), and the electron current from the p^+-region (J_{ndiff}). When the electric field inside the depletion layer is high enough, generated carriers will induce avalanche multiplication and result in an increase of photocurrent. Assuming J_{p} and J_{n} to be hole and electron currents inside the depletion layer, the schematic figure of current components inside the depletion layer can be shown as Fig. 2.2. In this case, the increment of hole current in the distance dx can be expressed in the following equation.

$$dJ_{\mathrm{p}} = J_{\mathrm{p}}\beta dx + J_{\mathrm{n}}\alpha dx + qu(x)dx. \tag{2.1}$$

Here, α and β are the impact ionization coefficients of electrons and holes, respectively, and $u(x)$ is the generation rate by the illumination inside the depletion layer. Because total current $J = J_{\mathrm{n}} + J_{\mathrm{p}}$ is constant inside the depletion layer, above equation can be rewritten as

$$\frac{dJ_{\mathrm{p}}}{dx} - (\beta - \alpha)J_{\mathrm{p}} = \alpha J + qu(x). \tag{2.2}$$

The solution to this equation will give the equation for the total current J as

$$J = \frac{J_{\mathrm{p}}(0) + J_{\mathrm{n}}(W)\cdot\exp\left[-\int_0^W(\beta-\alpha)dx\right] + q\int_0^W u(x)\cdot\exp\left[-\int_0^x(\beta-\alpha)dx'\right]dx}{1-\int_0^W \beta\cdot\exp\left[-\int_0^x(\beta-\alpha)dx'\right]dx} \tag{2.3}$$

$$\equiv M_{\mathrm{p}}J_{\mathrm{p}}(0) + M_{\mathrm{n}}J_{\mathrm{n}}(W) + M_{\mathrm{dep}}J_{\mathrm{dep}}. \tag{2.4}$$

Here M_{p}, M_{n}, and M_{dep} are the multiplication factors initiated by holes, electrons, and generated carriers inside the depletion layer, respectively, which can be expressed as follows:

$$M_{\mathrm{p}} = \frac{1}{1-\int_0^W \beta\cdot\exp\left[-\int_0^x(\beta-\alpha)dx'\right]dx} \tag{2.5}$$

$$M_{\mathrm{n}} = \frac{1}{1-\int_0^W \alpha\cdot\exp\left[-\int_x^W(\alpha-\beta)dx'\right]dx} \tag{2.6}$$

$$M_{\mathrm{dep}} = M_{\mathrm{p}}\cdot\frac{\int_0^W qu(x)\cdot\exp\left[-\int_0^x(\beta-\alpha)dx'\right]dx}{\int_0^W qu(x)dx}. \tag{2.7}$$

In particular, equations (2.5) and (2.6) will give the ionization integral explained in Chapter 1, which defines the breakdown voltage of a power device.

In photomultiplication measurement, the goal is to measure the reverse bias characteristics of M_{p} and M_{n} separately. By using the obtained M_{p} and M_{n}, ionization coefficients can be algebraically calculated, which will be explained in Section 2.4.

2.2.2 Toward the Accurate Measurement

In this section, details of the measurement condition of photomultiplication measurement will be discussed toward the accurate measurement of the pure multiplication factor M_{p}

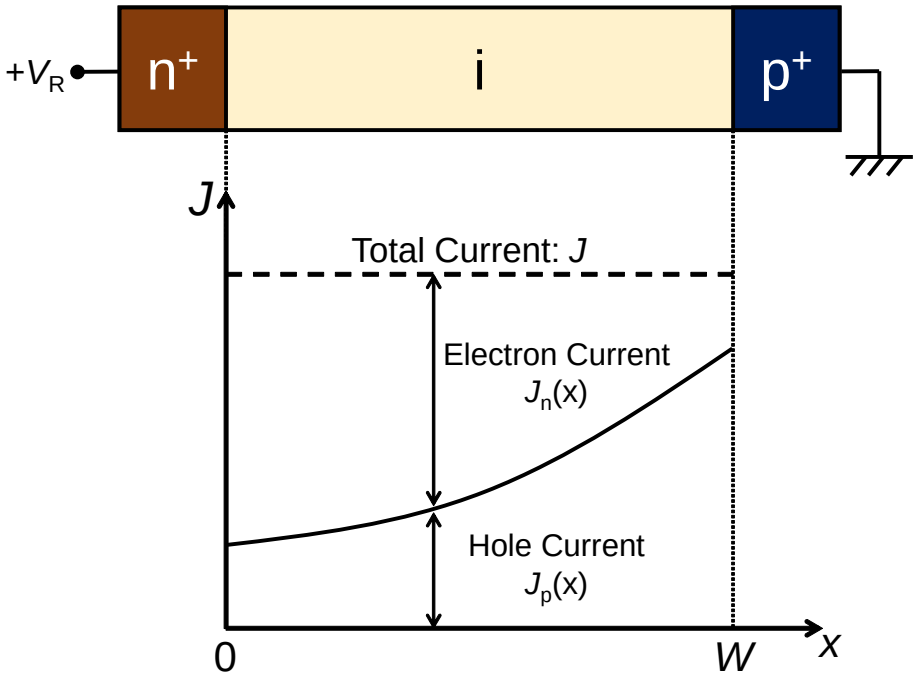


Figure 2.2: Schematic illustration of the quantities of hole and electron currents inside the depletion layer.

and M_{n}. Here, measurement of pure M_{p} using p^+-n-n^+ diode will be focused since the same discussion can be used for the measurement of pure M_{n} in other diode structure.

In equation (2.4), the current that will be measured is the total current J, which can be expressed as,

$$J = MJ_0 \tag{2.8}$$

where M is the measured multiplication factor and J_0 is the photocurrent without avalanche multiplication, which can be extracted from the measurement. Using equation (2.4), the measured multiplication factor can expressed by the following equation:

$$M = M_{\mathrm{p}} \cdot \frac{J_{\mathrm{p}}(0)}{J_0} + M_{\mathrm{n}} \cdot \frac{J_{\mathrm{n}}(W)}{J_0} + M_{\mathrm{dep}} \cdot \frac{J_{\mathrm{dep}}}{J_0}. \tag{2.9}$$

Because the multiplication factor that can be experimentally obtained is M, to measure M_{p} accurately, electron diffusion current $J_{\mathrm{n}}(0)$ and generation current J_{dep} must be reduced inside the photocurrent. In the case of $J_{\mathrm{p}}(0) \gg J_{\mathrm{n}}(W), J_{\mathrm{dep}}$, equation (2.4) reduces to $J = M_{\mathrm{p}} \cdot J_{\mathrm{p}}(0)$ and M_{p} can be accurately obtained from the measurement. During the measurement, the variable parameters will be the wavelength of the illumination light and the direction of the light illumination. To realize the condition $J_{\mathrm{p}}(0) \gg J_{\mathrm{n}}(W), J_{\mathrm{dep}}$, measurement procedure that needs to be done is to illuminate the n^+-side of the device with a short-wavelength light source. If the illumination wavelength is short enough, absorption occurs only near the surface of the diode: This will prevent the absorption in the depletion layer and in p^+-layer. Therefore, the one important parameter in the measurement that needs to be optimized is the illumination wavelength

To optimize the illumination wavelength during the photomultiplication measurement, one-dimensional simulation of photocurrent component was performed using an epilayer structure that will be used in this study. Figure 2.3 shows the schematic structure of the one-dimensional model used in this simulation. Here, n^+-type contact layer ($N_{\mathrm{d}} = 1 \times 10^{19}$ cm^{-3}, 1 μm) and n-type multiplication layer ($N_{\mathrm{d}} = 4 \times 10^{16}$ cm^{-3}, 13 μm) is grown on a p^+-type substrate, and illumination is assumed to be done from the top n^+-layer. The photocurrent components concerned are J_{pdiff}, J_{ndiff}, and J_{gen}, which are defined in Fig. 2.1. Using equations shown by Raynaud *et al.* [14], the percentage of the photocurrent component was calculated by the mean of illumination wavelength, which is shown in Fig. 2.4. Here, reverse bias voltage of 600 V was assumed and the wavelength dependence of absorption coefficient reported by Cha *et al.* [19] was used. From Fig. 2.4, hole diffusion current becomes nearly 100% of the photocurrent when illumination is done at a wavelength shorter than 280 nm. If the measurement was performed at a longer wavelength, other photocurrent component such as generation current will be included in the measured photocurrent, causing inaccuracy in measured multiplication factor, i.e., ionization coefficients.

Discussion described in this section can be applied to the measurement of M_{n}. For the measurement of M_{n}, measuring while illuminating from the p^+-side in Fig. 2.2 using a short-wavelength excitation source will realize the accurate value of M_{n}.

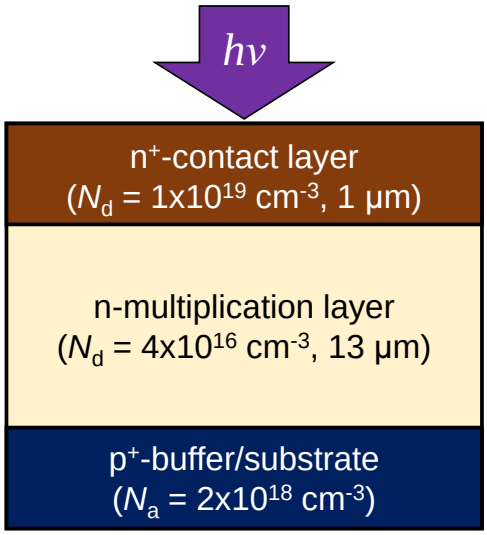


Figure 2.3: Schematic structure of the one-dimensional model assumed here for the simulation of photocurrent component by the change of illumination wavelength.

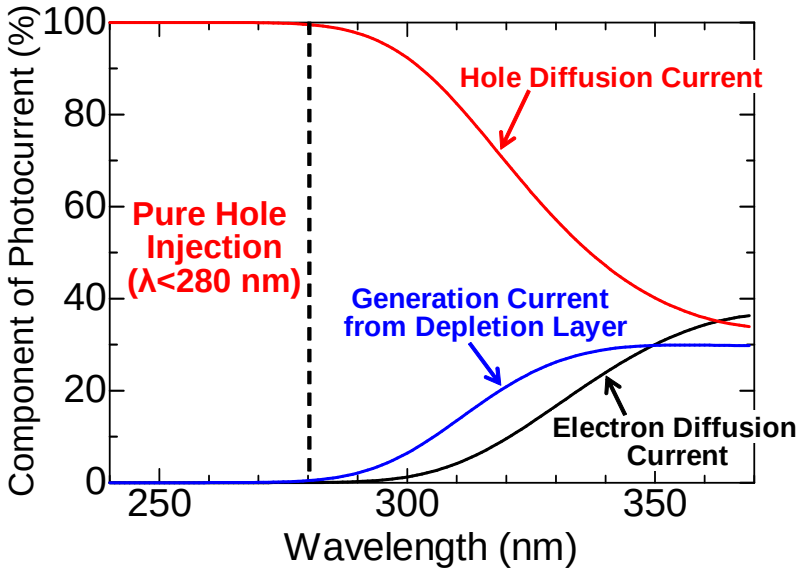


Figure 2.4: Simulated percentages of photocurrent components at different illumination wavelength.

2.2.3 Measurement Setup

According to the discussion described in the previous section, a schematic figure of the measurement setup used in this study is shown in Fig. 2.5. In this measurement, a Xe lamp combined with a band pass filter (BPF) of 254, 260, and 270 nm was employed as a nearly-monochromatic illumination source. The penetration depth in 4H-SiC at these wavelengths is small enough (<0.5 μm) to obtain pure carrier injection in all of the diode structures used in this study since absorption in the depletion layer is negligibly small [19]. While illuminating the devices from the top, reverse current-voltage (I–V) characteristics were measured. Here, devices were immersed in a silicone oil to avoid air sparking. In this study, high-temperature measurement was done by heating the stage up to 150°C, where the temperature limit was determined by the silicone oil used.

2.3 Device Fabrication

In this section, structure and fabrication process of PDs used in this study will be explained. The schematic structures of fabricated 4H-SiC PDs are shown in Fig. 2.6, and their detailed structures are summarized in Table 2.1. These doping densities and thicknesses were obtained by using capacitance-voltage (C–V) measurement, and also secondary ion mass spectrometry (SIMS) was performed to verify the depth profiles. During the C–V measurement, a dielectric constant of 10.2 was used because the diodes were fabricated on nearly (0001). In this study, PDs with various multiplication layer structures were used. The calculated electric field distributions inside the depletion region at breakdown for some of the diodes are shown in Fig. 2.7. Maximum electric field at breakdown will vary by the multiplication layer structures, meaning that the maximum electric field which the ionization coefficients can be extracted will differ in each device. Therefore, by using various multiplication layers, ionization coefficients can be extracted in a wide range of electric field. The details will be explained in Section 2.5. In these PDs, epilayers were grown by using chemical vapor deposition (CVD), where 4H-SiC (0001) substrates with an off-angle of 4° (n-type substrate) and 8° (p-type substrate) were used. Although these substrates have slightly different off-cut angles, the impacts on the ionization coefficient extraction is small based on results of diode fabrication on substrates with different off-cut angles, which were previously investigated in the author's group. In this study three devices for each type of PDs were measured to confirm the reproducibility. All the measured PDs had a diameter of 200 μm for NPT1–3, 250 μm for NPT4, and 450 μm for PT1–2. These diodes are free of macroscopic defects and threading screw dislocations.

Toward the accurate measurement of ionization coefficients, measured PDs needs to be optimized. The most important factor for the measured PDs are the alleviation of electric field crowding. When electric field crowding occurs in a device, unwanted avalanche multiplication in a local region will occur, which results in an inaccurate measurement.

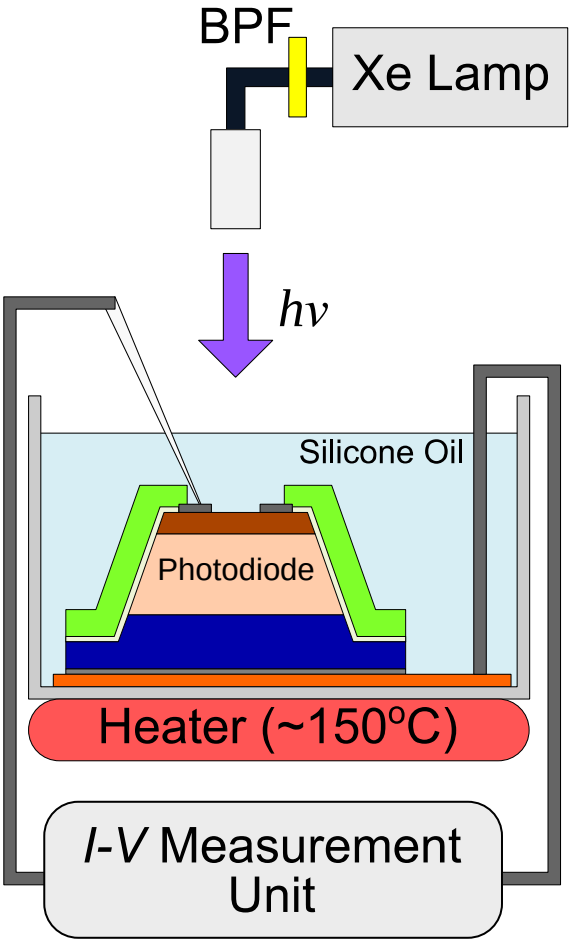


Figure 2.5: Schematic illustration of the measurement setup used for the photomultiplication measurement in this study.

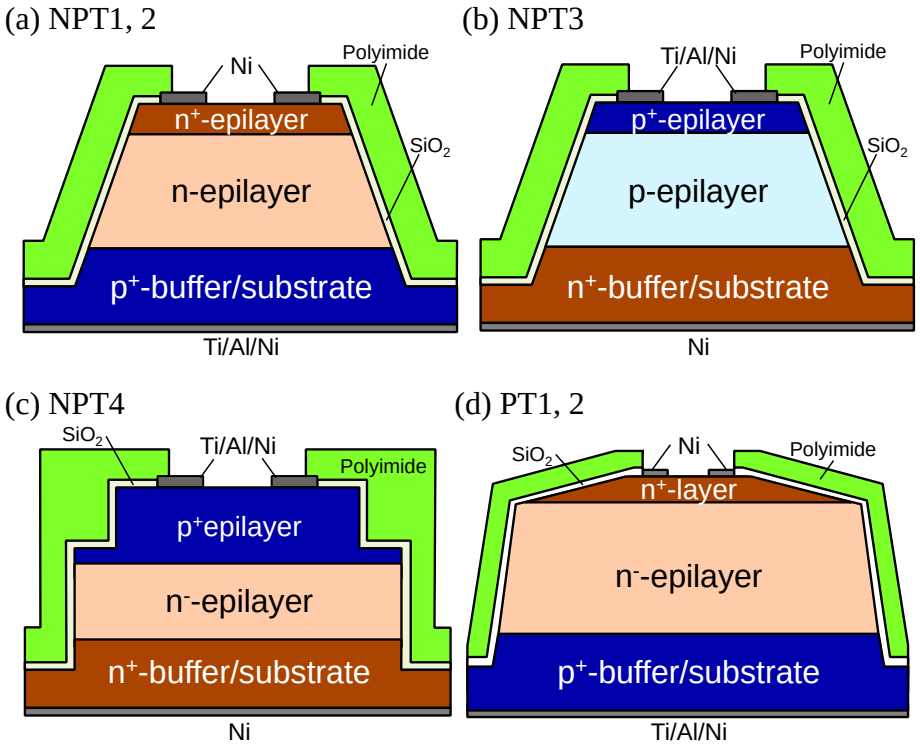


Figure 2.6: Schematic cross section of the fabricated PDs. Structures of the individual layers are summarized in Table 2.1.

Table 2.1: Doping concentration and thickness of the layers in photodiodes shown in Fig. 2.6.

Device Name	Top Contact Layer	Multiplication Layer	Buffer/Substrate
NPT1	1×10^{19} cm^{-3} 1 μm	4.0×10^{16} cm^{-3} 13 μm	2×10^{18} cm^{-3}
NPT2	1×10^{19} cm^{-3} 1 μm	2.0×10^{16} cm^{-3} 13 μm	2×10^{18} cm^{-3}
NPT3	1×10^{19} cm^{-3} 1 μm	3.7×10^{16} cm^{-3} 12 μm	2×10^{18} cm^{-3}
NPT4	7.5×10^{18} cm^{-3} 3 μm	1.3×10^{17} cm^{-3} 3 μm	2×10^{18} cm^{-3}
PT1	1×10^{18} cm^{-3} 0.8 μm	5×10^{14} cm^{-3} 4.75 μm	2×10^{18} cm^{-3}
PT2	1×10^{18} cm^{-3} 0.8 μm	5×10^{14} cm^{-3} 2.13 μm	2×10^{18} cm^{-3}

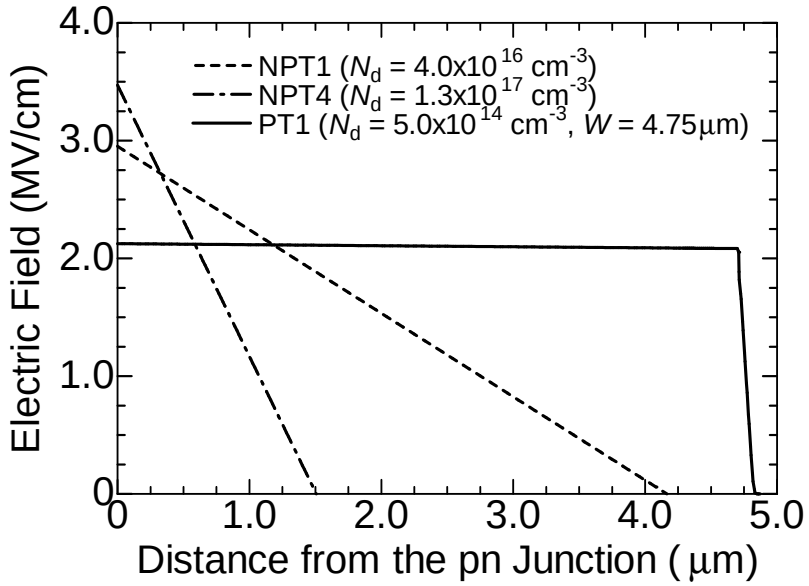


Figure 2.7: Electric field distribution inside the depletion layer of NPT1, NPT4, and PT1 at breakdown voltage.

Here, each device structure has different edge termination to alleviate unwanted electric field crowding, where the details will be explained in the next section. Another aspect that needs to be solved is the exclusion of unwanted illumination to the mesa sidewalls or edges. If a light absorption occurs at the mesa sidewalls, this can result in an increase of generation current inside the depletion layer, i.e., inaccuracy in measured multiplication factors. In this study, a polyimide (TORAY: PW-1500) was coated on the surface of PDs. Figure 2.8 shows the optical transmission spectrum of the polyimide film, where the film cuts off UV-light below 350 nm. Because the illumination wavelength used in this study is 254–270 nm, this polyimide will prevent the unwanted illumination to the mesa sidewalls or edges.

2.3.1 Non-Punchthrough Diodes for the Measurement in Medium Electric Field Range

Figures 2.6(a) and (b) show the schematic structures of two complementary non-punchthrough (NPT) diodes. These diodes were used to obtain ionization coefficients in the electric field range of 1.5–2.5 MV/cm. The junction of NPT1–2 [Fig. 2.6(a)] consists of n-type multiplication layer grown on a p^+-type buffer layer and substrate, and the junction of NPT3 [Fig. 2.6(b)] consists of a p-type multiplication layer grown on an n^+-type buffer layer and substrate. Here, punchthrough does not occur up to the breakdown voltage in these diodes. In these PDs, positive-bevel edge termination [20] with a bevel angle of 80° was employed by fully etching into the substrate to avoid the electric field crowding.

By using NPT1–2, M_p can be measured by illuminating from the top of the diode, as explained in the previous section. However, measurement of M_n using NPT1–2 will have severe difficulty; The thick p^+-substrate will prevent the generation of enough photocurrent for the M_n measurement in the case of back illumination. Therefore in this study, NPT3 was used for the measurement of M_n, where M_n can be obtained by illumination from the top.

Figure 2.9 shows the fabrication process of NPT1–3. First, SiO_2 was deposited using plasma-enhanced chemical vapor deposition (PECVD), then patterned using photolithography and capacitively-coupled-plasma reactive ion etching (CCP-RIE) to fabricate the etching mask. Using the SiO_2 mask, inductively-coupled-plasma reactive ion etching (ICP-RIE) with Cl_2-O_2 chemistry was performed and deep mesa to the substrate (Fig. 2.10: 15-μm-depth) was fabricated. Because Cl_2-based RIE have a lower etching rate of SiO_2 compared with a conventional CF_4-based chemistry [21, 22], high etching selectivity of SiC over SiO_2 can be obtained, which realized the deep mesa of 15-μm-depth. After the deep mesa etching, a 40-nm-thick oxide was formed for passivation by dry oxidation at 1300°C for 40 min, followed by nitridation in NO (10% diluted in N_2) at 1250°C for 70 min. Ti/Al (50/200 nm) and Ni (200 nm) annealed at 1000°C for 2 min were employed as ohmic contacts for the p^+-type and n^+-type, respectively. After the metallization, a 6-μm-thick polyimide was coated as a top-surface passivation layer and to block the illuminated UV light.

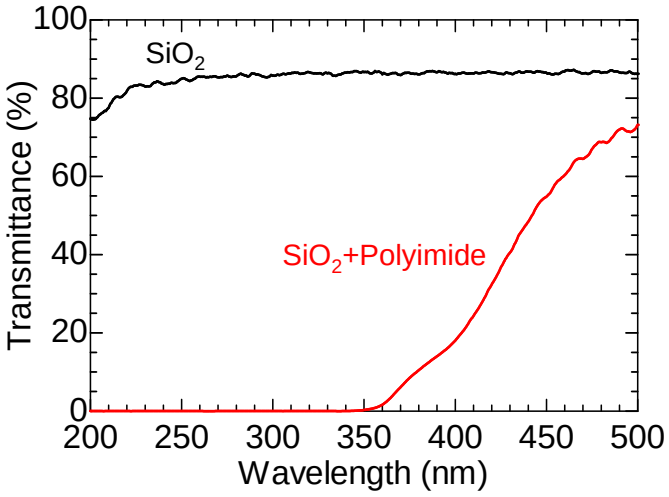


Figure 2.8: Transmittance characteristics of a polyimide used in this study.

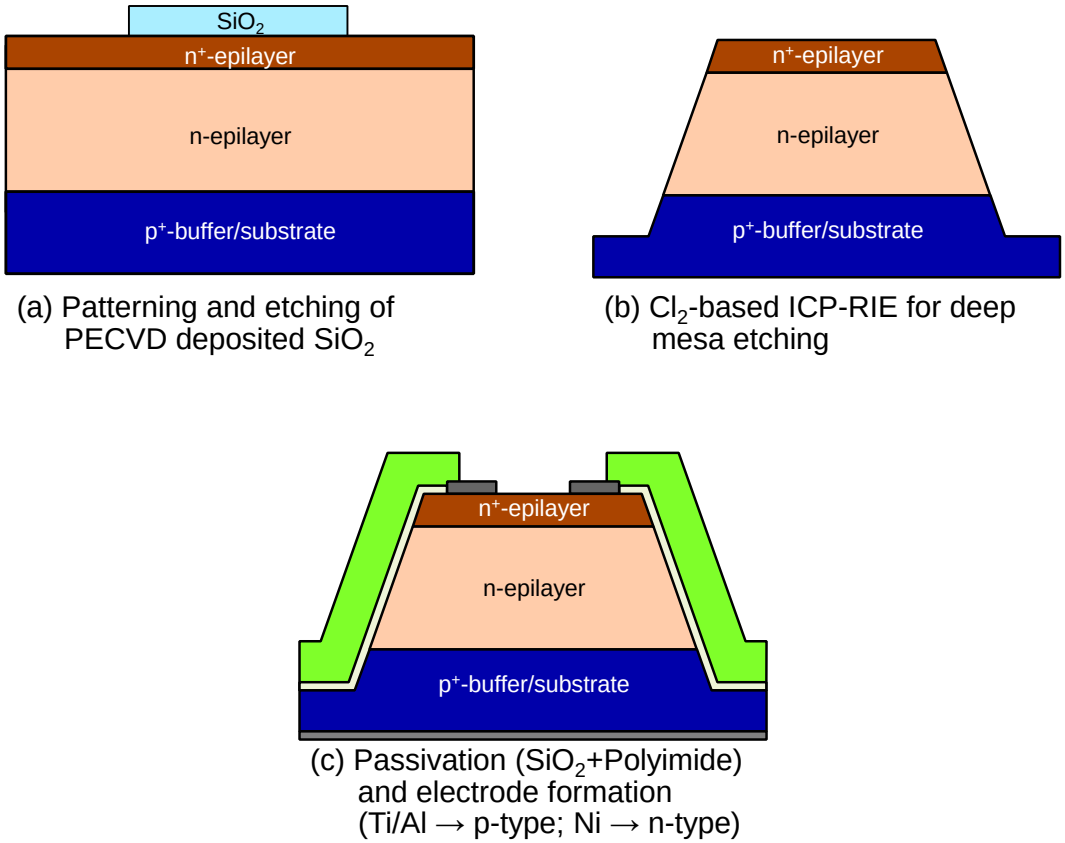


Figure 2.9: Schematic figure of the fabrication process of NPT1, NPT2, and NPT3.

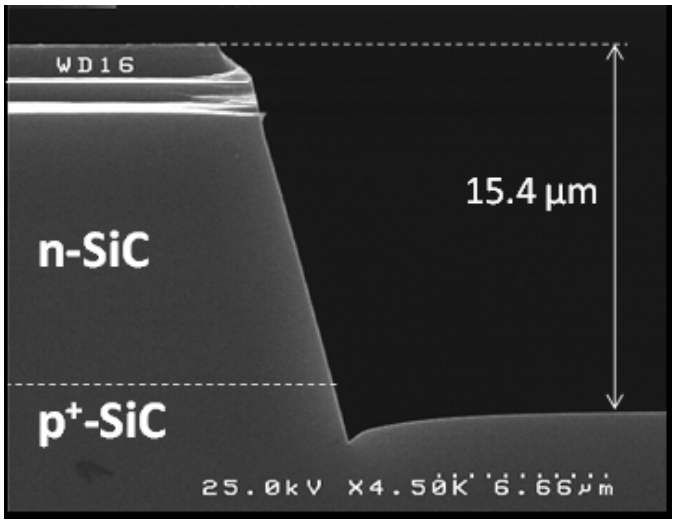


Figure 2.10: SEM image of a fabricated deep mesa by Cl_2-based ICP-RIE.

2.3.2 Non-Punchthrough Diode for the Measurement in High Electric Field Range

Figure 2.6(c) shows the schematic structure of an NPT diode with a highly-doped multiplication layer. Using this highly-doped multiplication layer, ionization coefficients at higher electric field (>2.5 MV/cm) can be obtained. NPT4 consists of p^+-type contact layer and n-type multiplication layer grown on an n^+-type buffer layer and substrate. When this PD is illuminated from the top, M_n can be measured. To avoid the electric field crowding occurring near the p^+/n interface, epilayers were etched down to the substrate with an angle of ∼90° to realize one-dimensional electric field distribution.

The fabrication process of NPT4 is shown in Fig. 2.11. First, a SiO_2 mask was formed as shown in NPT1–3, and using CF_4-based CCP-RIE, the top p^+-contact layer was etched down to just above the pn-junction. Then again, a SiO_2 mask was formed and CF_4-based CCP-RIE was used to etch down to the substrate. Here, two-step etching was done because etching all the way into the substrate by a single-step etching was difficult under this RIE condition. In this PD, Cl_2-based ICP-RIE used in NPT1–3 was not employed because the ICP-RIE process causes a bevel angle of 80° but not 90°. In the case of device structure used here, non-perpendicular mesa results in a negative bevel structure which enhances the electric field crowding [20]. Although CF_4-based CCP-RIE cannot realize single-etching into the substrate, it can etch the SiC while maintaining the perpendicular shape of SiO_2 mask which realizes the one-dimensional electric field distribution. The remaining of the device fabrication process including passivation and electrodes is the same as that of NPT1–3.

2.3.3 Punchthrough Diodes for the Measurement in Low Electric Field Range

Figure 2.6(d) shows the schematic structure of a punchthrough (PT) diode with a low-doping concentration multiplication layer. By using this diode, the ionization coefficients at low electric field (<1.5 MV/cm) can be obtained. PT1 and PT2 consist of implanted n^+-type contact layer and n^--type multiplication layer grown on a p^+-type buffer layer and substrate.

When a PT diode is fabricated using the diode structure shown in NPT1–3, electric field crowding occurs near the n^+/n^- interface. Figure 2.12 shows the electric field distribution at breakdown which was simulated using a commercial device simulator (Sentaurus TCAD). For a conventional structure, electric field crowding is occurring at the edge of n^+/n^- interface as shown in Fig. 2.12(a). To avoid the electric field crowding, a small-beveled mesa structure with a bevel angle of 2° was adopted on the top n^+-layer in this study. This small-beveled mesa structure will enhance the depletion of top n^+ layer at the edge of the device, which will alleviate the electric field crowding. The electric field distribution for PD with small-beveled mesa structure is shown in Fig. 2.12(b), and the simulation result of

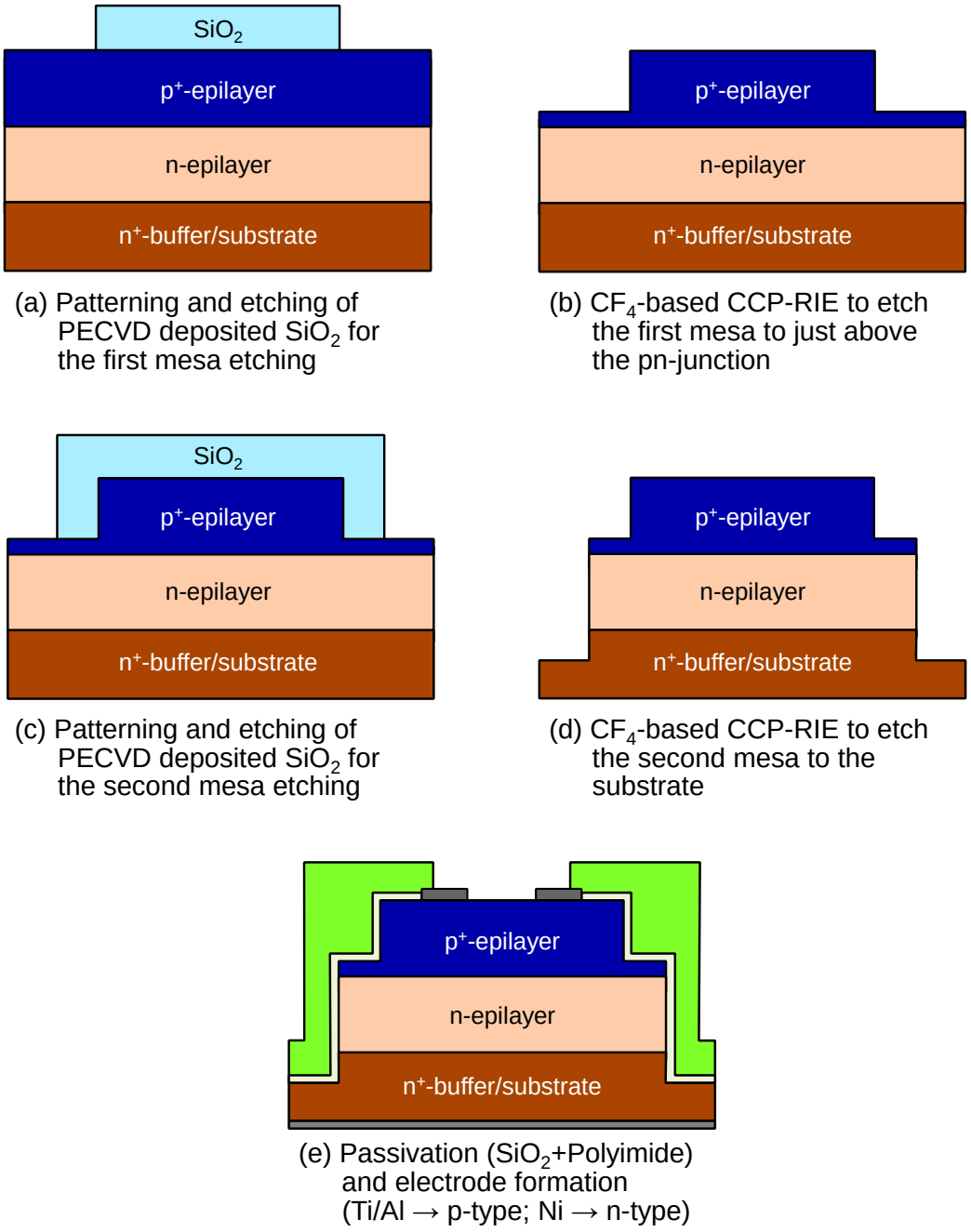


Figure 2.11: Schematic figure of the fabrication process of NPT4.

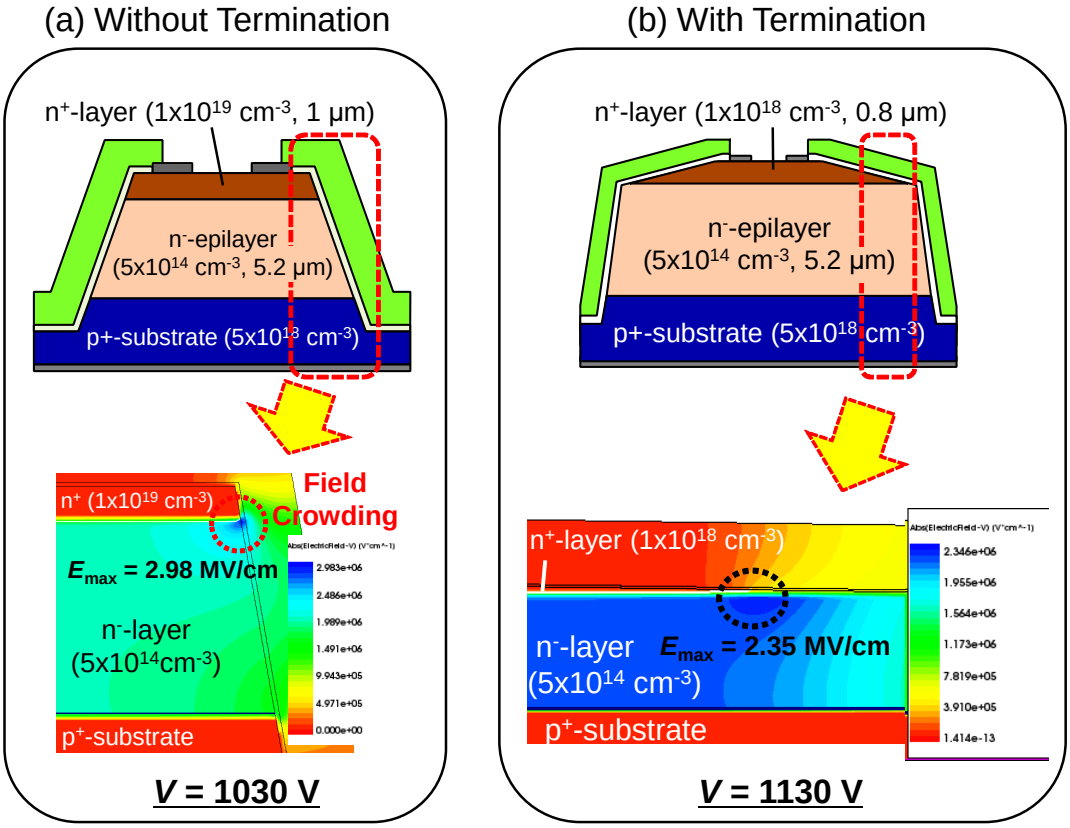


Figure 2.12: Simulated electric field distribution at breakdown voltage for a PT diode (a) without termination and (b) with termination.

reverse I–V characteristics are shown in Fig. 2.13. From Fig. 2.12, electric field crowding has been alleviated compared with the conventional structure. Therefore, from Fig. 2.13, breakdown voltage of this device is very close to the ideal breakdown voltage calculated for a one-dimensional structure.

The fabrication process of PT1–2 are shown in Fig. 2.14. First, a photolithography of thick photoresist ($\sim$27 μm) was done followed by a high-temperature post bake. This high-temperature post bake will cause reflow of patterned photoresist, making a lens-like photoresist structure. Then using the lens-like photoresist mask, CF_4-based CCP-RIE was performed to translate the lens-like structure to SiC. Here, an etching recipe with low selectivity of photoresist over SiC was used to fabricate the very small bevel angle [23]. The results of surface profile measurement of lens-like photoresist, and SiC after RIE are shown in Fig. 2.15. The edge part of lens-like structure has been successfully translated to SiC. After the formation of small-beveled mesa, the remaining of the device fabrication process including deep mesa etching, passivation, and electrodes is the same as that of NPT1–3.

2.4 Extraction Procedures of Impact Ionization Coefficients

When extracting impact ionization coefficients from the multiplication factors, several methods have been proposed in various materials [24–28]. However, these methods use M_p and M_n obtained from measurement of a single device, which is not the case in this study since M_p and M_n were obtained from different devices with different multiplication-layer structures. In this section, extraction procedures of impact ionization coefficients from the measured multiplication factors from different devices are explained. The derivation of the equations shown here will be explained in Appendix A.

2.4.1 Extraction of Hole Impact Ionization Coefficient β

The hole ionization coefficient β at relatively low electric field were extracted using M_p obtained from NPT1–2 and PT1–2. In both cases, $\alpha \to 0$ or $M_\mathrm{n} \to 1$ can be assumed since at sufficiently low electric field, it is known that β is much higher than α in magnitude. Under this assumption, β can be expressed by the following equation using M_p obtained from NPT1 and NPT2.

$$\beta(E_\mathrm{m}) = \frac{qN_\mathrm{d}}{\varepsilon_0\varepsilon_\mathrm{s}} \cdot \frac{1}{M_\mathrm{p}} \cdot \frac{dM_\mathrm{p}}{dE_\mathrm{m}}. \tag{2.10}$$

Here, N_d is the doping concentration of multiplication layer of the PD and E_m is the maximum electric field. For M_p obtained from PT1 and PT2, the following equation can be used because the electric field distribution inside the depletion layer can be assumed to be uniform Fig. 2.7.

$$\beta(E) = \frac{\ln(M_\mathrm{p})}{W}. \tag{2.11}$$

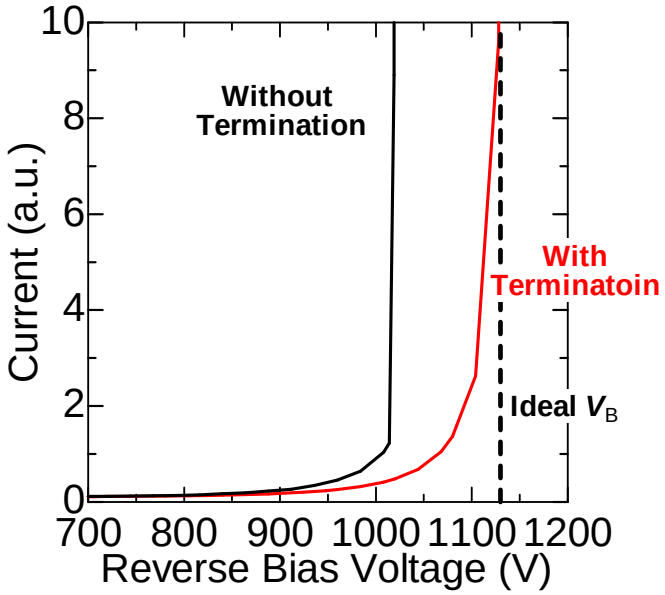
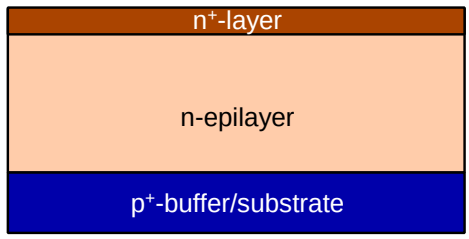
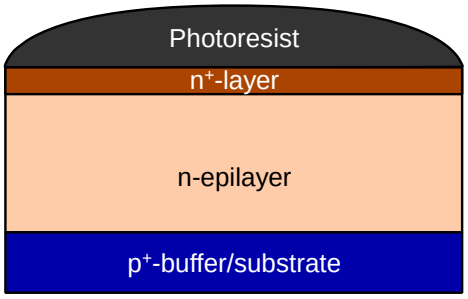


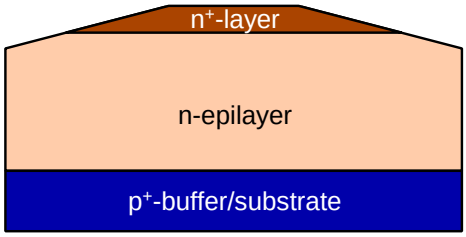
Figure 2.13: Simulated reverse I–V characteristics of PT diode with and without edge termination.



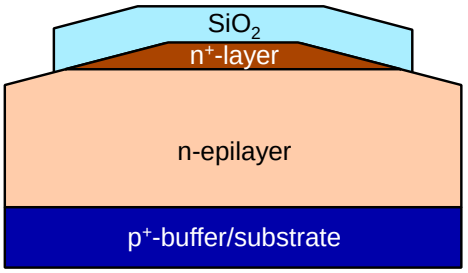
(a) N^+ and P^+ ion implantation followed by activation annealing (Ar, 1700°C, 20 min) to form the top n^+-contact layer



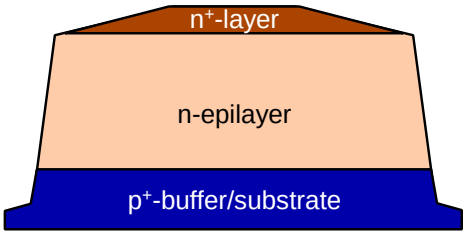
(b) Patterning of thick photoresist followed by high-temperature post bake for lens-like photoresist mask



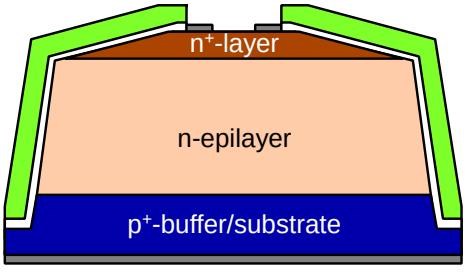
(c) CF_4-based CCP-RIE to translate the small bevel structure of photoresist mask to SiC



(d) Patterning and etching of PECVD deposited SiO_2 for the deep mesa etching



(e) Cl_2-based ICP-RIE for deep mesa etching



(e) Passivation (SiO_2+Polyimide) and electrode formation (Ti/Al → p-type; Ni → n-type)

Figure 2.14: Schematic figure of the fabrication process of PT1 and PT2.

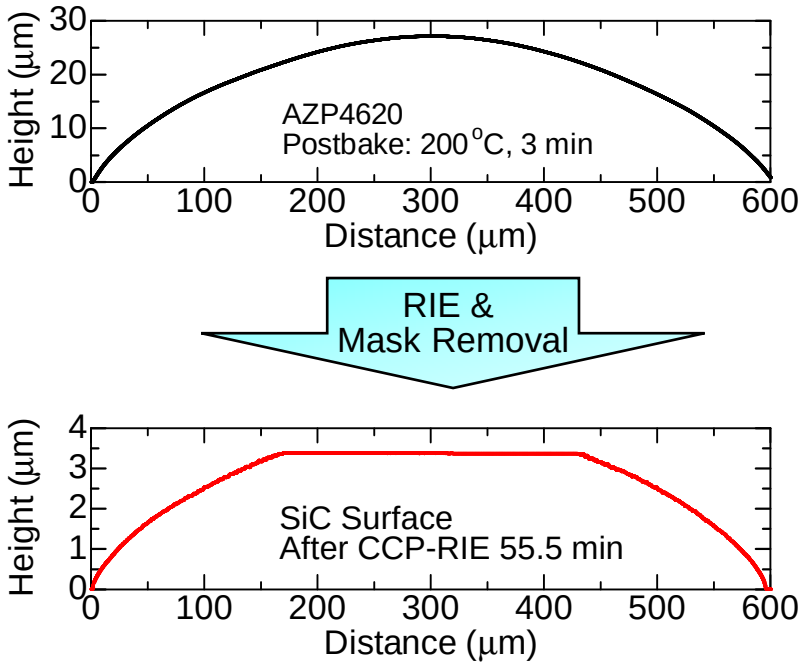


Figure 2.15: Surface profile of lens-like photoresist mask and the transferred small-beveled mesa of SiC.

Here, W is the width of multiplication layer [13]. At high electric field or near the breakdown voltage, the assumption $M_{\mathrm{n}} \to 1$ does not hold and equations (2.10) and (2.11) cannot be used.

2.4.2 Extraction of Electron Impact Ionization Coefficient α

The electron ionization coefficient α were extracted using M_{n} obtained from NPT3 and NPT4. Here, different equations of M_{n} are needed for NPT3 and NPT4 in the analysis because the multiplication factor depends on whether the carriers have been injected from the higher electric field side or the lower side. In other words, the equation of multiplication factor that represents the avalanche multiplication is different if the direction of carrier injection is different. The detail will be explained in Section 2.7. For M_{n} obtained from NPT3, carriers are injected from the lower electric field side, and the following equation can be used to extract α.

$$\alpha(E_{\mathrm{m}}) = \frac{qN_{\mathrm{a}}}{\varepsilon_0\varepsilon_{\mathrm{s}}} \cdot \frac{1}{M_{\mathrm{n}}^2} \cdot \frac{dM_{\mathrm{n}}}{dE_{\mathrm{m}}} \cdot \left(\frac{qN_{\mathrm{d}}}{\varepsilon_0\varepsilon_{\mathrm{s}}} \cdot \frac{1}{\beta(E_{\mathrm{m}}) \cdot M_{\mathrm{p}}^2} \cdot \frac{dM_{\mathrm{p}}}{dE_{\mathrm{m}}} \right)^{\frac{N_{\mathrm{d}}}{N_{\mathrm{a}}}}. \tag{2.12}$$

Here, N_{a} is the doping concentration of the multiplication layer of NPT3. N_{d} and M_{p} are the doping concentration of the multiplication layer and the measured multiplication factor of NPT1, respectively. In this equation, α can be obtained from the measured M_{n} and M_{p} obtained from a diode with a multiplication-layer structure close to that of NPT3, which is NPT1 in this study.

For M_{n} obtained from NPT4, on the other hand, carriers are injected from the higher electric field side and α can be expressed by the following equation in this case [26].

$$\alpha(E_{\mathrm{m}}) = \frac{qN_{\mathrm{d}}}{\varepsilon_0\varepsilon_{\mathrm{s}}} \cdot \frac{1}{M_{\mathrm{n}}} \cdot \frac{dM_{\mathrm{n}}}{dE_{\mathrm{m}}} - (M_{\mathrm{n}} - 1) \cdot \beta(E_{\mathrm{m}}). \tag{2.13}$$

Here, N_{d} is the doping concentration of the multiplication layer of NPT4.

In the case of NPT4, however, the dead space effect should be considered [4, 26]. The schematic illustration to explain the dead space effect is shown in Fig. 2.16. Here, a $\mathrm{p^+n}$ NPT structure is assumed where its electric field distribution can be shown in the upper part of the figure. When carriers are injected into the depletion layer, they need to gain enough energy (ionization threshold energy: $\varepsilon_{\mathrm{th}}$) before impact ionization occurs. Due to this acceleration of carriers, a region where impact ionization does not occur appears at each edge of depletion layer. For the lower electric field edge of depletion layer ($x = W$ in Fig. 2.16), this effect is negligibly small because its electric field is low enough and impact ionization does not occur. However, for carriers that are injected from the higher electric field side (in this case, electrons), appearance of the dead space region will affect the measured multiplication factor since large numbers of avalanche multiplication in this region is included in a conventional local model. In this study, the dead space region at the higher electric field side of depletion layer will be discussed. Because of this dead space effect for electrons, following effects must be considered:

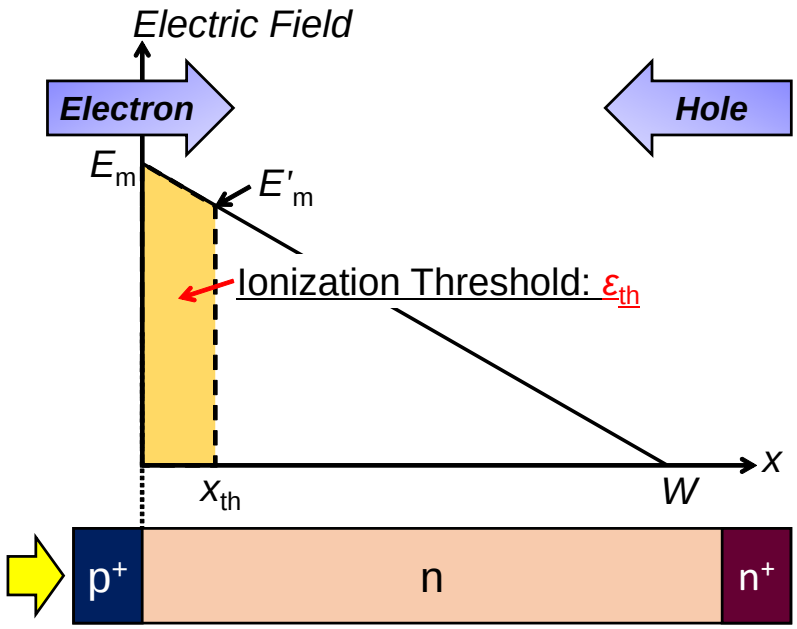


Figure 2.16: Schematic illustration of the dead space effect occurring in a p^+n NPT diode.

1. Because impact ionization does not occur in the dead space region, maximum electric field effective for the avalanche multiplication of electrons will decrease from E_{m} to E'_{m} in Fig. 2.16.

2. Although election impact ionization does not occur in this region, holes injected from the lower electric field side will cause impact ionization in the dead space region because they will have enough energy when they reach the region.

Due to these effects, the *"measured"* electron multiplication factor (M_{n}) will be different from the *"actual"* electron multiplication factor (M_{ni}) that can be used for the extraction of α shown in equation (2.13).

In this study, to take this dead space effect into account and to correct the *"measured"* M_{n} to the *"actual"* M_{ni}, a model proposed by Woods *et al.* [26] was employed while remodeling it to take the hole impact ionization into account. First, reduction of effective maximum electric field was taken into account by calculating the width of dead space region x_{th} using the following relationship between $\varepsilon_{\mathrm{th}}$ and x_{th}:

$$\varepsilon_{\mathrm{th}} = \int_0^{x_{\mathrm{th}}} E(x)\mathrm{d}x. \tag{2.14}$$

Here, $E(x)$ is the electric field profile inside the depletion layer. Then using the obtained x_{th}, effective maximum electric field E'_{m} can be calculated as $E(x_{\mathrm{th}})$. Next, the effect of hole impact ionization inside the dead space was considered using the following relationship between M_{n} and M_{ni}:

$$1 - \frac{1}{M_{\mathrm{n}}} = \left(1 - \frac{1}{M_{\mathrm{ni}}}\right) \cdot \exp\left(\int_0^{x_{\mathrm{th}}} \beta \mathrm{d}x\right). \tag{2.15}$$

Using the above equation, measured M_{n} was corrected to M_{ni}, and finally, obtained M_{ni} was used to extract α by equation (2.13) where M_{ni} was used instead of M_{n} in the equation. In all of these equations, β obtained from NPT1–2 and PT1–2 was used.

2.5 Determination of Impact Ionization Coefficients at Room Temperature

In this section, impact ionization coefficients will be derived from the photomultiplication measurement using PD structures and extraction methods explained in the previous section. Here, measurement results at room temperature (RT) are focused. The extracted ionization coefficients will be verified by calculating the breakdown voltage and multiplication factors, and comparing them with the measurement.

2.5.1 Impact Ionization Coefficients in Medium Electric Field Range

In this section, impact ionization coefficients in the medium electric field range are extracted using NPT1–3. The reverse I–V characteristics of NPT1 and NPT3 at RT are shown in Fig. 2.17 and Fig. 2.18. In both figures, (b) shows the photocurrent at relatively low reverse bias voltage. During the measurement, a BPF of 260 nm was used.

To calculate multiplication factors, initial unmultiplied current, or photocurrent without avalanche multiplication needs to be derived. Because the illuminated light is mainly absorbed near the surface of the diode, pure hole diffusion current and pure electron diffusion current from the top n^+ and p^+ layers will be the main component of the photocurrent in NPT1–2 and NPT3, respectively. The initial unmultiplied current can be obtained by fitting the following equation of the diffusion current to the measured photocurrent in the low reverse bias region where avalanche multiplication is not occurring.

$$I_{\mathrm{pdiff}} = qG_0 \frac{\alpha_0 L_{\mathrm{p}}}{1-\alpha_0^2 L_{\mathrm{p}}^2} \mathrm{e}^{-\alpha_0 w_{\mathrm{n}}} \cdot \left[\frac{L_{\mathrm{p}}(S + D_{\mathrm{p}}\alpha_0)\mathrm{e}^{\alpha_0 w_{\mathrm{n}}} - \left\{ L_{\mathrm{p}} S \cosh\left(\frac{w_{\mathrm{n}}}{L_{\mathrm{p}}}\right) + D_{\mathrm{p}} \sinh\left(\frac{w_{\mathrm{n}}}{L_{\mathrm{p}}}\right) \right\}}{D_{\mathrm{p}} \cosh\left(\frac{w_{\mathrm{n}}}{L_{\mathrm{p}}}\right) + L_{\mathrm{p}} S \sinh\left(\frac{w_{\mathrm{n}}}{L_{\mathrm{p}}}\right)} - L_{\mathrm{p}}\alpha_0 \right]. \tag{2.16}$$

Here, $G_0, \alpha_0, L_{\mathrm{p}}, D_{\mathrm{p}}, w_{\mathrm{n}}, S$ are the absorbed light flux, absorption coefficient, diffusion length of hole, diffusion coefficient of hole, neutral region width (width between top surface and top depletion layer edge), and surface recombination velocity [14]. The above equation can be used for NPT1–2, and by using L_{n}, D_{n}, and w_{p}, it can be also applied for NPT3. Using the above equation, the extrapolated initial unmultiplied current is shown by dot-dashed lines in Fig. 2.17 and Fig. 2.18 where the fitted parameters are shown in the table inside the figure. Here, the surface recombination velocity and absorption coefficients obtained by Kato *et al.* [29] and Cha *et al.* [19] were used, respectively. By dividing the measured current by the initial unmultiplied current, M_{p} and M_{n} were determined.

Figure 2.19 shows the calculated multiplication factors obtained at RT. In both figures, the inset plots $M-1$ on a logarithmic scale to show the small multiplication. M_{p} starts to increase at relatively low reverse bias voltage, whereas M_{n} increases abruptly near the breakdown voltage. This indicates that the hole ionization coefficient β is considerably higher than the electron ionization coefficient α at low electric field, which agrees well with the previous results [1, 5, 7, 8].

From obtained multiplication factors, ionization coefficients were extracted. For the calculation of β, equation (2.10) was used for M_{p} obtained from NPT1–2, and for α, equation (2.12) was used for M_{n} obtained from NPT3 and M_{p} obtained from NPT1. When using equation (2.12), the electric field dependence of β is needed. In this study, the final result of β shown in Section 2.5.4 was used here. The extracted electric field dependence of ionization coefficients are shown in Fig. 2.20. Ionization coefficients in the electric field range of

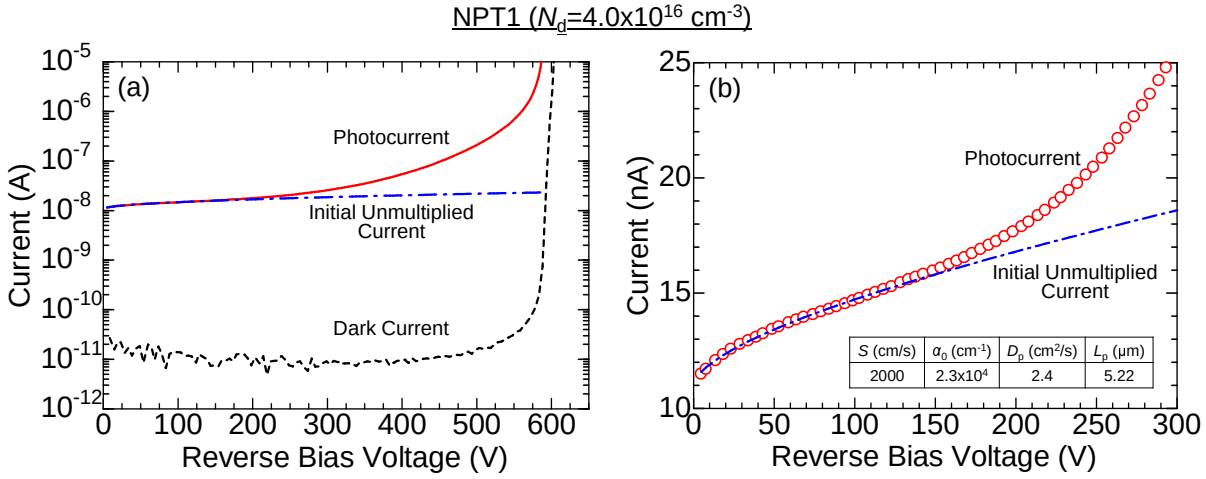


Figure 2.17: Reverse I–V characteristics of NPT1 at RT. Here, a BPF of 260 nm was used for the measurement of photocurrent. The initial unmultiplied current was obtained using equation (2.16).

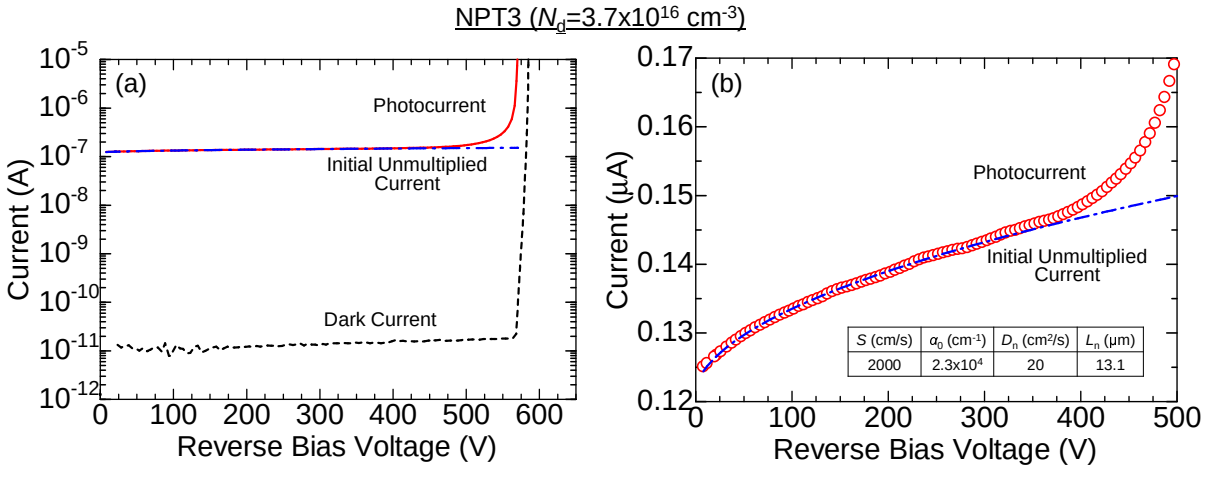


Figure 2.18: Reverse I–V characteristics of NPT3 at RT. Here, a BPF of 260 nm was used for the measurement of photocurrent. The initial unmultiplied current was obtained using equation (2.16).

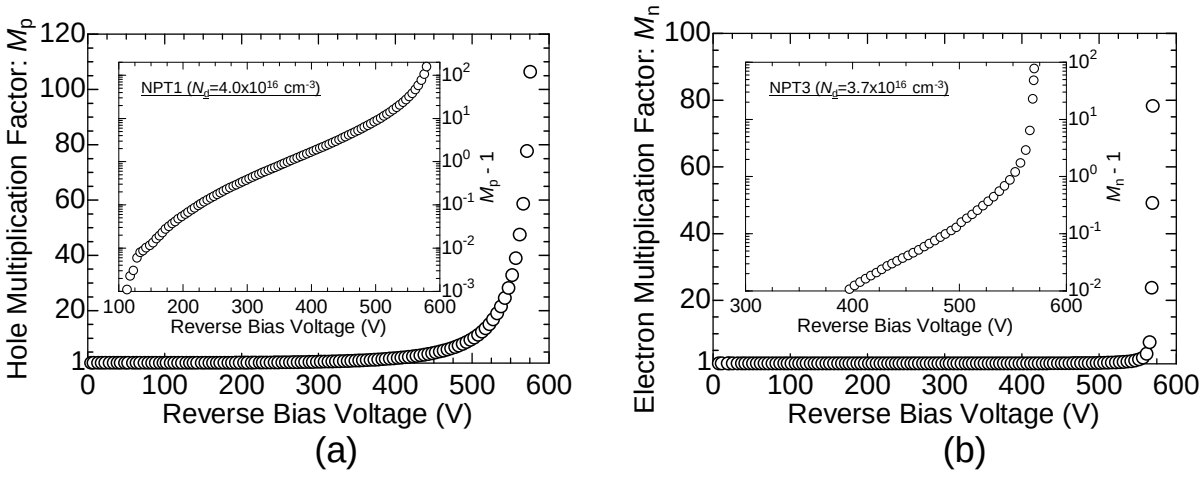


Figure 2.19: Reverse bias voltage dependence of multiplication factors. Inset shows the plot of $M-1$ on a logarithmic scale. (a) NPT1: measurement of M_{p}. (b) NPT3: measurement of M_{n}.

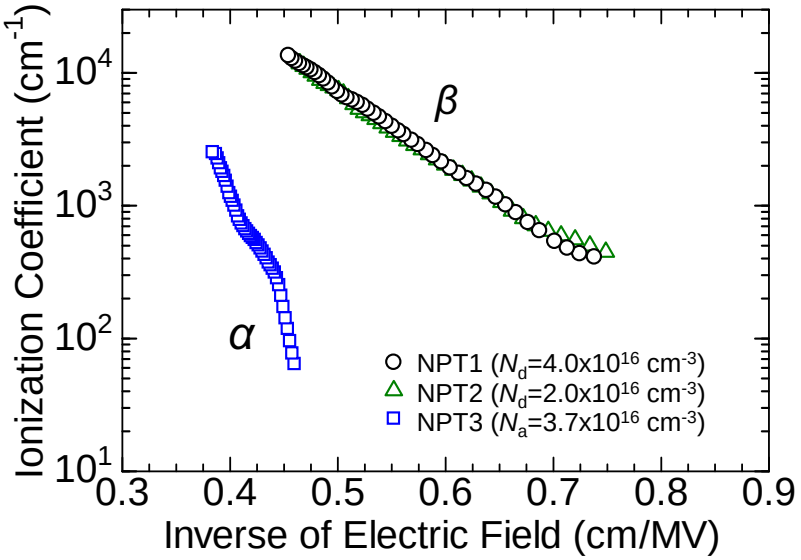


Figure 2.20: The extracted impact ionization coefficients from NPT1–3 at room temperature.

1.4–2.5 MV/cm ($0.4< 1/E <0.67$ cm/MV) was obtained by these PDs. For NPT1–2, calculated β is not shown for relatively high electric field (>2.3 MV/cm) because the assumption $M_{\mathrm{n}} \to 1$ does not hold in this region, and the equation (2.10) cannot be used.

2.5.2 Impact Ionization Coefficients in High Electric Field Range

In this section the impact ionization coefficient in a high electric field range are extracted using NPT4. The reverse I–V characteristics of NPT4 at RT is shown in Fig. 2.21. Here, a BPF of 260 nm was used during the measurement.

For the calculation of multiplication factor, the initial unmultiplied current needs to be obtained. In the case of this measurement, the initial unmultiplied current should take a constant value. For the ideal case, because the p^+-contact layer is highly doped compared with the multiplication layer, depletion layer width inside the p^+-contact layer should be extremely thin, and the change of its width should be negligible. Therefore, the width between top surface of the diode and depletion layer edge in p^+-contact layer should not change, resulting in a constant photocurrent. However, from Fig. 2.21(b), the initial unmultiplied current is increasing a little with the reverse bias voltage. This indicates that the depletion-layer broadening inside the p^+-contact layer may not be negligible in this case, because the multiplication layer has high doping concentration compared with a conventional PD such as NPT3, In this study, to take this depletion-layer broadening of the contact layer into account, a linear extrapolation of photocurrent at low reverse bias voltage where multiplication is not occurring was used, which is commonly employed in this type of analysis [7].[1] The extracted initial unmultiplied current is shown by dot-dashed line in Fig. 2.21. By dividing the measured photocurrent by the initial unmultiplied current, M_{n} was calculated.

Figure 2.22 shows the maximum electric field dependence of $M_{\mathrm{n}} - 1$ from NPT4 together with the experimental result of NPT3. Compared with NPT3, avalanche multiplication begins at higher maximum electric field for NPT4. When the doping concentration of the multiplication layer is higher, carriers cannot gain high energy from the electric field at a given maximum electric field. Therefore, larger maximum electric field are necessary for the same quantity of avalanche multiplication to occur for NPT4 having multiplication layer with higher doping concentration. Because avalanche multiplication occurs at higher maximum electric field for NPT4, it enables the extraction of ionization coefficient at higher electric field.

For the extraction of ionization coefficients using NPT4, however, the dead space effect must be considered. Here, dead space correction explained in Section 2.3.2 was done and the *"actual"* multiplication factor M_{ni} was extracted from the *"measured"* multiplication

[1] When equation (2.16) was assumed for the initial unmultiplied current, a good fitting could not be obtained probably due to the uncertainty of physical properties such as S and D_{n}.

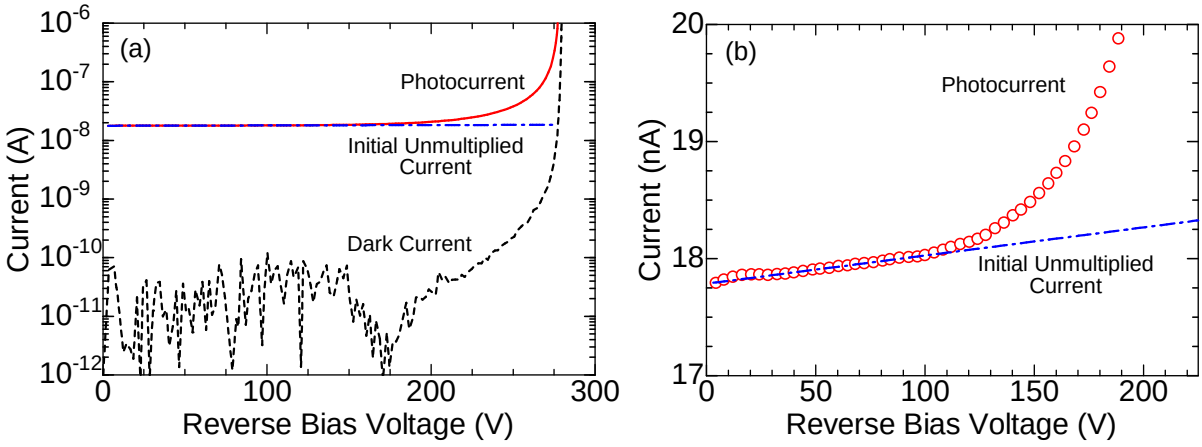


Figure 2.21: Reverse I–V characteristics of NPT4 at RT. Here, a BPF of 260 nm was used for the measurement of photocurrent. The initial unmultiplied current was obtained by a linear extrapolation.

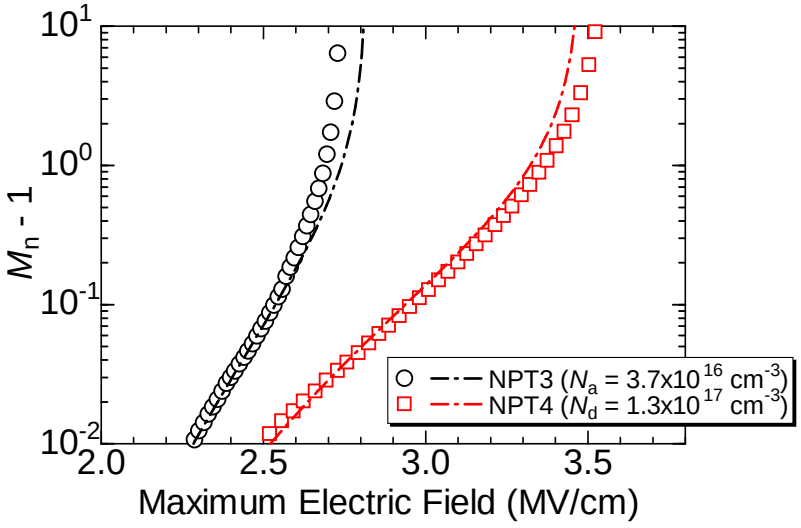


Figure 2.22: Maximum electric field dependence of $M_\mathrm{n} - 1$ obtained from NPT3 and NPT4. Here, symbols show the measurement results, and lines show the simulated $M_\mathrm{n} - 1$ using ionization coefficients obtained in this study.

factor $M_{\rm n}$ assuming various values of ionization threshold energy $\varepsilon_{\rm th}$. Figure 2.23 shows the *"effective"* maximum electric field $E'_{\rm m}$ dependence of $M_{\rm ni}$ at various values of $\varepsilon_{\rm th}$. When the dead space correction is made, corrected $M_{\rm ni}$ increases at low $E'_{\rm m}$, and decreases at high $E'_{\rm m}$. At low $E'_{\rm m}$ (<3.0 MV/cm), the dead space width is comparable to the whole depletion layer width. Therefore, effect of $E'_{\rm m}$ reduction, which also means an $M_{\rm ni}$ increase, is enhanced especially at this low electric field region. Because the dead space width will widen with the increasing $\varepsilon_{\rm th}$, $M_{\rm ni}$ is increasing (or $E'_{\rm m}$ decreasing) with $\varepsilon_{\rm th}$. At high $E'_{\rm m}$ (>3.3 MV/cm), on the other hand, impact ionization of holes inside the electron dead space region causes a large effect. Because large portion of the measured photocurrent with avalanche multiplication will contain carriers generated by the hole impact ionization in the dead space region, $M_{\rm ni}$ will become smaller than $M_{\rm n}$. Here, a wider dead space region (larger $\varepsilon_{\rm th}$) will cause much more avalanche multiplication by holes in the dead space, which results in the decrease of $M_{\rm ni}$ with the increasing $\varepsilon_{\rm th}$.

Using the corrected $M_{\rm ni}$, the electron ionization coefficient α was calculated using equation (2.13), while using $M_{\rm ni}$ instead of $M_{\rm n}$. Figure 2.24 shows the calculated α using various values of $\varepsilon_{\rm th}$. Fortunately, the impacts of $\varepsilon_{\rm th}$ on the calculated α was very small for the device structure used in this study. Because effect of the $E'_{\rm m}$ reduction and the hole impact ionization inside the dead space region have an opposite effect to $M_{\rm ni}$, it may have canceled out each other, resulting in the small difference of α. However, it should be noted that this does not mean that the dead space effect can be neglected in SiC. For example, Ng *et al.* [4] have shown experimentally that in an avalanche photodiode with a thin multiplication layer (∼0.1–0.2 μm) the dead space effect must be considered for its characterization. Furthermore, the dead space correction used in this study is the most simple case, and when the depletion layer is extremely thin, even the concept of impact ionization coefficients [$\alpha(E)$ and $\beta(E)$] may not be used in that case [26]. For the further understanding of the nonlocal effects in SiC, further theoretical studies will be required such as by Monte Carlo simulations [11].

Because the difference of $\varepsilon_{\rm th}$ was less sensitive to the calculated α, $\varepsilon_{\rm th}$ of 10 eV [1] was used for the extraction of α in this study. Figure 2.25 shows the extracted α from NPT4 together with α obtained from NPT3 in the previous section. Compared with the result of NPT3, α was successfully extracted to the higher electric field of 3.2 MV/cm.

2.5.3 Impact Ionization Coefficients in Low Electric Field Range

In this section, impact ionization coefficients at low electric field range are extracted using PT1–2 toward the accurate calculation of UHV devices. The reverse I–V characteristics of PT1 at RT is shown in Fig. 2.26. Here, a BPF of 254 nm was used during the measurement.

For the calculation of initial unmultiplied current, a linear extrapolation was used as similar to NPT4 to take the depletion layer broadening into account. Here, equation (2.16) could not be used because the top contact layer was fabricated by ion implantation: The

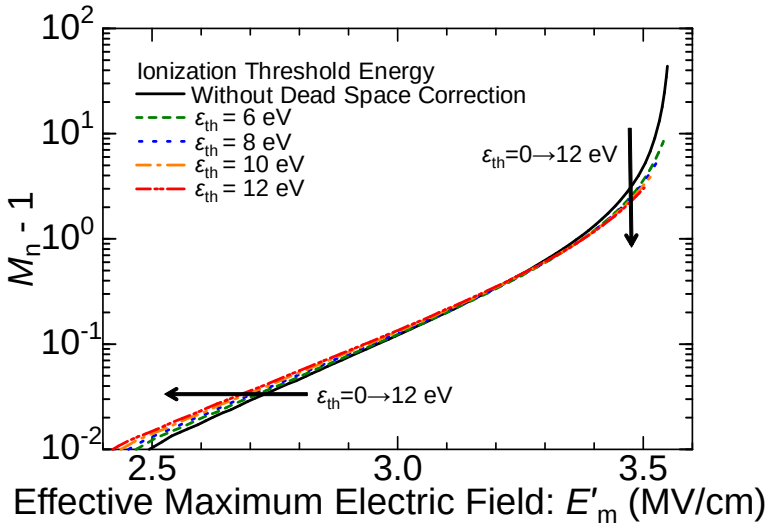


Figure 2.23: Effective maximum electric field (E'_{m}) dependence of "*actual*" multiplication factor M_{ni} calculated with various values of electron ionization threshold energy ($\varepsilon_{\mathrm{th}}$).

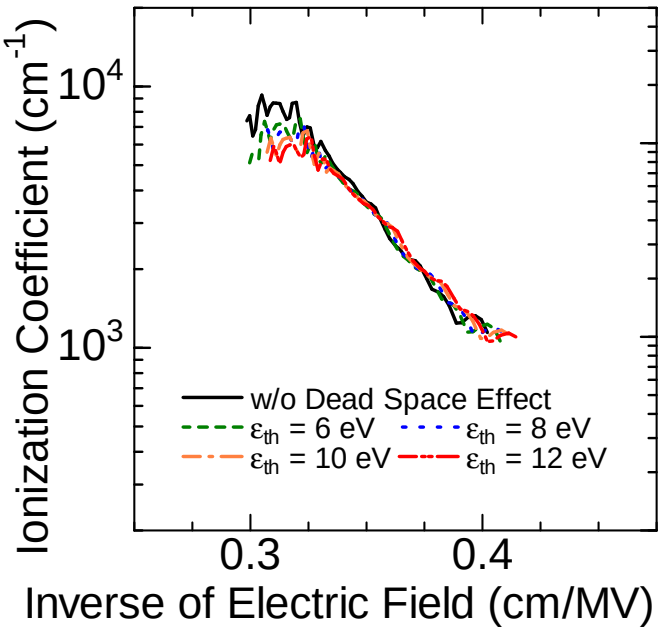


Figure 2.24: Extracted electron ionization coefficient α from NPT4, where M_{ni} calculated at various values of $\varepsilon_{\mathrm{th}}$ was used.

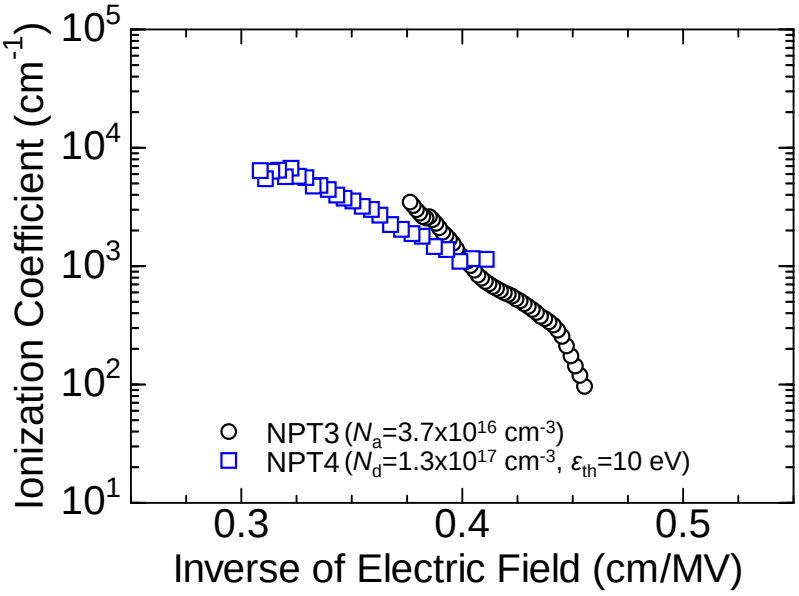


Figure 2.25: Extracted electron ionization coefficient α at room temperature from NPT3 and NPT4. For NPT4, $\varepsilon_{\mathrm{th}} = 10$ eV was used for the dead space correction.

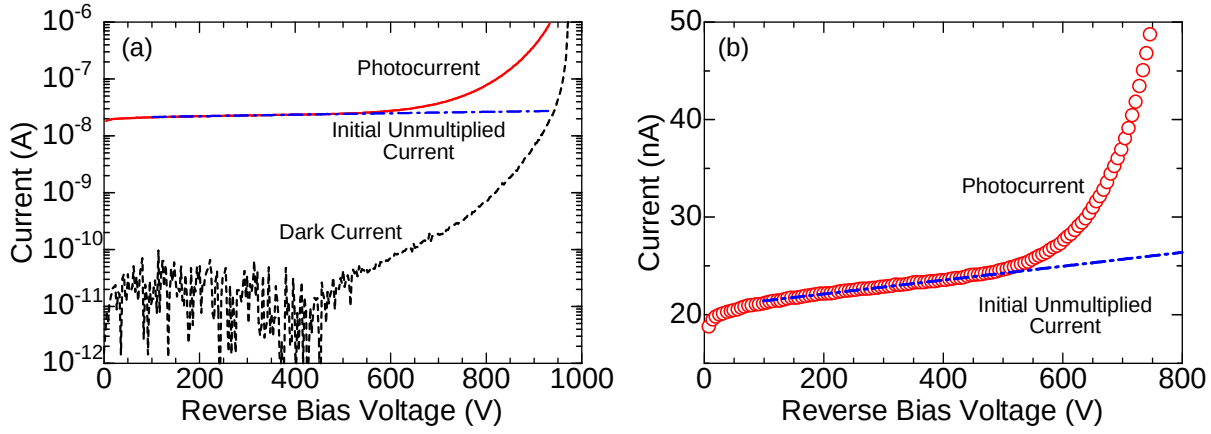


Figure 2.26: Reverse I–V characteristics of PT1 at RT. Here, a BPF of 254 nm was used for the measurement of photocurrent. The initial unmultiplied current was obtained by a linear extrapolation.

doping profile is complicated at the n^+/n^- junction, making calculation of width between the surface and depletion layer edge difficult. The extracted initial unmultiplied current is shown by dot-dashed line in Fig. 2.26. By dividing the measured photocurrent by the initial unmultiplied current, M_p was calculated.

Figure 2.27 shows the maximum electric field dependence of $M_p - 1$ from PT1–2 together with the experimental results of NPT1–2. For PT1–2, maximum electric field was calculated using constant electric field assumption: $E_m = V/W$ where V is the reverse bias voltage and W is the depletion layer width.Compared with NPT1–2, PT1–2 begins avalanche multiplication at lower maximum electric field. When the doping concentration is lower, injected carriers can gain more energy from the electric field at the same maximum electric field. This will result in a larger value of multiplication factor, making M_p of NPT2 to be larger than that of NPT1, and PT1–2 to be larger than NPT1–2 at the same maximum electric field. Between PT1–2, increasing the width of multiplication layer will cause a similar effect; PT1 exhibits a larger multiplication factor than PT2 at the same maximum electric field.

Using the obtained M_p, the hole ionization coefficient β was calculated using equation (2.11). Figure 2.28 shows the calculated β together with that of NPT1–2. By using PT1–2, β was successfully determined down to an electric field of 1 MV/cm accurately for the first time in SiC.[2] Ionization coefficients at this low electric field is the most important range for designing UHV devices.

2.5.4 Fitting and Verification of Extracted Impact Ionization Coefficients

To use the extracted impact ionization coefficients in a device simulation, experimental results must be fitted by mathematical equations. For the electric field dependence of ionization coefficients, a number of expressions have been proposed both empirically [30–32] and theoretically [33–36]. Among these expressions, modified Chynoweth's expression [30]: $\alpha, \beta = a \cdot \exp\left[-(b/E)^c\right]$ has been chosen in this study because it is the most simple, and most common expression used in the studies of ionization coefficients. In this equation, a, b, and c is the fitting parameters, and E is the electric field strength.

Figure 2.29 shows the extracted electron (α) and hole (β) impact ionization coefficients in this study. These experimental results were fitted and the results are shown by solid lines, where its equation can be expressed as follows:

$$\alpha(E) = 1.43 \times 10^5 \cdot \exp\left[-\left(\frac{4.93 \times 10^6}{E}\right)^{2.37}\right] \ \mathrm{cm}^{-1} \tag{2.17}$$

[2]Although Loh *et al.,* [7] have also extracted β down to 0.9 MV/cm, air sparking was occurring during the measurement, which will lead to inaccuracies for the extracted β. Furthermore, data points of the measurement is very few in their case.

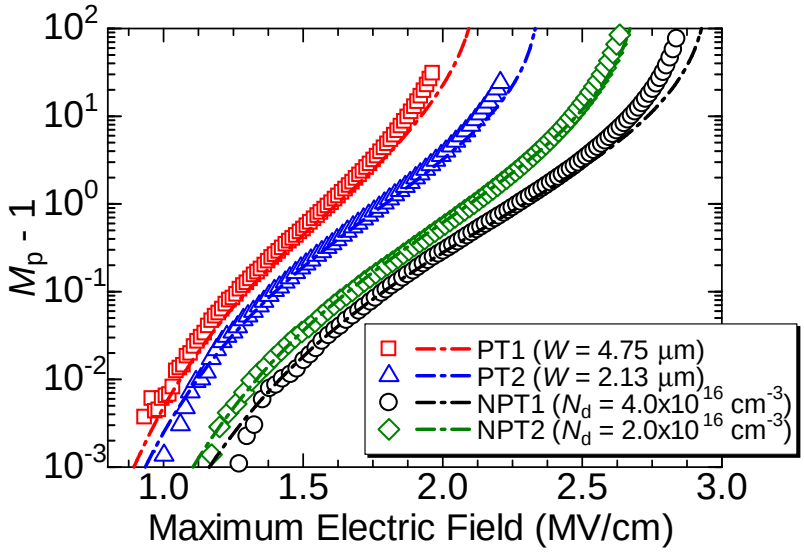


Figure 2.27: Maximum electric field dependence of $M_p - 1$ obtained from PT1–2 and NPT1–2. Here, symbols show the measurement results, and lines show the simulated $M_p - 1$ using ionization coefficients obtained in this study.

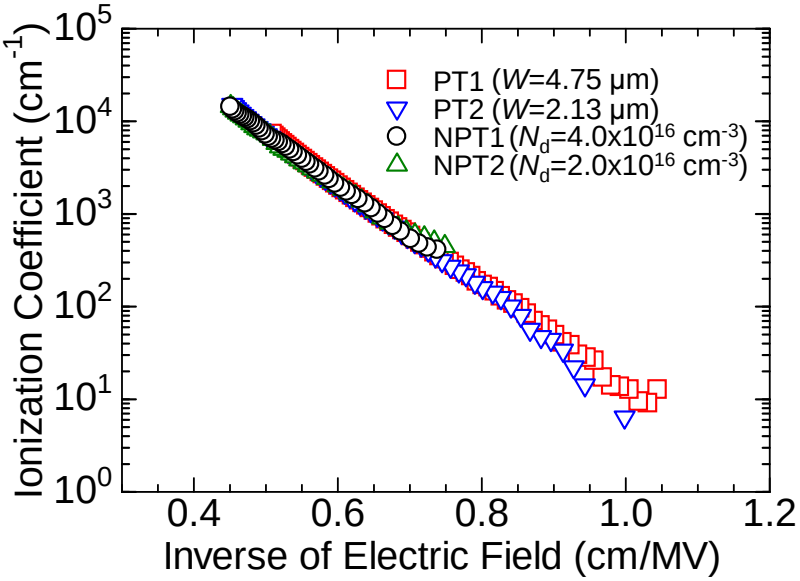


Figure 2.28: Extracted hole ionization coefficient β at RT from PT1–2 and NPT1–2.

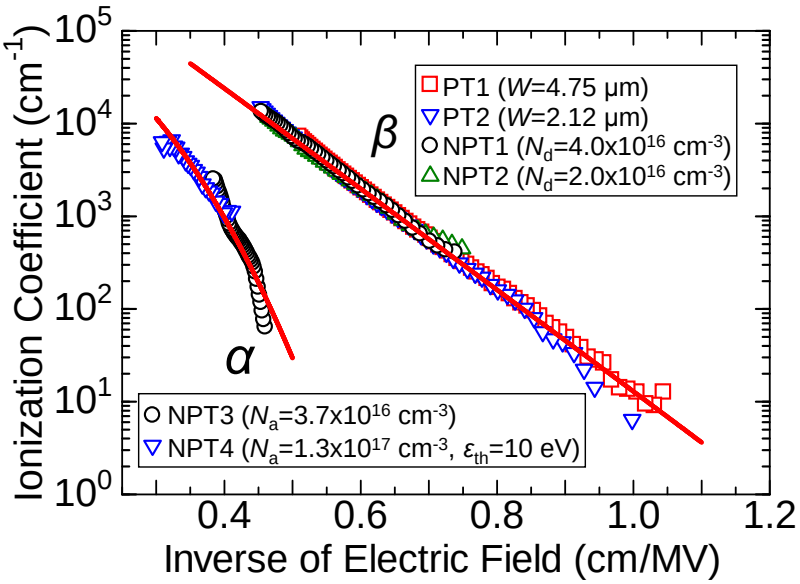


Figure 2.29: Fitting of ionization coefficients obtained in this work using modified Chynoweth's expression.

$$\beta(E) = 3.12 \times 10^6 \cdot \exp\left[-\left(\frac{1.18 \times 10^7}{E}\right)^{1.02}\right] \text{ cm}^{-1}. \quad (2.18)$$

Here, E is the electric field strength in V/cm. The determined impact ionization coefficients can be used in a wide range of electric field of 1–3 MV/cm.

The extracted ionization coefficients were first verified by calculating the multiplication factors. Calculated maximum electric field dependences of multiplication factors are shown by lines of Fig. 2.22 and Fig. 2.27. For the calculation of NPT4, the dead space effect with $\varepsilon_{\text{th}} = 10$ eV was considered for the calculation. The simulated multiplication factors agree very well with the experimental results in a wide range of electric field, indicating the successful extraction of ionization coefficients.

Figure 2.30 shows the doping concentration dependence of breakdown voltage for a p^+n NPT diode. In the figure, not only the experimental and calculated results of this study are shown, but also results from past literatures are shown. The breakdown voltage calculated using ionization coefficients obtained in this study has reproduced the experimental results including values reported from other groups very well. In addition, ideal breakdown voltage for PiN structure with various i-layer thickness has been calculated, as shown in Fig. 2.31. Here, circles show experimental results of PiN diodes [37] and BJT [38] with the corresponding i-layer structures, which shows fairly good agreement with the calculated results using the obtained ionization coefficients. Although these devices have an appropriate edge termination to alleviate the electric field crowding, complete alleviation is difficult in actual devices. Therefore, experimental breakdown voltage is slightly lower than the calculated ideal breakdown voltage. For the calculation results using other ionization coefficients, however, they are causing underestimation (for Loh's coefficients) or overestimation (for Konstantinov's coefficients) of breakdown voltage. These calculation results, indicates that ionization coefficients determined in this study can be used for the accurate design and the breakdown characterizations of SiC power devices. Toward the further improvement of accuracy in calculation of breakdown voltage, determination of α at lower electric field will be a key issue.

2.5.5 Discussion

In this section, the ionization coefficients extracted in this study are compared with those from past literatures, and the differences from them are discussed. Figure 2.32 shows the ionization coefficients obtained in this study with those reported by other groups. In the figure, symbols show the data actually determined and the lines are the fitted results.

For hole ionization coefficient β, the work by Loh and Green is taking similar values to the obtained β in this study. Because their measurement was done using a short-wavelength (244 nm) illumination as in this study (254 or 260 nm), an accurate measurement was realized, which resulted in the similar values of β. On the other hand, Konstantinov and

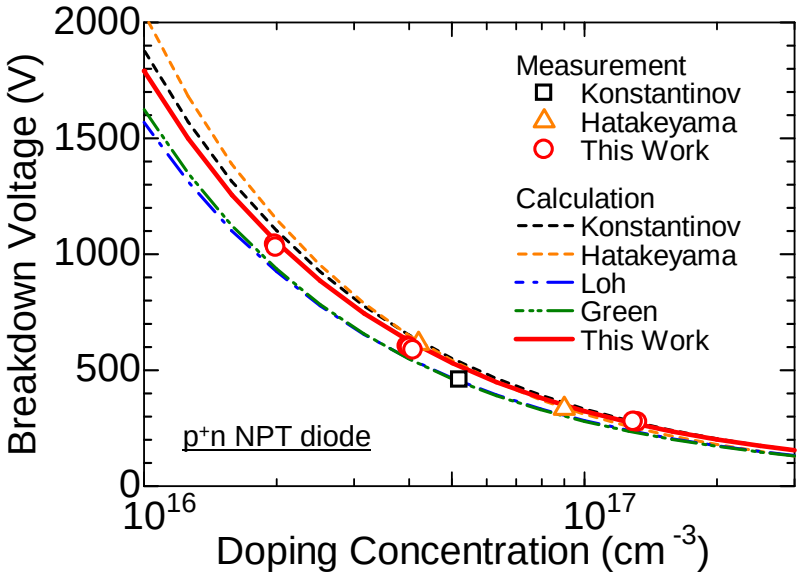


Figure 2.30: Simulated doping concentration dependence of ideal breakdown voltage and experimental results for p$^+$n NPT diodes. Calculation was done using ionization coefficients obtained from [1, 5, 7, 8] and values obtained in this study.

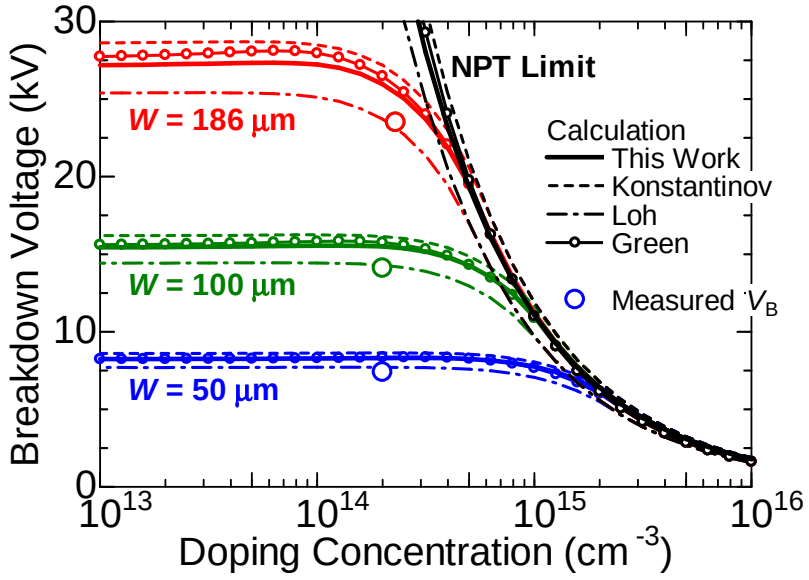


Figure 2.31: Simulated doping concentration dependence of ideal breakdown voltage and experimental results for PiN structures with various i-layer thicknesses. Experimental results were obtained from PiN diodes and BJT with appropriate edge termination, and calculation was done using ionization coefficients obtained from this study and [1, 5, 7, 8].

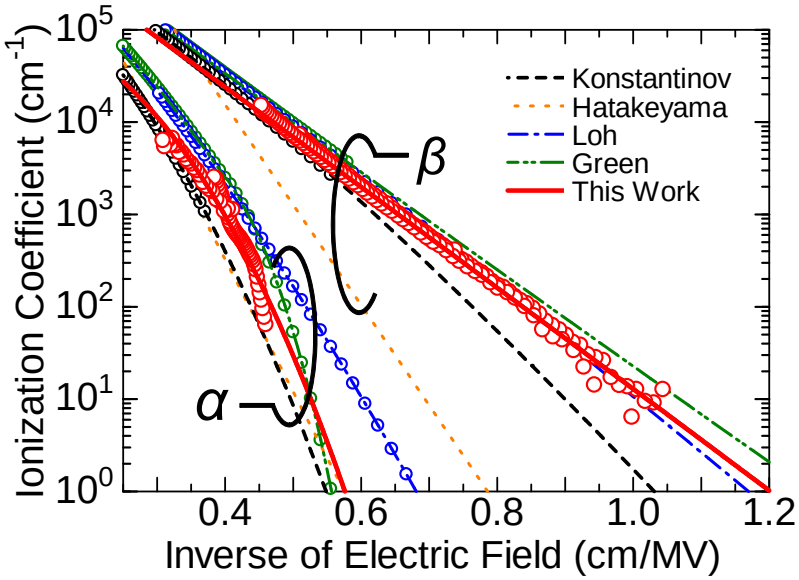


Figure 2.32: Ionization coefficients obtained in this study with results in [1, 5, 7, 8]. Symbols: extracted values from the experiment. Lines: calculation result of the fitting equations.

Hatakeyama's results are taking lower values than that of others. This difference can be explained by the difference in the wavelength of illumination light used in the measurement, as pointed out by Loh. When the photomultiplication measurement was done using illumination with inappropriate wavelength (not short enough), considerable effect of M_{dep} and M_{n} will occur for the measurement of M_{p}. From equation (2.5)–(2.7), M_{dep} and M_{n} are smaller than M_{p} at relatively high electric field for SiC. Because the measured M will be the average of M_{p}, M_{n}, and M_{dep} weighted by the component of photocurrent as shown in equation (2.9), measured M will be smaller than a pure M_{p}, meaning underestimation of M_{p} in the photomultiplication measurement. This may result in the underestimation of β, which is actually observed in Fig. 2.32.

Although β is taking a similar value in this study with Loh and Green, for the electron ionization coefficient α, there are definite differences among them. Because α takes much smaller values compared with β, and has a strong electric field dependence, both measurement and analyzing of M_{n} must be carefully conducted to determine α precisely. If M_{n} was measured using an excitation light with inappropriate wavelength, a mixed carrier multiplication will take place which will cause a large error in the measured M_{n}. In addition, extraction method using an approximation of electric field distribution (e.g. uniform distribution) must be carefully considered because this can also cause errors when extracting α. For example, if a difference between the maximum and the minimum electric field strength inside a PT depletion layer is not negligible, $\alpha(E)$ may have a distribution inside depletion layer by an order of magnitude due to the sharp increase of α by the change of electric field. In this case, if a constant electric field is assumed, it is impossible to approximate the $\alpha(E)$ to be constant by the large difference of $\alpha(E)$ inside the depletion layer. During the measurement by Loh and Green, there are a problem for this consideration: The doping concentration and thickness of multiplication layer used in their PD is not sufficient to use the constant electric field approximation. In this study, to obtain α accurately, a sufficiently short wavelength excitation was employed in the photomultiplication measurement to obtain a pure M_{n}. Moreover, the extraction method of α shown in equations (2.12) and (2.13) does not rely on any approximation in electric field distribution, which enables an accurate extraction of α. Therefore, the ionization coefficients in this study can accurately reproduce the experimental breakdown voltage as shown in Fig. 2.30, and will be suitable to simulate breakdown voltage of SiC power devices.

2.6 Temperature Dependence of Impact Ionization Coefficients

In this section, temperature dependence of impact ionization coefficients is investigated. A high temperature (HT) measurement up to 150°C was performed, and ionization coefficients were extracted by a similar method used in RT measurement. The temperature

dependence of ionization coefficients will be verified by comparing the experimental results with calculation results.

2.6.1 High Temperature Measurement for Impact Ionization Coefficients

The high temperature measurement of PDs was done by heating the stage of the measurement setup. Figure 2.33 shows the temperature dependence of reverse I–V characteristics of NPT1 and NPT3. Not only NPT1 and NPT3, but also other PDs have shown a positive temperature coefficient of breakdown voltage, indicating avalanche breakdown. For the dark current, its value has increased with temperature, which may be due to the generation current originating from carrier generation along the mesa periphery [39]. In the high-temperature measurement of the photocurrent, BPF was changed (260 nm $\rightarrow$ 270 nm) to obtain enough photocurrent, because photocurrent decreased due to the increase of absorption coefficient at high temperature [40]. Changing the BPF (260 nm $\rightarrow$ 270 nm) will increase the penetration depth of the illumination light and result in higher photocurrent, which is beneficial for accurate determination of ionization coefficients. Here, the penetration depth is still short enough for a pure carrier injection.

Figure 2.34 shows the temperature dependence of multiplication factors from NPT1 and NPT3, in other words M_{p} and M_{n}, respectively. As the temperature increases, both of the multiplication factors decrease resulting in the positive temperature coefficient of breakdown voltage. This also indicates the negative temperature coefficient of ionization coefficients, as in the case of other semiconductor materials.

Using the extraction method used in RT measurement, Fig. 2.35 shows the extracted impact ionization coefficients at elevated temperatures. This temperature dependence was modeled using the Okuto-Crowell model [31]:

$$\alpha, \beta(E) = a \cdot (1 + c(T - T_0))\, E^{\gamma} \cdot \exp\left[- \left(\frac{b[1 + d(T - T_0)]}{E} \right)^{\delta} \right] \ \mathrm{cm}^{-1} \tag{2.19}$$

where E, T are the electric field strength in V/cm and temperature in Kelvin. The obtained parameters are summarized in Table 2.2. These parameters are valid from room temperature to elevated temperatures up to 150°C. In this study, β showed a negative temperature coefficient. However, the temperature dependence of α was very small in the measured range of electric field and temperature. This makes the values of α obtained at room temperature to be used for high temperature simulation. The origin of the temperature dependency will be discussed in the next section.

2.6.2 Discussion

In this section, origins of the temperature dependency of ionization coefficients are discussed, followed by the verification of ionization coefficients by comparing the experiment

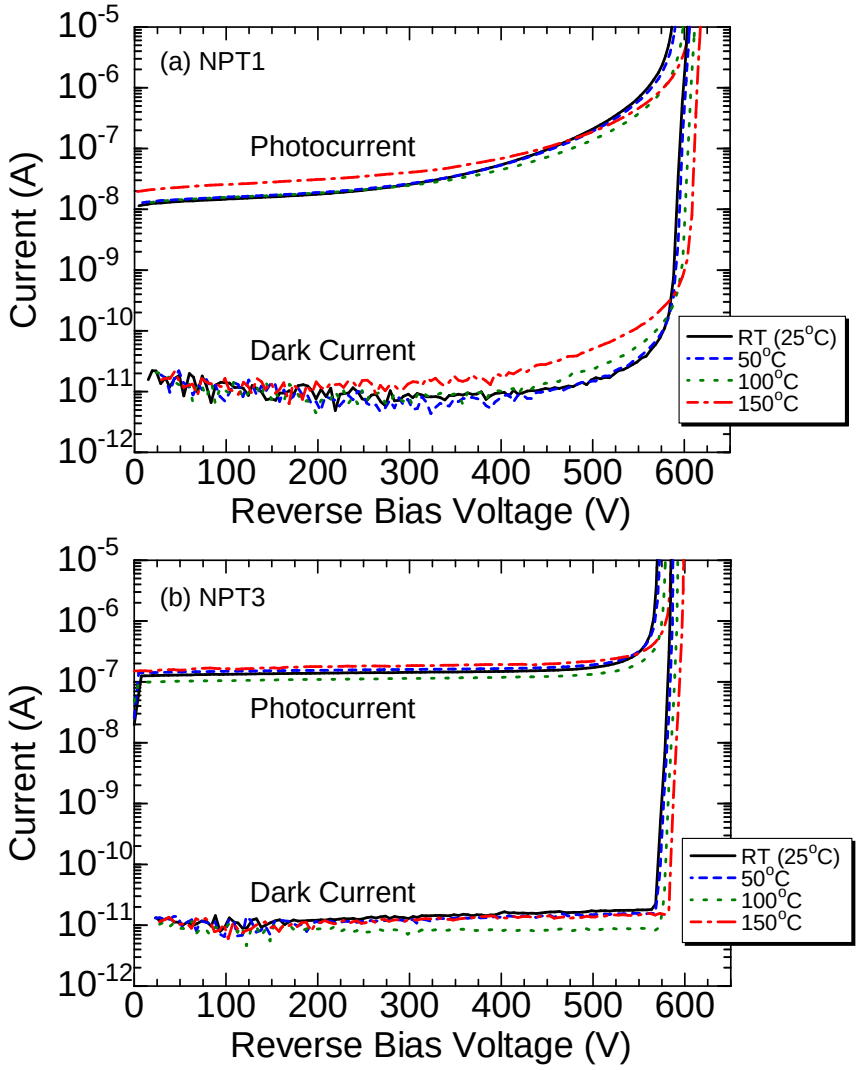


Figure 2.33: Dark and photo-current of (a) NPT1 and (b) NPT3 at room temperature and elevated temperatures up to 150°C.

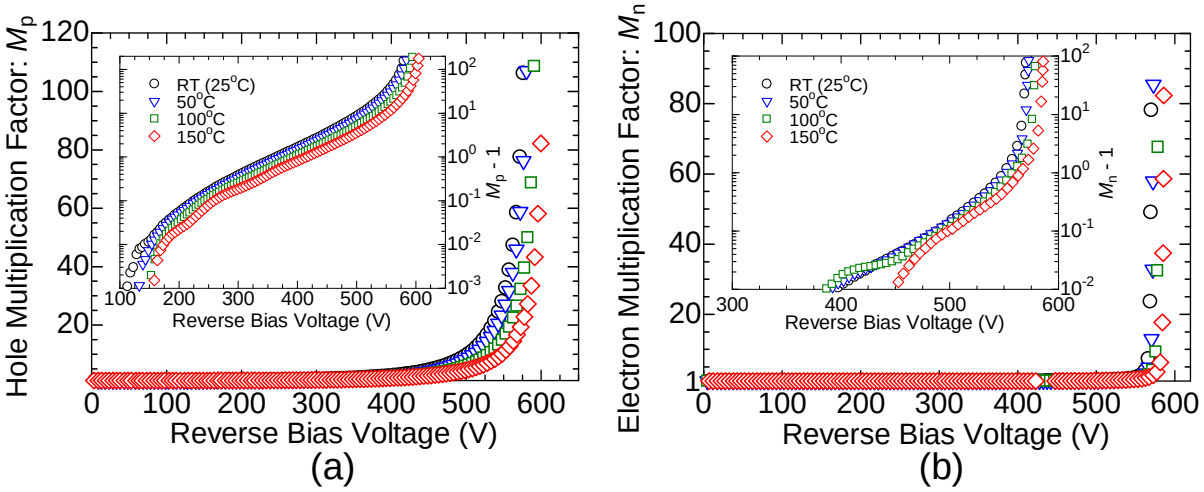


Figure 2.34: Reverse bias voltage dependence of multiplication factors at elevated temperatures up to 150°C. The inset shows the plot of $M-1$ on a logarithmic scale. (a) NPT1: measurement of M_{p}. (b) NPT3: measurement of M_{n}.

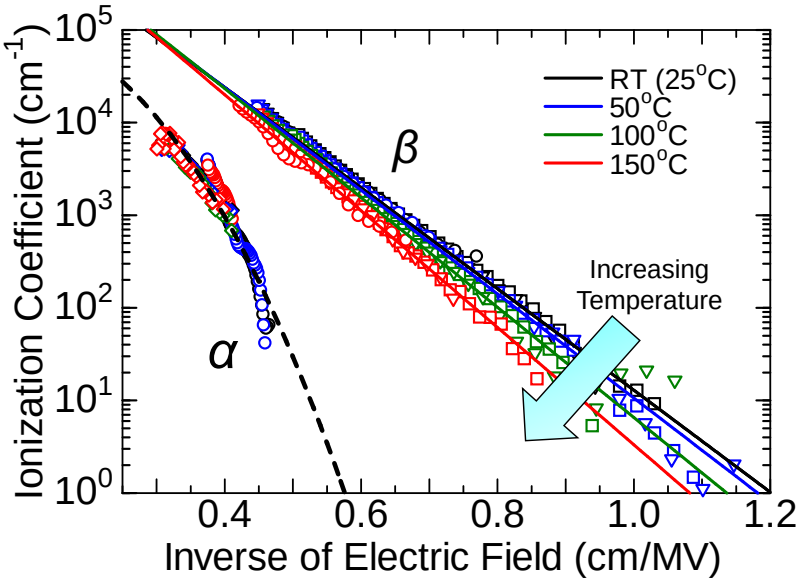


Figure 2.35: Measured ionization coefficients (symbols) and the modeled results using Okuto-Crowell model (lines) obtained at elevated temperatures.

Table 2.2: Parameters obtained from fitting temperature dependence of ionization coefficients by the Okuto-Crowell model.

	Electrons (α)	Holes (β)
a (1/V)	1.43×10^{5}	3.14×10^{6}
b (V/cm)	4.93×10^{6}	1.18×10^{7}
c (1/K)	0	6.30×10^{-3}
d (1/K)	0	1.23×10^{-3}
T_0 (K)	300	300
γ	0	0
δ	2.37	1.02

and calculation.

The β values showed a negative temperature coefficient which can be ascribed to the enhanced phonon scattering at elevated temperature as in other semiconductor materials [41]. The increase of phonon scattering will reduce the mean free path for the optical phonon generation, leading to the reduction of carrier energy obtained from the electric field. On the other hand, the temperature dependency of α is somewhat unusual. However, this may be linked to the fact that impact ionization of electrons along c-axis in 4H-SiC is strongly affected by the narrow width of the conduction band [1]. Although the increase of phonon scattering should occur at elevated temperatures, an opposite effect may exist such as widening of the unusual conduction band width in 4H-SiC, which will enable electrons to gain energy more easily. This may cancel out the negative temperature coefficient due to phonon scattering and may result in the small temperature dependence of α. To verify this speculation and to further understand the impact ionization of electrons in 4H-SiC, theoretical studies such as accurate calculation of the conduction band (up to the high energy region) is required.

Using the temperature dependence of ionization coefficients, temperature dependence of breakdown voltage was calculated. Figure 2.36 shows the comparison of temperature dependence of breakdown voltage measured in this work and the calculated result. For NPT1 and NPT2, measurement results and the calculation agree well with each other. For PT1, the measurement results are a bit lower than the calculated results, probably because electric field crowding near the edge could not be completely alleviated. However, the tendency for the increase of breakdown voltage agrees well with each other. These results suggest that the obtained temperature dependence of ionization coefficients can be used to accurately predict the breakdown voltage of power devices at high temperature, at least, up to 150°C.

2.7 Application of Impact Ionization Coefficients

In this section, critical electric field strength and ideal breakdown voltage are calculated using the impact ionization coefficients obtained in this study. Temperature dependence of critical electric field is also shown, together with an important reminder when using a critical electric field in device designing and characterization. For the ideal breakdown voltage, differences occurring by the different conduction type of voltage blocking layer are focused.

2.7.1 Critical Electric Field Strength

Critical electric field strength is defined as the maximum electric field strength at breakdown (ionization integral = 1) for a NPT diode structure. Although impact ionization coefficients are the key properties when simulating breakdown voltage, use of critical electric field

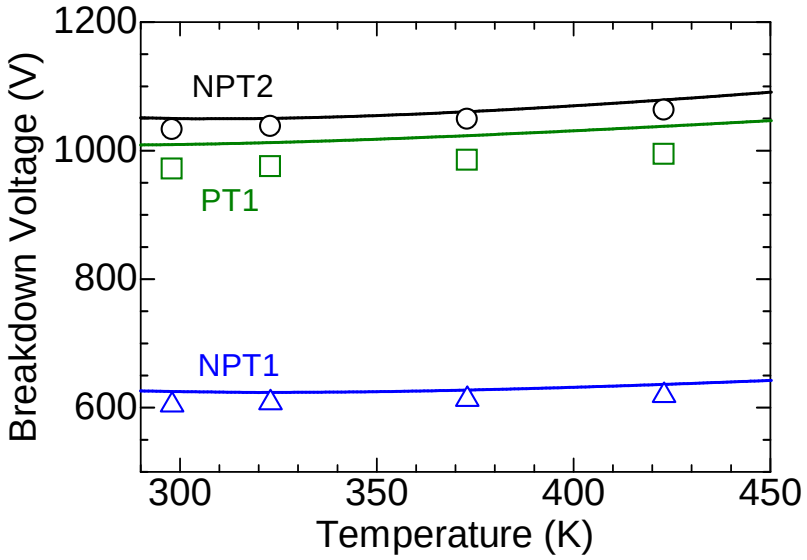


Figure 2.36: Temperature dependence of breakdown voltage for NPT1, NPT2, and PT1. Lines: simulated results using the temperature dependence of ionization coefficients obtained in this study.

strength is a more convenient way when designing power devices. By using the obtained temperature dependence of impact ionization coefficients, the temperature dependence of critical electric field strength was calculated. Here, p^+n NPT diodes were considered and the doping concentration of the n-blocking layer was varied. Figure 2.37 shows the doping concentration dependence of critical electric field strength (E_{cr}) at various temperatures. This temperature dependence can be fitted by using the following empirical formula where N_d (cm^{-3}) is the doping concentration of the n-blocking layer.

$$E_{cr} = \frac{A}{1 - \frac{1}{4}\log_{10}(N_d/10^{16})} \ \text{MV/cm} \tag{2.20}$$

$$A = 2.653 + 2.222 \times 10^{-6} \cdot T^2 - 1.166 \times 10^{-3} \cdot T \tag{2.21}$$

Here, T is the temperature in Kelvin, and $A = 2.503$ MV/cm at room temperature (298 K). Because impact ionization coefficients had a negative temperature coefficient, the critical electric field strength has increased with the temperature.

Before using this critical electric field strength, however, some important points have to be reminded. Because the critical electric field strength is calculated considering a NPT diode as in the definition, the maximum electric field at breakdown will be different for PT diodes or diodes having a non-uniform doping profile in a voltage blocking layer. Figure 2.38 shows the doping concentration dependence of maximum electric field strength at breakdown for p^+-n-n^+ structure with different voltage-blocking layer thickness. Below the doping concentration of PT, maximum electric field strength at breakdown becomes larger compared with the critical field strength given by the NPT structure. This is because at the same maximum electric field and doping concentration, larger number of avalanche multiplication will occur in NPT structure compared with PT structure because NPT structure has wider depletion layer width where impact ionization occurs. To obtain the same number of avalanche multiplication, PT structure will need larger maximum electric field, which leads to the larger maximum electric field strength at breakdown. Furthermore, not only the difference of NPT and PT, but also conduction type (n- or p-type) of the voltage-blocking layer will change the maximum electric field strength at breakdown, which will be explained in the next section. Therefore, the critical electric field strength shown in equation (2.20) only holds for the p^+n NPT structure, and cannot be used for other structures. This discussion is the same for the other critical field strength reported in the past literatures [1, 5], where the reported equations will only hold for the structure assumed in the calculation or measurement. From the above discussion, the author would like to remind that when designing or characterizing power devices using the critical electric field strength, one must keep in mind the device structure which the critical electric field strength was obtained from.

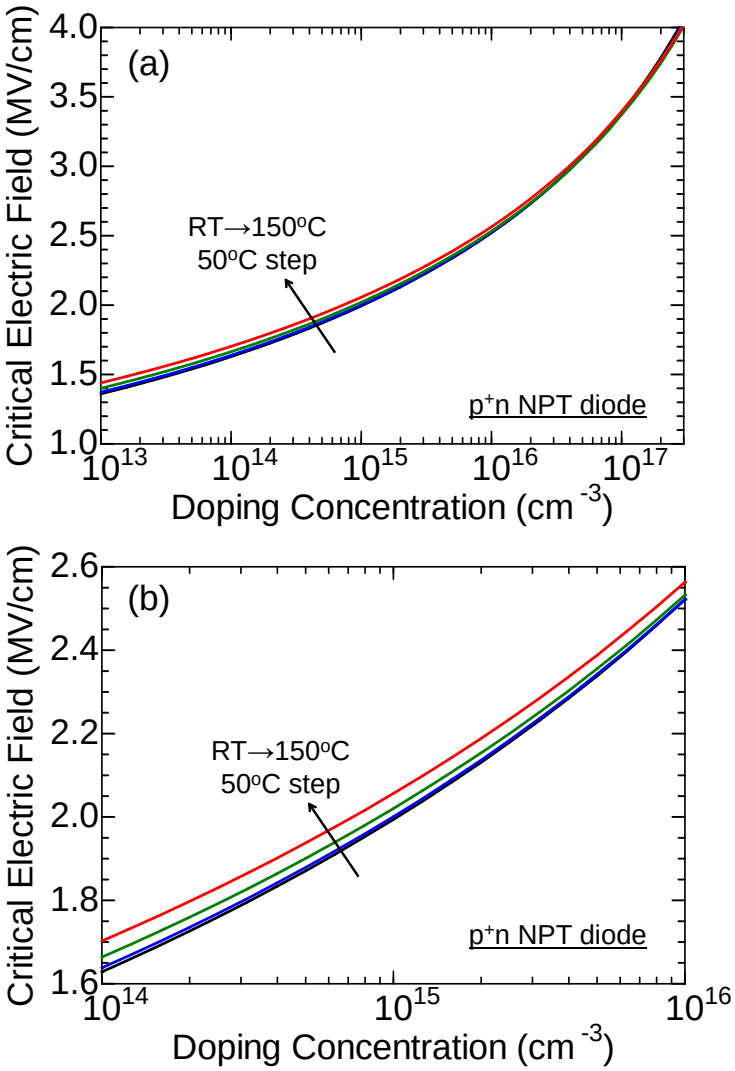


Figure 2.37: (a) Temperature dependence of critical electric field strength calculated for p^+n NPT structures. An enlarged figure is shown in (b).

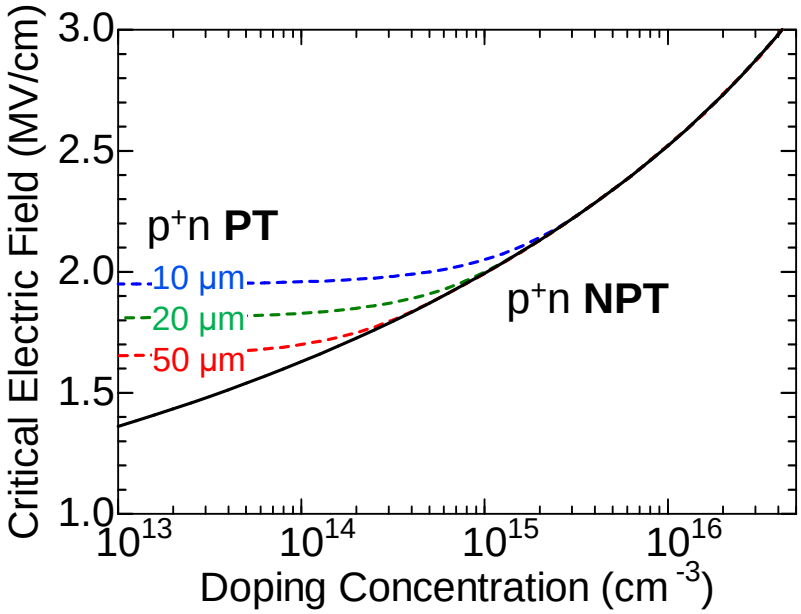


Figure 2.38: Doping concentration dependence of critical electric field for p^+n NPT structure and PT structure with various blocking layer thickness.

2.7.2 Conduction Type Dependence of Ideal Breakdown Voltage

In the previous section, critical electric field strength was calculated for a p^+n NPT structure, in other words, for n-type blocking layer structure. However, there are power devices such as IGBT or GTO which can be fabricated with both n-type and p-type blocking layer structure [20]. For these devices, differences such as ideal breakdown voltage between the conduction type of blocking layer needs to be clarified for the further understanding and improvement of device characteristics. In this study, ideal breakdown voltage was calculated for p^+n and n^+p structure to show the differences occurring by the different conduction type of blocking layer. The origin of the differences occurring between the different conduction type will be discussed, and clarify the superior blocking layer from the point of view of breakdown voltage.

Figure 2.39 shows the doping concentration dependence of ideal breakdown voltage and critical electric field strength for p^+n and n^+p NPT structure, in other words, n-type and p-type blocking layer structure, respectively. For both ideal breakdown voltage and critical electric field strength, n^+p (p-type blocking layer) structure takes a smaller value than that of p^+n (n-type blocking layer) structures. Specifically, n^+p structures have $\sim$9% lower ideal breakdown voltage, and $\sim$5% lower critical electric field strength than p^+n structures. Figure 2.40 shows the doping concentration dependence of ideal breakdown voltage for PiN structure with different i-layer thicknesses. Similar to the result of NPT structure, lower ideal breakdown voltage was obtained when the p-type blocking layer was assumed. However, when the doping concentration is reduced, the difference between the p-type and n-type blocking layers becomes smaller, and at last, the difference disappears.

The origin of this different ideal breakdown voltage between the conduction types of blocking layer is discussed. Figure 2.41 shows a band diagram and an electric field distribution at reverse bias for p^+n and n^+p structures. Here, the direction of carrier multiplication is considered in the following discussion. For p^+n structure, holes are injected from the lower electric field side and are multiplied to the higher electric field side. For electrons, which are injected from the higher electric field side or generate by the hole impact ionization, are multiplied to the direction toward the lower electric field side. On the other hand, for n^+p structure, the direction is completely opposite: Holes are multiplied toward the lower side, and electrons toward the higher side. Therefore, even if the doping concentration of the blocking layer is identical, the process of the carrier multiplication inside the depletion layer is different for these two structures. Because the carrier multiplication is different, the final result of avalanche breakdown voltage is different. Here, if the ionization coefficients of electrons and holes are the same, meaning $\alpha = \beta$, this effect will not occur because the process of the carrier multiplication is the same for the two. For example, when the same calculation is done in GaAs where α and β have very similar values [28], difference of the ideal breakdown voltage between the conduction type of blocking layer does not appear. However, in the c-axis direction of 4H-SiC, α and β exhibit a large difference to each other.

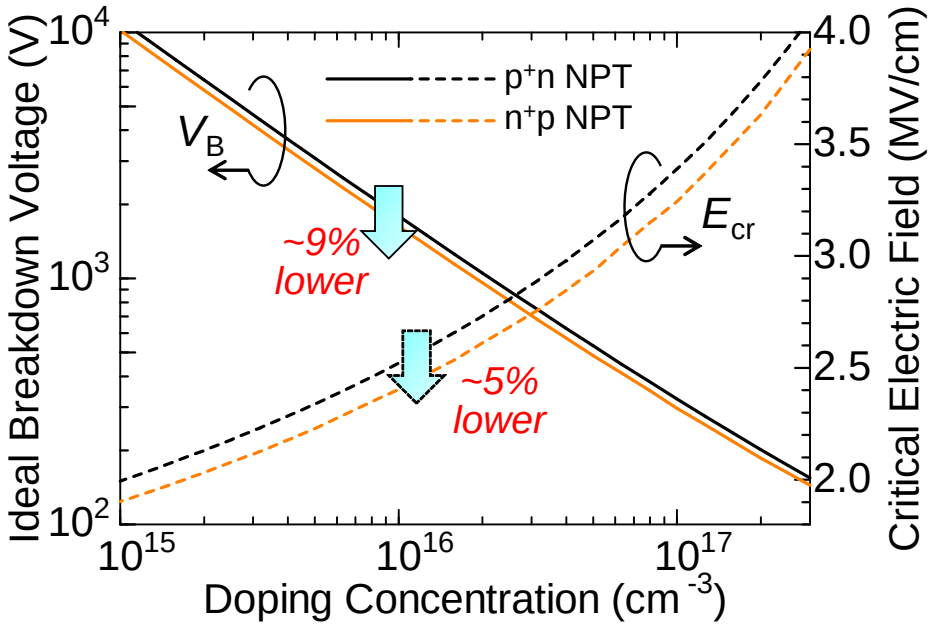


Figure 2.39: Doping concentration dependence of ideal breakdown voltage and critical electric field strength for p^+n (n-type blocking layer) and n^+p (p-type blocking layer) structures.

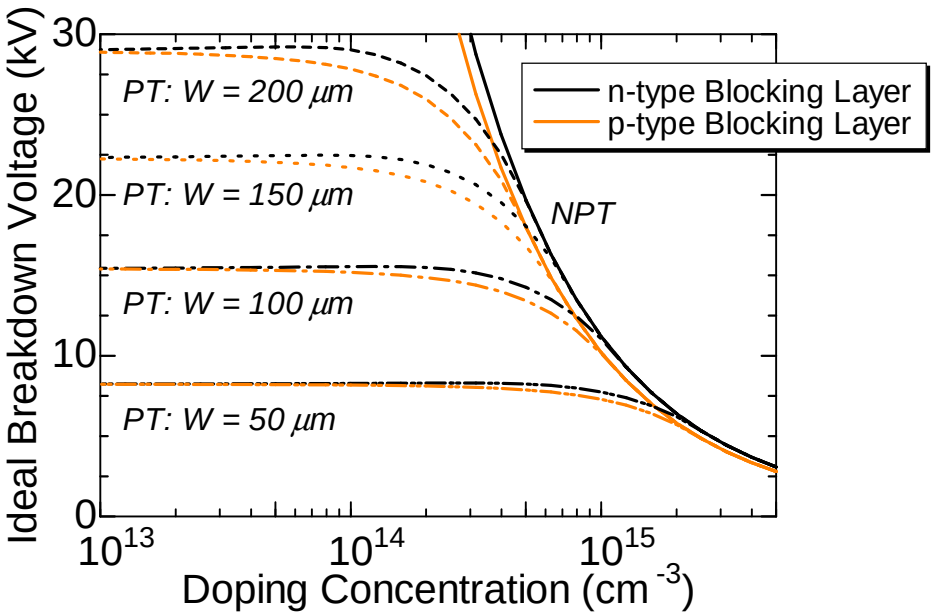


Figure 2.40: Doping concentration dependence of ideal breakdown voltage for PT structure with different blocking layer thickness for n-type and p-type blocking layer.

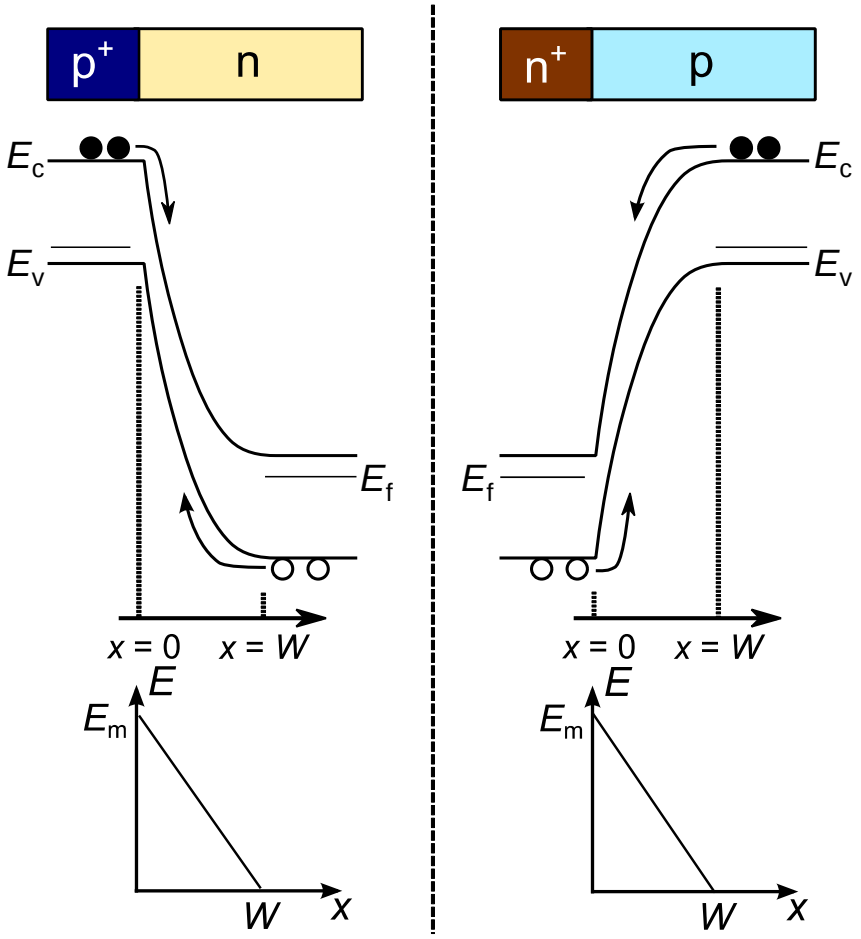


Figure 2.41: Schematic illustration of band diagram and electric field distribution at reverse bias for p^+n and n^+p diodes.

Therefore, from the large difference between the ionization coefficients, it has enhanced the difference between the ideal breakdown voltage as shown in Fig. 2.39.

In the case of PT structure, effect of conduction type difference will vary by the doping concentration and thickness. Figure 2.42 shows two types of electric field distribution for PT structure. When the doping concentration is sufficiently low or the thickness of blocking layer is thin, the electric field distribution inside the depletion layer will be nearly constant as shown in Fig. 2.42(a). In this case, there will be no higher or lower side of the electric field in depletion layer, which results in no difference of ideal breakdown voltage as seen in Fig. 2.40. However, if the doping concentration is not low enough, electric field distribution inside the depletion layer will not be constant as shown in Fig. 2.42(b). In this case, the same effect for NPT structure will occur, which is the lower ideal breakdown voltage for a device with p-type blocking layer.

Especially, this effect must be considered when designing UHV devices with breakdown voltage over 10 kV. Because the doping concentration that can be controlled in epitaxial growth is about 10^{14} cm^{-3} in SiC [42], the blocking layer thickness has to be thicken to achieve a high breakdown voltage. In this case, as shown in Fig. 2.40, the difference of ideal breakdown voltage between the conduction type of blocking layer appears clearly: For a device using a p-type blocking layer, it requires a thicker epilayer compared with a device using an n-type blocking layer. However, the fact that devices using an n-type blocking layer have higher ideal breakdown voltage than devices using a p-type blocking layer is a desirable result. In unipolar devices, the on-resistance relies on thickness of blocking layer and also mobility of the conducting carriers. Because electrons have a higher mobility than holes while a thinner n-type blocking layer is enough to obtain a given breakdown voltage, usage of an n-type blocking layer will be ideal in unipolar devices. On the other hand, in bipolar devices, this fact is also desirable because remarkable carrier lifetime enhancement and control have been achieved on for n-type SiC [43, 44], and a long carrier lifetime over 20 μs has been already realized [45]. A longer carrier lifetime will enhance the conductivity modulation in bipolar devices, leading to a lower on-resistance [46]. Furthermore, when n-channel and p-channel MOSFETs or IGBTs are compared, n-channel devices have lower on-resistance owing to the higher channel mobility for electrons [47].

In summary, due to the large difference between the ionization coefficients of electrons and holes, ideal breakdown voltage exhibits a conduction type dependency of blocking layer: n-type blocking layer structure has a higher breakdown voltage compared with p-type. From this fact, it can be concluded that power devices with an n-type blocking layer will have advantages in both on-resistance and breakdown voltage compared with devices with p-type blocking layer.

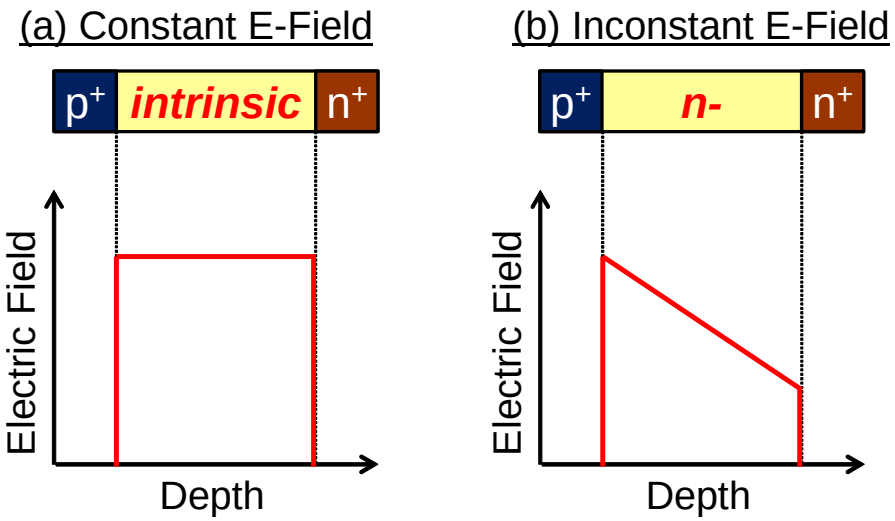


Figure 2.42: Difference of electric field distribution inside the depletion layer for PiN structure with different doping concentration of blocking layer.

2.8 Summary

In this chapter, the impact ionization coefficients of SiC along nearly ⟨0001⟩ were determined in a wide range of electric field of 1–3 MV/cm, and at high temperature up to 150°C. First, a measurement setup of photomultiplication measurement and structures of photodiodes used in this study were explained. Toward the accurate determination of impact ionization coefficients, these measurement setup and photodiode structures were optimized, and by using photodiodes with various multiplication layer structures, ionization coefficients were extracted in a wide range of electric field. Breakdown voltage calculated from the obtained impact ionization coefficients reproduced very well the experimental results, indicating the successful extraction. In this study, accurate measurement of ionization coefficients at high temperature was performed, which showed a negative temperature coefficient of β, and a very small temperature dependence of α. Then using the obtained impact ionization coefficients in this study, temperature dependence of critical electric field strength was calculated and showed an equation to express the temperature dependence for the quick designing of power devices. When an ideal breakdown voltage was calculated for n-type and p-type blocking layer, a difference of breakdown voltage has surprisingly occurred due to the large difference between α and β. From this difference of ideal breakdown voltage, the author would like to suggest that if one is trying to design a power device with a p-type blocking layer, one must be aware that potentially, those devices will have a lower breakdown voltage than a power device with n-type blocking layer.

These results obtained in this study is a basis of designing and analyzing SiC power devices. It will be essential for the further improvement and optimization of device performances. In the future, even more accurate values of impact ionization coefficients in a wider range of electric field and temperature will be important for the further understanding of high-field physics in SiC from an academic viewpoint.

References

[1] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, *Applied Physics Letters* **71**, 90 (1997).

[2] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, *Journal of Electronic Materials* **27**, 335 (1998).

[3] R. Raghunathan and B. J. Baliga, *Proceedings of 9th International Symposium on Power Semiconductor Devices and ICs* (1997) p. 173.

[4] B. K. Ng, J. P. R. David, R. C. Tozer, G. J. Rees, F. Yan, J. H. Zhao, and M. Weiner, *IEEE Transactions on Electron Devices* **50**, 1724 (2003).

[5] T. Hatakeyama, T. Watanabe, T. Shinohe, K. Kojima, K. Arai, and N. Sano, *Applied Physics Letters* **85**, 1380 (2004).

[6] T. Hatakeyama, *physica status solidi (a)* **206**, 2284 (2009).

[7] W. S. Loh, B. K. Ng, J. S. Ng, S. I. Soloviev, H.-Y. Cha, P. M. Sandvik, C. M. Johnson, and J. P. R. David, *IEEE Transactions on Electron Devices* **55**, 1984 (2008).

[8] J. E. Green, W. S. Loh, A. R. J. Marshall, B. K. Ng, R. C. Tozer, J. P. R. David, S. I. Soloviev, and P. M. Sandvik, *IEEE Transactions on Electron Devices* **59**, 1030 (2012).

[9] E. Bellotti, H. E. Nilsson, K. F. Brennan, P. P. Ruden, and R. Trew, *Journal of Applied Physics* **87**, 3864 (2000).

[10] M. Hjelm, H.-E. Nilsson, A. Martinez, K. F. Brennan, and E. Bellotti, *Journal of Applied Physics* **93**, 1099 (2003).

[11] A. Akturk, N. Goldsman, S. Potbhare, and A. Lelis, *Journal of Applied Physics* **105**, 033703 (2009).

[12] R. Raghunathan and B. J. Baliga, *Solid-State Electronics* **43**, 199 (1999).

[13] W. S. Loh, J. P. R. David, B. K. Ng, S. I. Soloviev, P. M. Sandvik, J. S. Ng, and C. M. Johnson, *Materials Science Forum* **615-617**, 311 (2009).

[14] C. Raynaud, D.-M. Nguyen, N. Dheilly, D. Tournier, P. Brosselard, M. Lazar, and D. Planson, *physica status solidi (a)* **206**, 2273 (2009).

[15] K. G. McKay and K. B. McAfee, *Physical Review* **91**, 1079 (1953).

[16] C. A. Lee, R. A. Logan, R. L. Batdorf, J. J. Kleimack, and W. Wiegmann, *Physical Review* **134**, A761 (1964).

[17] G. E. Stillman, C. M. Wolfe, A. G. Foyt, and W. T. Lindley, *Applied Physics Letters* **24**, 8 (1974).

[18] T. P. Pearsall, F. Capasso, R. E. Nahory, M. A. Pollack, and J. R. Chelikowsky, *Solid-State Electronics* **21**, 297 (1978).

[19] H.-Y. Cha and P. M. Sandvik, *Japanese Journal of Applied Physics* **47**, 5423 (2008).

[20] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer, 2008.

[21] E. Degenkolb, K. O. Park, J. B. Shorter, and M. Tabasky, *Journal of The Electrochemical Society* **132**, 2027 (1985).

[22] T. Ono, M. Oda, C. Takahashi, and S. Matsuo, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **4**, 696 (1986).

[23] F. Yan, C. Qin, J. H. Zhao, and M. Weiner, *Materials Science Forum* **389-393**, 1305 (2002).

[24] R. Van Overstraeten and H. De Man, *Solid-State Electronics* **13**, 583 (1970).

[25] W. N. Grant, *Solid-State Electronics* **16**, 1189 (1973).

[26] M. H. Woods, W. C. Johnson, and M. A. Lampert, *Solid-State Electronics* **16**, 381 (1973).

[27] T. Mikawa, S. Kagawa, T. Kaneda, Y. Toyama, and O. Mikami, *Applied Physics Letters* **37**, 387 (1980).

[28] G. E. Bulman, L. W. Cook, and G. E. Stillman, *Solid-State Electronics* **25**, 1189 (1982).

[29] M. Kato, A. Yoshida, and M. Ichimura, *Japanese Journal of Applied Physics* **51**, 02BP12 (2012).

[30] A. G. Chynoweth, *Physical Review* **109**, 1537 (1958).

[31] Y. Okuto and C. Crowell, *Solid-State Electronics* **18**, 161 (1975).

[32] S. Reggiani, E. Gnani, M. Rudan, G. Baccarani, C. Corvasce, D. Barlini, M. Ciappa, W. Fichtner, M. Denison, N. Jensen, G. Groos, and M. Stecher, *IEEE Transactions on Electron Devices* **52**, 2290 (2005).

[33] G. A. Baraff, *Physical Review* **128**, 2507 (1962).

[34] Y. Okuto and C. R. Crowell, *Physical Review B* **6**, 3076 (1972).

[35] K. K. Thornber, *Journal of Applied Physics* **52**, 279 (1981).

[36] T. Lackner, *Solid-State Electronics* **34**, 33 (1991).

[37] N. Kaji, H. Niwa, J. Suda, and T. Kimoto, *IEEE Transactions on Electron Devices* **62**, 374 (2015).

[38] H. Miyake, T. Okuda, H. Niwa, T. Kimoto, and J. Suda, *IEEE Electron Device Letters* **33**, 1598 (2012).

[39] T. Kimoto, N. Miyamoto, and H. Matsunami, *IEEE Transactions on Electron Devices* **46**, 471 (1999).

[40] N. Watanabe, T. Kimoto, and J. Suda, *Japanese Journal of Applied Physics* **53**, 108003 (2014).

[41] C. R. Crowell and S. M. Sze, *Applied Physics Letters* **9**, 242 (1966).

[42] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*, Wiley, 2014.

[43] L. Storasta, H. Tsuchida, T. Miyazawa, and T. Ohshima, *Journal of Applied Physics* **103**, 013705 (2008).

[44] T. Hiyoshi and T. Kimoto, *Applied Physics Express* **2**, 091101 (2009).

[45] S. Ichikawa, K. Kawahara, J. Suda, and T. Kimoto, *Applied Physics Express* **5**, 101301 (2012).

[46] K. Nakayama, A. Tanaka, M. Nishimura, K. Asano, T. Miyazawa, M. Ito, and H. Tsuchida, *IEEE Transactions on Electron Devices* **59**, 895 (2012).

[47] S.-H. Ryu, L. Cheng, S. Dhar, C. Capell, C. Jonas, J. Clayton, M. Donofrio, M. J. O'Loughlin, A. A. Burk, A. K. Agarwal, and J. W. Palmour, *Materials Science Forum* **717-720**, 1135 (2012).

Chapter 3

Fundamental Study on Junction Termination Structures in Ultrahigh-Voltage PiN Diodes

3.1 Introduction

Owing to the superior physical properties SiC has, it is an excellent candidate for the future high-power and high-temperature semiconductor devices. In recent years, several diodes and switches with breakdown voltage greater than 10 kV have been demonstrated [1–7]. However, fundamental studies targeting such high voltage are still needed to understand the basic device physics for realizing high-performance ultrahigh-voltage (UHV) devices. To fully achieve the performance which the material potentially has and to realize ultrahigh breakdown voltage, proper designing of the edge termination to reduce the well-known electric field crowding taking place at the junction edge is important [8]. Among the several edge termination techniques, junction termination extension (JTE) based technologies such as implanted JTE [9–11], mesa-combined JTE [2, 3, 12], and etched JTE [13, 14] have been investigated as promising structures in SiC from its easy design and relatively simple fabrication process. However, a major problem which the conventional single-zone JTE faces is the very narrow window of the JTE dose to obtain high breakdown voltage (optimum JTE-dose window). Because the JTE dose effective for the depletion inside the JTE can easily change by various factors, shooting the very narrow optimum JTE-dose window is a challenge. This makes difficulties in obtaining the expected breakdown voltage with a high yield using a single-zone JTE. Moreover, while JTE is one of the key component technologies to achieve high breakdown voltage, extensive experimental studies of JTE structures in UHV SiC devices are still missing.

In recent years, advanced structures such as space-modulated JTE (SM-JTE) [15], multiple-floating-zone JTE (MFZ-JTE) [16], JTE implementing diffusion of boron [17], and smoothly tapered JTE by gray-scale lithography [18] have been proposed for extension

of the optimum JTE-dose window. Among these JTE structures, SM-JTE, is one of the most promising termination structures with a wide optimum JTE-dose window. Due to its reduced implantation steps without increasing the complexity of fabrication processes, it is an excellent termination structure to fabricate UHV devices. However, the study on this SM-JTE is only based on a numerical device simulation, which makes experimental studies necessary to assure its effect, and consequently, apply it for the fabrication of UHV devices.

In this chapter, UHV SiC PiN diodes with various JTE structures have been fabricated. First, the breakdown characteristics of 10 kV-class PiN diodes have been investigated for various JTE structures, including single-zone JTE, two-zone JTE, and SM-JTE, to clarify the fundamental characteristics of JTEs in UHV devices. The JTE-dose dependence of breakdown voltage was characterized by both experiment and numerical device simulation, which clearly showed a performance limitation factor when using a JTE. Then on the basis of the obtained knowledge from the studies of 10 kV-class PiN diodes, 20 kV-class diodes having SM-JTE have been demonstrated for the first time in SiC to show a guideline for designing junction termination structures of UHV devices.

3.2 Device Structure and Fabrication

In this section, the device structure and the fabrication process of UHV SiC PiN diodes are explained. Technological background and the detail of SM-JTE used in this study are especially explained.

3.2.1 Widening of Optimum Junction Termination Extension (JTE) Dose Window and the Concept of Space-Modulated JTE

In this section, multi-zone JTE, a technique to widen the optimum JTE-dose window, is explained. Then, according to the physics and the fabrication process of multi-zone JTE, the concept and advantages of SM-JTE used in this study are shown.

To widen the optimum JTE-dose window, the most common method is to use a multi-zone JTE [19, 20]. Figure 3.1 shows the schematic structure of a conventional single-zone JTE, two-zone JTE, and multi-zone JTE in a planar PiN diode. In the two-zone JTE, the JTE region is divided into two parts, namely JTE1 and JTE2, where the dose of JTE2 (D_{JTE2}) is smaller than that of JTE1 (D_{JTE1}). Figure 3.2 shows the JTE1-dose ($Q1$ in the figure) dependence of breakdown voltage for a single-zone and two-zone JTE in Si PiN diode summarized from [19]. When the JTE dose is lower than the optimum JTE dose in a single-zone JTE, JTE completely depletes at a relatively low reverse bias voltage and cause electric field crowding at the edge of p^+-anode, which causes premature breakdown. On the other hand, when the JTE is overdosed in a single-zone JTE, JTE does not completely deplete

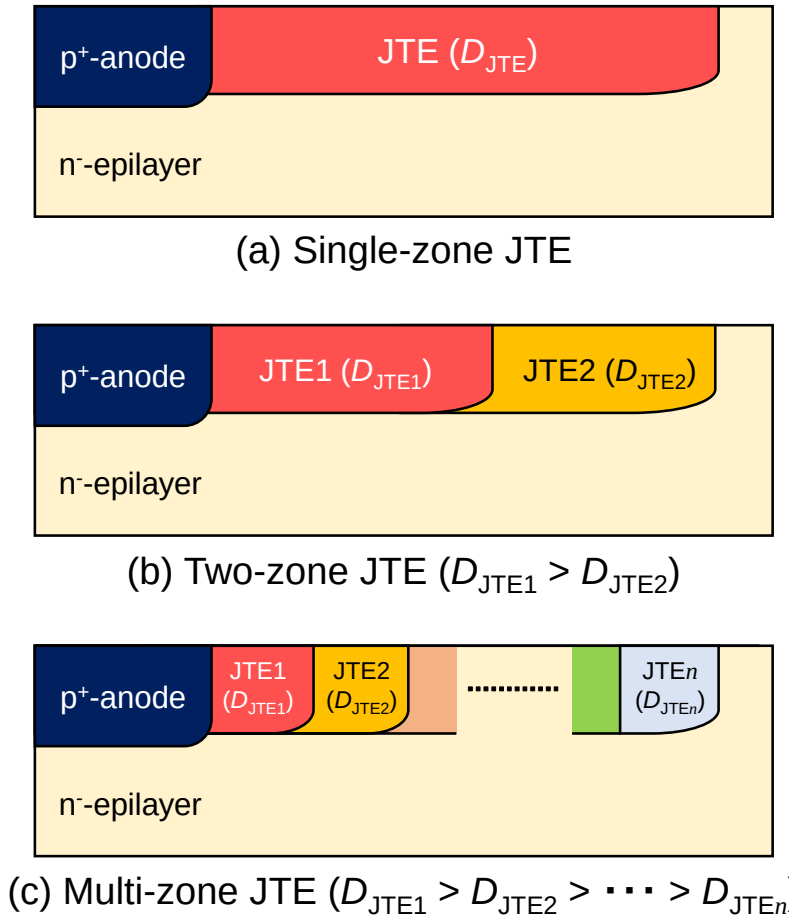


Figure 3.1: Schematic illustration of (a) single-zone JTE, (b) two-zone JTE, and (c) multi-zone JTE.

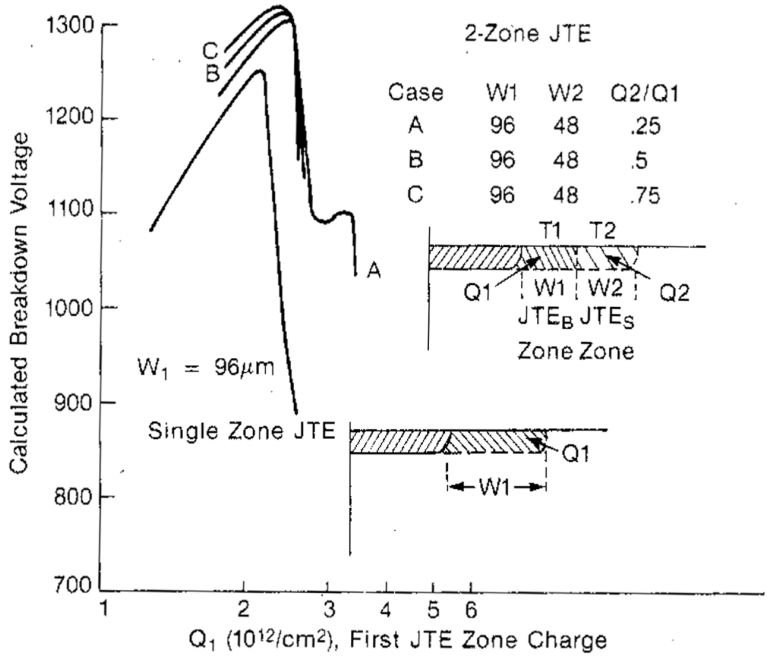


Figure 3.2: Simulated JTE-dose dependence of breakdown voltage for a single-zone and two-zone JTE summarized from [19].

and electric field crowding occurs at the outer edge of JTE, also causing the reduction of breakdown voltage. However, when a two-zone JTE is adopted, the electric field crowding occurring at the outer edge of JTE1 is alleviated by introduction of the outer JTE2, which increases the breakdown voltage. In other words, JTE2 is working as a *"JTE"* of JTE1. Therefore, by increasing the number of zones in JTE (Fig. 3.1 (c), $D_{\mathrm{JTE}n\text{-}1} > D_{\mathrm{JTE}n}$), each of the outer JTE will work as a new JTE for the inner JTE and prevent the premature breakdown. This will lead to the wider optimum JTE-dose window, which is essential for realization of high breakdown voltage with a high yield.

Although the multi-zone JTE is effective for widening the optimum JTE-dose window, it has a large drawback: Increase of the number of JTE zones causes an increase of implantation steps to fabricate it. Because the increase of implantation steps will cause an increase of fabrication cost and complexity in fabrication process, number of implantation steps must be reduced as much as possible. To realize multi-zone JTE in a reduced implantation steps, Feng *et al.* [15] have proposed the Space-Modulated JTE (SM-JTE). Figure 3.3 shows the schematic structure of SM-JTE combined with a single-zone JTE. In SM-JTE, the part of conventional JTE is fragmented into rings and spaces. Because the dose of the rings is relatively low, rings are depleted at reverse bias and the *"effective"* JTE-dose (D_{JTEeff}) can be macroscopically modulated to the ratio of ring width (d_{ring}) and space (d_{space}) which can be expressed as follow:

$$D_{\mathrm{JTEeff}} = D_{\mathrm{JTE}} \cdot \frac{d_{\mathrm{ring}}}{d_{\mathrm{ring}} + d_{\mathrm{space}}}. \tag{3.1}$$

Using this structure, a *quasi*-multi-zone JTE can be fabricated in less ion implantation steps as shown in lower part of Fig. 3.3. This concept of SM-JTE has been introduced by device simulation as shown in Fig. 3.4. Figure 3.4 shows the schematic structures of various JTE structures and its JTE-dose dependence of breakdown voltage for single-zone, two-zone, and single-zone combined with SM-JTE from [15]. By combining the SM-JTE to single-zone JTE, the optimum JTE-dose window has remarkably been widened compared with a conventional single-zone JTE. Moreover, by the optimization of SM-JTE structure, the optimum JTE-dose window becomes even wider than the two-zone JTE which needs two-step implantation.

From Fig. 3.4, it is clear that SM-JTE is an effective junction termination structure for realizing an UHV devices. However, the concept of SM-JTE has been shown only by a numerical device simulation where an ideal case such as complete activation of implanted species is assumed. Therefore, in this study, experimental studies have been done to assure that SM-JTE can actually be used to fabricate UHV devices. At the same time, conventional structures such as single-zone JTE have been employed to UHV devices to study the device physics in such a high voltage-class devices. Moreover, PiN diodes with extremely high breakdown voltage over 20 kV have been demonstrated to show the superior potential of SiC bipolar devices.

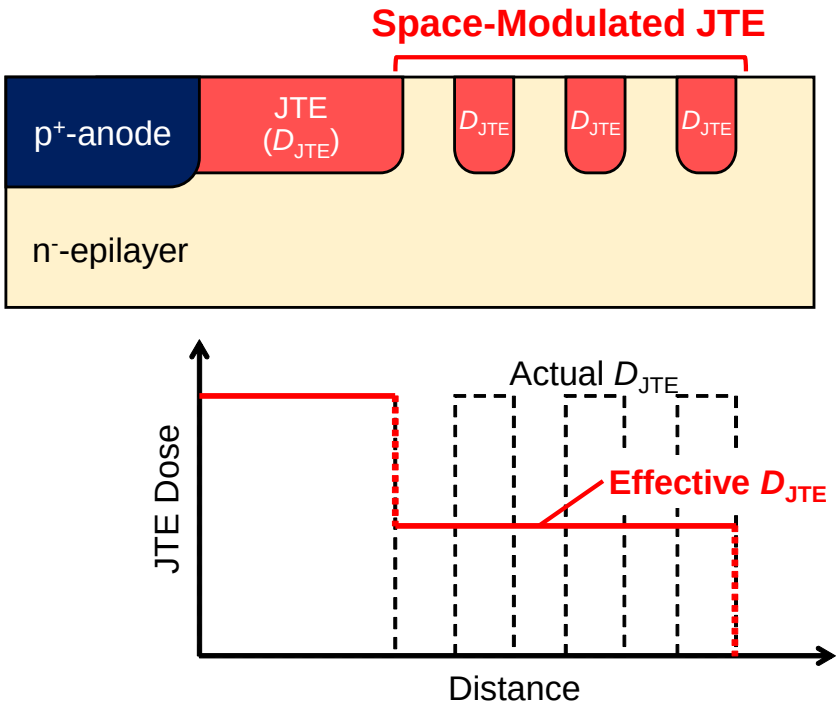


Figure 3.3: Schematic illustration of space-modulated JTE combined with single-zone JTE, together with the concept of *"effective"* JTE dose.

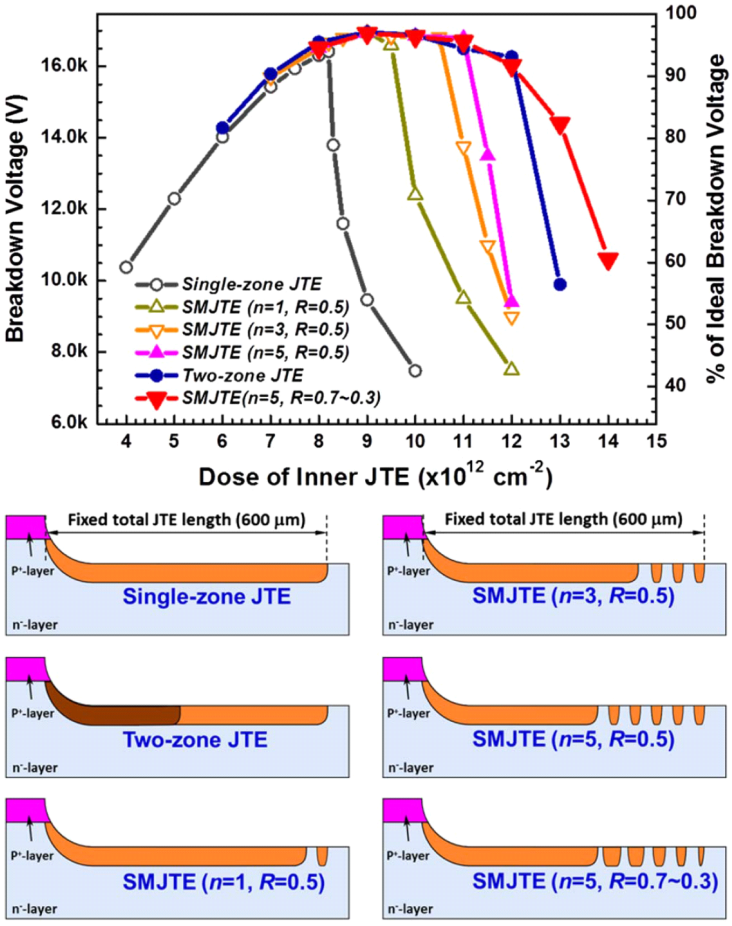


Figure 3.4: JTE-dose dependence of the simulated breakdown voltage for SiC PiN diodes with various JTE structures taken from [15]. The thickness and doping concentration of n^--epilayer used are 120 μm and 1×10^{14} cm^{-3}, respectively. Schematic illustration of each JTE structure is shown at the bottom.

3.2.2 Device Fabrication

In this section, fabrication process of PiN diodes used in this study is explained. The schematic structure of a fabricated SiC PiN diode with implanted two-zone JTE combined with SM-JTE is shown in Fig. 3.5. In this study, two types of voltage-blocking layer were used. For the "type A" epilayer, a 147-μm-thick n-type epilayer doped to 6–7$\times10^{14}$ cm^{-3} was used to realize 10 kV-class devices. On the other hand, for the "type B" epilayer, a 186-μm-thick n-type epilayer doped to 2×10^{14} cm^{-3} was used for the 20 kV-class devices. For both devices, the epilayer was grown on an n$^+$-type 8° off-axis 4H-SiC (0001) substrate.

Figure 3.6 shows the fabrication process of the PiN diode in this study. First, the p$^+$-anode layer was formed on the voltage-blocking layer. For type A epilayer, 0.8-μm-thick p$^+$-anode layer and 0.2-μm-thick p$^+$-contact layer were formed by high-dose Al$^+$ ion implantation at 500°C with a concentration of 2×10^{18} and 2×10^{20} cm^{-3}, respectively. The energies and doses of Al ion implantation are shown in Table 3.1. For type B epilayer, 2.0-μm-thick p$^+$-anode layer and 0.2-μm-thick contact layer were formed by epitaxial growth with concentrations of 5×10^{18} and 1×10^{19} cm^{-3}, respectively. Then, for the device isolation, an improved beveled mesa structure with a mesa height of 1.7 μm (for type A) or 2.6 μm (for type B) and a diameter of 300 μm was fabricated by reactive ion etching with a CF_4-O_2 chemistry using SiO_2 as an etching mask [3]. Improved beveled mesa structure has a rounded corner at the mesa bottom to reduce the electric field crowding occurring at the mesa bottom. The SEM image of the improved mesa structure is shown in Fig. 3.7. This rounded corner can be fabricated by using the isotropically etched SiO_2 mask, which has a rounded corner. Although the anode layer was formed by ion implantation for type A, a mesa structure was adopted here. Because better forward characteristics can be obtained in an epitaxial pn junction [21], the standard edge termination for PiN diode should consider the mesa structure (not planar structure) that is essential in an epitaxial p$^+$-anode. After the mesa fabrication, the JTE region was formed by Al$^+$ ion implantation, conditions of which are shown in Table 3.2, at room temperature with a total implantation dose of 0.5–2.45$\times10^{13}$ cm^{-2} to a depth of 0.8 μm using a SiO_2 mask. Following the implantation, activation annealing was done in Ar ambient at 1700°C for 20 min with a carbon cap [22], where nearly all of the implanted species were activated (>95%) in the JTE region and implanted anode-layer [23]. In addition, due to the extremely low diffusion constants of dopants, implanted profile of Al$^+$ has not changed even after the 1700°C annealing. For the passivation, 30-nm-thick oxides thermally-grown in 10%-diluted N_2O in N_2 at 1300°C for 5 h was employed. Ti/Al/Ni (20/100/80 nm) and Ni (100 nm) annealed at 1000°C for 2 min in Ar ambient were used as ohmic contacts on the anode and cathode, respectively. After the metallization, a 2.5-μm-thick polyimide was coated as an additional passivation layer.

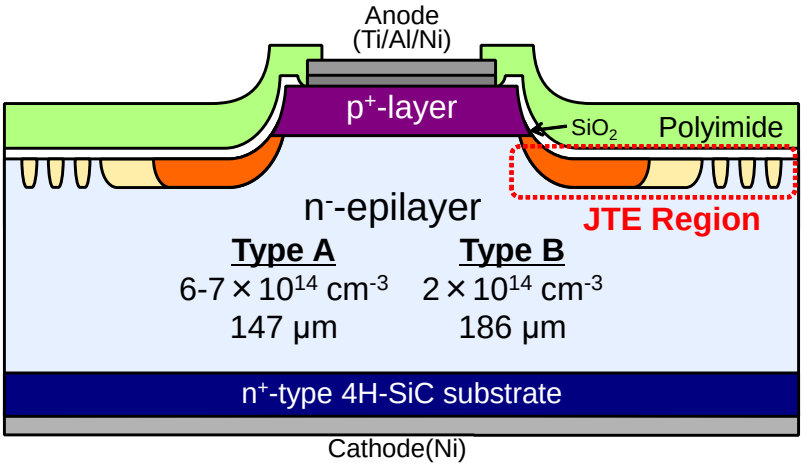
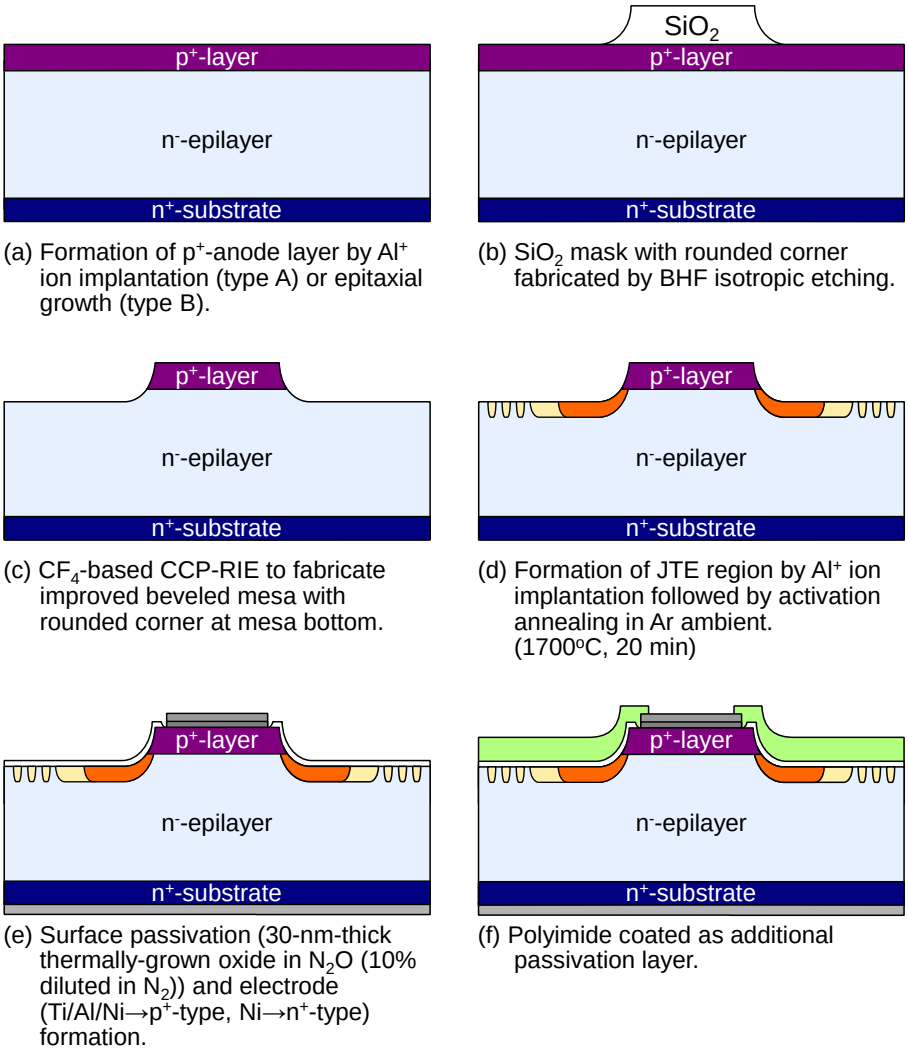


Figure 3.5: Schematic structure of a fabricated SiC PiN diode. Type A epilayer was used to fabricate 10 kV-class diodes, and type B epilayer was used to fabricate 20 kV-class diodes.



(a) Formation of p^+-anode layer by Al^+ ion implantation (type A) or epitaxial growth (type B).

(b) SiO_2 mask with rounded corner fabricated by BHF isotropic etching.

(c) CF_4-based CCP-RIE to fabricate improved beveled mesa with rounded corner at mesa bottom.

(d) Formation of JTE region by Al^+ ion implantation followed by activation annealing in Ar ambient. (1700°C, 20 min)

(e) Surface passivation (30-nm-thick thermally-grown oxide in N_2O (10% diluted in N_2)) and electrode (Ti/Al/Ni→p^+-type, Ni→n^+-type) formation.

(f) Polyimide coated as additional passivation layer.

Figure 3.6: Schematic illustrations of the fabrication process of SiC PiN diodes.

Table 3.1: Implantation energy and dose to form p^+-anode layer.

Energy (keV)	Dose (cm^{-2})	Temperature (°C)
700	3.0×10^{13}	RT
520	2.7×10^{13}	RT
360	2.7×10^{13}	RT
270	1.3×10^{13}	RT
150	1.95×10^{15}	500
100	1.56×10^{15}	500
60	1.14×10^{15}	500
30	7.02×10^{14}	500
20	3.9×10^{14}	500
10	3.9×10^{14}	500

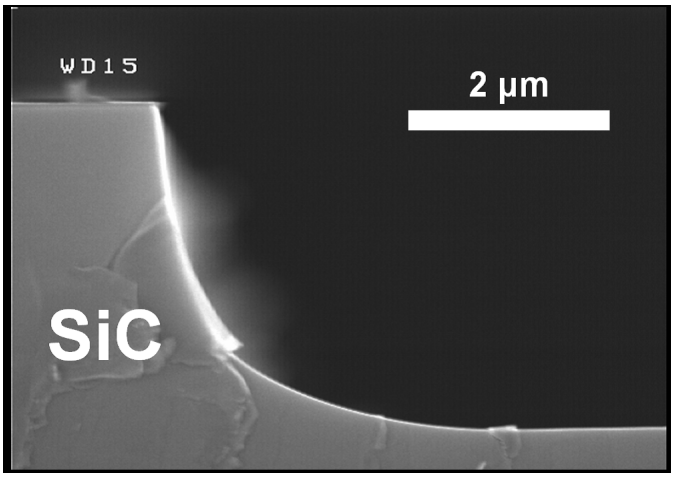


Figure 3.7: SEM image of the improved beveled mesa used in this study.

Table 3.2: Implantation energy and dose to form JTE region with a dose of 1.0×10^{13} cm^{-2}. All of the other doses were scaled equally.

Energy (keV)	Dose (cm^{-2})	Temperature (°C)
700	3.33×10^{12}	RT
450	2.22×10^{12}	RT
280	1.78×10^{12}	RT
170	1.25×10^{12}	RT
100	6.66×10^{11}	RT
55	4.66×10^{11}	RT
25	2.83×10^{11}	RT

3.3 Breakdown Characteristics of 10 kV-class PiN Diodes

In this section, breakdown characteristics of 10 kV-class PiN diodes (type A epilayer) are discussed. The JTE-dose dependence of breakdown voltage for various JTE structures is investigated both experimentally and by numerical device simulation, and by comparing them, importance of additional interface charge is discussed.

3.3.1 JTE Structures Fabricated

JTE structures investigated in this study are shown in Fig. 3.8. In this study, the effect of SM-JTE was evaluated by combining it with the two-zone JTE. For the SM-JTE, a minimum ring/space width of 10 μm was used to exclude the influence of photolithography misalignment. The total JTE length of all the structures was fixed to 500 μm, where the breakdown voltage starts to saturate in numerical device simulation [15], and also in experiment for the breakdown voltage of two-zone JTE as shown in Fig. 3.9. Although the breakdown voltage may not change by further widening of the total JTE length, structures with SM-JTE also have the fixed 500-μm-JTE-length to exclude the effect of breakdown voltage improvement by the widening of JTE-length. In two-zone JTE, the length and the dose ratio of JTE1 and JTE2 were optimized to be 4 : 1 and 3 : 2, respectively by device simulation, and the dose of the rings in SM-JTE was fixed to that of JTE2 to use the same implantation process of the conventional two-zone JTE.

Reverse characteristics of the fabricated diodes were measured in a custom-made ultrahigh-voltage DC measurement system as shown in Fig. 3.10. Here, diodes were immersed in Fluorinert^{TM} during the measurement to avoid the air sparking. When measuring the temperature dependence, the measurement stage was heated up to 120°C in this study.

3.3.2 Blocking Characteristics of 10 kV-class PiN Diodes

Figure 3.11 shows the breakdown voltage experimentally measured as a function of JTE1 dose for various JTE structures. In the single-zone JTE [Fig. 3.8 (a)] shown by triangles, a narrow window of the optimum JTE dose to achieve high breakdown voltage was observed. Due to this narrow window, the tolerance to the deviation of JTE dose is relatively low. This will cause difficulties in shooting the peak point and obtain high breakdown voltage the epilayer potentially has with a high yield. The highest breakdown voltage obtained in this structure was 11.8 kV, only corresponding to about 73% of the parallel-plane breakdown voltage for the epilayer structure ($\sim$ 16 kV), which was calculated by using ionization coefficients obtained in Chapter 2. In the two-zone JTE [Fig. 3.8 (b)] shown by circles, however, the window of the optimum JTE dose is clearly wider compared to the single-zone JTE, realizing a breakdown voltage of 15 kV (power supply limit). This corresponds to

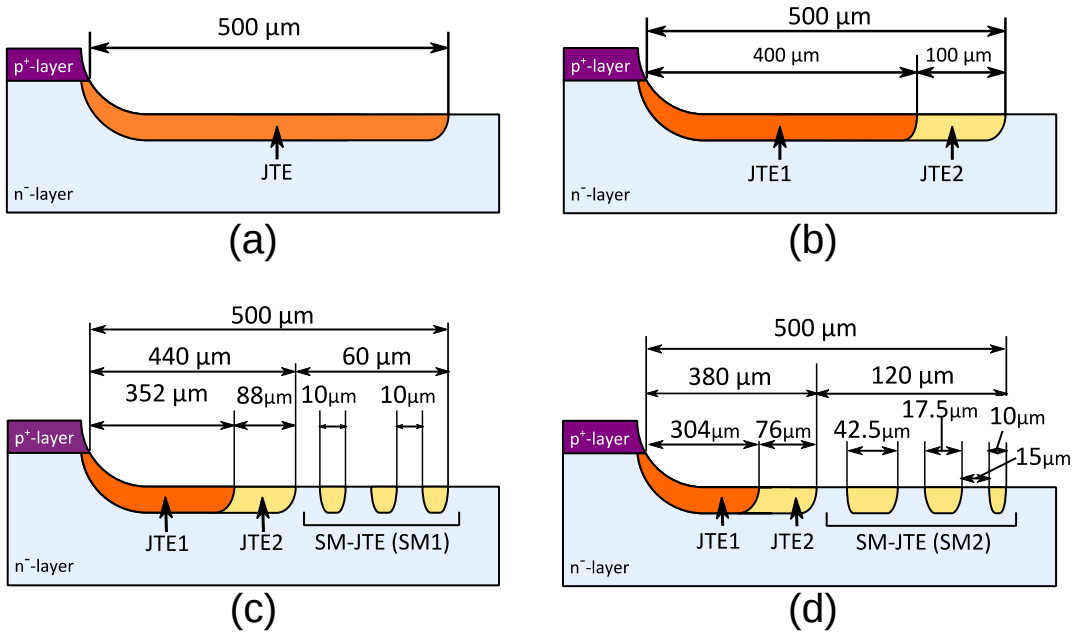


Figure 3.8: JTE structures fabricated in this study. Space-modulated JTEs were combined with the two-zone JTE while fixing the total JTE length to 500 μm, and dose ratio of 3 : 2. (a) Single-zone JTE. (b) Two-zone JTE. (c) Two-zone JTE + SM1. (d) Two-zone JTE + SM2.

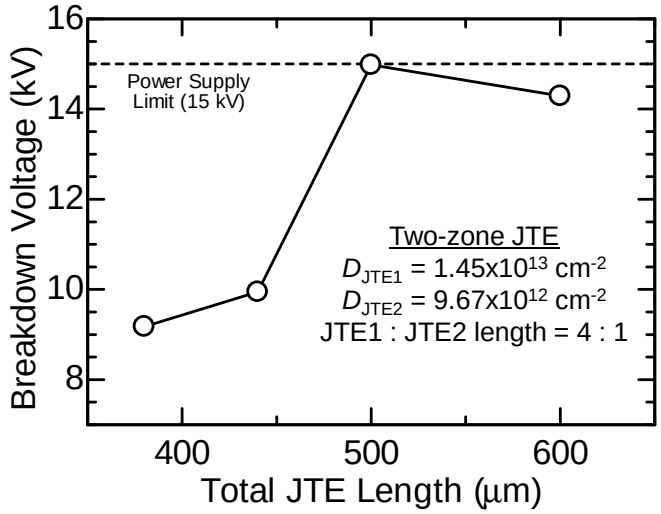


Figure 3.9: Total JTE-length dependence of the breakdown voltage for PiN diodes with two-zone JTE ($D_{\mathrm{JTE1}} = 1.45 \times 10^{13}$ cm^{-2}).

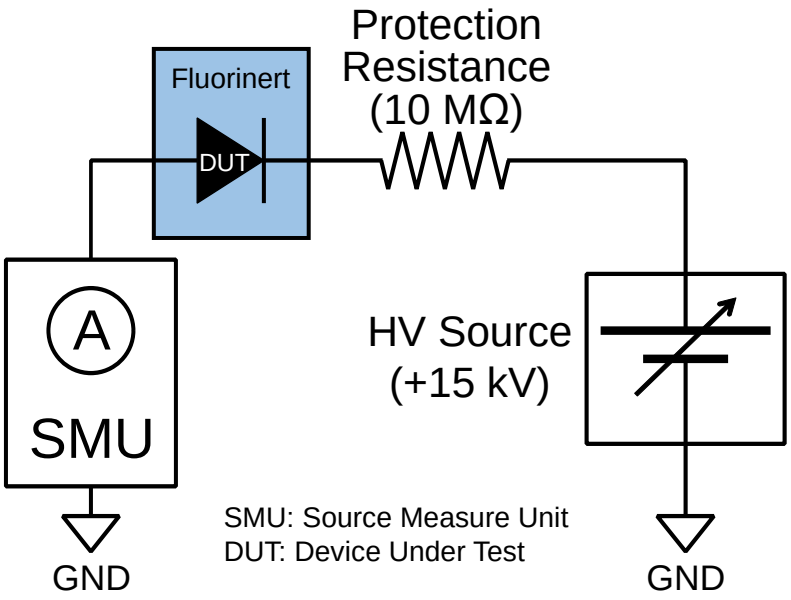


Figure 3.10: Schematic illustration of the custom-made ultrahigh-voltage DC measurement system used in this study.

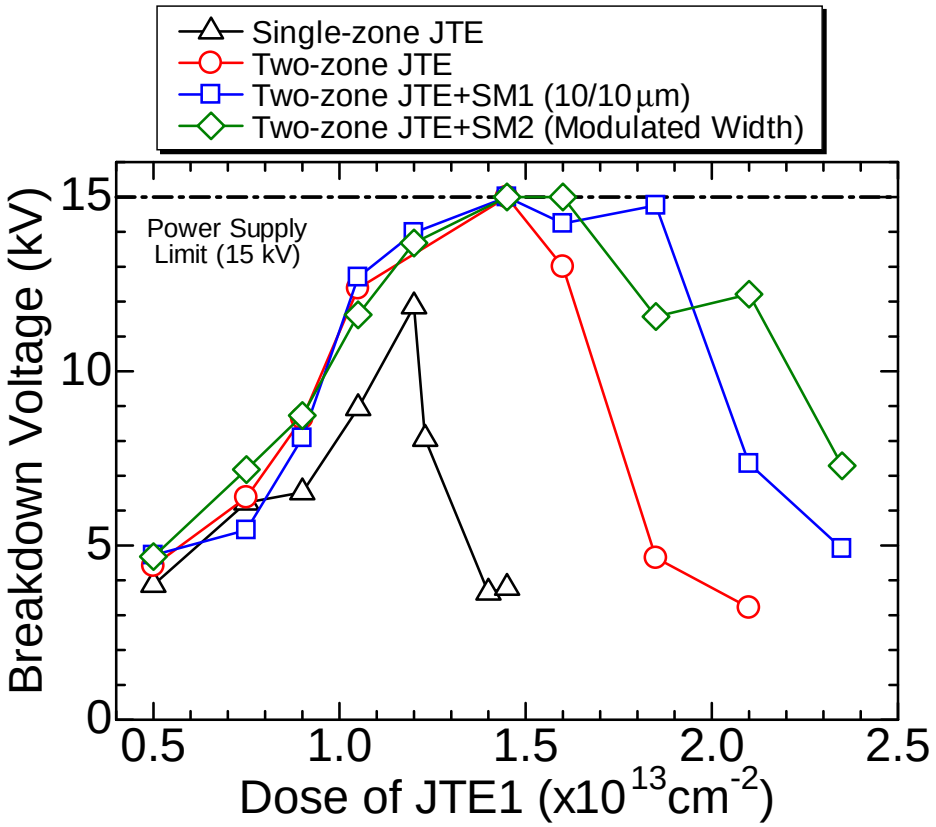


Figure 3.11: Experimental breakdown voltage vs. JTE dose for SiC PiN diodes with single-zone JTE (△), two-zone JTE (◯), and SM-JTE combined to two-zone JTE (□, ◇).

about 93% of the parallel-plane breakdown voltage, which is fairly high for over 10 kV-class SiC diodes. Furthermore, the increase of maximum breakdown voltage also indicates that single-zone JTE cannot sufficiently alleviate the electric field crowding occurring in a device, making single-zone JTE unsuitable for fabricating UHV devices.

First, SM-JTE consisting three sets of 10-μm-wide ring and 10-μm-space [Fig. 3.8 (c): SM1] combined with two-zone JTE was investigated. This SM-JTE structure (SM1) was designed as a JTE region with a smaller *effective* JTE dose than JTE2, making the whole JTE structure as a *quasi*-three-zone JTE. The results are shown by squares in Fig. 3.11. While keeping the maximum breakdown voltage of 15 kV as obtained in the two-zone JTE, the optimum JTE-dose window has extended to the higher JTE-dose region. Although 15 kV is the power supply limit, the real maximum breakdown voltage of the structure should not differ largely by addition of SM-JTE [15]. In the high JTE-dose region, electric field crowding takes place at the outer edge of JTE2 for two-zone JTE because the JTE region does not fully deplete at the high reverse bias voltage. By introducing the SM-JTE at the outer JTE2, electric field crowding is suppressed, which enables the high breakdown voltage and leads to the wide optimum JTE-dose window. Results on SM-JTE with a fixed space width of 15 μm and gradually reduced ring width toward the outer edge [Fig. 3.8 (d): SM2] are shown by rhombuses in Fig. 3.11. In this structure, the effective JTE dose is gradually reduced toward the outer edge. Maximum breakdown voltage of 15 kV and a wider optimum JTE-dose window compared to two-zone JTE were obtained. Although the JTE-dose window for obtaining breakdown voltage greater than 14 kV is narrower than the last SM-JTE structure (SM1), when the targeting breakdown voltage of the device is lower than 11 kV (about 70% of parallel-plane breakdown voltage), this structure is superior to the other structures fabricated in this study from the point of view of tolerance to the deviation of JTE dose.

I–V characteristics of a fabricated 15 kV-class SiC PiN diode with two-zone JTE and SM1 ($D_{\mathrm{JTE1}} = 1.45 \times 10^{13}$ cm^{-2}) are shown in Fig. 3.12. The current density for forward characteristics was calculated using a circular area with the diameter of the mesa. The differential on-resistance and the voltage drop at 100 A/cm^2 are 62 mΩcm^2 and 9.68 V, respectively, which shows a lower on-resistance than a Schottky diode using the same epilayer (about 180 mΩcm^2), indicating the effect of conductivity modulation. However, because this diode is a small device, current spreading may need to be considered which will make the real on-resistance a larger value. These on-resistance and forward voltage drop are relatively high because the p$^+$-anode layer was formed by ion implantation. To improve the forward characteristics, an epitaxial pn junction is essential [21]. For the reverse characteristics, the current density was calculated from the diameter including both mesa and JTE, where a leakage current density below 1×10^{-6} A/cm^2 was obtained even at a reverse bias voltage of -15 kV.

Figure 3.13 shows reverse characteristics at room temperature, 50°C, 80°C, and 120°C of a fabricated SiC PiN diode with two-zone JTE + SM2 at JTE1 dose of 1.2×10^{12} cm^{-2}.

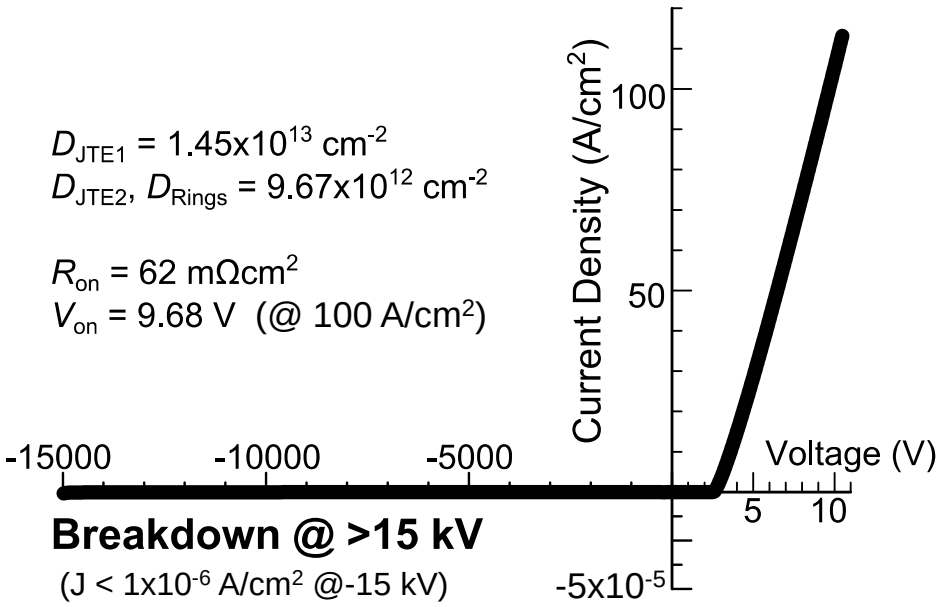


Figure 3.12: *I-V* characteristics of a 15 kV-class SiC PiN diode with two-zone JTE and SM-JTE [Fig. 3.8 (c)].

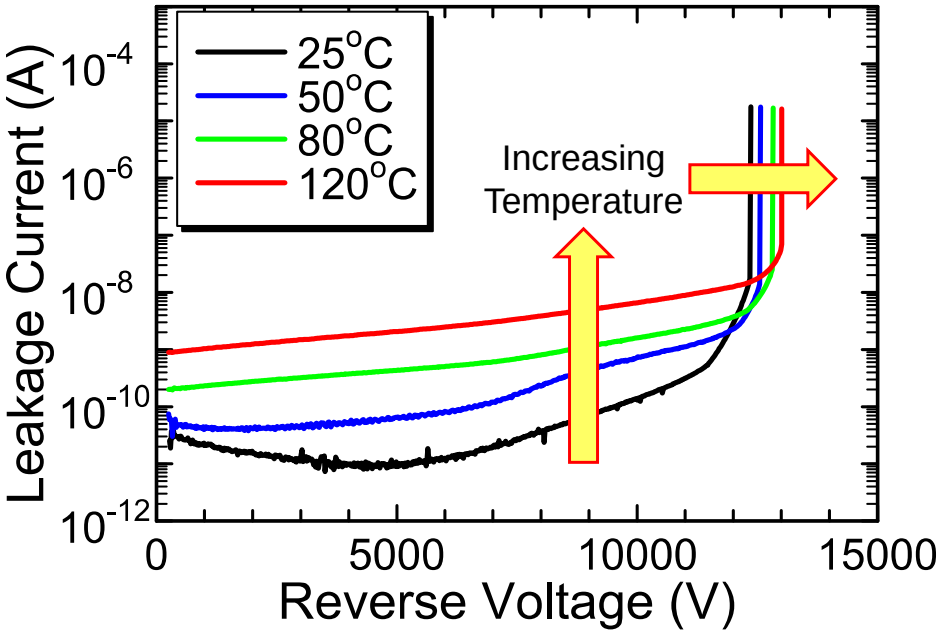


Figure 3.13: Reverse *I-V* characteristics of a PiN diode with two-zone JTE + SM2 ($D_{\mathrm{JTE1}} = 1.2 \times 10^{13}$ cm^{-2}) at room temperature (25°C), 50°C, 80°C, and 120°C.

A clear positive temperature coefficient of leakage current and breakdown voltage can be observed. Although these characteristics were measured in a DC mode, the diode did not show destructive breakdown even after the avalanche multiplication occurred, indicating high ruggedness of the diode. This indicates that electric field crowding is not taking place at a local point, showing that the present JTE structure is successfully relieving the electric field crowding in the diode.

From these results, the effectiveness of SM-JTE for realizing UHV devices has been experimentally demonstrated. Because SM-JTE can be fabricated with the same implantation steps of two-zone JTE, it can be easily adopted in the fabrication process of UHV devices. Further optimization of SM-JTE toward the widening of optimum JTE-dose window will be discussed in the following Sections.

3.3.3 Discussion: Influence of Interface Charges

In this section, the obtained JTE-dose dependence of breakdown voltage for single-zone JTE is investigated using a numerical device simulation. Here, single-zone JTE is used because of its simple structure and the easiness to clarify where the electric field crowding is taking place, making it suitable for discussion of the physics in a JTE structure.

Experimental and simulated JTE-dose dependences of breakdown voltage for the single-zone JTE structure are shown in Fig. 3.14. The numerical device simulation was performed by using DESSIS by Synopsys^{TM} TCAD, and the breakdown voltage was defined as the voltage when the calculated ionization integral approached unity. During the calculation, impact ionization coefficients obtained by Konstantinov *et al.* [24] was used. Although ionization coefficients by Konstantinov may cause inaccuracies in the calculated breakdown voltage, the tendency of JTE-dose dependence of breakdown voltage should not change. Moreover, the difference between the calculated breakdown voltage using ionization coefficients by Konstantinov and those obtained in this study is rather small ($\sim$ 1 kV) compared with the ideal breakdown voltage ($\sim$ 16 kV). The closed circles show the simulated results, where a highest breakdown voltage obtained was 13.1 kV at a dose of 9.95×10^{12} cm^{-2}, which is a slightly higher than the experimental results (11.8 kV). Compared with the simulation, the experimental results of the dose dependence showed a shift of 2×10^{12} cm^{-2} toward the heavier dose. Because the JTE-dose dependence of breakdown voltage is similar for all of the JTE structures in this study when a JTE dose is lower than the optimum JTE dose as shown in Fig. 3.11, this positive shift has occurred in all of the JTE structures. To understand the device physics occurring here, the origin of this positive shift is discussed.

First, the factor that can be considered immediately for this positive shift is the incomplete activation of implanted species. When the implanted species are not completely activated, the effective JTE-dose would be smaller than the implanted dose, causing a positive shift of experiment compared with the ideal case. However, the activation annealing condition used in this study can nearly activate the implanted species completely

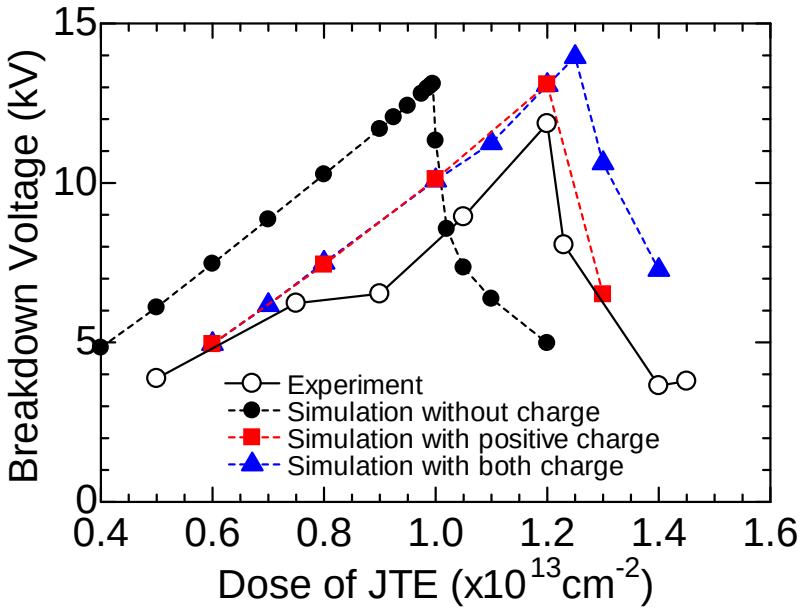


Figure 3.14: Experimental and simulated JTE dose dependence of breakdown voltage of PiN diodes with single-zone JTE. Positive charge ($+2\times10^{12}$ cm^{-2}) at the SiO_2/p-SiC interface, and/or negative charge (-1.4×10^{12} cm^{-2}) at the SiO_2/n-SiC interface were assumed in the simulation.

(>95%) [23]. Even assuming a 90% activation ratio still cannot explain the large shift of 2×10^{12} cm^{-2} observed in this study, making incomplete activation of implanted species to be excluded here.

Therefore, to explain this large shift, effects of the charges at the SiO_2/SiC interface were considered. At the SiO_2/p-SiC (JTE region) interface, there exists a positive charge of about 2×10^{12} cm^{-2} caused by holes trapped at the energetically deep interface states and the fixed oxide charge in this oxide formation process [25]. Simulation results of JTE-dose dependence taking account of the positive charge between the SiO_2/p-SiC interface are shown in closed squares in Fig. 3.14. Compared with the simulation without the interface charge, a positive shift of JTE-dose dependence was observed. The effect of positive charges can be explained using Fig. 3.15. When positive charge exist at the SiO_2/p-SiC interface, the negative charge of the ionized acceptors inside the JTE region is partly compensated. This will cause reduction of the ionized acceptors effective for depletion of JTE, in other words, reduction of *effective* JTE dose. Reduction of effective JTE dose means the shift of JTE-dose dependence toward the heavier dose in experimental breakdown voltage. This result also agrees with the simulation in [26] where the optimum JTE dose increases with positive oxide charge.

In addition to the positive charges at SiO_2/p-SiC interface, there is a fact that at the SiO_2/n-SiC (voltage-blocking layer) interface, there exists negative interface charge of -1.4×10^{12} cm^{-2} in this oxide formation process [27]. Simulation results of JTE-dose dependence considering both negative and positive interface charges are shown in closed triangles in Fig. 3.14. By introducing the negative charges at SiO_2/n-SiC interface, breakdown voltage for a JTE dose higher than the optimum JTE dose has increased. This effect can be explained using Fig. 3.16. When negative charge exist at the SiO_2/n-SiC interface, they will compensate the ionized donors near the surface of the epilayer and enhance the formation of depletion layer near the SiO_2/n-SiC interface as shown in Fig. 3.16 (a). This broadens the depletion layer near the outer edge of JTE, which will reduce the electric field near the JTE edge. Figure 3.16 (b) shows the electric field distribution along horizontal and vertical directions at the outer edge of JTE. In particular, electric field along the horizontal direction has decreased by the existence of negative charge, which results in the improvement of breakdown voltage. Since this decrease of electric field at the outer edge of JTE does not affect the breakdown voltage when electric field crowding takes place at the inner JTE or at the mesa edge, the increase of the breakdown voltage will occur only when the electric field crowding takes place at the outer JTE, which is the case when the JTE dose is larger than the optimum JTE dose.

In this section, it was shown that breakdown characteristics of SiC PiN diodes were severely affected by the charge near the SiO_2/SiC interface. Because the interface charge density will vary by the passivation or process conditions and may change by the operating temperature, these effects must be carefully taken into account when designing a JTE structure. Therefore, to tolerate the impact of interface charge, a JTE structure with a

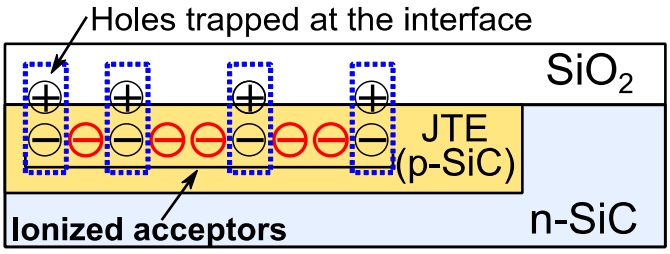


Figure 3.15: Schematic illustration of the effect of positive charge near the SiO_2/p-SiC interface.

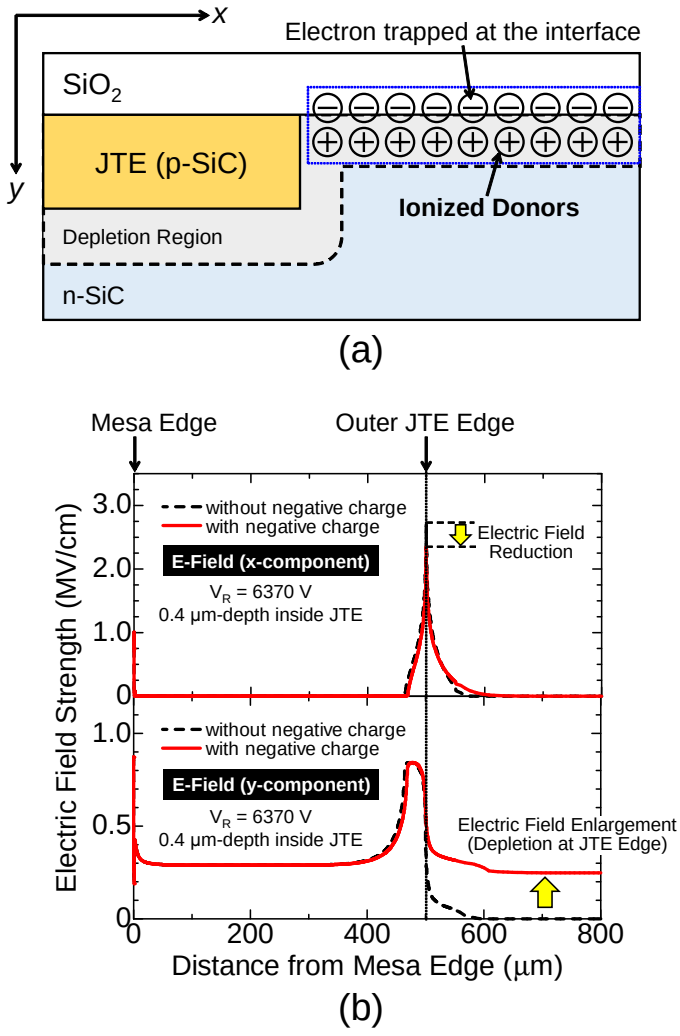


Figure 3.16: (a) Schematic illustration of the effect of negative charge near the SiO_2/n-SiC interface. (b) Simulated electric field distribution at 0.4-μm-depth inside the JTE for single-zone JTE with and without the negative charge near SiO_2/n-SiC interface. The reverse bias voltage is 6370 V, which is the breakdown voltage for a single-zone JTE without negative charge. Here, $x-$ and $y-$ direction are shown in (a).

wide optimum JTE-dose window is important to fabricate UHV devices.

3.4 Demonstration of 20 kV-class SiC PiN Diodes

In the previous section, the effect of interface charge near the SiO_2/SiC interface and the importance of JTE structure for fabricating UHV devices were shown. In this section, for the fabrication of 20 kV-class SiC PiN diode (type B), two-zone JTE and SM-JTE combined to it was modified to realize a JTE structure with a wide optimum JTE-dose window.

3.4.1 Device Simulation of JTE Structure: Space-Modulated Two-Zone JTE

Toward further widening of optimum JTE-dose window, 20 kV-class PiN diodes were fabricated using an improved JTE structure. Figure 3.17 shows the schematic structure of the space-modulated two-zone JTE (SM-two-zone JTE) and its effective JTE-dose distribution. To realize the tapered distribution of the effective JTE dose, SM-JTE was combined to the both JTE1 and JTE2. In the SM-JTE, the ratio of d_{ring} and d_{space} was decreased toward the outer JTE as (d_{space}, d_{ring}) = (10.5, 24.5), (17.5, 17.5), (24.5, 10.5) (in μm).

Figure 3.18 shows the simulated JTE1-dose dependence of breakdown voltage for PiN diode (type B epilayer) with SM-two-zone JTE. In this simulation, the ratio of the JTE dose in JTE1 and JTE2 for two-zone JTE were fixed to 3 : 2. Interface charge was not considered here for the observation of true characteristics of the JTE structure itself. In Fig. 3.18, results of PiN diodes with a conventional two-zone JTE are shown by closed circles. A maximum breakdown voltage of 26.4 kV was obtained, which approaches to the ideal breakdown voltage of 27 kV calculated from the epilayer structure. By combining SM-JTE to the outer JTE2 (SM2), the optimum JTE-dose window to obtain breakdown voltage over 20 kV has widened (closed triangle) while keeping the maximum breakdown voltage obtained in two-zone JTE. Addition of SM2 will decrease the electric field crowding taking place at the outer JTE2 in two-zone JTE, resulting in the increase of breakdown voltage in the dose region greater than the optimum JTE-dose. Results of SM-JTE combined to both JTE edges in two-zone JTE are shown by closed squares. By addition of SM-JTE to the outer JTE1 (SM1), the field crowding is further alleviated, increasing the breakdown voltage in the dose region of 1.2–1.5$\times 10^{13}$ cm^{-2}.

Figure 3.19 shows the electric field distribution at the place of field crowding occurring for various JTE doses. With the increase of JTE dose, the position of electric field crowding taking place has moved from the mesa edge to the outer edge of SM2. Figure 3.20 shows the electric field profile inside the JTE at 0.8-μm-depth for two-zone JTE and SM-two-zone JTE with both SM1 and SM2. At a JTE1 dose of 1.3$\times 10^{13}$ cm^{-2}, breakdown voltage for two-zone JTE is 16 kV, and the maximum electric field is 2.4 MV/cm. However, in the SM-two-zone JTE, electric field is distributed to each of the rings, and the maximum electric

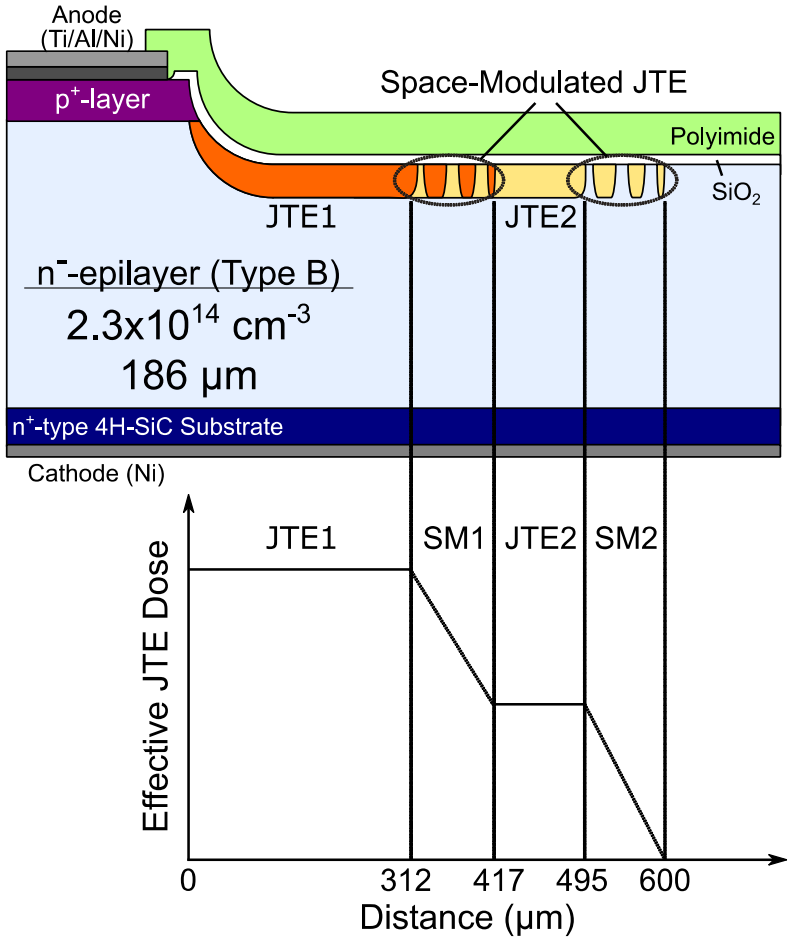


Figure 3.17: Schematic illustration of a fabricated SiC PiN diode with space-modulated two-zone JTE and its effective JTE-dose distribution.

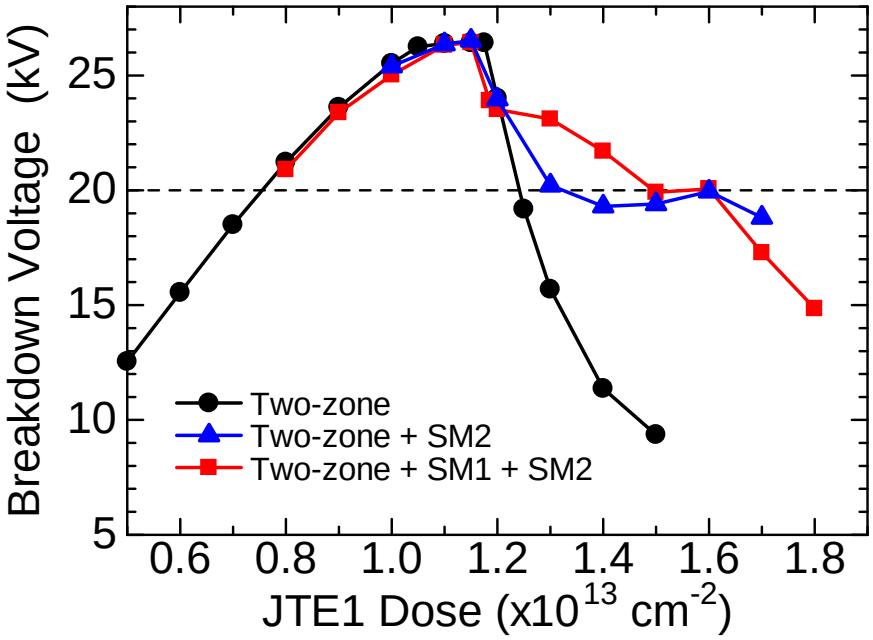


Figure 3.18: Simulated JTE1-dose dependence of breakdown voltage for PiN diode for two-zone JTE, two-zone JTE combined with SM2, and two-zone JTE combined with SM1 and SM2 (SM-two-zone JTE).

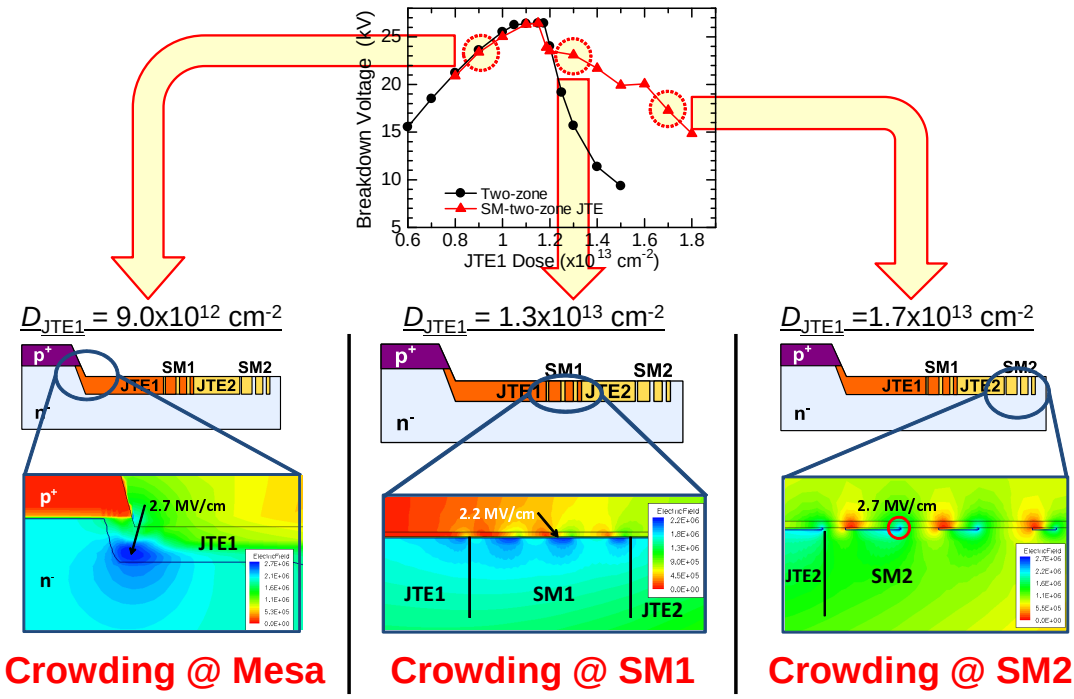


Figure 3.19: Electric field distribution in the region of electric field crowding occurring for various JTE doses at breakdown voltage.

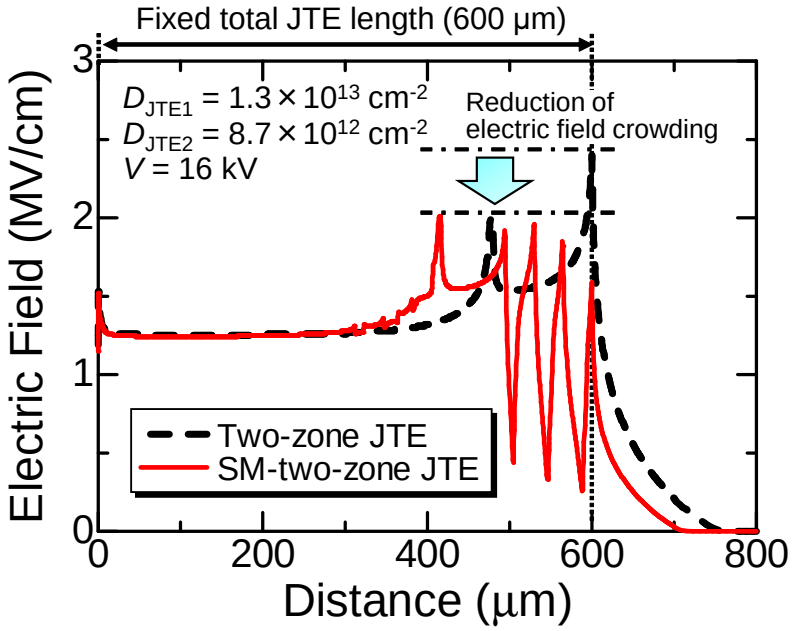


Figure 3.20: Electric field profile inside the JTE at 0.8-μm-depth for two-zone JTE and SM-two-zone JTE at a reverse bias voltage of 16 kV, which is the breakdown voltage for two-zone JTE.

field is lower than 2.0 MV/cm at this voltage. Note that the electric field strength inside the fragmented rings is not zero, indicating that the floating rings are depleted at high reverse bias voltage.

Figure 3.21 shows the JTE1-dose dependence of breakdown voltage for SM-two-zone JTE taking account of the interface charge. Here, positive charge ($+2 \times 10^{12}$ cm^{-2}) at the SiO_2/p-SiC interface and negative charge (-1.4×10^{12} cm^{-2}) at the SiO_2/n-SiC interface were assumed. By the positive charges, the whole JTE-dose dependence has shifted to the higher JTE-dose region. On the other hand, due to the negative charge, breakdown voltage especially at high JTE1 dose has increased due to the reduction of electric field along the horizontal direction.

3.4.2 Blocking Characteristics of 20 kV-class PiN Diodes

Figure 3.22 shows the experimental results of JTE1-dose dependence of breakdown voltage for SM-two-zone JTE and two-zone JTE, together with the simulation result of SM-two-zone JTE taking account of the interface charge. For the experimental results of SM-two-zone JTE and two-zone JTE, the obtained breakdown voltage did not changed up to 1.3×10^{13} cm^{-2}, because the electric field crowding occurs at the inner JTE1 or mesa edge. Here, breakdown voltage is relatively small compared with the simulation. This reason is not clear, but because this degradation is observed in both of the JTE structures, some problem may have occurred in the mesa fabrication process. Further studies will be needed to clarify this reason.

Although breakdown voltage did not change in the low JTE-dose region, at a JTE1 dose of 1.6×10^{13} cm^{-2}, a large difference between them has appeared. For the two-zone JTE, it only endured a reverse bias voltage of 8.6 kV. However, by using the SM-two-zone JTE, the author has achieved a record breakdown voltage of 21.7 kV. This large difference between them clearly show the effect of optimum JTE-dose widening in SM-two-zone JTE. This high breakdown voltage of 21.7 kV was the highest value among any solid-state devices at the time. Also, this breakdown voltage corresponds to nearly 80% of the parallel-plane breakdown voltage ($\sim$ 27 kV), which is relatively high in this UHV region. Figure 3.23 shows the I–V characteristics of a fabricated 20 kV-class SiC PiN diode. Here, the active area was assumed to be the mesa size ($\phi = 300$ μm) for the forward characteristics, and the whole area including mesa and JTE region ($\phi = 1500$ μm) for the reverse characteristics. For the forward characteristics, the differential on-resistance and the voltage drop at 100 A/cm^2 was 34.9 mΩcm^2 and 7.86 V, respectively. Differential on-resistance of a Schottky barrier diode using this epilayer was 529 mΩcm^2, indicating the effectiveness of the conductivity modulation. This value can further be improved by the deep-level-reduction-process [28] implementing thermal oxidation [29] or carbon implantation [30] to increase the carrier lifetime of the epilayer. For the leakage current, very low current density of $<1\times10^{-5}$ A/cm^2 was obtained even at reverse bias voltage of 20 kV.

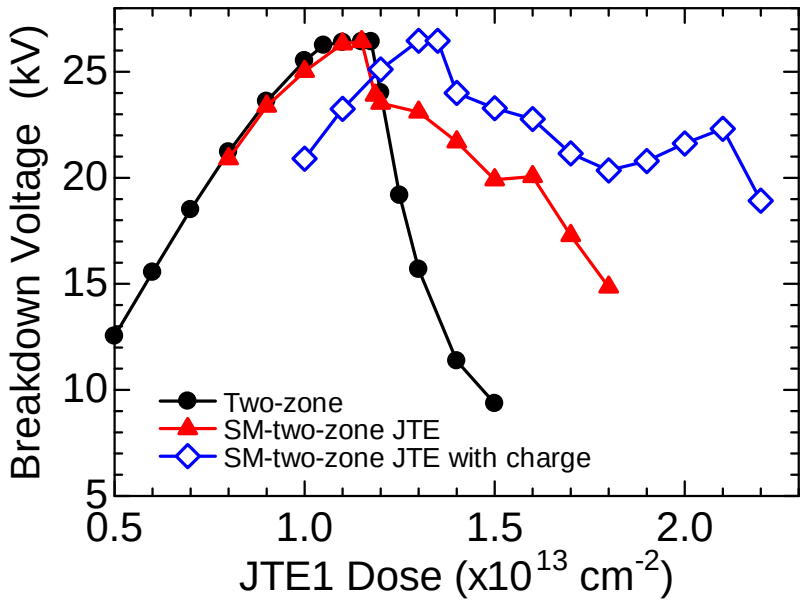


Figure 3.21: JTE1-dose dependence of breakdown voltage for SM-two-zone JTE taking account of the interface charge. Positive charge ($+2\times10^{12}$ cm^{-2}) at the SiO_2/p-SiC interface, and/or negative charge (-1.4×10^{12} cm^{-2}) at the SiO_2/n-SiC interface were assumed in the simulation.

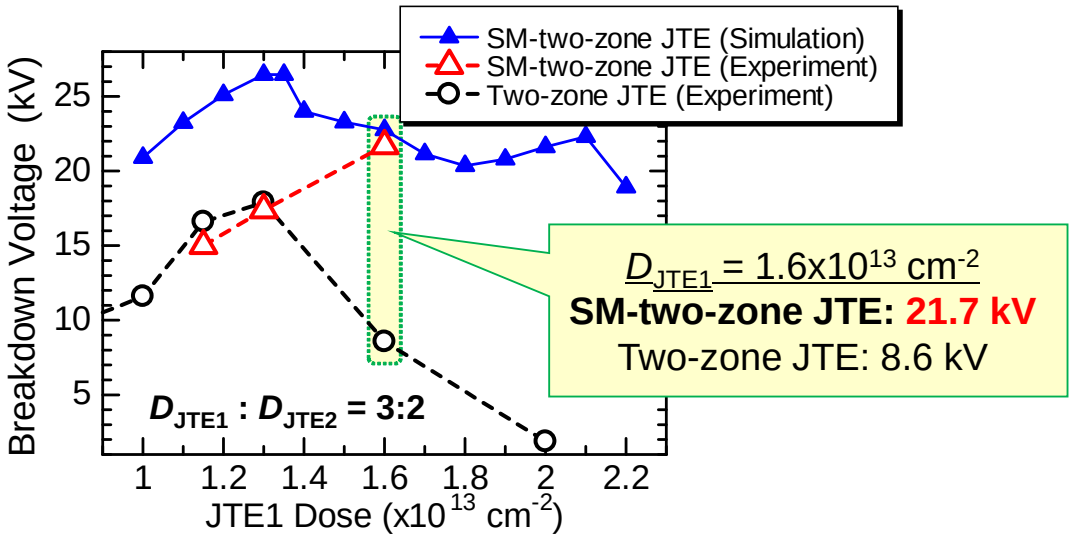


Figure 3.22: Experimental JTE1-dose dependence of breakdown voltage for SM-two-zone JTE and two-zone JTE, together with the simulation result of SM-two-zone JTE taking account of the interface charge.

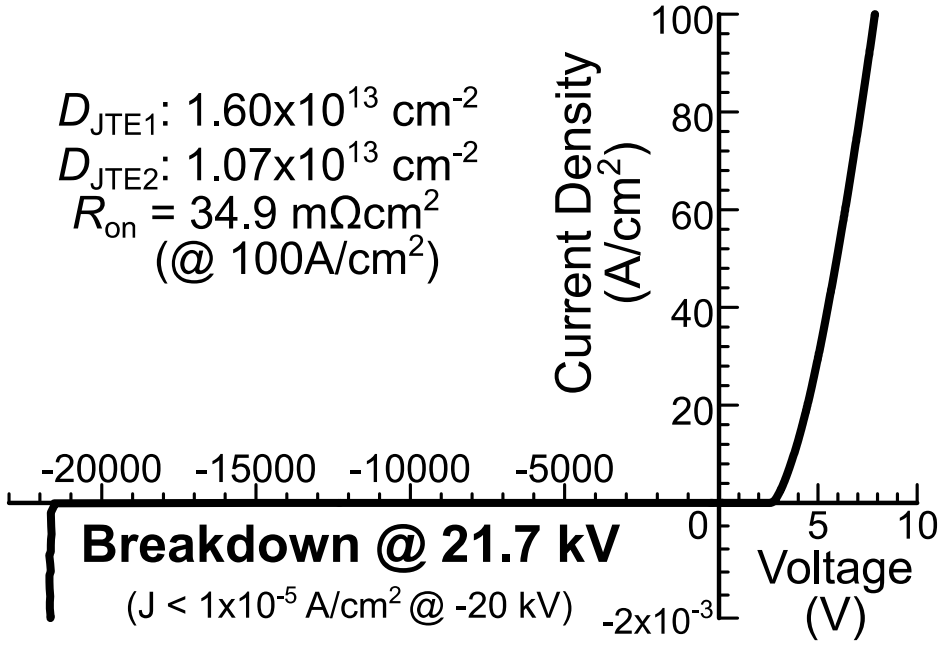


Figure 3.23: *I-V* characteristics of a fabricated 21.7 kV SiC PiN diode.

The temperature dependence (25–120°C) of the leakage current as a function of reverse bias voltage up to 15 kV for a 20 kV-class PiN diode is shown in Fig. 3.24. Here, the temperature dependence was obtained only up to 15 kV due to the limitation of measurement setup. A clear positive temperature coefficient of the leakage current can be observed. Even at 120°C, the leakage current is still below 10^{-5} A/cm^2 at a reverse bias voltage of 15 kV.

3.5 Improvement of Space-Modulated JTE

By using SM-JTE combined with the two-zone JTE, a PiN diode with an ultrahigh breakdown voltage of 21.7 kV has been demonstrated. However, a large breakdown voltage reduction compared with the simulation was observed in the low JTE-dose region where electric field crowding occurs at the mesa edge. This reduction will not occur in every mesa PiN diode (actually, not occurring at 10 kV-class PiN diodes in this study), but to exclude this effect, the region of the electric field crowding should be separated from the mesa edge by controlling the JTE dose. To control the electric field crowding region while maintaining the high breakdown voltage, a wider optimum JTE-dose window is required and the structure of SM-JTE should be further optimized. Moreover, although SM-two-zone JTE has wide optimum JTE-dose window for breakdown voltage over 20 kV, its window is not as wide if the targeted breakdown voltage is higher such as 23 kV. In this section, further improvement procedure of SM-JTE is discussed, where the goal is to realize ultrahigh-breakdown voltage in a wide range of JTE dose.

From Section 3.2, it was shown that the ideal JTE structure can be obtained by increasing the number of zones in multi-zone JTE. The extreme of the multi-zone JTE will be the continuously reduced JTE dose toward the outer edge, which is the case in VLD (Variation of Lateral Doping) structures used in Si devices [31]. However, VLD-structure uses diffusion of implanted dopants, which is difficult in the case of SiC where the diffusion coefficients for most of the dopants are extremely small [32]. Therefore, to realize the VLD-like dopant profile, SM-JTE structure shown in Fig. 3.25 is proposed. In this structure, while keeping the $d_{\mathrm{ring}} + d_{\mathrm{space}}$ constant to 50 μm, effective JTE dose was almost linearly decreased to the outer edge of JTE as shown in Fig. 3.26. The minimum d_{ring} and d_{space} used is 5 μm, since a wider width is attractive from the viewpoint of manufacturing process. Here, background of the SM-JTE was doped to D_{JTE2}, where the ratio between D_{JTE1} was $D_{\mathrm{JTE1}} : D_{\mathrm{JTE2}} = 4 : 1$. In this structure, background of SM-JTE was doped to remove the electrically floating region inside the JTE, which might affect the stability of high-speed switching operation [33].

Figure 3.27 shows the JTE1-dose dependence of breakdown voltage simulated for 20 kV-class PiN diodes with single-zone JTE, two-zone JTE, and the improved SM-JTE. Here, the voltage-blocking layer assumed has the doping concentration and thickness of 1×10^{14} cm^{-3} and 150 μm, respectively. The parallel-plane breakdown voltage obtained for this structure

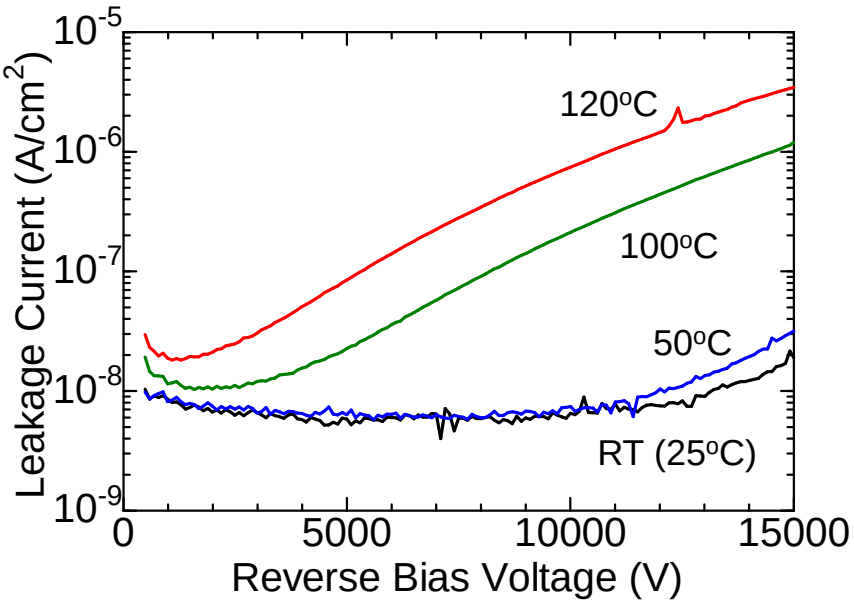


Figure 3.24: Temperature dependence of leakage current for a 20 kV-class PiN diode. A clear positive temperature coefficient of leakage current is observed.

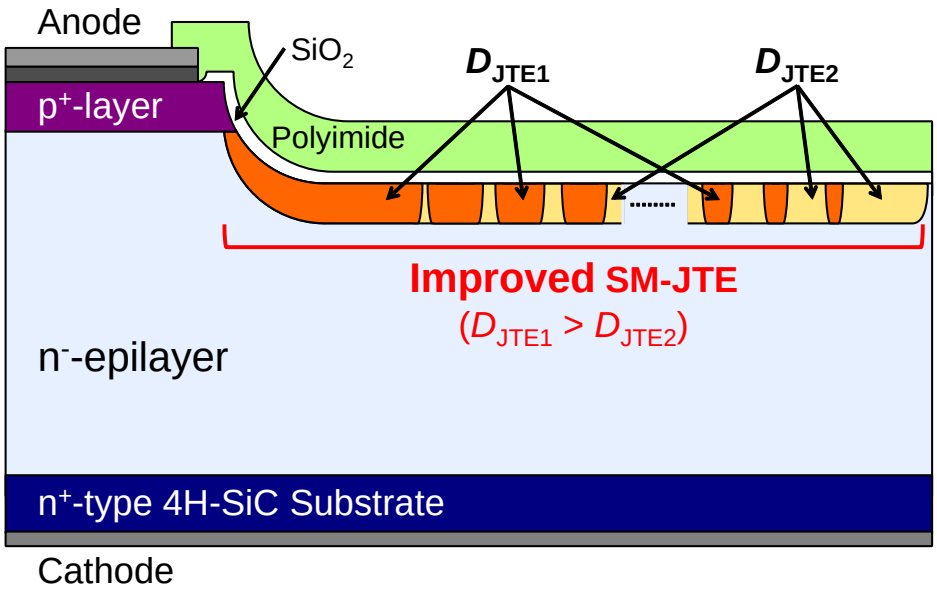


Figure 3.25: Improved SM-JTE structure proposed in this study where a VLD (Variation of Lateral Doping)-like dopant profile was realized in horizontal direction.

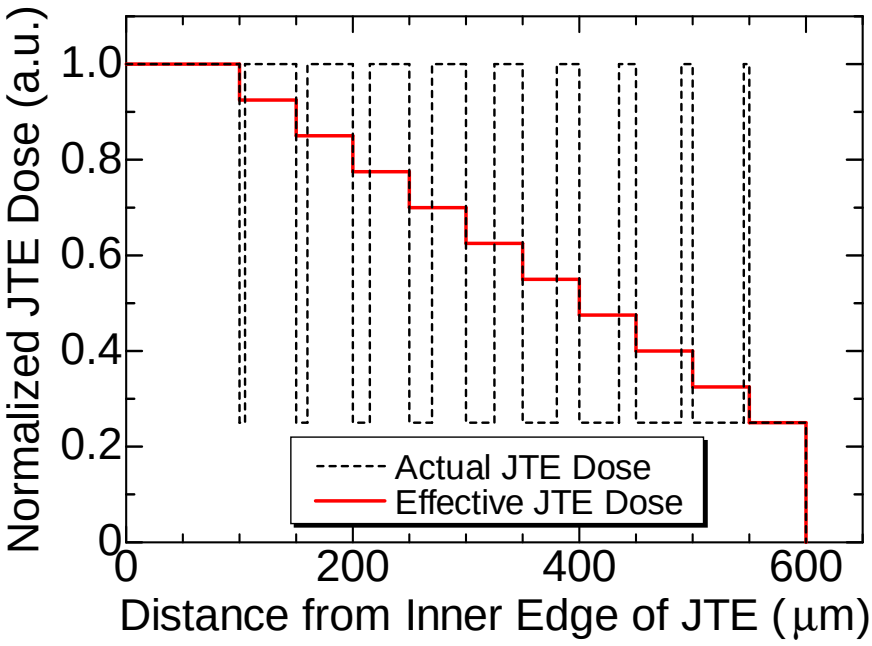


Figure 3.26: Effective JTE-dose distribution inside the improved SM-JTE together with the actual JTE dose distribution.

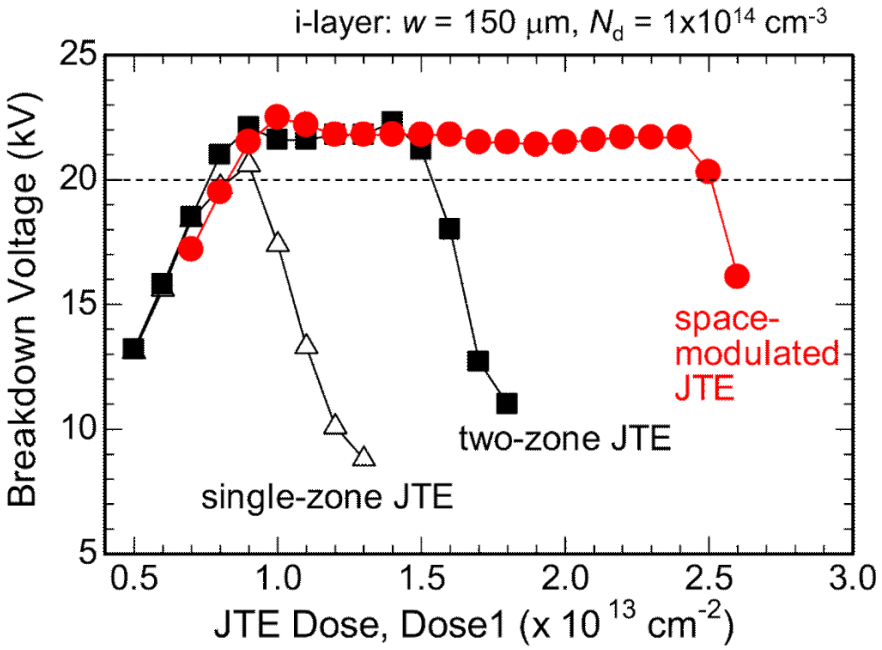


Figure 3.27: JTE1-dose dependence of breakdown voltage for SiC PiN diode with single-zone JTE, two-zone JTE, and the improved SM-JTE. Doping concentration and thickness of the voltage blocking layer assumed here was 1×10^{14} cm^{-3}, 150 μm.

is 23.7 kV, calculated from Konstantinov's ionization coefficients [24]. As shown in Fig. 3.27, the improved SM-JTE structure has realized the enlargement of optimum JTE-dose window compared with single-zone and two-zone JTE. Compared with the SM-two-zone JTE, widening of optimum JTE-dose window to maintain a near ideal breakdown voltage was realized in improved SM-JTE, which indicates the more efficient alleviation of electric field crowding by the increased number of rings in a SM-JTE. This optimum JTE-dose window ($\sim 1.5 \times 10^{13}$ cm^{-2}) seems to be wide enough because the interface charge density is in the order of low 10^{12} cm^{-2} for the passivation layer used here. When a wider optimum JTE-dose window is required, it can be realized by reducing the ring/space pitch and the minimum width used in the termination, which can realize a more VLD-like dopant profile. Furthermore, the horizontal dopant profile can be modified to be convex or concave shape instead of linear shape used in this study, which results in a wider optimum JTE-dose window while lowering the maximum breakdown voltage (for convex shape) or narrower optimum JTE-dose window while enhancing the maximum breakdown voltage (for concave shape) [34].

Using the design guideline of improved SM-JTE proposed in this section, a SiC PiN diode was fabricated using a 268-μm-thick voltage-blocking layer for the realization of 30 kV-class devices. Fig. 3.28 shows the I–V characteristics of the fabricated SiC PiN diode. Here, the improved SM-JTE with a 1050-μm total length and 18 rings inside was employed. The fabricated diode did not exhibit breakdown up to 26.9 kV, which was the limitation of measurement system used here. The leakage current was below 1×10^{-4} A/cm^2 at the maximum voltage. Because the lifetime-enhancement process (thermal oxidation of 72 h) was performed to the n$^-$-epilayer, this diode has superior forward characteristics close to the performance limitation. The differential on-resistance and forward voltage drop at 100 A/cm^2 were 9.72 mΩcm^2 and 4.72 V, respectively. These values are actually lower than that of 20 kV-class PiN diode fabricated in the previous section where thinner voltage-blocking layer was used, indicating the effect of the lifetime-enhancement process.

3.6 Summary

In this chapter, breakdown characteristics of UHV SiC PiN diodes with various JTE structures have been investigated. To overcome the narrow optimum JTE-dose window the conventional single-zone JTE has, SM-JTE was experimentally studied. By combining the SM-JTE to the two-zone JTE, widening of optimum JTE-dose window has been experimentally observed in 10 kV-class PiN diodes. Furthermore, from the experimental and simulated JTE-dose dependence of breakdown voltage, the effect of interface charge near the SiO_2/SiC interface was revealed. Particularly, the positive charge near the SiO_2/p-SiC interface has caused a shift of the JTE-dose dependence to the heavier JTE-dose region, making JTE structure with wide optimum JTE-dose window to be attractive for the fabrication of UHV

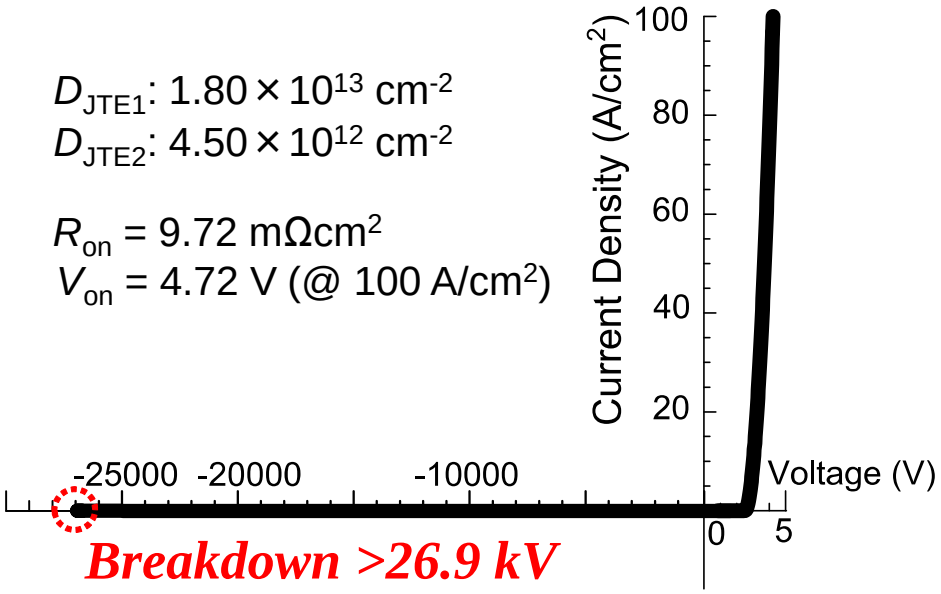


Figure 3.28: *I-V* characteristics of an UHV SiC PiN diode with voltage blocking layer thickness of 268 μm. Using the improved SM-JTE, breakdown voltage over 26.9 kV was achieved.

devices with a high yield.

Using the obtained knowledge from the study of 10 kV-class PiN diodes, a 20 kV-class PiN diode was fabricated. To tolerate the impact of interface charges, SM-two-zone JTE with a wide optimum JTE-dose window was employed. The fabricated SiC PiN diodes has exhibited a breakdown voltage of 21.7 kV, which is superior to the previous results. Furthermore, using a thicker voltage-blocking layer and a optimized SM-JTE with tapered VLD-like dopant distribution, SiC PiN diodes with breakdown voltage over 26.9 kV has also been realized.

From the easy fabrication process and the effectiveness shown in this study, it can be said that SM-JTE is a promising termination technology for realizing UHV SiC power devices. Moreover, from the ultrahigh-breakdown voltage and the low on-resistance obtained in this study, the superior potential of the UHV SiC bipolar devices has been demonstrated.

References

[1] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, and T. Hayashi, *Proceedings of 13th International Symposium on Power Semiconductor Devices and ICs* (2001) p. 27.

[2] A. Agarwal, M. Das, S. Krishnaswami, J. Palmour, J. Richmond, and S.-H. Ryu, *Material Research Society Symposium Proceeding* **815** (2004) p. 243.

[3] T. Hiyoshi, T. Hori, J. Suda, and T. Kimoto, *IEEE Transactions on Electron Devices* **55**, 1841 (2008).

[4] J. H. Zhao, P. Alexandrov, and X. Li, *IEEE Electron Device Letters* **24**, 402 (2003).

[5] R. S. Howell, S. Buchoff, S. Van Campen, T. R. McNutt, A. Ezis, B. Nechay, C. F. Kirby, M. E. Sherwin, R. C. Clarke, and R. Singh, *IEEE Transactions on Electron Devices* **55**, 1807 (2008).

[6] J. H. Zhao, P. Alexandrov, J. Zhang, and X. Li, *IEEE Electron Device Letters* **25**, 474 (2004).

[7] Q. Zhang, M. Das, J. Sumakeris, R. Callanan, and A. Agarwal, *IEEE Electron Device Letters* **29**, 1027 (2008).

[8] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer, 2008.

[9] D. C. Sheridan, G. Niu, and J. D. Cressler, *Solid-State Electronics* **45**, 1659 (2001).

[10] J. N. Merrett, T. Isaacs-Smith, D. C. Sheridan, and J. R. Williams, *Journal of Electronic Materials* **31**, 635 (2002).

[11] R. Pérez, D. Tournier, A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán, *IEEE Transactions on Electron Devices* **52**, 2309 (2005).

[12] P. A. Losee, S. K. Balachandran, L. Zhu, C. Li, J. Seiler, T. P. Chow, I. B. Bhat, and R. J. Gutmann, *Proceeding of 16th International Symposium on Power Semiconductor Devices and ICs* (2004), p. 301.

[13] R. Ghandi, B. Buono, M. Domeij, G. Malm, C.-M. Zetterling, and M. Östling, *IEEE Electron Device Letters* **30**, 1170 (2009).

[14] G. Pâques, S. Scharnholz, N. Dheilly, D. Planson, and R. W. De Doncker, *IEEE Electron Device Letters* **32**, 1421 (2011).

[15] G. Feng, J. Suda, and T. Kimoto, *IEEE Transactions on Electron Devices* **59**, 414 (2012).

[16] W. Sung, E. Van Brunt, B. J. Baliga, and A. Q. Huang, *IEEE Electron Device Letters* **32**, 880 (2011).

[17] A. V. Bolotnikov, P. G. Muzykov, Q. Zhang, A. K. Agarwal, and T. S. Sudarshan, *IEEE Transactions on Electron Devices* **57**, 1930 (2010).

[18] E. A. Imhoff, F. J. Kub, K. D. Hobart, M. G. Ancona, B. L. VanMil, D. K. Gaskill, K.-K. Lew, R. L. Myers-Ward, and C. R. Eddy, *IEEE Transactions on Electron Devices* **58**, 3395 (2011).

[19] V. A. K. Temple and W. Tantraporn, *IEEE Transactions on Electron Devices* **33**, 1601 (1986).

[20] W. Tantraporn and V. A. K. Temple, *IEEE Transactions on Electron Devices* **34**, 2200 (1987).

[21] H. Lendenmann, A. Mukhitdinov, F. Dahlquist, H. Bleichner, M. Irwin, and R. Soderholm, *Proceedings of 13th International Symposium on Power Semiconductor Devices and ICs* (2001) p. 31.

[22] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, *Journal of Applied Physics* **96**, 224 (2004).

[23] Y. Negoro, T. Kimoto, and H. Matsunami, *Journal of Applied Physics* **98**, 043709 (2005).

[24] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, *Applied Physics Letters* **71**, 90 (1997).

[25] M. Noborio, J. Suda, and T. Kimoto, *IEEE Transactions on Electron Devices* **56**, 1953 (2009).

[26] R. Ghandi, B. Buono, M. Domeij, R. Esteve, A. Schoner, J. Han, S. Dimitrijev, S. A. Reshanov, C.-M. Zetterling, and M. Östling, *IEEE Transactions on Electron Devices* **58**, 259 (2011).

[27] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami, *Japanese Journal of Applied Physics* **44**, 1213 (2005).

[28] K. Nakayama, A. Tanaka, M. Nishimura, K. Asano, T. Miyazawa, M. Ito, and H. Tsuchida, *IEEE Transactions on Electron Devices* **59**, 895 (2012).

[29] T. Hiyoshi and T. Kimoto, *Applied Physics Express* **2**, 091101 (2009).

[30] L. Storasta, H. Tsuchida, T. Miyazawa, and T. Ohshima, *Journal of Applied Physics* **103**, 013705 (2008).

[31] R. Stengl, U. Gosele, C. Fellinger, M. Beyer, and S. Walesch, *IEEE Transactions on Electron Devices* **33**, 426 (1986).

[32] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*, Wiley, 2014.

[33] N. Kaji, H. Niwa, J. Suda, and T. Kimoto, *Japanese Journal of Applied Physics* **52**, 070204 (2013).

[34] A. Bolotnikov, P. Losee, P. Deeb, M. Wang, S. Arthur, and L. Stevanovic, *Extended Abstract of 16 th International Conference on Silicon Carbide and Related Materials*, We–2A–2 (2015).

Chapter 4

Design and Fabrication of Ultrahigh-Voltage Mesa Merged PiN Schottky Diodes

4.1 Introduction

In a SiC bipolar device, its on-resistance can be reduced by the lifetime-enhancement process [1, 2]. Using this process, SiC PiN diodes with on-resistance of few $m\Omega cm^2$ have been realized for over 10 kV-class devices [3, 4]. However, as explained in Section 1.4, the built-in potential of 3 V causes a large power dissipation which cannot be escaped. Furthermore, at a low operating current density, bipolar devices may have larger conduction loss than unipolar devices even if the conductivity modulation occurs. Therefore, to reduce the conduction loss in the low current density, integration of bipolar and unipolar devices in a single chip is one solution to this problem.

The idea of integrating unipolar and bipolar devices has been proposed in Si transistors [5–7]. However, these transistors have complicated structures such as backside doping control which is challenging in the present technology of SiC. Therefore, for the first step of the study in hybrid operating devices, studies on a merged-PiN-Schottky (MPS) diode are important since it is the fundamental structure for such a device.

The schematic structure of a MPS diode is shown in Fig. 4.1, where an additional p^+-region is formed at the anode layer of Schottky barrier diode (SBD). Although it may look the same as the junction-barrier-Schottky (JBS) diode, the difference is the ohmic contact formed to the p^+-region, which realizes the bipolar operation. In this device, when the forward bias is low, electron current flows from the SBD region of the device at first. Afterwards, when the forward bias exceeds the built-in potential of the pn-junction, injection of holes from the p^+n junction triggers the bipolar operation (conductivity modulation) of the PiN diode region. Therefore, operation of this diode can be assumed to be a parallel operation of SBD and PiN diode.

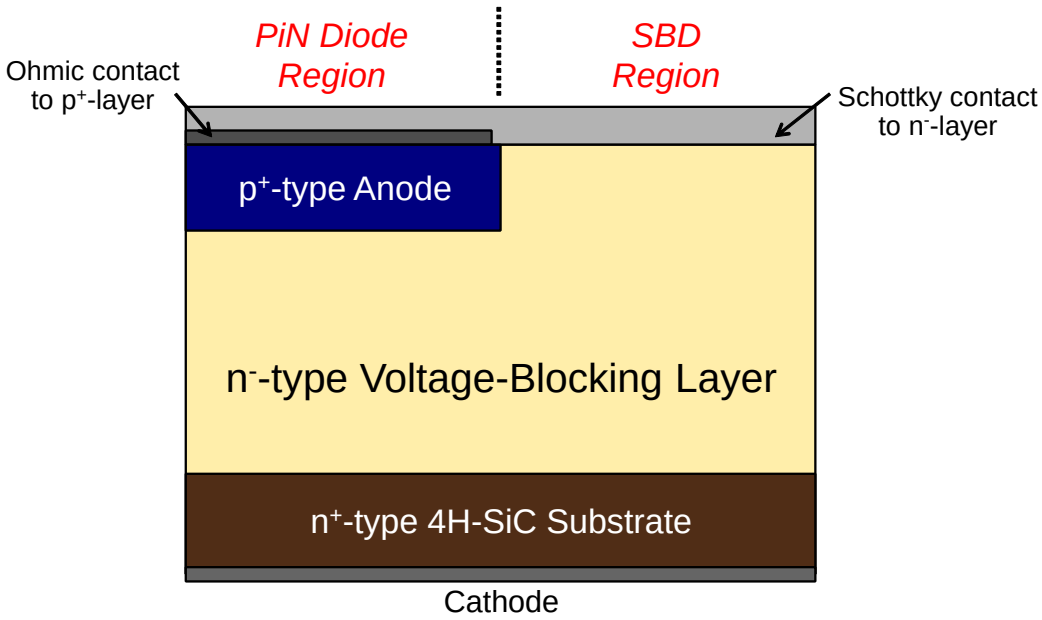


Figure 4.1: Schematic cross section of a planar MPS diode.

In SiC, studies on MPS diodes have been conducted mainly on 600 and 1200 V-class devices [8, 9]. In these devices, because on-resistance of unipolar operation (from here on, unipolar on-resistance) is low enough in this voltage-class, bipolar operation is not considered and it is only used for the improvement of surge current capability. On the other hand, for UHV MPS diodes, there is only one investigation by Van Brunt where a 10 kV-class MPS diode has been demonstrated [10]. However, this study mainly focuses on anode layer design to reduce the injection efficiency for the improvement of switching characteristics. Therefore, unipolar operation is not considered and there still exists the large 3 V built-in potential in the low current density region.

In this Chapter, toward the integrated unipolar/bipolar SiC transistors, fundamental studies on SiC MPS diodes are conducted which mainly focuses on the anode designing. First, the concept of a novel MPS structure where a mesa-type epitaxial PiN diode integrated with a JBS diode is shown. Following that, the designing of voltage-blocking layer, JBS structure, and edge termination to realize the ultrahigh breakdown voltage is explained. In the studies of anode designing, a "snapback" phenomenon during the forward operation is mainly investigated by analytical modeling, device simulation, and experiment to clarify this phenomenon. Using these obtained results, UHV SiC MPS diodes are fabricated to show the potential of SiC hybrid operating devices and guidelines to design such devices.

4.2 Designing of Ultrahigh-Voltage MPS Diodes

In this section, the concept of the UHV MPS diode proposed in this study is explained. In addition, each of the component structures, which is the voltage-blocking layer, JBS design, edge termination, and mesa structure of the MPS diode are optimized through analytical modeling and device simulation.

4.2.1 Structure of MPS Diodes

A conventional MPS diode structure is shown in Fig. 4.1, which is commonly referred as a planar structure. This is the standard structure in Si because p^+-anode can be easily formed by diffusion of p-type dopant such as boron. In SiC, because the diffusion coefficient for p-type dopant is extremely small, this diffusion process cannot be used for the fabrication. Therefore, ion implantation is the only way to form a local p^+-region during the fabrication of planar MPS diodes in SiC. However, it is known that ion implantation induces large number of point defects [11], which causes large increase of on-resistance in SiC PiN diodes [12]. Because bipolar operation is also important in the MPS diode of this study, implanted p^+-anode is unsuitable. Therefore, in this study, an epitaxially grown p^+-anode is employed. However, fabrication of planar structure using an epitaxially grown p^+-anode is challenging because it requires epitaxy inside a trench. This makes planar structure unsuitable for SiC hybrid operating devices.

In this study, to use the epitaxially grown p^+-anode, a mesa structure as shown in Fig. 4.2 has been employed. Fabrication of this structure is compatible to the mesa-type PiN diode investigated in Section 3, where an additional process for Schottky contact formation is required. In addition, because simple SBD structure will induce a large leakage current caused by electron tunneling [13], a JBS structure is employed by adding p^+-barriers in the SBD region using Al^+ ion implantation. Here, p^+-barriers can be fabricated by ion implantation because bipolar operation is not considered in the JBS region.

4.2.2 Designing of Voltage-Blocking Layer

The first step for designing an MPS diode is the optimization of voltage-blocking layer. In a conventional PiN diode, voltage-blocking layer can be designed by just changing the thickness of the epilayer. Because forward operation relies on the conductivity modulation, the background doping does not matter unless it is small enough. In the MPS diode of this study, however, both thickness and doping concentration must be optimized because unipolar operation is considered. In a unipolar device, it is known that optimized punchthrough structure can realize lower unipolar on-resistance than non-punchthrough structure at a given breakdown voltage. In this section, optimization of voltage-blocking layer will be analytically conducted while considering the doping concentration dependence of critical electric field strength.

Optimization of Punchthrough Structure

First, doping concentration dependence of critical electric field strength is assumed as follows:

$$E_{\mathrm{cr}} = a \cdot (N_{\mathrm{d}})^b. \tag{4.1}$$

Here, N_{d} is the doping concentration of voltage-blocking layer and a, b are the fitting parameter. In this case, depletion layer width at breakdown (W_{NPT}) and the breakdown voltage (BV_{NPT}) for a non-punchthrough structure can be expressed as,

$$W_{\mathrm{NPT}} = \frac{\varepsilon}{qN_{\mathrm{d}}} \cdot E_{\mathrm{cr}} = a'(N_{\mathrm{d}})^{b-1} \tag{4.2}$$

$$BV_{\mathrm{NPT}} = \frac{1}{2}E_{\mathrm{cr}}W_{\mathrm{NPT}} = \frac{1}{2}aa'(N_{\mathrm{d}})^{2b-1} = a''(N_{\mathrm{d}})^{2b-1}. \tag{4.3}$$

Using above equations, relationship of on-resistance ($R_{\text{ON-NPT}}$) and BV_{NPT} can be expressed as follow:

$$R_{\text{ON-NPT}} = \frac{W_{\mathrm{NPT}}}{q\mu N_{\mathrm{d}}} = \frac{a'}{q\mu(a'')^c}(BV_{\mathrm{NPT}})^c. \tag{4.4}$$

Here, $c = \frac{b-2}{2b-1}$.

For a punchthrough structure with a voltage-blocking layer thickness of W_{PT}, its breakdown voltage can be expressed as,

$$BV_{\mathrm{PT}} = E_{\mathrm{cr}}W_{\mathrm{PT}} - \frac{qN_{\mathrm{d}}}{2\varepsilon}W_{\mathrm{PT}}^2. \tag{4.5}$$

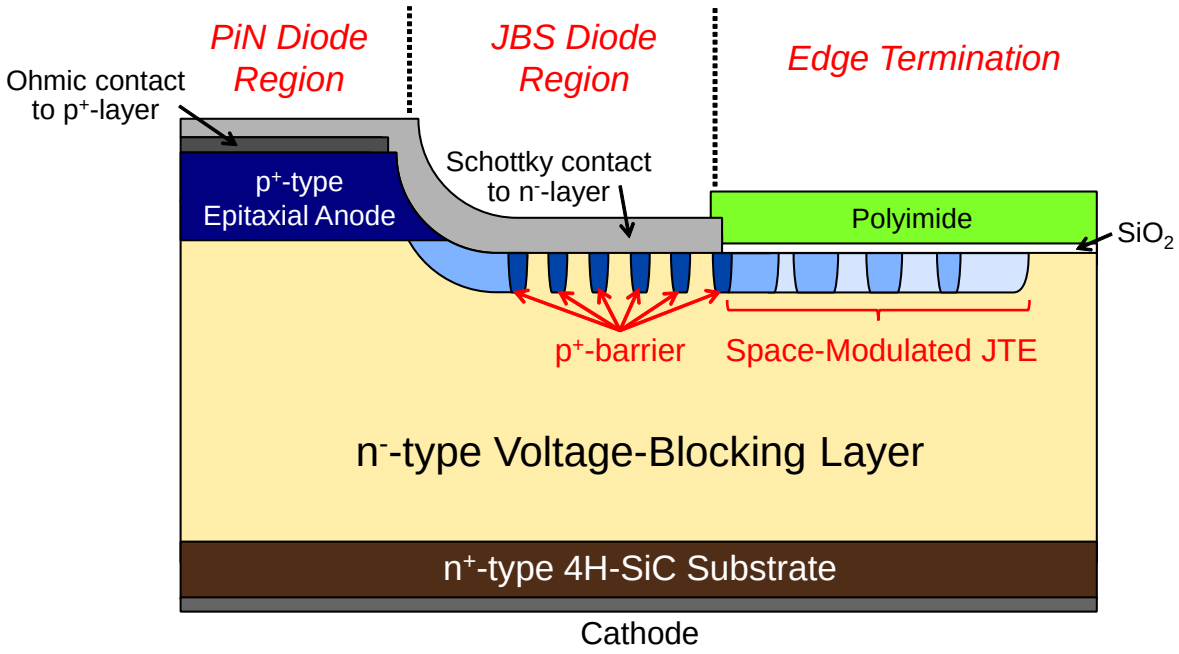


Figure 4.2: Schematic cross section of the mesa-type MPS diode using an epitaxial p^+-anode and JBS structure.

Although a punchthrough structure is considered, the maximum electric field at breakdown is assumed to be the critical electric field strength in a non-punchthrough case for easiness. However, if W_{PT} is close to W_{NPT}, the critical electric field strength can still be used in a punchthrough structure. Using equations (4.3) and (4.5), the following equation can be derived:

$$\frac{BV_{\mathrm{PT}}}{BV_{\mathrm{NPT}}} = 2 \cdot \frac{W_{\mathrm{PT}}}{W_{\mathrm{NPT}}} - \frac{W_{\mathrm{PT}}^2}{W_{\mathrm{NPT}}^2} = 2r - r^2. \tag{4.6}$$

Here, r is the ratio between W_{PT} and W_{NPT}. Similar to the case of non-punchthrough structure, $R_{\mathrm{ON\text{-}PT}} - BV_{\mathrm{PT}}$ relationship can be obtained as follow:

$$R_{\mathrm{ON\text{-}PT}} = \frac{W_{\mathrm{PT}}}{q\mu N_{\mathrm{d}}} = \frac{rW_{\mathrm{NPT}}}{q\mu N_{\mathrm{d}}} = \frac{a'}{q\mu (a'')^c} \frac{r}{(2r - r^2)^c} (BV_{\mathrm{PT}})^c. \tag{4.7}$$

Comparing equations (4.4) and (4.7), the ratio between on-resistance of punchthrough and non-punchthrough at a given breakdown voltage can be shown as

$$\frac{R_{\mathrm{ON\text{-}PT}}}{R_{\mathrm{ON\text{-}NPT}}} = \frac{r}{(2r - r^2)^c}. \tag{4.8}$$

The above equation predicts the minimum $R_{\mathrm{ON\text{-}PT}}$ at the following r:

$$r = \frac{2}{3}(b + 1). \tag{4.9}$$

Designing of Voltage-Blocking Layer of Ultrahigh Voltage MPS Diode

In this thesis, the critical electric field strength has been determined in Chapter 2. To express the critical electric field strength in the form of equation (4.1), fitting was performed at doping concentration of 10^{14}–10^{16} cm^{-3}, where $a = 7.456 \times 10^4$ V/cm and $b = 9.533 \times 10^{-2}$ were obtained. Therefore, equation (4.8) can be calculated as shown in Fig. 4.3, and the optimum r was determined to be 0.73. Figure 4.4 shows the R_{ON}–BV relationship for a non-punchthrough, and a punchthrough structure with $r = 0.73$. By using the optimized punchthrough structure, the relationship has improved.

Using the above relationship, a voltage-blocking layer for UHV MPS diode has been determined. In this study, 10 kV-class SiC MPS diodes are fabricated. Because the actual breakdown voltage can degrade due to the electric field crowding, ideal breakdown voltage should be larger than 10 kV. Assuming a 20% reduction, doping concentration and thickness of the voltage blocking layer was designed to be 7×10^{14} cm^{-3} and 100 μm, respectively. The ideal breakdown voltage for this epilayer was calculated to be 13.0 kV.

4.2.3 Designing of Junction Barrier Schottky Diode Region

In this section, a layout of p^+-barriers in the JBS region is optimized using a numerical device simulation (Synopsys TCAD). Figure 4.5 shows the assumed structure for the simulation, where a planar structure is assumed and a voltage-blocking layer structure determined in the previous section (7×10^{14} cm^{-3}, 100 μm) is employed. For the Schottky metal, titanium

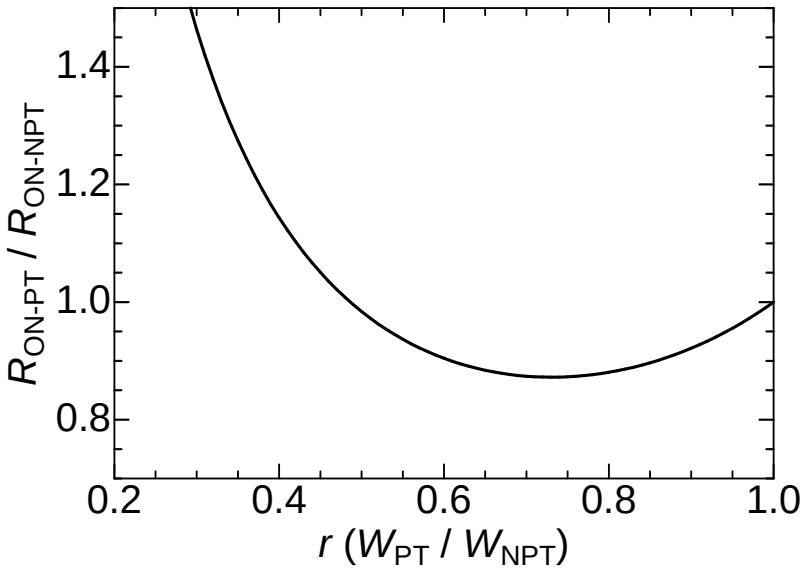


Figure 4.3: The ratio between on-resistance of PT and NPT as a function of ratio between the thickness of PT and NPT (r).

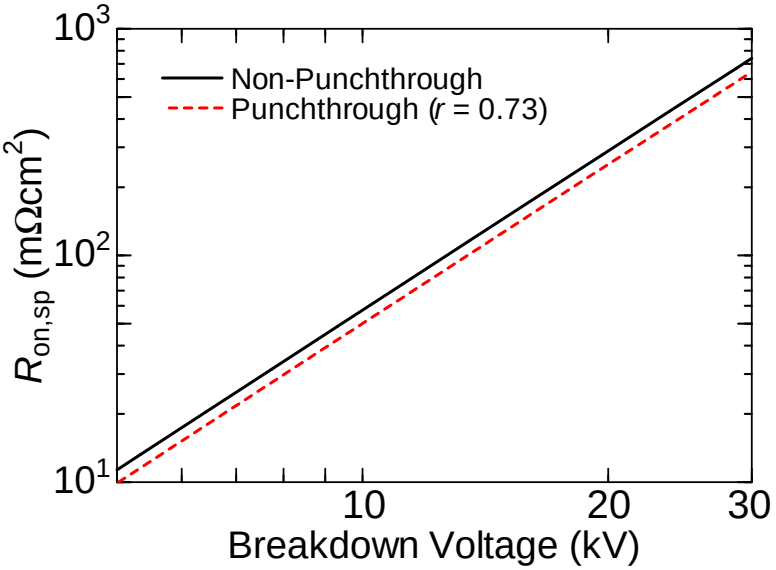


Figure 4.4: R_{ON}–BV relationship for NPT and PT with optimized ratio between PT and NPT thickness.

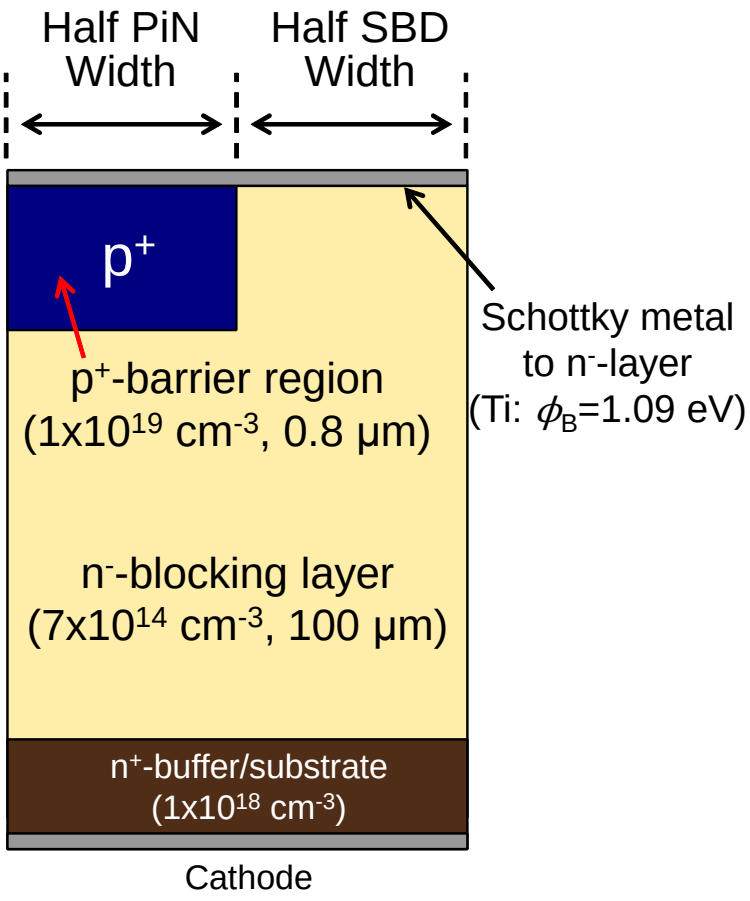


Figure 4.5: Schematic cross section of a planar JBS diode for the simulation of anode layout design.

(ϕ_B = 1.09 eV) has been employed [14]. During the simulation, the impact ionization coefficients obtained in Chapter 2 were employed, and an electron tunneling at the Schottky metal interface has been considered in the Schottky region.

First, effects of the p^+-region width are investigated. Figure 4.6 shows the p^+-region width dependence of reverse current-voltage (I–V) characteristics while assuming a constant SBD region width of 4 μm. In the figure, reverse I–V characteristics of SBD and PiN diode are also shown. Because electron tunneling is occurring at the Schottky interface, large leakage current appeared in the case of SBD. By adding a p^+-region, the electric field strength at the Schottky interface has decreased, and remarkable reduction of leakage current is observed. However, in the case of p^+-region width of 2 μm, the leakage current is slightly higher than the others. In the case of 2-μm-width, its width is too narrow and the effect of electric field crowding at the p^+-region curvature became large. At a reverse bias of 9 kV, 2-μm-width JBS has maximum electric field strength of 2.73 MV/cm, whereas 4-μm-width JBS has 2.48 MV/cm at the junction curvature. Therefore, 2-μm-width p^+-region is insufficient for leakage current suppression, and p^+-region width over 4 μm is appropriate. Because narrower p^+-region width is desirable from the point of view of forward conduction, p^+-region width of 4 μm is the optimized value for the JBS structure in this study.

Next, effects of the SBD-region width are investigated. Figure 4.7 shows the SBD-region width dependence of reverse I–V characteristics while assuming a constant p^+-region width of 4 μm. As the SBD-region width widens, the leakage current has increased because of the reduced shielding effect of p^+-barriers. In a conventional power device, the leakage current density should be below 1 mA/cm^2 at the rated voltage. In the case of this study, all of the SBD-region widths calculated here realize leakage current density below 1 mA/cm^2 at the reverse bias voltage of 10 kV.

To further optimize the SBD-region width, forward characteristics was investigated for the same epilayer (7×10^{14} cm^{-3}, 100 μm). Figure 4.8 shows the forward I–V characteristics of JBS diodes with various SBD-region widths. When the SBD-region width is too narrow, 2 μm in this case, a larger forward voltage must be applied to start the current flow. This is because too narrow SBD-region width caused the merge of depletion layer between the p^+-region even at 0 V, which induces an additional energy barrier to overcome at forward voltage. Therefore, too narrow SBD-region width is insufficient for JBS. Because forward I–V characteristics does not change much at SBD-region width over 6 μm, the optimized SBD-region width considering both reverse and forward characteristics can be determined to be 6 μm in this study.

4.2.4 Designing of Edge Termination Region

In this study, space-modulated junction termination extension (SM-JTE) investigated in Chapter 3 is adopted to the MPS diode. Because SM-JTE is placed outside the JBS region as shown in Fig. 4.2, device simulation using a planar PiN diode is performed to investigate

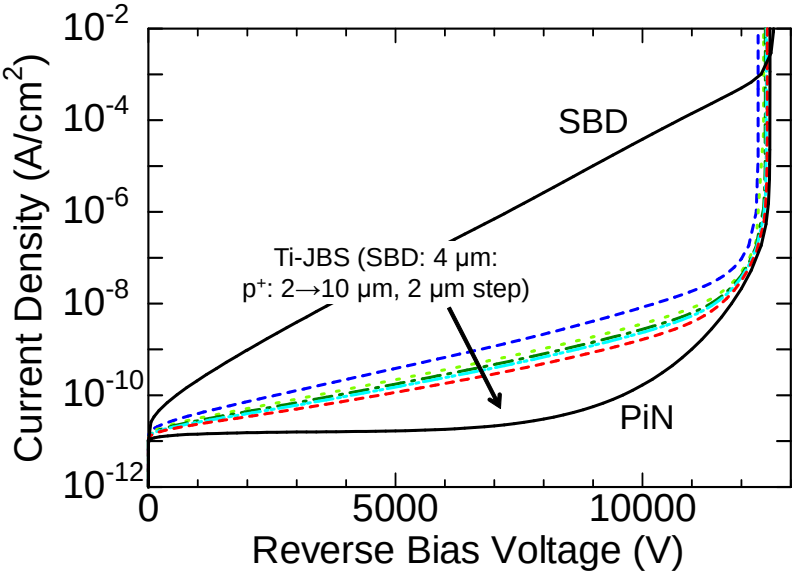


Figure 4.6: p$^+$-region width dependence of reverse I–V characteristics while assuming a constant SBD region width of 4 μm.

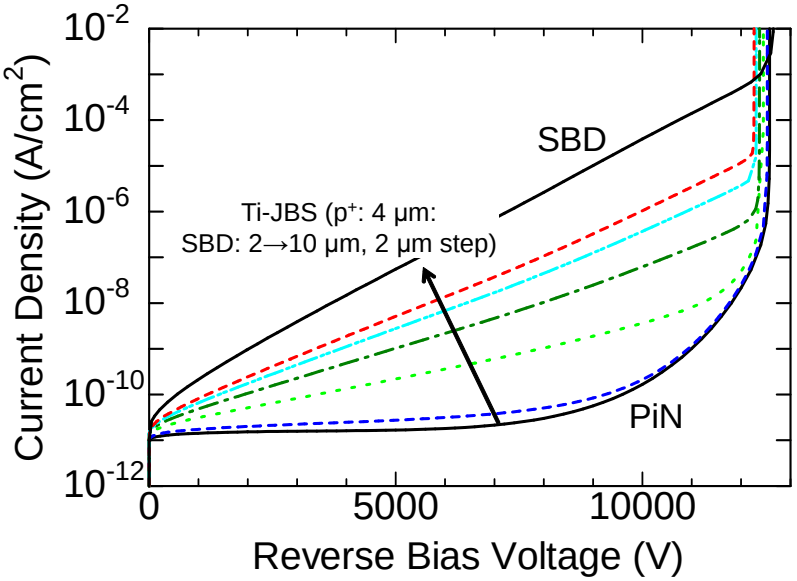


Figure 4.7: SBD-region width dependence of reverse I–V characteristics while assuming a constant p$^+$-region width of 4 μm.

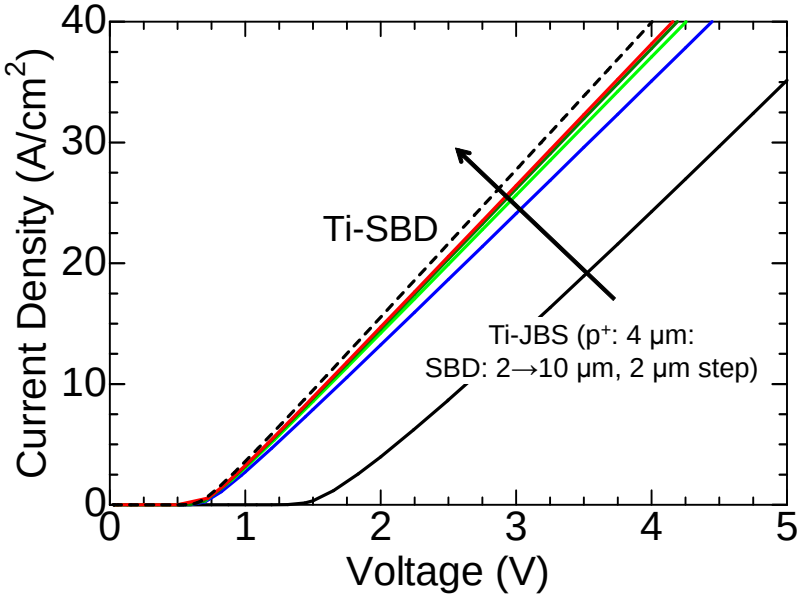


Figure 4.8: SBD-region width dependence of forward I–V characteristics while assuming a constant p^+-region width of 4 μm.

the JTE-dose dependence of breakdown voltage for SM-JTE in this section. Furthermore, improved SM-JTE structure is proposed to reduce the lithography complexities during the JTE fabrication.

Figure 4.9 shows the schematic structure of a planar PiN diode with SM-JTE assumed for the simulation. Here, voltage-blocking layer determined in the previous section (7×10^{14} cm^{-3}, 100 μm) is used. Lateral distribution of actual and *effective* JTE-dose inside the SM-JTE is shown in Fig. 4.10. Here, ratio of the JTE dose of rings (D_{ring}) and spaces (D_{space}) is set to 4 : 1. In this SM-JTE structure, *effective* JTE-dose is linearly decreased toward the outer edge of JTE while keeping the sum of ring width (d_{ring}) and space width (d_{space}) to 30 μm. Compared with the improved structure described in Chapter 3, this structure has smaller $d_{\mathrm{ring}} + d_{\mathrm{space}}$ which enables a more VLD-like dopant distribution.

Figure 4.11 shows the D_{ring} dependence of breakdown voltage for Cartesian and cylindrical coordinate. Here, simulation using Cartesian coordinate corresponds to the simulation of JTE along one side of the device, and cylindrical coordinate corresponds to JTE at the corner of the device. During the simulation using cylindrical coordinate, radius of the p^+-anode was set to 4 μm, which is actually used for the outermost p^+-barriers in the JBS region of the fabricated device. From Fig. 4.11, simulation using the cylindrical coordinate has smaller breakdown voltage than Cartesian especially at small D_{ring}. Because cylindrical coordinate generates spherical p^+n junction, effects of the electric field crowding are enhanced if it occurs at the edge of p^+-anode, which is the case for small D_{ring}. However, optimum JTE-dose window to obtain breakdown voltage over 10 kV is still wide ($\sim 2 \times 10^{13}$ cm^{-2}) although the degradation of breakdown voltage is occurring at the corner. This value is larger than that of SM-JTE described in Chapter 3, which indicates the larger robustness to the interface charge near SiO_2/SiC.

Although the explained SM-JTE structure showed a great potential for realizing UHV MPS diodes, there is one large problem. When, $d_{\mathrm{ring}} + d_{\mathrm{space}}$ is reduced to realize a better VLD-like dopant profile, the minimum width of d_{ring} and d_{space} must be also reduced. In the case of the structure shown in Fig. 4.10, the minimum width is 2 μm. Because too narrow d_{ring} and d_{space} can cause problems during the photolithography process, minimum width of d_{ring} and d_{space} should not be reduced too much. Therefore, in this study, SM-JTE is further improved by modulating the *effective* JTE-dose in two-dimensional direction. Figure 4.12(a) shows the mask layout design for MPS diode with conventional SM-JTE structure. Here, a hexagonal unit cell structure is assumed. At the innermost and outermost parts of SM-JTE, d_{ring} and d_{space} become especially narrow. In the improved SM-JTE shown in Fig. 4.12(b), the rings are fragmented two-dimensionally while keeping d_{ring} and d_{space} to a moderate width, which was 8 μm in this case. Although d_{ring} and d_{space} are kept wide, the *effective* JTE-dose is modulated two-dimensionally and lateral distribution shown in Fig. 4.10 is realized.

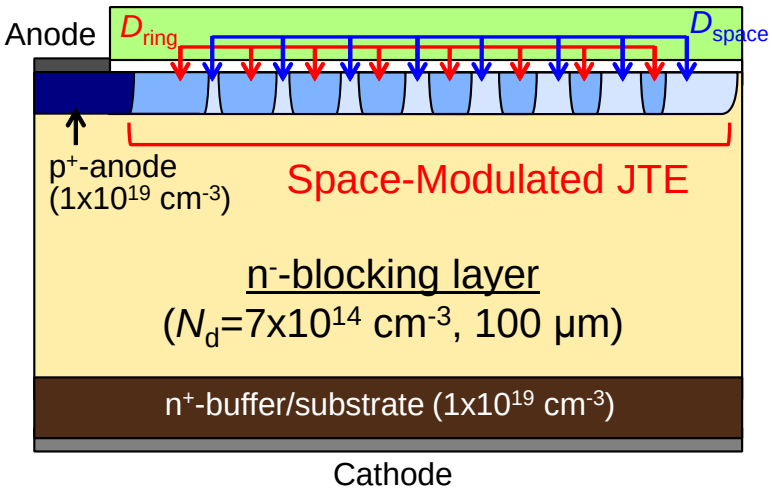


Figure 4.9: Schematic structure of a planar PiN diode with SM-JTE assumed for the simulation of breakdown voltage.

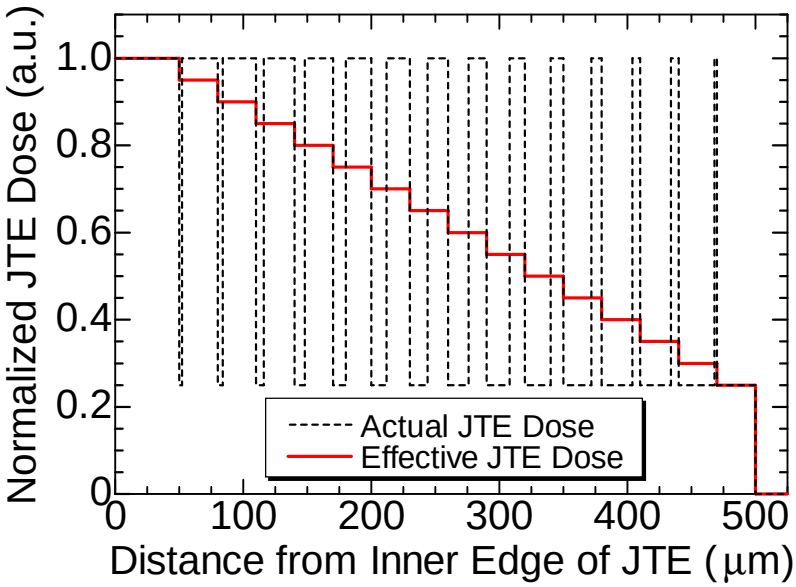


Figure 4.10: Lateral distribution of actual and *effective* JTE dose inside the SM-JTE.

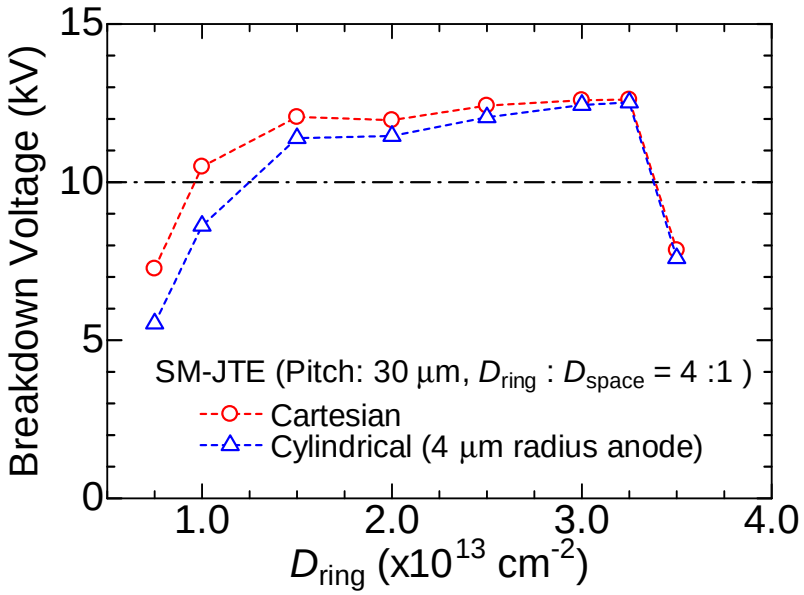


Figure 4.11: Simulated D_{ring} dependence of breakdown voltage in Cartesian and cylindrical coordinate.

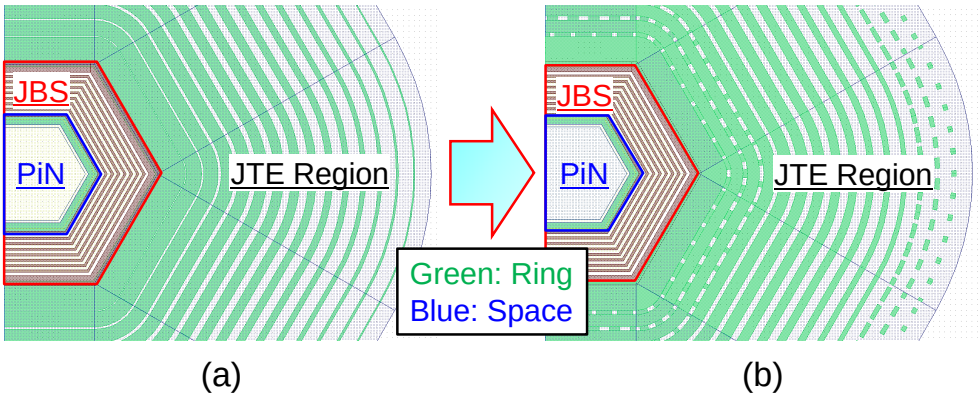


Figure 4.12: Mask layout design for (a) conventional SM-JTE used in Chapter 3 and (b) improved SM-JTE with two-dimensionally modulated structure.

4.2.5 Designing of Mesa Structure

In addition to the JBS and edge termination region, mesa structure is another region where electric field crowding occurs and degrades the breakdown voltage. Because using a mesa structure is indispensable for MPS diode with epitaxial p^+-anode, this region must be carefully studied.

Figure 4.13 shows the simulated structure of a mesa MPS diode to investigate the influence of mesa structure to the breakdown voltage. Here, p^+-regions at the mesa top and bottom correspond to the p^+-anode and p^+-barrier in the JBS region, respectively. In this study, to reduce the electric field crowding occurring at the corner of mesa, a p-type region has been implanted in the mesa region. Considering the fabrication process, this implantation should be performed at the same time of p^+-barriers or JTE implantation. Therefore, reverse characteristics are simulated using implantation dose used for p^+-barriers and JTE implantation.

Figure 4.14 shows the simulated reverse I–V characteristics of mesa structure for the voltage blocking layer determined in the previous section (7×10^{14} cm^{-3}, 100 μm). For the comparison, result of a planar PiN diode is also shown. From Fig. 4.14, mesa structure had smaller breakdown voltage than the planar PiN diode. Furthermore, smallest breakdown voltage was obtained when the implanted dose was that of p^+-barriers. When the implanted dose is too large, the p-type region does not deplete at reverse bias and breakdown voltage degrades. If the dose is not as large (Dose: $1.5 - 2.5 \times 10^{13}$ cm^{-2}), the implanted p-type region will deplete and have a smaller electric field strength at the corner of the p-type region. However, because breakdown voltages for all of the implanted doses have values close to or even higher than that of the JBS region and the JTE region with optimum dose, this region will not become a critical weak point when designing UHV devices. Furthermore, the effect of mesa structure may become less effective in experiment because an improved bevel mesa structure with rounded corner will be used as the mesa structure in this study. This structure can alleviate electric field crowding at the mesa corner, which will further reduce the electric field crowding at the mesa corner.

4.3 Device Fabrication

In this section, fabrication process of mesa MPS diodes is described. The schematic structure of a fabricated MPS diode is shown in Fig. 4.2. In this study, two types of voltage-blocking layers shown in Table 4.1 were used. For the "Type A" epilayer, a 95-μm-thick n-type epilayer doped to 6×10^{14} cm^{-3} was used for the 10 kV-class device. Here, the doping concentration and thickness were optimized to realize the smallest unipolar on-resistance at the given breakdown voltage according to the analysis performed in the previous section. On the other hand, for the "Type B" epilayer, a 270-μm-thick n-type epilayer doped to 1×10^{14} cm^{-3} was used. This Type B epilayer is not optimized for the unipolar operation

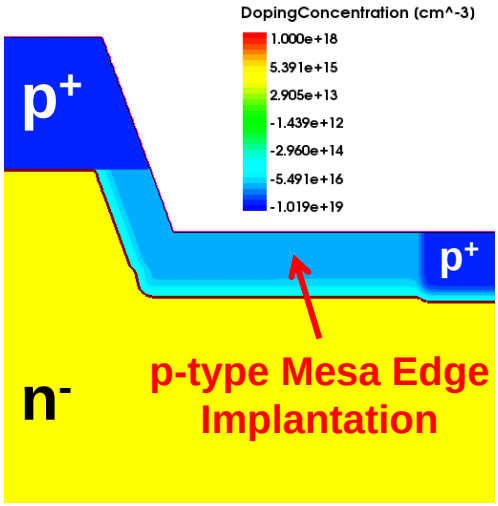


Figure 4.13: The simulated structure of a mesa MPS diode to investigate the influence of mesa structure to the breakdown voltage.

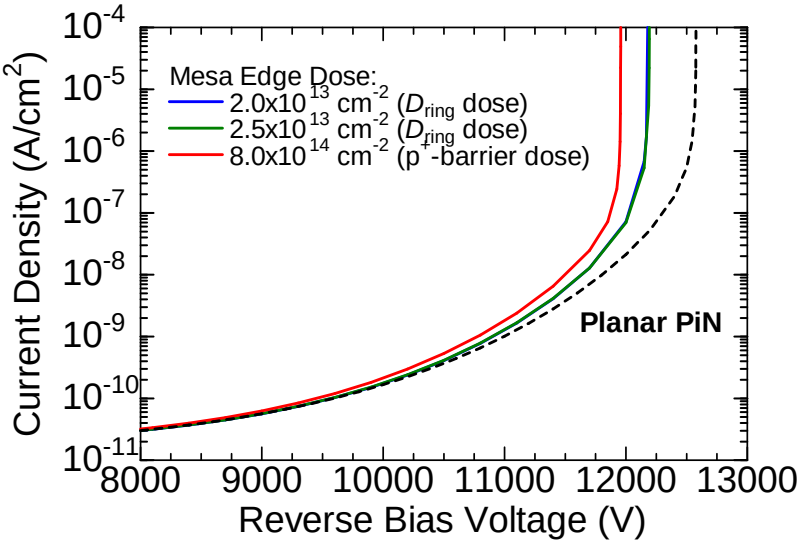


Figure 4.14: Reverse I–V characteristics of mesa structure with various implanted mesa dose.

Table 4.1: Doping concentration and thickness of the voltage-blocking layer used in the fabricated MPS diode.

Epilayer	Doping Concentration	Thickness
Type A	$N_{\mathrm{d}} = 6 \times 10^{14}$ cm^{-3}	95 μm
Type B	$N_{\mathrm{d}} = 1 \times 10^{14}$ cm^{-3}	270 μm

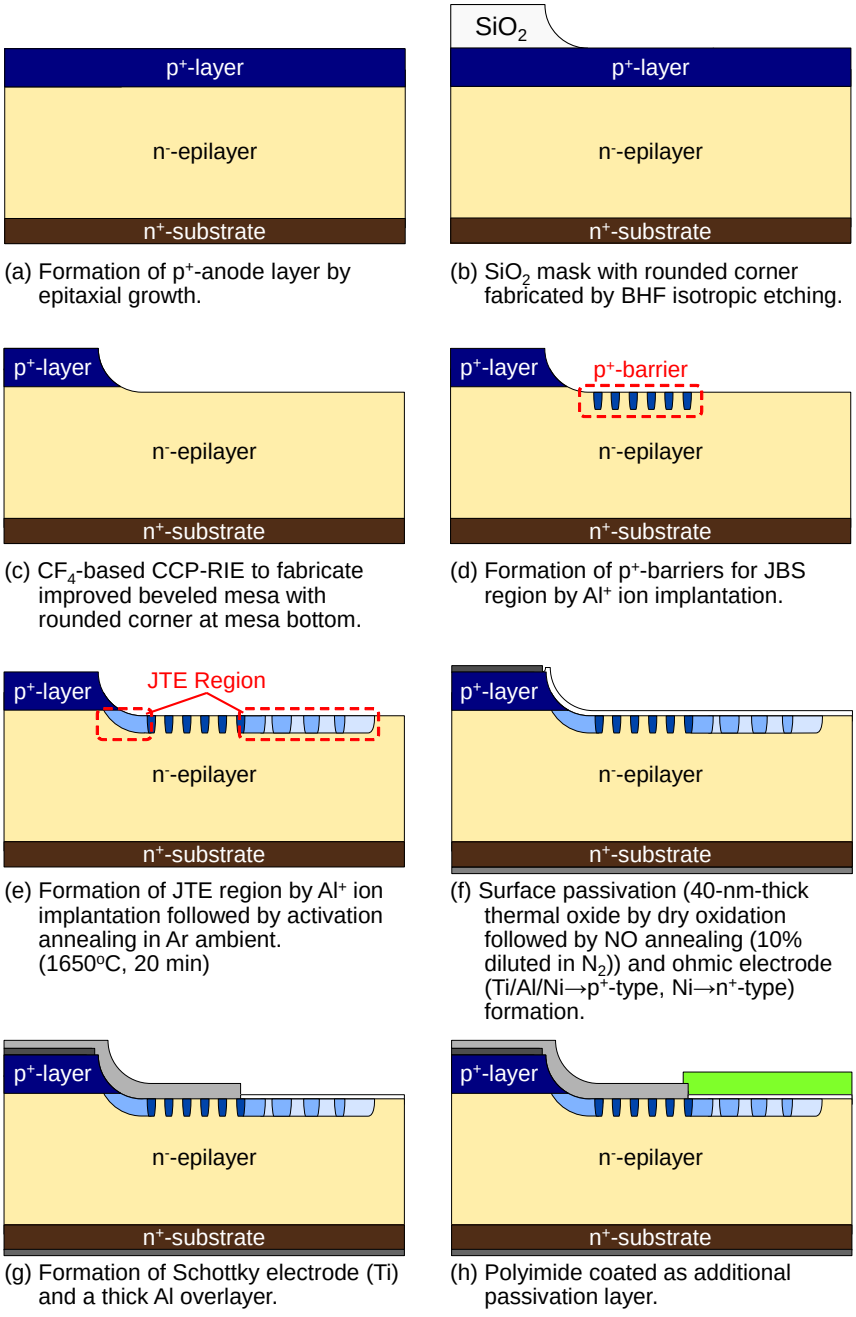
and it is only used during the analysis of snapback voltage (Section 4.4). For both devices, the epilayer was grown on an n^+-type 8° off-axis 4H-SiC (0001) substrate. To enhance the carrier lifetime in the epilayer for reducing on-resistance during the bipolar operation, lifetime enhancement process via thermal oxidation at 1400°C (Type A: 24 h, Type B: 72 h) was employed.

Figure 4.15 shows the fabrication process of the mesa-type MPS diode in this study. First, the p^+-anode and contact layer were formed on the voltage-blocking layer by epitaxial growth. Here, 2.0-μm-thick p^+-anode layer and 0.2-μm-thick contact layer were formed with concentrations of 1×10^{19} and 1×10^{20} cm^{-3}, respectively. Afterwards, for the device isolation, an improved beveled mesa structure with a mesa height of 2.7 μm was fabricated by reactive ion etching with a CF_4-O_2 chemistry using SiO_2 as an etching mask [15], as used for PiN diodes in Chapter 3. After the mesa fabrication, p^+-barriers (JBS region) and JTE region was formed by Al^+ ion implantation, conditions of which are shown in Tables 3.2 and 4.2, to a depth of 0.8 μm using a SiO_2 mask. According to the device simulation performed in previous section, total implantation dose of 2.0×10^{13} and 2.5×10^{13} cm^{-2} has been used for D_{ring} while keeping the ratio of D_{ring} and D_{space} to be 4 : 1. Following the implantation, activation annealing was done in Ar ambient at 1650°C for 20 min with a carbon cap [16], where nearly all of the implanted species were activated (>95%) in the JBS and JTE region [17]. In addition, due to the extremely low diffusion constants of dopants, implanted profile of Al^+ has not changed even after the 1650°C annealing. For the passivation, 40-nm-thick thermally-grown oxide was formed by dry oxidation at 1300°C, followed by annealing in 10%-diluted NO in N_2 at 1250°C for 70 min. Ti/Al (50/200 nm) and Ni (200 nm) annealed at 1000°C for 2 min in vacuum were used as ohmic contacts on the p^+-anode and cathode, respectively. After the metallization annealing, Ti (200 nm) was formed as a Schottky metal, followed by thick Al overlayer (1.5 μm) to reduce the spreading resistance of the anode metal. At last, a 7.0-μm-thick polyimide was coated as an additional passivation layer.

4.4 Snapback Voltage of MPS Diodes

4.4.1 Introduction

One of the largest issues in the MPS diode or hybrid operating power devices, is the snapback phenomenon. Figure 4.16 shows simulated forward I–V characteristics of an unoptimized mesa-type MPS diode investigated in the following sections. When the operation mode switches from unipolar to bipolar operation, a smooth switching does not occur and a voltage *"spike"* appears just before the switch in operation. In other words, voltage greater than the built-in voltage of PiN diode must be applied before the bipolar operation can start. This snapback phenomenon causes a large problem when multiple devices are operated in parallel. If one of the devices turns to a bipolar mode faster than others, large current will



(a) Formation of p^+-anode layer by epitaxial growth.

(b) SiO_2 mask with rounded corner fabricated by BHF isotropic etching.

(c) CF_4-based CCP-RIE to fabricate improved beveled mesa with rounded corner at mesa bottom.

(d) Formation of p^+-barriers for JBS region by Al^+ ion implantation.

(e) Formation of JTE region by Al^+ ion implantation followed by activation annealing in Ar ambient. (1650°C, 20 min)

(f) Surface passivation (40-nm-thick thermal oxide by dry oxidation followed by NO annealing (10% diluted in N_2)) and ohmic electrode (Ti/Al/Ni→p^+-type, Ni→n^+-type) formation.

(g) Formation of Schottky electrode (Ti) and a thick Al overlayer.

(h) Polyimide coated as additional passivation layer.

Figure 4.15: Schematic illustrations of the fabrication process of SiC MPS diodes.

Table 4.2: Implantation energy and dose to form p^+-barriers in JBS region.

Energy (keV)	Dose (cm^{-2})	Temperature (°C)
700	3.0×10^{13}	RT
520	2.7×10^{13}	RT
360	2.7×10^{13}	RT
270	1.3×10^{13}	RT
150	1.95×10^{15}	500
100	1.56×10^{15}	500
60	1.14×10^{15}	500
30	7.02×10^{14}	500
20	3.9×10^{14}	500
10	3.9×10^{14}	500

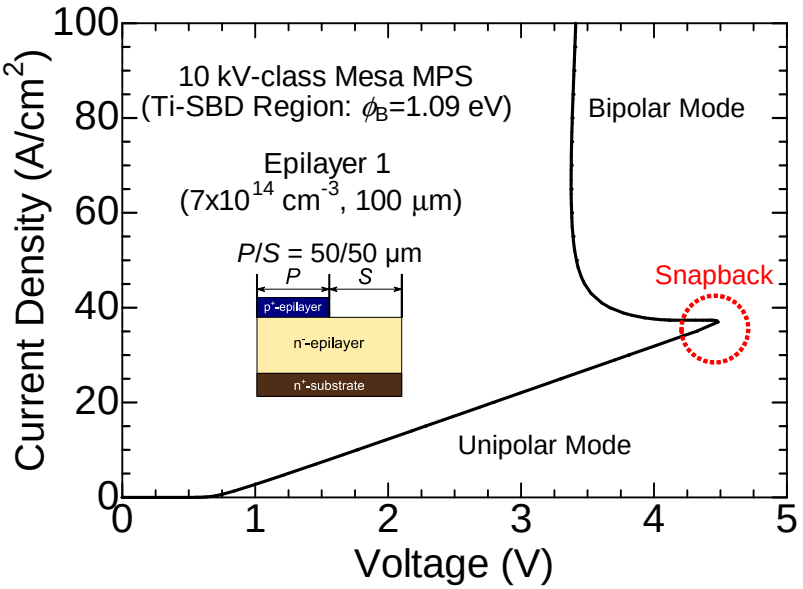


Figure 4.16: Simulated forward I–V characteristics of an unoptimized mesa-type MPS diode.

flow into a single device and can result in a catastrophic failure. Therefore, mechanism of the snapback must be precisely investigated to predict and suppress it in a device.

The snapback phenomenon occurs due to the lateral current flow under the p^+-anode as shown in Fig. 4.17. In Fig. 4.17, dashed arrows show the electron current flow during the unipolar operation. As the current increases, the lateral electron current flow causes voltage drop between p^+-anode and n^--blocking layer. When the voltage drop exceeds the built-in voltage of pn-junction, holes are injected from the p^+-anode and the bipolar operation starts. However, in an unoptimized structure, the applied voltage to the pn-junction is smaller than the applied voltage to the device itself and the snapback phenomenon appears.

This snapback phenomenon has been intensively studied in Si reverse-conducting IGBT (RC-IGBT) structure where an additional n-buffer layer exists between the p^+-anode and n^--blocking layer [18]. In this case, one-dimensional lateral current flow inside the n-buffer layer is assumed to obtain the lateral distribution of the voltage drop between p^+-anode and n-buffer layer. In the case of MPS diode, however, two-dimensional lateral current flow must be considered and the analysis used in RC-IGBT cannot be applied. Therefore, an accurate analysis of the snapback phenomenon in MPS diodes can be performed only using a two-dimensional numerical device simulation. However, because such a device simulation will require a large calculation time, a simple analytical model of the snapback phenomenon in MPS diodes will have a large impact on designing and analyzing such a power device.

In this section, the snapback phenomenon is analytically modeled by using a JBS current-distribution model proposed in this study. Analytical results of snapback voltage are compared with the results of numerical device simulation, and from fabricated MPS diodes. Furthermore, designing guidelines toward a snapback-free MPS diode is presented.

4.4.2 Analytical Modeling of Snapback Voltage

Toward the analytical modeling of snapback phenomenon, a JBS current-distribution model is proposed in this study. In this model, two-dimensional current flow during the unipolar operation is assumed to be divided into two parts as shown in Fig. 4.18; the current spreading region (Region 1) and the uniform current flow region (Region 2). This current flow model is known to have a good accuracy in simulating the on-resistance of JBS diode [19]. In this study, this current flow model is applied for the analysis of snapback phenomenon of a MPS diode.

In a mesa-type MPS diode with half-PiN width of P and half-SBD width of S (Fig. 4.18), the specific on-resistance of Region 1 ($R_{1\mathrm{sp}}$) and Region 2 ($R_{2\mathrm{sp}}$) during the unipolar operation can be expressed as follows [19].

$$R_{1\mathrm{sp}} = \rho_{\mathrm{D}}(P+S)\tan\theta \cdot \ln\left(\frac{P+S}{S}\right) \tag{4.10}$$

$$R_{2\mathrm{sp}} = \rho_{\mathrm{D}}(d - P\tan\theta). \tag{4.11}$$

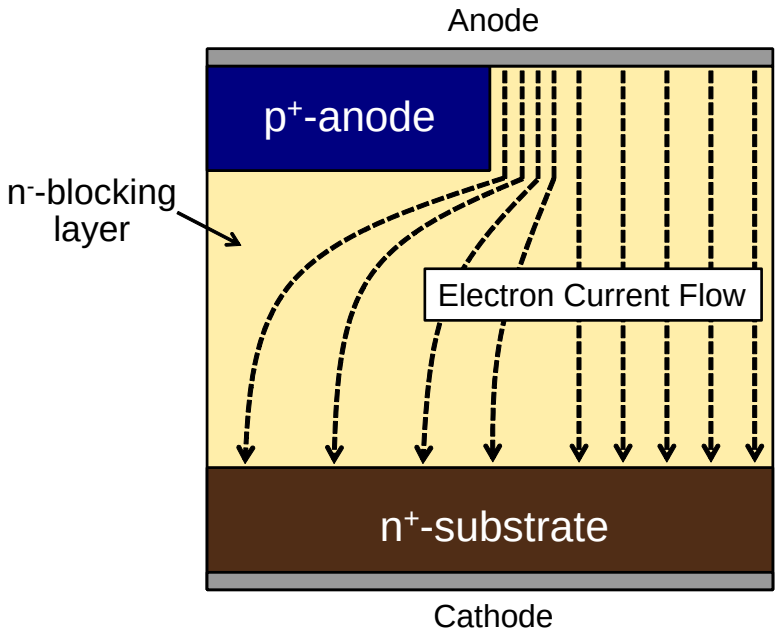


Figure 4.17: Schematic figure of an electron current flow in the unipolar operation mode for a planar MPS diode.

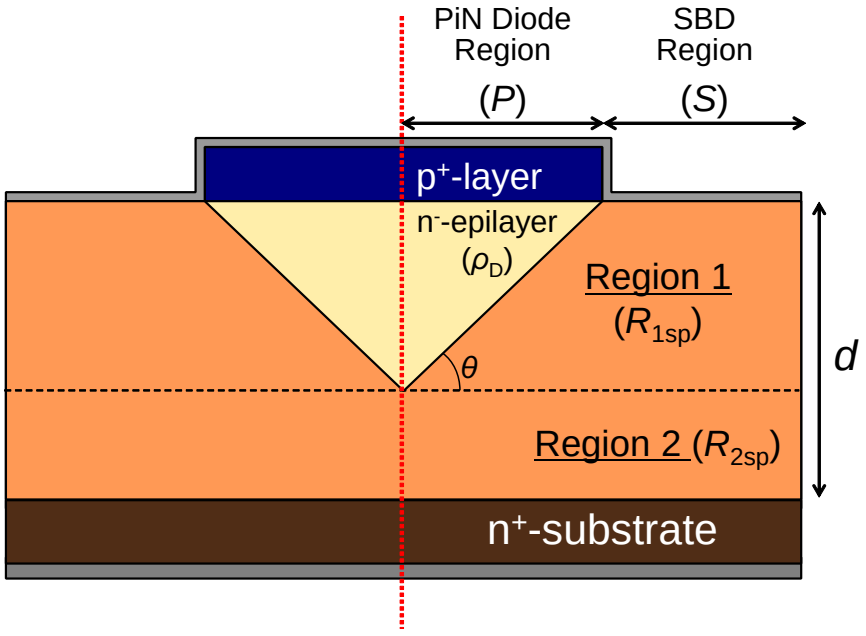


Figure 4.18: Schematic illustration of the approximated electron current flow in the JBS current-distribution model.

Here, ρ_{D} and d are the resistivity and thickness of the voltage-blocking layer, and θ is the current spreading angle. Using these resistance components, the specific on-resistance of MPS diode itself during the unipolar operation (R_{ON}) can be expressed as follows.

$$R_{\mathrm{ON}} = R_{1\mathrm{sp}} + R_{2\mathrm{sp}} + R_{\mathrm{sub}} + R_{\mathrm{c}}. \tag{4.12}$$

Here, R_{sub} and R_{c} are the resistance of n^+-substrate and the contact resistance. However, because the resistance of voltage-blocking layer is extremely large in a UHV device, R_{sub} and R_{c} can be neglected. Therefore, the forward voltage drop of MPS diode (V_{F}) at a current density of J_{F} during the unipolar operation can be expressed by the following equations.

$$V_{\mathrm{F}} = V_{\mathrm{Sch}} + (R_{1\mathrm{sp}} + R_{2\mathrm{sp}})J_{\mathrm{F}} \tag{4.13}$$

$$V_{\mathrm{Sch}} = \phi_{\mathrm{B}} + \frac{kT}{q} \cdot \ln\left(\frac{P+S}{S} \cdot \frac{J_{\mathrm{F}}}{A^* T^2}\right). \tag{4.14}$$

Here, ϕ_{B}, A^*, T are the Schottky barrier height, effective Richardson's constant (146 $\mathrm{A/cm^2 \cdot K^2}$ for SiC), and absolute temperature, respectively. In this equation, V_{Sch} represents the voltage drop across the Schottky barrier. Using these equations, the voltage drop between p^+-anode and n^--blocking layer by lateral electron current flow can be analyzed.

As the electron current flow increases, the lateral current flow produces lateral distribution of voltage drop across the junction of p^+-anode and n^--blocking layer. This voltage drop becomes largest at the center of p^+-anode while considering the electron current flow from the SBD region at the other side of p^+-anode. The junction voltage across the p^+-anode center (V_{J}) can be expressed as follow.

$$V_{\mathrm{J}} = V_{\mathrm{Sch}} + R_{1\mathrm{sp}} J_{\mathrm{F}}. \tag{4.15}$$

When a sufficient voltage drop is produced, the p^+-anode starts injecting holes and when the bipolar current exceeds the unipolar current, snapback occurs for an unoptimized structure. Assuming $V_{\mathrm{J}} = V_{\mathrm{Bi}}$ to be the junction voltage when the snapback occurs, unipolar current density at snapback (J_{snap}) can be written as follow.

$$J_{\mathrm{snap}} = \frac{V_{\mathrm{Bi}} - V_{\mathrm{Sch}}}{R_{1\mathrm{sp}}} = \frac{V_{\mathrm{Bi}} - V_{\mathrm{Sch}}}{\rho_{\mathrm{D}}(P+S)\tan\theta \cdot \ln\left(\frac{P+S}{S}\right)}. \tag{4.16}$$

Therefore, snapback voltage (V_{snap}) can be written as follow.

$$\begin{aligned} V_{\mathrm{snap}} &= V_{\mathrm{Sch}} + (R_{1\mathrm{sp}} + R_{2\mathrm{sp}})J_{\mathrm{snap}} \\ &= V_{\mathrm{Sch}} + (V_{\mathrm{Bi}} - V_{\mathrm{Sch}}) \left\{ 1 + \frac{d - P\tan\theta}{(P+S)\tan\theta \cdot \ln\left(\frac{P+S}{S}\right)} \right\}. \end{aligned} \tag{4.17}$$

When P and S are normalized to the voltage-blocking layer width d, equation (4.17) can be also expressed as follows.

$$V_{\mathrm{snap}} = V_{\mathrm{Sch}} + (V_{\mathrm{Bi}} - V_{\mathrm{Sch}}) \left\{ 1 + \frac{1 - r_{\mathrm{P}}\tan\theta}{(r_{\mathrm{P}} + r_{\mathrm{S}})\tan\theta \cdot \ln\left(1 + \frac{r_{\mathrm{P}}}{r_{\mathrm{S}}}\right)} \right\}. \tag{4.18}$$

Here, $r_P = P/d$ and $r_S = S/d$.

From equation (4.18), one important statement can be made: The snapback voltage depends mainly on r_P and r_S, and resistivity of voltage-blocking layer (ρ_D) does not affect its value. Therefore, regardless to the doping concentration of voltage-blocking layer, V_{snap}–r_P, r_S relationship obtained in one voltage-blocking layer structure can be used for other structures, too.

Furthermore, in this JBS current distribution model, a designing guideline for snapback-free MPS diodes can be predicted. Because the snapback phenomenon occurs when $V_{snap} > V_{Bi}$, it can be suppressed by making $V_{snap} = V_{Bi}$. This condition can be realized when $R_{2sp} = 0$, or when there are region where unipolar current is not flowing and PiN diode/SBD are operating in parallel. From $R_{2sp} = 0$, the following condition can be obtained for the condition of snapback-free MPS.

$$\frac{P}{d} = r_P > \frac{1}{\tan\theta}. \tag{4.19}$$

Therefore, the snapback phenomenon can be controlled by changing the P width against the voltage-blocking layer thickness d. The value of θ will be obtained by fitting the equation to the simulation result in the following section. Furthermore, validity of this model will be evaluated by investigating effect of other parameters such as S or temperature.

4.4.3 Simulation Results of Snapback Voltage

In this section, the snapback phenomenon is analyzed using a numerical device simulation, and is compared with the analytical model proposed in the previous section. Figure 4.19 shows the schematic illustration of the mesa type MPS diode assumed in the simulation. The simulated device consist of half the width of PiN and SBD region. For the Schottky metal, a titanium ($\phi_B = 1.09$ eV) has been employed [14]. Using a current sweep with a slow ramp rate of 100 A/sec, quasi-stationary forward I–V characteristics are simulated. During the simulation, three types of voltage-blocking layers were assumed which are summarized in Table 4.3. Epilayer 1 is for the 10 kV-class MPS diode where 100-μm-thick voltage-blocking layer is used. For Epilayer 2, 150-μm-thick layer is used for the 15 kV-class MPS diode. Both of the doping concentration were optimized to obtain the lowest unipolar on-resistance by calculation performed in the previous section. On the other hand, Epilayer 3 is an unoptimized epilayer where 100-μm-thickness and a low doping concentration of 1×10^{14} cm^{-3} has been assumed for the comparison with Type A epilayer. For all of the epilayers, a carrier lifetime of 10 μs was used for the voltage-blocking layer, which is a reasonable value after the deep-level reduction process.

Figure 4.20 shows the simulated forward I–V characteristics of 10 kV-class MPS diodes (Epilayer 1) with various PiN-diode-region widths (P). Here, Schottky-region width (S) has been kept the same as that of P. With the increase of P-width, V_{snap} has decreased and at a P-width of 150 μm, the snapback phenomenon has disappeared. Figure 4.21 shows the r_P

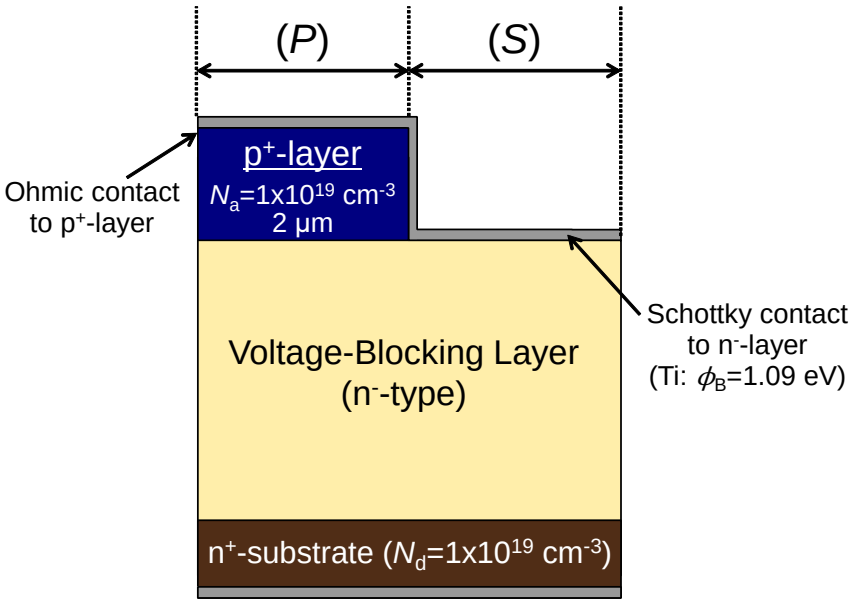


Figure 4.19: Schematic illustration of the mesa type MPS diode assumed in the simulation.

Table 4.3: Doping concentration and thickness of the voltage-blocking layer used in the simulation of snapback phenomenon in MPS diode.

Epilayer	Doping Concentration	Thickness
Epilayer 1	$N_{\mathrm{d}} = 7 \times 10^{14}$ cm^{-3}	100 μm
Epilayer 2	$N_{\mathrm{d}} = 4.5 \times 10^{14}$ cm^{-3}	150 μm
Epilayer 3	$N_{\mathrm{d}} = 1 \times 10^{14}$ cm^{-3}	100 μm

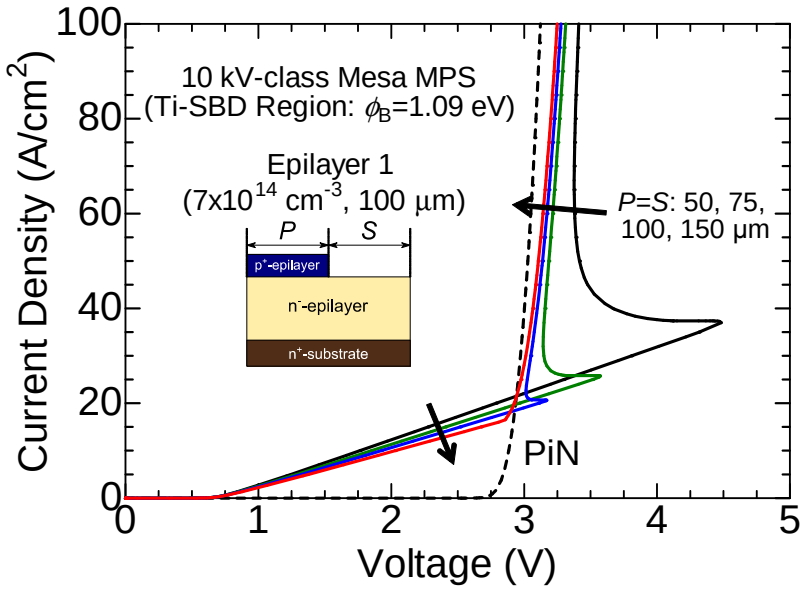


Figure 4.20: Simulated forward I–V characteristics of 10 kV-class MPS diodes (Epilayer 1) with various PiN diode region widths (P).

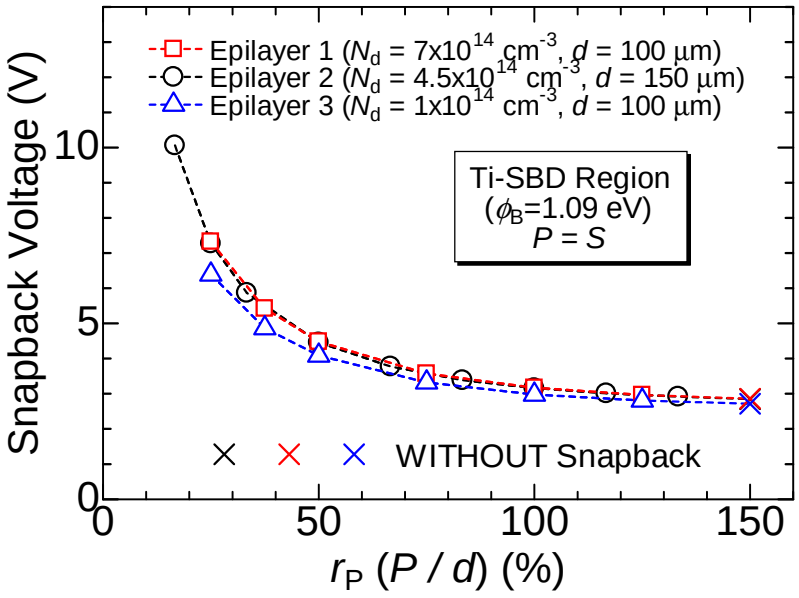


Figure 4.21: Simulated r_P (P/d) dependence of snapback voltage (V_{snap}) for MPS diodes with different voltage-blocking layer structures.

(P/d) dependence of V_{snap} for MPS diodes with different voltage-blocking layer structures. Here, results shown in ($\times$) indicate the MPS diodes without a snapback phenomenon, and the value shows where the bipolar operation started. As it was predicted in the previous section, r_{P} dependence of V_{snap} has not changed by voltage-blocking layer resistivity especially for Epilayer 1 and 2. Although simulation results for Epilayer 3 exhibit differences compared with the others, its difference is very small especially at large r_{P}. Furthermore, the snapback phenomenon has disappeared at $r_{\mathrm{P}} = 150\%$ for all of the epilayers.

To compare the simulation results with the analytical model, the current spreading angle θ and V_{Sch} must be determined. In particular, to determine V_{Sch}, J_{snap} must be determined first. In this study, for the determination of V_{Sch}, J_{snap} is first approximated by assuming $V_{\mathrm{Sch}} = 0$ V and $\theta = 45^{\circ}$ in equation (4.16). Because V_{Sch} is just a few tenths volts, the value of J_{snap} will not change largely by this approximation due to the large resistivity of UHV devices. After the approximation of J_{Sch}, V_{Sch} is derived for the calculation of V_{snap}, where θ will be now determined by fitting analytical V_{snap} to the simulation using θ as a fitting parameter. Figure 4.22 shows the fitted r_{P} dependence of V_{snap} together with the simulation results. Here, the built-in voltage (V_{d}) was used for V_{Bi}, and it was found that the analytical model shows good agreement with simulation at $\theta = 42^{\circ}$. In addition, Fig. 4.23 shows the r_{P} dependence of J_{snap} for Epilayer 1 and 2 calculated now using V_{Sch} and the obtained θ. Although V_{Sch} was calculated using an approximated J_{snap}, the calculated J_{snap} taking account of V_{Sch} has shown a good agreement with the simulation.

Although MPS diodes with Epilayer 1 and 2 had a similar V_{snap} at a given r_{P}, Epilayer 3 had a smaller value than their values. This is probably due to the difference of V_{Bi}. To realize a complete bipolar operation in a MPS diode, the bipolar current from p^{+}-anode must exceed the unipolar current flowing in that voltage. Because Epilayer 3 is not optimized for unipolar operation, unipolar current which the bipolar current needs to overcome is relatively smaller for Epilayer 3. Therefore, V_{Bi} required for Epilayer 3 is smaller than that of Epilayer 1 and 2, resulting in a smaller value of V_{snap}.

From equation (4.19), snapback-free MPS can be realized when $r_{\mathrm{P}} > 111\%$ in the analytical model ($\theta = 42^{\circ}$). Therefore, in Fig. 4.22, the analytical snapback-free region is shown in a dashed line which corresponds to the value of V_{d}. However, the snapback phenomenon has occurred in the device simulation at least up to $r_{\mathrm{P}} = 133.3\%$ in Epilayer 2, although it should not occur according to the analytical model. This is due to the linear approximation of the current flow inside the voltage blocking used in this model (Fig. 4.18). Although the main electron current flow may be similar to that of Fig. 4.18, the actual electron current flow is more complicated and voltage drop caused by the electron current flow can exist outside the approximated area. This can cause additional voltage drop outside the approximated area, which will induce the snapback phenomenon. However, because the main tendency of r_{P} dependence for both V_{snap} and J_{snap} are showing excellent agreement between the analytical model and simulation, this analytical model is useful for predicting the snapback phenomenon. Furthermore, although Epilayer 3 had smaller V_{snap} than Epilayer 1

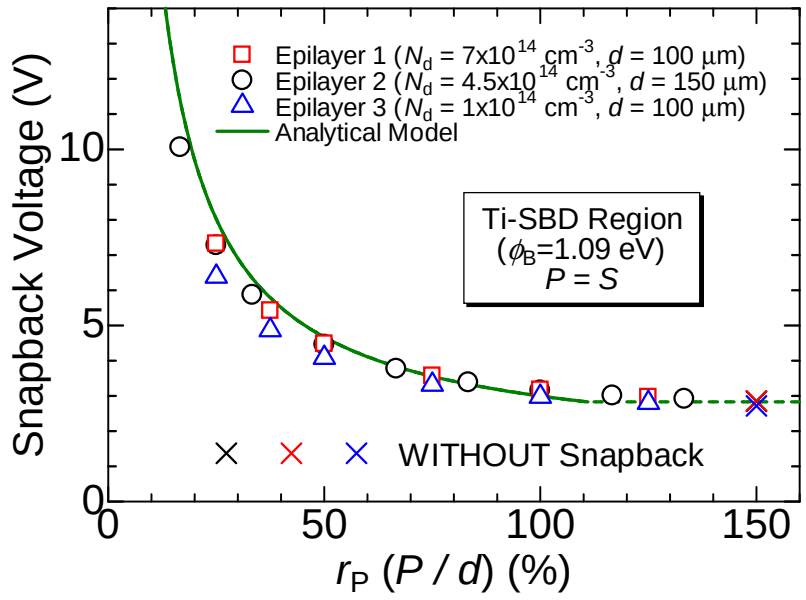


Figure 4.22: Simulated and analytical r_P dependence of V_{snap}. Analytical results best fits the simulation at a current spreading angle θ of 42°.

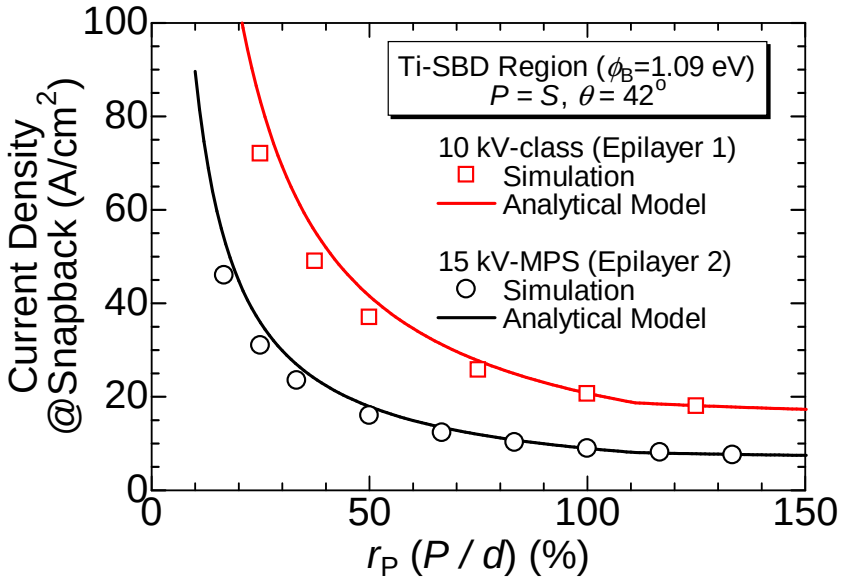


Figure 4.23: Simulated and analytical r_P dependence of snapback current (J_{snap}).

and 2, the value of r_{P}, at which the snapback-free MPS can be realized, is very similar to that of Epilayer 1 and 2. This can also be concluded from equation (4.19) because r_{P} at which the snapback-free MPS can be realized only depends on the current spreading angle θ, which should not largely differ from that of Epilayer 1 and 2.

4.4.4 Experimental Results of Snapback Voltage

In this section, the snapback phenomenon is investigated experimentally by fabricated SiC MPS diodes. Figure 4.24 shows the (a) schematic structure and (b) an optical picture of the fabricated MPS diode. Devices were fabricated using fabrication process described in Section 4.3, but without JTE implantation. Here, SBD regions with and without p^+-barriers have been fabricated. For a SBD region with p^+-barriers, the region will be called "JBS region" from now on. In this section, all of the analyzed MPS diodes use a SBD region if it is not specified. In this study, all of the MPS diodes have anode geometry with p^+-anode inside the SBD region to make unipolar current flow from all of the sides of the p^+-anode. When the anode geometry is not specified, all of the experimental results in this section are from MPS diodes with a square anode and square SBD region as shown in Fig. 4.24(b).

Figure 4.25 shows the forward I–V characteristics measured from fabricated MPS diodes with $P = S = 50$ μm for Type A and B epilayers (Table 4.1). These I–V characteristics were measured by using a current sweep. Because r_{P} is too small for these devices, the snapback phenomenon has occurred in both devices. Figure 4.26 shows the measured r_{P} dependence of V_{snap} for MPS diodes with different P/S ratios, and Fig. 4.27 shows the forward I–V characteristics of MPS diodes with Type A epilayer for $P = 50, 100, 150$ μm. Here, results shown in ($\times$) indicate the MPS diodes without the snapback phenomenon, and the value shows the voltage where the bipolar operation started. As it was predicted in the analytical modeling and simulation, the V_{snap} has decreased with increasing r_{P}. For Type A epilayer, the snapback phenomenon has nearly disappeared at $r_{\mathrm{P}} = 105\%$, and for $r_{\mathrm{P}} \geq 158\%$, it has completely vanished and parallel operation of SBD and PiN diode has been realized. For Type B epilayer, however, the snapback phenomenon has disappeared at $r_{\mathrm{P}} = 74\%$. Figure 4.28 shows the forward I–V characteristics of MPS diode with Type B epilayer for $r_{\mathrm{P}} = 74\%$ ($P = 200$ μm). Due to the thick epilayer used here, larger forward voltage must be applied to realize enough conductivity modulation. Therefore, although the snapback phenomenon may be occurring, it could not be explicitly observed because the effect of conductivity modulation is still low in this voltage. In addition, for both epilayers, the snapback voltage has decreased as the P/S ratio increased (reducing S-width at a given P-width). This will be discussed in the following section.

The effect of using a JBS region on V_{snap} has been investigated. Figure 4.29 shows forward I–V characteristics of MPS diodes with and without p^+-barriers. By the introduction of p^+-barriers, V_{snap} has greatly decreased in both of the diodes. Furthermore, unipolar on-resistance has increased by the introduction of the JBS region. This reduction of V_{snap} is

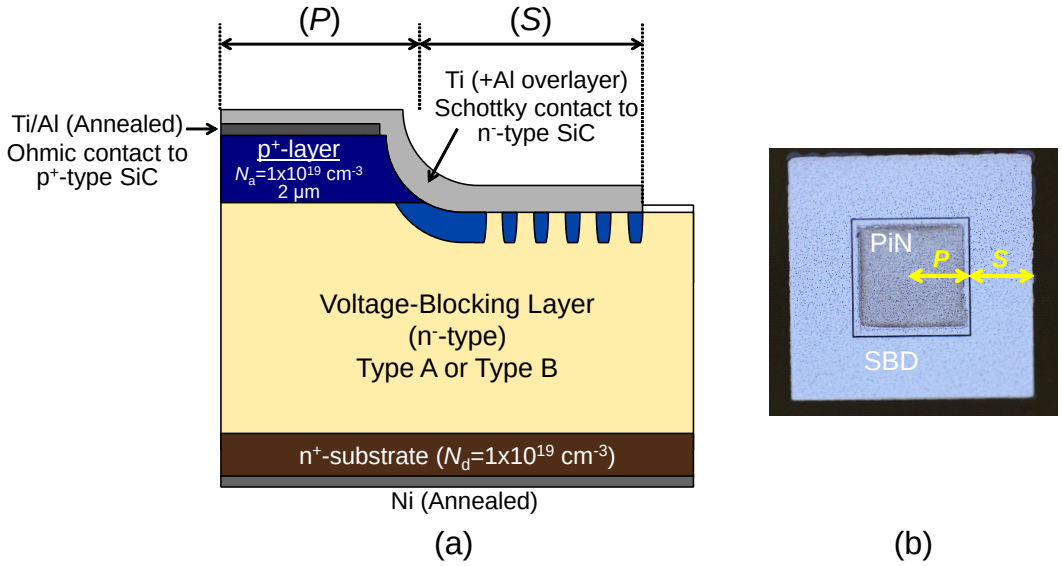


Figure 4.24: (a) Schematic structure of the fabricated MPS diode for analysis of forward characteristics. (b) Optical picture of a fabricated MPS diode.

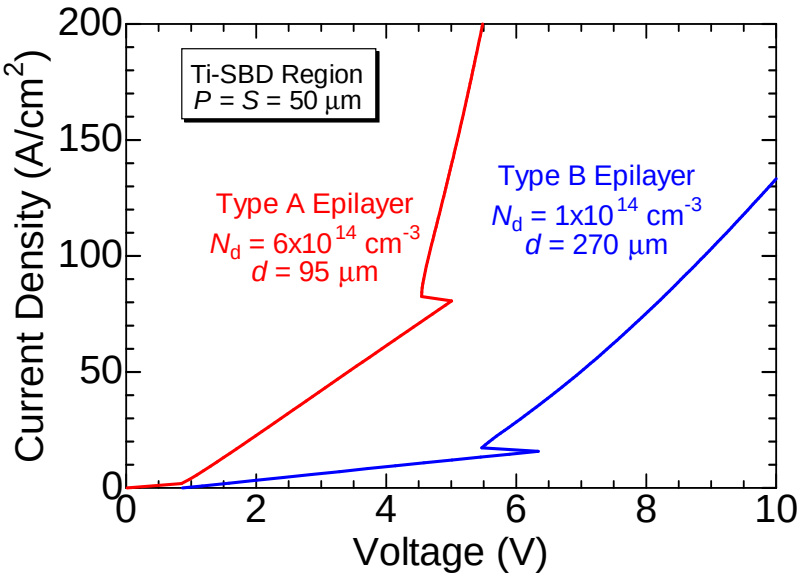


Figure 4.25: Measured forward I–V characteristics from fabricated MPS diodes with $P = S = 50$ μm for Type A and B epilayers.

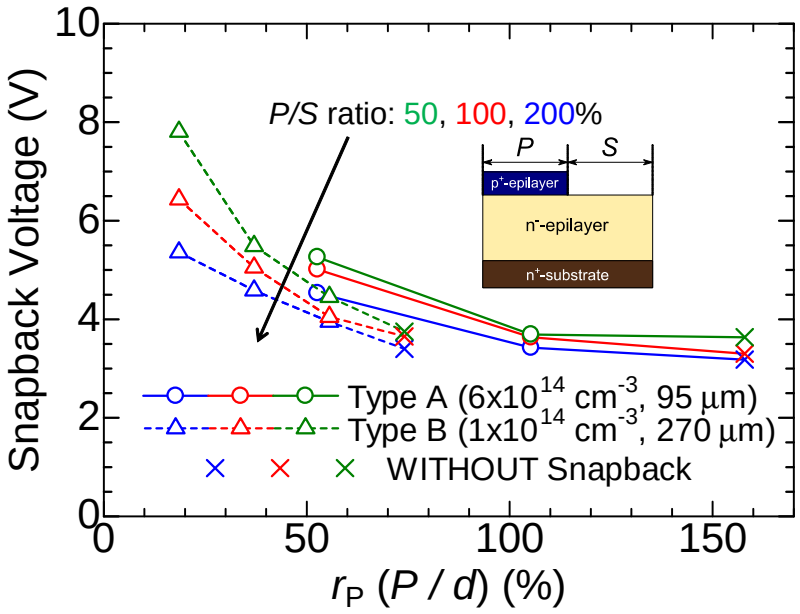


Figure 4.26: Experimentally obtained r_{P} dependence of V_{snap} for MPS diodes with different P/S ratios.

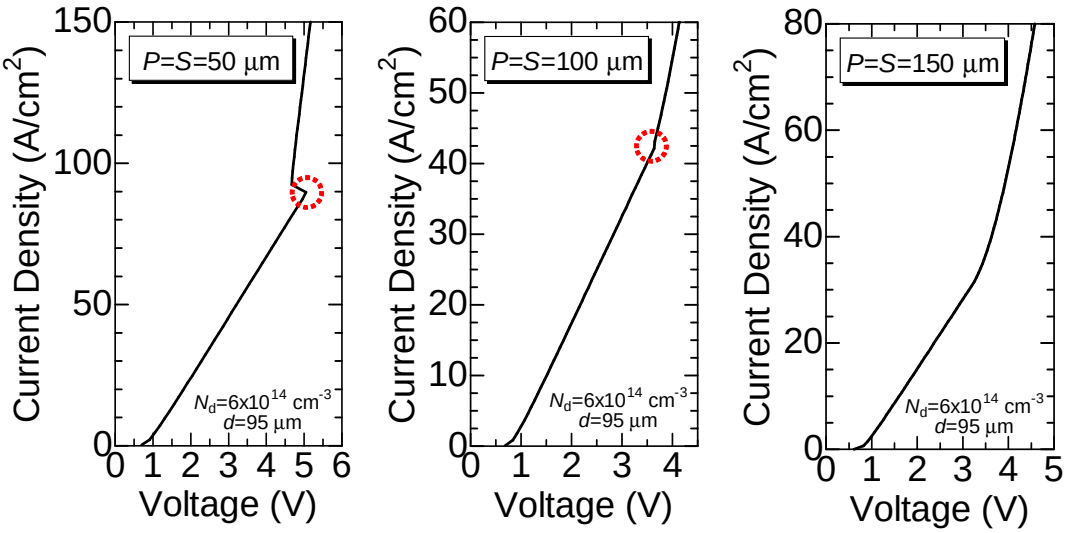


Figure 4.27: Forward I–V characteristics of MPS diodes with Type A epilayer for P-width of 50, 100, 150 μm.

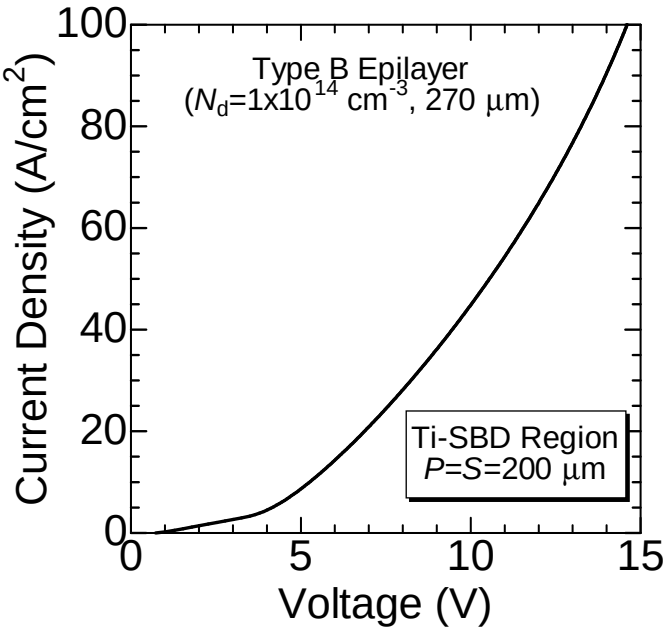


Figure 4.28: Forward I–V characteristics of MPS diode with Type B epilayer for P-width of 200 μm.

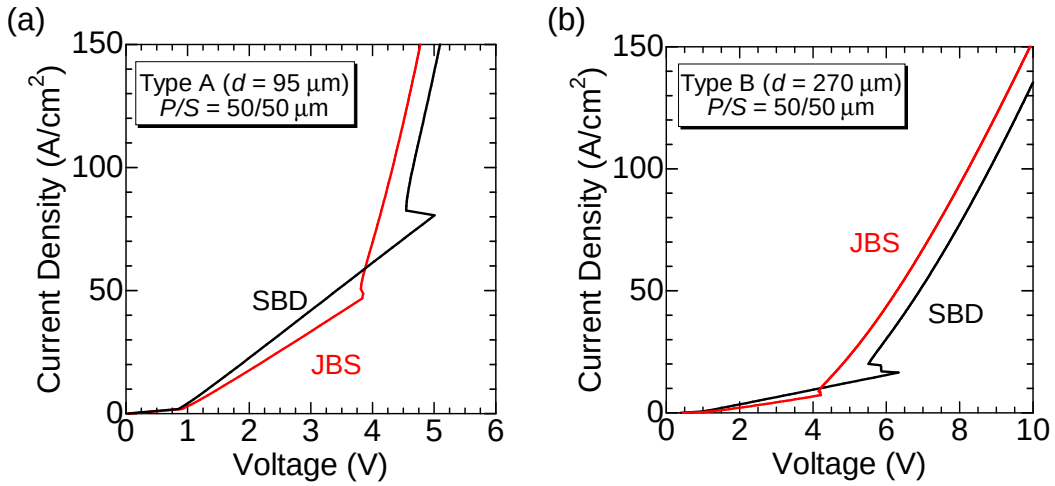


Figure 4.29: Forward I–V characteristics of MPS diodes with (JBS) and without (SBD) p$^+$-barriers for P-width of 50 μm.

due to the additional voltage drop occurring at the p^+-barriers. In a JBS diode, additional conducting channel resistance is induced between the p^+-barriers, which can be observed from the unipolar on-resistance. This additional voltage drop will increase the voltage drop induced by the lateral electron current flow, which reduces V_F needed to start the bipolar operation. Although introduction of p^+-barriers increases the unipolar on-resistance, it can be minimized by the optimization of p^+-barrier layout. For the bipolar operation, MPS diodes with the JBS region have larger forward current at a given voltage. This is due to the difference of voltage applied to the p^+n junction, and when a snapback-free operation is realized, this large difference will not occur. Because the JBS region is required for SiC in terms of reverse characteristics, this positive effect to V_{snap} is a desirable feature.[1] Therefore, toward the hybrid operation of MPS diodes, the JBS region is an indispensable technology that must be adopted and optimized for the MPS diode.

Figure 4.30 shows the temperature dependence of V_{snap}. Figure 4.30(a) demonstrates the difference for MPS diodes with SBD or JBS region. At any temperature investigated, MPS diodes with the JBS region had lower snapback voltage than diodes with the normal SBD region. Figure 4.30(b) shows the difference for MPS diodes with SBD region with different S-widths. Similar to Fig. 4.30(a), snapback voltage decreased with increasing temperature. In all of the cases, "slope" of the V_{snap} reduction was very similar. From equation (4.18), parameters that have temperature dependency in V_{snap} are V_{Sch} and V_{Bi}. Because addition of p^+-barriers or difference of S-width does not change these values in general, the temperature dependence of V_{Sch} and V_{Bi} has directly appeared in the temperature dependence of snapback voltage. Although V_{Sch} differs by existence of p^+-barriers or by difference of S-width (J_F differs by structure), its contribution to the V_{Sch}-value is comparably small. Therefore, tendency of the temperature dependence of snapback voltage will be the same for all of the MPS diodes: Increasing the temperature will reduce the snapback voltage. Further investigation by comparing it with the analytical model is given in the following section.

4.4.5 Discussion

In this section, difference of V_{snap} by changing the MPS diode structure or measurement temperature is discussed using the proposed model, and is compared with the device simulation and experiments to reveal the problem which the model may contain. Furthermore, validity and inaccuracy of the proposed model are discussed.

Figure 4.31 shows the r_P dependence of V_{snap} obtained by the analytical model (solid line), device simulation (closed symbols), and experiment (open symbols). As previously explained, the tendency of V_{snap} reduction with increasing r_P was observed in all three methods. However, experimental results does not completely agree with the analytical model and simulation. For the snapback voltage at $r_P \sim 100\%$, the experimental result takes a larger value than that of analytical model and simulation. This is due to the inaccuracies when

[1] At least, negative effects will not occur to the snapback phenomenon.

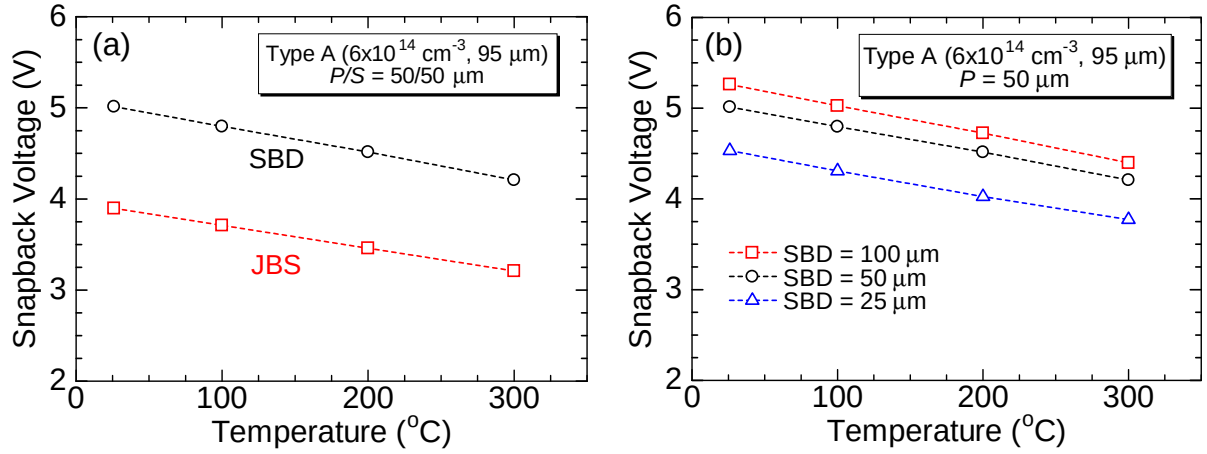


Figure 4.30: Temperature dependence of V_{snap} experimentally obtained. (a) MPS diodes with SBD or JBS region. (b) MPS diodes with different S-width at given P-width of 50 μm.

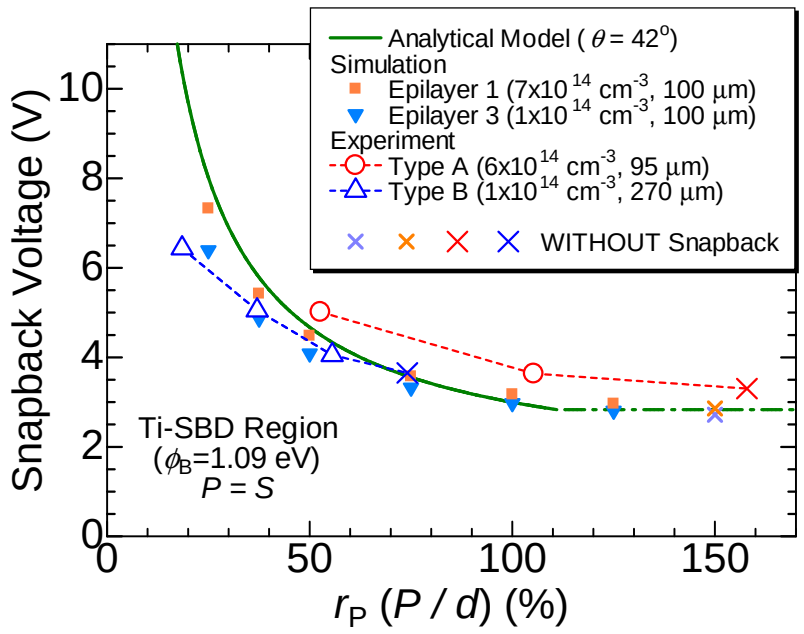


Figure 4.31: r_{P} dependence of V_{snap} for the analytical model (solid line), device simulation (closed symbols), and experiment (open symbols).

simulating bipolar operation. Because conductivity modulation consists of complicated carrier recombination process which has not been precisely investigated in SiC, accurate device simulation of bipolar operation is difficult. Therefore, underestimation of on-resistance occurs in device simulation[2], which also underestimates the V_{Bi} and i.e. V_{snap}. In addition, the analytical model also uses underestimated V_{Bi} (not enough conductivity modulation occurring at $V_{\mathrm{F}} = V_{\mathrm{d}}$ in experiment), which results in underestimation of V_{snap}.

For Type B epilayer, however, its experimental snapback voltage is taking a lower value than analysis and simulation especially at small r_{P}. One of this reason is the accuracy of actual thickness of voltage-blocking layer. Because errors in epilayer thickness can easily change the value of r_{P}, and because the value of V_{snap} can change drastically at small r_{P}, experimental V_{snap} can easily be different from simulation and analysis especially at small r_{P}. In addition, nonlinearity of current spreading (approximation of current spreading angle θ) can also cause differences in the analytical V_{snap}. Furthermore, difference in the unit cell structure of the device may have an impact on V_{snap}. In the device simulation and analytical model, a stripe structure [Fig. 4.32(a)] where unipolar current flow from two side walls contribute to the snapback phenomenon. In the experiment, however, a square structure [Fig. 4.32(b)] was used where unipolar current flow from four side walls contribute to the snapback phenomenon. This difference may change the unipolar current flow and make differences in the snapback phenomenon. For a more accurate device simulation and analysis, a three-dimensional simulation is required.

Figure 4.33 shows the S-width dependence of V_{snap} while fixing P-width to 50 μm. In all of the methods, V_{snap} increased with increasing S-width. From equation (4.10), increasing the S-width reduces the value of R_{1sp}. This will result in increase of J_{snap}, which will increase the V_{snap} in equation (4.17). Although the absolute value of V_{snap} does not agree with each other, this can be due to the inaccuracies in physical properties or from the difference of unit cell structure assumed.

Figure 4.34 shows the temperature dependence of V_{snap} for the MPS diode with Type A epilayer. The temperature dependency in the analytical model was calculated by using temperature dependence of V_{d} and V_{Sch}. During the calculation of V_{Sch}, the temperature term T and J_{F} ($= J_{\mathrm{snap}}$) was varied with the temperature. From Fig. 4.34, although all of the three methods has resulted in reduction of snapback voltage with increasing temperature, the slope of analytical model is smaller than the rest. This indicates that other parameters in equation (4.18) except V_{Bi} ($= V_{\mathrm{d}}$) and V_{Sch} changed by temperature. For example, current spreading angle θ may change by temperature because electron mobility has anisotropy and temperature dependency.

From comparison of the analytical model with the device simulation and experiment as shown in Figs. 4.31, 4.33, and 4.34, the following conclusion can be made for the proposed model.

[2]Can be seen by comparing Figs. 4.18 and 4.20. Fabricated diodes have larger forward voltage drop at a given current.

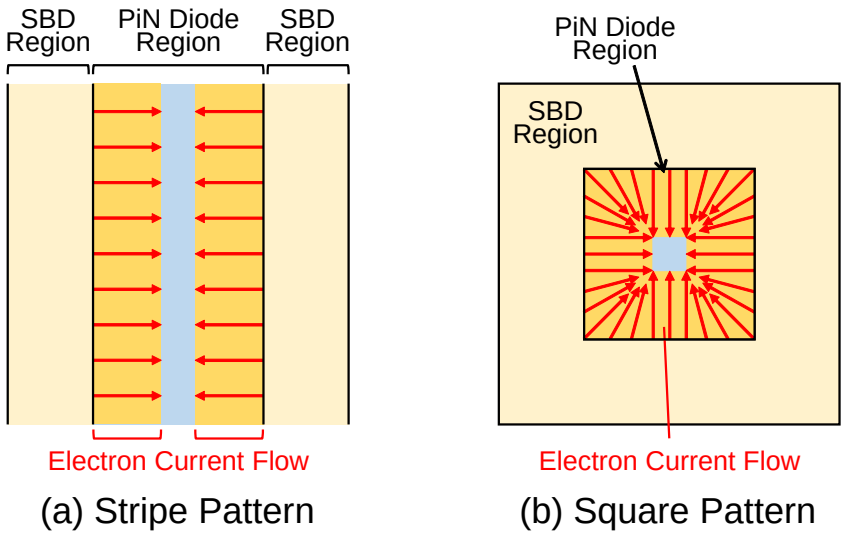


Figure 4.32: Schematic illustration of the unit cell structure and electron current flow for (a) stripe and (b) square patterns.

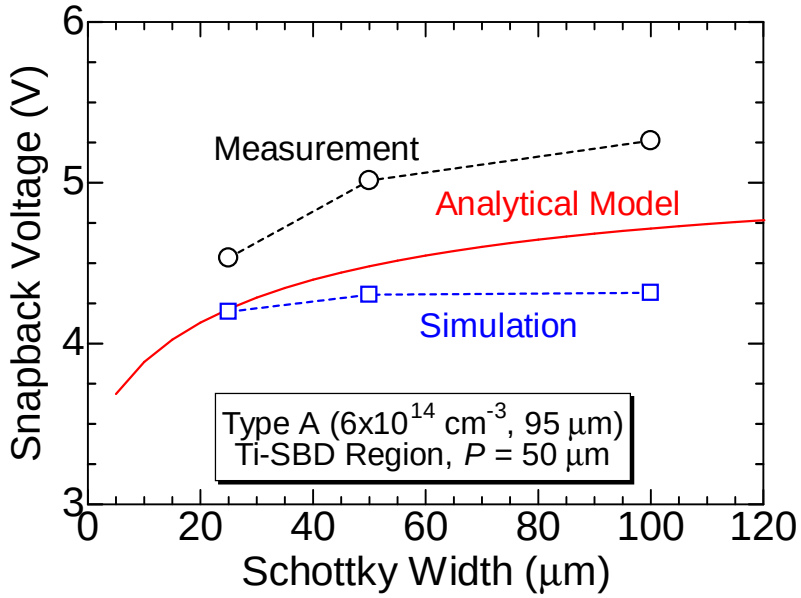


Figure 4.33: S-width dependence of V_{snap} for the analytical model, device simulation, and experiment.

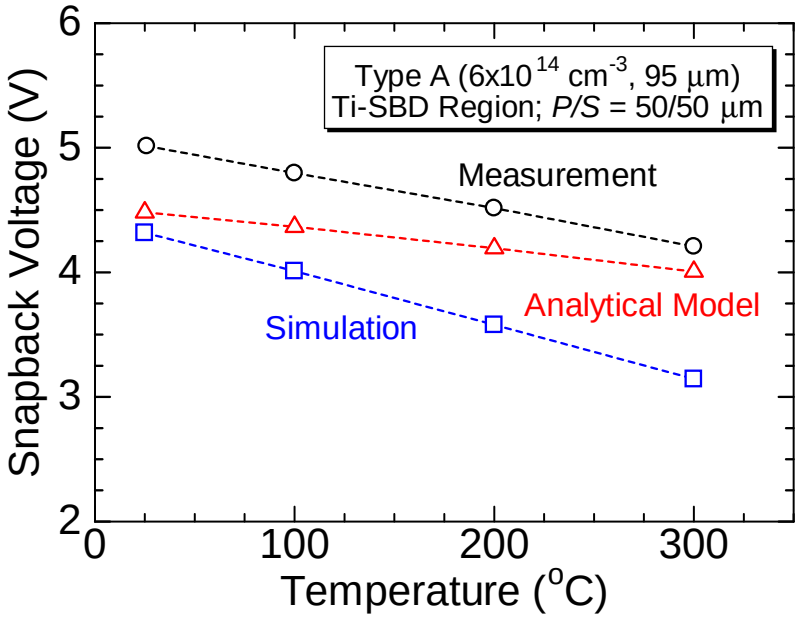


Figure 4.34: Temperature dependence of V_{snap} for the analytical model, device simulation, and experiment.

- Tendency of snapback voltage by changing the device structure and temperature can be accurately reproduced by the model.
- Although an accurate tendency can be obtained, the absolute value of V_{snap} in simulation and experiment cannot be completely reproduced.

The difference of the absolute value of V_{snap} compared with simulation and experiment is mainly due to the accuracy of θ and V_{Bi}. Because MPS diodes utilizing unipolar operation have large unipolar current, using built-in potential V_{d} as V_{Bi} is insufficient and larger voltage must be assigned. For the difference between the experiment and analytical model, in addition to the accuracies of the previous parameters, influence of unit cell structure of the device has to be further investigated. However, this model can be defined as a semi-quantitative model of snapback phenomenon because the value of V_{snap} does not largely differ from simulation and experiment, The analytical model proposed in this study can reproduce the tendency of snapback voltage, and will serve as a simple and powerful tool to understand the physics of snapback phenomenon in a MPS diode.

4.5 Forward Characteristics of MPS Diodes

In this section, forward characteristics of MPS diodes without the snapback phenomenon are investigated. Unipolar and bipolar on-resistance of MPS diodes with various PiN/Schottky structures are experimentally studied and are compared with conventional PiN diodes and JBS diodes. Furthermore, device simulation of static and switching characteristics are conducted to present the design guideline of MPS diode considering hybrid operation.

4.5.1 On-Resistance of MPS Diodes

Schematic structure of the fabricated MPS diodes is the same as that used in the previous section. In this section, Type A epilayer was used as a voltage-blocking layer, and P-width of 150 μm ($r_{\mathrm{P}} = 158\%$) was used to realize the snapback-free operation. In addition, the JBS structure was employed in the SBD region for all of the fabricated MPS diodes investigated in this section.

Figure 4.35 shows the forward I–V characteristics of an MPS diode with $P = S = 150$ μm. In the same figure, measurement results of a PiN diode and JBS diode with the same area are also shown. Here, the MPS diode has the same anode geometry shown in Fig. 4.24, which is the square p^+-anode inside the square JBS region. For unipolar and bipolar operation, MPS diode exhibits larger on-resistance than JBS and PiN diode, respectively. Because the active area of JBS and PiN diode regions in the MPS diode is smaller than the full JBS and PiN diode, this increase of on-resistance is inevitable. Figure 4.36 shows the forward I–V characteristics of MPS diodes with different S-widths while keeping the P-width to 150 μm. When S-width is reduced, the area of JBS region decreases and

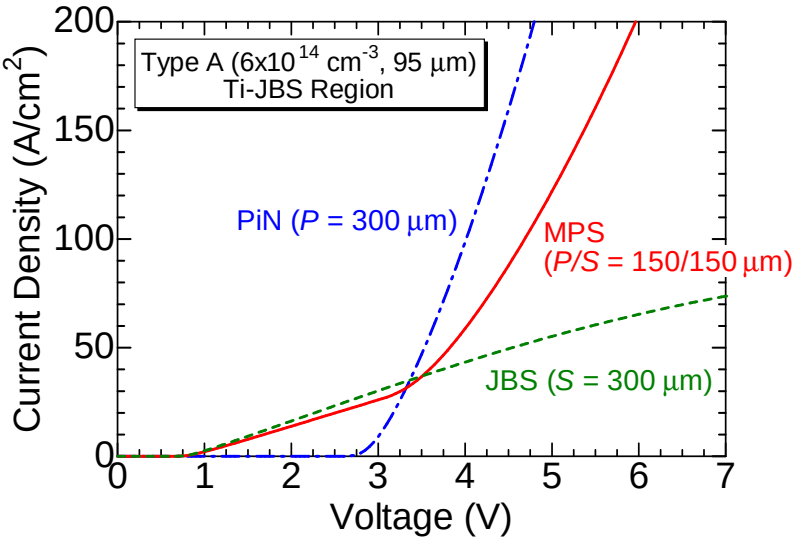


Figure 4.35: Measured forward I–V characteristics of an MPS diode with $P = S = 150$ μm. In the same figure, measurement results of PiN diode and JBS diode with the same area are also shown.

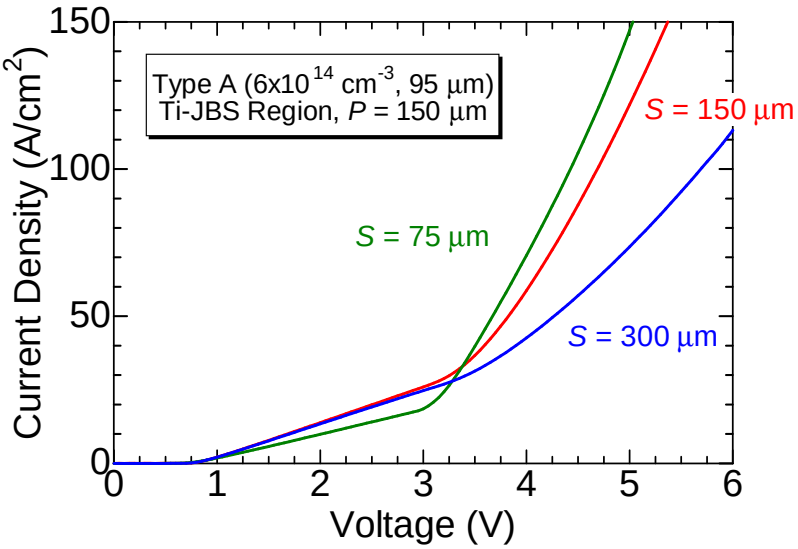


Figure 4.36: Measured forward I–V characteristics of MPS diodes with different S-widths while keeping P-width to 150 μm.

the unipolar on-resistance increased.[3] However, bipolar on-resistance has decreased while reducing the S-width because the ratio of the PiN diode area increases. Therefore, unipolar and bipolar on-resistances are in a trade-off relationship, which can be controlled by the S-width.

Figure 4.37 shows the forward I–V characteristics of MPS diodes with different anode geometry shown in Fig. 4.38. Here, P and S-widths are kept to 150 μm for all of the devices. From Fig. 4.37, the I–V characteristics did not change much by the anode geometry. This can also be explained by the ratio of JBS and PiN diode area of the device. Table 4.4 shows the unit cell area of JBS region (width: S) and PiN diode region (width: P) for three different anode geometries used in this study. Although the absolute value of the area differs, the ratio of JBS and PiN diode area is the same for all, resulting in almost the same I–V characteristics. Furthermore, this result also indicates that the unipolar and bipolar on-resistance can be controlled by the unit cell structure. For example, while using a circular PiN diode region, by changing the circular unit cell structure of JBS region to square, unipolar on-resistance can be reduced due to the larger area of JBS region.

By using a wide implanted p^+-barrier as a p^+-anode layer, planar MPS diodes with an implanted p^+-anode have also been fabricated. Figure 4.39 shows the forward I–V characteristics of MPS diodes with implanted and epitaxial p^+-anode. Here, P and S are set to 150 μm. For unipolar operation, there are no differences between formation process of the p^+-anode layer. However, for bipolar operation, clear conductivity modulation could not be observed until a large forward voltage was applied for implanted p^+-anode. Because both unipolar and bipolar operation must be considered in the MPS diodes in this study, it has been confirmed that MPS diodes with implanted p^+-anode is unsuitable for hybrid operation.

4.5.2 Temperature Dependence of On-Resistance

High temperature measurement of MPS diodes without the snapback phenomenon has been performed to investigate the temperature dependence of unipolar and bipolar operation. Figure 4.40(a) shows the temperature dependence of forward I–V characteristics of MPS diode with P and S-widths of 150 μm, and Fig. 4.40(b) shows the temperature dependence of unipolar (V = 2 V) and bipolar (J = 100 A/cm^2) on-resistance. With increasing temperature, unipolar on-resistance has increased due to the reduced electron mobility. For the bipolar on-resistance, it had a negative temperature coefficient due to the increased carrier lifetime at elevated temperature, which resulted in the increase of conductivity modulation. Because unipolar on-resistance increases with temperature, impact of using hybrid operating MPS diodes at high temperature is relatively small compared with room temperature.

[3]Unipolar on-resistance for S = 300 μm did not differ from S =150 μm probably due to the spreading resistance of the anode metal. When the device area becomes large, an additional resistance is added to the I–V characteristics.

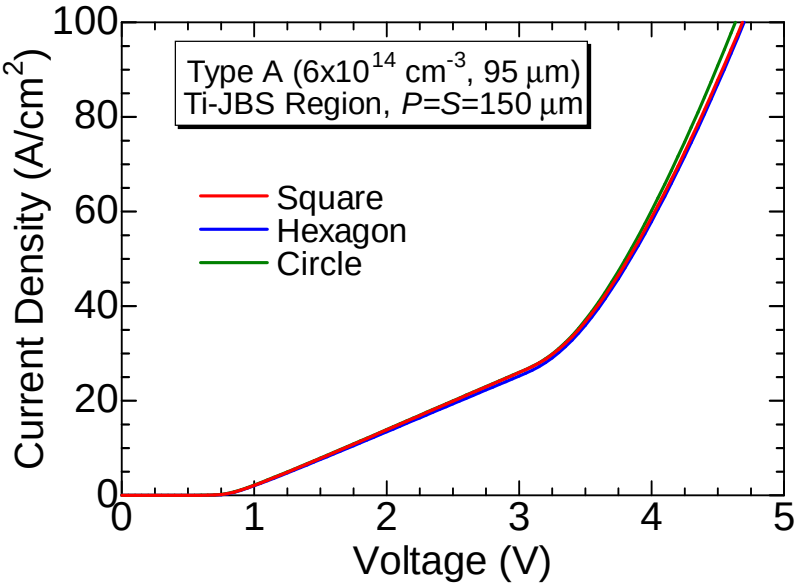


Figure 4.37: Measured forward I–V characteristics of MPS diodes with different anode geometries. Here, P and S-widths were kept to 150 μm.

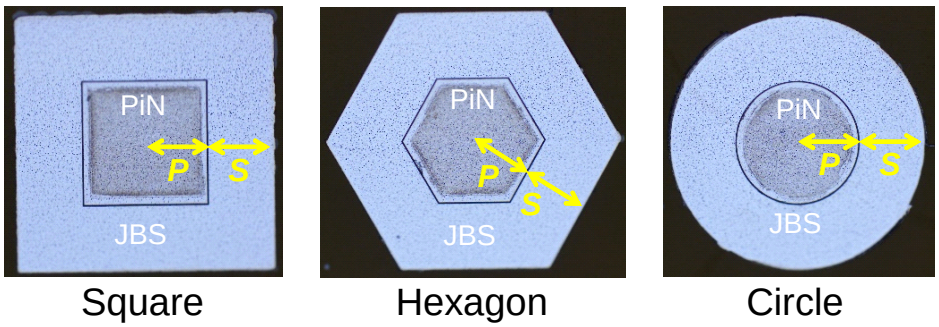


Figure 4.38: Optical picture of different anode geometries measured in this study. These MPS diodes have P- and S-widths of 150 μm.

Table 4.4: Unit cell area of JBS region (A_{JBS}, width: S), PiN diode region (A_{PiN}, width: P), and MPS diode (A_{All}, $A_{\mathrm{PiN}} + A_{\mathrm{JBS}}$). Ratio of PiN and JBS area is also shown.

	Square	Hexagon	Circle
A_{PiN}	$4P^2$	$2\sqrt{3}P^2$	πP^2
A_{JBS}	$4(S^2+2PS)$	$2\sqrt{3}(S^2+2PS)$	$\pi(S^2+2PS)$
A_{All}	$4(P+S)^2$	$2\sqrt{3}(P+S)^2$	$\pi(P+S)^2$
$A_{\mathrm{PiN}}/A_{\mathrm{JBS}}$	$\frac{P^2}{S^2+2PS}$	$\frac{P^2}{S^2+2PS}$	$\frac{P^2}{S^2+2PS}$

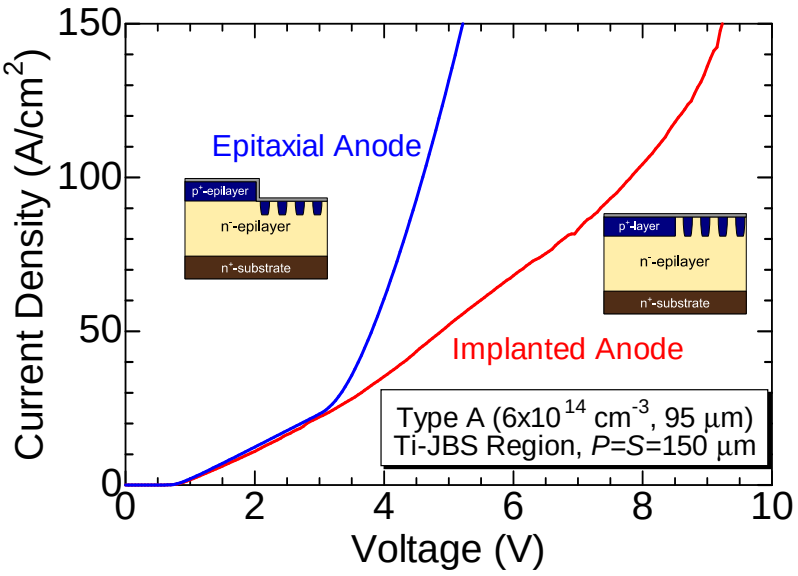


Figure 4.39: Measured forward I–V characteristics of MPS diodes with implanted and epitaxial p^+-anode.

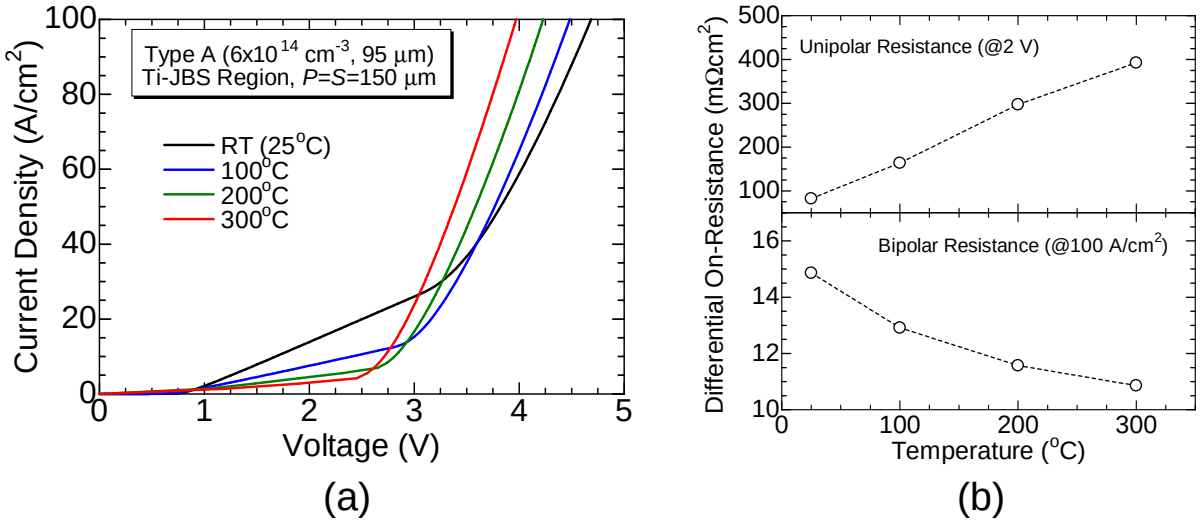


Figure 4.40: (a) Temperature dependence of forward I–V characteristics of an MPS diode with P and S-width of 150 μm experimentally measured. (b) Temperature dependence of unipolar ($V = 2$ V) and bipolar ($J = 100$ A/cm^2) on-resistance.

Therefore, operating temperature must be carefully chosen when using MPS diodes in a hybrid operation.

In addition, MPS diodes with implanted p^+-anode has been characterized at high temperature. Figure 4.41 shows the temperature dependence of forward I–V characteristics of MPS diodes with implanted and epitaxial p^+-anode. Although the implanted p^+-anode MPS diode had extremely small effect of conductivity modulation at room temperature, conductivity modulation effect started to appear at high temperature. Therefore, if the MPS diodes are designed for high temperature operation, using an implanted p^+-anode can become one choice in this case.

4.5.3 Discussion

In this section, device simulation of static and switching characteristics are conducted to further investigate the on-resistance of MPS diodes. Furthermore, design guidelines of an MPS diode considering hybrid operation are discussed based on device simulation and experimental results in the previous section.

Figure 4.42(a) shows the forward I–V characteristics of MPS diodes with voltage-blocking layer of Epilayer 1 (7×10^{14} cm^{-3}, 100 μm), and Fig. 4.42(b) shows the unipolar on-resistance ($V = 2$ V) and forward voltage drop at $J = 100$ A/cm^2. Here, the P-width was chosen to be longer than 150 μm to exclude the snapback phenomenon, and the S-width was set to be the same as the P-width. In the simulation, the p^+-barrier was not used in the SBD region (not JBS). In Fig. 4.42(a), forward I–V characteristics with half the current density of PiN diode and SBD are also shown to compare with the MPS diodes.

From Fig. 4.42, as the width of P and S becomes wider, the device approaches the "half I"$-V$ characteristics of PiN diode and SBD, respectively. In other words, completely parallel operation of PiN diode and SBD with half the active area is realized. For the unipolar operation, unipolar on-resistance is below the on-resistance of half SBD (two times the on-resistance of SBD). This is due to the current spreading below the p^+-anode, which increases the *effective* active area of the SBD region of the MPS diode. Because the current spreading region for the MPS diode with a shorter P-width takes a larger portion of the whole MPS diode area, the MPS diode with a shorter P-width has smaller unipolar on-resistance. On the other hand, for bipolar operation, forward voltage drop decreases with increasing P-width. This is due to the non-uniformity of conductivity modulation below the p^+-anode. Figure 4.43 shows the simulated hole density at 100 A/cm^2 for an MPS diode with $P = S = 250$ μm. Near the boundary of PiN and SBD region, full conductivity modulation is not occurring below the p^+-anode because spreading current from SBD region reduces the voltage applied to the p^+n junction. Therefore, as the P-width widens, ratio of the fully conductivity modulated region of PiN region increases, which reduces the bipolar on-resistance and forward voltage drop. Furthermore, for $P \geq 250$ μm, the forward voltage drop becomes smaller than that of half PiN diode because additional current flow of SBD

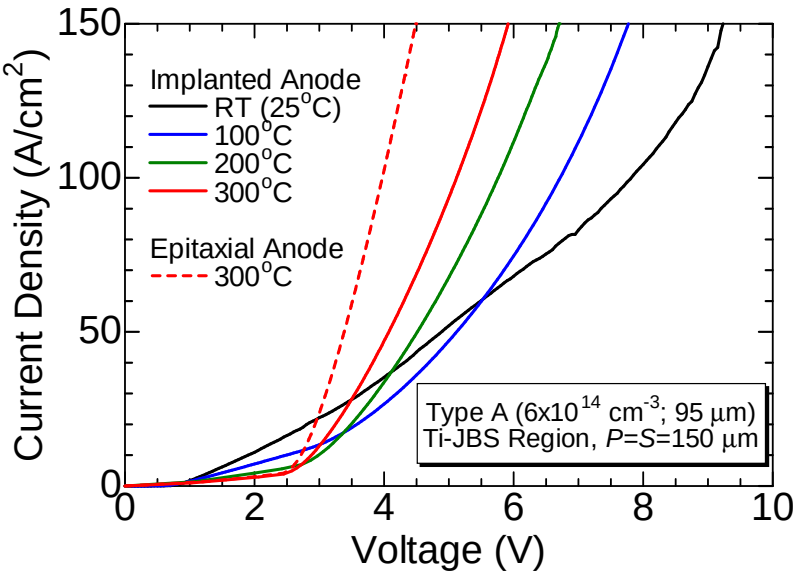


Figure 4.41: Temperature dependence of forward I–V characteristics of MPS diodes with implanted and epitaxial p^+-anode.

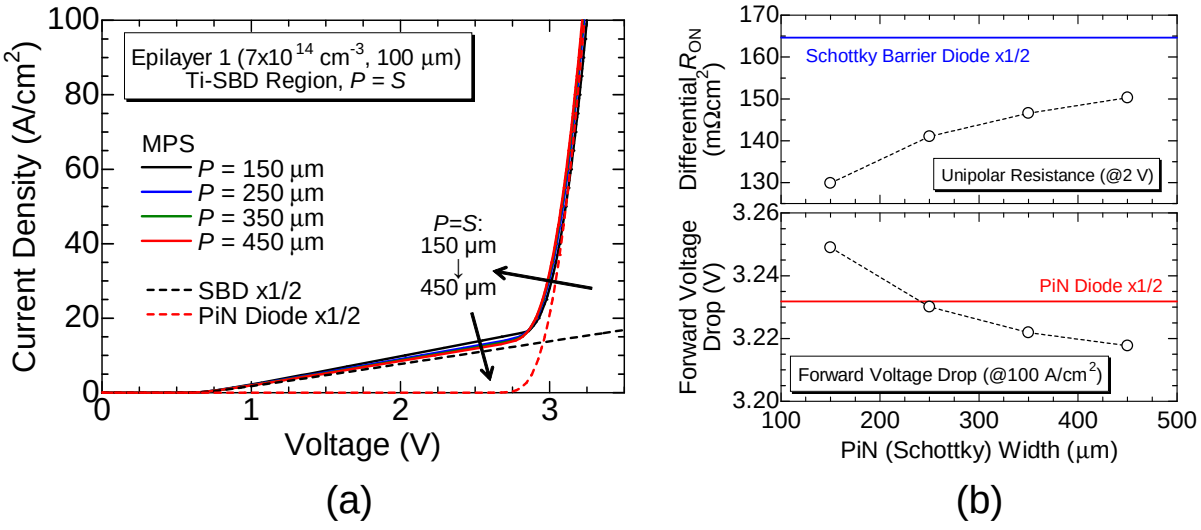


Figure 4.42: (a) Simulated forward I–V characteristics of MPS diodes (Epilayer 1) with P-width larger than 150 μm. (b) P-width dependence of unipolar on-resistance ($V = 2$ V) and forward voltage drop at $J = 100$ A/cm^2.

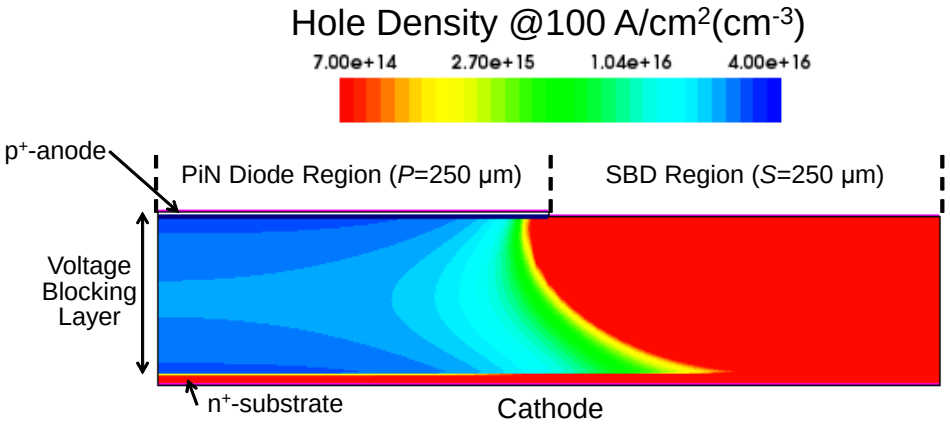


Figure 4.43: Simulated hole density at 100 A/cm^2 for an MPS diode with P and S-width of 250 μm.

is included in the MPS diode.

Figure 4.44 shows the simulated reverse recovery characteristics of MPS diode and PiN diode. Here, diodes were turned off from a forward current density of 100 A/cm^2 with a current turn-off rate (di/dt) of 500 A/μs and a dc-link voltage ($V_{\rm R}$) of 1.5 kV. Regarding the peak reverse recovery current, the MPS diode had a smaller value than that of PiN diode in all of the cases. For MPS diodes with various P-widths, larger peak reverse recovery current was obtained for wider P-width.

Figure 4.45 shows the relationship of reverse recovery charge ($Q_{\rm rr}$) and forward voltage drop ($V_{\rm F}$) at 100 A/cm^2. Here, $Q_{\rm rr}$ was extracted by integration of the turn-off waveform of the current. Because $V_{\rm F}$ directly corresponds to the conduction loss and $Q_{\rm rr}$ corresponds to the switching loss, these two values are required to be as small as possible. Compared with the PiN diode, the MPS diodes exhibited nearly half the value of $Q_{\rm rr}$, indicating smaller switching loss. In addition, it was even smaller than the $Q_{\rm rr}$ of PiN diode at 50 A/cm^2, which corresponds to the forward current of a PiN diode with half the area. Because forward current of MPS diode includes additional SBD current, it reduced the bipolar current component at a given total current. For MPS diodes with various P-widths, $Q_{\rm rr}$ increased for a wider P-width. This is because an MPS diode with a wider P-width has a larger portion of fully conductivity modulated region.

From the obtained simulated results, the following conclusion can be made for the forward characteristics of MPS diodes ($P = S$).

- Unipolar Operation: Due to the spreading current below p$^+$-anode, increasing the P-width increases the unipolar on-resistance. Furthermore, smaller on-resistance can be obtained compared with half the size of SBD.

- Bipolar Operation: Increasing the P-width causes larger portion of fully conductivity modulated region, which reduces $V_{\rm F}$ (bipolar on-resistance) but increases $Q_{\rm rr}$.

From Figs. 4.44 and 4.45, the difference of $V_{\rm F}$ by changing the P-width is relatively small compared with the difference of $Q_{\rm rr}$. Therefore, a shorter P-width is desirable for a hybrid operating MPS diode due to the reduced unipolar on-resistance and $Q_{\rm rr}$. Because too short P-width can cause snapback phenomenon from Fig. 4.31, it can be concluded that a P-width satisfying $r_{\rm P} = 150\%$ is the optimum value. However, because using JBS-region can reduce the snapback voltage, a smaller value of $r_{\rm P}$ may be used when the JBS-region is used for the MPS diode. While using a p$^+$-anode with $r_{\rm P} = 150\%$, unipolar and bipolar operation can be controlled by changing the S-width or the unit cell geometries of the PiN and SBD region.

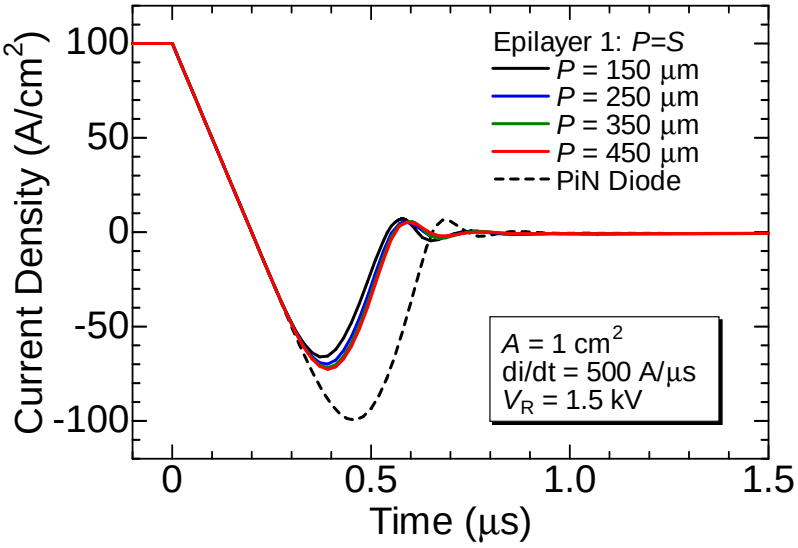


Figure 4.44: Simulated reverse recovery characteristics of MPS diode and PiN diode.

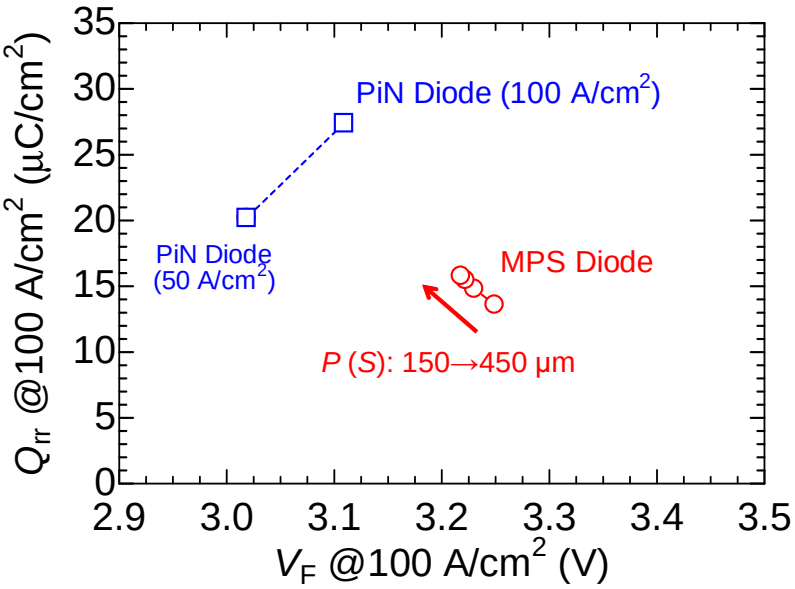


Figure 4.45: Relationship of reverse recovery charge ($Q_{\rm rr}$) and forward voltage drop at 100 A/cm^2 ($V_{\rm F}$) simulated for 10 kV-class SiC MPS and PiN diodes (Epilayer 1).

4.6 Reverse Characteristics of MPS Diodes

4.6.1 Blocking Characteristics

In this section, reverse characteristics of MPS diodes with improved SM-JTE explained in Section 4.2 are investigated. For the voltage-blocking layer, Type A epilayer has been used to fabricate 10 kV-class MPS diodes. Here, the hexagonal pattern (Fig. 4.38) is used for the unit cell structure, and the JBS region is used to reduce the leakage current. The measured MPS diodes have P and S-widths of 100 μm. Forward I–V characteristics of a fabricated MPS diode are shown in Fig. 4.46. For this P-width, snapback phenomenon occurs in MPS diodes with a SBD-region as shown in Fig. 4.26. However, because additional voltage drop occurs between the p^+-barriers, snapback phenomenon did not occur in the MPS diode characterized here, and an excellent hybrid operation was observed.

Using the above MPS diode, reverse I–V characteristics have been measured using the measurement setup described in Chapter 3. Figure 4.47 shows the reverse I–V characteristics in a linear plot. Here, current density was calculated by dividing the measured current by the total device area including the JTE region. Unfortunately, the measured MPS diode had a large leakage current. Because this large leakage current was also observed in a PiN diode from the same chip, origin of this leakage current is not due to the MPS structure itself. Problems in fabrication process such as passivation process, or crystalline defects in the epilayer may be the origin. However, further investigations are required. For the breakdown characteristics, a sharp increase of reverse current was observed. which indicates a clear breakdown. Here, a breakdown voltage of 11.3 kV was obtained, showing that mesa MPS diodes proposed in this study can realize UHV devices.

4.6.2 Discussion

Here, the measured breakdown voltage is compared with the device simulation. Figure 4.48 shows the simulated D_{ring} dependence of breakdown voltage (shown in Fig. 4.11) together with the experimental results shown by stars. In addition, simulated breakdown voltages for JBS, mesa structure, and JTE, together with measurement results are shown in Table 4.5. Although the voltage-blocking layer structure is slightly different between the simulation (Epilayer 1) and experiment (Type A), they can be quantitatively compared because ideal breakdown voltage is nearly the same between the two epilayer (Epilayer 1: 13.1 kV, Type A: 13.3 kV)

From the comparison between simulations, the smallest breakdown voltage was obtained for the cylindrical JTE simulation, indicating breakdown to be occurring in the JTE region. Therefore, experimental results should take a similar value of breakdown voltage to what was obtained by JTE simulation in the ideal case. Actually, experimental results agree very well with JTE simulation especially for $D_{\mathrm{ring}} = 2.0 \times 10^{13}$ cm^{-2}. This indicates the very accurate device simulation of UHV devices, owing to the accurate impact ionization

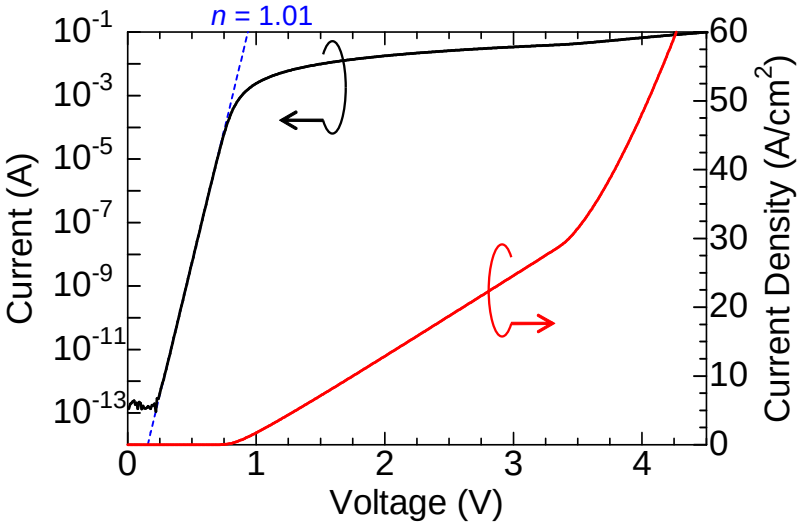


Figure 4.46: Forward I–V characteristics of an MPS diode having JBS region and P-width of 100 μm.

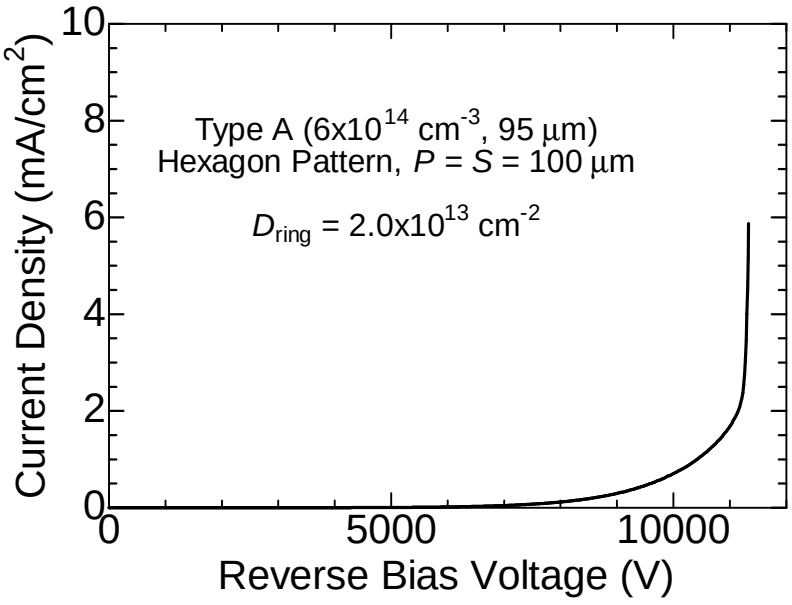


Figure 4.47: Reverse I–V characteristics of MPS diode with improved SM-JTE.

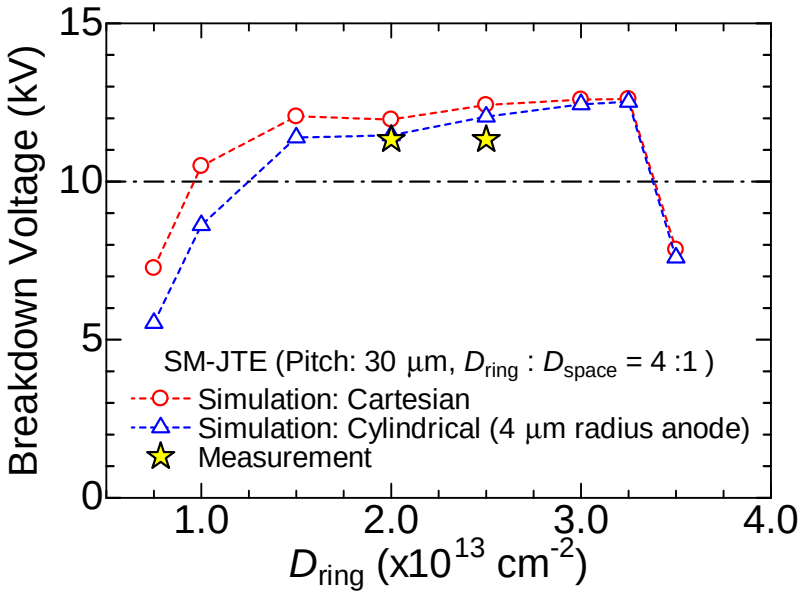


Figure 4.48: D_{ring} dependence of breakdown voltage by simulation and experiment.

Table 4.5: Comparison of breakdown voltage obtained in the device simulation and experiment.

JTE (Ring) Dose	2.0×10^{13} cm^{-2}	2.5×10^{13} cm^{-2}
JBS Simulation	12.4 kV	12.4 kV
Mesa Edge Simulation	12.2 kV	12.2 kV
JTE Simulation (Cylindrical)	11.5 kV	12.1 kV
Experiment	11.3 kV	11.3 kV

coefficients obtained in Chapter 2. In addition, an MPS diode with $D_{\mathrm{ring}} = 2.5 \times 10^{13}$ cm^{-2} has also realized over 10 kV breakdown voltage, which indicates the wide optimum JTE-dose window of the improved SM-JTE. Furthermore, this demonstration of ultrahigh-breakdown voltage in MPS diodes shows the potential of using MPS diodes in the UHV region.

4.7 Summary

In this chapter, toward the integration of unipolar and bipolar operation in a SiC power device, fundamental studies on SiC MPS diodes have been performed. First, the concept of novel MPS structure where a mesa PiN diode with an epitaxial p^+-anode layer integrated with a JBS diode has been introduced. Each of the component structures of the mesa MPS diode, which are the voltage-blocking layer, JBS region, edge termination, and mesa structure were investigated analytically and by device simulation toward the realization of ultrahigh breakdown voltage and low on-resistance. In this study, snapback phenomenon during the forward operation was extensively investigated. To analyze the snapback phenomenon and predict its snapback voltage, a simple JBS current distribution model has been proposed in this study, and was compared with device simulation and experiment to evaluate its validity. From the comparison, it was found that the model could reproduce the tendency of snapback voltage when the device structure was changed, which makes this model to be a semi-quantitative model for analyzing snapback phenomenon.

Further investigations were performed using a snapback-free MPS diodes. From the measurement of unipolar and bipolar on-resistances of an MPS diodes with various PiN/Schottky structures, it was found that the unipolar and bipolar operations could be controlled by changing the area of PiN and SBD regions. In addition, from the device simulation of static and switching characteristics, increasing the P-width has reduced V_{F} while increasing Q_{rr}. Because the difference of V_{F} was relatively small compared with Q_{rr}, a shorter P-width was found to be desirable for hybrid operating MPS diode. Considering the snapback phenomenon, P-width satisfying $r_{\mathrm{P}} = 150\%$ was the optimum value. Furthermore, using the improved SM-JTE structure, UHV MPS diodes with a breakdown voltage of 11.3 kV have been realized. These results demonstrate the potential of SiC mesa MPS diodes to be applied as UHV power devices, and will become the basis for designing SiC hybrid operating devices.

References

[1] L. Storasta, H. Tsuchida, T. Miyazawa, and T. Ohshima, *Journal of Applied Physics* **103**, 013705 (2008).

[2] T. Hiyoshi and T. Kimoto, *Applied Physics Express* **2**, 091101 (2009).

[3] L. Cheng, J. W. Palmour, A. K. Agarwal, S. T. Allen, E. V. Brunt, G. Y. Wang, V. Pala, W. J. Sung, A. Q. Huang, M. J. O'Loughlin, A. Burk, D. E. Grider, and C. Scozzie, *Materials Science Forum* **778-780**, 1089 (2014).

[4] N. Kaji, H. Niwa, J. Suda, and T. Kimoto, *IEEE Transactions on Electron Devices* **62**, 374 (2015).

[5] F. Udrea, G. Amaratunga, and N. Udugampola, *Proceedings of 2004 International Semiconductor Conference (CAS2004)* **1** (2004) p. 17.

[6] M. Westmoreland, P. J. Ward, and P. A. Mawby, *Proceedings of the 14th European Conference on Power Electronics and Applications (EPE 2011)* (2011) p. 1.

[7] B. T. Donnellan, P. A. Mawby, M. Rahimo, and L. Storasta, *27th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)* (2012) p. 152.

[8] R. Rupp, M. Treu, S. Voss, F. Björk, and T. Reimann, *Proceedings of 18th International Symposium on Power Semiconductor Devices and ICs* (2006) p. 1.

[9] R. Rupp, R. Gerlach, A. Kabakow, R. Schörner, C. Hecht, R. Elpelt, and M. Draghici, *Proceedings of 26th International Symposium on Power Semiconductor Devices and ICs* (2014) p. 67.

[10] E. Van Brunt, *Development of Optimal 4H-SiC Bipolar Power Diodes for High-Voltage High-Frequency Applications*, Ph.D. Thesis, North Carolina State University, 2013.

[11] K. Kawahara, J. Suda, G. Pensl, and T. Kimoto, *Journal of Applied Physics* **108**, 033706 (2010).

[12] H. Lendenmann, A. Mukhitdinov, F. Dahlquist, H. Bleichner, M. Irwin, and R. Soderholm, *Proceedings of 13th International Symposium on Power Semiconductor Devices and ICs* (2001) p. 31.

[13] T. Hatakeyama and T. Shinohe, *Materials Science Forum* **389-393**, 1169 (2002).

[14] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*, Wiley, 2014.

[15] T. Hiyoshi, T. Hori, J. Suda, and T. Kimoto, *IEEE Transactions on Electron Devices* **55**, 1841 (2008).

[16] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, *Journal of Applied Physics* **96**, 224 (2004).

[17] T. Kimoto, O. Takemura, H. Matsunami, T. Nakata, and M. Inoue, *Journal of Electronic Materials* **27**, 358 (1998).

[18] U. Vemulapati, N. Kaminski, D. Silber, L. Storasta, and M. Rahimo, *IET Circuits, Devices Systems* **8**, 168 (2014).

[19] L. Zhu and T. P. Chow, *IEEE Transactions on Electron Devices* **55**, 1857 (2008).

Chapter 5

Conclusions

5.1 Conclusions

In this thesis, fundamental studies on high-voltage SiC diodes were performed. Toward improvement of reverse characteristics, impact ionization coefficients in SiC were determined to realize accurate analysis of breakdown characteristics. In addition, fundamental studies on edge termination structures were performed by both experiment and device simulation, and the obtained results were applied for designing of UHV PiN diodes. Toward improvement of forward characteristics, MPS diodes were fabricated to verify the concept of hybrid operation of unipolar and bipolar devices in a single chip.

In Chapter 2, temperature dependence of impact ionization coefficients in SiC was studied in a wide range of electric field of 1–3 MV/cm toward accurate designing of ultrahigh-voltage devices. First, the measurement method of ionization coefficients, and important aspects that must be considered for the accurate extraction were extensively explained in Section 2.2. Then in Section 2.3, structure and fabrication process of photodiodes used for the measurement were explained. In Section 2.4, extraction procedures, together with assumptions that were used to extract impact ionization coefficients, were explained. Especially for the extraction of electron ionization coefficients, the dead space effect on the measurement has been described.

In Section 2.5, impact ionization coefficients were accurately determined by solving the problems in measurement and analysis which the past studies were facing. By using a multiplication layer structure with low doping concentration, the hole impact ionization coefficient was extracted at a low electric field of 1 MV/cm, which is especially important for designing UHV devices. Extracted ionization coefficients were compared with the results from past literatures, and the origin of differences between them was discussed. High-temperature measurement results were shown up to 150°C in Section 2.6. The hole ionization coefficient decreased with the increase of temperature, as observed in other semiconductor materials. For the electron ionization coefficient, however, its temperature dependence was very small and values obtained at room temperature could be used, at least, up to 150°C.

In Section 2.7, using the ionization coefficients obtained in this study, critical electric field strength and ideal breakdown voltage were calculated. When calculation was performed for n^+p and p^+n structures, a difference has appeared where p^+n structure had a larger ideal breakdown voltage. This was found to originate from the large difference between electron and hole ionization coefficients in 4H-SiC.

In Chapter 3, extensive studies of various JTE structures applied to UHV SiC PiN diodes were performed. In Section 3.2, the physics and the fabrication process of JTE were explained, followed by the technological background and advantages of SM-JTE used in this study. In addition, fabrication process of PiN diodes used in this study was shown.

First, in Section 3.3, 10 kV-class PiN diodes with various JTE structures (single-zone, two-zone, various SM-JTE) were fabricated to experimentally investigate the breakdown characteristics such as JTE-dose dependence of breakdown voltage. Single-zone JTE was studied by numerical device simulation, and the effect of the charges at SiO_2/SiC interface was clarified. It was found that the negative charge has caused a shift of optimum JTE dose, which shows the effectiveness of SM-JTE having a wide optimum JTE-dose window.

In Section 3.4, SM-JTE was improved and a thicker voltage-blocking layer was used for demonstration of 20 kV-class SiC PiN diodes. The novel SM-two-zone JTE was proposed, and its effect was clarified by both experiment and device simulation. By using this JTE structure, breakdown voltage of 21.7 kV was demonstrated, which was the highest value among any solid-state devices at the time. In addition, further optimization of SM-JTE was done in Section 2.5 where a VLD (Variation of Lateral Doping)-like dopant profile was realized. The device simulation has shown further widening of optimum JTE-dose window, and the fabricated PiN diode with a thicker voltage-blocking layer did not exhibited breakdown up to 26.9 kV.

In Chapter 4, fundamental studies on UHV SiC MPS diodes were performed toward the hybrid unipolar/bipolar operating devices. In Section 4.2, the concept of an UHV mesa MPS diode proposed in this study has been explained. Each of the component structures of the mesa MPS diode, which are the voltage-blocking layer, JBS region, edge termination, and mesa structure, has been investigated through analytical modeling and device simulation. In addition, fabrication process of the mesa MPS diodes was explained in Section 4.3.

In Section 4.4, the snapback phenomenon was extensively studied by both device simulation and experiment. First, a simple analytical model was proposed for analyzing the snapback phenomenon in a MPS diode, and to predict the snapback-free condition. This analytical model was compared with the results of numerical device simulation and experimental results of fabricated MPS diodes. It was found that the proposed model could reproduce the tendency of snapback voltage very accurately, making this model to be a semi-quantitative model of the snapback phenomenon.

In Section 4.5, forward characteristics of MPS diodes without the snapback phenomenon were investigated. Unipolar and bipolar on-resistance of MPS diode with various PiN/Schottky structures were experimentally studied. Furthermore, device simulation

of static and switching characteristics were performed to present the design guideline of hybrid operating MPS diodes. In addition, reverse characteristics were investigated in Section 4.6. By using the improved SM-JTE, a breakdown voltage of 11.3 kV was achieved in the experiment, which shows the potential of using the proposed MPS diodes for UHV devices.

5.2 Future Outlook

Through this study, performance improvement of UHV SiC devices was challenged through the investigations of impact ionization coefficients, edge termination structures, and hybrid operating devices. However, several issues still remains that must be solved in the future.

Impact Ionization Coefficients in SiC

- Measurement in Wide Temperature Range
  In this study, temperature dependence of ionization coefficients was obtained at room temperature and high temperature up to 150°C. However, when actual applications of SiC power devices are considered, the values in a wider range of temperature are required. For example, the values at low temperature below 0°C will be important in the case that inverters are used at extremely cold climate, and those at higher temperature such as 300°C will be important in the case of high temperature application or reduced cooling systems. Therefore, experimental studies will be required whether the temperature dependence of ionization coefficients obtained in this study could be used or not in the wider temperature range.

- Determination of α in Low Electric Field Range
  In this study, the hole impact ionization coefficient β was determined in the low electric field range of 1 MV/cm. On the other hand, for the electron ionization coefficient α, it was not extracted due to the extremely low value of α in these electric field range. However, values at low electric field is also important to accurately calculate the ideal breakdown voltage because the ionization integral shown in Section 1.3 [equation (1.2), (1.3)] contains both α and β. To accurately determine ionization coefficients with values below 10^1 cm^{-1}, measurement using a photodiode is inconvenient because the accuracy of unmultiplied current directly affects the obtained ionization coefficients. Therefore, to determine α in low electric field region, measurements using BJTs [1] or JFETs [2, 3] are preferred.

- Anisotropy of Ionization Coefficients
  In 4H-SiC, there exists anisotropy in the critical electric field where the values perpendicular to the c-axis is 75% of that along c-axis [4]. Therefore, from the anisotropy of critical electric field, there should be anisotropy in ionization coefficients, too. Al-

though Hatakeyama *et al.* have measured anisotropy in ionization coefficients [5], their measurement contains some problems as pointed out in Section 2.5. Because real power device structure has various electric field directions due to the two- or three-dimensional structures, anisotropy of ionization coefficients must be taken into account for accurate calculation [6]. Therefore, the ionization coefficients perpendicular to the c-axis must be determined using the accurate measurement method applied in this study.

- Theoretical Studies on Impact Ionization Phenomenon in 4H-SiC
  As mentioned in Section 2.6, the very small temperature dependence of α may be ascribed to the strong conduction band structure effect along the c-axis of 4H-SiC. To confirm this hypothesis, theoretical studies are important. In addition, the fact of this strong conduction band structure effect will also indicate the strong anisotropy of α. In GaAs, where a similar band structure is observed for the $\langle 111 \rangle$ direction, Shichijo *et al.* have shown theoretically that there was no anisotropy in α because contribution of ballistic electrons in impact ionization was negligibly small [7]. Therefore, similar Monte Carlo studies are required especially for electrons to clarify the impact ionization phenomenon in SiC.

Edge Termination Structures in SiC Devices

- Area Efficient Edge Termination Structure
  For SM-JTE used in this study, a wide JTE length had to be used for realizing high breakdown voltage. However, this resulted in a large area of edge termination region inside the device, which will lead to a high device cost (large chip size). Reducing the termination area has also been investigated in Si, and termination structure such as deep trench edge termination has been proposed [8]. Because the device cost is very high in SiC, such studies focusing on reducing the termination area will have a large impact especially in UHV devices requiring a wide JTE length nowadays.

- Application to UHV SiC Transistors
  In this thesis, SM-JTE was applied to UHV PiN diodes to clarify its effect since a PiN diode is the most fundamental structure in power devices. Although two-zone JTE combined with SM-JTE (SM1) shown in Section 3.3 was applied to UHV BJTs and breakdown voltage over 20 kV has been achieved [9], the optimized SM-JTE shown in Section 3.5 must be confirmed in transistors, too. Moreover, the optimized edge termination and also the lifetime enhancement process introduced in Section 3.5 should be both applied to transistors such as IGBTs to demonstrate UHV, low-loss SiC transistors.

SiC Power Devices with Hybrid Unipolar/Bipolar Operation

- Analytical Model to Accurately Predict the Snapback-Free Condition
  In this study, an analytical model to explain the snapback phenomenon has been proposed. Although this model could predict the tendency of snapback voltage accurately and the value of snapback voltage to a certain extent, it could not completely reproduce the value of snapback voltage itself and could not completely predict the snapback-free condition. This is mainly due to the simple linear approximation of electron current flow, which can be improved by using more complicated function as the electron current flow. Furthermore, snapback free conditions when a JBS region is used must also be predicted because this will be the standard structure used in an actual device.

- SiC Transistors with Hybrid Operation and Application to Real Systems
  Using the results obtained from SiC MPS diodes, demonstration of SiC transistors with hybrid operation will be the next step. In this case, the snapback voltage can be analyzed by the model of this study and also by the model proposed for RC-IGBT [10]. Although doping control of the device backside is required, this can be realized by using a free-standing n^--substrate. Furthermore, applying these hybrid operating devices to a real system and characterizing its performance will be an important goal for these devices.

Finally, the author sincerely wishes that studies done in this thesis will serve for the realization of high performance UHV SiC devices. Furthermore, the author wishes that these UHV SiC devices will contribute to the higher efficiency of power converter systems, and play a part in solving energy problems which the human society is facing.

References

[1] W. Maes, K. De Meyer, and R. Van Overstraeten, *Solid-State Electronics* **33**, 705 (1990).

[2] I. Takayanagi, K. Matsumoto, and J. Nakamura, *Journal of Applied Physics* **72**, 1989 (1992).

[3] S. Reggiani, E. Gnani, M. Rudan, G. Baccarani, C. Corvasce, D. Barlini, M. Ciappa, W. Fichtner, M. Denison, N. Jensen, G. Groos, and M. Stecher, *IEEE Transactions on Electron Devices* **52**, 2290 (2005).

[4] S. Nakamura, H. Kumagai, T. Kimoto, and H. Matsunami, *Applied Physics Letters* **80**, 3355 (2002).

[5] T. Hatakeyama, T. Watanabe, T. Shinohe, K. Kojima, K. Arai, and N. Sano, *Applied Physics Letters* **85**, 1380 (2004).

[6] T. Hatakeyama, *physica status solidi (a)* **206**, 2284 (2009).

[7] H. Shichijo and K. Hess, *Physical Review B* **23**, 4197 (1981).

[8] D. Dragomirescu, G. Charitat, F. Morancho, and P. Rossel, *Proceedings of 1999 International Semiconductor Conference (CAS 1999)* (1999) p. 67.

[9] H. Miyake, T. Okuda, H. Niwa, T. Kimoto, and J. Suda, *IEEE Electron Device Letters* **33**, 1598 (2012).

[10] U. Vemulapati, N. Kaminski, D. Silber, L. Storasta, and M. Rahimo, *IET Circuits, Devices Systems* **8**, 168 (2014).

Appendix A

Equations for Extraction of Ionization Coefficients

In this appendix, equations used for the extraction of impact ionization coefficients in Section 2 will be derived.

For a p^+n NPT diode, its multiplication factor can be expressed by the following equation.

$$1 - \frac{1}{M_\mathrm{p}} = \int_0^W \beta \exp\left[-\int_0^x (\beta - \alpha) dx'\right] dx \tag{A.1}$$

$$1 - \frac{1}{M_\mathrm{n}} = \int_0^W \alpha \exp\left[-\int_x^W (\alpha - \beta) dx'\right] dx \tag{A.2}$$

Here W is the depletion layer width. By differentiating both sides of equation (A.1) with respect to W, we obtain

$$\beta = \frac{1}{M_\mathrm{p}^2} \cdot \frac{dM_\mathrm{p}}{dW} \cdot \exp\left[\int_0^W (\beta - \alpha) dx\right] \tag{A.3}$$

Using Lee's expression [1]:

$$\exp\left[\int_0^W (\beta - \alpha) dx\right] = \frac{M_\mathrm{p}}{M_\mathrm{n}} \tag{A.4}$$

equation (A.3) can be transformed to the following expression [2].

$$\beta = \frac{1}{M_\mathrm{p} M_\mathrm{n}} \cdot \frac{dM_\mathrm{p}}{dW} = \frac{qN_d}{\varepsilon_0 \varepsilon_\mathrm{s}} \cdot \frac{1}{M_\mathrm{p} M_\mathrm{n}} \cdot \frac{dM_\mathrm{p}}{dE_\mathrm{m}} \tag{A.5}$$

Here N_d is the doping concentration of n-layer. In this work, $\alpha \to 0$ or $M_\mathrm{n} \to 1$ was assumed because at sufficiently low electric field, it is known that β is much higher than α in 4H-SiC. Therefore, equation (2.10) can be obtained and β can be extracted only from M_p.

Next, to obtain α, equation (A.4) is differentiated with respect of W, and by using equation (A.5), we obtain the following equation [2].

$$\begin{aligned} \alpha &= \frac{1}{M_\mathrm{n}} \cdot \frac{dM_\mathrm{n}}{dW} - (M_\mathrm{n} - 1) \cdot \beta \\ &= \frac{qN_d}{\varepsilon_0 \varepsilon_\mathrm{s}} \cdot \frac{1}{M_\mathrm{n}} \cdot \frac{dM_\mathrm{n}}{dW} - (M_\mathrm{n} - 1) \cdot \beta \end{aligned} \tag{A.6}$$

This equation was used for the analysis of NPT4 in this study [equation (2.13)].

In the case of analysis of NPT3, equation (A.6) cannot be used because the multiplication factor depends on whether the carriers are injected from the higher electric field side or the lower side. For NPT3, M_{n} is given by the following equation.

$$1 - \frac{1}{M_{\mathrm{n}}} = \int_0^W \alpha \exp\left[-\int_0^x (\alpha - \beta) dx'\right] dx \tag{A.7}$$

By differentiating both sides of this equation with respect to W, we obtain

$$\alpha = \frac{1}{M_{\mathrm{n}}^2} \cdot \frac{dM_{\mathrm{n}}}{dW} \cdot \exp\left[\int_0^W (\alpha - \beta) dx\right] \tag{A.8}$$

Then using equations (A.3) and (A.8), the following equation can be derived to obtain α from measurement of M_{p} and M_{n} from different $\mathrm{p^+n}$ and $\mathrm{n^+p}$ NPT diodes [3].

$$\alpha(E_{\mathrm{m}}) = \frac{qN_{\mathrm{a}}}{\varepsilon_0 \varepsilon_{\mathrm{s}}} \cdot \frac{1}{M_{\mathrm{n}}^2} \cdot \frac{dM_{\mathrm{n}}}{dE_{\mathrm{m}}} \cdot \left(\frac{qN_d}{\varepsilon_0 \varepsilon_{\mathrm{s}}} \cdot \frac{1}{\beta(E_{\mathrm{m}}) \cdot M_{\mathrm{p}}^2} \cdot \frac{dM_{\mathrm{p}}}{dE_{\mathrm{m}}}\right)^{\frac{N_d}{N_{\mathrm{a}}}} \tag{A.9}$$

Here, E_{m} and N_{a} are the maximum electric field and doping concentration of p-layer in $\mathrm{n^+p}$ diode, respectively. This equation was used for the analysis of NPT3 in this study [equation (2.12)].

For a PT structure (PT1, PT2), assuming PiN structure with i-layer width of W, the following equation can be used to obtain β [4].

$$\beta(E_{\mathrm{m}}) = \frac{1}{W} \cdot \frac{M_{\mathrm{p}} - 1}{M_{\mathrm{p}} - M_{\mathrm{n}}} \cdot \ln\left(\frac{M_{\mathrm{p}}}{M_{\mathrm{n}}}\right) \tag{A.10}$$

Using similar assumption $M_{\mathrm{n}} \to 1$ again, equation (2.11) can be derived which was used in this study to obtain β from PT1 and PT2.

References

[1] C. A. Lee, R. A. Logan, R. L. Batdorf, J. J. Kleimack, and W. Wiegmann, *Physical Review* **134**, A761 (1964).

[2] M. H. Woods, W. C. Johnson, and M. A. Lampert, *Solid-State Electronics* **16**, 381 (1973).

[3] H. Niwa, J. Suda, and T. Kimoto, *Materials Science Forum* **778-780**, 461 (2014).

[4] G. E. Stillman and C. M. Wolfe, *Semiconductors and Semimetals* **12**, Academic Press, 1977.

List of Publications

A. Full Length Papers and Letters

1. H. Niwa, G. Feng, J. Suda, and T. Kimoto,
"Breakdown Characteristics of 15-kV-Class 4H-SiC PiN Diodes With Various Junction Termination Structures,"
IEEE Transactions on Electron Devices **59**, 2748 (2012).

2. H. Niwa, J. Suda, and T. Kimoto,
"21.7 kV 4H-SiC PiN Diode with a Space-Modulated Junction Termination Extension,"
Applied Physics Express **5**, 064001 (2012).

3. H. Miyake, T. Okuda, H. Niwa, T. Kimoto, and J. Suda,
"21-kV SiC BJTs With Space-Modulated Junction Termination Extension,"
IEEE Electron Device Letters **33**, 1598 (2012).

4. N. Kaji, H. Niwa, J. Suda, and T. Kimoto,
"Ultrahigh-Voltage SiC PiN Diodes with an Improved Junction Termination Extension Structure and Enhanced Carrier Lifetime,"
Japanese Journal of Applied Physics **52**, 070204 (2013).

5. N. Kaji, H. Niwa, J. Suda, and T. Kimoto,
"Ultrahigh-Voltage SiC p-i-n Diodes With Improved Forward Characteristics,"
IEEE Transactions on Electron Devices **62**, 374 (2015).

6. H. Niwa, J. Suda, and T. Kimoto,
"Impact Ionization Coefficients in 4H-SiC Toward Ultrahigh-Voltage Power Devices,"
IEEE Transactions on Electron Devices **62**, 3326 (2015).

7. H. Niwa, J. Suda, and T. Kimoto,
"Ultrahigh-Voltage SiC Merged PiN Schottky (MPS) Diode toward Hybrid Unipolar/Bipolar Operation,"
to be submitted to *IEEE Transactions on Electron Devices*.

B. International Conferences

1. H. Niwa, G. Feng, J. Suda, and T. Kimoto,
"Experimental Study on Various Junction Termination Structures Applied to 15 kV 4H-SiC PiN Diodes,"
The 14th International Conference on Silicon Carbide and Related Materials (ICSCRM2011), Cleveland, USA, September 2011.

2. H. Niwa, J. Suda, and T. Kimoto,
"Fundamental Study on Junction Termination Structures for Ultrahigh-Voltage SiC PiN Diodes," (IMFEDK Best Paper Award)
The 2012 International Meeting for Future of Electron Devices, Kansai (IMFEDK2012), Osaka, Japan, May 2012.

3. H. Niwa, J. Suda, and T. Kimoto,
"Breakdown Characteristics of 12-20 kV-class 4H-SiC PiN Diodes with Improved Junction Termination Structures," (Charitat Award)
The 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD2012), Bruges, Belgium, June 2012.

4. T. Kimoto, J. Suda, K. Kawahara, H. Niwa, T. Okuda, N. Kaji, and S. Ichikawa,
"Defect Electronics toward Ultrahigh-Voltage SiC Bipolar Devices," (Invited)
The 9th European Conference on Silicon Carbide and Related Materials (ECSCRM2012), St. Petersburg, Russia, September 2012.

5. N. Kaji, H. Niwa, J. Suda, and T. Kimoto,
"Designing and Fabrication of 20 kV-class 4H-SiC PiN Diodes with Space-Modulated Junction Termination Extension,"
The 9th European Conference on Silicon Carbide and Related Materials (ECSCRM2012), St. Petersburg, Russia, September 2012.

6. T. Kimoto, J. Suda, G. Feng, H. Miyake, K. Kawahara, H. Niwa, T. Okuda, S. Ichikawa, and Y. Nishi,
"Defect Electronics in SiC and Fabrication of Ultrahigh-Voltage Bipolar Devices," (Plenary)
Electrochemical Society Fall Meeting 2012, Honolulu, USA, October 2012.

7. T. Kimoto, K. Kawahara, H. Niwa, T. Okuda, and J. Suda,
"Junction Technology in SiC for High-Voltage Power Devices," (Plenary)
IEEE 13th International Workshop on Junction Technology, Kyoto, Japan, June 2013.

8. H. Niwa, J. Suda, and T. Kimoto,
"Temperature Dependence of Impact Ionization Coefficients in 4H-SiC," (Invited)
The 15th International Conference on Silicon Carbide and Related Materials (ICSCRM2013), Miyazaki, Japan, October 2013.

9. N. Kaji, H. Niwa, J. Suda, and T. Kimoto,
"Ultrahigh-Voltage (>20 kV) SiC PiN Diodes with a Space-Modualted JTE and Lifetime Enhancement Process via Thermal Oxidation,"
The 15th International Conference on Silicon Carbide and Related Materials (ICSCRM2013), Miyazaki, Japan, October 2013.

10. T Kimoto, H. Miyake, H. Niwa, T. Okuda, N. Kaji, and J. Suda,
"Progress and Future Challenges of High-Voltage SiC Power Devices,"
2013 Material Research Society Fall Meeting, Boston, USA, December, 2013.

11. T Kimoto, K. Kawahara, H. Niwa, N. Kaji, and J. Suda,
"Ion Implantation Technology in SiC for Power Device Applications," (Plenary)
IEEE 14th International Workshop on Junction Technology, Shanghai, China, May 2014.

12. H. Niwa, J. Suda, and T. Kimoto,
"Determination of Impact Ionization Coefficients in 4H-SiC toward Ultrahigh-Voltage Power Devices,"
The 10th European Conference on Silicon Carbide and Related Materials (ECSCRM2014), Grenoble, France, September 2014.

13. T Kimoto, H. Niwa, T. Okuda, N. Kaji, and J. Suda,
"Progress and Future Challenges in SiC Material for High-Voltage Power Devices," (Invited)
American Vacuum Society 61st International Symposium, Baltimore, USA, November 2014.

14. H. Niwa, J. Suda, and T. Kimoto,
"Impact Ionization Coefficients and Critical Electric Field Strength in 4H-SiC,"
The 16th International Conference on Silicon Carbide and Related Materials (ICSCRM2015), Giardini Naxos, Italy, October 2015.

15. K. Yamada, H. Niwa, T. Okuda, J. Suda, and T. Kimoto,
"Promise and Limitation of Ultrahigh-Voltage SiC PiN Diodes with Long Carrier Lifetimes Studied by Device Simulation,"
The 16th International Conference on Silicon Carbide and Related Materials (ICSCRM2015), Giardini Naxos, Italy, October 2015.