Short Channel Effects and Mobility Improvement in SiC MOSFETs

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Abstract

Silicon carbide (SiC) is attracting attention as a power device material that can break through the limitation of Si power devices. In particular, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) can theoretically reduce the conduction loss to about 1/500 of that of Si transistors at a given blocking voltage.

Although SiC MOS transistors are now commercially available, the conduction loss of SiC MOSFETs for a medium blocking voltage (< 1000 V) are currently 50-100 times lower than that for Si MOSFETs. SiC MOSFETs have yet to show their full potential. The origin of high conduction loss is the low channel mobility, which is attributable to the high density of interface states (D_{it}) at the SiC/SiO_2 interface. In order to further improve the performance of SiC MOSFET, it is essential to reduce channel resistance. There are two approaches to reduce the channel resistance: 1) shortening the channel length, and 2) improving the channel mobility by reducing interface defects.

In this thesis, the author intensively conducted a systematic study on short-channel effects in SiC MOSFETs and proposed a new technique to improve the channel mobility by reducing the high density of interface states.

In Chapter 2, SiC MOSFETs with various channel lengths and acceptor concentrations (N_{A}) were fabricated in order to investigate the short-channel effects in SiC MOSFETs. The influence of high-density traps at the SiC/SiO_2 interface on short-channel effects was investigated, and a model describing channel length dependence of the threshold voltage (i.e., the gate voltage at a given drain current) was proposed. The critical channel lengths (the channel length at which short-channel effects begin to occur) in SiC MOSFETs were also experimentally determined. The author proposed a new method for determining the critical channel length in SiC MOSFETs, focusing on the increase rate of the drain current in the saturation region, and defined the critical channel length for the fabricated SiC MOSFETs with various acceptor concentrations in the p-body region. The obtained critical channel lengths in the SiC MOSFETs are slightly longer than those in Si MOSFETs, which is caused by the larger built-in potential of SiC compared to that of Si and the existence of a high density of interface states, which enhance the short-channel effects.

In Chapter 3, effects of high-temperature (1400 – 1600°C) N_2 annealing on the interface states of SiC/SiO_2 were investigated. It was demonstrated that high-temperature N_2 annealing is effective not only for the reduction of the interface state density near the con-

duction band edge but also for that near the valence band edge. The interface state density near the valence band edge of the sample annealed in an N_2 ambient was 1×10^{11} cm^{-2}, which is about half of that annealed in a NO ambient.

In Chapter 4, SiC MOSFETs with thermally-grown oxide annealed in N_2 were fabricated and the channel mobilities were evaluated. N_2 annealing effectively improves the both n- and p-channel mobilities. The field-effect mobility of n-channel MOSFETs reached 34 cm^2/Vs being about 12% lower than that of the NO-annealed MOSFETs. On the other hand, the field-effect mobility of p-channel MOSFETs reached 17 cm^2/Vs, being about 30% higher than that of the NO-annealed MOSFETs. Bias temperature instability of the MOSFETs annealed in an N_2 ambient was almost similar to that of the MOSFETs annealed in a NO ambient.

In Chapter 5, the author tried to reduce interface states by creating SiC/SiO_2 structure by the oxidation-minimized process. It was demonstrated that H_2 etching in Si-rich ambient prior to SiO_2 deposition is effective in reducing interface states at the formation of SiC (0001)/SiO_2 interface. A significant reduction of D_{it} (4×10^{10} cm^{-2}eV^{-1}at $E_{\mathrm{c}}-$ 0.2 eV) was achieved for the procedure of H_2 etching of the SiC surface, SiO_2 deposition, and interface nitridation. The D_{it} reduction effect is about five times to that of annealing in NO ambient which has been widely used in SiC MOS community. It was also demonstrated that the above process that minimizes oxidation is effective for the reduction of D_{it} at SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO_2 interface. Substantial low D_{it} of $2-4 \times 10^{10}$ cm^{-2}eV^{-1} were obtained for the samples on $(11\bar{2}0)$ and $(1\bar{1}00)$ faces.

In Chapter 6, n-channel MOSFETs on SiC (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ were fabricated using the oxidation-minimized process and the channel mobilities were evaluated by measuring their electrical characteristics. Compared with the conventional technique (dry oxidation + NO annealing), the channel mobility was drastically improved when the oxide film was formed using the oxidation-minimized process. For the (0001) MOSFETs, the channel mobility reached about 25 cm^2/Vs ($N_{\mathrm{A}} = 1 \times 10^{18}$ cm^{-3}), which is about twice higher than that formed by the conventional method. The obtained channel mobilities were 125 cm^2/Vs for $(11\bar{2}0)$ MOSFETs ($N_{\mathrm{A}} = 1 \times 10^{18}$ cm^{-3}) and 80 cm^2/Vs for $(1\bar{1}00)$ MOSFETs ($N_{\mathrm{A}} = 5 \times 10^{18}$ cm^{-3}), which are 6 and 100 times higher than those obtained by conventional processing, respectively.

In Chapter 7, conclusions of this study and suggestions for future work are described.

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Chapter 1

Introduction

1.1 Background

Semiconductors have become ubiquitous. They are used in integrated circuits (ICs), such as those in computers, lighting devices, such as those in displays, and power devices, such as those in electric vehicles. The spread of semiconductor devices has led to greatly increased electricity consumption. High-efficiency devices are thus required to realize a sustainable society.

About 10% of electric power in modern devices is lost as Joule heat during conversion processes. Conversion efficiency is mainly limited by the performance of semiconductor power switching devices. The design of such devices can thus directly contribute to reducing energy dissipation. Electric power loss in switching devices consists of conduction loss during the on-state, which is due to the resistance of power devices, and switching loss during turn-off and turn-on transients. Typically, on-state power loss is dominant at low operating frequencies and switching loss is dominant at high operating frequencies. It should be noted that there is usually a trade-off between on-state power loss and blocking voltage, as described later.

Si-based power devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs), are commonly used in power electronic systems [1, 2]. For Si MOSFETs, which are the most commonly used unipolar switching devices, the on-state loss increases rapidly with increasing blocking voltage when the blocking voltage is higher than 100 V. To reduce on-state loss, the super-junction structure has been proposed. However, for high-voltage (> 1 kV) applications, it is difficult to fabricate the super-junction structure. Si IGBTs have a low on-resistance for medium-voltage (> 300) applications owing to the conductivity modulation effect caused by minority carrier injection. However, this injection causes excessive power dissipation during switching transients, limiting Si IGBTs to operation at low frequencies.

The performance of Si power devices is mature and thus extremely difficult to enhance. Several wide-bandgap semiconductors, such as silicon carbide (SiC), gallium nitride

(GaN), gallium oxide (Ga_2O_3), and diamond, are regarded as promising materials for next-generation power devices because they mitigate the trade-off between the blocking voltage and on-state conduction loss. Major categories of power devices based on Si, SiC, and other wide-bandgap semiconductors are shown in Fig. 1.1 [3].

1.2 SiC Power Devices

SiC, a IV-IV compound semiconductor, consists of 50% Si and 50% C. It has excellent material properties for power device applications [4–13] and has numerous polytypes (> 200) with various stacking sequences of the Si-C pair along the *c*-axis. Among these polytypes, 4H-SiC is the most attractive for power devices due to its high critical electric field (E_{cr}) and high bulk mobility (μ_{bulk}) [14–18]. The main physical properties of 4H-SiC are listed in Table 1.1, which also lists those of Si, GaN [19, 20], Ga_2O_3 [21, 22], and diamond [23]. Compared with Si, SiC has a wider bandgap, higher critical electric field, and higher thermal conductivity. SiC power devices are thus expected to outperform those fabricated with Si.

The breakdown electric field is an important parameter for achieving low on-resistance (R_{on}) in power devices. For unipolar devices such as Schottky barrier diodes (SBDs) and MOSFETs with a non-punch-through structure, the theoretical limit of R_{on} per unit area (specific on-resistance) is determined by the material properties as follows [2]:

$$R_{\mathrm{on}} = \frac{4V_{\mathrm{B}}^2}{\epsilon_{\mathrm{s}}\mu_{\mathrm{bulk}}E_{\mathrm{cr}}^3}, \tag{1.1}$$

where V_{B} is the blocking voltage, ϵ_{s} is the permittivity of the semiconductor, μ_{bulk} is the carrier mobility, and E_{cr} is the critical electric field. Equation (1.1) indicates that the on-resistance of power devices increases with increasing blocking voltage and that R_{on} depends on E_{cr} and μ_{bulk}. Thus, a semiconductor material with a high E_{cr} is preferred. The E_{cr} value of 4H-SiC is about 3 MV/cm, which is about 10 times higher than that of Si. Hence, at a given blocking voltage, the R_{on} of SiC power devices can be reduced by 2–3 orders of magnitude compared with that for Si unipolar devices.

Compared with other wide-bandgap semiconductors such as GaN, SiC has the most mature technology in terms of device fabrication and crystal growth. For device processing, both n- and p-type SiC can be prepared via ion-implantation [24–28] or epitaxial growth [5, 12, 29–34] across a wide doping range. Another advantage of SiC is the mass production of high-quality single-crystalline wafers with a 150-mm (6-inch) diameter. Extensive research on SiC material and device processing technology has led to the commercial availability of SiC SBDs (in 2001) and MOSFETs (in 2010).

Table 1.1: Physical properties of Si, 4H-SiC, GaN, β-Ga_2O_3, and diamond (data obtained at room temperature).

Property	Si	4H-SiC	GaN	β-Ga_2O_3	Diamond
Bandgap (eV)	1.12	3.26	3.42	4.9	5.5
Electron Mobility (cm^2/Vs)	1400	1000 ($\perp$ c) 1200 ($\parallel$ c)	1300 (bulk) 2000 (2DEG)	300	4000
Hole Mobility (cm^2/Vs)	450	120	30		3800
Electron Saturation Velocity (cm/s)	1×10^7	2.2×10^7	2.7×10^7	1.0-1.5×10^7	2.5×10^7
Critical Electric Field (MV/cm)	0.3	2.5–2.8	2.5–2.8	8 ?	10 ?
Thermal Conductivity (W/cmK)	1.5	4.9	2.0	0.2	20
Relative Permittivity	11.9	9.7 ($\perp$ c) 10.3 ($\parallel$ c)	9.5 ($\perp$ c) 10.4 ($\parallel$ c)	10	5.7

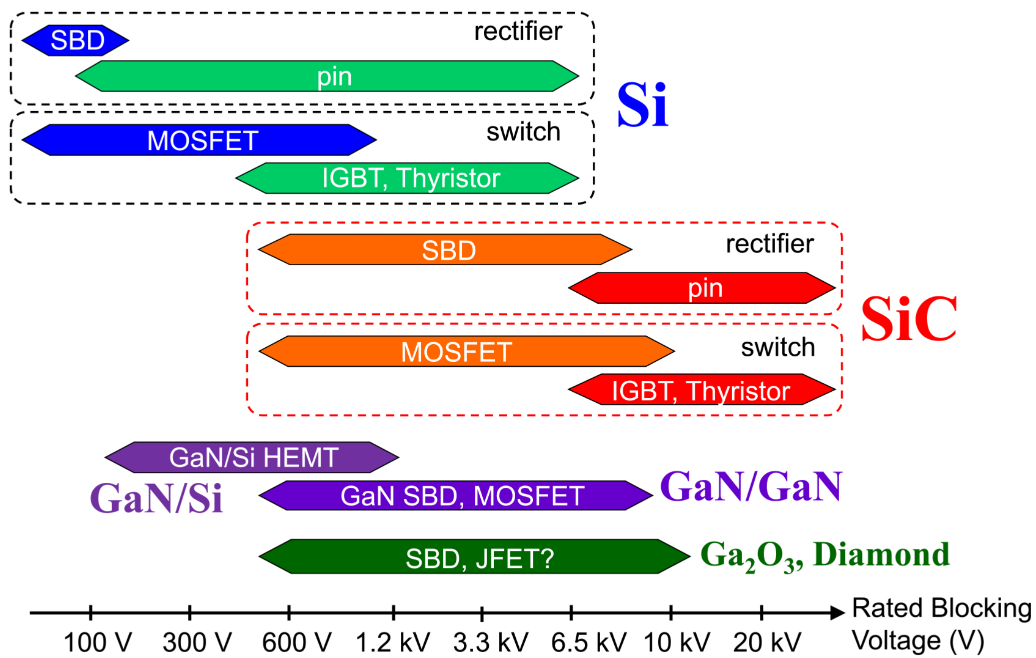

Figure 1.1: Major categories of power devices based on Si, SiC, and other wide-bandgap semiconductors [3].

1.3 Key Issues for SiC MOSFETs

As described in Sec. 1.2, SiC low-loss devices can exceed the limits of Si devices [6, 12]. In particular, SiC MOSFETs are a promising candidate for high-voltage-class (∼1 kV) power devices. Their performance has improved over time [35–42].

However, the performance is still far from that expected based on the material properties of SiC because the channel mobility is so low that the total on-resistance of medium-voltage-class (∼1 kV) SiC power MOSFETs is dominated by the channel resistance rather than the drift layer resistance. Because channel mobility is independent of blocking voltage, the total on-resistance of SiC MOSFETs with a blocking voltage of 600 or 1200 V is dominated by the channel resistance. This poor channel mobility in the inversion layer, which is a long-standing problem for SiC MOSFETs, is attributable to the severe carrier trapping effects at the SiC/SiO_2 interface [3, 43–55]. A schematic band diagram of the SiC metal-oxide-semiconductor (MOS) interface for an n-channel SiC MOSFET in inversion mode is shown in Fig. 1.2. As shown, the electrons in the inversion layer are trapped at the interface states and thus become immobile. Furthermore, the density of interface states ($D_{\rm it}$) exponentially increases toward $E_{\rm c}$. $D_{\rm it}$ is typically about 1×10^{12} to 10^{13} cm^{-2}eV^{-1} near $E_{\rm c}$, which is approximately two orders of magnitude higher than that at the Si/SiO_2 interface (about 1×10^{10} to 10^{11} cm^{-2}eV^{-1}), as shown in Fig. 1.3 [56, 57].

Fig. 1.4 shows a schematic cross section of a vertical MOSFET (DMOSFET) and Fig. 1.5 shows the trade-off relationship between specific on-resistance and breakdown voltage for Si and SiC {0001}. For the Si unipolar limit, only the drift resistance of the voltage blocking layer was considered. The specific on-resistance for SiC includes the resistances that originate from the drift region, substrate, and channel region and other resistances (JFET and contact resistances) [3, 12]. In the calculation, the channel length, cell pitch, and oxide field were assumed to be 0.5 μm, 8 μm, and 3 MV/cm, respectively. The channel mobilities were assumed to be 25 and 100 cm^2/Vs. Note that the doping concentration dependence of the critical electric field was considered in the calculation of resistance in drift regions for both Si and SiC [2, 34]. Although the specific on-resistance of SiC MOSFETs for a medium blocking voltage ($<$ 1000 V) is currently 50-100 times lower than that for Si MOSFETs, SiC MOSFETs have yet to show their full potential. Among series resistances (except for drift resistance), channel resistance accounts for most of the specific on-resistance. If the channel mobility is increased by a factor of four (i.e., from 25 to 100 cm^2/Vs), the on-resistance can be decreased by about half, as shown in Fig. 1.5.

The main resistance components of the specific on-resistance of 600-, 1200-, and 3300-V SiC power MOSFETs are shown in Fig. 1.6. At a high blocking voltage of 3300 V, the specific on-resistance is mainly dominated by drift resistance. At blocking voltages of 600 and 1200 V, channel resistance accounts for about 66% and 48% of the specific on-resistance, respectively [3]. Thus, a reduction in channel resistance is required for a further reduction in the specific on-resistance.

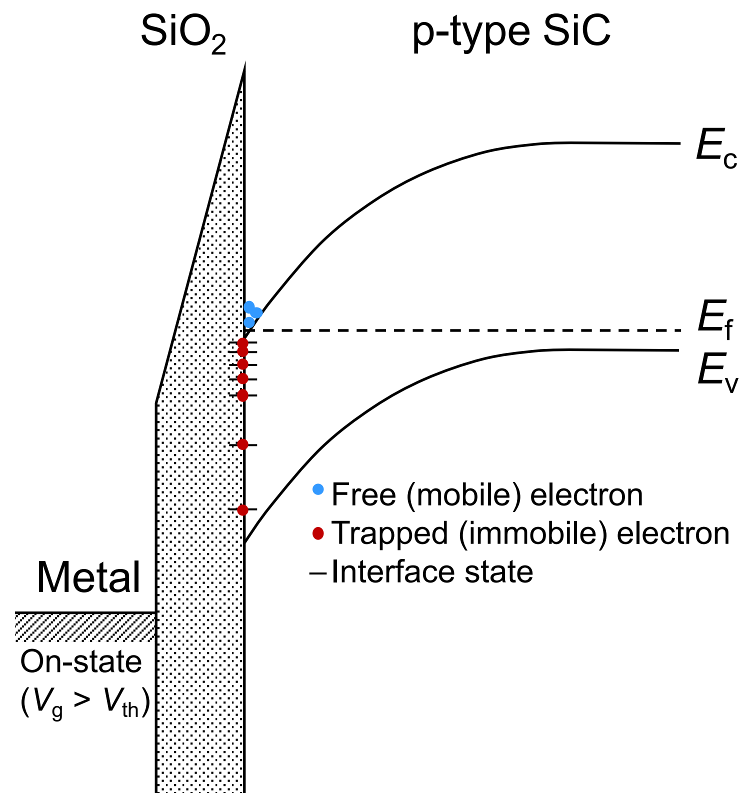

Figure 1.2: Energy band diagram at SiC/SiO_2 interface for a n-channel SiC MOSFET at on-state.

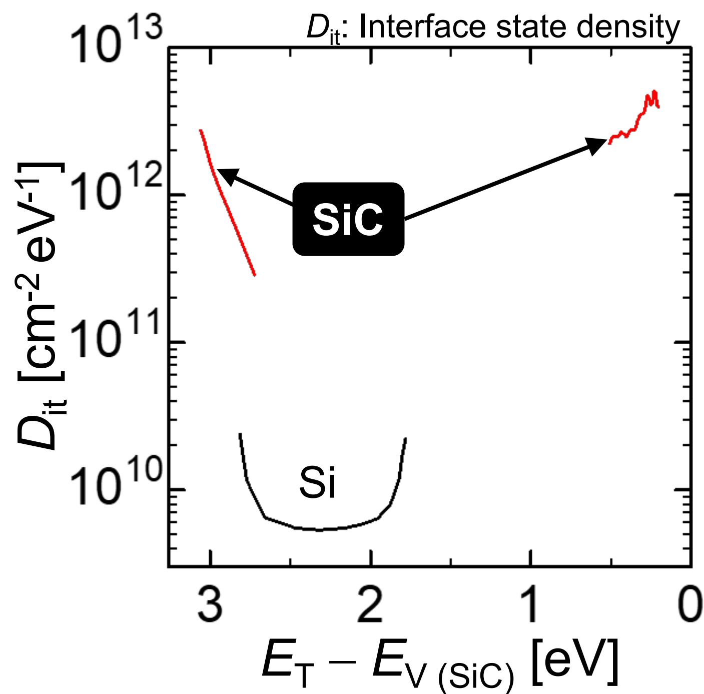

Figure 1.3: Energy distribution of density of interface states (D_{it}) at SiC/SiO_2 interface (thermally grown SiO_2) and typical Si/SiO_2 interface.

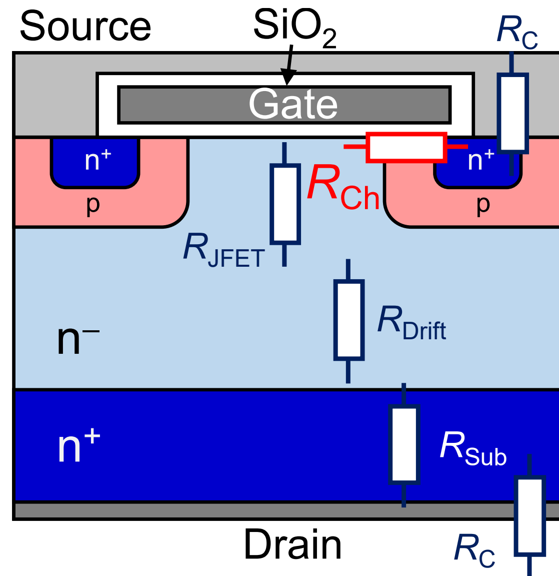

Figure 1.4: Schematic structure of DMOSFET and major resistance components.

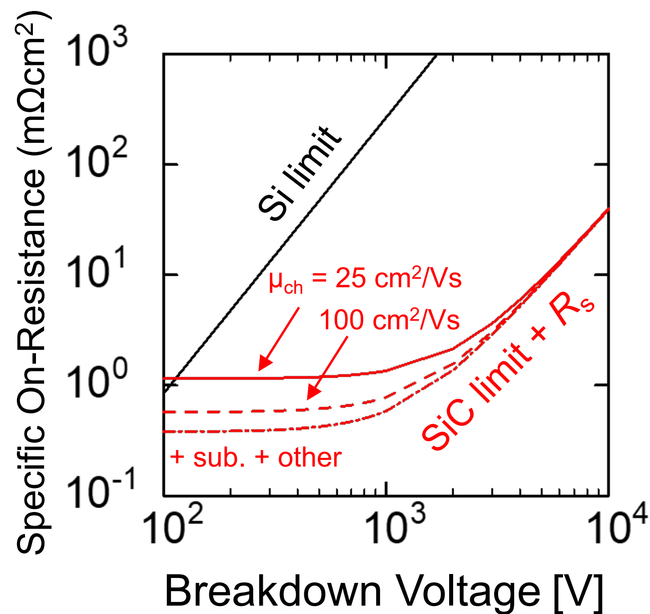

Figure 1.5: Trade-off relationship between breakdown voltage and specific on-resistance for SiC power MOSFETs, taking into account resistances that originate from drift region, substrate, and channel region and other resistances (e.g., JFET and contact resistances) [3, 12]. For Si unipolar limit, only drift resistance of voltage blocking layer was considered [2].

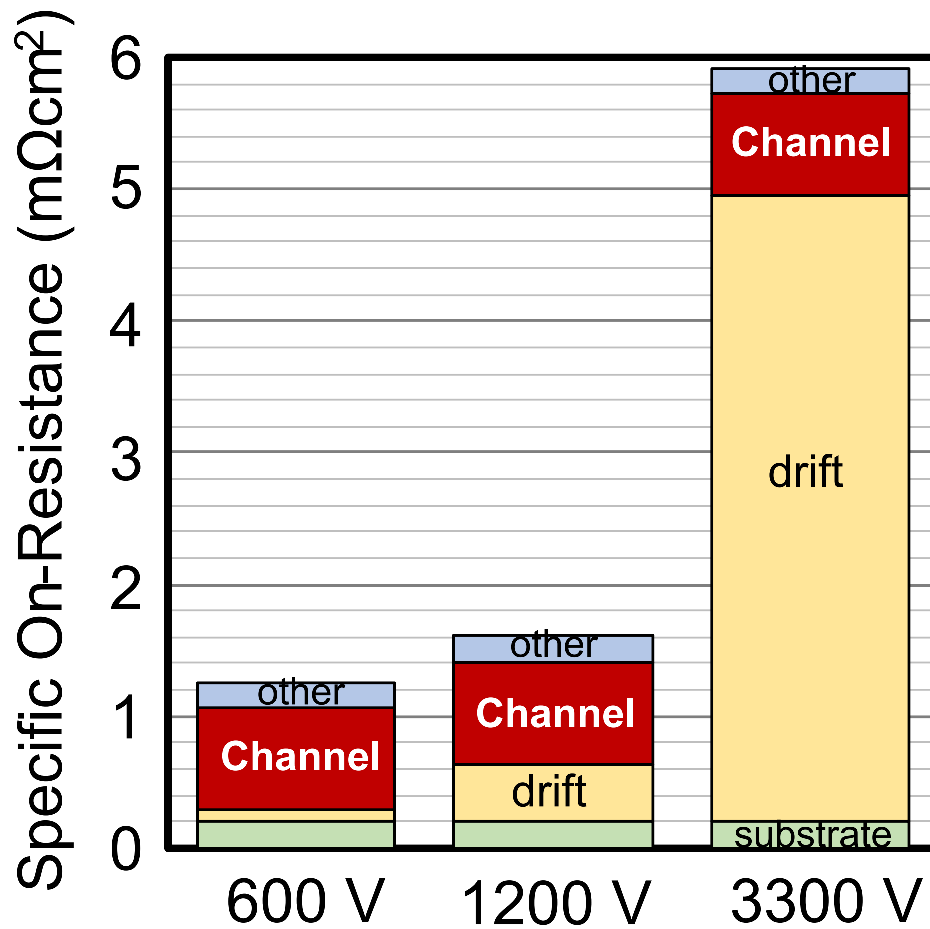

Figure 1.6: Major components of specific on-resistance of SiC power MOSFETs with blocking voltage of 600, 1200, or 3300 V.

There are two approaches for reducing channel resistance, namely shortening the channel length and improving channel mobility.

1.3.1 Short-Channel Effects

Shortening the channel length is an effective approach for directly lowering channel resistance. However, for a sub-micron channel length, short-channel effects (SCEs) may occur depending on the acceptor concentration in the p-body region [58]. Fig. 1.7 shows a schematic band diagram at the MOS interface from the source to the drain region for long- and short-channel MOSFETs. In the long-channel MOSFET, the channel length is much longer than the width of depletion layer extending from the source and drain regions. The potential barrier height from the source to the channel strongly depends on the drain voltage when the width of the depletion layer extending from the source and drain regions becomes comparable to the channel length, as can be seen for the short-channel case. This unintentional reduction in barrier height at the channel near the source end, called the SCE, causes undesirable device characteristics. For example, SCEs decrease the threshold voltage (V_T), lead to the non-saturation of the drain current (I_D) and punch-through behavior, and deteriorate the sub-threshold slope. For Si MOSFETs, there is generalized guideline for the scaling down of MOSFETs with suppression of SCEs [58, 59]. This guideline was semi-empirically determined based on simulation and experimental results for Si MOSFETs. The critical channel lengths are almost uniquely determined, whether determined from simulations or measurements of device characteristics for fabricated Si MOSFETs.

Although most commercial SiC MOSFETs utilize very short channel structures, only a few investigations have been conducted on SCEs in 4H-SiC MOSFETs [60–62]. Several physical properties, such as bandgap and relative permittivity, of SiC are different from those of Si. Thus, there is a possibility that the mechanism of SCEs in SiC MOSFETs is different from that of those in Si MOSFETs. The interface states at the SiC/$\mathrm{SiO_2}$ interface might significantly influence the occurrence of SCEs [61]. To clarify the design criteria of SiC MOSFETs with suppression of SCEs, it is necessary to elucidate the effect of interface defects on SCEs and determine the critical channel length (L_crit) at which SCEs begin to appear, following the numerical studies on Si MOSFETs for giving a guideline. Therefore, fundamental studies on SCEs in SiC MOSFETs and the determination of L_crit with various acceptor concentrations of the p-body are required. SCEs in SiC MOSFETs are described in Chapter 2.

1.3.2 Reduction in Interface States at SiC/$\mathrm{SiO_2}$ Interface and Mobility Improvement in MOSFETs

As mentioned in Sec. 1.3, reducing interface states and improving channel mobility are effective approaches for reducing channel resistance. The typical channel mobility for n-

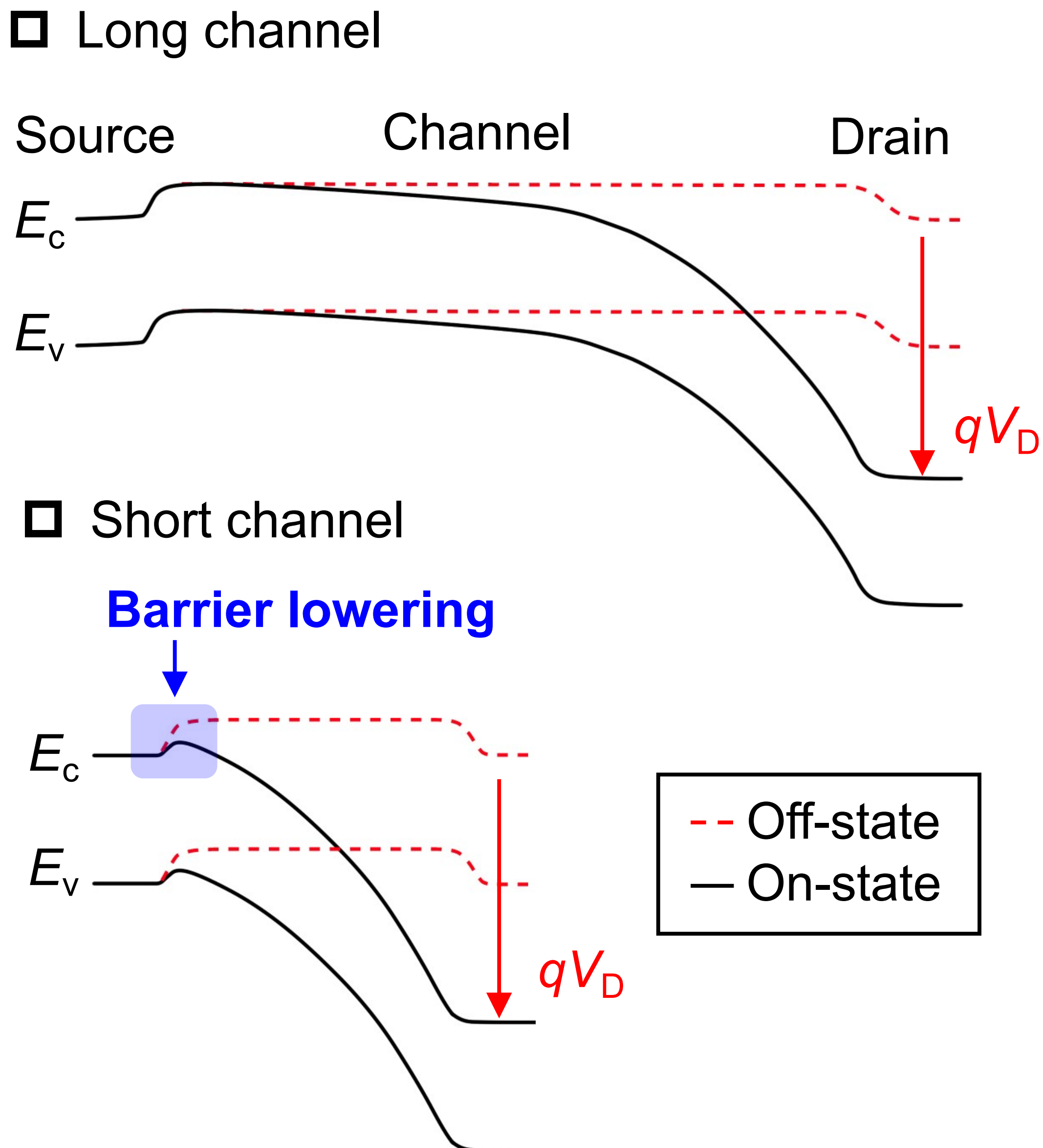

Figure 1.7: Energy band diagram at MOS interface from source to drain for long- and short-channel MOSFETs. Potential barrier from source to channel is lowered by applying drain voltage in short-channel MOSFET.

type SiC(0001) MOSFETs with a thermally grown oxide is about 5–8 cm^2/Vs which is only a fraction of the bulk mobility (1020 cm^2/Vs). In contrast, for Si MOSFETs, the channel mobility reaches about 500 cm^2/Vs [63, 64], which is about one-third of the bulk mobility (1400 cm^2/Vs). The channel mobility can be expressed as 1.2:

$$\mu_{\mathrm{ch}} = \mu_{\mathrm{drift}} \frac{n_{\mathrm{free}}}{n_{\mathrm{free}} + n_{\mathrm{trap}}}, \tag{1.2}$$

where n_{free} and n_{trap} are the densities of mobile electrons and electrons trapped at interface states, respectively. μ_{drift} is the real electron mobility, which can be obtained from MOS Hall effect measurements.

As shown in Fig. 1.3, the interface state density at the SiC/SiO_2 interface is typically about 10^{12} to 10^{13} $cm^{-2}eV^{-1}$ near the conduction and valence band edges, which is about two orders of magnitude higher than that at the Si/SiO_2 interface ($\sim 10^{10}$ $cm^{-2}eV^{-1}$). The density of trapped electrons in the SiC MOS structure is so high that the induced electron sheet density is almost comparable to the density of trapped electrons. The free carrier ratio at the typical MOS interface without any passivation is only about 5% [65]. This is one of the reasons why the channel mobility is extremely poor in SiC MOSFETs. Interface nitridation via annealing in nitric oxide (NO) [66–71] is widely used to improve channel mobility because it attains a relatively high mobility of 20–40 cm^2/Vs without significantly degrading the breakdown characteristics of the gate oxide or causing threshold voltage instability. However, about 70% of electrons are trapped at the interface even after NO annealing [34, 65]. Therefore a substantial reduction in interface states has been strongly required.

Another factor that limits channel mobility is low Hall mobility (drift mobility), which is regarded as the channel mobility of free electrons in an inversion layer. The Hall mobility for n-channel MOSFETs with a low acceptor concentration of the body (e.g., 1×10^{15} cm^{-3}) is as low as 100 cm^2/Vs, which is about 10% of the bulk mobility of SiC. Although NO annealing effectively reduces D_{it} the enhancement of channel mobility is attributable to the increase in the density of mobile electrons and Hall mobility is not improved by NO annealing [34, 65]. Many studies have investigated the scattering mechanism of drift mobility at the SiC/MOS interface; surface roughness scattering, Coulomb scattering, and scattering by neutral defects are considered as candidates [47, 48, 50, 65, 72–81]. It is also quite important to improve the real electron mobility if the carrier trapping problem is solved.

The above discussion has been limited to the case where the MOS channel is fabricated on the (0001) plane (DMOSFET). There are more advanced designs for SiC MOSFETs that can lower the on-resistance. Fig. 1.8 shows the basic structure of a typical planar power MOSFET (DMOSFET) and Fig. 1.9 shows the basic structure of a trench power MOSFET. The trench structure eliminates the JFET resistance in a DMOSFET and makes the unit area per MOSFET smaller than that for DMOSFETs because the channel is oriented per-

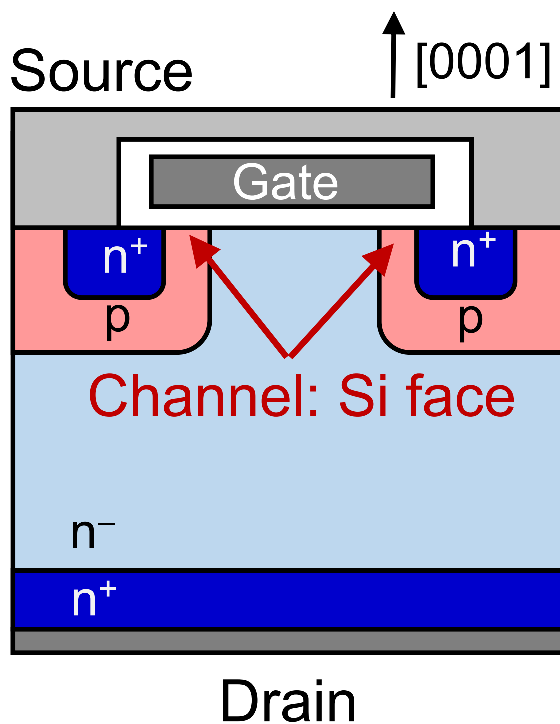

Figure 1.8: Schematic structure of planar MOSFET (DMOSFET).

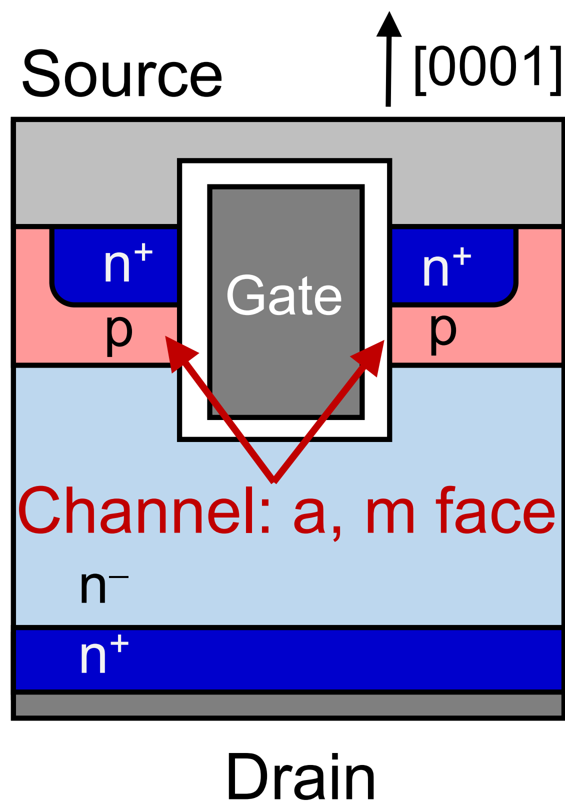

Figure 1.9: Schematic structure of trench MOSFET.

pendicular to the surface. Note that for trench MOSFETs, the oxide fields are significantly crowded at the trench corners if appropriate design optimization is not conducted. In addition to these geometric advantages, trench MOSFETs fabricated on SiC(0001) wafers have another advantage.

Fig. 1.10 shows the hexagonal unit cell of SiC, where the major crystal faces for practical applications, namely (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$, are indicated. In this thesis, (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ are referred to as the Si, a, and m faces, respectively. It is known that the MOS channel formed on a non-polar face, such as $(11\bar{2}0)$ and $(1\bar{1}00)$, of the SiC crystal has much higher channel mobility than that of a channel formed on (0001). High channel mobilities (>90 cm^2/Vs) have been obtained for $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs with NO annealing; these faces are a good choice for the vertical sidewalls of trench-type SiC MOSFETs [71]. However, the channel mobilities on $(11\bar{2}0)$ and $(1\bar{1}00)$ suddenly decrease (10–40 cm^2/Vs) when the acceptor concentration exceeds 1×10^{18} cm^{-3}. Thus, it is essential that further enhancement in the channel mobility for heavily doped $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs. Approaches for increasing channel mobility are described in Chapters 3, 4, 5, and 6.

1.4 Purpose and Outline of This Thesis

In this thesis, the author conducted the following studies as a step toward the realization of ultra-low-loss SiC power MOSFETs.

1. Characterization of SCEs in SiC MOSFETs

   The channel length should be as short as possible because shortening the channel effectively reduces channel resistance. However, the critical (minimum) channel length (i.e., that which does not adversely affect device performance) has not yet been determined. For this purpose, the author quantitatively studied the impact of SCEs on SiC MOSFETs and determined the critical channel length.

2. Proposal of technique for improving channel mobility of SiC MOSFETs

   To greatly improve the performance of SiC MOSFETs, it is necessary to enhance channel mobility in addition to shortening the channel length. For this purpose, the author proposes a technique for creating a SiC/SiO_2 structure that improves channel mobility.

The following experiments are conducted.

In Chapter 2, SiC MOSFETs with various channel lengths and acceptor concentrations are fabricated to investigate SCEs in SiC MOSFETs. The influence of high-density traps at the SiC/SiO_2 interface on SCEs is investigated and a model that describes the channel length dependence of the threshold voltage (i.e., the gate voltage at a given drain current) is proposed.

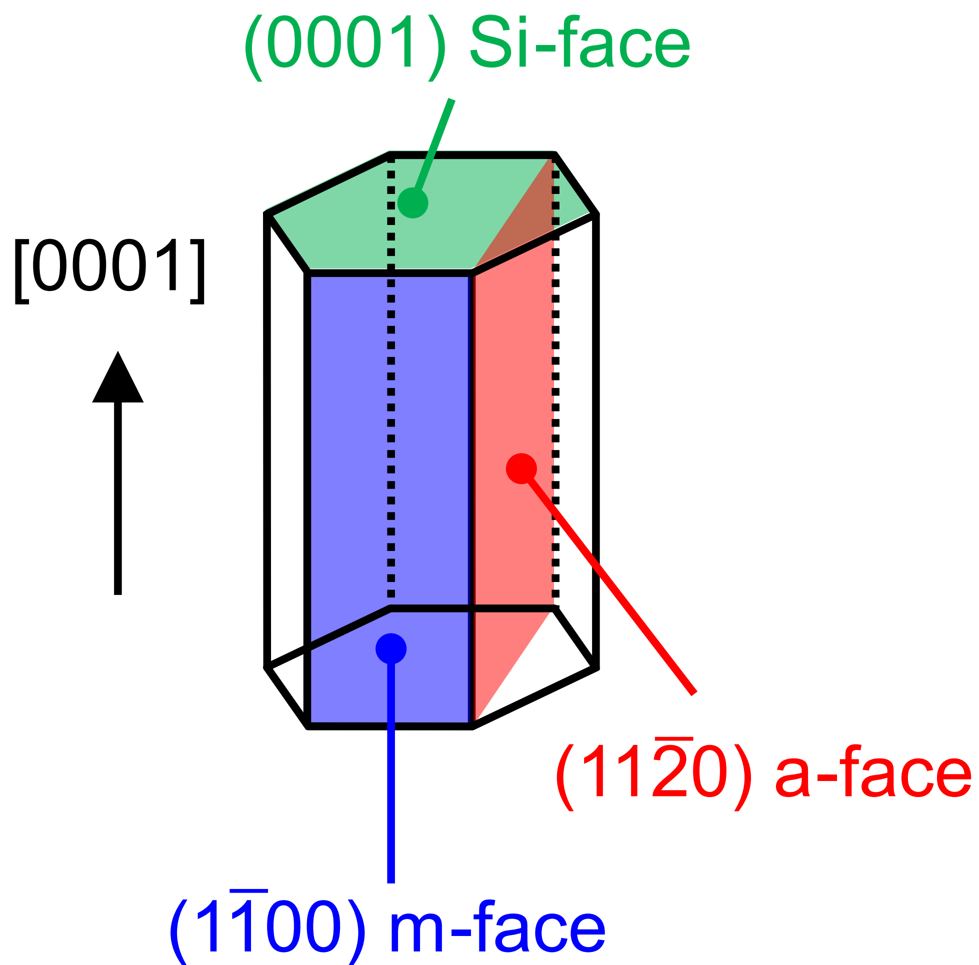

Figure 1.10: Hexagonal cell of 4H-SiC, of which the major crystal faces, namely (0001), (11$\bar{2}$0) and (1$\bar{1}$00) are indicated.

The critical channel length (the channel length at which SCEs begin to occur) in SiC MOSFETs is also experimentally determined. The author proposes a method for determining the critical channel length in SiC MOSFETs, focusing on the increase rate of the drain current in the saturation region, and defines the critical channel length for the fabricated SiC MOSFETs with various acceptor concentrations in the p-body region.

In Chapter 3, the effects of high-temperature (1400–1600°C) N_2 annealing on the interface states of the 4H-SiC/SiO_2 interface are investigated. MOS capacitors with an NO- and N_2-annealed gate insulator are fabricated and the energy distributions of $D_{\rm it}$ near the conduction and valence band edges are extracted. The temperature dependence of the flat-band voltage shifts are also characterized for determining the reliability of the gate insulator.

In Chapter 4, n- and p-channel SiC MOSFETs with a thermally grown oxide annealed in N_2 are fabricated and the channel mobilities are investigated. The mechanism of the mobility improvement of the N_2-annealed MOSFETs is discussed by comparing the field-effect mobility and $D_{\rm it}$ extracted from MOSFETs and MOS capacitors.

In Chapter 5, the author proposes a method for reducing $D_{\rm it}$ at the SiC/SiO_2 interface via an oxidation-minimized process. MOS capacitors are formed on SiC (0001), $(1\bar{1}00)$, and $(11\bar{2}0)$ under various conditions and the electrical properties and the energy distribution of $D_{\rm it}$ are compared. The influences of the thermal oxidation of SiC and H_2 etching prior to SiO_2 deposition on $D_{\rm it}$ are experimentally investigated. H_2 etching is performed under various conditions to determine the key factor for reducing $D_{\rm it}$. X-ray photoelectron spectroscopy (XPS) is conducted on the SiC surface after H_2 etching and the relationship between these results and $D_{\rm it}$ is discussed.

In Chapter 6, n-channel MOSFETs with various acceptor concentrations formed on SiC (0001), $(1\bar{1}00)$, and $(11\bar{2}0)$ are fabricated using the proposed oxidation-minimized process and their channel mobilities are evaluated based on their electrical characteristics. The electrical properties are also measured at low temperature (160 K) to discuss the mechanism of mobility enhancement. The correlation between the channel mobility and the crystal face orientation is also discussed.

In Chapter 7, the conclusions of this study and suggestions for future work are given.

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Chapter 2

Short Channel Effects in SiC MOSFETs

2.1 Introduction

In this study, 4H-SiC MOSFETs with various channel lengths and acceptor concentrations in the p-body regions are fabricated to investigate the SCEs in SiC MOSFETs. Influence of high-density traps at the SiC/SiO_2 interface on short-channel effects is quantitatively analyzed. The model describing channel length dependence of the threshold voltage (i.e., the gate voltage at a given drain current) is proposed, considering the influence of trapped carriers at the MOS interface. The experimental determined and calculated channel length dependencies of the threshold voltage are compared. The author also proposes a new method for determining the critical channel length in SiC MOSFETs and experimentally determines critical channel lengths in SiC MOSFETs.

2.2 Device Fabrication and Basic Characteristics of MOSFETs

To fabricate short-channel MOSFETs, p-type 4H-SiC epilayers on 4°off-axis (0001) substrates were prepared. The acceptor concentrations (N_{A}) in the p-body region were 1.5 $\times$ 10^{16}, 5.1 $\times$ 10^{16}, 2.0 $\times$ 10^{17}, 5.9 $\times$ 10^{17}, and 1.2 $\times$ 10^{18} cm^{-3}. The source and drain regions were formed by P^+ ion implantation with a 1-μm-deep box profile and an average P atom concentration of 4 $\times$ 10^{20} cm^{-3}. After the ion implantation, activation annealing was performed at 1650°C for 20 min. To form the gate oxide, dry oxidation was carried out at 1300°C for 30 min with subsequent NO annealing at 1250°C for 70 min. The resulting oxide thickness was about 42 nm. The channel length (L) and width (W) of the MOSFETs were 0.4 $-$ 20 μm and 29 $-$ 520 μm, respectively, as measured using scanning electron microscopy. The peak of the field-effect mobilities (μ_{FE}) was 26, 12, and 3.9 cm^{2}V^{-1}s^{-1} for

N_A = 1.5 × 10^{16}, 2.0 × 10^{17}, and 5.9 × 10^{17} cm^{-3}, respectively.

Fig. 2.1 shows the typical drain characteristics for the fabricated MOSFETs (N_A = 1.5 × 10^{16} cm^{-3}) with (a) L = 9.8 μm, (b) L = 2.0 μm, and (c) L = 0.6 μm. The gate voltage (V_G) was varied from 0 to 16 V in a 2 V step. For the sufficiently long-channel MOSFET (L = 9.8 μm), the drain current saturated when the drain voltage became larger than the pinch-off voltage. In contrast, the short-channel MOSFETs (L = 2.0, 0.6 μm) exhibited non-saturation characteristics. Furthermore, for the MOSFET with shortest channel length (L = 0.6 μm), a punch-through phenomenon was observed (Fig. 2.1 (c)). The depletion layer width is larger in more lightly doped MOSFETs, which leads to a decrease in the channel length at which the punch-through phenomenon occurs.

Fig. 2.2 (a) and (b) show the gate characteristics of the fabricated MOSFETs (N_A = 1.5 × 10^{16} cm^{-3}, L = 0.6 – 9.8 μm) for drain voltages in the measurements set to 0.2 and 15 V, respectively. The drain current was normalized by the channel length (L) and channel width (W) as $I_{DN} = I_D \times L/W$. A shift of I_D–V_G toward the negative direction was clearly observed with decreasing channel length; the shift was more significant at V_D = 15 V than at V_D = 0.2 V. This can be explained by the drain-induced barrier lowering (DIBL) effect, which is a typical observation of SCEs. These results indicate that the SCEs become significant with shortening the channel length.

2.3 Influence of Interface States on Threshold Voltage Roll-Off Characteristics

2.3.1 Estimation Method of Threshold Voltage

In n-channel SiC MOSFETs, a positive shift of threshold voltage (V_{th}) occurs because of the high density of negative charge caused by trapped electrons existing at the SiC/SiO_2 interface. In short-channel MOSFETs, however, the positive voltage shift will become smaller due to the release of trapped electrons from the interface states near the drain end of the channel [1]. Fig. 2.3 (a) shows the schematic cross section of a MOSFET, and Fig. 2.3 (b) depicts the schematic band diagram near the drain end in the on-state of a MOSFET. In the depletion layer, the quasi Fermi level for electrons (E_{fn}) is lowered as shown in Fig. 2.3 (b). Since the density of interface states drastically increases as getting closer to the conduction band edge (E_c) [2], the majority of the electrons trapped at the interface states is emitted near the drain end. This effect becomes relatively significant when the channel length is comparable to the depletion-layer width. Therefore, the positive shift of the threshold voltage caused by the trapped electrons becomes smaller as the channel length becomes shorter.

In calculating the gate voltage in SiC short-channel MOSFETs, the aforementioned effect should be taken into account in addition to the charge-share model [3]. The channel

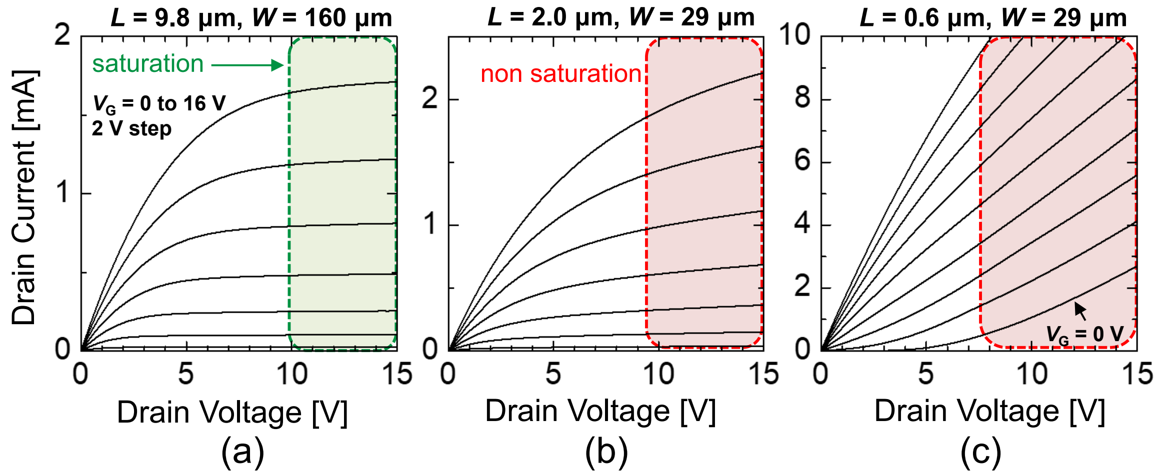


Figure 2.1: Drain characteristics of fabricated SiC MOSFETs ($N_{\mathrm{A}} = 1.5 \times 10^{16}$ cm^{-3}) with (a) $L = 9.8$ μm, (b) $L = 2.0$ μm, (c) $L = 0.6$ μm.

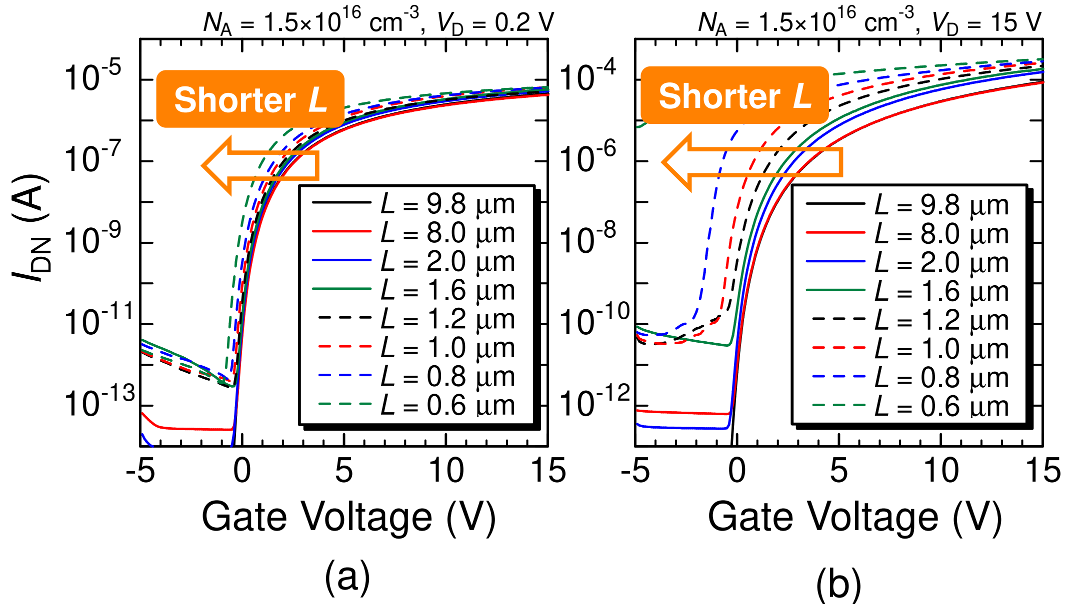
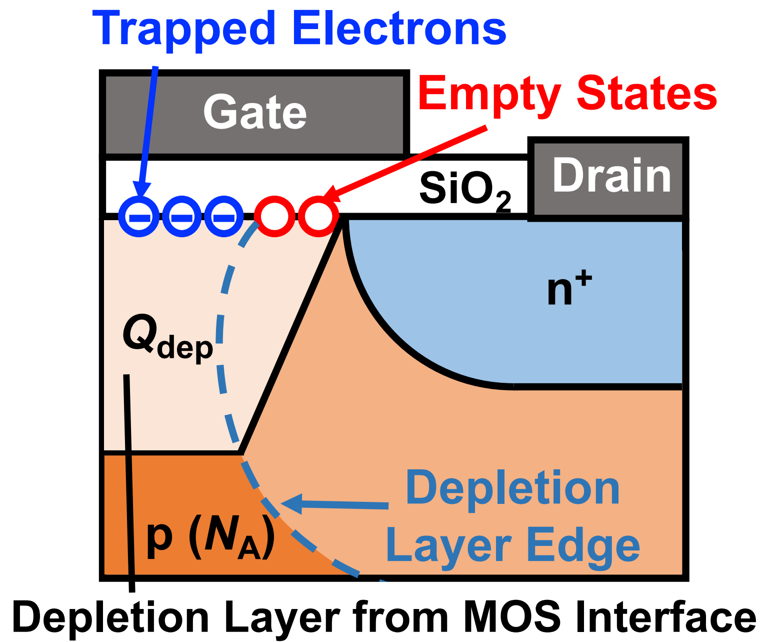
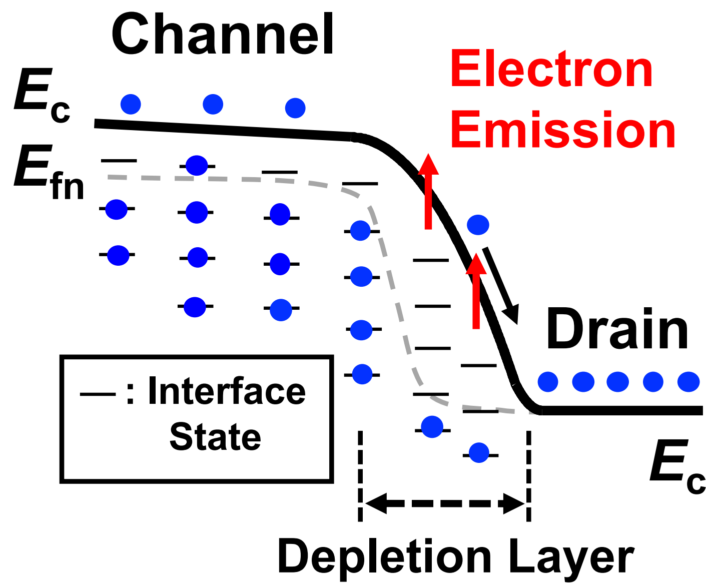


Figure 2.2: Gate characteristics of the fabricated SiC MOSFETs with $N_{\mathrm{A}} = 1.5 \times 10^{16}$ cm^{-2}. V_{D} was set to (a) 0.2 and (b) 15 V and I_{D} was normalized by L and W as $I_{\mathrm{DN}} = I_{\mathrm{D}} \times L/W$.



(a)



(b)

Figure 2.3: (a) Schematic cross section of the SiC MOSFET near the drain end. (b) Schematic band diagram at the MOS interface near the drain end in the on-state of MOSFET. Q_{dep} is the total charge of ionized acceptors and E_{fn} is the quasi Fermi level for electrons.

length dependence of the gate voltage can be described as [1]:

$$\begin{aligned} V_{\mathrm{G}} = V_{\mathrm{FB}} + \psi_{\mathrm{s}} &+ \frac{-Q_{\mathrm{dep}}(L, \psi_{\mathrm{s}}) - Q_{\mathrm{fix}} + en_{\mathrm{free}}(\psi_{\mathrm{s}})}{C_{\mathrm{ox}}} \\ &+ \frac{en_{\mathrm{trapD}}(\psi_{\mathrm{s}})L + e(n_{\mathrm{trap}}(\psi_{\mathrm{s}}) - n_{\mathrm{trapD}}(\psi_{\mathrm{s}}))L'}{C_{\mathrm{ox}}L}, \end{aligned} \tag{2.1}$$

where V_{FB} is the ideal flat-band voltage (i.e., the difference of the work function in metal and that of the Fermi level in the semiconductor), ψ_{s} the surface potential, Q_{fix} the fixed charge (i.e., the charge located at or near the oxide/semiconductor interface), Q_{dep} the charge of depletion layer under the MOS interface, e the elementary charge, n_{free} the density of electrons in the inversion layer, n_{trap} the density of electrons trapped at interface states (n_{trap}: not in the drain-end depletion layer, n_{trapD}: in the drain-end depletion layer), C_{ox} the oxide capacitance, L' the difference between the channel length and the depletion layer width of the drain junction.

In this study, the threshold voltages were extracted in the linear region. Under such a condition, the drain current is dominated by diffusion. Then, the electric field along the channel is negligibly small and the surface potential can be treated as flat in the channel between source and drain regions.

The trapped-electron density was calculated from the energy distribution of D_{it} which is described later. The D_{it} distribution was obtained by fitting the calculated gate characteristic [4] to the experimental result in the MOSFET with a sufficiently long channel length ($L = 9.8$ μm). As well as the gate voltage (2.1), the drain current is also a function of the surface potential:

$$I_{\mathrm{D}} = \frac{W}{L} e\mu n_{\mathrm{free}}(\psi_{\mathrm{s}}) V_{\mathrm{D}} \text{ (in the linear region)}, \tag{2.2}$$

where μ is the drift mobility, V_{D} the drain voltage. In calculating equations (2.1) and (2.2), $n_{\mathrm{trap}}(\psi_{\mathrm{s}})$ is obtained by integrating the product of $D_{\mathrm{it}}(E)$ and the Fermi-Dirac distribution function $F_{\mathrm{FD}}(E_{\mathrm{fn}}, E)$ ($n_{\mathrm{trap}}(E_{\mathrm{fn}}) = \int D_{\mathrm{it}}(E) F_{\mathrm{FD}}(E_{\mathrm{fn}}, E) dE$). To calculate n_{trapD}, the author supposed the decrease of quasi Fermi level to be $\Delta E_{\mathrm{fn}} = 0.2$ eV in the drain-end depletion region because the gate characteristic was measured at $V_{\mathrm{D}} = 0.2$ V. n_{trap} and n_{trapD} were obtained by integrating the intrinsic level to sufficiently high energy at which $F_{\mathrm{FD}} \simeq 0$. For the calculation of $n_{\mathrm{free}}(\psi_{\mathrm{s}})$, the author considered two-dimensional density of states (2D-DOS) [5] and assumed the drift mobility to be constant ($\mu = 100$ cm^2/Vs [6]). $D_{\mathrm{it}}(E)$ was assumed to be expressed as follows:

$$D_{\mathrm{it}}(E) = D_1 + D_2 \exp\left[\frac{E - E_{\mathrm{c}}}{E_{\mathrm{p}}}\right], \tag{2.3}$$

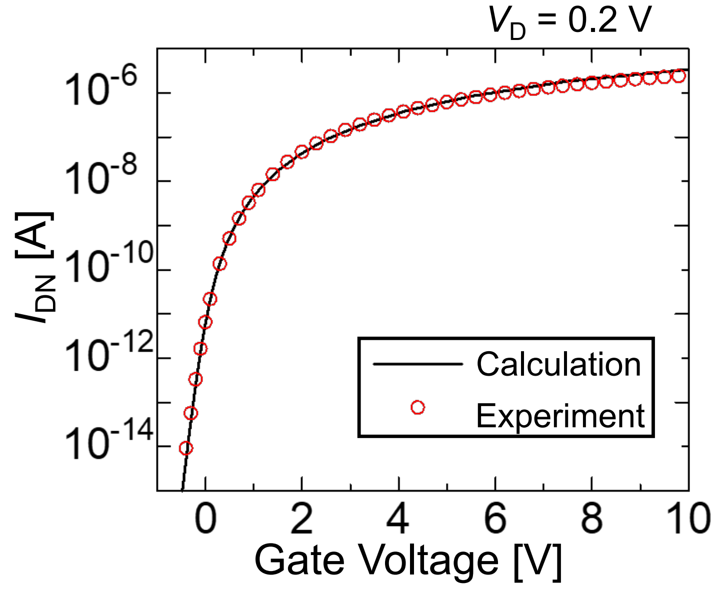
Here, E_{c} is the energy of the conduction band edge and D_1, D_2 and E_{p} are the fitting parameters. The author used four fitting parameters, Q_{fix}, D_1, D_2 and E_{p} to reproduce

MOSFET characteristics by using equations (2.1)-(2.3). Fig. 2.4(a) shows the gate characteristics of a fabricated MOSFET ($L = 9.8$ μm) and the fitted curve by this model. The gate characteristic calculated with $D_{\rm it}$ and $Q_{\rm fix}$ ("$D_{\rm it}$+$Q_{\rm fix}$") shows very good agreement with the experimental result. Fig. 2.4(b) illustrates the energy distribution of $D_{\rm it}$ obtained from this fitting. The obtained $D_{\rm it}$ distribution is quantitatively consistent with that acquired by the C-$\psi_{\rm s}$ method [7] for a MOS capacitor fabricated under a similar condition (with NO annealing).

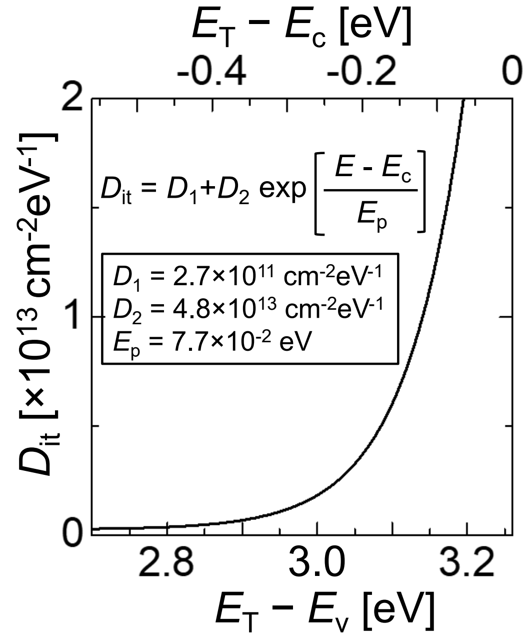
2.3.2 Comparison of Estimated and Calculated Threshold Voltage Roll-Off Characteristics

In this study, the threshold voltage is defined as the voltage at which the normalized drain current $I_{\rm DN} \equiv I_{\rm D} \times L \,/\, W$ equals to a reference value since it is highly ambiguous to determine $V_{\rm th}$ from the linear extrapolation of the gate characteristics in SiC MOSFETs. Solid and dashed curves in Fig. 2.5 show the channel length dependence of the threshold voltage calculated by equation (2.1). In calculating the threshold voltage from equation (2.1), first, $\psi_{\rm s}$ at a given $I_{\rm DN}$ was calculated through equation (2.2). Then, $n_{\rm free}(\psi_{\rm s})$, $n_{\rm trap}(\psi_{\rm s})$ and $n_{\rm trapD}(\psi_{\rm s})$ at given $\psi_{\rm s}$ was obtained in the way described later. The reference value of the drain current was set as $I_{\rm DN} = 1\times10^{-9}$, 1×10^{-8} and 1×10^{-7} A. In Fig. 2.5, the threshold voltages derived from the fabricated MOSFETs are indicated by open circles, while calculation results with "$D_{\rm it}$+$Q_{\rm fix}$" and without "$D_{\rm it}$+$Q_{\rm fix}$" are indicated by solid and dashed curves, respectively.

From Fig. 2.5, the density of positive fixed charge and trapped charges were estimated as $Q_{\rm fix}/e = 1.1\times10^{12}$ cm^{-2}, and $n_{\rm trap} = 6.3\times10^{11}$, 9.4×10^{11} and 1.6×10^{12} cm^{-2}, and $n_{\rm trap}-n_{\rm trapD} = 2.8\times10^{11}$, 5.5×10^{11} and 1.1×10^{12} cm^{-2} at reference drain currents of $I_{\rm DN} = 1\times10^{-9}$, 1×10^{-8} and 1×10^{-7} A, respectively. The threshold voltages without the effect of "$D_{\rm it}$+$Q_{\rm fix}$" do not agree with the experimental results in the following aspects. First, the threshold voltages in relatively long channel MOSFETs ($L = 4.8 - 9.8$ μm) are much different from the experimental results because the voltage shift caused by the charges at the SiC/SiO_2 interface was not considered. Second, compared to the experimental data, reduction of calculated threshold voltage occurred at shorter channel length. This discrepancy originates from ignoring the channel length dependence of threshold voltage shift expressed by the last term of equation (2.1). On the other hand, the channel length dependence of the calculated threshold voltage with "$D_{\rm it}$+$Q_{\rm fix}$" exhibited a good agreement with experimental results even when the reference drain current and channel length were changed. The gradual decrease of threshold voltages as shortening the channel length was well simulated. This means that the threshold voltage in SiC short-channel MOSFETs can be estimated by the proposed method if the density of fixed charge and $D_{\rm it}$ distribution are known.



(a)



(b)

Figure 2.4: (a) Gate characteristic of a fabricated MOSFET ($L = 9.8\ \mu$m) and the fitting curve by the calculation model considering "$D_{\rm it}$+$Q_{\rm fix}$". (b) $D_{\rm it}$ distribution obtained from the fitting.

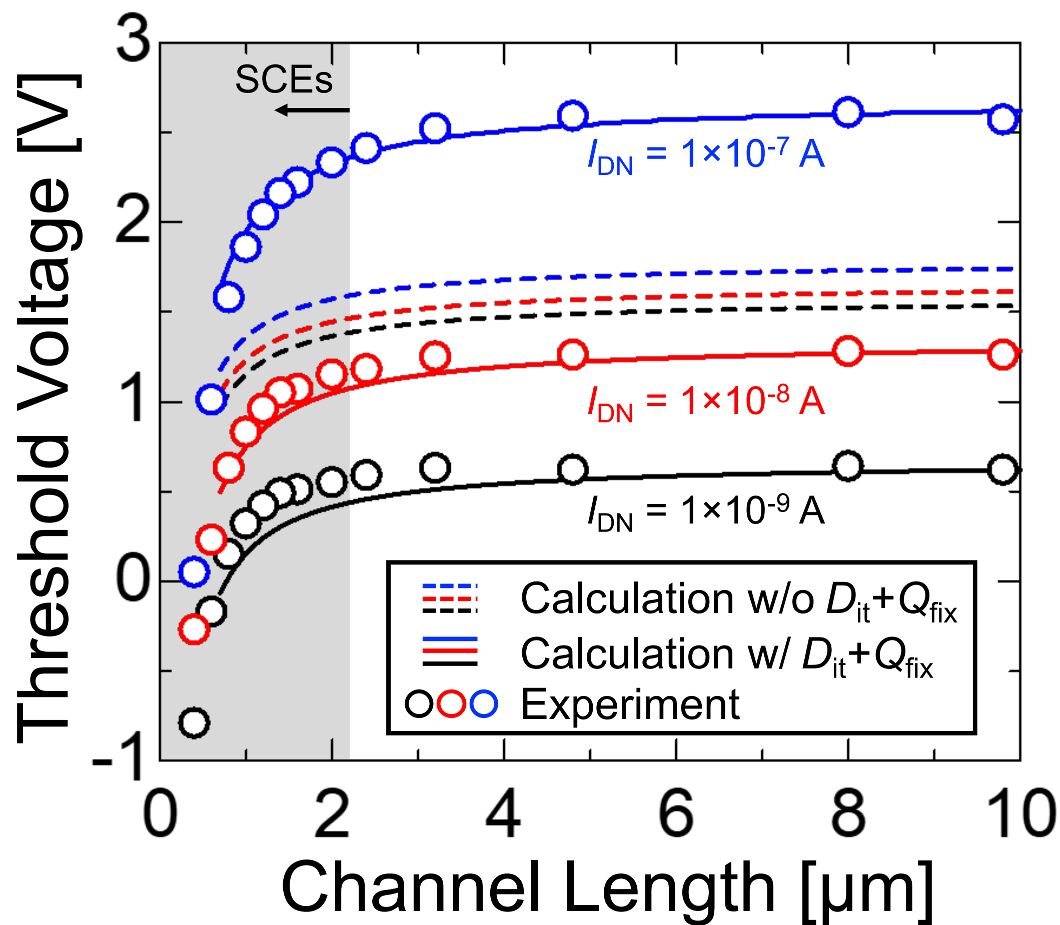


Figure 2.5: Channel length dependence of the threshold voltage in 4H-SiC MOSFETs. The threshold voltages derived from the fabricated MOSFETs are indicated by open circles and the calculation results with "D_{it}+Q_{fix}" and without "D_{it}+Q_{fix}" are indicated by solid and dashed curves, respectively.

2.4 Determination of Critical Channel Length in SiC MOSFETs

2.4.1 Method to Determine Critical Channel Length

In Si MOSFETs, there are several criteria to determine the boundary between a "long-channel" and a "short-channel" MOSFET [8, 9]. (1) L_{crit} is defined as the channel length at which the drain current departs from its linear dependence on $1/L$. (2) L_{crit} is defined as the channel length at which the subthreshold drain current starts to depend on the drain voltage due to the DIBL effect (defined as the channel length when the threshold voltage shift becomes larger than 100 mV). As discussed in section 2.3, interface states severely affects the dependence of the subthreshold characteristics on channel length such as causing the degradation of roll-off characteristics of the threshold voltages. Therefore, it is quite difficult to use these criteria for the device characteristics of SiC MOSFETs in the similar manner as in Si MOSFETs. From the above reasons, a new method to determine the L_{crit} is required. Here, the author proposes a new criterion to simply determine L_{crit} focusing on the rate of change in the drain current in the saturation region, based on the fact that short-channel MOSFETs exhibit the non-saturation of the drain characteristic.

The drain characteristics of the fabricated MOSFETs ($N_{\mathrm{A}} = 1.5 \times 10^{16}$ cm^{-3}) with channel lengths of 9.8 and 2.0 μm are shown in Fig. 2.6 (a) and (b), respectively. The gate voltage (V_{G}) was varied from 0 to 12 V in 2 V steps. For the long-channel MOSFET ($L =$ 9.8 μm), the drain current became saturated when the drain voltage exceeded the pinch-off voltage ($V_{\mathrm{p}} = V_{\mathrm{G}} - V_{\mathrm{th}}$).

In contrast, the short-channel MOSFET ($L = 2.0$ μm) exhibited non-saturation characteristics. These results indicate that the SCEs were significant for short-channel MOSFETs. In this study, L_{crit} is defined as the channel length at which the drain current increases by 10% when the drain voltage is increased from 10 to 15 V. The gate voltage is set to 12 V so that the drain voltage region mentioned above is higher than the pinch-off voltage. The dashed line indicates a value of 1.1 $\times I_{\mathrm{D}}$ at a V_{d} of 10 V, which is the criterion line for short-channel MOSFETs. For the long-channel MOSFET with a channel length of 9.8 μm (Fig. 2.6 (a)), I_{d} at a V_{d} of 15 V does not exceed the criterion line. In contrast, for the short-channel MOSFET with a channel length of 2.0 μm (Fig. 2.6 (b)), I_{d} exceeds the criterion line. In this case, the MOSFETs with a channel length of 2.0 μm are considered to be short-channel MOSFETs. Figure 2.7 shows the channel length dependence of the increase rate of the drain current (V_{d} = 10 to 15 V) for MOSFETs with various acceptor concentrations. The results for $N_{\mathrm{A}} = 5.1 \times 10^{16}$ and 1.2×10^{18} cm^{-3} are not shown in this figure. The increase rate of the drain current rises as the channel length becomes shorter, indicating that SCEs occur for a short channel length. The L_{crit} values were determined as 2.7, 1.3, and 0.9 μm for MOSFETs with $N_{\mathrm{A}} = 1.5 \times 10^{16}$, 2.0×10^{17}, and 5.9×10^{17} cm^{-3}, respectively. The obtained L_{crit} decreases with increasing acceptor concentration, which is

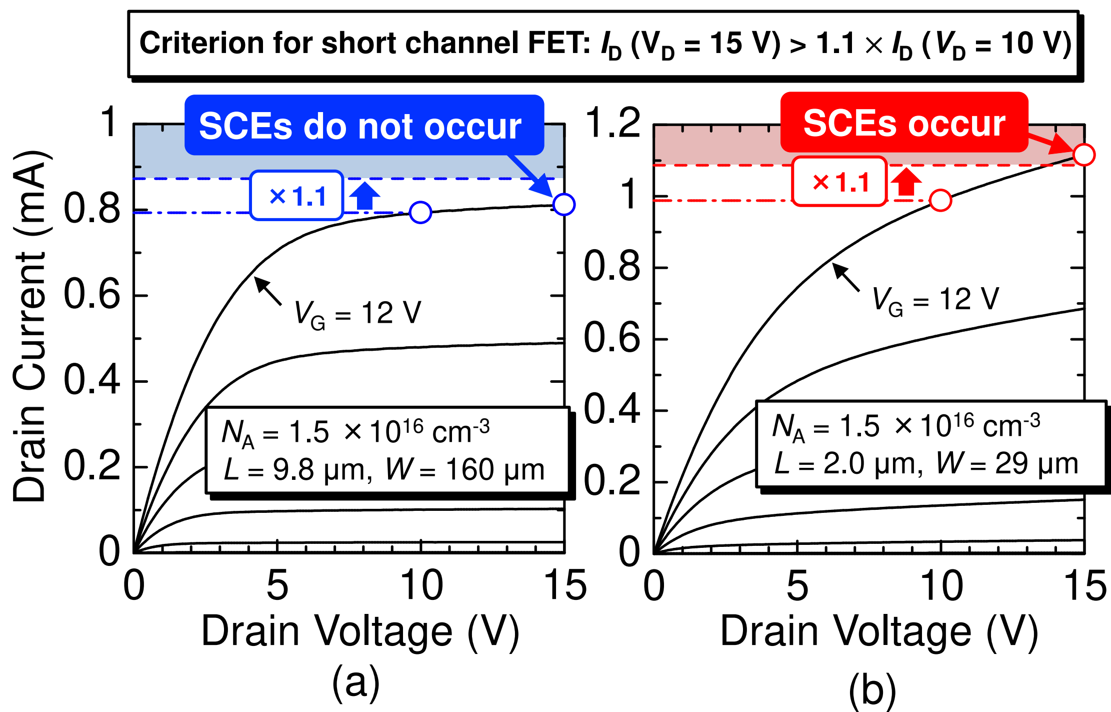


Figure 2.6: Drain characteristics of fabricated SiC MOSFETs ($N_A = 1.5 \times 10^{16}$ cm^{-3}) with (a) $L = 9.8$ μm and (b) $L = 2.0$ μm. L_{crit} is defined as the channel length at which the drain current increases by 10% when the drain voltage is increased from 10 to 15 V.

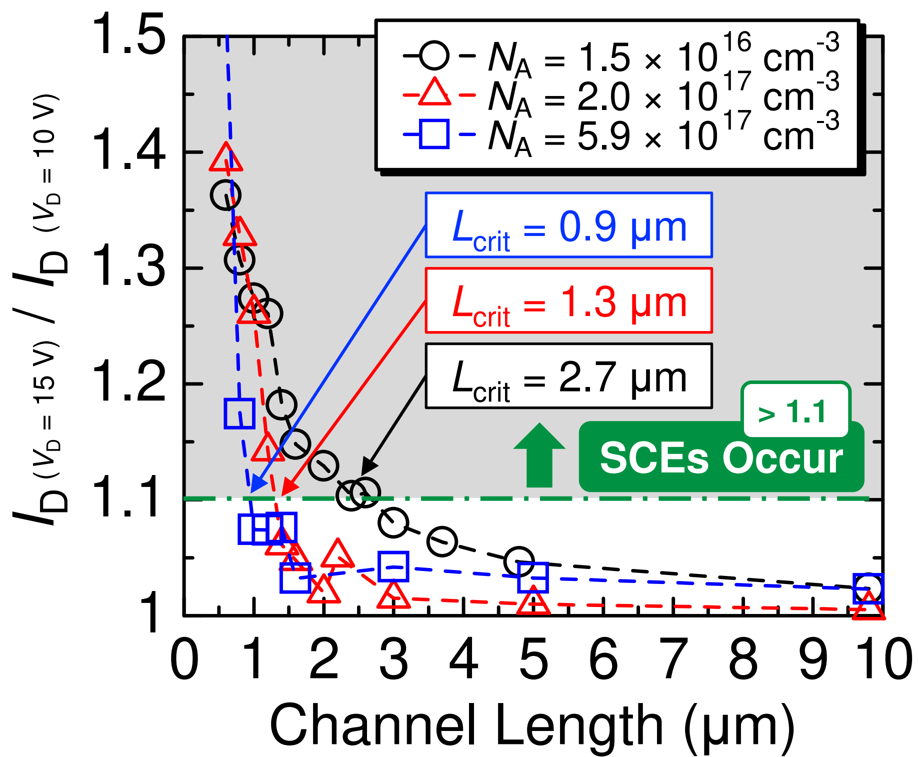


Figure 2.7: Channel length dependence of increase rate of the drain current (V_d = 10 to 15 V) for MOSFETs with various acceptor concentrations. L_{crit} is defined as the channel length at which I_d (V_d = 15 V) / I_d (V_d = 10 V) reaches 1.1.

consistent with the fact that SCEs become more significant in lightly doped MOSFETs. It should be noted that the gate voltage does not significantly affect this relationship between L_{crit} and N_{A} (data shown later). This result indicates that the proposed method is less influenced by the characteristics of SiC MOSFETs, such as the gradual decrease in the threshold voltage, allowing it to uniquely determine L_{crit}.

2.4.2 Acceptor Concentration Dependence of Critical Channel Length

Finally, the experimentally obtained relationship between L_{crit} and N_{A} for SiC MOSFETs is discussed and compared with that for Si MOSFETs. In Si MOSFETs, the critical channel length is empirically described as [8]:

$$L_{\mathrm{crit}} = 0.4\gamma^{1/4}[\mu\mathrm{m}] \tag{2.4}$$

$$\gamma = r_{\mathrm{j}} d_{\mathrm{ox}} (W_{\mathrm{D}} + W_{\mathrm{S}})^2 \times 10^{-4}[\mu\mathrm{m}] \tag{2.5}$$

$$W_{\mathrm{S,D}} = \sqrt{\frac{2\varepsilon_{\mathrm{SiC}}(V_{\mathrm{bi}} + V_{\mathrm{S,D}})}{qN_{\mathrm{a}}}} \tag{2.6}$$

where r_{j} is the junction depth in the source and drain regions [μm], respectively, d_{ox} [μm] is the oxide thickness, and W_{S} [μm], W_{D} [μm] are the depletion layer widths at the source and drain ends, respectively, $\varepsilon_{\mathrm{SiC}}$ is the permittivity of SiC, V_{bi} is the built-in potential in SiC, V_{S} and V_{D} are the source and the drain voltages, respectively, and q is the elementary charge.

Figure 2.8 (a) and (b) show the relationship between L_{crit} and N_{A}. The circles denote the L_{crit} values acquired using the proposed method. The dashed lines show the calculated results for Si and SiC MOSFETs obtained using equations (2.4) and (2.5) [8]. In Fig. 2.8 (a), it can be seen that the L_{crit} values of SiC MOSFETs determined using the proposed method show a similar tendency to the calculated results of L_{crit}. It should be noted that the calculated results depend on drain bias because the depletion layer width of the drain end depends on the drain voltage. Figure 2.8 (b) shows the N_{A} dependence of L_{crit} when the gate voltage is 10, 12, and 14 V. L_{crit} could be almost uniquely determined to N_{A} by this method regardless of the gate voltage.

The experimentally obtained L_{crit} is slightly longer than the calculated L_{crit}. Note that in the logarithmic plot, the experimental results at the higher acceptor concentration seem to be larger than the calculated results. However, the author confirmed that the experimentally obtained L_{crit} is always slightly longer (by about 0.2 μm) than the calculated L_{crit} even at all the acceptor concentration. When the physical properties are considered, L_{crit} for SiC may be longer than that for Si for the following reasons. First, at a given N_{A}, the depletion layer width in a p-n junction in SiC MOSFETs (W_{SiC}) is slightly longer than that in Si MOSFETs (W_{Si}) because the built-in potential in a SiC p-n junction ($V_{\mathrm{bi_SiC}} \sim 3.0$ V) is

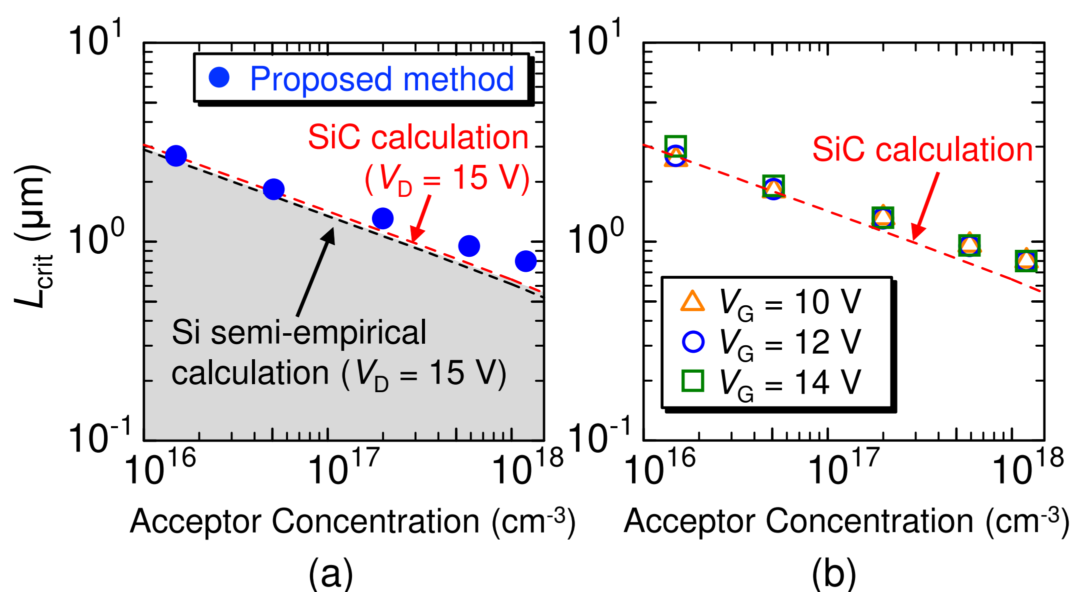


Figure 2.8: (a) Relationship between L_{crit} and N_{A}. Circles are the L_{crit} values acquired for the fabricated 4H-SiC MOSFETs. The dashed lines denote L_{crit} obtained from Si semi-empirical and SiC calculations. (b) Comparison of the experimental results for gate voltages of 10, 12, and 14 V. Experimentally obtained L_{crit} values were almost uniquely determined.

larger than that of Si ($V_{\text{bi_Si}} \sim 0.9$ V). The longer p-n junctions near the source and drain ends increase the occurrence of SCEs. The calculated L_{crit} is thus slightly longer for SiC MOSFETs than Si MOSFETs.

Second, the existence of trapped electrons at MOS interfaces enhances SCEs [1]. In n-channel SiC MOSFETs, a positive shift of the threshold voltage is caused by the trapped-electron charge at interface states. However, the trapped electrons near the drain end are emitted due to the lowering of the quasi-Fermi level caused by the applied drain voltage. As a result, the positive shift of the threshold voltage due to trapped electrons becomes smaller as the channel length becomes shorter, meaning that the threshold voltage shifts toward the negative direction, leading to the degradation of the roll-off characteristics of the threshold voltage. Interface states may also affect the drain characteristics. The drain current increases with increasing drain voltage, which is caused by a decrease in the threshold voltage due to the emission of electrons from interface states becoming prominent as the applied drain bias increases. Consequently, the drain characteristics become more unsaturated. This may be the reason why the experimentally obtained L_{crit} is thus slightly longer than the calculated L_{crit}.

2.5 Discussion

In power MOSFETs, the depletion layer width expanding into the p-body from the drain end becomes smaller than that of lateral MOSFETs at a given drain voltage because power MOSFETs have an n^+pn^- (not n^+pn^+) configuration. Then, the negative shift of threshold voltage in power MOSFETs will become smaller than that of lateral MOSFETs. At the same time, however, the drain voltage can be very high under certain operation conditions such as a switching event, and thus an extended study on this matter is required by using SiC power MOSFETs.

Also it should be to worthwhile to discuss the difference in critical channel length between planar and trench structures (fabricated on Si-face or a-, m-face) for design guidelines. It is considered that the critical channel length of planar MOSFETs is similar to (or slightly longer than) trench MOSFETs. As described above, the drain characteristics in the saturation region is influenced by interface states to small extent, resulting in a slightly longer critical channel length than a calculated result. This influence caused by interface states becomes smaller as the density of interface states decreases. Hence, the critical channel length must be slightly longer in the MOSFETs fabricated on the Si-face than in the MOSFETs fabricated on the a- or m-face.

2.6 Summary

In this chapter, influence of interface states at SiC/SiO_2 on short-channel effects was investigated. A new model describing channel length dependence of the threshold voltage (i.e., the gate voltage at a given drain current) for SiC MOSFETs was proposed. First, the densities of interface states and fixed charge in 4H-SiC n-MOSFETs were obtained by fitting the calculated gate characteristics to the experimental data. Then, threshold voltages were calculated by considering that majority of the trapped electrons are emitted near the drain end due to formation of a depletion layer. The channel length dependence of the threshold voltage calculated by the proposed model showed a good agreement with the experimental results even when the definition of threshold voltage was changed. The present model taking account of the fixed charge and of the trapped electron charge enables the estimation of the threshold voltage in 4H-SiC short-channel MOSFETs.

The critical channel length (the channel length at which short-channel effects begin to occur) in SiC MOSFETs was also experimentally determined. The author proposed a method for determining the critical channel length in SiC MOSFETs, focusing on the increase rate of the drain current in the saturation region, and defined the critical channel length for the fabricated SiC MOSFETs with various acceptor concentrations in the p-body region. The relationship between the critical channel length and the acceptor concentration for these SiC MOSFETs shows a similar tendency to that for Si MOSFETs. The obtained critical channel lengths in the SiC MOSFETs are slightly longer than those in Si MOSFETs, which is caused by the larger built-in potential of SiC compared to that of Si and the existence of a high density of interface states, which enhance the short-channel effects. This work provides guidelines for the design of SiC MOSFETs that utilize very short channel structures.

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Chapter 3

Reduction of Interface States in SiC/SiO_2 Structure near Both Conduction and Valence Band Edges by N_2 Annealing

3.1 Introduction

As described in Chapter 2, the author has quantified the influence of interface states on short-channel effect in SiC MOSFETs, and has succeeded in providing design guidelines for MOS devices that do not exhibit short-channel effects. However, further reduction in channel resistance cannot be realized only by reducing the on-resistance through shortening the channel length. It is necessary to decrease the high-density interface defects for achieving further reduction of channel resistance. In addition, the low channel mobility severely hampers operation of SiC-based complementary MOS (CMOS) integrated circuits. Thus, reduction of interface state density (D_{it}) near the conduction band edge (E_{c}) and the valence band edge (E_{v}) is of great importance for development of low-loss SiC power MOSFETs and high-performance SiC CMOS.

Extensive studies have been conducted to reduce D_{it} at the SiC/SiO_2 interface in the last decades [1–13]. Several passivation methods were experimentally found, and so far, annealing in a nitric oxide (NO) [1, 3, 5] has been the standard process in the SiC MOS community because it can reduce D_{it} to some extent without degrading the reliability of a gate oxide.

Although NO annealing is effective for reduction of D_{it}, the channel mobility is not sufficient in the present stage. Furthermore, it is preferable to avoid using a NO gas because NO is a highly toxic gas. It should also be noted that NO annealing creates hole traps in the SiO_2 side and causes the negative-bias threshold voltage instability [14–17]. Thus, an alternative passivation method to reduce the D_{it} without degrading the oxide reliability

is strongly required. High-temperature ($\sim$ 1400°C) pure-N_2 annealing [9, 18] may be an alternative method for nitridation of the SiC/SiO$_2$ interface.

In this study, the author demonstrates that high-temperature ($>$ 1400°C) N_2 annealing is effective not only for reducing D_{it} near E_c but also for that near E_v. D_{it} near E_v of the N_2-annealed sample is much lower than that of a NO-annealed sample. The breakdown electric field of N_2-annealed gate oxide and bias temperature instability of the MOS capacitors are also investigated.

3.2 Experimental Details

In this study, n-type MOS capacitors were fabricated on an n-type 4H-SiC (0001) epilayer on an n-type substrate and p-type MOS capacitors were fabricated on a p-type 4H-SiC (0001) epilayer on a p-type substrate. The doping concentrations of epitaxial layers were 5×10^{15} cm^{-3} for n-type and 1×10^{15} cm^{-3} for p-type. The gate oxide was formed by dry oxidation at 1300°C for 20 min and its thickness was about 30 nm. After the oxidation, NO annealing (1250°C, 70 min) or high-temperature N_2 annealing (1400 – 1600°C) was performed. In figures in this article, "NO" and "N_2" denote the NO-annealed and N_2-annealed samples respectively. "As-Ox." means the samples without performing any annealing (thermal oxidation only).

The N_2 annealing was performed in a custom-made thermal annealing system using induction heating and cold-wall furnace. The loading and unloading conditions are described below. First, the author loaded samples into the annealing system at room temperature. N_2 was introduced into the furnace after the furnace was evacuated by pumping. The flow rate of N_2 gas was fixed at 0.4 slm. The temperature ramping up rate is 600°C/min. In the cooling process, the temperature drops from 1400°C to below 800°C within about 1 min and it cools down to room temperature within 20 min. The samples were unloaded from the furnace in N_2 ambient at room temperature. The equivalent oxide thickness (EOT) hardly increases after the high-temperature N_2 annealing. It should be noted that the fast cooling rate is not the key process for achieving low D_{it}. Ohmic-contact annealing was conducted for the p-type MOS capacitors.

3.3 Energy Distribution of Interface State Density near the Conduction Band Edge

3.3.1 Capacitance-Voltage Characteristics

Fig. 3.1 (a) depicts the frequency dispersion of the C–V characteristics obtained from the n-type MOS capacitors. C–V stretch-out and frequency dispersion are suppressed in the NO and N_2 samples (1400°C, 45 min). The C–V characteristics of the N_2 sample (1600°C,

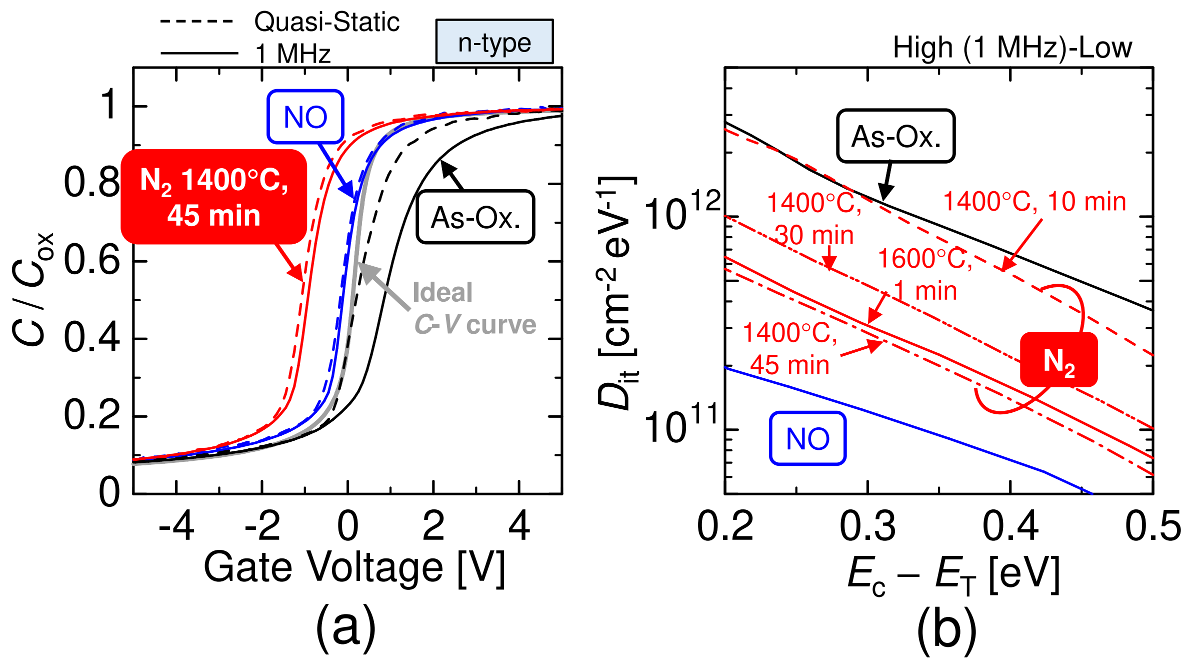

Figure 3.1: (a) Frequency dispersion of C–V characteristics obtained from the fabricated n-type SiC MOS capacitors (As-oxidized, NO-annealed, and N_2-annealed samples). The ideal C–V curve is also indicated for comparison. (b) Energy distribution of D_{it} extracted by a high (1 MHz)-low method.

1 min) were very similar to the results of the N_2 sample (1400°C, 45 min). The densities of the effective fixed charges estimated from the flat-band voltage shift were 1.1×10^{11} cm^{-2} (positive) for the NO-annealed sample and 5.6×10^{11} cm^{-2} (positive) for the N_2-annealed sample.

3.3.2 Energy Distribution of Interface State Density

Fig. 3.1 (b) shows the comparison of the energy distributions of D_{it} near E_{c} extracted by the High(1 MHz)-Low method. The energy position of D_{it} was calculated by using the quasi-static C–V characteristics, where the integration constant was defined under the assumption that the surface potential becomes 0 eV when high-frequency capacitance equals the ideal flat-band capacitance [19]. In the case of N_2 annealing at 1400°C for 10 min, the obtained D_{it} is similar to that obtained from the As-Ox. sample. The D_{it} was reduced as increasing the annealing time and a lowest D_{it} of 6×10^{11} cm^{-2}eV^{-1} at $E_{\mathrm{c}} - 0.2$ eV was obtained by N_2 annealing at 1400°C for 45 min. When the annealing temperature was elevated to 1600°C, the D_{it} was effectively reduced in a short period of annealing ($\sim$ 1 min). Although the energy distribution of D_{it} of the N_2-annealed samples (1600°C, 1 min, 1400°C, 45 min) is much lower than that of the As-Ox. sample, it is still higher than that of the NO-annealed sample by a factor of about 3.

3.4 Energy Distribution of Interface State Density near the Valence Band Edge

3.4.1 Capacitance-Voltage Characteristics

Fig. 3.2 (a) represents the C–V curves of the p-type SiC MOS capacitors fabricated with different processes. The C–V characteristics of the As-Ox. samples is not indicated in this figure due to a very large flat-band voltage of -21.5 V. As in the case of n-type MOS capacitors, the C–V characteristics of N_2 sample (1600°C, 1 min) are not shown for the same reason (the C–V characteristics of the N_2 sample (1600°C, 1 min) were very similar to those of the N_2 sample (1400°C, 45 min)). The negative flat-band voltage shift and frequency dispersion are substantially reduced in the NO-annealed and the N_2-annealed samples (1400°C, 45 min). The densities of the effective fixed charges estimated from the flat-band voltage shift were 1.4×10^{12} cm^{-2} (positive) for the NO sample and 9.6×10^{11} cm^{-2} (positive) for the N_2 sample. The amount of effective fixed charge estimated from flat-band voltage shift is different between n- and p-type MOS capacitors. This phenomenon arises from the difference in the density of trapped carriers at the interface states between n- and p-type MOS capacitors because the effective fixed charge for MOS capacitors is determined by the sum of the fixed charge and trapped carriers at interface states. Although a large negative shift of a C–V curve is very common in the p-type SiC MOS capacitors due to

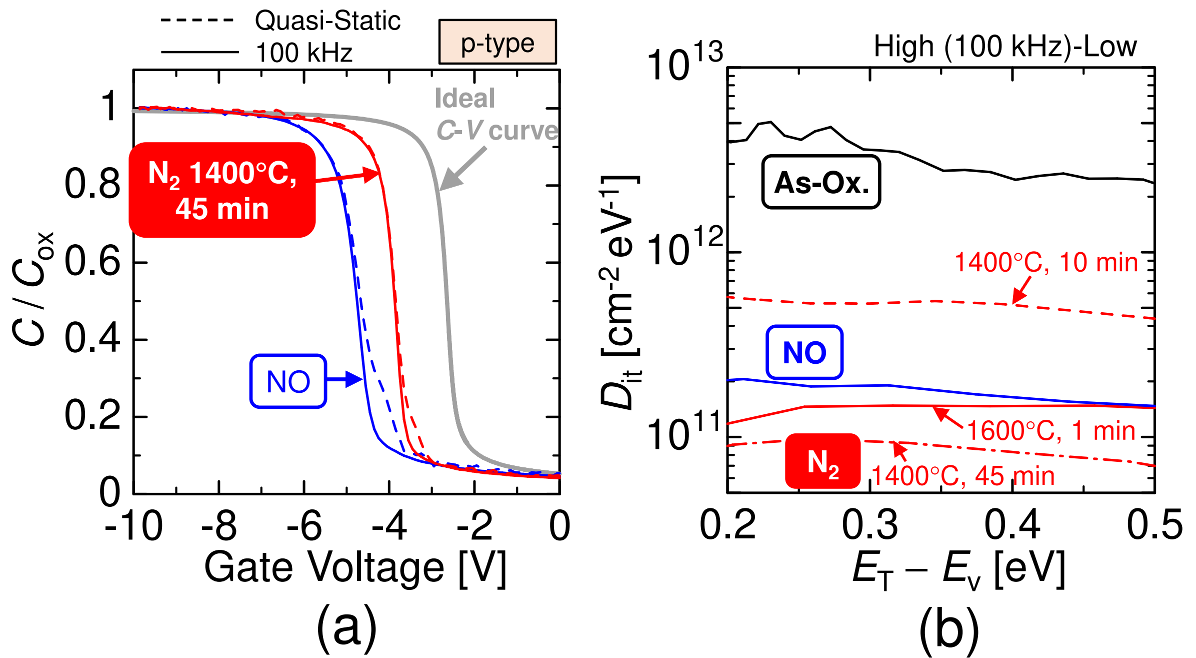

Figure 3.2: (a) Frequency dispersion of C–V characteristics obtained from the fabricated p-type SiC MOS capacitors (NO-annealed and N_2-annealed samples). The ideal C–V curve is also indicated for comparison. (b) Energy distribution of D_{it} extracted by a high (100 kHz)-low method. As-Ox. sample are not indicated because of large flat-band voltage shift of -21.5 V.

a high density of donor-like traps at the interface [20], the C–V curve acquired for the N_2-annealed sample is close to the ideal characteristic.

3.4.2 Energy Distribution of Interface State Density

The energy distributions of D_{it} near E_{v} extracted from the High(100 kHz)-Low method are plotted in Fig. 3.2 (b). As in the case of the D_{it} near E_{c}, interface properties were not effectively improved by N_2 annealing at 1400°C for 10 min. However, the samples annealed in N_2 at 1600°C for 1 min and 1400°C for 45 min showed a remarkable reduction in D_{it}. The D_{it} values are as low as about 1×10^{11} cm^{-2}eV^{-1} in the energy range from $E_{\mathrm{v}} + 0.2$ eV to $E_{\mathrm{v}} + 0.5$ eV, being lower than that of NO annealing.

3.5 Depth profile of Nitrogen Atoms near interface and inside the Oxide

In order to investigate the difference of the nitrogen concentration piled-up at the interface between NO-annealed and N_2-annealed samples, secondary ion mass spectrometry (SIMS) measurements were performed. Fig. 3.3 shows the depth profiles of the incorporated nitrogen atom density by NO annealing and N_2 annealing (1600°C, 1 min or 1400°C, 45 min). At the SiC/SiO_2 interface, the incorporated nitrogen atoms density for the N_2-annealed sample ($\sim 8 \times 10^{20}$ cm^{-3}) is slightly lower than that for the NO-annealed sample ($\sim 1.2 \times 10^{21}$ cm^{-3}). On the other hand, the density of nitrogen atoms incorporated inside the oxide by N_2 annealing (in the 10^{20} cm^{-3} range) is much higher than that by NO annealing. Note that both of the equivalent oxide thickness (EOT) and the oxide thickness measured by an ellipsometer decreased by about 0.5 nm after N_2 annealing when the relative permittivity of the gate oxide was fixed as 3.90. Assuming that the oxide thickness did not change before and after the N_2 annealing, the relative permittivity of the N_2-annealed oxide could be calculated as 3.97, being much lower than that of SiON ($\sim$ 7). On the other hand, both of EOT and the oxide thickness measured by ellipsometry for NO samples increase by 0.5 nm during the nitridation annealing, resulting in a thickness of 30.5 nm. The EOT of p-type MOS capacitors is slightly higher (by about 1 nm) than that of n-type MOS capacitors. In the case of the N_2 annealing, the nitrogen atom density inside SiO_2 gradually decreases from the surface to the interface, as shown in Fig. 3.3. Since the N_2 annealing temperature (1400 – 1600°C) is much higher than the NO annealing temperature (1250°C), nitridation of SiO_2 itself may also take place during diffusion of nitrogen toward the SiC/SiO_2 interface. For more quantitative discussion, both gas-phase reactions at high temperature and chemical reactions at the interface must be analyzed.

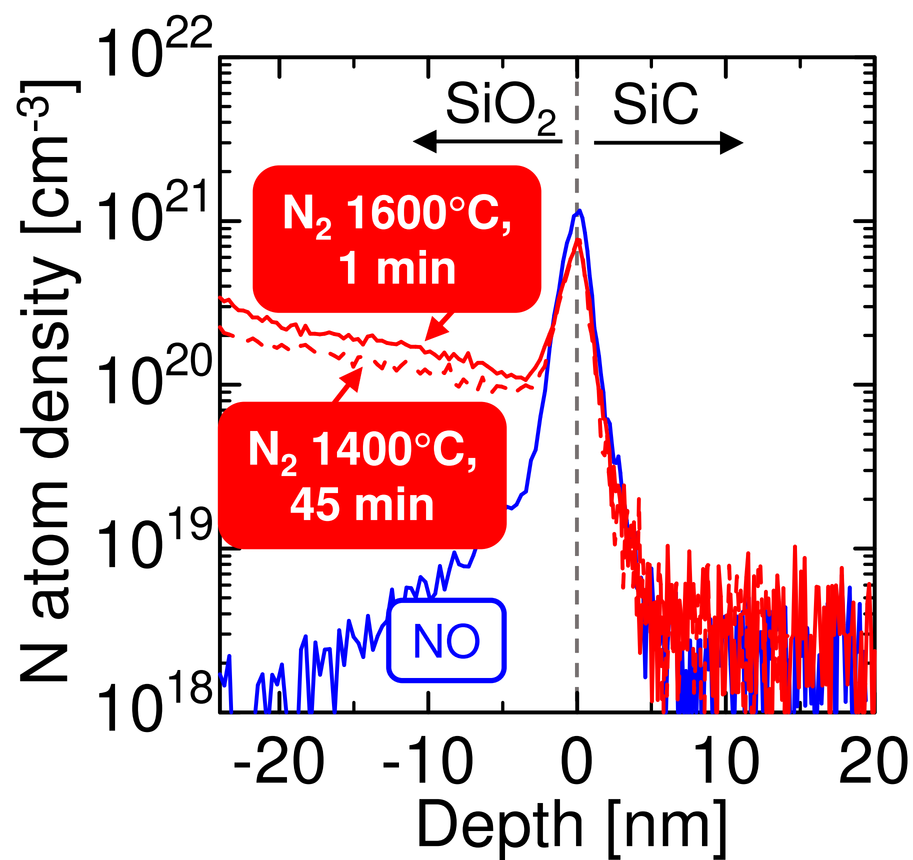

Figure 3.3: Depth profiles of nitrogen atom density near the SiC/SiO_2 interface and inside SiO_2. In the N_2-annealed samples (red lines), nitrogen atoms are incorporated inside the oxide, not only at the interface.

3.6 Dielectric Properties of Gate Insulator

3.6.1 Positive and Negative Bias-stress Instability of Flat-band Voltage

Positive bias stress instabilities were investigated by evaluating the flat-band voltage shift of the fabricated n-type SiC MOS capacitors after the intentional bias stress. Fig. 3.4 (a) shows the bias-stress time dependence of the flat-band voltage shift ($\Delta V_{\rm fb}$) of n-type SiC MOS capacitors (N_2-annealed and NO-annealed samples) at room temperature and 423 K. To assess the bias stress instability, the positive flat-band voltage shift was monitored when the positive voltage was applied to the gate of the MOS capacitors for certain periods (10, 100 and 1000 s). The initial bias stress voltage was selected as 15 V (oxide field $\sim$ 5 MV/cm). Fresh samples were used for each temperature measurement. After the voltage stress, voltage sweeping was immediately conducted to the reverse direction from the initial voltage stress without delay time. In the case of NO annealing, the C–V curve shifts toward the positive direction as the bias-stress time increases, which can be ascribed to the increase of electron trapping at defect levels inside the gate oxide, and the voltage shift becomes more significant as the temperature increases. This tendency is consistent with previous studies [15, 16]. On the other hand, in the N_2-annealed sample, the C–V curve hardly shifts with the increase in the bias-stress time. This result indicates that the positive bias-stress instability of the N_2 sample is superior to that of the NO sample.

The negative bias stress instabilities were monitored for p-type SiC MOS capacitors and the results are plotted in Fig. 3.4 (b). Fresh samples were used for each measurement and voltage sweeping was immediately conducted to the reverse direction from the initial voltage stress without delay time after the initial stress. The C–V curve shifts toward the negative direction in both the NO-annealed and N_2-annealed samples as the bias-stress time increases due to hole trapping inside the gate oxide. The value of the negative voltage shift of the N_2 sample is superior to that of the NO-annealed sample at room temperature. Furthermore, at 423 K, the NO sample exhibits about 2 $\sim$ 3 times larger $V_{\rm fb}$ shifts than the N_2 sample. The $\Delta V_{\rm fb}$ of the NO sample was -1.15 V at 423 K after 1000 second bias stress. In the case of the N_2 sample, $V_{\rm fb}$ shifted by -0.5 V. Compared with the NO-annealed sample, the negative flat-band voltage shift is much smaller in the N_2-annealed sample. The density of trapped charges by the voltage stress can be calculated as $\Delta V_{\rm fb} \times \epsilon_{\rm SiO_2}/t_{\rm EOT}$ under the assumption that hole traps are located almost at the SiC/SiO$_2$ interface. The calculated values are 6.7 $\times$ 10^{11} cm^{-2} for the NO-annealed sample and 3.8 $\times$ 10^{11} cm^{-2} for the N_2-annealed sample. These results indicate the positive and negative bias-stress instabilities of the N_2-annealed sample are superior to those of the NO-annealed sample. The flat-band shifts are different in the NO sample and the N_2 sample. It means the oxide electric field at the flat-band condition in the NO sample is different from that in the N_2 sample. Therefore, the oxide electric field does not become the same even if the bias voltages for BTI measurement are

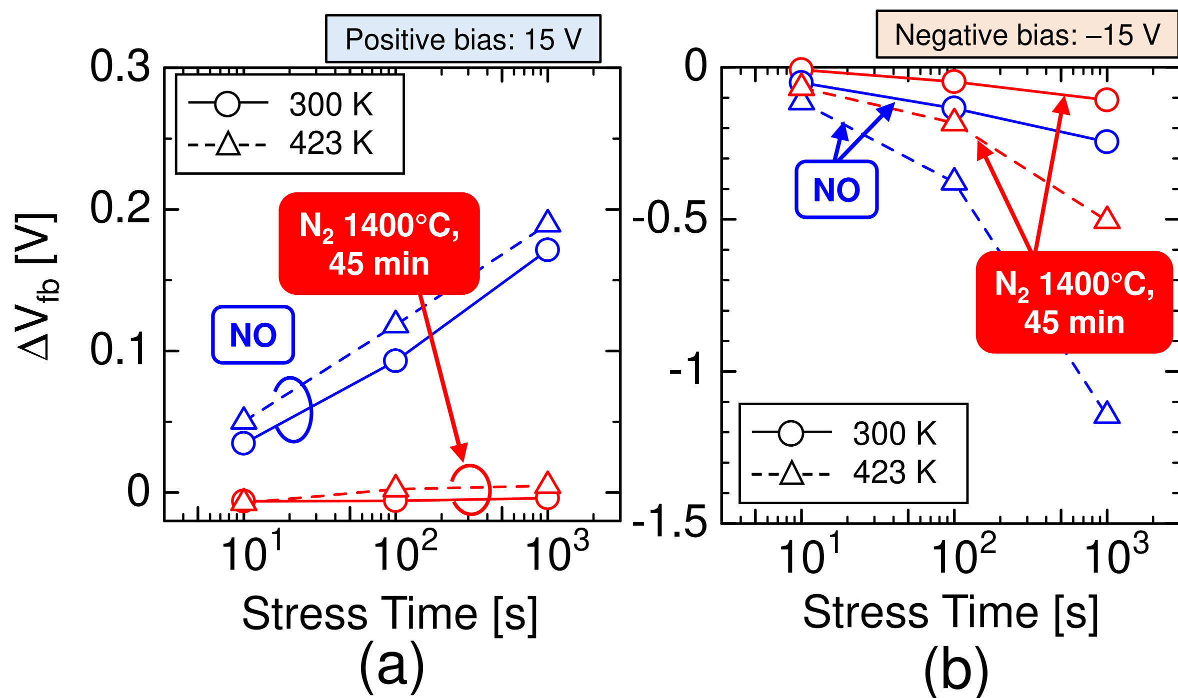

Figure 3.4: (a) Positive and (b) negative bias stress time dependence of $\Delta V_{\rm fb}$. Positive bias was sequentially applied for n-type and negative bias was sequentially applied for p-type MOS capacitors. Fresh samples were used for each temperature measurements.

selected by considering the difference in the flat-band shift. In this study, BTI test was conducted under the same bias voltage for the NO sample and the N_2 sample. Note that the difference of EOT between the NO and the N_2 samples is negligibly small. Actually, the EOT is slightly thinner (by about 2 nm) in the N_2 sample than that in the NO sample, meaning that the oxide electric field of the N_2 sample is slightly higher than that in NO sample. Hence, it does not affect the conclusion that the N_2 sample shows better BTI than the NO sample. The results of BTI characteristics for the fabricated MOSFETs are described later.

3.6.2 Dielectric Breakdown Characteristics of NO- and N_2-annealed Gate Oxides

Fig. 3.5 depicts the current-voltage (I–V) characteristics of the n-type SiC MOS capacitors under a positive-bias condition (accumulation state). The leakage current density is plotted against the electric field applied to the gate oxide. In all the samples, the leakage current density was negligibly low when the oxide field was lower than 5 MV/cm. Above 6 – 7 MV/cm, the leakage current is dominated by the Fowler–Nordheim (F–N) tunneling, indicating good quality of the gate oxides. The barrier heights for the F–N tunneling were estimated 2.8 eV for As-Ox. sample, 2.7 eV for NO sample and 2.7 eV for N_2 sample. The barrier height of As-Ox sample. is in agreement with the reported conduction band offset at the SiC/SiO_2 interface [21, 22]. The breakdown electric fields of oxides were about 11.0 – 11.5 MV/cm for the As-Ox. sample, 10.5 – 11 MV/cm for the NO sample, and 10 MV/cm for the N_2 sample (1400°C, 45 min). Compared with the As-Ox. and the NO sample, the breakdown electric fields of the N_2-annealed samples are slightly lower. However, sufficiently high breakdown electric fields (about 10 MV/cm) were obtained in the case of N_2 annealing.

3.7 Summary

Effects of high-temperature (1400 – 1600°C) N_2 annealing on the interface states of 4H-SiC/SiO_2 were investigated. It was demonstrated that high-temperature N_2 annealing is effective not only for reduction of the interface state density near the conduction band edge but also for that near the valence band edge. The interface state density near the valence band edge of the sample annealed in an N_2 ambient is 1×10^{11} cm^{-2}, which is about half of that annealed in a NO ambient.

The reliability of N_2-annealed gate oxide were also investigated. N_2-annealed gate oxide showed superior both positive and negative bias-stress instabilities, compared with those for the NO-annealed gate oxide. Sufficiently high breakdown electric fields of oxide of 10 MV/cm was obtained for the N_2-annealed gate oxide.

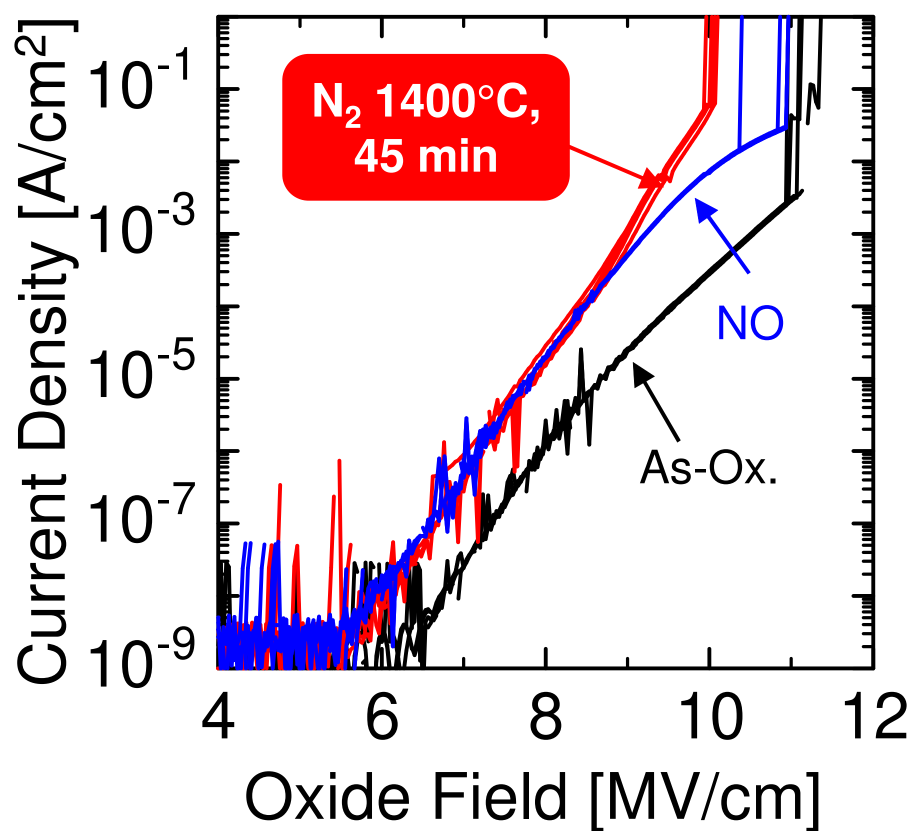

Figure 3.5: *I–V* characteristics of the prepared n-type SiC MOS capacitors. The oxide field was calculated by dividing the applied gate voltage by the effective oxide thickness.

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Chapter 4

Mobility Improvement in Both n- and p-channel 4H-SiC MOSFETs by N_2 Annealing

4.1 Introduction

As described in Chapter 3, the author succeeded in reducing the interface states near both E_c and E_v by high-temperature N_2 annealing. However, it is crucial to demonstrate that the channel mobility of N_2-annealed MOSFETs is higher than (or at least comparable to) that of NO-annealed MOSFETs to state that N_2 annealing effectively reduces D_{it}.

In this chapter, MOSFETs with performing NO or N_2 annealing are fabricated and these electrical characteristics are compared. The interface state density is also estimated from the subthreshold slopes in the MOSFETs and extracted by the C–ψ_s method for discussing the mechanism in the mobility improvement.

4.2 Experimental Details

Lateral n-channel MOSFETs were fabricated on a p-type 4H-SiC (0001) epilayer on a p-type substrate and p-channel MOSFETs were fabricated on an n-type 4H-SiC (0001) epilayer on an n-type substrate. The acceptor concentration of the p-type epilayer is 1×10^{15} cm^{-3} and donor concentration of the n-type epilayer is 8×10^{15} cm^{-3}. The gate oxide was formed in the same manner as in the case of MOS capacitors described in Chap. 3.2. Ohmic-contact annealing was conducted for both the n- and p-type MOSFETs.

4.3 Characterization of Fabricated MOSFETs

4.3.1 N-channel MOSFETs

Fig. 4.1 depicts the typical gate characteristics of the fabricated n-channel MOSFETs and the field-effect mobility at 300 K and 423 K. The channel mobility was extracted by measuring two devices with different channel lengths to exclude the influence of parasitic resistance of source and drain regions. The applied drain voltage was 0.1 V in this measurement. The peak value of field-effect mobility of the N_2-annealed (1400°C, 45 min) MOSFETs (34 cm^2/Vs) is slightly lower than that of the NO-annealed sample (40 cm^2/Vs).

As the temperature was elevated to 423 K, the peak mobility at low electric field increased to approximately 36 cm^2/Vs for the N_2-annealed MOSFET and 41 cm^2/Vs for the NO-annealed MOSFET. The I–V characteristics slightly shift to the negative direction due to the electron emission from the interface states. In order to evaluate the shift of I–V curve in the subthreshold region, the threshold voltage (V_{th}) is defined as the voltage at which drain current reaches 1×10^{-9} A. The shifts of V_{th} was −0.14 V for the NO sample and −0.25 V for the N_2 sample as the measurement temperature was raised from 300 K to 423 K. This shift is attributable to the enhanced carrier emission from the interface states at higher temperature. Compared with NO annealing, it was expected that the V_{th} was lower for the N_2-annealed MOSFET because a higher density of positive (fixed) charges was obtained with the N_2 annealing (Fig. 3.1). However, the V_{th} of the N_2-annealed MOSFET (−0.43 V) was almost comparable to that of the NO-annealed MOSFET (−0.45 V). The subthreshold swing (SS) improves from 202 mV/decade at 300 K to 147 mV/ decade at 423 K for the NO-annealed MOSFETs and from 216 mV/decade at 300 K to 156 mV for the N_2-annealed MOSFETs at 423 K. It may be attributable to the carrier emission from the interface states.

4.3.2 P-channel MOSFETs

Fig. 4.2 depicts the subthreshold characteristics of fabricated p-channel MOSFETs and the field-effect mobility at 300 K and 423 K. As expected from a lower interface state density near E_v (Fig. 3.2), N_2 annealing (1400°C, 45 min) resulted in higher field-effect mobility of 17 cm^2/Vs than that of NO annealing (13 cm^2/Vs). This channel mobility is the highest among the reported mobilities of p-channel SiC MOSFETs (e.g. 15.6 cm^2/Vs obtained by wet oxidation [1] and 13 cm^2/V by ultrahigh-temperature oxidation [2]). The SS improves from 223 mV/decade to 204 mV/decade for the NO sample and from 177 mV/decade to 156 mV/decade for the N_2 sample respectively as temperature rises from 300 K to 423 K. V_{th} shifted to the positive direction as the measurement temperature was raised from 300 K to 423 K and the V_{th} shift was +0.32 V for the NO sample and +0.27 V for the N_2 sample. The positive shift of V_{th} at elevated temperature indicates hole emission from the interface states. Both NO- and N_2-annealed MOSFETs show the comparable threshold

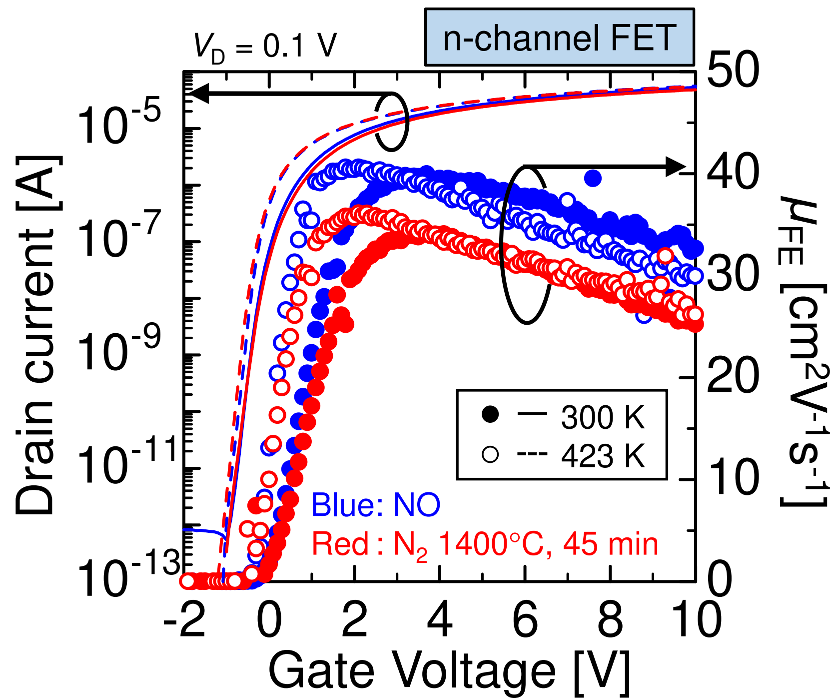

Figure 4.1: Subthreshold characteristics and field-effect mobility as a function of the gate voltage of fabricated NO- and N_2-annealed n-channel MOSFETs at 300 and 423 K.

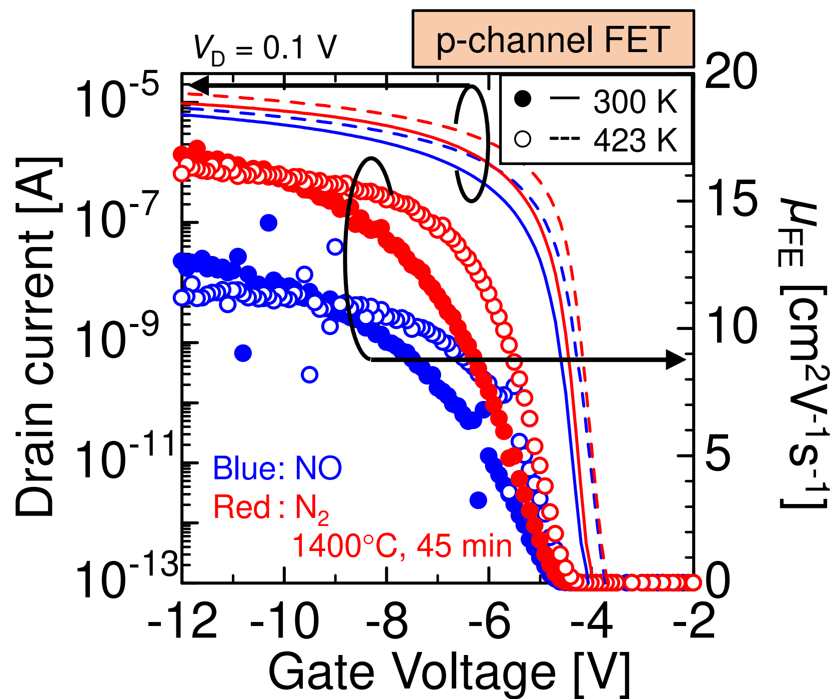

Figure 4.2: Subthreshold characteristics and field-effect mobility as a function of the gate voltage of fabricated NO- and N_2-annealed p-channel MOSFETs at 300 and 423 K.

voltages. On the other hand, the flat-band voltages in the NO-annealed MOS capacitors are different from those in the N_2-annealed MOS capacitors. The oxide and semiconductor electric fields in the subthreshold state for MOSFETs differ from those in the flat-band state for MOS capacitors. Thus, the threshold voltage of the MOSFETs does not match the flat-band voltage of the MOS capacitors because the amount of trapped carriers inside SiO_2 is different for MOSFETs and MOS capacitors (Figs. 3.1 and 3.2).

If N atoms act as dopants, the flat-band voltage of p-type MOS capacitors shifts to the negative direction. Also, the threshold voltage of p-channel MOSFETs should shift to a more negative direction and the channel mobility becomes lower when N atoms act as surface dopants. Hence, the possibility of N atoms acting as surface dopants can be excluded. It has been recently reported that a short time NO annealing is better for p-channel MOSFETs [3]. Further studies are required for optimization of both NO and N_2 annealing condition for p-channel MOSFETs. In order to verify that BTI of the fabricated MOSFETs shows a similar trend with the case of the MOS capacitors. PBTI and NBTI characteristics were evaluated by monitoring the threshold voltage shift after the bias stress of ± 12 V for 1000 s. In the case of PBTI, the magnitude of the threshold voltage shift was negligibly small (< 0.1 V) for both the N_2-annealed and the NO-annealed n- and p-channel MOSFETs. In the case of NBTI, the threshold voltage showed a negative shift of $-$ 0.2 V for both the N_2-annealed and the NO-annealed n- and p-channel MOSFETs after the intentional bias stress. Based on these results, the author concluded that the BTI characteristics of the N_2-annealed MOSFETs are almost similar to those of the NO-annealed MOSFETs though the N_2-annealed MOS capacitor shows slightly superior BTI characteristics than the NO-annealed MOS capacitor. For practical use, further studies of bias-stress instability for MOSFETs are required.

4.4 Discussion

In SiC MOSFETs, a high density of interface states is considered to be a main limiting factor of low channel mobility. The high D_{it} near E_{c} ($> 10^{12}$ cm^{-2}eV^{-1} at $E_{\mathrm{c}} - E_{\mathrm{T}} = 0.2$ eV) is effectively reduced (to $\sim 10^{11}$ cm^{-2}eV^{-1} at $E_{\mathrm{c}} - E_{\mathrm{T}} = 0.2$ eV) by a nitridation process in the case of evaluation by the High–Low method. However, the High–Low method generally underestimates the interface state density for the following reasons [4]. (1) The High–Low method cannot monitor fast states which respond faster than the high probing frequency. (2) A large standard deviation of surface potential, which is peculiar to SiC MOS structure, causes considerable dispersion of response time of interface states. Moreover, it is well known that D_{it} near E_{c} at nitrided SiC/SiO_2 on the Si face is significantly underestimated by the High–Low method, because a substantial amount of fast interface states are generated by nitridation [5, 6]. Then, it is highly desirable to characterize energy distributions of D_{it} by other techniques. In this paper, D_{it} was also estimated from a subthreshold slope (SS) of

the fabricated MOSFETs. SS is defined by the following formula [7]:

$$\mathrm{SS} = \frac{dV_\mathrm{G}}{d(\log_{10} I_\mathrm{D})} = \frac{kT}{e}\ln 10 \frac{C_\mathrm{ox} + C_\mathrm{D} + e^2 D_\mathrm{it}}{C_\mathrm{ox}}, \tag{4.1}$$

where e is the elementary charge, T is the temperature in Kelvin, k is the Boltzmann constant, C_ox is the oxide capacitance, and C_D is the semiconductor capacitance. From equation (4.1), D_it can be estimated, the energy level of which is about 0.3 – 0.6 eV away from E_c or E_v (weak inversion). For estimating the energy range of D_it corresponding to the drain current, the relationship between the surface Fermi energy (E_fs) and the drain current is used. Drain current in the subthrehold region is approximately expressed by [7]

$$I_\mathrm{D,subthrehold} = \frac{W}{L} e\mu n_\mathrm{free}(E_\mathrm{fs}) V_\mathrm{D}, \tag{4.2}$$

where μ is the drift mobility, n_free is the density of free carriers, and V_D is the drain voltage. Here, the mobilities of electrons [8] and holes [3] were assumed to be constant and two-dimensional density of states (2D-DOS) was considered for calculation of the density of free electrons [9].

Fig. 4.3 (a) and (b) illustrate the estimated D_it plotted against the drain current for the n- and p-channel MOSFETs. The estimated energy levels of D_it at a given drain current region are also indicated. The estimated energy range of D_it is not much affected by the assumed mobility of carriers. In the case of n-channel MOSFETs, D_it is slightly higher in the N_2-annealed MOSFET than in the NO-annealed MOSFET, which is a similar tendency to the results acquired for n-type MOS capacitors (Fig. 3.1 (b)). The values of D_it evaluated from SS are about an-order-of-magnitude higher than D_it extracted by the High–Low method from the MOS capacitors. In the case of p-channel MOSFETs, the derived D_it from SS in the N_2-annealed MOSFETs is lower than that in the NO-annealed MOSFETs. There also exists discrepancy that D_it estimated from SS is about 10 times higher than that from the C–V characteristics of MOS capacitors as in the case of near E_c (Fig. 3.2 (b)) The author speculates that this discrepancy is attributable to the fast states created by nitridation and fluctuation of surface potential [4, 6].

In order to discuss more detail, energy distribution of D_it was also acquired by the C–ψ_s method from the MOS capacitors [10]. Fig. 4.4 (a) and (b) depict the comparison of the D_it energy distributions extracted by the High–Low method and the C–ψ_s method near E_c and E_v, respectively. In the C–ψ_s method, the integration constant was determined so that the linear relationship between $1/{C_\mathrm{hf}}^2$ and ψ_s coincides with the ideal relationship of $1/{C_\mathrm{D}}^2$ and ψ_s [10]. Where C_hf is the high-frequency capacitance, C_D is the ideal depletion capacitance, and ψ_s is the surface potential. D_it is shown up to the energy level of 0.3 eV from E_v. It was difficult to evaluate the shallow D_it accurately by the C–ψ_s method when the high-frequency in the C–V measurement was selected as 100 kHz due to the high resistivity of the p-type substrate. D_it estimated by the C–ψ_s method is about 6-10 times higher than that by the High–Low method for both n- and p-type MOS capacitors. On the other hand, the values

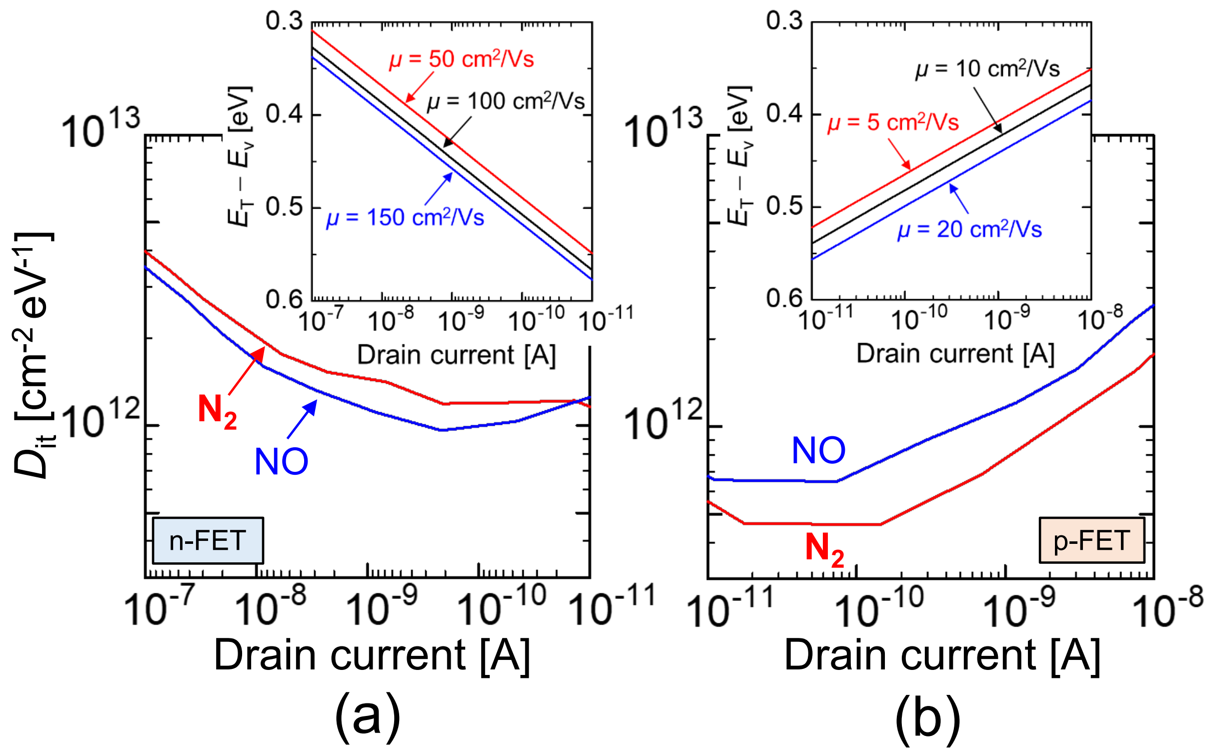

Figure 4.3: $D_{\rm it}$ extracted from subthreshold slopes plotted against drain current for (a) n-channel MOSFETs and (b) p-channel MOSFETs. The energy range of $D_{\rm it}$ corresponding to drain current was roughly calculated (insets). The energy range of $D_{\rm it}$ extracted by SS values is estimated at approximately 0.6 eV $> E_{\rm c}-E_{\rm T}$ or $E_{\rm T}-E_{\rm v} >$ 0.3 eV for the drain current of 10^{-11}–10^{-7} A.

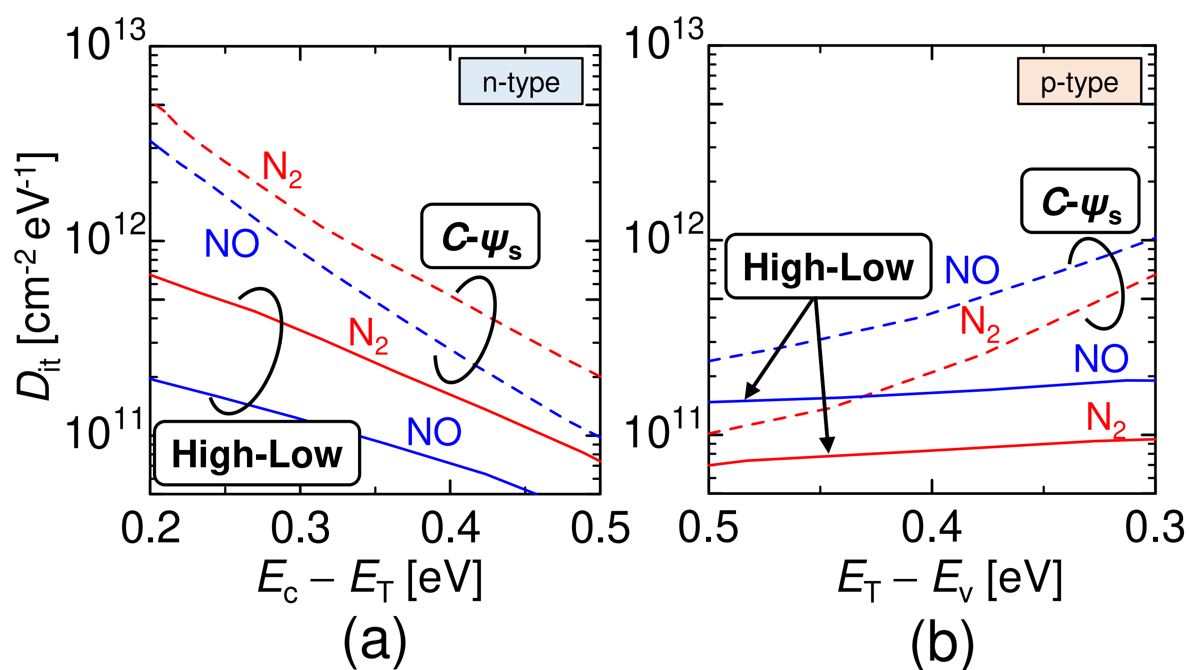

Figure 4.4: Comparison of the D_{it} energy distributions extracted by the High–Low method and the C–ψ_s method near (a) E_c and (b) E_v from MOS capacitors (NO and N_2 (1400°C, 45 min)).

of D_{it} evaluated from SS are almost comparable to (slightly higher than) D_{it} estimated by the C–ψ_{s} method for the MOS capacitors. These results indicate that there exist fast states not only near E_{c} but also near E_{v} and these fast states actually influence the characteristics and channel mobilities of both n- and p-channel SiC MOSFETs.

It is believed that NO annealing is considered to create hole traps in the SiC/SiO_2 [11] and the hole traps increase with increasing the amount of incorporated N atoms [11, 12]. It is also reported that the field-effect mobility and hole mobility of a NO-annealed p-channel MOSFET decreases with increasing the annealing time [3]. These previous reports suggest that excess nitridation of SiC/SiO_2 induce lowering p-channel mobility. From the SIMS results, the amount of N atoms incorporated at SiC/SiO_2 by N_2 annealing is less than that by NO annealing. This is one of the speculations that the higher channel mobility is attributable to the lower density of N atoms piled up at SiC/SiO_2 by N_2 annealing, compared with that by NO annealing.

4.5 Summary

The author has investigated effects of N_2 annealing on the interface properties of SiC/SiO_2. High-temperature (1400 – 1600°C) N_2 annealing has much potential to improve the interface properties at a similar level to the NO annealing without using a toxic gas. In particular, N_2 annealing effectively reduces the D_{it} near E_{v}, and the field-effect mobility of p-channel MOSFETs reaches 17 cm^2/Vs, being about 30 % higher than that of the NO-annealed MOSFETs. Bias temperature instability of the MOSFETs annealed in an N_2 ambient is almost similar to that of the MOSFETs annealed in a NO ambient. These results indicate that high-temperature N_2 annealing is one of the promising candidates for fabricating SiC-based complementary MOS (CMOS) integrated circuits because the performance of CMOS is principally limited by p-channel MOSFETs having lower channel mobility than n-channel MOSFETs.

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Chapter 5

Formation of High-Quality SiC/SiO_2 Structure by Oxidation-Minimized Process

5.1 Introduction

It has been demonstrated that N_2 annealing is as effective as NO annealing for the reduction in D_{it} at the SiC/SiO_2 structure. Both of NO and N_2 annealing can improve the channel mobility of n-channel MOSFETs from 3–5 to 30–40 cm^2/Vs. However, further improvement is necessary to take full advantage of the potential of SiC.

As described in Chapter 4, various studies have been conducted to improve the channel mobility, and it has been experimentally demonstrated that several passivation methods after oxide formation are effective to improve the interface quality [1–20]. These trials are roughly divided into three categories: (1) the incorporation of particular atoms at the SiC/SiO_2 interface (e.g., nitrogen (N) [1–7], hydrogen (H) [8], phosphorous (P) [9, 10], and boron (B) [11]), (2) metal-enhanced oxidation (e.g., sodium (Na) [12, 13]) and barium (Ba) [14–16])), and (3) the use of Al-based high-k dielectrics (e.g. Al_2O_3 [17–19], and AlON [20]). Although some methods (P, B, Na, Ba, and Al_2O_3) achieve a significant increase in the channel mobility (> 70 cm^2/Vs), these methods are not suitable for MOSFETs production due to the severe bias-temperature instability (caused by mobile ions or trapping of injected carriers in the gate oxide), high leakage current (due to the small conduction band offset), and low breakdown electric field (formation of defects inside the oxide).

Although the origin of the high D_{it} for SiC/SiO_2 structures has not yet been identified, it has been widely considered that carbon atoms that remain at the interface are plausible candidates [21–23]. Recent theoretical calculations support this speculation and suggest that carbon defects most likely form defect levels near the conduction-band edge [22, 23]. It was also theoretically predicted that conduction band fluctuation is another possible origin of high D_{it} [24, 25]). Therefore, the key to obtaining a high-quality SiC/SiO_2 interface may

be the formation of SiO_2 on SiC without formation of carbon-related defects and crystalline disorder. Thus, one solution may be elimination of oxidation from the SiO_2 formation process as much as possible. The authors group has reported that a significantly lower $D_{\rm it}$ can be obtained by creating a SiC/SiO_2 structure via Si deposition [26]. In this process, a gate oxide was created by the following process. First, a thin Si film was deposited on a SiC surface after H_2 etching. Then, SiO_2 was formed by oxidation of Si at a low temperature (750°C). Finally, interface nitridation was conducted.

In this chapter, the author proposes another approach to exclude oxidation process for SiO_2 formation using chemical vapor deposition (CVD). In addition to suppressing SiC oxidation, the author found that H_2 etching in Si-rich ambient plays a vital role in reducing $D_{\rm it}$ near $E_{\rm c}$ of SiC. The author discusses the possible mechanism of the significant reduction in $D_{\rm it}$ based on experimental results.

5.2 Reduction in Interface States by H_2 Etching prior to Formation of Gate Oxide on (0001)

5.2.1 Experimental Details

MOS capacitors were formed on n-type 4H-SiC (0001) epilayers (donor density: 1×10^{16} cm^{-3}). The processing conditions for gate oxide formation are indicated in Fig. 5.1. H_2 etching was performed for some samples at 1350°C for 15 min. After H_2 etching, sacrificial oxidation was performed at 1300°C for some samples (the oxide thickness was about 18 nm and was removed by buffered HF). Some samples were etched in H_2 ambient again. The gate oxides were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400°C, resulting in an oxide thickness of 20–30 nm. Then, high-temperature N_2 annealing at 1400°C for 45 min or Ar annealing at 1400°C for 10 min was performed. Finally, circular Al electrodes were deposited (diameter: 300–500 μm). Designations for the prepared samples are indicated in Fig. 5.1. For comparison, MOS capacitors with SiO_2 (thickness: 30 nm) formed by dry oxidation (+ NO annealing) were prepared. The sample not subject to annealing is designated "As-Ox".

5.2.2 Capacitance-Voltage Characteristics

Fig. 5.2 (a) depicts the quasi-static and 1-MHz capacitance–voltage (C–V) characteristics of the MOS capacitors at 300 K. High-frequency and quasi-static C–V characteristics were simultaneously measured using KEITHLEY 82 C–V System. Voltage sweeping was conducted from the depletion side to the accumulation side. In the figure, the ideal C–V curve with an oxide thickness of 25 nm and a donor density of 1×10^{16} cm^{-3} is also indicated for comparison. A large frequency dispersion is observed for the As-Ox sample. The dispersion is well reduced in the CVD-N_2 sample and further suppression is achieved by performing H_2

Figure 5.1: Processes for fabrication of gate oxide. The designations for the fabricated samples are also indicated.

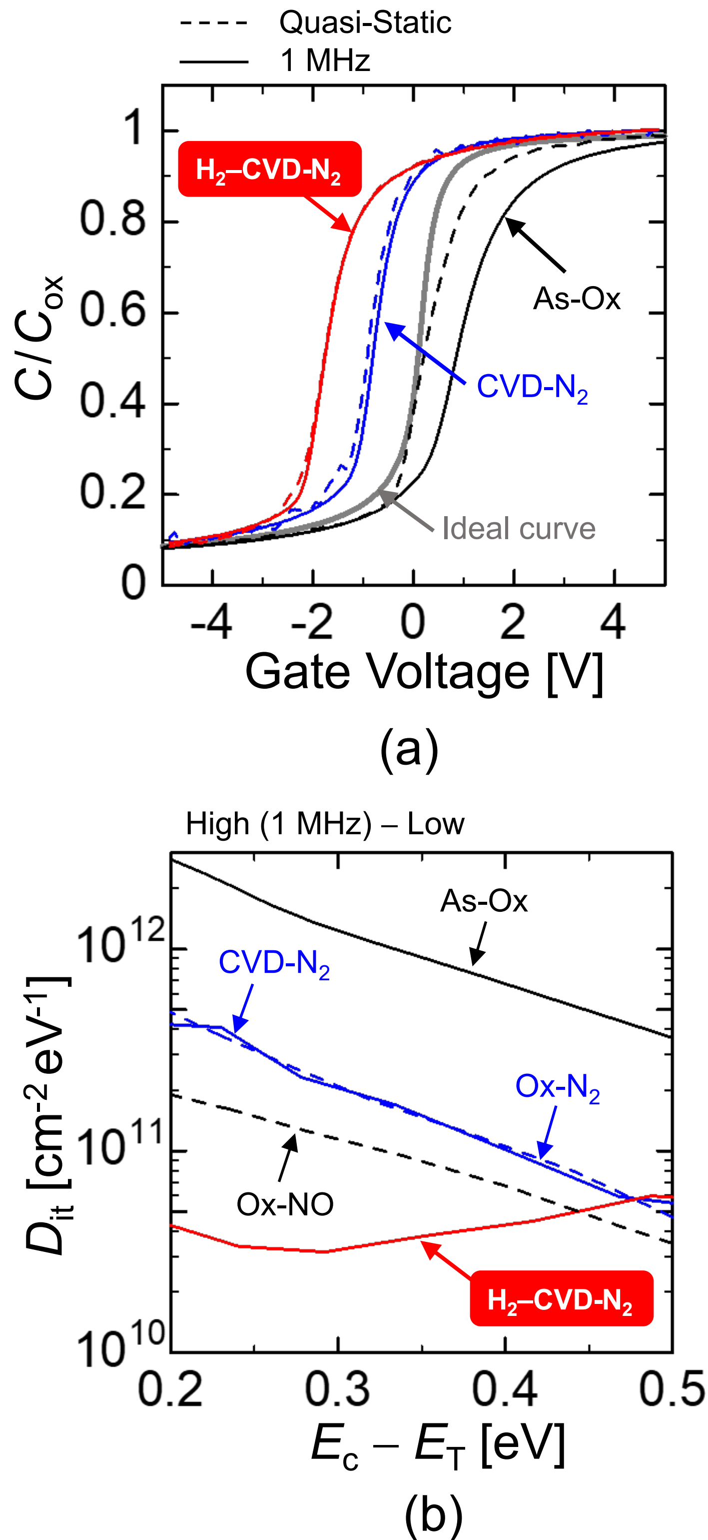


Figure 5.2: (a) Quasi-static and 1-MHz C–V characteristics of the prepared MOS capacitors. The ideal C–V curve is also indicated for comparison. (b) Energy distribution of D_{it} extracted by the high (1 MHz)-low method. A substantial reduction in D_{it} is achieved when H_2 etching is performed before SiO_2 deposition.

etching prior to SiO_2 deposition (H_2-CVD-N_2 sample). The densities of the effective fixed charge estimated from the flat-band voltage shifts are 6.7×10^{11} cm^{-2} (negative), 7.5×10^{11} cm^{-2} (positive), and 1.7×10^{12} cm^{-2} (positive) for the As-Ox. sample, the CVD-N_2 sample, and the H_2-CVD-N_2 sample, respectively.

5.2.3 Energy Distribution of Interface State Density

Figure 5.2 (b) illustrates the energy distributions of D_{it} estimated by a high (1 MHz)–low method. Note that the hysteresis of the C–V characteristics was negligibly small and the energy distribution of D_{it} was almost uniquely determined regardless of the sweeping direction. Compared with the As-Ox sample, a ten-fold reduction in D_{it} is achieved in the N_2-annealed samples with the SiO_2 formed by either SiC oxidation or SiO_2 deposition. The D_{it} for the N_2 sample is comparable to that of the CVD-N_2 sample. As expected from the C–V characteristics (Fig. 5.2 (a)), a marked reduction in D_{it} is achieved by performing H_2 etching prior to SiO_2 deposition (about 4×10^{10} cm^{-2}eV^{-1} at E_c– 0.2 eV). The D_{it} value is about one order-of-magnitude lower than the reported D_{it} for an N_2-annealed sample with a pre-annealing process (4×10^{11} cm^{-2}eV^{-1} at E_c– 0.2 eV) [41] and for the NO sample.

To clarify that SiC oxidation increases D_{it}, the author performed sacrificial oxidation after the H_2 etching. Figure 5.3 (a) shows the effect of sacrificial oxidation on D_{it}. The figure shows that D_{it} is not effectively reduced when sacrificial oxidation was performed after H_2 etching (and prior to SiO_2 deposition: H_2-Ox-CVD-N_2), though D_{it} energy distribution is reduced when H_2 etching was performed again after sacrificial oxidation (H_2-Ox-H_2-CVD-N_2). It was also confirmed that the D_{it} energy distribution was not reduced when SiO_2 was formed by oxidation after H_2 etching (H_2-Ox-N_2).

The following summarizes the above experimental results: (1) A substantial reduction of D_{it} is achieved by H_2 etching prior to SiO_2 CVD. (2) SiC oxidation results in higher D_{it} even after performing H_2 etching. (3) Even after SiC oxidation, D_{it} decreases when H_2 gas etching is performed again. Based on the above results, the author considers that oxidation creates a high density of defects on the SiC surface and these surface defects are the major origin of a high D_{it} at the SiC/SiO_2 interface.

Next, high-temperature Ar annealing was performed instead of N_2 annealing to investigate whether N_2 annealing is necessary for reducing the interface states. Figure 5.3 (b) depicts a comparison of the energy distribution of D_{it} for N_2-annealed and Ar-annealed MOS capacitors. For Ar annealing, D_{it} is relatively high (1×10^{12} cm^{-2}eV^{-1}at $E_c - 0.2$ eV). It was also performed that forming gas annealing (H_2/N_2: 1/9) at 800°C for 2 min after Ar annealing. However, this resulted in only a slightly lower D_{it} than when only Ar annealing was performed.

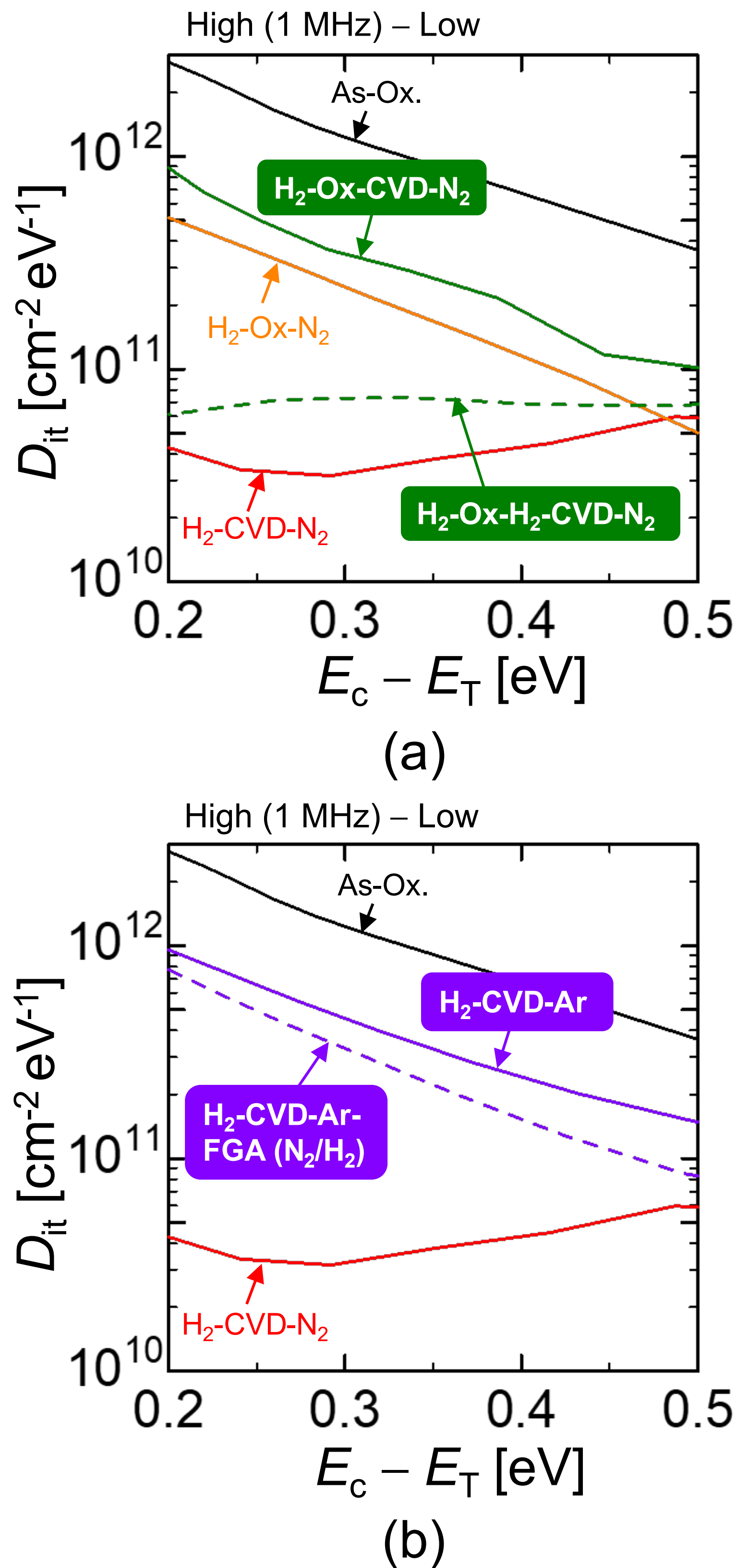


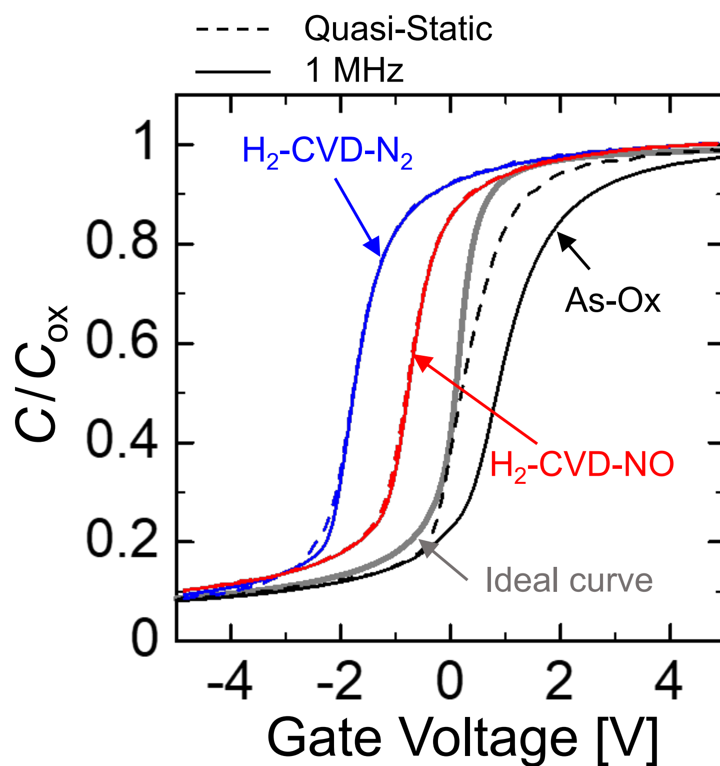
Figure 5.3: Energy distribution of D_{it} extracted by the high (1 MHz)-low method for the prepared MOS capacitors. (a) Comparison with the case with sacrificial oxidation performed after the H_2 etching. The SiO_2 formed by oxidation was removed by BHF before the CVD. (b) Effect of Ar annealing (+ N_2/H_2 FGA) instead of N_2 annealing after the SiO_2 deposition.

5.3 NO and N_2 annealing after SiO_2 deposition

In the previous sections, the author have shown that N_2 annealing after the formation of gate oxide is necessary for obtaining low $D_{\rm it}$. In this subsection, the author describes the C–V characteristics and energy distribution of $D_{\rm it}$ in the case of nitridation with NO or N_2 annealing after formation of gate oxide.

Fig. 5.4 (a) shows the quasi-static and 1 MHz capacitance–voltage (C–V) characteristics of the H_2-CVD-NO and the H_2-CVD-N_2 samples. The C–V curve of the As-Ox sample and ideal C–V characteristics of an oxide thickness of 25 nm and a donor density of 1×10^{16} $\rm cm^{-3}$ are also depicted for comparison. The capacitance equivalent thicknesses (CETs) were 31 nm, 30 nm, and 22 nm for the As-Ox, the H_2-CVD-NO, and the H_2-CVD-N_2 samples, respectively. The As-Ox sample shows a large discrepancy between the quasi-static and the 1 MHz C–V characteristics. On the other hand, the quasi-static C–V curves are almost coincident with the 1 MHz C–V curves for both the H_2-CVD-NO and the H_2-CVD-N_2 samples, which indicates a substantial reduction in $D_{\rm it}$. Compared with the ideal C–V curve, a negative flat-band voltage shift was observed for the H_2-CVD-NO and the H_2-CVD-N_2 samples. The densities of the effective fixed charge extracted from the flat-band voltage shifts were 6.7×10^{11} $\rm cm^{-2}$ (negative), 5.1×10^{11} $\rm cm^{-2}$ (positive), and 1.7×10^{12} $\rm cm^{-2}$ (positive) for the As-Ox, the H_2-CVD-NO, and the H_2-CVD-N_2 samples, respectively. The negative shift is reduced in the H_2-CVD-NO sample, compared with that in the H_2-CVD-N_2 sample.

The energy distributions of $D_{\rm it}$ estimated by a high (1 MHz)–low method are given in Fig. 5.4 (b). The results for the MOS capacitors with thermally oxidized SiO_2 with NO or N_2 annealing are also shown for comparison. As expected from the C–V curves, H_2 etching before SiO_2 deposition provides a substantial improvement in the interface quality. $D_{\rm it}$ for the H_2-CVD-NO sample (6×10^{10} $\rm cm^{-2}eV^{-1}$) was almost equivalent to (slightly higher than) that of the H_2-CVD-N_2 sample (4×10^{10} $\rm cm^{-2}eV^{-1}$) at $E_{\rm c} - 0.2$ eV. In the above discussion, thermal oxidation was suggested to create C-related defects or to induce disorder of the SiC crystal near the surface, and these are the possible origins of the high $D_{\rm it}$. These defects introduced by sacrificed oxidation are considered to be effectively removed by the H_2 etching before the SiO_2 deposition, leading to substantial reduction in $D_{\rm it}$. The SiO_2 thickness is increased by a sub-nanometer during NO annealing. As such, both the equivalent oxide thickness and the oxide thickness measured by ellipsometry for the Ox-NO sample were increased by 0.5 nm after NO annealing. It can be inferred from the increase in the SiO_2 thickness by 0.5 nm that one Si-C bilayer is oxidized during NO annealing. In previous reports [17, 19], a significant increase in the channel mobility was demonstrated for Al_2O_3/SiO_2/SiC MOSFETs. when the SiO_2 thickness was about 1 nm and the mobility was significantly decreased when the SiO_2 thickness was thicker than 2 nm. Based on these results, it was speculated that ultra-thin SiO_2 formation by oxidation ($<$1 nm thickness) does not seriously degrade the interface properties.



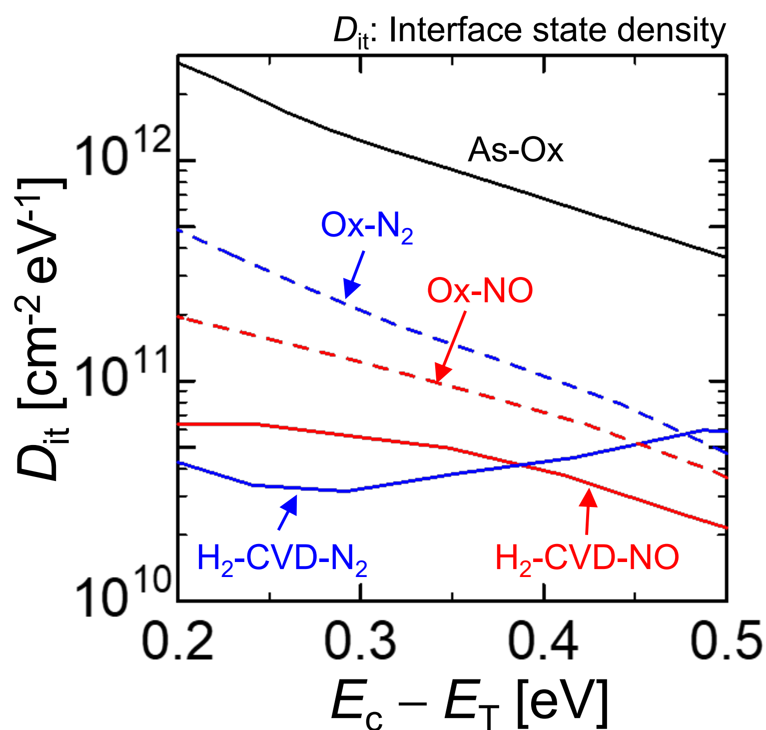


Figure 5.4: (a) Quasi-static and 1 MHz C–V characteristics of the prepared MOS capacitors. Ideal C–V characteristics with a donor density of 1×10^{16} cm^{-3} are also indicated for comparison. (b) Energy distribution of $D_{\rm it}$ extracted by the high (1 MHz)-low method.

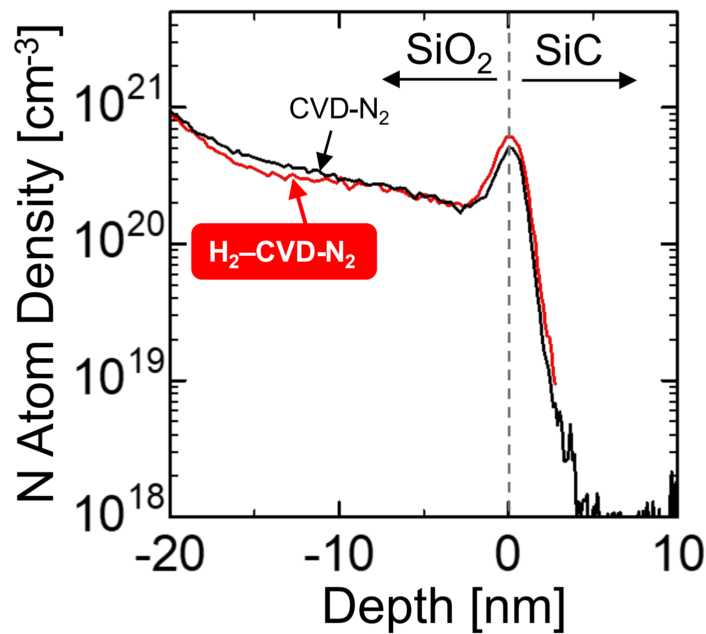
5.3.1 Depth Profile of Nitrogen Atoms near the Interface and inside the Oxide

To evaluate the nitrogen atom profiles near the interface, secondary ion mass spectrometry (SIMS) measurements were performed after depositing SiO_2 and nitridation. Figure 5.5 (a) shows the depth profiles for the nitrogen atom density in samples with and without H_2 etching (CVD-N_2 and H_2-CVD-N_2). The depth profiles for N atoms are almost identical in CVD-N_2 and H_2-CVD-N_2. Figure 5.5 (b) shows the results for NO and N_2 samples for comparison. The nitrogen atom density incorporated at the interface was comparable among all the samples (7–10$\times10^{20}$ cm^{-3}). Inside the oxide, N_2 annealing induced a much higher nitrogen atom density (1$\times10^{20}$ cm^{-3}) than when NO annealing was performed. Note that the density of N atoms inside the oxide film was about 5-10 times higher in the H_2-CVD-N_2 sample than in the Ox-N_2 sample. This may arise from the difference in the properties of the oxide films formed by thermal oxidation and deposition. For example, a SiO_2 film formed by deposition at low temperature becomes relatively oxygen-poor. Although the mechanism for the large negative flat-band voltage shift in the H_2-CVD-N_2 sample is unclear at present, a high density of nitrogen atoms introduced inside the oxide may be the possible origin.

Here, the author briefly summarizes the key points in common between this study and our previous work [26] for obtaining low D_{it}. There are three common processes: (1) H_2 etching, (2) SiO_2 formation without oxidation, and (3) interface nitridation. The author concludes that all of these processes are necessary for a substantial decrease in D_{it}.

5.4 Dielectric Properties of Gate Insulator

Fig. 5.6 (a) shows bi-directional 1-MHz C–V curves measured for the H_2-CVD-N_2 sample (EOT $\sim$ 20 nm) at 448 K. Before voltage sweeping, a bias voltage of 10 (5 MV/cm) or $-$ 10 V was applied for 600 s. Voltage sweeping was immediately conducted in the reverse direction from the initial voltage after the bias stress. The bi-directional C–V curves show a negligibly small hysteresis, meaning that the density of mobile ions and electron traps inside the oxide is negligibly small. Note that the density of holes at the MOS interface without light illumination is extremely low due to the wide bandgap of SiC. Hence, only the electron trapping is evaluated in this measurement. Fig. 5.6 (b) depicts the current–voltage ($I-V$) characteristics of the prepared SiC MOS capacitors under a positive-bias condition (accumulation state). For comparison, the I–V characteristics of the As-Ox, Ox-NO, and Ox-N_2 samples are also indicated. Above 6–7 MV/cm, a Fowler–Nordheim (F–N) tunneling current is observed. The breakdown characteristics of the gate oxide for the H_2-CVD-NO sample and the H_2-CVD-N_2 sample show a similar tendency with the Ox-NO and the Ox-N_2 samples and the obtained breakdown electric fields are about 10.5 MV/cm for the H_2-CVD-N_2 sample and 11.5 MV/cm for the H_2-CVD-NO sample.



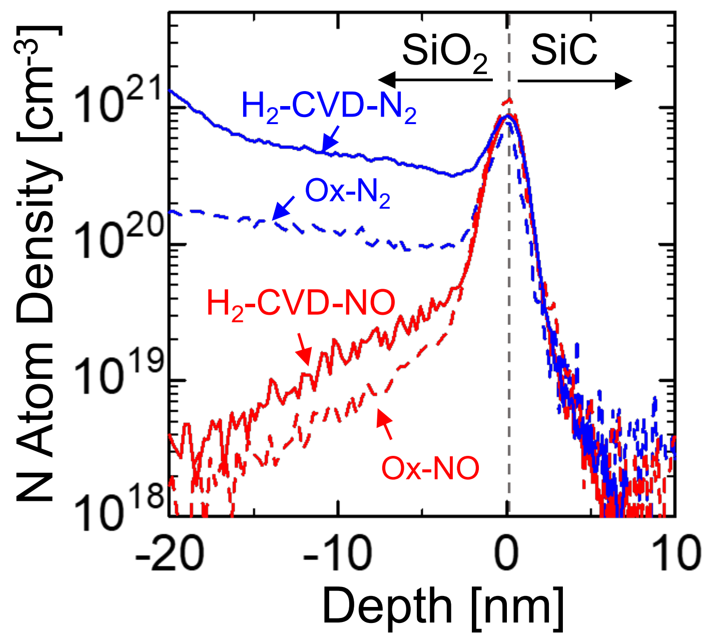
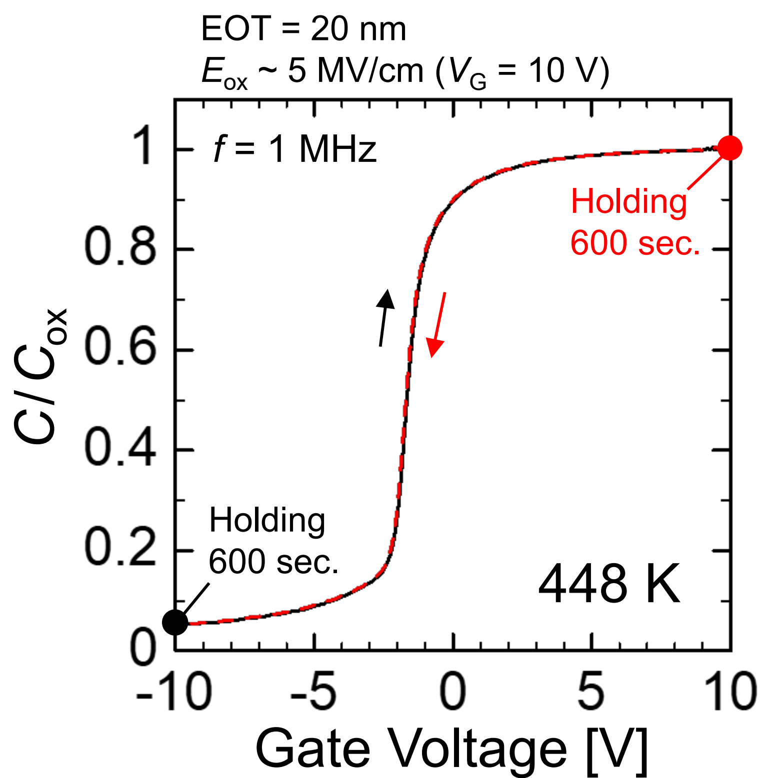


Figure 5.5: Depth profile of nitrogen atoms for N_2-annealed SiC/SiO_2 structures obtained by SIMS for (a) comparison with and without H_2 etching before the SiO_2 deposition and (b) comparison with the N_2- or NO-annealed SiC/SiO_2 structure by thermal oxidation. H_2 etching does not affect the amount of accumulated N atoms at the interface.



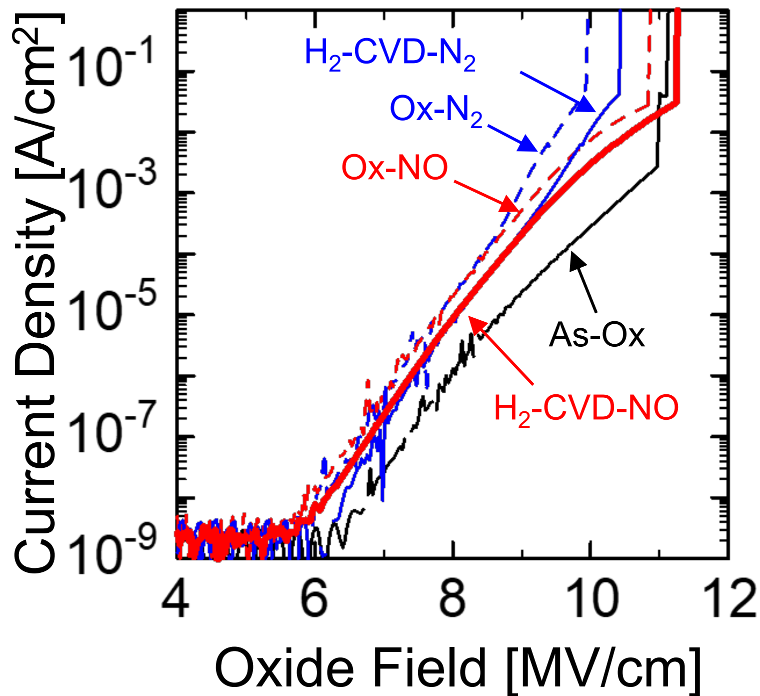


Figure 5.6: (a) Bi-directional C–V characteristics at 448 K after a bias stress of + 10 V (− 10 V) for 600 sec. (b) Breakdown characteristics for the prepared MOS capacitors in the accumulation state.

5.5 H_2 etching in Si-rich Ambient

So far, it has been shown that H_2 etching prior to SiO_2 deposition is the key to achieve significant reduction in D_{it}. However, the author found that the effects of H_2 etching on lowering D_{it} became less and less as H_2 etching performed. In this study, H_2 etching has been performed in a Hot-Wall chemical vapor deposition system (HW-CVD), which was also used for homoepitaxial growth of SiC. There was a possibility that Si remained in the furnace and its memory effects played an important role to reduce D_{it}. Thus, the author investigated whether H_2 etching in Si-rich environment is the key to reduce interface defects.

5.5.1 Experimental Details

MOS capacitors were formed on n-type 4H-SiC (0001) epilayers (donor density: 1×10^{16} cm^{-3}). After RCA cleaning, samples were loaded in HW-CVD system. In the HW-CVD system, H_2 etching (1350°C) was performed. The detailed process condition is described later. The gate oxides were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400°C, resulting in an oxide thickness of 30 nm. Then, NO annealing at 1250°C for 70 min was performed. Finally, circular Al electrodes were deposited (diameter: 300–500 μm). The sample not subject to H_2 etching is designated "CVD-NO".

In order to find out whether H_2 etching in Si-rich ambient is key process for obtaining low D_{it} or not, H_2 etching was performed in the following two conditions. 1. Si piece was intentionally loaded in the furnace during H_2 etching (H_2-CVD-NO w/ Si). 2. A small amount of SiH_4 flowed in to the reactor (H_2 = 5 slm, SiH_4 = 1 sccm, 100 Torr) during H_2 etching (H_2/SiH_4-CVD-NO). Note that samples etched in H_2 and SiH_4 ambient were dipped in HNO_3 + HF (HydroFluoric acid) in order to remove the deposited Si on SiC. The sample not subject to H_2 etching in Si-rich ambient is designated "H_2-CVD-NO w/o Si".

5.5.2 Energy Distribution of Interface State Density

Fig. 5.7 depicts the energy distributions of D_{it} estimated by a high (1 MHz)–low method. D_{it} for the H_2-CVD-NO w/o Si sample is comparable to the results of the CVD-NO sample. On the other hand, 5∼8-fold reduction in D_{it} is achieved when H_2 etching was performed with Si piece or SiH_4 flowing. This result indicates that the key to obtain low D_{it} is performing H_2 etching in a Si-rich ambient.

Next, the author investigated whether D_{it} was effectively reduced when H_2/SiH_4 annealing was performed at relatively low temperature (750°C). Both samples annealed at 750°C and 1350°C in H_2/SiH_4 were dipped in HNO_3 + HF. After that, SiO_2 was deposited by PECVD and NO annealing was performed.

Fig. 5.8 depicts the energy distributions of D_{it} estimated by a high (1 MHz)–low method. The D_{it} for the sample annealed at 750°C is almost comparable to the results of CVD-NO. On the other hand, D_{it} is substantially reduced when H_2 annealing was performed at 1350°C.

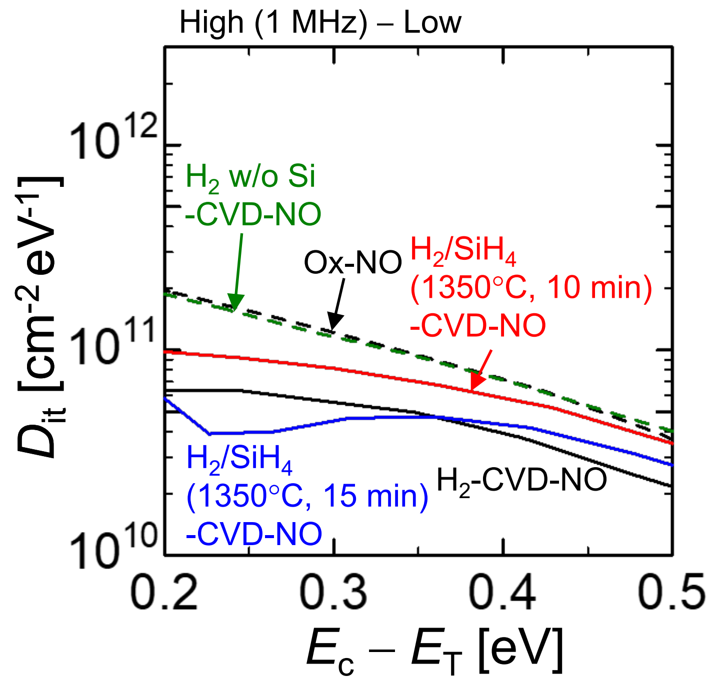


Figure 5.7: Energy distribution of D_{it} extracted by a high (1MHz)-low method. A substantial reduction in D_{it} is achieved when H_2 etching is performed in Si-rich ambient before SiO_2 deposition.

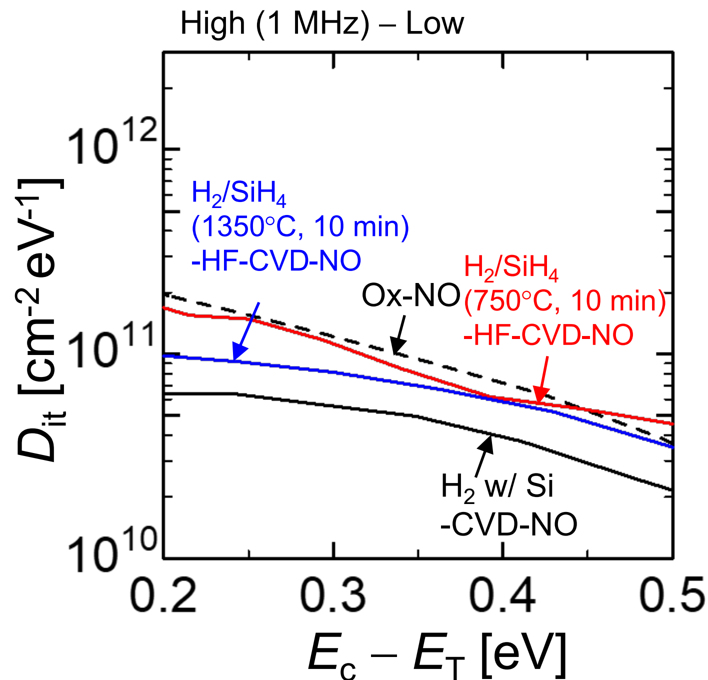


Figure 5.8: Energy distribution of D_{it} extracted by a high (1MHz)-low method. D_{it} is effectively reduced when H_2 annealing temperature is 1350°C. On the other hand, D_{it} of the sample annealed at 750°C is almost comparable to that for the Ox-NO sample.

From these result, there are two important points to obtain the high-quality interfaces. 1. H_2 etching must be performed in Si-rich ambient. 2. H_2 etching needs to be performed at high temperature as high as 1350°C.

5.6 X-Ray Photoelectron Spectroscopy (XPS) Analysis of SiC Surface after H_2 etching

It was experimentally demonstrated that H_2 etching in Si-rich ambient have a vital role in reducing D_{it}. However, the passivation mechanism and the effect of H_2 etching on SiC surface remain unclear. Chemical analysis should be performed so as to clarify the microscopic mechanism defect passivation by H_2 etching. In this study, the author investigates the composition and bonding state of SiC surface by X-Ray Photoelectron Spectroscopy (XPS) Analysis.

5.6.1 XPS Analysis of SiC Surface

Fig. 5.9 shows the XPS intensity of Si 2p spectra acquired from near-surface SiC regions with and without performing H_2 etching with Si piece. The take-off angle of photoelectron (θ_{e}) is 15°. In addition to the intense peak at a binding energy of 101 eV, which originates from Si-C bonds in SiC, an additional signal component in higher energies (102 – 103 eV) is observed for the sample with H_2 etching in Si-rich ambient. Such a component presumably is due to the Si-O bonds, suggesting the creation of oxide/suboxide at the topmost surface. The result for the sample with H_2 etching in Si-rich ambient after removing the oxide suboxide by HF is also indicated in Fig. 5.10. Compared with the as-grown sample, the peak intensity increases in the sample when H_2 etching in Si-rich ambient is performed, suggesting that suboxide components are removed.

Fig. 5.11 depicts the XPS intensity of Si 2p spectra obtained from near-surface SiC regions with and without performing H_2 etching after the formation of gate oxide. Gate oxides were formed by SiO_2 deposition + NO annealing, followed by removal of SiO_2 by HF. Compared with the sample without H_2 etching, the peak intensity is higher in the sample with H_2 etching even after NO annealing was performed. Note that there was no dominant difference in the peak intensities for N atoms.

5.6.2 Correspondence of XPS Results and Energy Distribution of Interface State Density

From the XPS results, suboxide component is formed by H_2 etching in Si-rich ambient. To clarify that the insertion layer of SiO_x formed by H_2 etching plays crucial role for reduction of D_{it}, the author evaluates the energy distribution of D_{it} when suboxide component formed

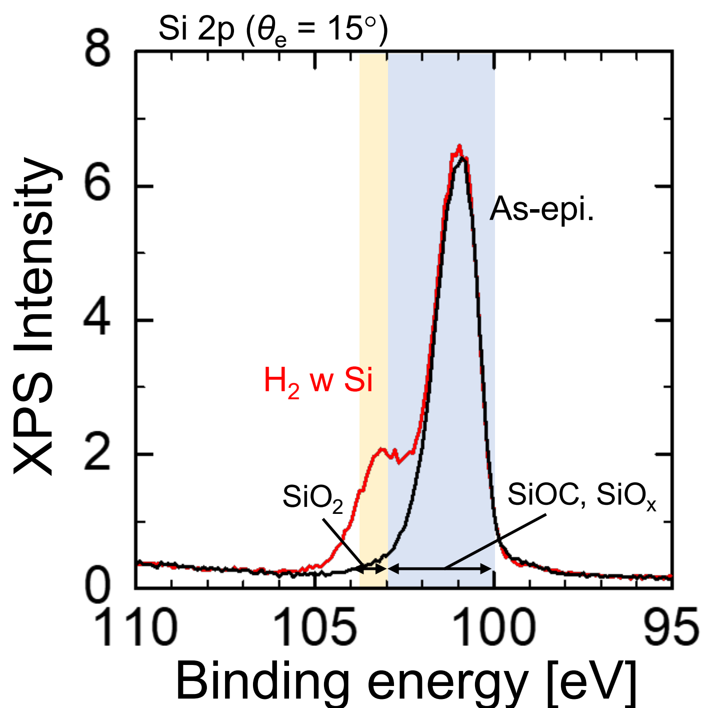


Figure 5.9: XPS intensity of Si 2p spectra obtained from SiC surface with and without H_2 etching in Si-rich ambient. The take-off angle of photo electron is 15°.

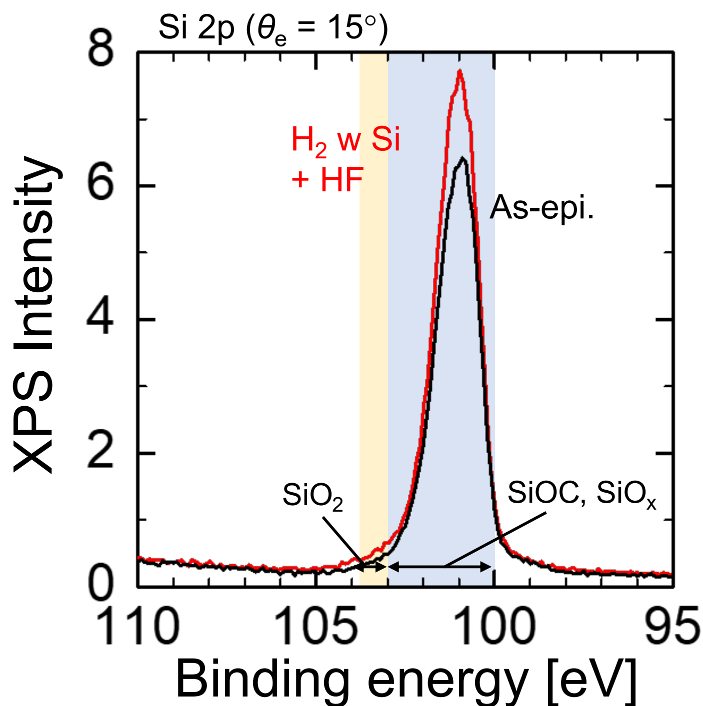


Figure 5.10: XPS intensity of Si 2p spectra obtained from SiC surface for the As-epi. sample and the sample with H_2 etching in Si-rich ambient + HF.

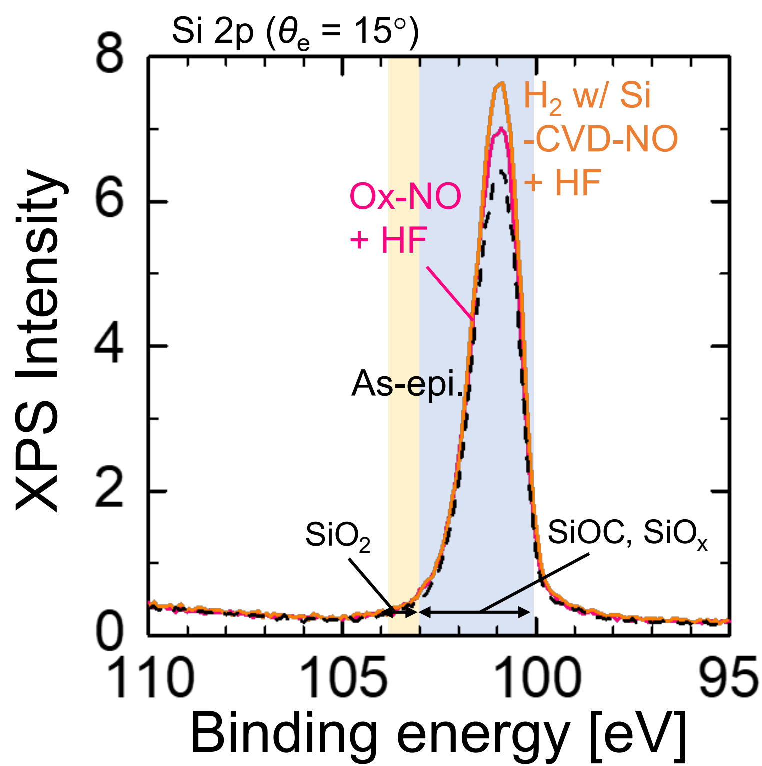


Figure 5.11: XPS intensity of Si 2p spectra taken from the SiC surface after gate oxide was removed by HF. Gate oxide is formed by SiO_2 deposition and NO annealing.

by H_2 etching is removed by HF (Fig. 5.12). D_{it} is effectively reduced when the suboxide components are removed by HF after H_2 etching. From this result, suboxide formation on SiC surface by H_2 etching in Si-rich ambient is not the major key for reducing D_{it}.

The mechanism of reduction in D_{it} is unclear at present, there are two possible speculation from XPS results. 1. SiC surface is clearly terminated by Si atoms. 2. Si-rich layer is formed in the SiC surface. In both cases, the chemical bonding states of Si and O and the passivation mechanism by incorporation of N atoms could be different, compared with the SiC/SiO_2 structure formed by only deposition or thermal oxidation.

5.7 Reduction in Interface States by H_2 Etching prior to Formation of Gate Oxide on $(11\bar{2}0)$, $(1\bar{1}00)$

5.7.1 Experimental Details

MOS capacitors were formed on n-type 4H-SiC $(11\bar{2}0)$ epilayers (donor density: 3×10^{15} cm^{-3}) and $(1\bar{1}00)$ (donor density: 3×10^{16} cm^{-3}) epilayers. Gate oxides were formed by same manners described in Section 5.2.1. For comparison, MOS capacitors with SiO_2 (thickness: 30-58 nm) formed by dry oxidation and NO annealing were prepared. Note that H_2 means "H_2 etching with Si piece" in the following sentences.

5.7.2 Capacitance-Voltage Characteristics

Fig. 5.13 (a) depicts the quasi-static and 1-MHz capacitance–voltage (C–V) characteristics of the MOS capacitors at 300 K. Frequency dispersion is well suppressed as in the case of (0001) MOS capacitors. However, large negative flat-band voltage shift is observed in the case of $(11\bar{2}0)$ and $(1\bar{1}00)$ MOS capacitors. The densities of the effective fixed charge estimated from the flat-band voltage shifts are 6.7×10^{11} cm^{-2} (negative), 3.7×10^{11} cm^{-2} (positive), and 3.6×10^{12} cm^{-2} (positive) for the As-Ox. sample, the $(11\bar{2}0)$ H_2-CVD-NO sample, and the $(1\bar{1}00)$ H_2-CVD-NO sample, respectively.

5.7.3 Energy Distribution of Interface State Density

Fig. 5.13 (b) illustrates the energy distributions of D_{it} near E_c extracted by the High(1 MHz)-Low method for the prepared $(11\bar{2}0)$ and $(1\bar{1}00)$ MOS capacitors. Compared with the D_{it} of Ox-NO samples, a marked decrease in D_{it} is achieved by H_2-CVD-NO process for the both faces. D_{it} values (energy range from E_c − 0.2 eV to E_c − 0.5 eV) are as low as $2-4\times10^{10}$ cm^{-2}eV^{-1} for the samples on $(11\bar{2}0)$ and $(1\bar{1}00)$ faces. Note that the D_{it} value of the sample on $(1\bar{1}00)$ face is slightly lower than that on $(11\bar{2}0)$ face. However, the obtained D_{it} value is close to the detection limit of the High-Low method (1×10^{10} cm^{-2}eV^{-1}). Thus,

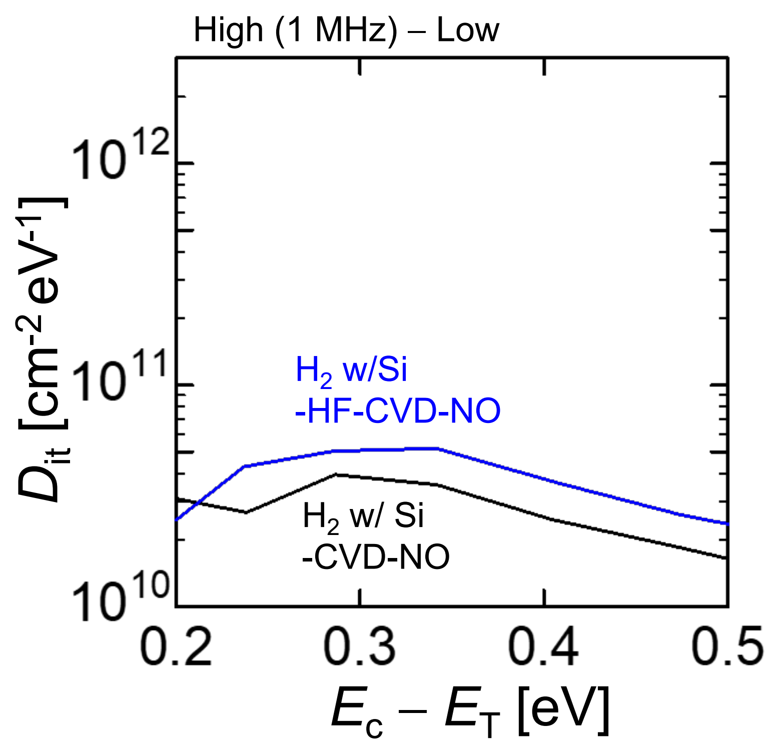
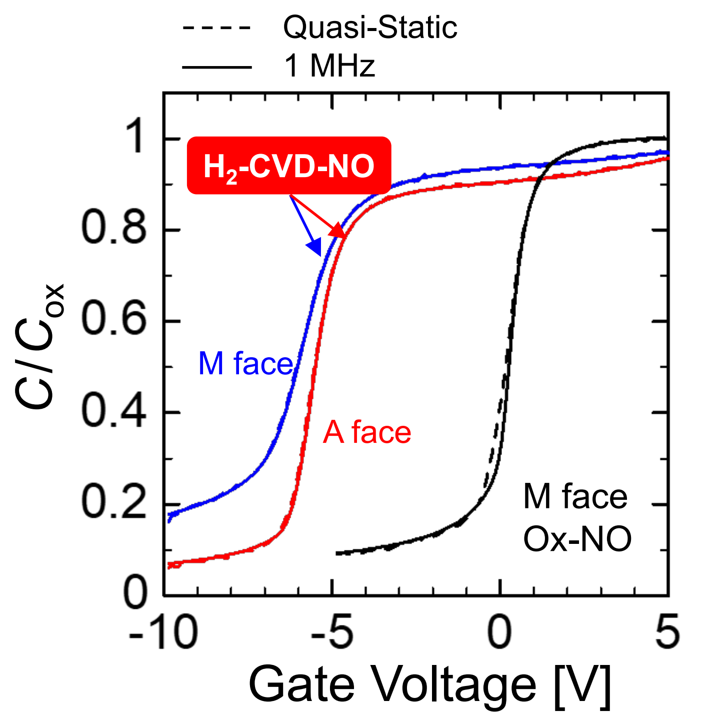
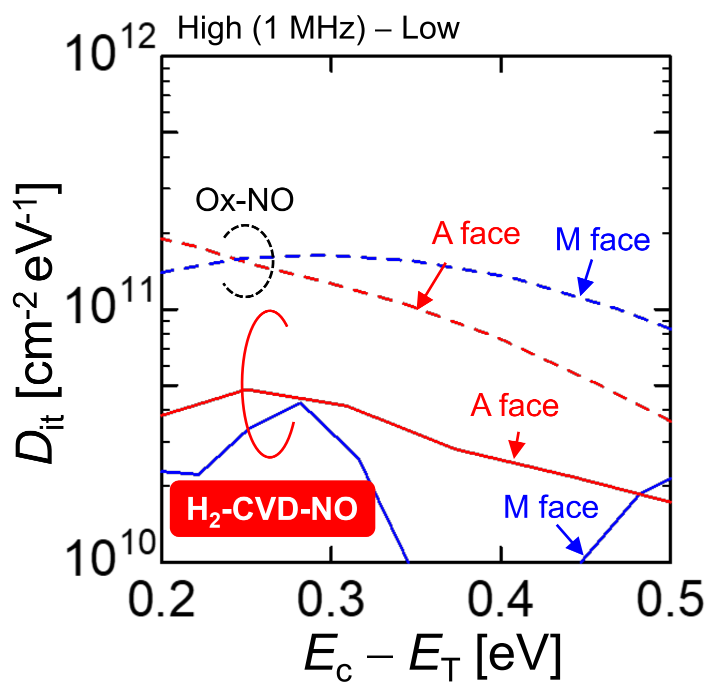


Figure 5.12: Energy distribution of $D_{\rm it}$ extracted by a high (1MHz)-low method. Regardless of SiO$_x$ removal, substantial low $D_{\rm it}$ is obtained.



(a)



(b)

Figure 5.13: (a) Quasi-static and 1 MHz C–V characteristics of the prepared $(11\bar{2}0)$ and $(1\bar{1}00)$ MOS capacitors. (b) Energy distribution of D_{it} extracted by the high (1 MHz)-low method.

it is difficult to conclude D_{it} is lower in the H_2-CVD-NO sample on $(1\bar{1}00)$ than that on $(11\bar{2}0)$.

5.8 Summary

In conclusion, the author demonstrated that H_2 etching in Si-rich ambient prior to SiO_2 deposition is effective in reducing D_{it} at the formation of (0001) SiC/SiO_2 interface. The mechanism for obtaining high-quality SiC/SiO_2 structure is unclear at present, H_2 etching in Si-rich ambient plays a important role to effectively reduce the D_{it}. A significant reduction of D_{it} (4×10^{10} $cm^{-2}eV^{-1}$at E_c- 0.2 eV) was achieved for the procedure of H_2 etching of the SiC surface, SiO_2 deposition, and interface nitridation. The D_{it} reduction effect is about five times to that of nitridation process which has been widely used in SiC MOS community. It was also demonstrated that the above process that minimizes oxidation is effective for the reduction of D_{it} at $(1\bar{1}00)$ and $(11\bar{2}0)$ SiC/SiO_2 interface. Substantial low D_{it} of $2-4 \times 10^{10}$ $cm^{-2}eV^{-1}$ are obtained for the samples on $(11\bar{2}0)$ and $(1\bar{1}00)$ faces.

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Chapter 6

Mobility Improvement in 4H-SiC MOSFETs Fabricated on (0001), $(11\bar{2}0)$ and $(1\bar{1}00)$ using Oxidation-Minimized Process

6.1 Introduction

In Chapter 5 a substantial reduction in D_{it} is achieved by the following procedures: (1) H_2 etching in Si-rich ambient, (2) SiO_2 deposition, (3) interface nitridation. However, it has not been demonstrated whether these processes are effective for improvement of the channel mobilities of SiC MOSFETs. In addition, it should be also investigated the acceptor concentration dependence of the channel mobility because practical SiC MOSFETs utilize heavily doped p-body ($> 5 \times 10^{17}$ cm^{-3}).

In this chapter, the author investigates the effects of the minimized-oxidation process on the channel mobility of (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ MOSFETs. MOSFETs with various acceptor concentration of p-body are fabricated and the field-effect mobilities were evaluated. The correration between the channel mobility and the crystal face orientation is discussed.

6.2 Device Fabrication

Lateral n-channel MOSFETs were fabricated on p-type 4H-SiC (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ epilayers. For (0001), N_{A} values for the p-type epilayers were 1×10^{15} cm^{-3} $-$ 1×10^{18} cm^{-3}. For $(11\bar{2}0)$, N_{A} values for the p-type epilayers were 1×10^{17} cm^{-3} and 1×10^{18} cm^{-3}. For $(1\bar{1}00)$, N_{A} values for the p-type epilayers were 3×10^{17} cm^{-3} and 5×10^{18} cm^{-3}. The gate oxide was formed by the H_2-CVD-N_2 or the H_2-CVD-NO processes which are described in Chapter 5 (thickness: 30-35 nm). For the comparison, MOSFETs with the gate oxide formed by the Ox-NO process were also fabricated. Al electrodes were deposited onto the

source and drain regions and ohmic contact annealing was conducted for 4 min at 400°C. The channel length and width of the MOSFETs were 100 μm and 170 μm, respectively.

6.3 Mobility Improvement in 4H-SiC MOSFETs Fabricated on (0001)

6.3.1 Gate Characteristics

Fig. 6.1 shows the transfer characteristics of the fabricated MOSFETs. Compared with the Ox-N_2 and Ox-NO devices, both the H_2-CVD-N_2 and the H_2-CVD-NO MOSFETs exhibited a marked increase in drain current. Although a significant increase in drain current is achieved, the H_2-CVD-N_2 MOSFET shows the normally-on operation due to the large negative shift of the threshold voltage. On the other hand, the negative threshold voltage shift is suppressed in the H_2-CVD-NO MOSFET. Threshold voltages in the present study were acquired by linear extrapolation of the gate characteristics. The threshold voltages were 0.81 V for the Ox-N_2 device, 0.94 V for the Ox-NO device, −2.0 V for the H_2-CVD-N_2 device, and 0.92 V for the H_2-CVD-NO device.

Hystereses in the gate characteristics were measured because it is known that N atoms in SiO_2 act as traps [1]. The hystereses in the gate characteristics are indicated in Fig. 6.2. The solid lines show the results for sweeping from negative to positive voltage and the dashed lines depict those for sweeping from positive to negative voltage (−6 to 10 V). The hystereses in the bi-directional gate characteristics were 0.1 V, 0.1 V, and 0.05 V for the Ox-NO, the Ox-N_2, and the H_2-CVD-NO devices, respectively, indicating that the density of trapped carriers inside the SiO_2 is very small. On the other hand, the H_2-CVD-N_2 device showed a slightly larger hysteresis ($\sim$ 0.3 V), compared with other devices. This difference may arise from the fact that the density of N atoms in the SiO_2 for the H_2-CVD-N_2 device is higher than that in other devices.

6.3.2 Channel Mobilities

Fig. 6.3 exhibits the field effect mobility as a function of the gate voltage. The peak mobilities were 85 cm^2/Vs for the H_2-CVD-N_2 MOSFET and 80 cm^2/Vs for the H_2-CVD-NO MOSFET, which are approximately twice as high as the peak channel mobilities for the Ox-N_2 and the Ox-NO devices. The peak channel mobility of the H_2-CVD-NO device was slightly lower than that of the H_2-CVD-N_2 device. This tendency does not contradict to the result of $D_{\rm it}$ (Fig. 5.4).

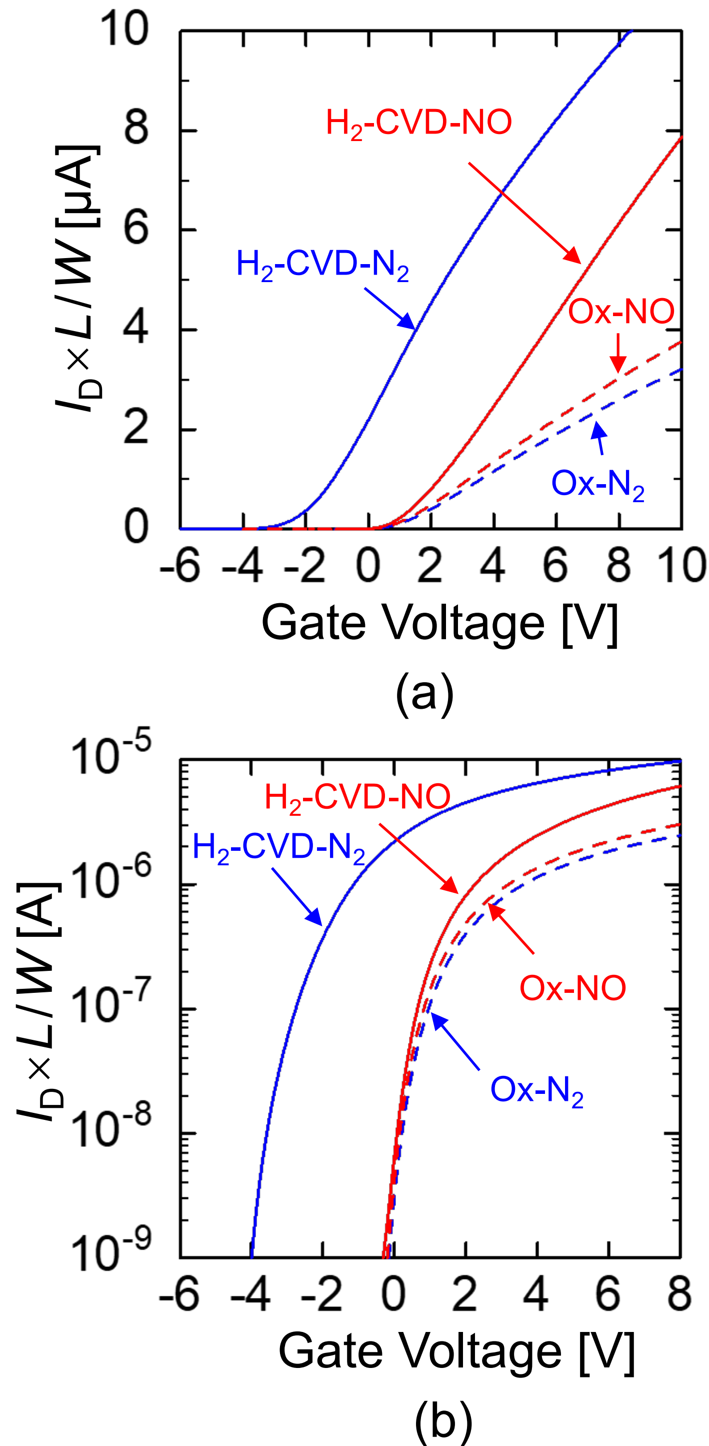


Figure 6.1: Transfer characteristics of the fabricated SiC MOSFETs with (a) a linear scale and with (b) a semi-logarithmic scale. The drain current (I_D) was normalized with respect to the channel length (L) and channel width (W). The drain current rises steeply in the subthreshold region and increases in the linear region for the H_2-CVD-N_2 and the H_2-CVD-NO MOSFETs.

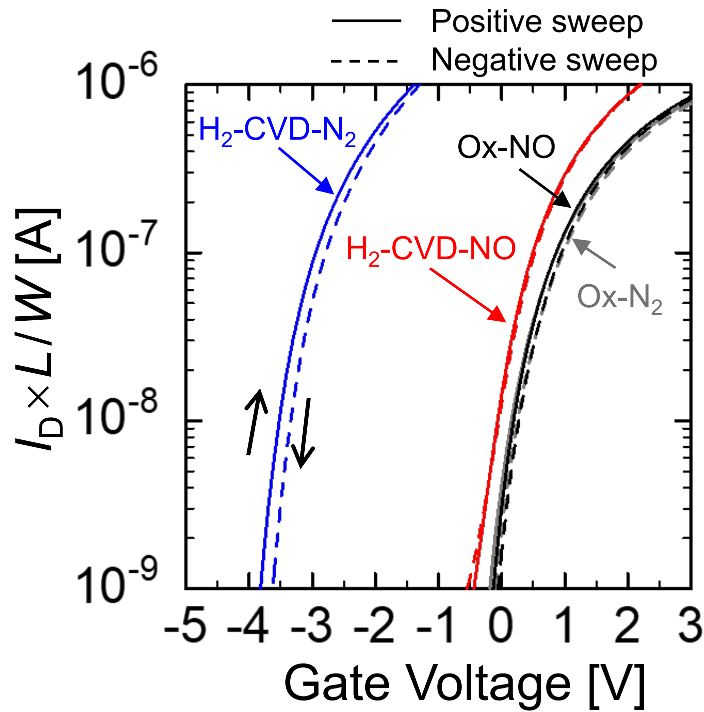


Figure 6.2: Hysteresis in gate characteristics of the fabricated SiC MOSFETs. Gate voltage was swept from −6 to 10 V.

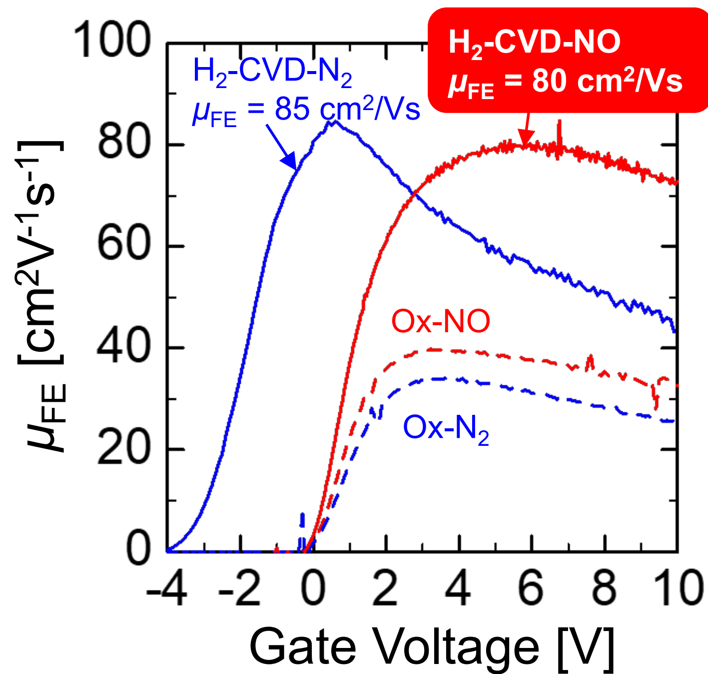


Figure 6.3: Field-effect mobilities for the fabricated SiC MOSFETs as a function of the gate voltage.

6.3.3 Acceptor Concentration Dependence of Gate Characteristics and Channel Mobilities

The typical gate characteristics and field-effect mobility for the fabricated (0001) MOSFETs with various acceptor concentrations are shown in Fig. 6.4. The gate characteristics shifts to positive direction as the doping concentration increases and drain current clearly increases compared with the results for Ox-NO MOSFETs. The peak mobilities for the H_2-CVD-NO devices are approximately twice as high as those for the Ox-NO devices for N_A values of 1 $\times$ 10^{17} cm^{-3} and 1 $\times$ 10^{18} cm^{-3}. Note that the channel mobility reaches 25 cm^2/Vs when N_A is 1 $\times$ 10^{18} cm^{-3}.

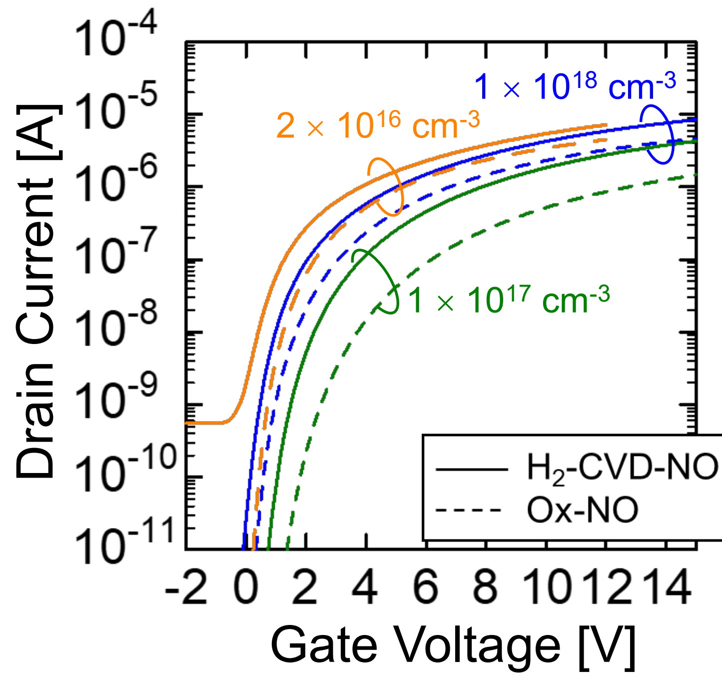
6.4 Mobility Improvement in 4H-SiC MOSFETs Fabricated on $(11\bar{2}0)$ and $(1\bar{1}00)$

6.4.1 Gate Characteristics

The typical gate characteristics of the fabricated $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs are shown in Fig. 6.5 (a) and Fig. 6.6 (a), respectively. As in the case for the H_2-CVD-NO (0001) MOSFETs, both of H_2-CVD-NO $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs. exhibit high drain current. Voltage shifts in the $I-V$ characteristics are well suppressed ($\sim$ 1 V) although MOS capacitors formed on $(11\bar{2}0)$ and $(1\bar{1}00)$ SiC with H_2-CVD-NO process show the large negative flat-band voltage shift ($>$ 5 V) as shown in Fig. 5.13.

6.4.2 Channel Mobilities

The field-effect mobilities of the fabricated $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs are depicted in Fig. 6.5 (b) and Fig. 6.6 (b), respectively. As in the case of the (0001) MOSFETs, the channel mobility was improved by the H_2-CVD-NO process. The channel mobility reached 125-130 cm^2/Vs for the $(11\bar{2}0)$ MOSFETs and 80-112 cm^2/V for the $(1\bar{1}00)$ MOSFETs. Compared with the Ox-NO process, the H_2-CVD-NO process increases the channel mobility by a factor of about 1.5 for the $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs with N_A values of 1 $\times$ 10^{17} cm^{-3} and 3 $\times$ 10^{17} cm^{-3}. The difference in channel mobility between the Ox-NO and H_2-CVD-NO MOSFETs greatly increases with increasing N_A of the p-body. The channel mobility improvement is 6-fold for $(11\bar{2}0)$ MOSFETs (N_A = 1 $\times$ 10^{18} cm^{-3}) and 100-fold for $(1\bar{1}00)$ MOSFETs (N_A = 5 $\times$ 10^{18} cm^{-3}).



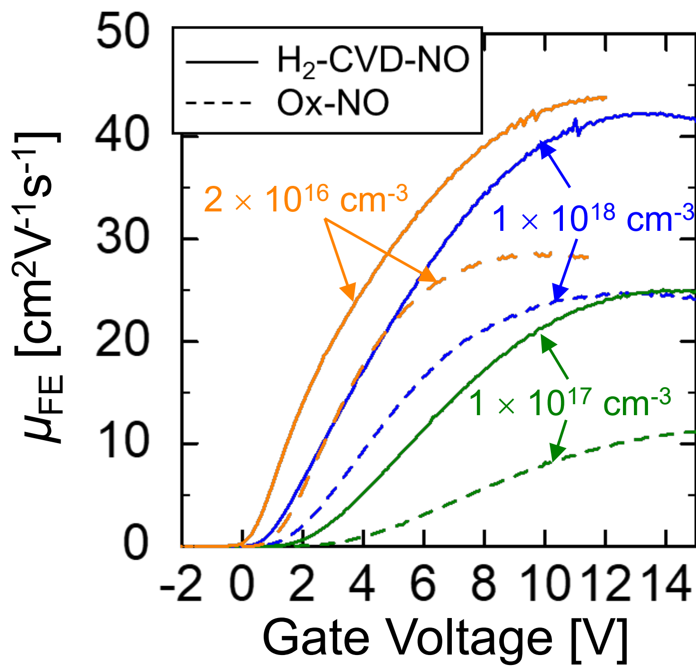


Figure 6.4: Transfer characteristics (a) and field-effect mobility (b) as function of gate voltage for fabricated SiC MOSFETs on (0001).

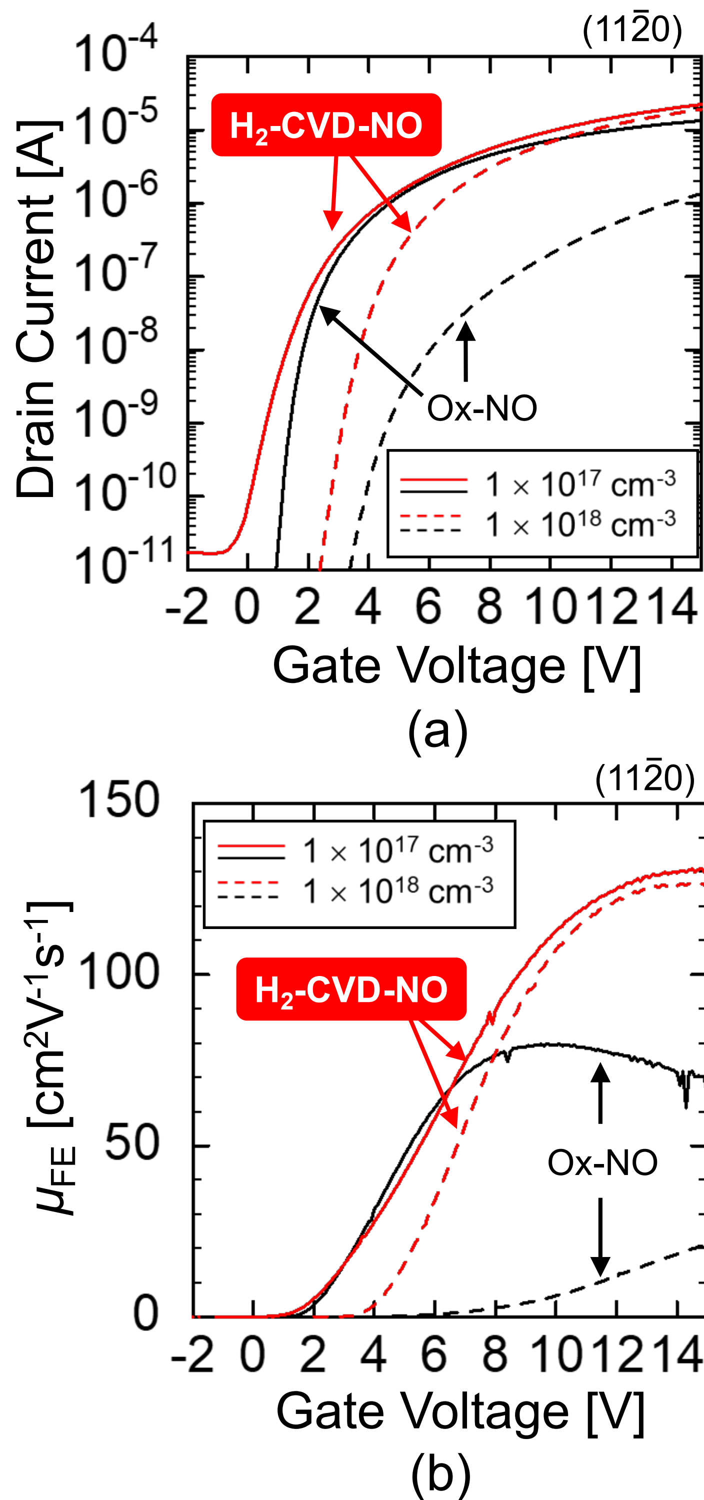


Figure 6.5: Transfer characteristics (a) and field-effect mobility (b) as function of gate voltage for MOSFETs fabricated on (11$\bar{2}$0).

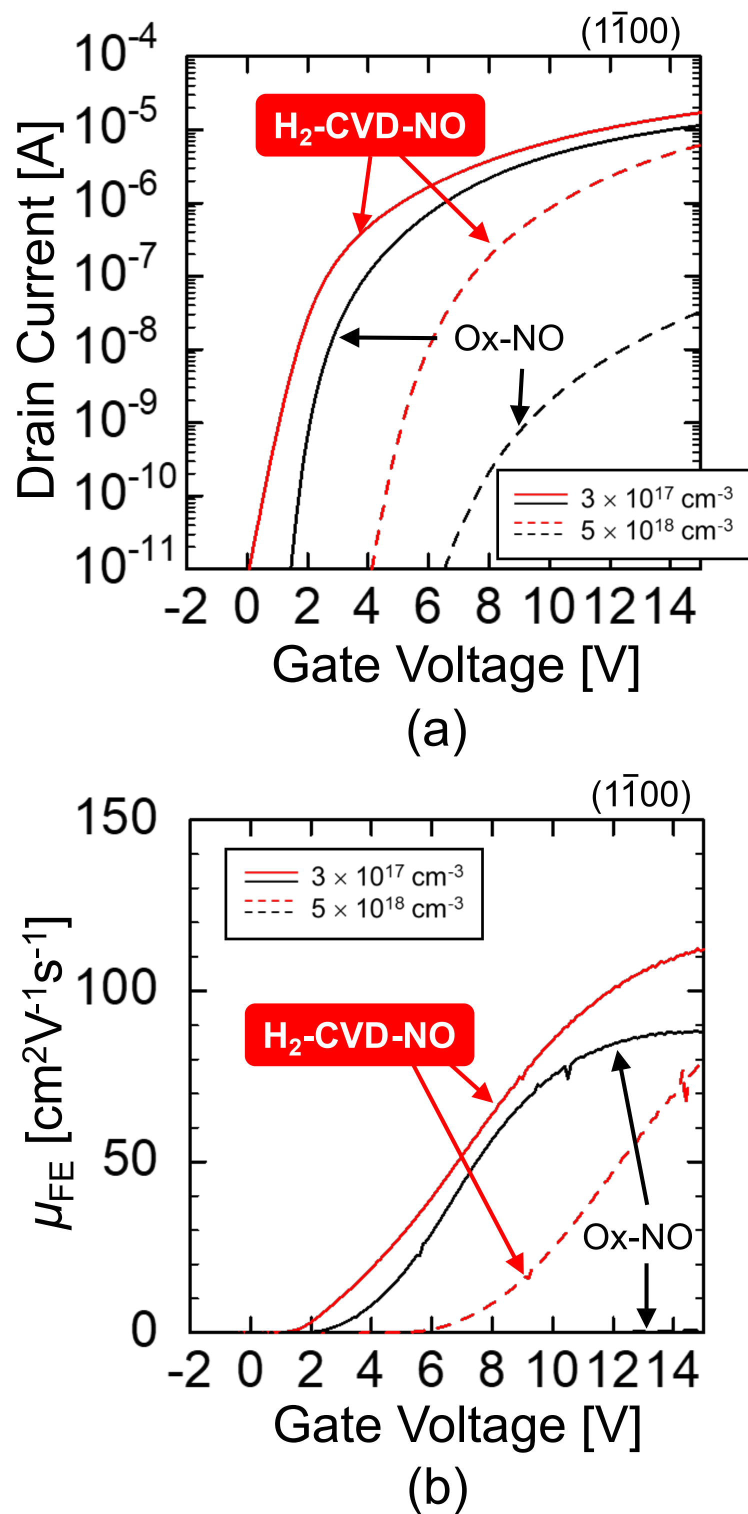


Figure 6.6: Transfer characteristics (a) and field-effect mobility (b) as function of gate voltage for MOSFETs fabricated on (1$\bar{1}$00).

6.5 Characteristics of Heavily Doped MOSFETs Fabricated on (0001) and (11$\bar{2}$0) at Low Temperature

6.5.1 Gate Characteristics

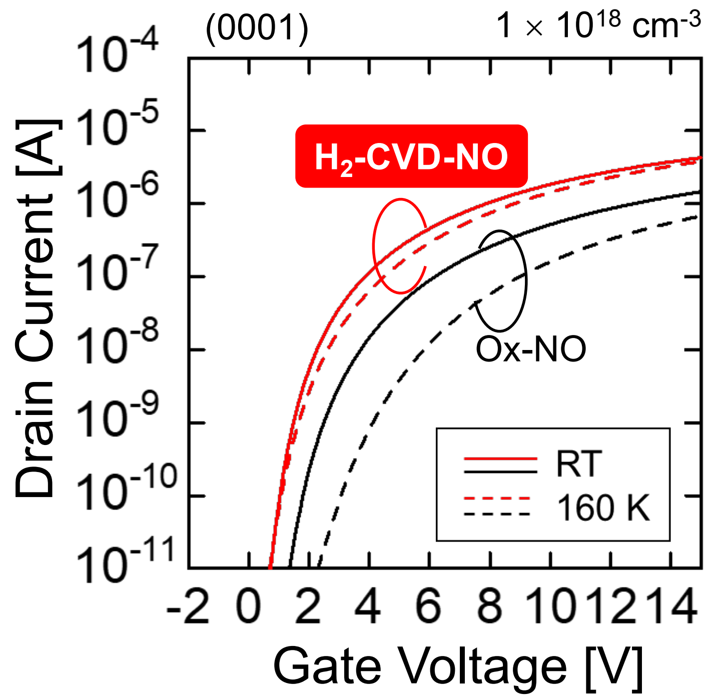
To investigate the main factor causing the mobility enhancement in the H_2-CVD-NO process, the gate characteristics of the (0001) and (11$\bar{2}$0) MOSFETs ($N_A = 1 \times 10^{18}$ cm^{-3}) were measured at 160 K (Fig. 6.7 (a), Fig. 6.8 (a)). For a quantitative discussion, the threshold voltage (V_{th}) is defined as the gate voltage at which the drain current reaches 1×10^{-7} A. It is known that the gate characteristics of the (0001) SiC MOSFETs with NO treatment show a clear increase in threshold voltage and a decrease in channel mobility as the temperature decreases due to pronounced electron trapping at the SiC/SiO_2 interface [2]. The shift of V_{th} for the Ox-NO (0001) MOSFETs between room temperature and 160 K was 2.8 V, which result is similar to the reported result [2]. In contrast, for the H_2-CVD-NO device, the shift of V_{th} was only 0.6 V. The fabricated (11$\bar{2}$0) MOSFETs show a trend similar to that for the (0001) MOSFETs. The shift of V_{th} was 0.9 V for the Ox-NO device and 0.2 V for the H_2-CVD-NO device.

6.5.2 Channel Mobilities

The peak channel mobility for the Ox-NO device decreased from 12 to 8 cm^2/Vs with lowering the temperature, whereas that for the H_2-CVD-NO device increased from 25 to 26 cm^2/Vs. Generally, the field-effect mobility increases with decreasing temperature because the influence of phonon scattering is relaxed at low temperature. However, in the case of SiC (0001) MOSFETs, the peak field-effect mobility decreases as lowering temperature due to the carrier trapping effects at SiC/SiO_2. Thus, the increase in mobility with lowering the temperature is suggestive of reduction of D_{it}. The both of the fabricated SiC (11$\bar{2}$0) MOSFETs with the Ox-NO and the H_2-CVD-NO processes shows negative temperature dependence of the field-effect mobility, meaning that D_{it} at SiC (0001)/SiO_2 structure is lower than SiC (11$\bar{2}$0)/SiO_2 structure. Furthermore, in the case of H_2-CVD-NO (11$\bar{2}$0) MOSFETs, the channel mobility is much improved from 125 to 145 cm^2/Vs as the temperature decreases. These results indicate that D_{it} near E_c is substantially reduced in the H_2-CVD-NO MOSFETs.

6.6 Discussion

The superior mobility in SiC (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs compared with that in SiC (0001) MOSFETs fabricated with the conventional process (Ox-NO) is well known and



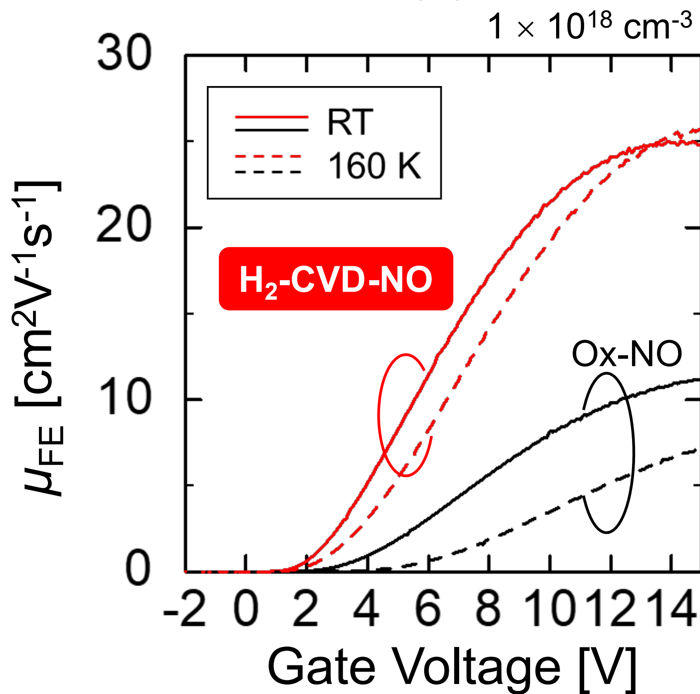
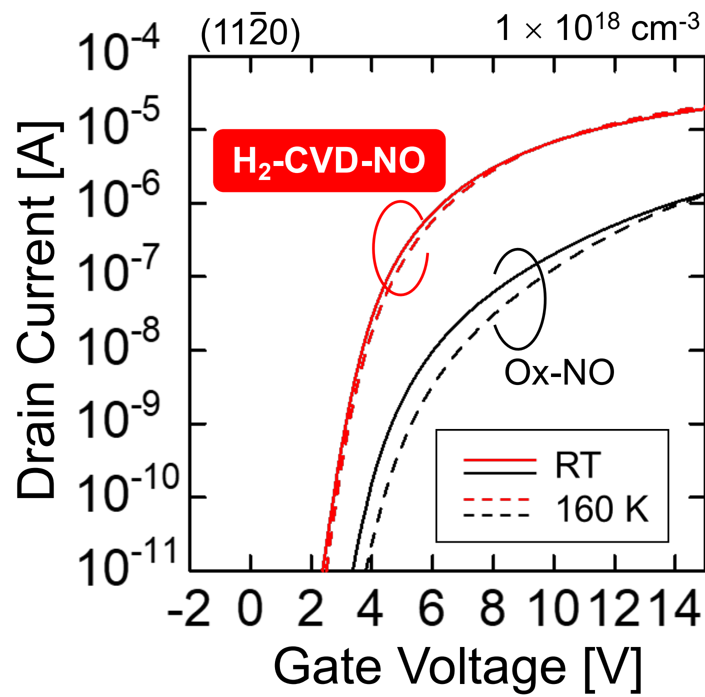
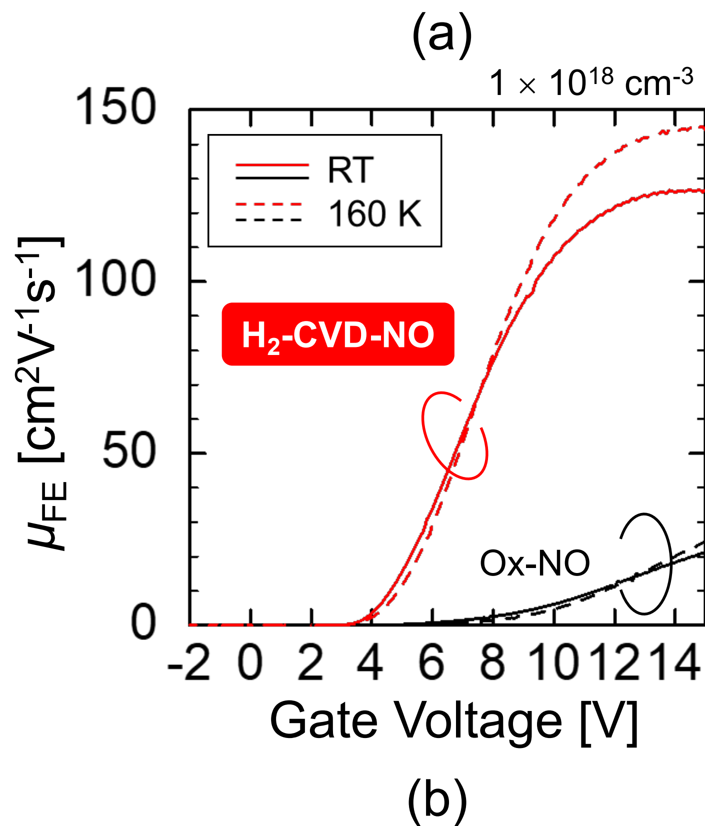


Figure 6.7: Subthreshold characteristics of fabricated (a) (0001) and (b) $(11\bar{2}0)$ MOSFETs ($N_\mathrm{a} = 1 \times 10^{18}$ cm^{-3}) at 300 and 160 K.



(a)



(b)

Figure 6.8: Subthreshold characteristics of fabricated (a) (0001) and (b) (11$\bar{2}$0) MOSFETs (N_a = 1 × 10^{18} cm^{-3}) at 300 and 160 K.

has been ascribed to the lower D_{it} near the conduction band edge [3]. A similar logic will be valid in the case of the proposed process (H_2-CVD-NO), as indicated in Fig. 5.4, Fig. 5.13, Fig. 6.7 (b), and Fig. 6.8 (b). The D_{it} values near the conduction band edge on SiC ($11\bar{2}0$) and ($1\bar{1}00$) with the proposed process are very low, being in the low 10^{10} $cm^{-2}eV^{-1}$ range (Fig. 5.4 and Fig. 5.13) and the shift in the subthreshold characteristics by cooling the MOSFET is extremely small compared with SiC (0001) MOSFETs (Fig. 5.4). It is, however, difficult to explain the surprisingly large difference in the channel mobility between "H_2-CVD-NO" MOSFETs and "Ox-NO" MOSFETs fabricated on heavily-doped ($11\bar{2}0$) and ($1\bar{1}00$) simply by the observed D_{it} difference in the energy range from $E_c - 0.2$ eV to $E_c - 0.5$ eV (Fig. 5.4 and Fig. 5.13). The D_{it} difference may be more striking in the energy range closer to E_c (The D_{it} for MOS structures formed by the conventional process may be much higher). As another potential reason, the roughness scattering in ($11\bar{2}0$) and ($1\bar{1}00$) MOSFETs fabricated with the proposed process may be reduced, since the surface of SiC ($11\bar{2}0$) and ($1\bar{1}00$) epilayers is very flat in an atomistic scale [4]. With the proposed process, this very flat surface can be easily maintained, leading to high channel mobility in heavily-doped ($11\bar{2}0$) and ($1\bar{1}00$) MOSFETs. However, this discussion is still speculative and further investigations on the channel mobility by conducting MOS-Hall effect measurements are required.

6.7 Summary

The author has investigated effects of oxidation-minimized process improves the channel mobility of (0001), ($11\bar{2}0$), and ($1\bar{1}00$) MOSFETs with high N_A of p-body ($> 1 \times 10^{17}$ cm^{-3}). For the (0001) MOSFETs ($N_a = 1 \times 10^{18}$ cm^{-3}), channel mobility reaches 25 cm^2/Vs, which is about 2 times higher than that for Ox-NO MOSFETs. For the ($11\bar{2}0$) MOSFETs ($N_a = 1 \times 10^{18}$ cm^{-3}) and ($1\bar{1}00$) MOSFETs ($N_a = 5 \times 10^{18}$ cm^{-3}), channel mobility reaches 125 and 80 cm^2/Vs, which are about 6 and 100 times higher than that for the Ox-NO MOSFETs.

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Chapter 7

Conclusions

7.1 Conclusions

In this thesis, the author conducted a systematic study on Short channel effects in SiC MOSFETs and proposed a technique for reducing interface defects and improving channel mobility as a step toward the realization of high-performance SiC power MOSFETs. The main conclusions obtained in this study are summarized as follows.

In Chapter 2, the author fabricated SiC MOSFETs with various channel lengths and acceptor concentrations of the p-body and analyzed their electrical characteristics.

First, the influence of high-density interface states at the SiC/SiO_2 interface on the threshold voltage roll-off characteristics was quantitatively investigated. The author established a model that can accurately predict the threshold voltage drop due to the electron emission from the interface states at the drain end by taking into account the energy distribution of the interface states. The calculated threshold voltage showed a good agreement with the experimental results regardless of the criterion used for the threshold voltage. The proposed model enables the estimation of the threshold voltage in 4H-SiC short-channel MOSFETs.

Second, the author determined the critical channel lengths for various acceptor concentrations to provide MOSFET design guidelines. A method for determining the critical channel length was proposed by focusing on the saturation characteristics of the drain current. The critical channel lengths determined using the proposed method were slightly longer than that for Si MOSFETs. This can be explained by the larger depletion layer width in SiC compared to that in Si due to the large built-in potential and the existence of a high density of interface states. These results can be used as guidelines for the design of power devices and SiC CMOS devices.

In Chapter 3, the author investigated the effect of high-temperature N_2 annealing after the thermal oxidation of SiC on the interface states near the conduction and the valence band edges. D_{it} was effectively reduced near the conduction band edge; it was as low as 6×10^{11} $\mathrm{cm^{-2}eV^{-1}}$ at $E_{\mathrm{c}} - 0.2$ eV, which is higher than that after NO annealing (conventional

process) by a factor of about 2-3. A low interface state density of 1×10^{11} cm^{-2}eV^{-1} in the energy range of E_v + 0.2 to E_v + 0.5 eV was obtained; this value is 50% lower than that after NO annealing.

The reliability of an N_2-annealed gate oxide was investigated. Compared with an NO-annealed gate oxide, the N_2-annealed gate oxide showed superior positive and negative bias-stress instabilities. In particular, the N_2-annealed sample exhibited an about 3 times smaller flat-band voltage shift at 423 K for a high negative voltage (> 3 MV) for 1000 s. Sufficiently high breakdown electric fields of the oxide of 10 MV/cm was obtained for the gate oxide treated with high-temperature N_2 annealing.

In Chapter 4, the author fabricated SiC MOSFETs with an N_2-annealed gate oxide to evaluate the mobility improvement effect by N_2 annealing. The peak value of the field-effect mobility of the N_2-annealed n-channel MOSFETs was 34 cm^2/Vs, which is slightly lower than that of NO-annealed MOSFETs (40 cm^2/Vs). A high channel mobility of 17 cm^2/Vs was obtained; this value is 30% higher than that for the NO-annealed MOSFETs (13 cm^2/Vs). The interface state density estimated from the subthreshold slopes for the MOSFETs is much higher than that extracted using the high–low method but comparable to that estimated using the C–ψ_s method for interface states near the conduction and valence band edges. These results suggest that there exist fast states (> 1 MHz) near the valence band edge and that these fast states affect the channel mobilities of p-channel SiC MOSFETs, as is the case for n-channel MOSFETs.

The performance of CMOS is principally limited by a low channel mobility of either the n-channel or (usually) p-channel MOSFET. These results indicate that N_2 annealing is a promising technique for improving the performance of SiC low-loss power MOSFETs and SiC-based CMOS integrated circuits.

In Chapter 5, the author proposed a technique for significantly reducing the SiC/SiO_2 interface states on SiC (0001), $(1\bar{1}00)$, and $(11\bar{2}0)$ by H_2 etching in Si-rich ambient prior to SiO_2 deposition and interface nitridation. For the (0001) face, the proposed process resulted in an about five times lower D_{it} ($4-6 \times 10^{10}$ cm^{-2}eV^{-1}) than that for thermally grown SiO_2 treated with NO annealing. The D_{it} value was further reduced to $2 - 4 \times 10^{10}$ cm^{-2}eV^{-1} for the $(1\bar{1}00)$ and $(11\bar{2}0)$ faces. A substantial reduction in D_{it} could not be achieved when sacrificial oxidation was performed after H_2 etching. It was also experimentally demonstrated that D_{it} was not significantly reduced when H_2 etching was not performed in Si-rich ambient. These results confirm that H_2 etching itself does not significantly reduce D_{it} and that the thermal oxidation of SiC increases D_{it}. A dramatic reduction in interface states can be obtained by 1) hydrogen etching in Si-rich ambient, 2) SiO_2 formation without the oxidization of SiC, and 3) interface nitridation.

In Chapter 6, n-channel MOSFETs on SiC (0001), $(1\bar{1}00)$, and $(11\bar{2}0)$ were fabricated using the proposed method. Compared with the conventional technique (dry oxidation + NO annealing), the channel mobility was drastically improved when the oxide film was formed using the proposed process. For the (0001) MOSFET, the channel mobilities reached about

80 cm^2/Vs ($N_A = 1 \times 10^{15}$ cm^{-3}) and 25 cm^2/Vs ($N_A = 1 \times 10^{18}$ cm^{-3}), which are about twice as high as those obtained with thermal oxidation and NO annealing. Surprisingly, about six to one hundred times higher channel mobilities were obtained for the $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs compared with those obtained with dry oxidation and NO annealing. The channel mobilities reached 125 cm^2/Vs for the $(11\bar{2}0)$ MOSFET ($N_A = 1 \times 10^{18}$ cm^{-3}) and 80 cm^2/Vs for the $(1\bar{1}00)$ MOSFET ($N_A = 5 \times 10^{18}$ cm^{-3}). If the proposed method is used for industrial applications, the total conduction loss for DMOSFETs and trench MOSFETs is expected to decrease by 20%.

7.2 Future Prospects

The author studied SiC MOSFETs from various aspects in this thesis. However, several issues, which will be considered in future studies, remain to be solved.

- **Elucidation of mechanism of channel mobility improvement due to oxidation-minimized process H_2 etching in Si-rich ambient:** The author significantly improved the channel mobility of SiC MOSFETs using an oxidation-minimized process (H_2-CVD-NO). However, the mechanism of the mobility enhancement was not quantitatively discussed. To clarify whether the mobility enhancement is due to an improvement in the true electron mobility or a reduction in the interface states, it is necessary to conduct MOS Hall effect measurements. In particular, extremely high channel mobilities for heavily doped SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs could not be explained by only a reduction in interface defects. Systematic studies on the channel mobilities using MOS Hall effect measurements are required. To understand the mobility-limiting factor of SiC MOSFETs, the electron scattering in the inversion channel should also be analyzed.

- **Investigation on effect of H_2 etching in Si-rich ambient on SiC surface:** It was experimentally demonstrated that the thermal oxidation of SiC induces a high density of interface states and that these states are effectively reduced by H_2 etching in Si-rich ambient. However, the physical nature of the interface defects and the passivation mechanism of H_2 etching in Si-rich ambient remain unclear. Although various chemical analyses (e.g., XPS, SIMS) were conducted on the SiC surface and the SiC/SiO_2 interface to identify the microscopic nature of the interface defects [1–8], it was only revealed that excess carbon atoms exist at the SiC/SiO_2 interface. These analyses should be performed on the SiC surface and the SiC/SiO_2 interface after H_2 treatment to clarify the effect of H_2 treatment and identify the atomistic form of the interface defects. Detailed analyses of the SiC/SiO_2 interface formed by the oxidation-minimized process will contribute to further improvements in channel mobility.

- **Proof of mobility enhancement on p-channel SiC MOSFETs by oxidation-minimized process:** In this study, the author showed that the oxidation-minimized process is effective in improving the mobility of n-channel MOSFETs. As a next step, it is necessary to investigate whether the oxidation-minimized process can improve the channel mobility of p-channel MOSFETs. Further mobility improvement in p-channel SiC MOSFETs will accelerate the realization of SiC CMOS. Therefore, it is necessary to investigate the channel mobility of p-channel SiC MOSFETs with the gate oxide formed using the oxidation-minimized process.

- **Characterization of threshold voltage instability in SiC/SiO_2 at elevated temperature:** Although the proposed technique enables the creation of high-quality SiC/SiO_2 interfaces, it is necessary to ensure the high reliability of the oxide film for practical applications. The hysteresis of the gate characteristics and the breakdown voltage of the gate insulator at room temperature were investigated. The reliability was found to be almost similar to or better than that of the oxide film formed using the conventional method. However, there are concerns about the degradation of the threshold voltage instability in a high-temperature environment and the long-term dielectric breakdown strength. Thus, the positive and negative bias temperature instabilities and the time-dependent dielectric breakdown at elevated temperature must be carefully investigated.

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List of Publications

A. Full Length Papers and Letters

1. K. Tachiki, T. Ono, T. Kobayashi, H. Tanaka, and T. Kimoto,
"Estimation of threshold voltage in SiC short channel MOSFETs,"
IEEE Transaction on Electron Devices **65**, 3077 (2018).

2. T. Kobayashi, K. Tachiki, K. Ito, and T. Kimoto,
"Reduction of interface state density in SiC (0001) MOS structures by low-oxygen-partial-pressure annealing,"
Applied Physics Express **12**, 031001 (2019).

3. T. Kobayashi, T. Okuda, K. Tachiki, K. Ito, Y. Matsushita, and T. Kimoto,
"Design and formation of SiC (0001)/SiO_2 interfaces via Si deposition followed by low-temperature oxidation and high-temperature nitridation,"
Applied Physics Express **13**, 091003 (2020).

4. K. Tachiki, M. Kaneko, T. Kobayashi, and T. Kimoto,
"Formation of high-quality SiC(0001)/SiO_2 structures by excluding oxidation process with H_2 etching before SiO_2 deposition and high-temperature N_2 annealing,"
Applied Physics Express **13**, 121002 (2020).

5. K. Tachiki and T. Kimoto,
"Improvement of both n- and p-channel mobilities in 4H-SiC MOSFETs by high-temperature N_2 annealing,"
IEEE Transaction on Electron Devices **68**, 638 (2021).

6. K. Tachiki, M. Kaneko, and T. Kimoto,
"Mobility improvement of 4H-SiC (0001) MOSFETs by a three-step process of H_2 etching, SiO_2 deposition, and interface nitridation,"
Applied Physics Express **14**, 131001 (2021).

7. K. Tachiki, T. Ono, T. Kobayashi, and T. Kimoto,
   "Short-channel effects in SiC MOSFETs based on analyses of saturation drain current,"
   IEEE Transaction on Electron Devices **68**, 1382 (2021).

8. K. Tachiki, K. Mikami, K. Ito, M. Kaneko, and T. Kimoto,
   "Mobility enhancement in heavily doped 4H-SiC (0001), $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs via an oxidation-minimized process,"
   in preparation

B. International Conferences

1. K. Tachiki, T. Ono, T. Kobayashi, and T. Kimoto,
   "Experimental study on short channel effects in 4H-SiC MOSFETs,"
   International Conference on Silicon Carbide and Related Materials 2017, Washington, USA, September (2017), TU.DP.16, Poster, Late News.

2. T. Kobayashi, K. Tachiki, K. Ito, Y. Matsushita, and T. Kimoto,
   "Reduction of interface state density in SiC (0001) MOS structures by very-low-oxygen-partial-pressure annealing,"
   European Conference on Silicon Carbide and Related Materials 2018, Birmingham, UK, September (2018), TU.01a.05, Oral.

3. K. Tachiki, T. Ono, T. Kobayashi, and T. Kimoto,
   "Estimation of threshold voltage in SiC short-channel MOSFETs,"
   European Conference on Silicon Carbide and Related Materials 2018, Birmingham, UK, September (2018), TU.04a.04, Oral.

4. K. Tachiki, T. Ono, T. Kobayashi, and T. Kimoto,
   "Degradation in threshold voltage roll-off characteristics of SiC MOSFETs induced by interface states,"
   International Symposium on Photonics and Electronics Science and Engineering 2019, Kyoto, Japan, March (2019), P-16, Poster.

5. T. Kimoto, T. Kobayashi, K. Tachiki, and K. Ito,
   "Promise and future challenges of SiC power MOSFETs (invited),"
   21st International Conference on Insulating Films on Semiconductors, Cambridge, UK, July (2019), 4.1, Oral.

6. K. Tachiki and T. Kimoto,
"Reduction of interface states in 4H-SiC/SiO_2 near both conduction and valence band edges by high-temperature nitrogen annealing,"
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The 9th Asia-Pacific Workshop on Widegap Semiconductors, Okinawa, Japan, November (2019), ThP-HC-13, Poster.

8. K. Tachiki and T. Kimoto,
"Investigation of gate oxide reliabilities in N_2 annealed SiC/SiO_2 structure,"
International Symposium on Creation of Advanced Photonic and Electronic Devices 2020, Kyoto, Japan, March (2020), P-33, Poster.

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International Symposium on Creation of Advanced Photonic and Electronic Devices 2020, Kyoto, Japan, March (2021), A16, Poster.

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11. K. Tachiki and T. Kimoto,
"Reduction of C-related defects near the SiO_2/SiC interface,"
Mini-Conference on Materials, Processing and Fabrication of Advanced Wide Bandgap Power Devices, Columbus, USA/Online, May (2021), 2-1, Oral.

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"Reduction of interface state density in the SiC MOS structures by non-oxidation process (invited)," *2021 International Conference on Solid State Devices and Materials*, Online September (2021), D-4-01, Oral.

13. K. Mikami, K. Ito, K. Tachiki, and T. Kimoto,
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European Conference on Silicon Carbide and Related Materials 2020$\cdots$2021, Tours, France/Online, October (2021), TU-1B-01, Oral.

14. K. Tachiki, K. Ito, M. Kaneko, and T. Kimoto,
"Mobility improvement in 4H-SiC MOSFETs by H_2 etching before SiO_2 deposition and interface nitridation (invited),"
European Conference on Silicon Carbide and Related Materials 2020· · · 2021, Tours, France/Online, October (2021), TU-1B-Inv, Oral.

15. T. Kimoto, M. Kaneko, T. Kobayashi, H. Tanaka, K. Tachiki, A. Iijima, S. Yamashita, X. Chi, Y. Zhao, D. Stefanakis, and Y. Matsushita,
"A New horizon of SiC technology driven by deeper understanding of physics (plenary),"
European Conference on Silicon Carbide and Related Materials 2020·2021, Tours, France/Online, October (2021), Th-PS-01, Oral.

16. T. Kimoto, M. Kaneko, K. Tachiki, K. Ito, R. Ishikawa, X. Chi, D. Stefanakis, T. Kobayashi, and H. Tanaka,
"Physics and Innovative Technologies in SiC Power Devices (invited),"
67th IEEE International Electron Devices Meeting, San Francisco, USA/Online, December (2021), 36-1, Oral.