# A Study on Plasma Process-Induced Defect Creation in Si-Based Devices

**Yoshihiro Sato**

**2023**

# Preface

This study was conducted from 2017 to 2022 at the Department of Aeronautics and Astronautics, Kyoto University, Japan. I started developing complementary metal–oxide–semiconductor (CMOS) image sensors at Panasonic Corporation in 2012. I have been working on the development of low-leakage current CMOS image sensors (CISs) by optimizing the device structure and impurity profile formed by ion implantation. The plasma process is indispensable in the manufacture of semiconductor devices, such as CISs. A proper understanding of the effects of plasma-induced physical damage (PPD)—defect creation in a material by the bombardment of incident ions from plasma—during the semiconductor manufacturing process to further decrease leakage current in electronic devices is crucial. The main objective of this study is to clarify the effect of PPD on the performance of low-leakage current devices.

Chapter 1 briefly summarizes the evolution of semiconductor devices and the research background of plasma-induced damage. Chapter 2 explains test sample structures, instrumentation, and analysis techniques used in this study. Chapter 3 discusses the electronic structure and profile of low-density latent defects in the vertical (depth) direction created in the test structures during plasma etching. Various analysis techniques combined with conventional transmission electron microscopy and spectroscopic ellipsometry were applied to assess defects in low-density regions. Chapter 4 focuses on plasma-induced defect creation in the vertical and lateral directions of Si substrates. Devices with different p–n junction structures were designed to evaluate low-density defects in Si substrates, particularly in the lateral direction—lateral PPD. Chapter 5 proposes a model for the effects of created defects on the p–n junction leakage current

increase in combination with technology computer-aided design simulations. Chapter 6 discusses the influence of the lateral PPD on the increase in p–n junction leakage current (dark current) of CISs. Chapter 7 concludes with the achievements of this study.

# Table of contents

# Symbols

| | |
|---|---|
| $A$ | atomic weight |
| $c$ | the speed of light in vacuum [m/s] |
| $C_p$ | measured parallel capacitance [F/cm$^2$] |
| $C_0$ | capacitance at zero bias [F/cm$^2$] |
| $d_{IL}$ | thickness of an interfacial layer [nm] |
| $d_R$ | Si recess depth [nm] |
| $d_{SL}$ | thickness of a surface layer [nm] |
| $d_{total}$ | the total thickness of surface layer (SL) and interfacial layer (IL) [nm] |
| $D_{CJ}$ | lateral distance from the sidewall surface of a contact hole to the center of depletion region |
| $D_{edge}$ | lateral distance between the sidewall surface of a contact hole and the edge of n-type region |
| $D_n$, $D_p$ | the diffusion coefficient of electron/hole |
| $D_{pn}$ | lateral distance between p- and n-type regions [nm] |
| $D_+$ | positron diffusion coefficient |
| $e$, $q$ | elementary charge (= $1.602 \times 10^{-19}$ [C]) |
| $E$ | energy in the Si band diagram [eV] |
| $E_b$ | beam energy in a cathodoluminescence (CL) measurement [eV] |
| $E_C$ | the bottom edge of the conduction band of Si [eV] |
| $E_F$ | the Fermi energy level of Si [eV] |
| $E_g$ | the energy band gap of Si [eV] |
| $E_i$ | the Fermi level of the intrinsic Si [eV] |
| $E_{PAS}$ | incident positron energy [eV] |
| $E_\gamma$ | γ-ray energy in a positron annihilation measurement [eV] |
| $E_t$ | energy level of carrier trapping sites (trap level) [eV] |
| $E_V$ | the top edge of the valence band of Si [eV] |
| $f$ | modulation frequency in a capacitance—voltage measurement [Hz] |
| $f_{Si}$ | the volume fraction of silicon region |
| $F_m$ | maximum electric field at the p–n junction [V/cm] |
| $F_0$ | a material-dependent constant for band-to-band tunneling |
| $h$ | Planck constant (= $6.626 \times 10^{-34}$ [J·s]) |
| $\hbar$ | reduced Planck constant ($\hbar = h/2\pi$) |
| $I_{dark}$ | dark current [A] |
| $I_L$ | lateral leakage current [A] |

| | |
|---|---|
| $I_{leak}$ | leakage current [A] |
| $I_V$ | vertical leakage current [A] |
| $J_A$ | areal current density [A/cm$^2$] |
| $J_{BBT}$ | band-to-band tunneling current density [A/cm$^2$] |
| $J_{diff}$ | diffusion current density [A/cm$^2$] |
| $J_p$ | hole diffusion current density [A/cm$^2$] |
| $J_{PF}$ | Poole–Frenkel current density [A/cm$^2$] |
| $J_n$ | electron diffusion current density [A/cm$^2$] |
| $J_{SRH}$ | Shockley–Read–Hall (SRH) current density [A/cm$^2$] |
| $J_{TAT}$ | trap-assisted tunneling (TAT) current density [A/cm$^2$] |
| $J_0$ | saturation current density [A/cm$^2$] |
| $k$, $k_B$ | Boltzmann constant (= $1.3807 \times 10^{-23}$ [J/K]) |
| $L_d$ | diffusion length [nm] |
| $L_g$ | gate length [nm] |
| $L_n$, $L_p$ | the diffusion length of electrons/holes [nm] |
| $m$ | mass of atom [kg] |
| $m^*$ | effective mass of the carriers [kg] |
| $n$ | electron/positron density [cm$^{-3}$] |
| $N_A$ | acceptor concentration [cm$^{-3}$] |
| $N_B$ | doping concentration [cm$^{-3}$] |
| $N_D$ | donor concentration [cm$^{-3}$] |
| $N_{peak}$ | peak densities (of defects) [cm$^{-2}$] |
| $n_{dam}$ | density of defects [cm$^{-3}$] |
| $n_i$ | intrinsic carrier density [cm$^{-3}$] |
| $n_t$ | density of recombination centers (density of traps) [cm$^{-3}$] |
| $n_0$ | peak densities (of defects) [cm$^{-3}$] |
| $p$ | hole density [cm$^{-3}$] |
| $R_p$ | projection range [nm] |
| $S_j$ | area of p–n junction |
| $T$ | absolute temperature [K] |
| $T_{ox}$ | oxide thickness [nm] |
| $T_{sub}$ | Si substrate temperature during electrical measurement [K] |
| $U$ | recombination rate |
| $v_{th}$ | thermal velocity of carriers [cm/s] |
| $V$ | applied voltage [V] |
| $V_b$ | bias voltage [V] |

| | |
|---|---|
| $V_{bi}$ | built-in voltage [V] ($eV_{bi}$: built-in potential [eV]) |
| $V_{CG}$ | control gate voltage [V] |
| $V_{CL}$ | electron beam acceleration voltage in a CL measurement [V] |
| $V_D$ | drain voltage [V] |
| $V_{dc}$ | self-dc bias voltage [V] |
| $V_{FB}$ | flat-band voltage [V] |
| $V_G$ | gate voltage [V] |
| $V_{pn}$ | reverse bias voltage applied to p–n junction [V] |
| $V_{pp}$ | peak-to-peak voltage [V] |
| $V_{NW}$ | bias voltage applied to n-type well (n-well, Nwell) [V] |
| $V_{PW}$ | bias voltage applied to p-type well (p-well, Pwell) [V] |
| $V_r$, $V_{rev}$ | reverse bias voltage [V] |
| $V_S$ | source voltage [V] |
| $V_{sub}$ | substrate voltage [V] |
| $W$ | gate width, channel width [nm] |
| $W_{dep}$ | depletion width [nm] |
| $W_{p–n}$ | lateral p–n junction width [nm] |
| $W_0$ | depletion (region) width at zero-bias voltage [nm] |
| $Z$ | atomic number |
| $\alpha$ | impurity gradient [$cm^{-4}$] |
| $\Gamma$ | field enhancement factor |
| $\Delta J_{pn}$ | p–n junction leakage current density increase [$A/cm^2$] |
| $\varepsilon_{Si}$, $\varepsilon_s$ | the relative permittivity of silicon (= 11.7) |
| $\varepsilon_0$ | permittivity of vacuum (= $8.85 \times 10^{-12}$ [F/m]) |
| $\lambda$ | characteristic length of a defect profile [nm] |
| $\sigma$ | the standard deviation of defect distribution [cm] |
| $\kappa_{eff}$ | effective decay rate [$s^{-1}$] |
| $\rho$ | density of material [$g/cm^3$] |
| $\sigma_n$, $\sigma_p$ | capture cross-section of electrons/holes [$cm^2$] |
| $\sigma_0$ | capture cross-section of carriers [$cm^2$] |
| $\tau$ | carrier life time [s] |
| $\tau_g$ | carrier generation lifetime [s] |
| $\tau_n$ | electron lifetime [s] |
| $\tau_p$ | hole lifetime [s] |
| $\varphi_p$ | plasma potential [V] |
| $\Phi$ | diameter of a contact hole [nm] |

# Abbreviations

| | |
|---|---|
| APM | ammonium hydrogen peroxide mixture |
| CCP | capacitively coupled plasma |
| CDE | chemical dry etching |
| CG | control gate |
| CIS | CMOS image sensor |
| CL | cathodoluminescence |
| CMOS | complementary metal−oxide−semiconductor |
| *CV*, *C*−*V* | capacitance−voltage |
| CVD | chemical vapor deposition |
| DHF | diluted hydrofluoric acid |
| DTEG | device TEG |
| ECR | electron cyclotron resonance |
| EMA | effective medium approximation |
| ESR | electron spin resonance |
| FA | furnace annealing |
| FD | floating diffusion |
| FG | floating gate |
| FET | field-effect transistor |
| GP-IB | general purpose interface bus |
| HF | hydrofluoric acid |
| HTO | high-temperature oxide |
| IC | integrated circuit |
| ICP | inductively-coupled plasma |
| IL | interfacial (transition) layer |
| ISSG | in-situ steam generation |
| ITRS | International Technology Roadmap for Semiconductors |
| *IV*, *I*−*V* | current−voltage |
| LCR | inductance−capacitance−resistance |
| LSI | large-scale integration |
| LT | low temperature |
| MD | molecular dynamics |
| MEMS | micro-electro-mechanical systems |
| MIM | metal−insulator−metal |
| MOS | metal–oxide–semiconductor |

| | |
|---|---|
| MSE | mean squared error |
| NAND | Not AND |
| OPF | organic photoconductive film |
| PAS | positron annihilation spectroscopy |
| PD | photo diode |
| PE | plasma etching |
| PID | plasma-induced damage |
| PMD | pre-metal dielectric |
| PPD | plasma-induced physical damage |
| PTEG | process TEG |
| RF | radio frequency |
| RIE | reactive ion etching |
| RS | reset |
| RTA | rapid thermal annealing |
| SE | spectroscopic ellipsometry |
| SEL | select |
| SF | (source follower) amplifier |
| SIMS | secondary ion mass spectroscopy |
| SL | surface (oxidized) layer |
| SMU | source monitor unit |
| SoC | system on a chip |
| SPM | sulfuric acid–hydrogen peroxide mixture |
| SRH | Shockley–Read–Hall |
| sub, Sub | substrate |
| TAT | trap-assisted tunneling |
| TCAD | technology computer-aided design |
| TEG | test element group |
| TEM | transmission electron microscopy |
| TO | transverse optical |
| TOF | time-of-flight |
| Tr | transistor |
| TRS | transfer |
| ULSI | ultra-large-scale integration |
| UV | ultraviolet |
| VEPFIT | variable energy positron fit |
| VLSI | very-large-scale integration |

| | |
|---|---|
| VUV | vacuum ultraviolet |
| WE | wet etching/wet (etch) cleaning |
| 2D | two dimensional |
| 3D | three dimensional |

# Chapter 1

# General introduction

## 1.1 Brief history of semiconductors

Semiconductors are essential components of current electronic devices. The major development of semiconductor devices dates back to the invention of transistors over half a century ago. Bardeen and Brattain at the Bell Laboratories invented a point-contact transistor in 1947.[1] Shockley at the Bell Laboratories designed a "junction" transistor in 1948.[2] Atalla and Kahng at the Bell Laboratories proposed a metal–oxide–semiconductor field-effect transistor (MOSFET) in 1959, which is a basic element of modern electronics.[3] In the 1960s, integrated circuits (ICs) comprising transistors, resistors, and capacitors were developed. In the 1970s, large-scale integration (LSI) circuits were introduced in computer memories and pocket calculators. In the 1980s, with the development of semiconductor manufacturing technologies, ICs with more than 100,000 transistors on a single chip were produced. ICs with more than 100,000 transistors on a single chip are called very-large-scale integrated (VLSI) circuits, and ICs with more than 1 million transistors are called ultra-large-scale integrated circuits.[4] In the 2000s, the mass production of a system-on-a-chip (SoC) began. SoC is an integrated circuit or chip that combines various components of a computer system onto a single chip.[5,6] The present semiconductor devices in which billions of transistors are implemented have a growing significance in our daily lives.

## 1.2 Scaling of MOSFETs

Semiconductor device technology has evolved substantially over the past half-century according to Moore's law.[7] According to Moore's law, the number of transistors on a microchip doubles about every two years. In 1974, Dennard reported that the operating speed of a device can be improved as the dimensions of a transistor were shrunk by the scaling factor $k$.[8] The schematic of MOSFET scaling by a factor of $k$ is shown in Fig. 1.1. Scaling factors for device or circuit parameters are listed in Table 1.1. This scaling trend has a guiding significance for the reduction in feature sizes of MOSFETs. The reduction in the gate length of MOSFETs over the past three decades is shown in Fig. 1.2. Although the decreasing rate of MOSFET scaling has gradually reduced recently, the performance of MOSFETs has been improved with the introduction of novel device structures and materials.[9,10]

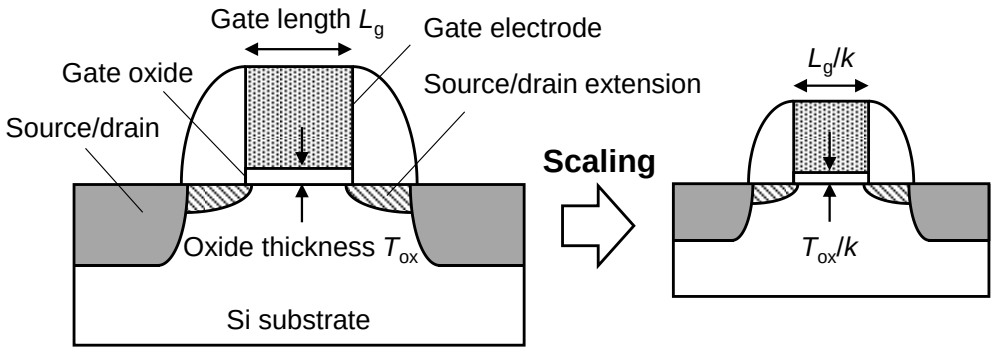



Figure 1.1 Schematic of MOSFET scaling.

Table 1.1 Scenarios of MOSFET scaling under a constant voltage operation.

| Device or circuit parameter | Scaling factor |
|---|---|
| Oxide thickness $T_{ox}$ | $1/k$ |
| Gate length $L_g$ | $1/k$ |
| Gate width $W$ | $1/k$ |
| Doping concentration $N_D$, $N_A$ | $k$ |
| Voltage $V$ | $1/k$ |
| Current $I$ | $1/k$ |
| Decay time $VC/I$ | $1/k$ |
| Power density | 1 |

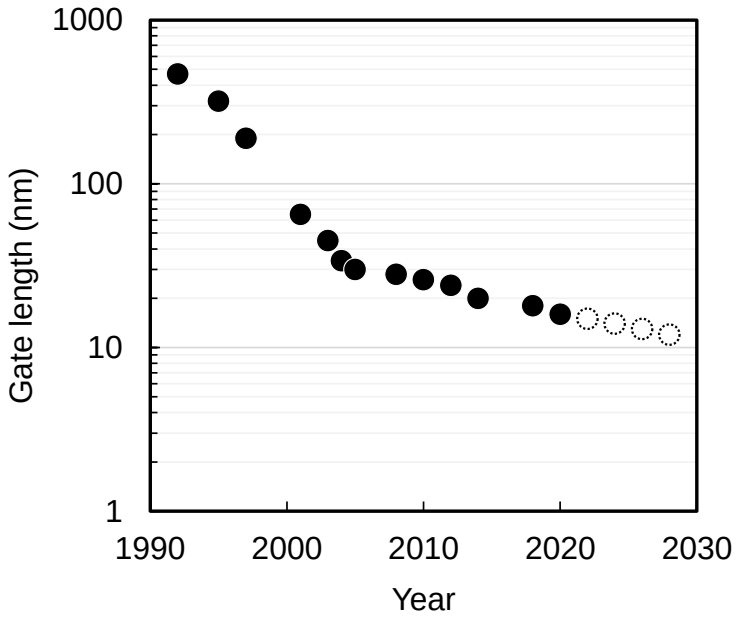



Figure 1.2 Scaling of gate length in MOSFETs against the year of production.

## 1.3 More Moore devices—FinFET and NAND Flash memory

The terms "More Moore" and "More than Moore" were defined in the 2007 International Technology Roadmap for Semiconductors (ITRS).[11] The trend of More Moore and More than Moore is shown in Fig. 1.3. "More Moore" refers to an attempt to further scale a MOSFET. It includes the transition of the device from a two-dimensional (2D) to a three-dimensional (3D) structure with the incorporation of novel materials and process technologies, in addition to the basic geometric scaling of the device feature sizes. "More than Moore" refers to an attempt to incorporate various functions into devices, although it does not necessarily follow Moore's law. More-than-Moore devices include radio frequency (RF) devices, power electronics, micro-electro-mechanical systems (MEMS), and sensors with complementary metal–oxide–semiconductor (CMOS) image sensors. This subsection briefly describes fin field-effect transistors (FinFETs) and 3D NAND flash memories.

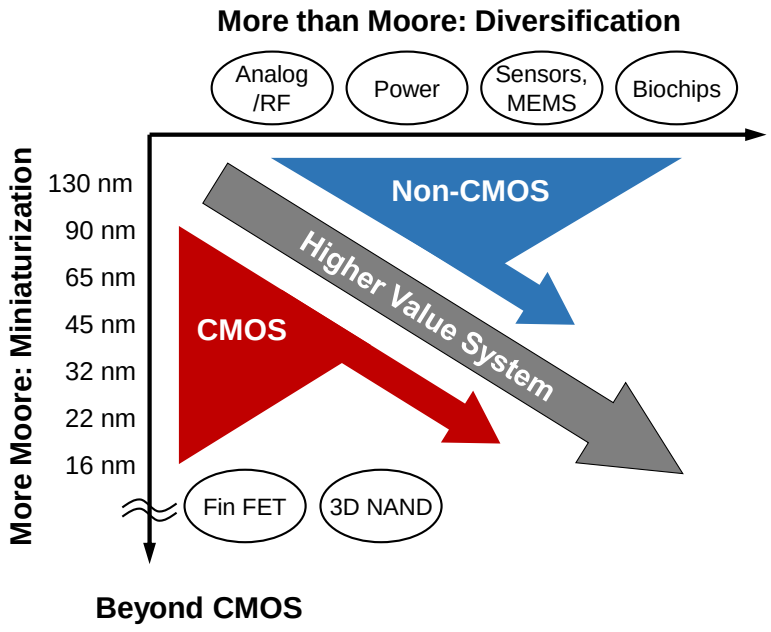



Figure 1.3 Trends of "More Moore" and "More than Moore".[11]

A FinFET is a 3D structure with Si fins functioning as the drain and source. The channel region is covered partially with the gate electrode.[12] The schematics of a conventional 2D planar FET and a 3D FinFET are shown in Figs. 1.4(a) and 1.4(b), respectively. As shown in Fig. 1.4(b), the structure in which the gate electrode surrounds the channel region provides better electrical control of the channel, leading to the reduction of off-state leakage current and suppression of the short-channel effect. Precisely controlled plasma etching (PE) is widely used in the fabrication of FinFETs. However, the defects created by PE may influence device performance.[13–15]

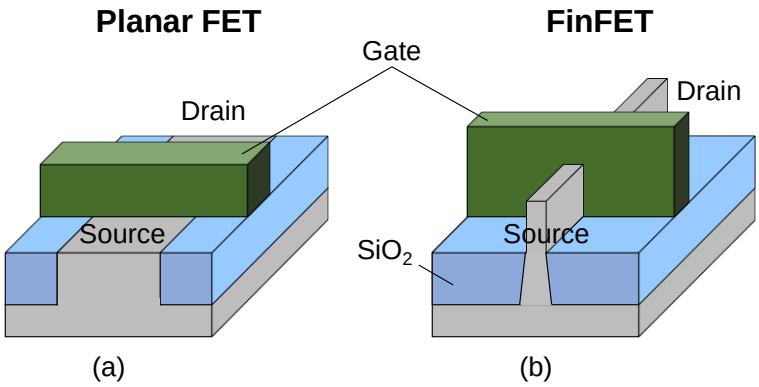
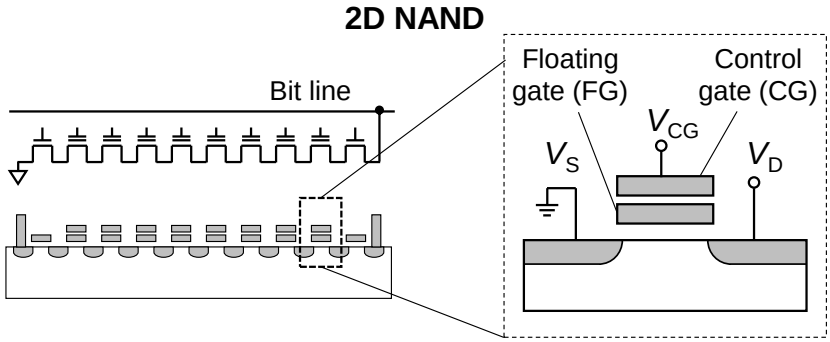


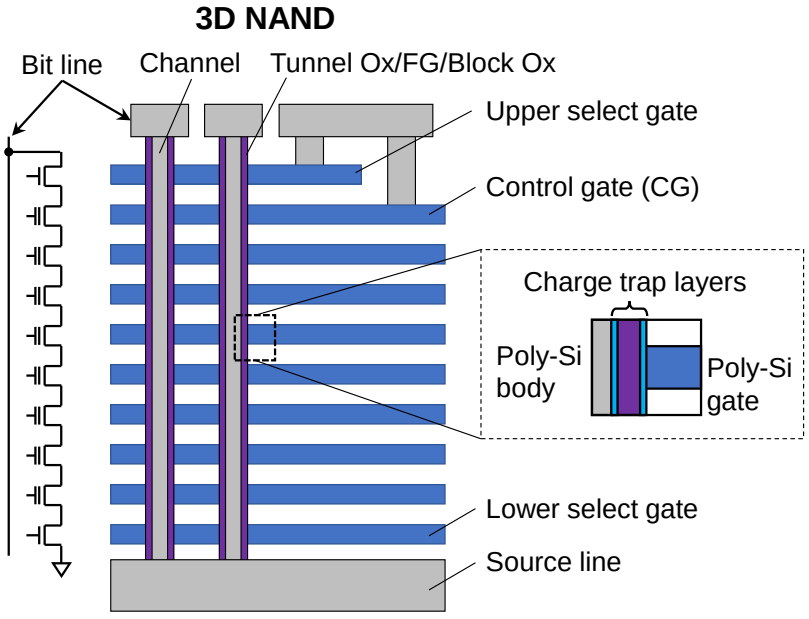

Figure 1.4 Schematics of (a) planar FET and (b) FinFET structures.

NAND flash memory is a type of non-volatile memory. With the increasing density of planar-type (2D) NAND flash memory, the degradation of reliability owing to memory-cell leakage current is becoming problematic. The device structure of NAND flash memory has evolved into a 3D structure to overcome the scaling limit of 2D NAND flash memory.[16] The schematics of conventional 2D and 3D NAND flash memory cell structures are shown in Figs. 1.5(a) and 1.5(b), respectively. The 3D NAND flash memory

has a vertical stack of memory cells beyond 100 layers to increase "per-chip density." High aspect ratio (> 40) vertical "channel" holes through the stacked cell layers are formed by PE. High-energy ions from plasma create defects not only in the Si substrate (the source line) but also near the sidewall (in the lateral direction) of the channel holes. Thus, understanding the impacts of plasma-induced damage (PID) on performance is crucial to realizing high-quality and high-performance devices.




(a)




(b)

Figure 1.5 Cross-sectional schematics and equivalent circuits of (a) 2D NAND and (b) 3D NAND flash memory cell.

## 1.4 More-than-Moore device—CMOS image sensor

This subsection describes CMOS image sensors (CIS) as an example of "More than Moore" devices. CIS is an electronic device that converts the light received through the optical lens into an electrical image signal.[17] CISs are used in digital cameras and smartphones, as well as in broadcast, industry, medical, and consumer applications. The imaging area comprises a 2D array of pixels arranged in columns and rows. Generally, each pixel has three or four transistors and a photodiode. A typical circuit diagram and a cross-sectional schematic of a pixel are shown in Figs. 1.6 and 1.7(a), respectively.[18,19] The pixel circuit comprises a photoconversion device (photodiode), a transfer transistor, a reset transistor, a source follower transistor, a select transistor, and the floating diffusion (FD) region. Incident light is converted into charges (electrons) using a photodiode (PD). The charges in the PD are transferred to the FD with the cycle of turning ON the transfer transistor. The charges in the FD region are amplified by the source follower transistor, providing an electrical signal output. Another CIS pixel with a photoelectric conversion unit being separated from a charge storage [see Fig. 1.7(a)] unit was also investigated. A cross-sectional schematic of a pixel of an organic photoconductive film (OPF) image sensor is shown in Fig. 1.7 (b).[20] The charges generated by photoelectric conversion in the OPF are accumulated in the FD in the Si substrate. The leakage current (dark current) in the PD and FD regions is a major issue because it determines the imaging performance under conditions of low light illumination. Even low-density of defects might increase the loss of stored charges, degrading the performance of CISs. Thus, understanding the creation of low-density defects during plasma processing and its impact on device performance, such as dark current is crucial to design future ultra-low leakage devices, such as CISs.

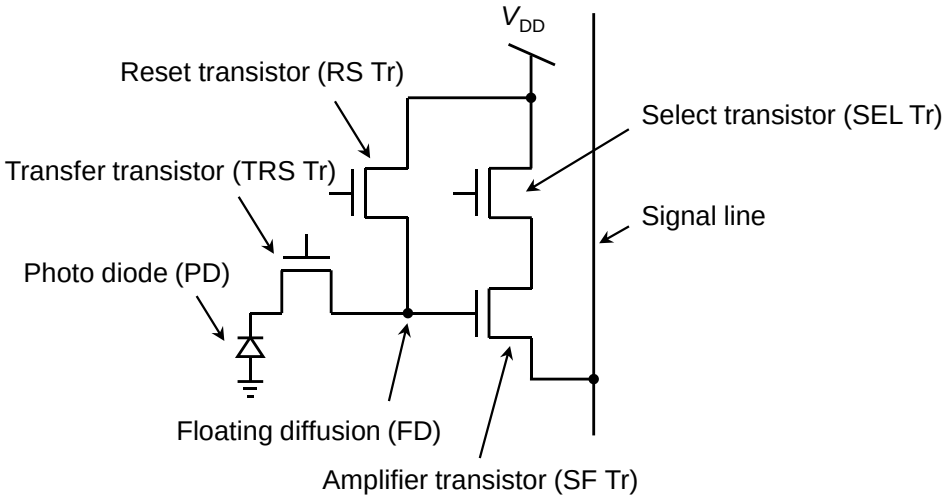



Figure 1.6 Circuit diagram of a four-transistor CMOS image sensor pixel.

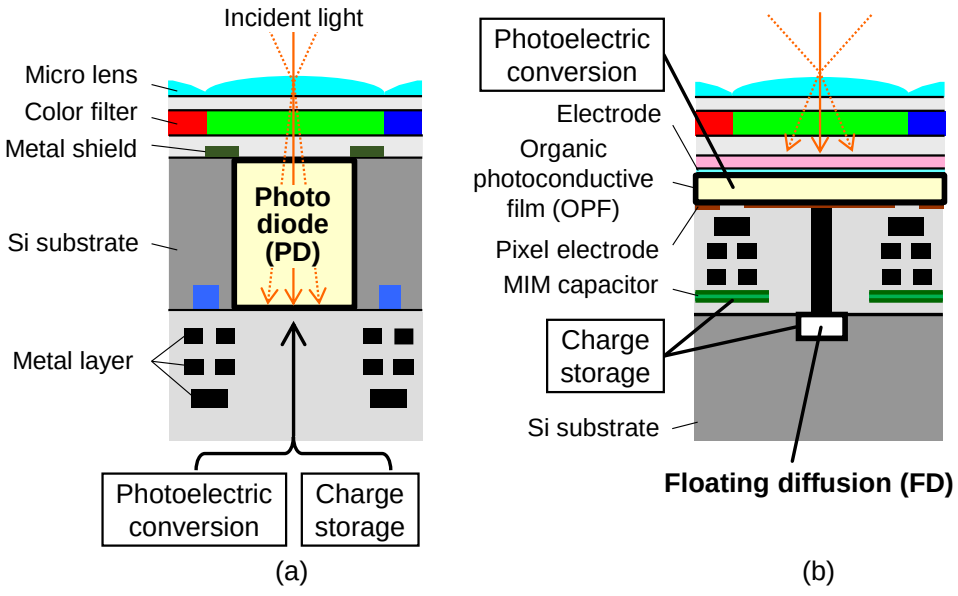



Figure 1.7 Cross-sectional schematics of (a) a back-illuminated CMOS image sensor and (b) an OPF CMOS image sensor.

## 1.5 Plasma etching and plasma-induced damage

Here, the fabrication technologies of advanced electronic devices are briefly reviewed. Photolithography and dry (plasma) etching processes are crucial in the manufacture of semiconductor ICs. Photolithography is the process of transferring circuit patterns on a mask onto a substrate or a film coated with a resist. During photolithography, ultraviolet (UV) light is irradiated to a light-sensitive chemical photoresist (or resist) on a material [Fig. 1.8(a)] through a geometric pattern (a photomask). In the next resist development process, a chemical developer [Fig. 1.8(b)] dissolves the light-irradiated positive photoresist. The area not covered by the photoresist is removed by dry etching (wet etching in some cases). Thus, the photomask pattern is subsequently transferred to the materials to be processed [Fig. 1.8(c)].

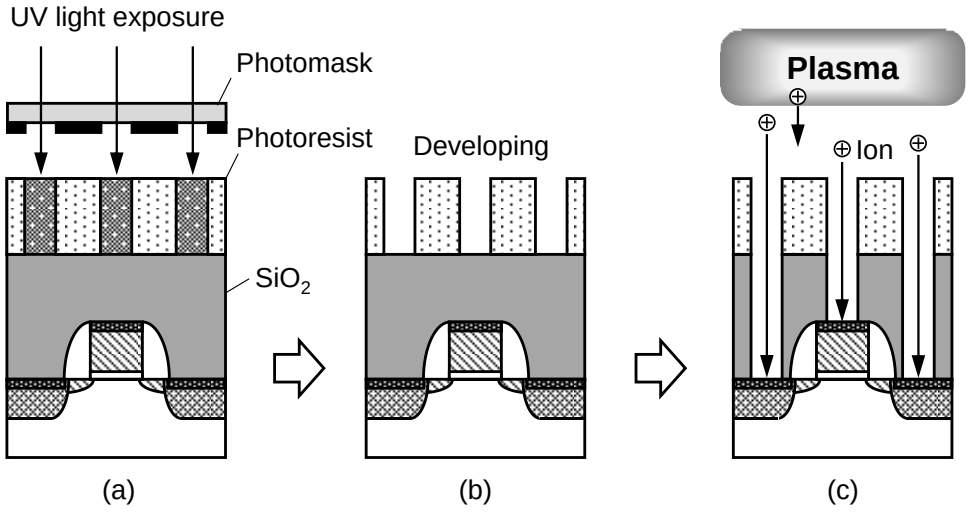



Figure 1.8 Photolithography and dry etching processes. (a) Photoresist coating and UV light exposure, (b) developing, and (c) dry etching.

Two types of etching processes exist, wet and dry etching. Wet etching (WE) utilizes liquid chemicals or etchants to remove materials. For example, diluted hydrofluoric acid (DHF) is used for WE of an oxide film. Conversely, dry etching utilizes plasma or reactive gases to remove materials from surfaces. Dry etching is classified into three types based on the etching mechanism: physical, chemical, and reactive ion etching (RIE).[21,22] In physical etching (sputtering), the surface region of a material is etched by the bombardment of high-energy incident ions. In chemical etching, the etching mechanism is governed by the chemical reaction between gas species (radicals) generated in plasma and elements in the material. Generally, chemical etching proceeds isotopically. RIE combines chemical and physical reactions. RIE is primarily advantageous in that the etching process can be designed to be highly anisotropic. The schematic of parallel plate RIE equipment is shown in Fig. 1.9.[23–25] In parallel plate RIE equipment, an upper plate is grounded, whereas RF power is applied to a lower plate. Plasma is generated between a pair of parallel plate electrodes in the chamber under low pressure (generally $<10^3$ Pa). The boundary region between the plasma bulk and the electrodes (chamber wall) is called a "plasma sheath."[23,25] Plasma sheath forms a positive plasma potential with respect to the grounded chamber wall, as shown on the right side of Fig. 1.9. The chemical etching reaction on the material surface is promoted by the energy of incident ions accelerated in the plasma sheath. RIE processes enabling anisotropy etching features are commonly employed in manufacturing semiconductor devices.

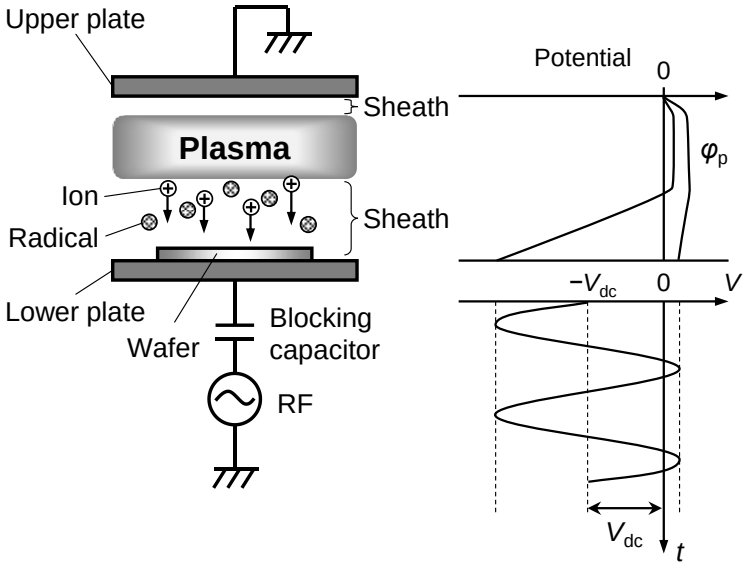



Figure 1.9 Schematic of a parallel plate PE equipment and plasma potential profiles in response to applied bias in an RIE process.

Plasma processing is widely used to fabricate fine patterns with anisotropic features and is indispensable in manufacturing advanced devices, such as fin-FETs, 3D NAND flash memories, and image sensors. The bombardment of ions accelerated in the plasma sheath during PE results in the creation of defects.[26–29] Defect creation during plasma processing is referred to as PID. Plasma-induced damage is crucial in the design of leading-edge devices because PID is not inherently scalable in accordance with the device's feature size. Principally, PID is classified into three categories based on the mechanisms of its creation,[30] (1) physical damage (plasma-induced physical damage, PPD),[29,31–33] (2) charging damage,[34–36] and (3) radiation damage,[37–39] as shown in Fig. 1.10.

Physical damage is induced by the bombardment of ions accelerated in the sheath. Generally, the energy of ions is sufficiently high (sometimes larger than hundreds of eV) to create defects in the material exposed to the plasma. Incident ions penetrate the device structure leading to the deformation of the network of atomic bonding in a region with a depth of several nm from the material surface. In the 1980s, PPD to Si substrates was reported by Oehrlein.[32] and Yabumoto et al.[31] A recent issue with PPD is the formation of the Si recess structure.[28] A Si recess formation owing to PPD is shown in Fig. 1.11. A heavily damaged layer in a Si substrate is formed during the etching of gate electrodes or offset spacers at the gate sidewall. The heavily damaged layer is easily oxidized when exposed to air. The oxidized region is removed by subsequent WE resulting in the formation of Si recess. The change in the topological feature of source/drain regions degrades device performance, that is, enhances the fluctuations in transistor properties, such as threshold voltage. Localized defects are found in the plasma-exposed Si substrates even after removing the defects created in the surface region by subsequent WE. Notably, the region containing these localized defects is rarely removed because the region is not subject to oxidation by air exposure. This study focuses on these localized defects, defined as latent defects. Notably, latent defects beneath the oxidized region after plasma exposure remain after WE and subsequent annealing processes.[40–43] The influence of PPD on device performance and reliability is critical in the context of scaled CISs requiring an extremely low-defect density. This study aims to clarify the PPD mechanism.

Charging damage is induced by high electric field stress on the gate oxide of a MOSFET during plasma processing. The electrical stress originates from plasma non-uniformity (that is, the variation of plasma potential and density over a wafer). The gate oxide is degraded by the charging current, degrading the oxide reliability. Charging

damage is enhanced by interconnected structures, e.g., the area ratio of an antenna to the gate oxide. This enhanced mechanism is called "the antenna effect." Charging damage must be addressed in the plasma process and circuit layout design.

Radiation damage is induced by high-energy photons, such as UV and vacuum ultraviolet (VUV) photons from plasma. High-energy photons generate electron-hole pairs in a dielectric film (e.g., $SiO_2$ film), resulting in a shift in the threshold voltage of MOSFETs. UV/VUV radiation is considered to break chemical bonds in materials, such as low-*k* dielectric films. Bond breaking increases the dielectric constant of a film.

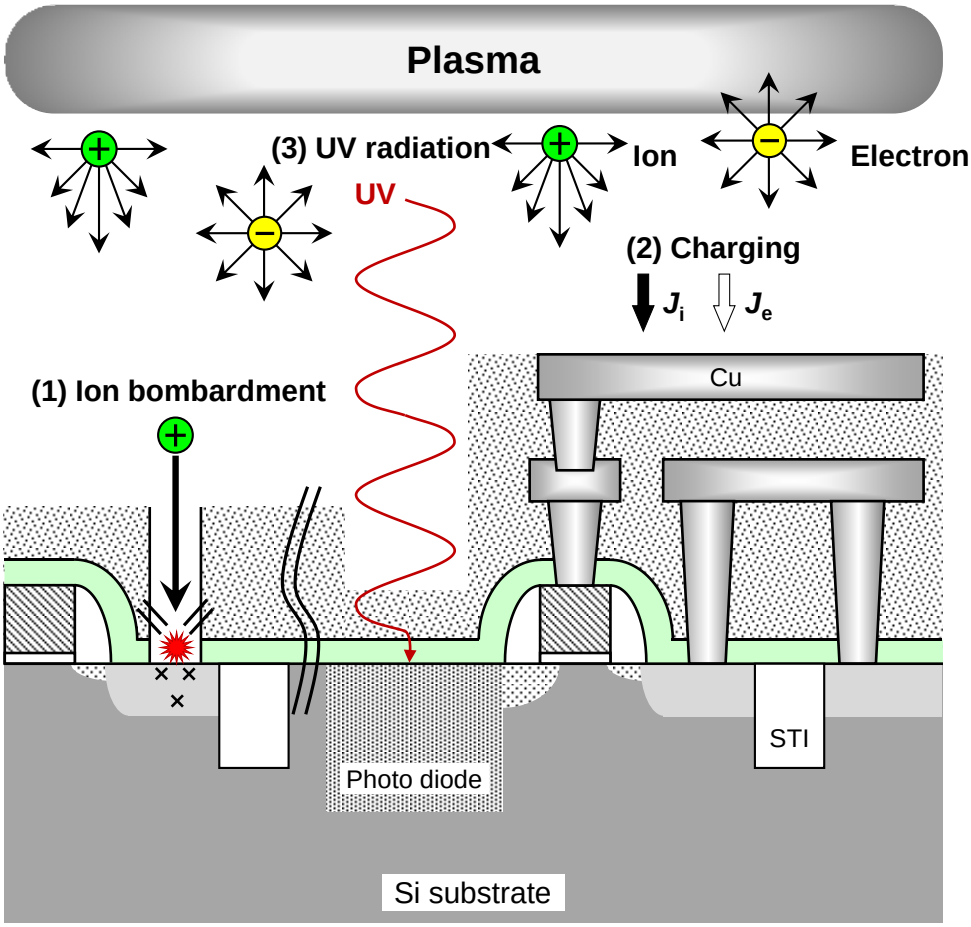



Figure 1.10 Schematic of plasma-induced degradation mechanisms.

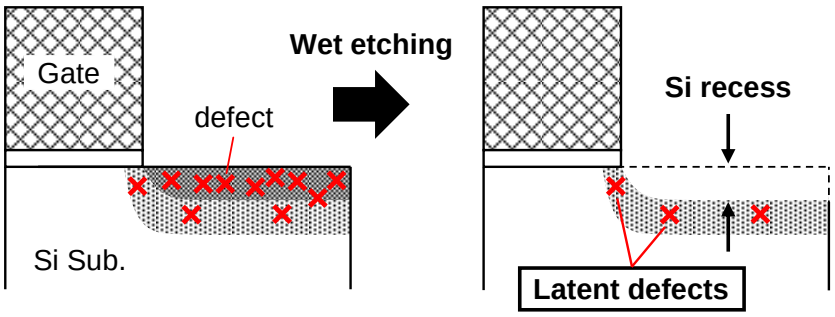



Figure 1.11 Si recess formation owing to PPD.

The thickness of a damaged layer and the density of defects are principal parameters in the assessment of PPD. Transmission electron microscopy (TEM) and spectroscopic ellipsometry (SE) are widely used techniques for thickness assessment.[44–46] Electrical techniques, such as current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) measurements are used to characterize the defect density.[43,47–53] Although these methods can detect the presence of defects (in Si substrates) after PPD, quantifying defect densities $< 10^{18}$ $cm^{-3}$ and detailedly predicting their profiles is challenging owing to detection limits. However, few studies have focused on the sensitivity or detection limits of PPD evaluation techniques. The quantification of latent defects in low-density regions is crucial in the design of advanced devices, such as CISs. The presence of low-density defects significantly increases the dark current, degrading the CIS performance. A highly sensitive defect detection technique is indispensable to understanding the defect creation mechanism and assigning defect distribution.[54]

According to the transition of advanced devices from 2D to 3D, defect creation both in the vertical and lateral directions has become a major issue. The lateral defect

creation mechanism is attributed to the straggling of incident ions. In the case of ion implantation process designs, Furukawa et al. reported on the theoretical analysis of the lateral spreading of implanted ions. [55] Molecular dynamics (MD) simulations predict the lateral straggling in fin structures in the case of PE.[13] Impinging ions penetrate the crystalline Si region to be etched "in the vertical and lateral directions" owing to stochastic mechanisms during the etching of a fin structure. The defect density in the lateral direction is considerably lower than that in the vertical direction by at most 1/10,[13,56] indicating the difficulty in assessing the defect density. Spatially resolved structural analysis and/or electrical measurements using specifically designed devices should be employed to assign the lateral (spatial) distribution of defects created by PPD. Electrical methods are believed to be sufficiently sensitive for PPD analysis. Both *I–V* measurements using Schottky contact structures and *C–V* measurements of the change in damaged-layer capacitance are used.[43,47–51] However, in terms of the defect density, these conventional methods cannot be applied to assess the defects created by stochastic straggling in the lateral direction, as shown in Fig. 1.12. Specific test structures should be designed to improve the detection limit of lateral PPD characterization.

The presence of lateral defects has been predicted using MD simulation as aforementioned. However, to date, the effect of low-density defects created by lateral straggling of incident species on leakage current remains unclear. A simplified model to predict the effect of low-density defects created by lateral straggling on leakage current is required to design low-leakage devices, such as CISs. The relationship between created defects and junction leakage current must be clarified to design future CISs.

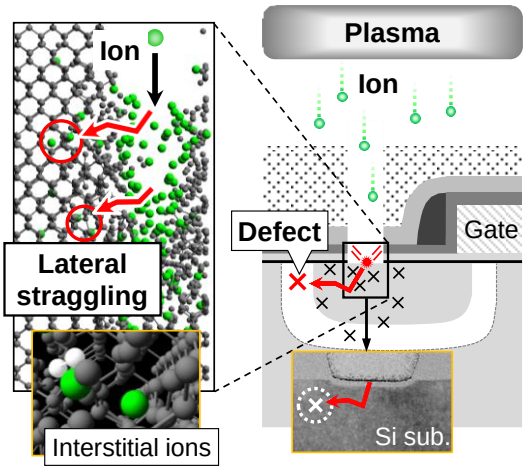



Figure 1.12 Schematic of the creation mechanism of PPD in a Si substrate.

## 1.6 Objective of this study

This study aims to establish an evaluation scheme for low-density defects by plasma exposure and to clarify their effects on ultra-low leakage devices.

The structure of this study is outlined in Fig. 1.13. In Chapter 2, the test sample structures, instrumentation, and analysis techniques are examined. Chapter 3 focuses on the structure and profile of latent defects in the vertical (depth) direction created by PE. Secondary ion mass spectrometry (SIMS), time-of-flight SIMS (TOF−SIMS), positron annihilation spectroscopy (PAS), and the cathodoluminescence (CL) method, as well as TEM and SE analyses, were utilized to assess defects in low-density regions. In Chapter 4, defect creation in the vertical and lateral directions of Si substrates using designed devices with different p–n junction structures was investigated. Chemical dry etching (CDE) was employed after plasma exposure to examine the influence of the residual species in a damaged layer. Blanket wafers were prepared for physical analyses and *C–V*

measurement to evaluate the effects of plasma conditions and furnace annealing (FA). Chapter 5 proposes a model focusing on the effects of created defects on p–n junction leakage current increase ($\Delta J_{pn}$) combined with technology computer-aided design (TCAD) simulations. The prediction model was implemented to experimentally assign the profile of defects in devices with a lateral p–n junction after exposure to fluorocarbon-containing plasma. In Chapter 6, a CIS structure was employed to examine the effects of the lateral PPD on an increase in dark current ($I_{dark}$). Two test structures, that is, a single device with a p–n junction and a CIS device were used to reveal the relationship among the obtained performance changes in response to PPD. A comprehensive comparison of the parameters, such as leakage current ($I_{leak}$) in single devices and $I_{dark}$ in a CiS circuit was extensively conducted. The results obtained in this study are summarized in Chapter 7.

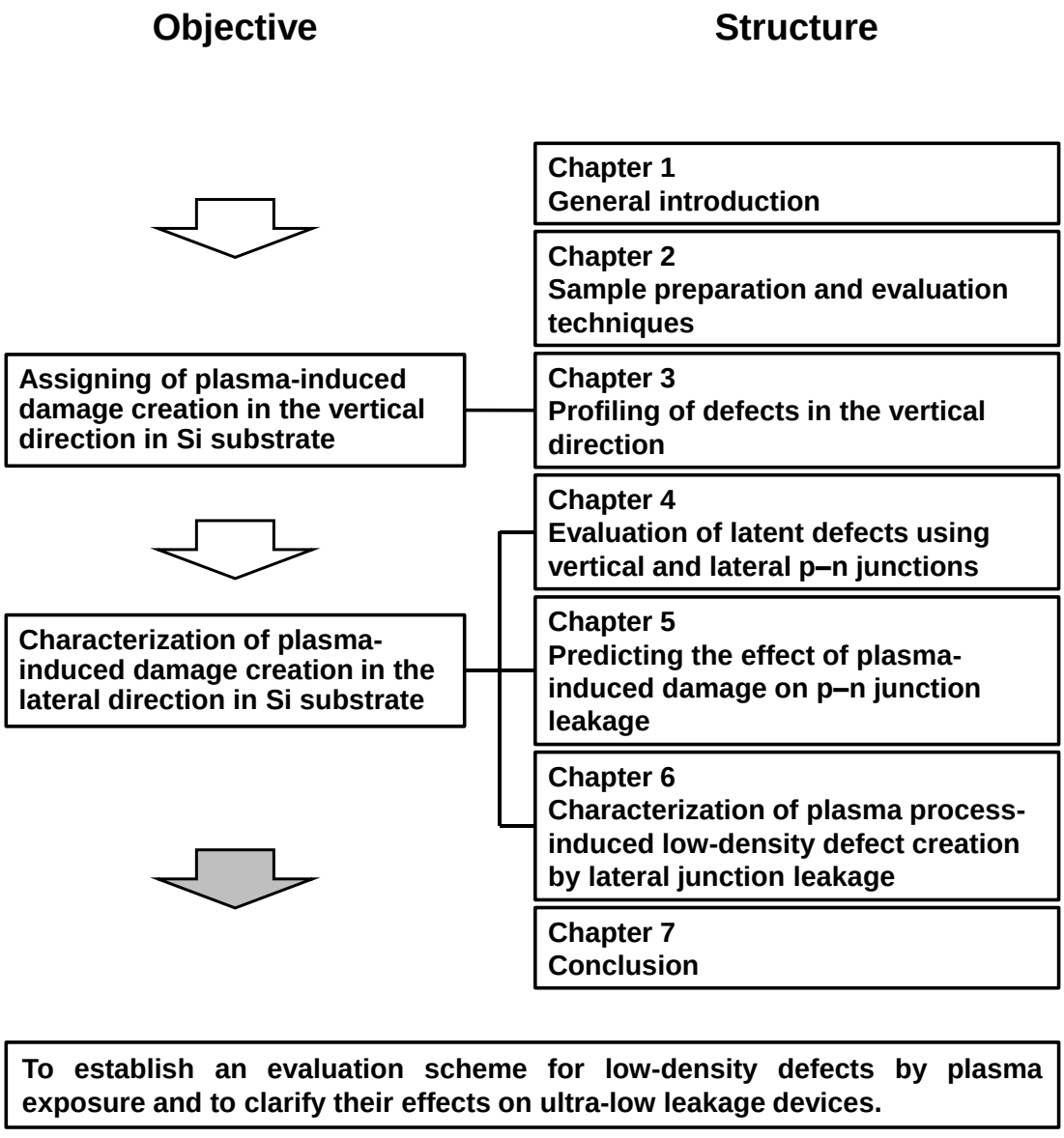



Figure 1.13 Outline of the study.

**References**

[1] J. Bardeen and W. H. Brattain, Phys. Rev. **74**, 230 (1948).

[2] W. Shockley, Bell Syst. Tech. J. **28**, 435 (1949).

[3] D. Kahng and M. M. Atalla, in *IRE-AIEEE Solid-State Device Research Conference*, Pittsburgh, 1960.

[4] J. S. Kilby, IEEE Trans. Electron Devices **23**, 648 (1976).

[5] D. Chin, in *Proc. IEEE Int. Electron Devices Meeting*, 1998, pp. 3–8.

[6] A. M. Rincon, W. R. Lee, and M. Slattery, in *Proc. IEEE Custom Integrated Circuits Conference*, 1999, pp. 83–90.

[7] G. E. Moore, IEEE Solid-State Circuits Soc. Newslett. **11**, 33 (2006).

[8] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, IEEE J. Solid-State Circuits **9**, 256 (1974).

[9] M. T. Bohr and I. A. Young, IEEE Micro **37**, 20 (2017).

[10] S. B. Samavedam, J. Ryckaert, E. Beyne, K. Ronse, N. Horiguchi, Z. Tokei, I. Radu, M. G. Bardon, M. H. Na, A. Spessot, and S. Biesemans, in *Proc. IEEE Int. Electron Devices Meeting*, 2020, pp. 1.1.1–1.1.10.

[11] SIA, *The international technology roadmap for semiconductors (ITRS)*, 2007.

[12] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, in *Proc. IEEE Int. Electron Devices Meeting*, 1989, pp. 833–836.

[13] K. Eriguchi, A. Matsuda, Y. Takao, and K. Ono, Jpn. J. Appl. Phys. **53**, 03DE02 (2014).

[14] K. Mizotani, M. Isobe, and S. Hamaguchi, J. Vac. Sci. Technol. A **33**, 021313 (2015).

[15] N. Kuboi, T. Tatsumi, H. Minari, M. Fukasawa, Y. Zaizen, J. Komachi, and T. Kawamura, J. Vac. Sci. Technol. A **35**, 061306 (2017).

[16] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi,

M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, and A. Nitayama, in *Proc. IEEE Symp. VLSI Technol.*, 2007, pp. 14–15.

[17] P. J. W. Noble, IEEE Trans. Electron Devices **15**, 202 (1968).

[18] O. Yadid-Pecht, R. Ginosar, and Y. Shacham-Diamand, IEEE Trans. Electron Devices **38**, 1772 (1991).

[19] A. J. P. Theuwissen, Solid-State Electron. **52**, 1401 (2008).

[20] K. Nishimura, S. Shishido, Y. Miyake, H. Kanehara, Y. Sato, J. Hirase, Y. Sato, Y. Tomekawa, M. Yamasaki, M. Murakami, M. Harada, and Y. Inoue, Jpn. J. Appl. Phys. **57**, 1002B4 (2018).

[21] J. W. Coburn and H. F. Winters, J. Vac. Sci. Technol. **16**, 391 (1979).

[22] C. Steinbrüchel, Appl. Phys. Lett. **55**, 1960 (1989).

[23] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing* (Wiley, New York, 2005).

[24] J. W. Coburn and H. F. Winters, J. Appl. Phys. **50**, 3189 (1979).

[25] K. Nojiri, *Dry Etching Technology for Semiconductors* (Springer International Publishing, New York, 2015).

[26] S. A. Vitale and B. A. Smith, J. Vac. Sci. Technol. B **21**, 2205 (2003).

[27] K. Eriguchi, Y. Nakakubo, A. Matsuda, Y. Takao, and K. Ono, IEEE Electron Device Lett. **30**, 1275 (2009).

[28] T. Ohchi, S. Kobayashi, M. Fukasawa, K. Kugimiya, T. Kinoshita, T. Takizawa, S. Hamaguchi, Y. Kamide, and T. Tatsumi, Jpn. J. Appl. Phys. **47**, 5324 (2008).

[29] T. Shigetoshi, M. Fukasawa, K. Nagahata, and T. Tatsumi, Jpn. J. Appl. Phys. **54**, 06GB05 (2015).

[30] K. Eriguchi and K. Ono, J. Phys. D: Appl. Phys. **41**, 024002 (2008).

[31] N. Yabumoto, M. Oshima, O. Michikami, and S. Yoshii, Jpn. J. Appl. Phys. **20**, 893 (1981).

[32] G. S. Oehrlein, Mater. Sci. Eng. B **4**, 441 (1989).

[33] T. Morimoto, H. Ohtake, and T. Wanifuchi, J. Vac. Sci. Technol. B **33**, 051811 (2015).

[34] W. M. Greene and C. K. Lau, J. Electrochem. Soc. **139**, 2948 (1992).

[35] S. Fang and J. P. McVittie, IEEE Electron Device Lett. **13**, 347 (1992).

[36] Y.-P. Tsai, C.-H. Wu, C. J. Lin, and Y.-C. King, IEEE Trans. Electron Devices **63**, 2497 (2016).

[37] J. Lee and D. B. Graves, J. Phys. D: Appl. Phys. **44**, 325203 (2011).

[38] T. Yunogami, T. Mizutani, K. Suzuki, and S. Nishimatsu, Jpn. J. Appl. Phys. **28**, 2172 (1989).

[39] M. Fukasawa, H. Matsugai, T. Honda, Y. Miyawaki, Y. Kondo, K. Takeda, H. Kondo, K. Ishikawa, M. Sekine, K. Nagahata, F. Uesawa, M. Hori, and T. Tatsumi, Jpn. J. Appl. Phys. **52**, 05ED01 (2013).

[40] Y. Sato, S. Shibata, R. Sakaida, and K. Eriguchi, in *Ext. Abs. 17th Int. Workshop on Junction Technol.*, 2017, pp. 73–76.

[41] H. Weman, J. L. Lindström, G. S. Oehrlein, and B. G. Svensson, J. Appl. Phys. **67**, 1013 (1990).

[42] T. Iwai, K. Eriguchi, S. Yamauchi, N. Noro, J. Kitagawa, and K. Ono, J. Vac. Sci. Technol. A **33**, 061403 (2015).

[43] Y. Nakakubo, A. Matsuda, M. Fukasawa, Y. Takao, T. Tatsumi, K. Eriguchi, and K. Ono, Jpn. J. Appl. Phys. **49**, 08JD02 (2010).

[44] S. C. Vitkavage and E. A. Irene, J. Appl. Phys. **64**, 1983 (1988).

[45] Y. Nakamura, T. Tatsumi, S. Kobayashi, K. Kugimiya, T. Harano, A. Ando, T. Kawase,

S. Hamaguchi, and S. Iseda, J. Vac. Sci. Technol. A **25**, 1062 (2007).

[46] A. Matsuda, Y. Nakakubo, Y. Takao, K. Eriguchi, and K. Ono, Thin Solid Films **518**, 3481 (2010).

[47] X. C. Mu, S. J. Fonash, A. Rohatgi, and J. Rieger, Appl. Phys. Lett. **48**, 1147 (1986).

[48] W. Wu and P. K. McLarty, J. Vac. Sci. Technol. A **13**, 67 (1995).

[49] K. T. Sung, S. W. Pang, M. W. Cole, and N. Pearce, J. Electrochem. Soc. **142**, 206 (1995).

[50] M. Koyama, C. Cheong, K. Yokoyama, and I. Ohdomari, Jpn. J. Appl. Phys. **36**, 6682 (1997).

[51] K. Egashira, K. Eriguchi, and S. Hashimoto, in *Proc. Int. IEEE Electron Devices Meeting*, 1998, pp. 563–565.

[52] Y. Nakakubo, K. Eriguchi, and K. Ono, ECS J. Solid State Sci. Technol. **4**, N5077 (2015).

[53] T. Hamano, K. Urabe, and K. Eriguchi, J. Phys. D: Appl. Phys. **52**, 455102 (2019).

[54] Y. Sato, S. Shibata, A. Uedono, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. A **37**, 011304 (2018).

[55] S. Furukawa, H. Matsumura, and H. Ishiwara, Jpn. J. Appl. Phys. **11**, 134 (1972).

[56] K. Eriguchi, J. Phys. D: Appl. Phys. **50**, 333001 (2017).

# Chapter 2

# Sample preparation and evaluation techniques

## 2.1 Test structures and plasma treatments

### 2.1.1 Sample structures

Two types of blanket wafer samples (Type-A and Type-B) were prepared to evaluate PPD in Si substrates. Sample structures of Type-A and Type-B are shown in Figs. 2.1(a) and 2.1(b), respectively. The samples of Type-A were directly exposed to an electron cyclotron resonance (ECR) plasma source. For Type-B samples, a 50-nm oxide layer was formed on the Si substrate surface by in situ steam generation (ISSG)[1,2] oxidation (10 nm), followed by chemical vapor deposition (CVD) (40 nm). Next, Type-B samples ($SiO_2$/Si) were exposed to the ECR plasma.

Two types of test structures with p–n junctions (Type-C and Type-D) were designed to evaluate the impacts of PPD on the leakage current. Cross-sectional views of the test structures of Type-C and Type-D are shown in Figs. 2.1(c) and 2.1(d), respectively. The Type-C sample is a single device comprising a contact hole array (~504000), denoted as a process test element group (PTEG). The Type-D sample is a CIS with an OPF.[3] The CIS (~3000 pixels) device was denoted as a device TEG (DTEG). Both device structures with p–n junctions can detect the presence of defects from an increase in the junction leakage current.

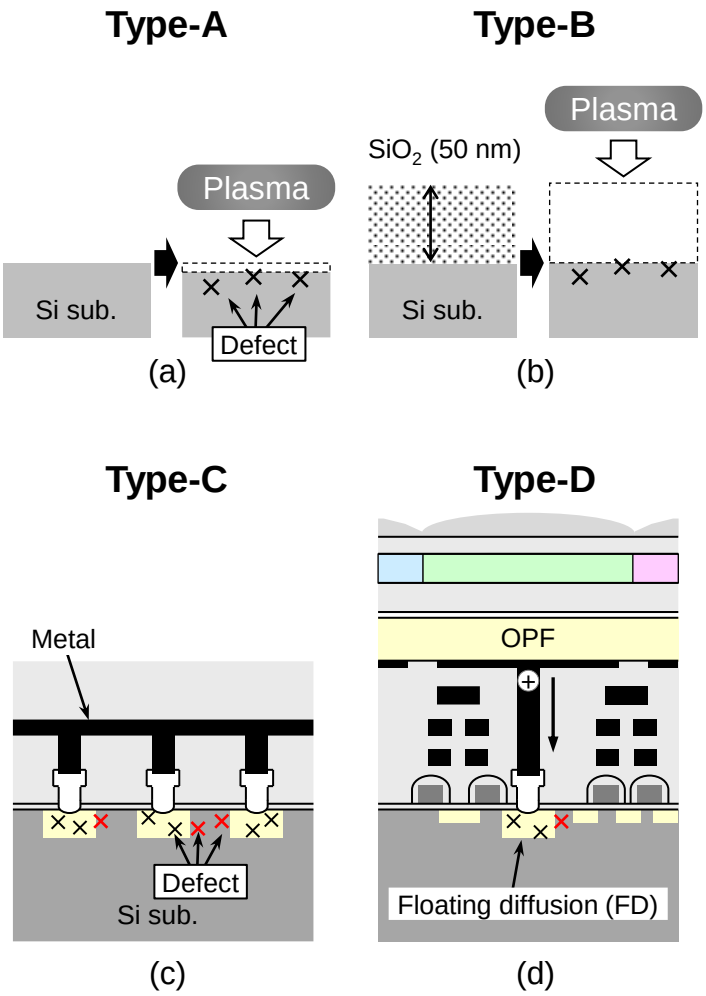



Figure 2.1 Cross-sectional views of sample structures of (a) Si blanket wafer (Type-A), (b) Si blanket wafer with an oxide film on the surface (Type-B), (c) a contact-hole array (Type-C), and (d) a CMOS image sensor with an organic photoconductive film (Type-D).

### 2.1.2 Test structure layouts

The layout and cross-sectional views of PTEG (Type-C) and DTEG (Type-D) are shown in Fig. 2.2. Both device structures were designed to detect the presence of defects using an increase in junction leakage current. The lateral distance between the p- and n-type regions ($D_{pn}$) varied from 0 to 210 nm for Type-C devices and was 90 nm for Type-D devices. The n-type region located at the bottom of a contact hole in the PTEG was set to 160 × 160 nm. The contact opening diameters ($\Phi$) of PTEG and DTEG are listed in Table 2.1.

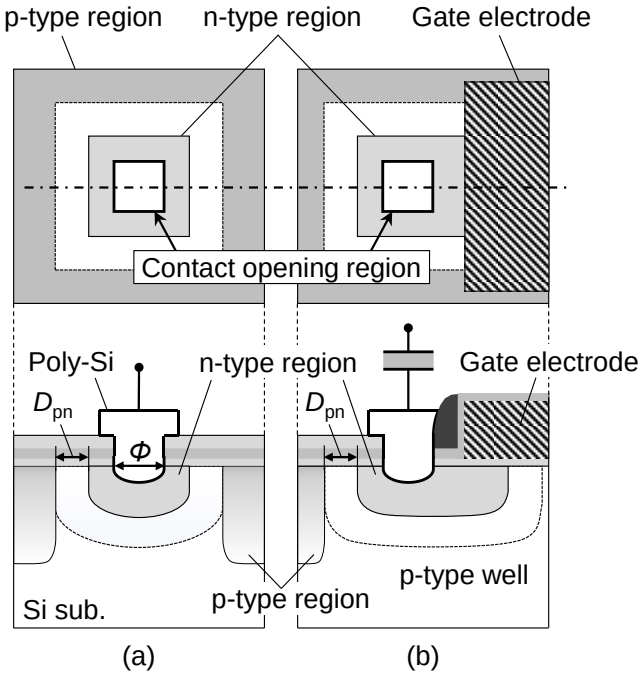



Figure 2.2 Layouts and cross-sectional views of test structures; (a) PTEG (Type-C) and (b) DTEG (Type-D).

Table 2.1 Detailed sample structures. The contact-hole diameter ($\Phi$) was varied in this study.

| Type | ID | $\Phi$ (nm) | Number of contact holes in each TEG | Number of measured samples |
|---|---|---|---|---|
| PTEG (Type-C) (Single device) | P0 | 70 | 504,000 Parallel connected | 36 |
| | P1 | 80 | | 36 |
| | P2 | 90 | | 36 |
| | P3 | 100 | | 36 |
| | P4 | 120 | | 36 |
| DTEG (Type-D) (CIS) | D1 | 80 | 1 at each pixel (Number of pixel array 3,000) | 1 |
| | D2 | 90 | | 1 |

### 2.1.3 Process flows

The sample preparation flowchart for two types of samples: Type-A and Type-B are shown in Fig. 2.3 and Table 2.2. The samples of Type-A (the left column in Fig. 2.3) were directly exposed to the ECR plasma source [(b1) in Fig. 2.3]. The ECR plasma was generated by a 2.45-GHz microwave and a bias power with a frequency of 400 kHz was applied to a wafer stage. The source power was 500 W and the chamber pressure was 3 Pa. The discharge gas was $CF_4/CHF_3/Ar/O_2$ = 30/90/60/5 sccm. The incident energy of the ions was controlled by changing the peak-to-peak voltage at the wafer stage, $V_{pp}$. In this case, a self-bias voltage ($V_{dc}$) can be estimated from $V_{pp}$. The exposure time was 30 s. The plasma conditions employed in this study are listed in Table 2.3 (Process A–F). Wet cleaning with sulfuric acid–hydrogen peroxide mixture (SPM) was conducted after PE to remove the residual $CF_x$ polymer on the surface. The sample structure after

processes A and E was analyzed using cross-sectional transmission electron microscopy (TEM) after removing the residual polymer. Spectroscopic ellipsometry (SE) was used to estimate the thicknesses of a surface oxidized layer (SL) and an interfacial transition layer (IL) for the samples treated by processes A–F. Time-of-flight secondary ion mass spectrometry (TOF−SIMS) was employed to evaluate impurity elements in the Si substrates for the samples after processes A, B, and E. The analysis area was 200 × 200 μm. In a positron annihilation spectroscopy (PAS) analysis, Doppler broadening spectra were measured as a function of the incident positron energy $E_{PAS}$. The central region of spectra was defined as 511 ± 0.76 keV. The monoenergetic positron beam line at the University of Tsukuba was used in the experiment.[4–6] The measurement was performed for the sample after process E, after the oxide-layer removal using a hydrofluoric (HF) acid solution. A sample was cleaned by an ammonium hydrogen-peroxide mixture (APM) served as the reference sample for the TOF−SIMS and PAS measurements. In this study, a 10 nm-thick oxide film was formed on the Si substrates using a high-temperature oxide (HTO) process[7] at 750 °C [(c) in Fig. 2.3] to suppress the surface recombination of carriers during cathodoluminescence (CL) measurement. In the CL measurements, an electron beam was irradiated on the sample using a scanning electron microscope and the spectrum was obtained using an InGaAs detector. The acceleration voltage of the electron beam was 10 and 25 kV and its maximum range was determined to be approximately 1.5 and 6.9 μm, respectively, based on the Kanaya–Okayama model.[8] All CL measurements were performed at 37 K to suppress thermal broadening. CL measurements were conducted for the samples with processes A–F. A sample cleaned by APM, followed by HTO film deposition on the Si surface, serving as the reference sample in the CL analysis.

The samples of Type-B (the right column in Fig. 2.3) were exposed to the ECR

plasma after an oxide film was formed on the Si substrates. A 50-nm oxide layer was formed on Si substrates [(a) in Fig. 2.3] by ISSG oxidation (10 nm), followed by CVD (40 nm). The oxide film was etched under the condition denoted by process E in Table 2.3 [(b2) in Fig. 2.3] or by HF solution [(b3) in Fig. 2.3]. The plasma-etched sample was subjected to sufficient over-etching after the removal of the oxide film. In (b2) in Fig. 2.3 using process E, the etching time was longer than (b1) because of the thicker oxide film thickness. Wet cleaning with SPM was conducted after PE to remove the residual polymer on the Si substrate surface. Ion implantation [(d) in Fig. 2.3] and furnace annealing (FA) [(e) in Fig. 2.3] were performed after these etching steps. Subsequently, 10 keV As ions were implanted in the Si substrates at an incident angle of 0° with a dose of $3.0 \times 10^{13}$ $cm^{-2}$. Subsequently, the implanted samples were thermally annealed at 850 °C for 10 min in ambient $N_2$ gas. SIMS analysis was performed after ion implantation and annealing for plasma- and wet-etched samples. The impurity (carbon, fluorine, oxygen, and arsenic) profiles were analyzed in the region from the Si surface to a depth of 250 nm. The PAS measurement was performed after PE and after annealing of plasma- and wet-etched samples.

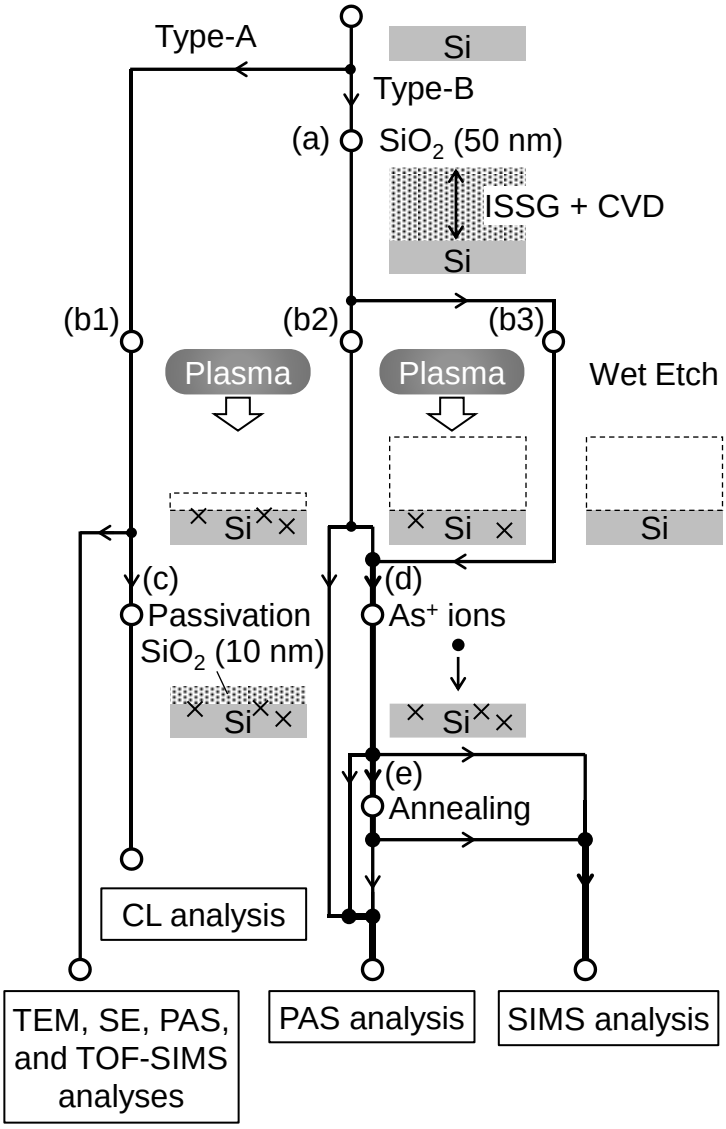



Figure 2.3 Sample preparation flowchart for two types of samples: Type-A and Type-B.

Table 2.2 Sample preparation procedure for Type-A and Type-B. The samples were processed and evaluated at the step labeled "●." Details of the plasma conditions denoted by A–F are shown in Table 2.3. A 10 nm-thick passivation film was formed on the Si substrate surface for CL measurements.

| | Type-A | | | | | | Type-B | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Sample ID | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| $SiO_2$ deposition | — | — | — | — | — | — | ● | ● | ● | ● | ● |
| Plasma etching | A | B | C | D | E | F | E | E | E | — | — |
| Wet etching | — | — | — | — | — | — | — | — | — | ● | ● |
| Ashing | ● | ● | ● | ● | ● | ● | ● | ● | ● | — | — |
| Wet cleaning | ● | ● | ● | ● | ● | ● | ● | ● | ● | — | — |
| As I/I | — | — | — | — | — | — | — | ● | ● | ● | ● |
| Annealing | — | — | — | — | — | — | — | — | ● | — | ● |
| Characterization | | | | | | | | | | | |
| TEM | ● | — | — | — | ● | — | — | — | — | — | — |
| SE | ● | ● | ● | ● | ● | ● | — | — | — | — | — |
| PAS | — | — | — | — | ● | — | ● | — | ● | — | ● |
| TOF–SIMS | ● | ● | — | — | ● | — | — | — | — | — | — |
| SIMS | — | — | — | — | — | — | — | ● | ● | ● | ● |
| CL | ● | ● | ● | ● | ● | ● | — | — | — | — | — |

Table 2.3 Plasma process conditions employed in this study. $V_{pp}$ is the peak-to-peak voltage. The chamber pressure is 3 Pa and the discharge gas is $CF_4/CHF_3/Ar/O_2$ = 30/90/60/5 sccm.

| Process | $V_{pp}$ (V) | Source/RF bias power (W) |
|---|---|---|
| A | 320 | 500/10 |
| B | 395 | 500/20 |
| C | 500 | 500/33 |
| D | 600 | 500/46 |
| E | 700 | 500/58 |
| F | 861 | 500/80 |

The sample preparation flowchart for the PTEG and DTEG is shown in Fig. 2.4. A 65-nm CMOS FET technology was employed to form p–n junctions on p-type (100) Si substrates with resistivities ranging from 11 to 14 Ω cm. The alignment accuracy in patterning contact holes connected to the n-type region was controlled within 5 nm. The detailed process conditions to form p–n junctions are explained in the sample preparation flowchart of p–n junction devices (PTEG) in Fig. 2.6. An oxide film (thickness: 60 nm) was etched with $CF_4/CHF_3/Ar/O_2$ plasma generated by microwave at 2.45 GHz. The PPD was created during PE of the contact holes on the Si substrate. The contact-opening process consisted of $SiO_2$ etching and Si over-etching. Defects were created in the lateral direction during contact etching, as well as the vertical direction. Moreover, $\Phi$ at the bottom of the contact hole and the Si recess depth ($d_R$) were measured using TEM.

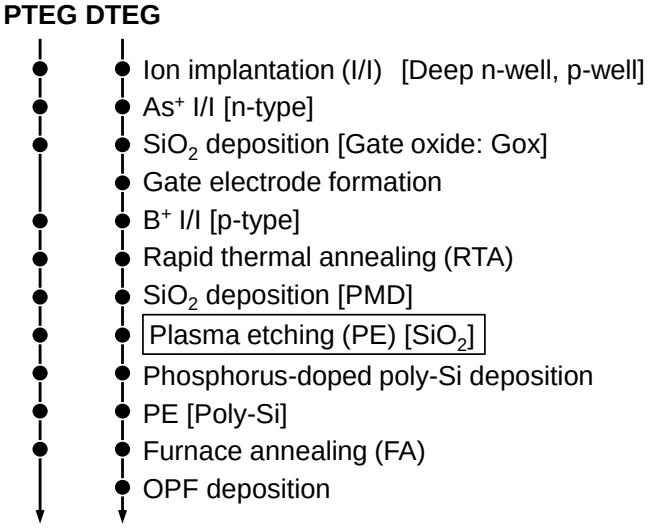



Figure 2.4 Sample preparation flowchart for PTEG (Type-C) and DTEG (Type-D).

A chemical dry etching (CDE)[9–11] process was performed after plasma exposure to examine the influence of residual species, such as O, C, and F in the damaged layer. Blanket wafers were used for physical and *C–V* analyses to evaluate the effects of plasma conditions and subsequent FA. PTEGs were used for *I–V* analyses to investigate PPD. A sample preparation flowchart of the blanket wafer to evaluate the influence of residual species in the damaged layer is shown in Fig. 2.5. The samples were made from p-type (100) Si substrates with resistivities ranging from 8 to 12 Ω cm. After wet etching (WE) with an APM, the samples were exposed to the ECR plasma generated by a 2.45-GHz microwave. A 400-kHz bias was applied to a wafer stage in a chamber under 3 Pa; the source and bias powers were 500 W and 58 W, respectively. The plasma discharge gas was a mixture of $CF_4/CHF_3/Ar/O_2$ (30/90/60/5 sccm) and the incident energy of the ions was controlled by changing $V_{pp}$ at the wafer stage; in this case, $V_{dc}$ can be estimated from $V_{pp}$ (= 700 V). The plasma exposure time was 30 s. A residual $CF_x$ polymer on the surface was stripped off by ashing and WE with an SPM and APM. CDE was performed on several samples after the residual polymer was removed. Detailed process conditions applied to each sample are listed in Table 4.1 of Chapter 4. The conditions of three CDE processes to evaluate the influence of residual species on PID: low-temperature CDE (LT), high-temperature CDE with $O_2$ addition (HT1), and without $O_2$ (HT2) are listed in Table 2.4. The CDE plasma was generated by the 2.45-GHz microwave and $CF_4/O_2$ discharge gas was used for the LT and HT1 samples, whereas $CF_4$ was used for the HT2 samples. A 10-nm thick surface layer on the Si substrates was etched by each CDE process; the RF power was 400 W and the pressure was 30 Pa. Furnace annealing (FA) at 850 °C for 10 min in $N_2$ was performed for several samples after WE with SPM and APM.

The damaged layers after PE and HT2 CDE were analyzed using TEM. SE was

used to estimate the thicknesses of surface-oxidized and interfacial transition layers: $d_{SL}$ and $d_{IL}$, respectively. The SE system uses a Xe-lamp (210–1690 nm) as a light source; the diameter of the beam spot was 125 μm and the incident angles were 65°, 70°, and 75°. The impurities detected by TOF–SIMS were those that remained in the damaged Si substrates after the completion of the process indicated in Table 4.1; the inspected area was 200 × 200 μm. An Hg probe system was used to measure the *C–V* characteristics. All samples (IDs 1–9 in Table 4.1 of Chapter 4) were analyzed using TOF–SIMS and *C–V* measurements, with sample ID 1 acting as a reference.

For CL analysis, a 10-nm thick HTO film was formed on the Si substrates at 750 °C to suppress the surface recombination of carriers. The samples were irradiated with an electron beam using a scanning electron microscope and the CL spectrum was obtained using an InGaAs detector. The acceleration voltage of the electron beam was either 10 or 25 kV and based on the Kanaya-Okayama model,[8] the corresponding maximum electron generation was approximately 1.5 or 6.9 μm, respectively. CL measurements were performed for sample IDs 1–3, 5, and 9. All CL measurements were performed at 37 K to suppress thermal broadening. An APM-cleaned Si sample with a deposited HTO film acted as the reference.

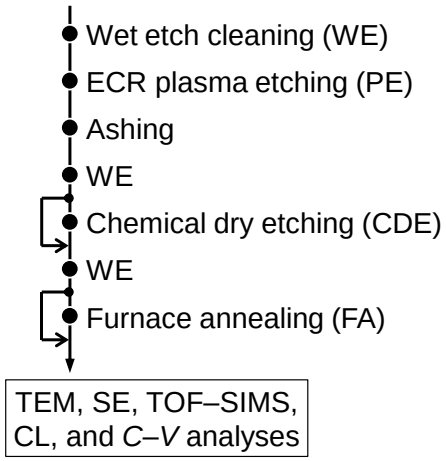



Figure 2.5 Blanket wafer sample preparation flowchart to evaluate the influence of residual species on a damaged layer.

Table 2.4 Chemical dry etching (CDE) processing conditions.

| CDE | Temperature (°C) | Microwave power (W) | $CF_4$ (sccm) | $O_2$ (sccm) |
|---|---|---|---|---|
| LT | 25 | 400 | 180 | 420 |
| HT1 | 100 | 400 | 180 | 420 |
| HT2 | 100 | 400 | 100 | — |

A sample preparation flowchart of PTEG is shown in Fig. 2.6. The n-type well region ("deep n-well") was formed by ion implantation with 500-keV P ions up to a dosage of $5.0 \times 10^{12}$ $cm^{-2}$. The p-type well ("p-well") was formed by ion implantation

with 100-keV B ions up to a dosage of $4.0 \times 10^{12}$ $cm^{-2}$. The n-type region ("n-type") was formed by ion implantation with 100-keV As ions up to a dosage of $1.0 \times 10^{12}$ $cm^{-2}$. The p-type region ("p-type") was formed by ion implantation with 50-keV B ions up to a dosage of $3.0 \times 10^{12}$ $cm^{-2}$ and 10-keV B ions up to a dosage of $1.2 \times 10^{13}$ $cm^{-2}$. An oxide film of approximately 10 nm thick was formed on Si substrates using an ISSG oxidation process. The implanted samples were thermally annealed at 1050 °C using a spike rapid thermal annealing (RTA) system and an oxide layer was subsequently formed on the Si substrate by CVD (~50 nm), resulting in a total surface thickness of 60 nm. The samples with a photoresist mask were exposed to the ECR plasma; the etching time was adjusted to remove the oxide film and form a contact hole. Si over-etching was performed to create a Si recess structure once a contact hole was formed. A residual $CF_x$ polymer on the surface and within the contact hole was stripped off by subsequent ashing and WE with SPM and APM. After removing the residual polymer, HT1 and HT2 CDE (18 s) were conducted for samples II and III (in Table 4.2 of Chapter 4), respectively. The LT CDE was excluded from the Type-C sample group because it is expected to significantly increase the depth of the Si recess structure owing to large amount of oxidation, which can be attributed to the longer $CF_4/O_2$ process time. Diluted HF (DHF) was used to remove the native oxide layer on the Si surface before the poly-Si film doped with $7.0 \times 10^{20}$ $cm^{-3}$ Phosphorus (P) was deposited; the poly-Si film was used as the electrode connected to the n-type. After the poly-Si film was etched to form probing pads, FA was performed to recover the damaged structures in the Si substrate and to decrease the contact resistance caused by P diffusion into the Si substrate. The interfaces at the bottom of contact holes in samples were analyzed using TEM. A list of figures and tables corresponding to the structures and process flows of each sample is shown in Table 2.5.

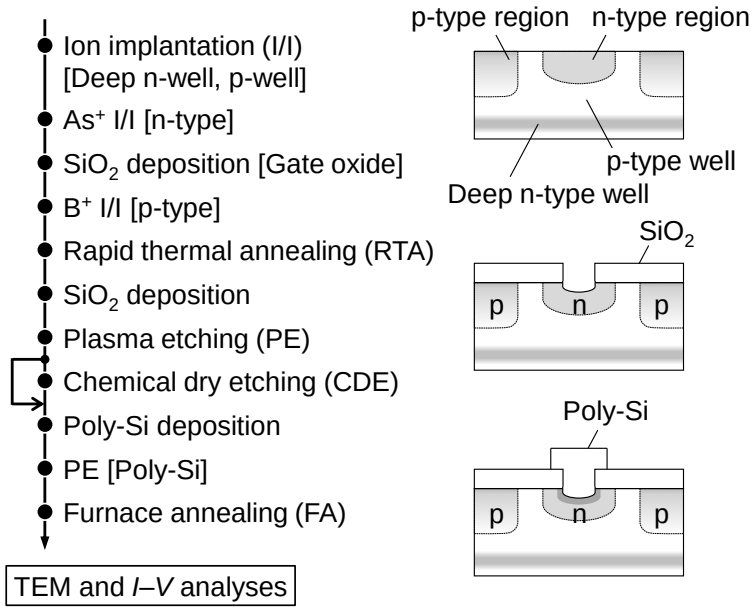



Figure 2.6 Sample preparation flowchart for PTEG. A CDE process was performed after plasma exposure to evaluate the influence of residual species, such as O, C, and F on the damaged layer.

Table 2.5 List of figures and tables corresponding to the structures and process flow of each sample.

| | **Type-A** | **Type-B** | **Type-C (PTEG)** | **Type-D (DTEG)** |
|---|---|---|---|---|
| Sample structure | Blanket wafer | | Device with p–n junction | |
| Layout | — | — | Fig. 2.2(a) | Fig. 2.2(b) |
| Process flow (w/o CDE) | Fig. 2.3 | Fig. 2.3 | Fig. 2.4 | Fig. 2.4 |
| Process condition (w/o CDE) | Table 2.2 | Table 2.2 | Table 2.1 | Table 2.1 |
| Process flow (w/ CDE) | Fig. 2.5 | — | Fig. 2.6 | — |
| Process condition (w/ CDE) | Table 4.1 (Chapter 4) | — | Table 4.2 (Chapter 4) | — |

### 2.1.4 Plasma process equipment

This study used a commercially available ECR plasma system (Hitachi High-Tech Corp., U-8150) for 12-inch (300 mm) Si wafers. A rotational motion of ions proceeding with the cyclotron frequency is proceeded by a magnetic field. When the input microwave frequency matches the electron cyclotron frequency, electrons accelerate owing to resonance. The increased probability of collisions by accelerated electrons enables the generation of high-density plasma (~$10^{11}$ $cm^{-3}$) at low pressure (0.05~0.5 Pa). A schematic of the ECR plasma system used in this study is shown in Fig. 2.7. The ECR plasma was generated by a 2.45-GHz microwave and a bias power with a frequency of 400 kHz was applied to the wafer stage. The source power was 500 W and the chamber pressure was 3 Pa. The discharge gas was $CF_4/CHF_3/Ar/O_2$ = 30/90/60/5 sccm. The incident energy of the ions was controlled by changing the peak-to-peak voltage at the wafer stage, $V_{pp}$.

Some samples in this study were performed in the CDE process after plasma exposure to investigate the influence of residual species, such as O, C, and F in a damaged layer. CDE is widely used for poly-Si etching and photoresist ashing processes. Generally, the CDE process is isotropic and exhibits high selectivity. The schematic of the CDE apparatus (Shibaura Mechatronics Corp., CDE300) used in this study is shown in Fig. 2.8. The CDE apparatus comprised two main chambers-discharge and reaction. The CDE plasma was generated by a 2.45-GHz microwave and two types of discharge gas: $CF_4/O_2$ and $CF_4$ were used in this study. The plasma generated in the discharge chamber propagates to the reaction chamber by diffusion through a transfer tube. Charged particles recombine at the tube wall and disappear resulting in only radicals, such as F, O, and $CF_x$ reaching the reaction chamber. Because the neutral radicals attack the wafer from all

angles, this process is isotropic. The influence of CDE on the damaged layer is examined in Chapter 4.

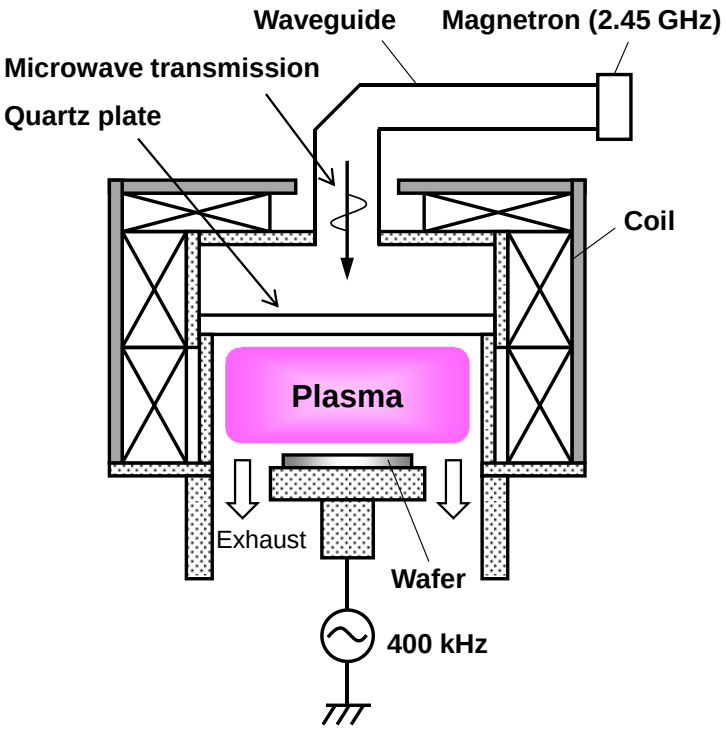



Figure 2.7 Schematic of an ECR plasma system used in this study.

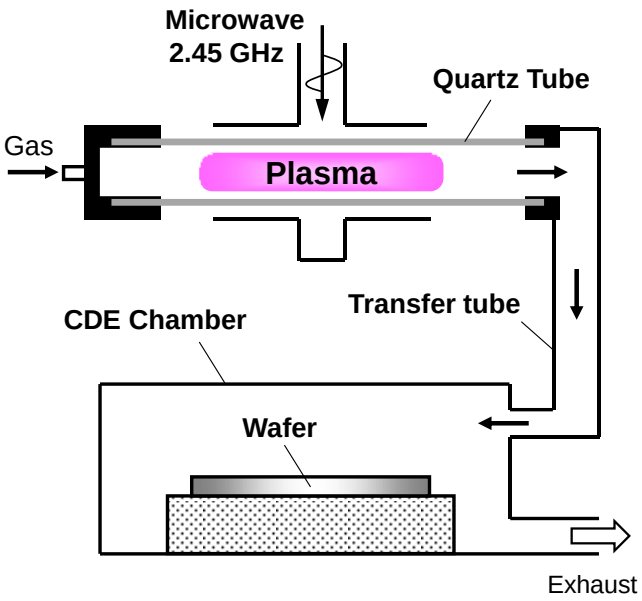



Figure 2.8 Schematic of a CDE apparatus used in this study.

## 2.2 Physical analyses

Various defect analysis techniques were employed to examine the behavior of defects induced by plasma exposure. In addition to TEM and SE analyses, SIMS, TOF−SIMS, PAS, and CL methods were applied to assess defects in low-density regions. In this study, the aforementioned PPD characterization methods are denoted as physical analyses.

### 2.2.1 Transmission electron microscopy

In TEM analysis, a high-energy electron beam is irradiated to a very thin sample (< 200 nm thick). Interaction between electrons and atoms can be used to observe the crystal structure and morphology at an atomic level. A schematic of a TEM apparatus and

an example image of TEM observation is shown in Fig. 2.9. Electrons are emitted from the electron gun at the top of the TEM apparatus. A magnetic condensing lens is used to condense the electrons. The emitted electrons are highly focused by the electromagnetic lens in a vacuum and irradiated to a thin sample.

TEM provides information on the crystal structure. Although the amorphous layer and end-of-range defects can be observed using TEM, the assignment of point defects, such as vacancies and interstitial impurities is challenging. In this study, the "detection limit" is defined as the minimum number of defects that can be detected by the respective analysis techniques. The detection limit for defects in a Si substrate using TEM observation is approximately $5 \times 10^{20}$ $cm^{-3}$.

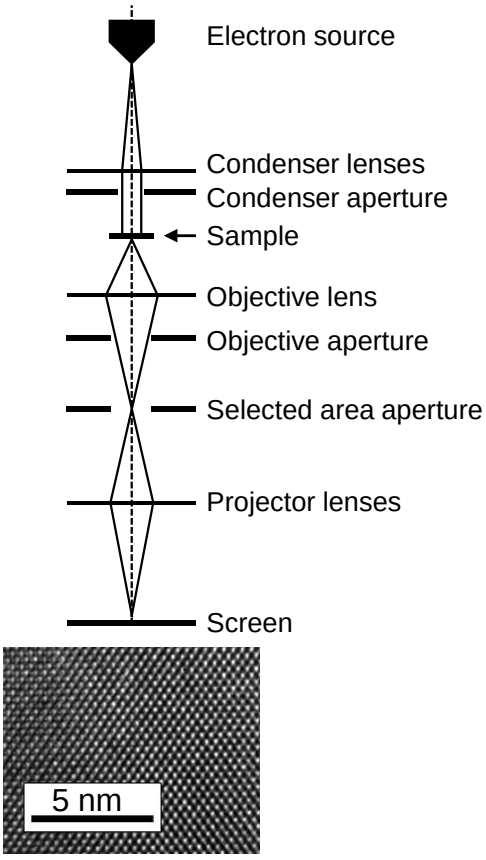



Figure 2.9 Schematic of TEM.

### 2.2.2 Spectroscopic ellipsometry

The thickness of a damaged layer after PE was evaluated by SE. Generally, SE is a non-destructive measurement technique to obtain the optical properties of thin film and bulk materials through reflected light waves. SE uses polarized light at an oblique incidence to a sample surface, as shown in Fig. 2.10. The measured data is expressed using two parameters: Psi ($\Psi$) and Delta ($\Delta$). $\Psi$ and $\Delta$ describe the change in polarization that occurs when the incident light interacts with the sample surface. Polarization changes originate from the reflectivity difference between electric field components oriented parallel (*p* polarization) and perpendicular (*s* polarization) to the plane of incidence. A schematic of the experimental setup of an SE system used in this study (J. A. Woollam Co., Inc., M-2000FI) is shown in Fig. 2.11 The SE system uses an Xe-lamp with a wavelength range of 210–1690 nm as a light source. The beam spot diameter was 125 μm. SE spectra were obtained at incident angles of 65°, 70°, and 75°. The measurements in this study were performed in the 200–900 nm (1.38–6.2 eV) spectral range.

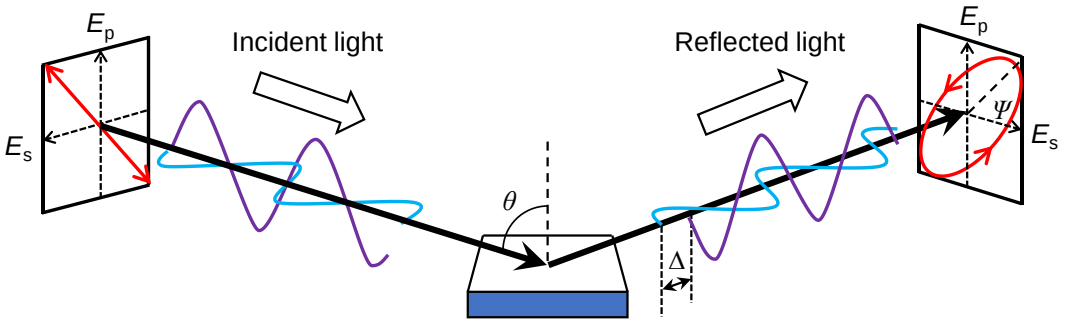



Figure 2.10 Measurement principle of SE.

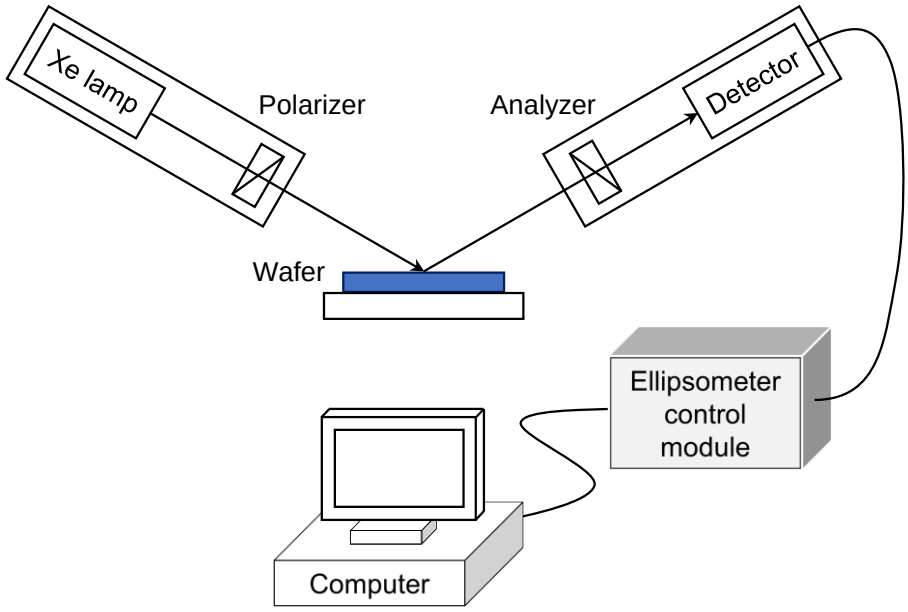



Figure 2.11 Schematic of the experimental setup of SE.

The damaged layer formed by plasma processes primarily comprises two regions: the surface oxidized layer (SL) and the interfacial transition layer (IL) with displaced Si and interstitial atoms.[12] SE was used to estimate the thicknesses of the SL and IL for samples after plasma processes. The thicknesses of IL and SL were defined as $d_{IL}$ and $d_{SL}$, respectively. In this study, two optical models assuming transition layers composed of amorphous Si and crystalline Si (Model X) or amorphous Si and $SiO_2$ phase (Model Y) were employed for comparison, as shown in Fig. 2.12. The surface layer was assumed to be thin $SiO_2$. The effective optical constants of the IL layer were estimated using the Bruggeman effective medium approximation.[13,14] The effective optical constant $\varepsilon$ in the Bruggeman model is expressed as:

$$f_{Si}\frac{\varepsilon_{Si}-\varepsilon}{\varepsilon_{Si}+2\varepsilon}+\left(1-f_{Si}\right)\frac{\varepsilon_{a}-\varepsilon}{\varepsilon_{a}+2\varepsilon}=0, \quad (2.1)$$

where $\varepsilon_a$ is the dielectric constant of the amorphous Si for Model X and $SiO_2$ for Model

Y, $f_{Si}$ and $\varepsilon_{Si}$ are the volume function and dielectric constant of Si, respectively. Three parameters, $d_{SL}$, $d_{IL}$, and $f_{Si}$, were determined using Model X and Model Y.

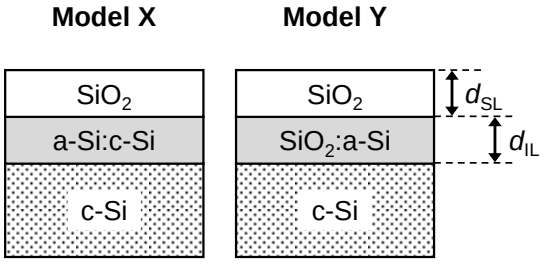



Figure 2.12 Optical models employed for SE analysis.

### 2.2.3 Secondary ion mass spectrometry

SIMS is a surface analytical technique for solid materials. In SIMS analysis, a few atomic layers from the surface of a sample are sputtered using a focused primary ion beam, such as $Ar^+$, $O^-$, $O_2^+$, $Cs^+$, and $Ga^+$ at 1–30 keV. For example, an oxygen ion is used to analyze positive secondary ions, whereas a cesium ion is used to analyze negative secondary ions. When a solid sample is sputtered by primary ions, neutrals and secondary ions are ejected from the surface of the sample. The secondary ions ejected from the sample provide information about the elemental and molecular composition of the material. Continuous analysis during sputtering produces information along the depth direction as the sample is gradually sputtered by ion irradiation. SIMS is a sensitive technique for surface analysis. The detection limit of SIMS is between $10^{12}$ and $10^{16}$ atoms/cm$^3$.[15] Several types of mass analyzers exist, including magnetic sector, TOF, and quadrupole. In general, TOF analyzers are suitable for static SIMS, whereas quadrupole and magnetic sector analyzers are suitable for dynamic SIMS. TOF–SIMS is a technique

of irradiating an ion beam on a solid sample and separating the mass by utilizing the difference in the TOF of the ions emitted from the surface. TOF–SIMS can obtain information on elements or molecular species present within a depth of 1 nm from the sample surface at high sensitivity. In this study, SIMS analyses were performed using a SIMS4500 (CAMECA). $Cs^+$ was used as a primary ion beam. The energy of primary ions was 1 keV and the tilt angle was 50° from the normal. TOF–SIMS analyses were performed using a TOF.SIMS5 (ION–TOF). $Bi_3^+$ with 15 keV was used as a primary ion beam source and $Cs^+$ with 1 keV was used as a sputtering ion beam source.

### 2.2.4 Cathodoluminescence

The CL method is based on the phenomenon of light emission from materials owing to electron irradiation.[16] A high-energy electron beam excites electrons from the valence band into the conduction band of a material. A photon is emitted from a sample when the electron and hole recombine. The light emitted from the sample is introduced to a spectroscope through a collector mirror. In the case of crystalline Si substrates, the CL spectrum identifies typical defect structures, such as dislocation-related luminescence (D lines) and interstitial carbon and oxygen complex ($C_iO_i$)-related luminescence lines (C lines). The transverse optical (TO) line at 1.09 eV denotes the TO-phonon of the band-to-band transition.[17] In general, the CL emission is suppressed by the presence of defects because defects near the Si surface cause surface recombination of excited carriers. A schematic of the CL emission process is shown in Fig. 2.13. The number of defects can be approximated from the TO-line intensity.[18] The measurement region of CL is determined by the penetration depth of the electron beam and diffusion of generated electron–hole pairs. The depth profile of defects is obtained by changing the electron

beam energy that defines the projection range of incident electrons. The maximum range $R_e$ is a function of beam energy $E_b$ (keV):[8]

$$R_e = (0.0276A / \rho Z^{0.889}) E_b^{1.67} \text{ (μm)}, \quad (2.2)$$

where $A$ is the atomic weight, $\rho$ is the density of the material (g/cm$^3$), and $Z$ is the atomic number. The detection limit of the CL analysis is considered to range from $10^{14}$ cm$^{-3}$.[16]

This study uses CL analysis to detect defects in damaged Si substrates. An SEM (Hitachi, S-4300SE) with a Schottky emission-type gun was used as the excitation source. The emitted luminescence was analyzed using a single monochromator equipped with an InGaAs multichannel detector (Jobin Yvon, HR-320) covering the photon energy ranging from 0.77 to 1.38 eV. All CL measurements were performed at 37 K. The acceleration voltage of the electron beam was 10 or 25 kV. The electron penetration depth in Si substrates was estimated using the Kanaya–Okayama model[8] to be approximately 1.5 μm at 10 kV and 6.9 μm at 25 kV.

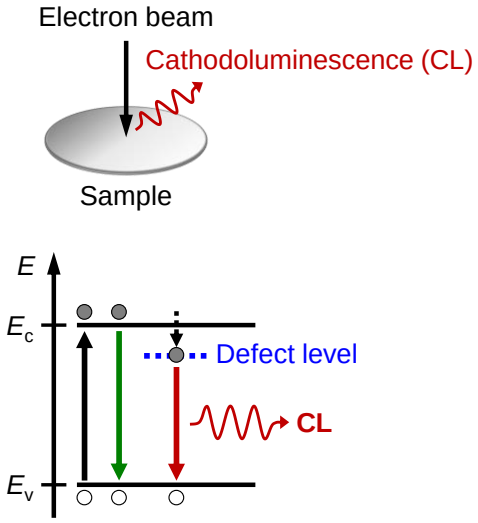



Figure 2.13 Schematic of the CL emission process.

### 2.2.5 Positron annihilation spectroscopy

PAS analysis detects low-density defects with high sensitivity by assuming that positrons are selectively trapped in vacancy-type defects, where positive ions are lost. Positron has an electric charge of +*e* and a spin of 1/2 (same as electrons) and has the same mass as an electron. The schematic of positron annihilation is shown in Fig. 2.14. Positrons can be generated through the beta ($\beta^+$)-decay of radioactive isotopes. In this study, the radioactive isotope $^{22}$Na was used as a positron source. Annihilation (electron–positron) radiation occurs when a positron collides with an electron in a sample. The mass of the electron–positron pair is converted into energy and in most cases, two γ-ray photons are emitted in opposite directions. The amount of energy ($E_\gamma$) produced by the annihilation equals the mass that disappears multiplied by the square of the speed of light in a vacuum [that is, $E = m_0c^2 = 511$ keV, where $m_0$ is the electron (positron) rest mass and $c$ (m/s) is the speed of light]. The motion of the electron–positron pair causes a Doppler shift in the energy of the annihilation radiation.[19] Generally, vacancy-type defects can be detected by measuring the Doppler broadening spectra of the annihilation radiation.[6] The change in the Doppler broadening spectrum is characterized by the *S* (Shape) parameter.[19] The *S* parameter is a ratio of counts in a defined bandwidth of a spectrum near the peak to the total counts of the spectrum. Positron annihilation at (a) defect-free state and (b) trapped state by an open-volume defect is shown in Fig. 2.15.[20] The *S* value increases with the size of agglomerated vacancies (defect structure and/or density).

The relationship between the *S* parameter and incident positron energy $E_{PAS}$ can be analyzed using a variable energy positron fit (VEPFIT) program developed by van Veen *et al*.[21] The time-independent one-dimensional positron diffusion can be expressed as[22]

$$D_+ \frac{d^2}{dz^2} n(\mathrm{z}) \; - \; \kappa_{\mathrm{eff}} n(z) + P(z, E) = 0, \tag{2.3}$$

where $n(z)$ is the positron density at a distance $z$ from the surface, $D_+$ is the positron diffusion constant, $\kappa_{\mathrm{eff}}$ is the effective decay rate of positrons, and $P(z, E)$ is the positron implantation profile as a function of the incident energy. The positron diffusion length $L_{\mathrm{d}}$ is expressed as:

$$L_{\mathrm{d}} = \sqrt{\frac{D_+}{\kappa_{\mathrm{eff}}}} \; . \tag{2.4}$$

$P(z, E)$ is expressed as[23]

$$P(z, E) = \frac{m z^{m-1}}{z_0^m} \exp\left[-\left(\frac{z}{z_0}\right)^m\right] \text{ with } z_0 = \frac{AE^r}{\rho \Gamma\left(1 + \frac{1}{m}\right)} \quad , \tag{2.5}$$

where $m$, $r$, and $A$ are empirical parameters, $\rho$ is the mass density of the sample and $\Gamma(x)$ ($x = 1 + 1/m$) is the gamma function. The obtained $S$–$E$ curve is fitted using

$$S(E) = S_{\mathrm{s}} F_{\mathrm{s}}(E) + \sum S_{\mathrm{i}} F_{\mathrm{i}}(E), \tag{2.6}$$

$$F_{\mathrm{s}}(E) + \sum F_{\mathrm{i}}(E) = 1, \tag{2.7}$$

where $F_{\mathrm{s}}(E)$ and $F_{\mathrm{i}}(E)$ are the fractions of thermalized positrons annihilated at the surface and in the $i$-th block of the bulk, respectively. $S_{\mathrm{s}}$ and $S_{\mathrm{i}}$ are the $S$ parameters for the annihilation of positrons at the surface and in the $i$-th block of the bulk, respectively. The VEPFIT program solves Eq. (2.3) and provides the fraction of positrons annihilated in each block as well as the corresponding $S$ parameter. Generally, the detection limit of the PAS analysis is considered to range from $10^{16}$ cm$^{-3}$ in crystalline Si[20], as shown in Fig. 2.16.

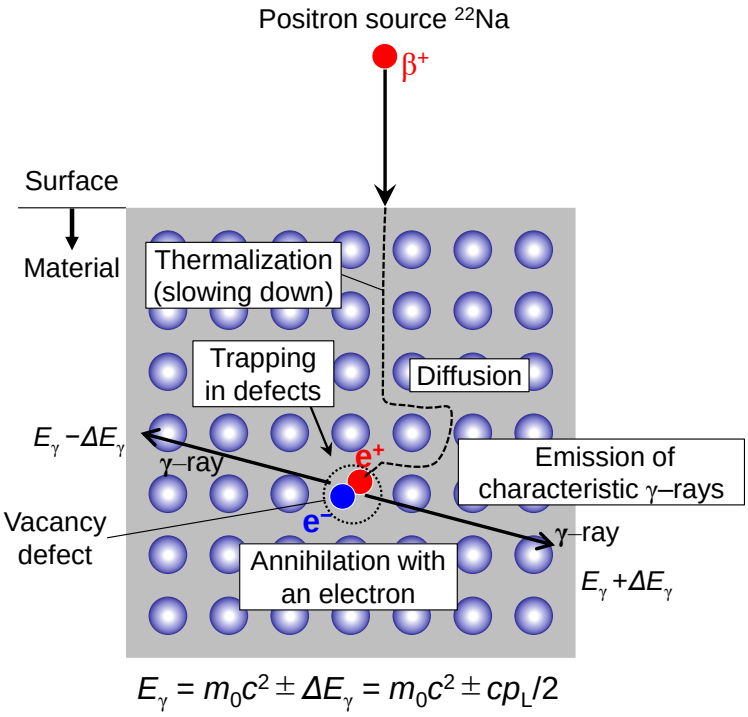



Figure 2.14 Schematic of positron annihilation.

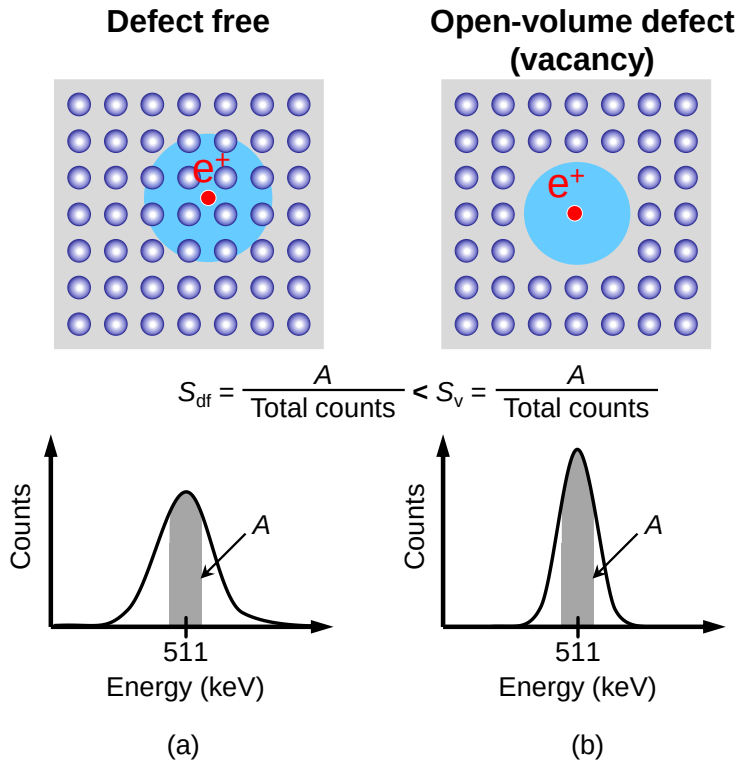



Figure 2.15 Positron annihilation in (a) the defect-free state and (b) the trapped state by an open-volume defect.

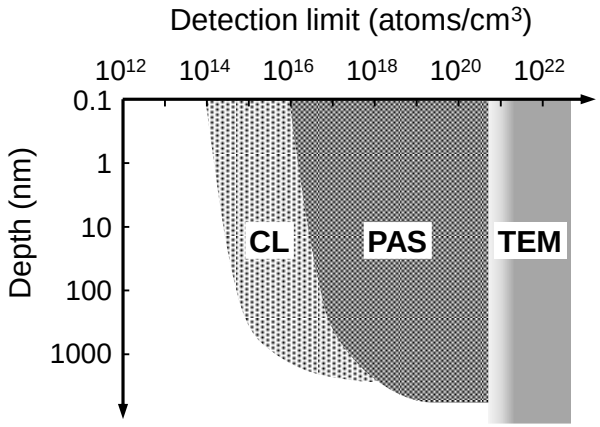



Figure 2.16 Defect characterization techniques with respect to the detection limit.

## 2.3 Electrical analyses

*C–V* and *I–V* measurements were conducted to understand the nature of PPD mechanisms. A schematic of the *C–V* measurement setup for blanket wafer samples is shown in Fig 2.17. The system is equipped with a precision semiconductor parameter analyzer (Hewlett-Packard, 4156A) and a precision LCR meter (Agilent, 4284A). *C–V* measurements of blanket wafer samples were performed at room temperature using a mercury (Hg) probe platform in a shield box (Solid State Measurement, Inc., SSM 495 CV SYSTEM). A 100-kHz modulation voltage was superimposed upon a DC bias voltage. The amplitude was 10 mV. The area of the Hg metal contact was $7 \times 10^{-3}$ $cm^2$.

A schematic of a *C–V* and *I–V* automatic test equipment system for 300-mm-diameter wafer samples (Tester: Keysight, 4082F, Prober: Tokyo Seimitsu, UF3000EX-e) is shown in Fig. 2.18 The test system was equipped with a built-in semiconductor pulse generator unit and an LCR meter. The system is equipped with eight source monitor units (SMUs). The SMU comprises two low-current and six standard-current ports. The measurement ranges for the low- and standard-current ports are 1 fA to 100 mA (2 μV to 100 V) and 10 fA to 1 A (2 μV to 200 V), respectively. *I–V* measurements of the device structure samples were performed at 25, 40, 60, 80, and 100 °C.

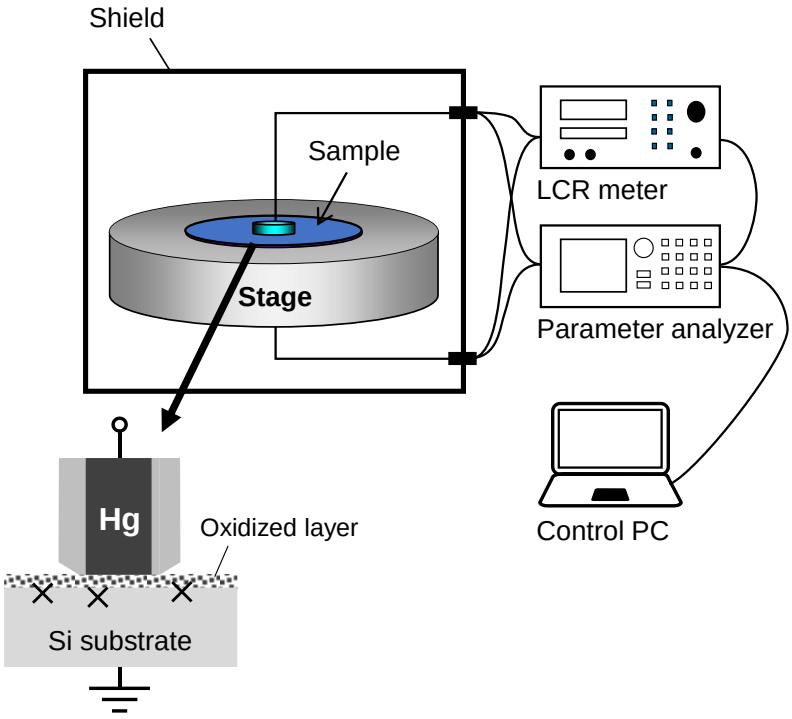



Figure 2.17 Schematic of the *C*–*V* measurement setup for blanket wafer samples.

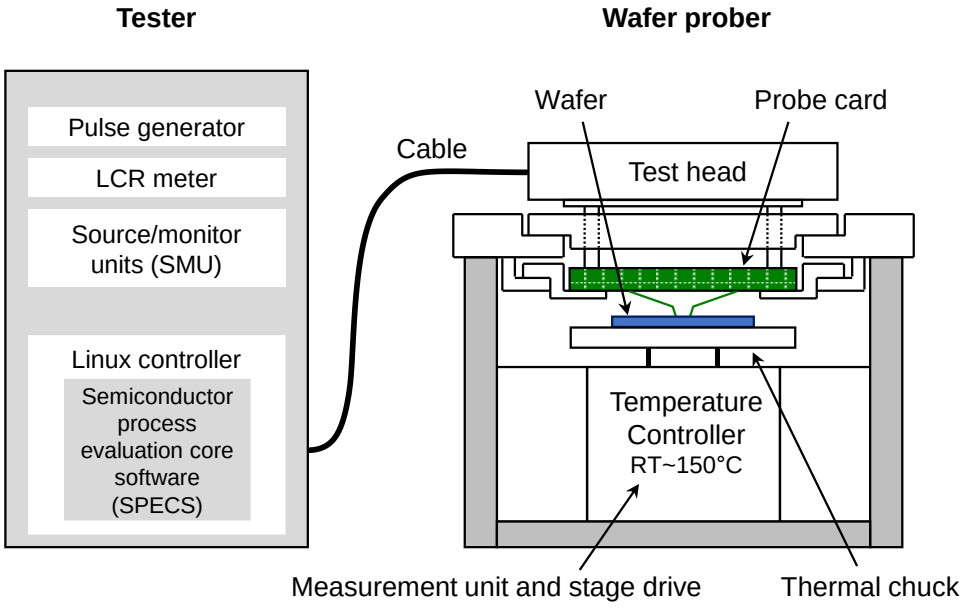



Figure 2.18 Wafer test system.

## 2.4 Modeling of electrical properties

### 2.4.1 Capacitance–voltage characteristics

The $1/C^2$–$V$ techniques have been widely utilized to quantify the doping concentration in Si substrates in the design of ion implantation processes.[24] For a one-sided abrupt junction, $1/C^2$ and the differential capacitance can be described as follows:

$$\frac{1}{C_p{}^2} = \frac{2(V_{bi} - V)}{q\varepsilon_0\varepsilon_{Si}N_B}, \tag{2.8}$$

$$\frac{d}{dV}\left(\frac{1}{C_p{}^2}\right) = \frac{-2}{q\varepsilon_0\varepsilon_{Si}N_B}, \tag{2.9}$$

where $C_p$ is the measured parallel capacitance, $V_{bi}$ is the built-in voltage, $V$ is the applied bias voltage, $\varepsilon_{Si}$ is the relative dielectric constant of the Si substrate, $\varepsilon_0$ is the permittivity of the vacuum, and $N_B$ is the doping concentration of the substrate. The slope provides the impurity concentration of the substrate $N_B$ and the intercept (at $1/C^2 = 0$) provides $V_{bi}$, as shown in Fig. 2.19.

The damaged structures after plasma exposure can be evaluated by the distortion of the $C$–$V$ curve and the flat-band voltage ($V_{FB}$) shift. The differential capacitance on the depletion/inversion side is severely influenced by the presence of defects. By introducing the volumetric density of defects $n_{dam}$, the differential capacitance with a damaged layer can be expressed as[25]

$$\left|\frac{d}{dV}\left(\frac{1}{C_p{}^2}\right)\right| = \frac{2}{q\varepsilon_0\varepsilon_{Si}(N_B + n_{dam})}. \tag{2.10}$$

The slope of $1/C_p{}^2$–$V$ defines $N_B + n_{dam}$. Changes in the slope correspond to the presence of defect sites. $n_{dam}$ can be quantified in Si substrates created by PPD using this methodology.

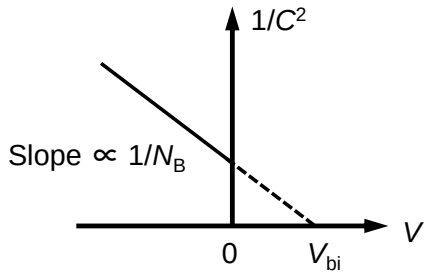



Figure 2.19 Plot of $1/C^2$ versus $V$.

### 2.4.2 Current-voltage characteristics

*I–V* measurements were performed using Schottky contact structures,[26–30] p–n junctions,[31,32] and MOS structures.[33,34] This study employs a device with a p–n junction for the PPD evaluation. The energy band diagrams of a p–n junction under forward and reverse bias conditions are shown in Figs. 2.20(a) and 2.20(b), respectively. The total current through the p–n junction is expressed as[24]

$$J = J_{\mathrm{p}} + J_{\mathrm{n}} = J_0 \left[\exp\left(\frac{qV}{kT}\right) - 1\right], \tag{2.11}$$

$$J_0 \equiv \frac{qD_{\mathrm{p}}n_{\mathrm{i}}^2}{L_{\mathrm{p}}N_{\mathrm{D}}} + \frac{qD_{\mathrm{n}}n_{\mathrm{i}}^2}{L_{\mathrm{n}}N_{\mathrm{A}}} = qn_{\mathrm{i}}^2\left(\frac{1}{N_{\mathrm{D}}}\sqrt{\frac{D_{\mathrm{p}}}{\tau_{\mathrm{p}}}} + \frac{1}{N_{\mathrm{A}}}\sqrt{\frac{D_{\mathrm{n}}}{\tau_{\mathrm{n}}}}\right), \tag{2.12}$$

where $J_{\mathrm{p}}$ is the hole diffusion current density in the n-type region, $J_{\mathrm{n}}$ is the electron diffusion current density in the p-type region, $J_0$ is the saturation current density, $q$ is the elementary charge, $V$ is positive for forward bias and negative for reverse bias and $k$ is the Boltzmann constant. $T$ is the absolute temperature in degrees Kelvin, $D_{\mathrm{p}}$ is the hole diffusion coefficient, $D_{\mathrm{n}}$ is the electron diffusion coefficient, $n_{\mathrm{i}}$ is the intrinsic carrier density, $L_{\mathrm{p}}$ is the diffusion length of holes, $L_{\mathrm{n}}$ is the diffusion length of electrons, $N_{\mathrm{D}}$ is the donor concentration, $N_{\mathrm{A}}$ is the acceptor concentration, $\tau_{\mathrm{p}}$ is the hole lifetime, and $\tau_{\mathrm{n}}$ is the electron lifetime.

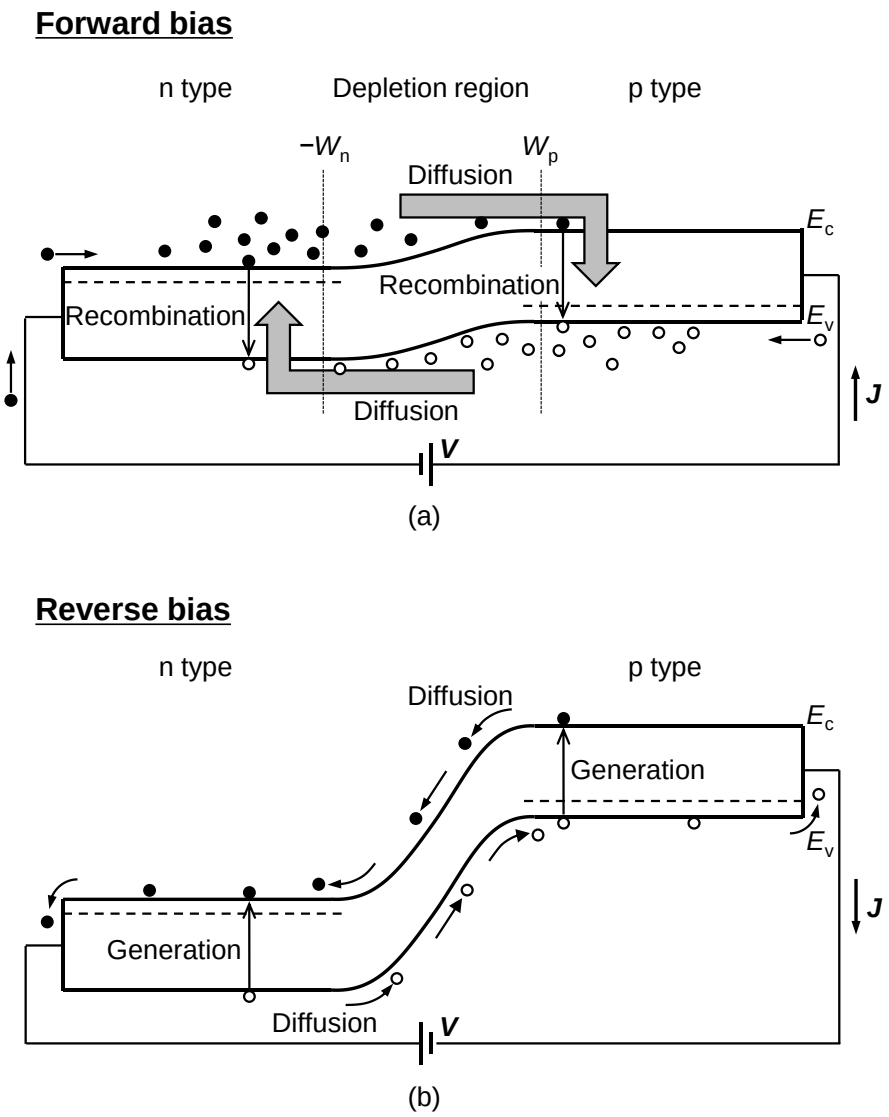



Figure 2.20 Energy band diagrams of a p–n junction under (a) forward bias and (b) reverse bias conditions.

Carrier generation and recombination processes are shown in Fig. 2.21. $E_c$ is the bottom edge of the conduction band, $E_v$ is the top edge of the valence band, and $E_g$ is the energy gap of Si.[35] Carrier generation is a process in which electron-hole pairs are

generated by exciting an electron from the valence to the conduction band. Recombination is a process in which electrons and holes from the conduction and valence bands, respectively, recombine and are annihilated. Recombination can be classified into two groups, radiative (band-to-band) and non-radiative recombination. Non-radiative recombination can be categorized into trap-assisted recombination by defects (Shockley–Read–Hall recombination) or auger recombination. In Si (indirect-bandgap semiconductors), the dominant transitions are indirect generation/recombination via intermediate levels. Based on the Shockley–Read–Hall theory,[24,36] the recombination rate is expressed as

$$U = \frac{\sigma_n \sigma_p v_{th} n_t (pn - n_i^2)}{\sigma_n \left[ n + n_i \exp\left(\frac{E_t - E_i}{kT}\right) \right] + \sigma_p \left[ p + n_i \exp\left(-\frac{E_t - E_i}{kT}\right) \right]}, \quad (2.13)$$

where $\sigma_n$ is the capture cross-section of electrons, $\sigma_p$ is the capture cross-section of holes, $v_{th}$ is the thermal velocity of carriers, $n_t$ is the concentration of the recombination centers (the density of traps) in the Si substrate, and $n$ is the electron density. $p$ is the hole density, $E_t$ is the energy level of the recombination center (trap level), and $E_i$ is the intrinsic Fermi level. Under reverse bias voltage conditions, the carrier concentration ($n$, $p$) in the depletion region is considerably smaller than the intrinsic carrier concentration ($n_i$); hence, $n << n_i$ and $p << n_i$. When $n << n_i$ and $p << n_i$, the rate of electron–hole pair generation is expressed as follows:

$$G = -U = \left[ \frac{\sigma_n \sigma_p v_{th} n_t}{\sigma_n \exp\left(\frac{E_t - E_i}{kT}\right) + \sigma_p \exp\left(-\frac{E_t - E_i}{kT}\right)} \right] n_i \equiv \frac{n_i}{\tau_g}, \quad (2.14)$$

where $\tau_g$ is the generation lifetime. Assuming $\sigma_n = \sigma_p = \sigma_0$,[37,38] Eq. (2.14) yields

$$G = \frac{n_i \sigma_0 v_{th} n_t}{2\cosh\left(\frac{E_t - E_i}{kT}\right)}. \quad (2.15)$$

The generation current density (SRH generation current density, $J_{SRH}$) in the depletion region is expressed as[24]

$$J_{\mathrm{SRH}} = \int_0^{W_{\mathrm{dep}}} qGdx \approx qGW_{\mathrm{dep}} = \frac{qn_{\mathrm{i}}W_{\mathrm{dep}}}{\tau_{\mathrm{g}}} = \frac{qn_{\mathrm{i}}\sigma_0 v_{\mathrm{th}}W_{\mathrm{dep}}n_{\mathrm{t}}}{2\cosh\left(\frac{E_{\mathrm{t}}-E_{\mathrm{i}}}{kT}\right)}, \tag{2.16}$$

where $W_{\mathrm{dep}}$ is the depletion width. The area current density $J_{\mathrm{A}}$ for a p–n$^+$ junction is dominated by the diffusion current density ($J_{\mathrm{diff}}$) in the neutral regions and the generation current density in the depletion region:

$$J_{\mathrm{A}} \approx q\sqrt{\frac{D_{\mathrm{n}}}{\tau_{\mathrm{n}}}}\frac{n_{\mathrm{i}}^2}{N_{\mathrm{A}}} + q\frac{n_{\mathrm{i}}W_{\mathrm{dep}}}{\tau_{\mathrm{g}}}. \tag{2.17}$$

We can determine whether $J_{\mathrm{diff}}$ or $J_{\mathrm{SRH}}$ is more dominant by evaluating the temperature dependence of the junction leakage current density ($J_{\mathrm{leak}}$). Notably, $J_{\mathrm{diff}}$ and $J_{\mathrm{SRH}}$ are proportional to $n_{\mathrm{i}}^2$ and $n_{\mathrm{i}}$, respectively and $n_{\mathrm{i}}$ is temperature dependent, as follows:[39]

$$n_{\mathrm{i}} = 1.640 \times 10^{15} T^{1.706} \exp\left(-\frac{E_{\mathrm{g}}}{2kT}\right). \tag{2.18}$$

The activation energies of $J_{\mathrm{diff}}$ and $J_{\mathrm{SRH}}$ equal $E_{\mathrm{g}}$ and $E_{\mathrm{g}}/2$, respectively.

The emission of carriers from the trap levels to the conduction or valence band in the depletion region is enhanced by the electric field in the p–n junction ($F_{\mathrm{m}}$). For an electric field of $10^5$–$10^6$ V/cm, trap-assisted tunneling (TAT) becomes dominant. The TAT current density ($J_{\mathrm{TAT}}$) significantly depends on the bias voltage (electric field) in the p–n junction. $J_{\mathrm{SRH}}$ is enhanced by the field enhancement factor $\Gamma$.[40,41]

$$J_{\mathrm{TAT}} = J_{\mathrm{SRH}} \cdot \Gamma(F_{\mathrm{m}}), \tag{2.19}$$

$$\Gamma(F_{\mathrm{m}}) = \sqrt{3\pi}\frac{F_\Gamma}{F_{\mathrm{m}}}\left[\exp\left(\frac{F_{\mathrm{m}}}{F_\Gamma}\right)^2 - \exp\left(\frac{F_{\mathrm{m}}W_0}{F_\Gamma W_{\mathrm{dep}}}\right)^2\right], \tag{2.20}$$

$$F_\Gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar}, \tag{2.21}$$

where $W_0$ is the depletion width at zero bias, $m^*$ ($m^* = 0.25m_0$[42]) is the effective mass of carriers, and $\hbar = h/2\pi$ ($h$-Planck constant). The voltage dependence of the depletion capacitance and the width of the depletion region are expressed as[40]

$$C(V_{\mathrm{rev}}) = \frac{C_0}{\left(1 - \frac{V_{\mathrm{rev}}}{V_{\mathrm{int}}}\right)^P}, \tag{2.22}$$

$$W_{\mathrm{dep}}(V_{\mathrm{rev}}) = W_0\left(1 - \frac{V_{\mathrm{rev}}}{V_{\mathrm{int}}}\right)^p, \tag{2.23}$$

where $C_0$ is the capacitance at zero bias. $V_{\mathrm{int}}$ and $p$ are determined by fitting the capacitance to Eq. (2.23). $F_{\mathrm{m}}$ as a function of the reverse bias voltage ($V_{\mathrm{rev}}$) is expressed as[40]

$$F_{\mathrm{m}}(V_{\mathrm{rev}}) = \frac{V_{\mathrm{int}}}{(1-p)W_0}\left(1 - \frac{V_{\mathrm{rev}}}{V_{\mathrm{int}}}\right)^{1-p}. \tag{2.24}$$

The dominant mechanism for reverse bias leakage current is listed in Table 2.6. The leakage current of the Poole–Frenkel effect ($F_{\mathrm{m}} \sim 10^4$ V/cm) and band-to-band tunneling (BBT) ($F_{\mathrm{m}} > 10^6$ V/cm) are analyzed in Appendix A.1. In the following chapters, the model predictions will be performed based on these mechanisms.

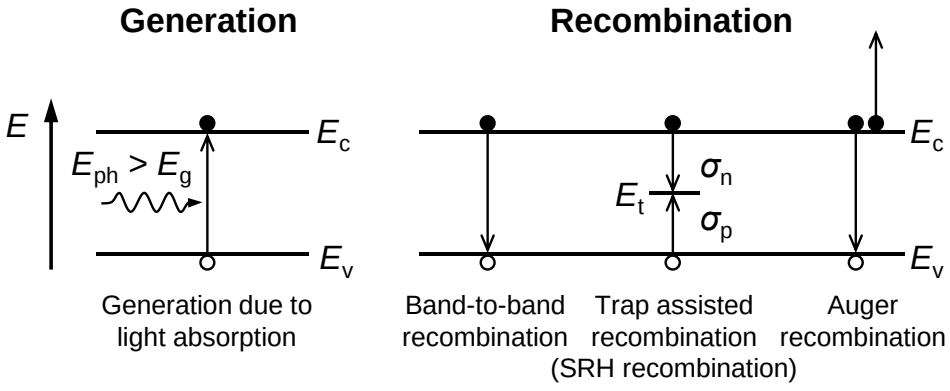



Figure 2.21 Carrier generation and recombination processes.

Table 2.6 Dominant mechanisms for the reverse bias leakage current.

| Components of p–n junction leakage current | Electric field range | Current equations |
|---|---|---|
| Diffusion | — | $J_{\text{diff}} = q\sqrt{\frac{D_{\text{n}}}{\tau_{\text{r}}}}\frac{n_{\text{i}}^2}{N_{\text{A}}}$<br>$n_{\text{i}} = 1.640 \times 10^{15} T^{1.706} \exp\left(-\frac{E_{\text{g}}}{2kT}\right)$ |
| Generation/ recombination (SRH) | — | $J_{\text{SRH}} = \int_0^{W_{\text{dep}}} qGdx \approx qGW_{\text{dep}} = \frac{qn_{\text{i}}W_{\text{dep}}}{\tau_{\text{g}}}$<br>$G = -U = \left[\frac{\sigma_{\text{n}}\sigma_{\text{p}}v_{\text{th}}n_{\text{t}}}{\sigma_{\text{n}}\exp\left(\frac{E_{\text{t}}-E_{\text{i}}}{kT}\right)+\sigma_{\text{p}}\exp\left(-\frac{E_{\text{t}}-E_{\text{i}}}{kT}\right)}\right]n_{\text{i}}$ |
| Poole–Frenkel conduction | ~ $10^4$ V/cm | $J_{\text{PF}} \sim F_{\text{m}}\exp\left(\frac{q}{kT}\sqrt{\frac{qF_{\text{m}}}{\pi\varepsilon_{\text{Si}}}}\right)$ |
| Trap-assisted tunneling (TAT) | ~ a few $10^5$ V/cm | $J_{\text{TAT}} = J_{\text{SRH}} \cdot \Gamma(F_{\text{m}})$<br>$\Gamma(F_{\text{m}}) = \sqrt{3\pi}\frac{F_\Gamma}{F_{\text{m}}}\left[\exp\left(\frac{F_{\text{m}}}{F_\Gamma}\right)^2 - \exp\left(\frac{F_{\text{m}}W_0}{F_\Gamma W_{\text{dep}}}\right)^2\right]$<br>$F_\Gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar}$ |
| Band-to-band tunneling (BBT) | > $10^6$ V/cm | $J_{\text{BBT}} \sim V\left(\frac{F_{\text{m}}}{F_0}\right)^{\frac{3}{2}}\exp\left(-\frac{F_0}{F_{\text{m}}}\right)$<br>$F_0$ is a constant that is temperature dependent |

**References**

[1] H. N. Al-Shareef, A. Karamcheti, T. Y. Luo, G. Bersuker, G. A. Brown, R. W. Murto, M. D. Jackson, H. R. Huff, P. Kraus, D. Lopes, C. Olsen, and G. Miner, Appl. Phys. Lett. **78**, 3875 (2001).

[2] T. Y. Luo, M. Laughery, G. A. Brown, H. N. Al-Shareef, V. H. C. Watt, A. Karamcheti, M. D. Jackson, and H. R. Huff, IEEE Electron Device Lett. **21**, 430 (2000).

[3] K. Nishimura, S. Shishido, Y. Miyake, H. Kanehara, Y. Sato, J. Hirase, Y. Sato, Y. Tomekawa, M. Yamasaki, M. Murakami, M. Harada, and Y. Inoue, Jpn. J. Appl. Phys. **57**, 1002B4 (2018).

[4] A. Uedono, T. Mori, K. Morisawa, K. Murakami, T. Ohdaira, R. Suzuki, T. Mikado, K. Ishioka, M. Kitajima, S. Hishita, H. Haneda, and I. Sakaguchi, J. Appl. Phys. **93**, 3228 (2003).

[5] A. Uedono, K. Tsutsui, S. Ishibashi, H. Watanabe, S. Kubota, Y. Nakagawa, B. Mizuno, T. Hattori, and H. Iwai, Jpn. J. Appl. Phys. **49**, 051301 (2010).

[6] A. Uedono, Y. Mizushima, Y. Kim, T. Nakamura, T. Ohba, N. Yoshihara, N. Oshima, and R. Suzuki, J. Appl. Phys. **116**, 134501 (2014).

[7] Ph. Candelier, B. Guillaumot, F. Mondon, G. Reimbold, H. Achard, and F. Martin, Microelectron. Eng. **36**, 87 (1997).

[8] K. Kanaya and S. Okayama, J. Phys. D: Appl. Phys. **5**, 43 (1972).

[9] N. Aoto, M. Nakamori, S. Yamasaki, H. Hada, N. Ikarashi, K. Ishida, Y. Teraoka, and I. Nishiyama, J. Appl. Phys. **77**, 3899 (1995).

[10] T. Nakahata, K. Yamamoto, J. Tanimura, T. Inagaki, T. Furukawa, S. Maruno, Y. Tokuda, A. Miyamoto, S. Satoh, and H. Kiyama, J. Cryst. Growth **226**, 443 (2001).

[11] C.-L. Cheng, K.-S. Chang-Liao, and T.-K. Wang, Solid-State Electron. **50**, 103 (2006).

[12] A. Matsuda, Y. Nakakubo, Y. Takao, K. Eriguchi, and K. Ono, Thin Solid Films **518**, 3481 (2010).

[13] D. E. Aspnes, J. B. Theeten, and F. Hottier, Phys. Rev. B **20**, 3292 (1979).

[14] I. P. Herman, *Optical Diagnostics for Thin Film Processing* (Academic Press, San Diego, 1996).

[15] S. Joo and H. Liang, in *Encyclopedia of Tribology*, edited by Q. J. Wang and Y.-W. Chung (Springer US, Boston, MA, 2013), pp. 2989–2994.

[16] B. G. Yacobi and D. B. Holt, J. Appl. Phys. **59**, R1 (1986).

[17] G. Davies, Phys. Rep. **176**, 83 (1989).

[18] R. Sugie, K. Inoue, and M. Yoshikawa, J. Appl. Phys. **112**, 033507 (2012).

[19] R. Krause-Rehberg and H. S. Leipner, *Positron Annihilation in Semiconductors: Defect Studies* (Springer, Berlin, 1999).

[20] A. Uedono, Oyo Buturi **84**, 402 (2015) (in Japanese).

[21] A. van Veen, H. Schut, J. de Vries, R. A. Hakvoort, and M. R. Ijpma, AIP Conf. Proc. **218**, 171 (1991).

[22] P. J. Schultz and K. G. Lynn, Rev. Mod. Phys. **60**, 701 (1988).

[23] S. Valkealahti and R. M. Nieminen, Appl. Phys. A **32**, 95 (1983).

[24] S. M. Sze and M.-K. Lee, *Semiconductor Devices, Physics and Technology*, 3rd ed. (Wiley, New York, 2012).

[25] Y. Nakakubo, K. Eriguchi, and K. Ono, ECS J. Solid State Sci. Technol. **4**, N5077 (2015).

[26] X. C. Mu, S. J. Fonash, A. Rohatgi, and J. Rieger, Appl. Phys. Lett. **48**, 1147 (1986).

[27] K. T. Sung, S. W. Pang, M. W. Cole, and N. Pearce, J. Electrochem. Soc. **142**, 206 (1995).

[28] W. Wu and P. K. McLarty, J. Vac. Sci. Technol. A **13**, 67 (1995).

[29] K. Egashira, K. Eriguchi, and S. Hashimoto, in *Proc. IEEE Int. Electron Devices Meeting*, 1998, pp. 563–565.

[30] C.-F. Yeh and C.-H. Liu, in *1998 3rd Int. Symp. Plasma Process-Induced Damage*, 1998, pp. 223–226.

[31] T. Morimoto, H. Ohtake, and T. Wanifuchi, J. Vac. Sci. Technol. B **33**, 051811 (2015).

[32] Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. B **38**, 012205 (2019).

[33] G.-H. Kim, Y.-R. Kang, W.-J. Kim, S.-Y. Kim, and C.-I. Kim, Thin Solid Films **515**, 4892 (2007).

[34] M. Kamei, Y. Takao, K. Eriguchi, and K. Ono, Jpn. J. Appl. Phys. **50**, 08KD05 (2011).

[35] C. D. Thurmond, J. Electrochem. Soc. **122**, 1133 (1975).

[36] W. Shockley and W. T. Read, Phys. Rev. **87**, 835 (1952).

[37] T. Hamamoto, S. Sugiura, and S. Sawada, IEEE Trans. Electron Devices **45**, 1300 (1998).

[38] J.-P Carrère, S. Place, J.-P Oddou, D. Benoit, and F. Roy, in *2014 IEEE Int. Reliab. Phys. Symp.*, 2014, pp. 3C.1.1–3C.1.6.

[39] A. B. Sproul and M. A. Green, J. Appl. Phys. **73**, 1214 (1993).

[40] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 2090 (1992).

[41] G. Roll, M. Goldbach, and L. Frey, Microelectron. Reliab. **51**, 2081 (2011).

[42] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 331 (1992).

# Chapter 3

# Profiling of defects in the vertical direction

## 3.1 Introduction

In the manufacturing of electronic devices, the precise control of the depth profiles of impurities in ion-implanted Si substrates and the device topological features defined by plasma etching (PE) is indispensable. Both ion implantation and PE create damage in crystalline Si substrates (e.g., point defects, defect clusters, and amorphous regions) because of high-energy ion bombardment.[1–6] Ion bombardment damage does not naturally scale with the reduction of the device feature size; hence, the influence of damage creation on device characteristics and reliability is expected to increase with the continued decrease in feature size. Thus, a methodology to assess defects at densities lower than conventional impurity densities is required to decrease and control the number of defects created during manufacturing.

The ion implantation and PE processes can be classified into three categories in terms of defect creation (damage) owing to ion bombardment: high-dose ion implantation, low-dose ion implantation, and PE. In the case of high-dose ion implantation (generally, more than $1 \times 10^{14}$ atoms/cm$^2$), an amorphous layer is formed on the surface.[7] The end-of-range defects[8,9] are created beneath the crystalline/amorphous interface in the Si substrate after thermal annealing. Generally, these defects have been evaluated using TEM and Rutherford backscattering spectrometry.[10]

In the case of low-dose ion implantation (generally, less than $1 \times 10^{14}$ atoms/cm$^2$), defects are created near the Si surface that cannot be identified by TEM observation [that is, the number of defects is below the detection limit of TEM (~ $5 \times 10^{20}$ cm$^{-3}$ as mentioned in Chapter 2)]. Most of these defects are believed to be recoverable following annealing at high temperatures (above 1000 °C).[11] However, the detailed recovery process remains unclear owing to the detection limit of TEM. Positron annihilation spectroscopy (PAS)[12] and the cathodoluminescence (CL) method[13] have been considered promising techniques to identify the presence of residual defects after high-temperature annealing in this regime owing to their increased sensitivity (~ $1 \times 10^{16}$ cm$^{-3}$ and ~ $1 \times 10^{14}$ cm$^{-3}$, respectively, as mentioned in Chapter 2).[14]

In the case of PE, the damaged layer is formed by the bombardment of ions accelerated in the plasma sheath.[15] Primarily, the damaged layer consists of two regions: the SL and IL with displaced Si and interstitial atoms.[16] SL and IL have been evaluated using TEM and spectroscopic ellipsometry (SE). During wet etching (WE), which follows PE, the SL and a portion of the IL are stripped off. However, completely removing the interstitial species and displaced Si atoms underneath the IL is challenging. Localized and isolated defects (latent defects) remain even after the damage recovery processes, such as conventional WE or annealing, and lead to the degradation of Si device performance.[17] Although the presence and behavior of latent defects have been previously examined based on experimental data and model predictions,[18,19] few studies have focused on the sensitivity or detection limits of PPD evaluation techniques. Thus, by considering the sensitivity of defect analysis techniques, a comprehensive methodology to identify the detailed structure and profile of latent defects in low-density regions is crucial.

This chapter focuses on the structure and profile of latent defects in the vertical

(depth) direction created by PE. Various process technologies in the present manufacturing were employed to clarify the behavior of latent defects. In addition to TEM and SE analyses, secondary ion mass spectrometry (SIMS), time-of-flight SIMS (TOF−SIMS), PAS, and CL methods were applied to assess defects in low-density regions.

## 3.2 Experimental procedure

Two types of samples were prepared: Type-A (sample ID: 1–6) and Type-B (sample ID: 7–11), as shown in Fig. 2.1. P-type (100) Si substrates were used. The samples of Type-A (Si sub.) were directly exposed to the electron cyclotron resonance (ECR) plasma source. The samples of Type-B ($SiO_2$/Si sub.) were exposed to the ECR plasma. The sample preparation flowchart is shown in Fig. 2.3 and Table 2.2. The plasma conditions (Process A–F) are listed in Table 2.3. TEM, SE, SIMS, TOF−SIMS, PAS, and CL methods were employed, as listed in Table 2.2. Experimental procedures for Type-A and Type-B samples are shown in Figs. 3.1(a) and 3.1(b), respectively.

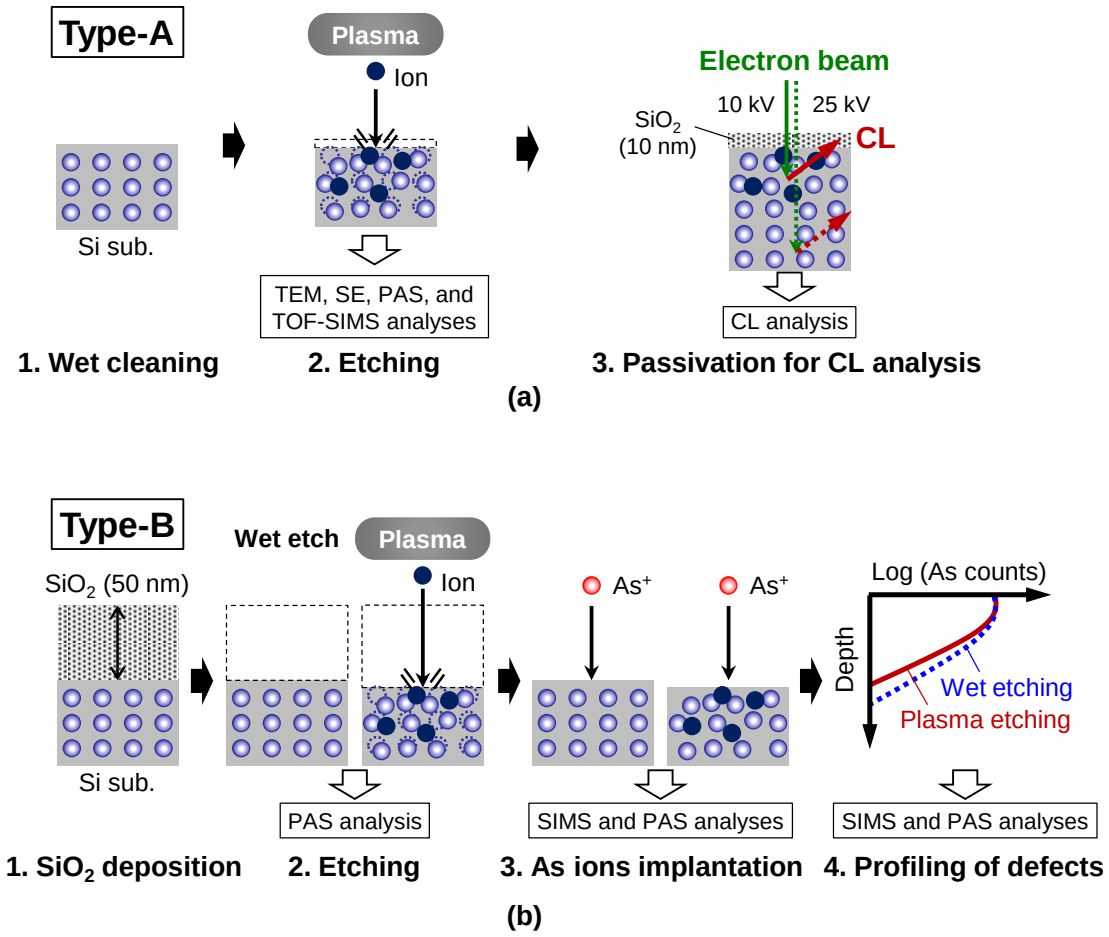



Figure 3.1 Experimental procedures to assign plasma-induced damages in Si substrates using (a) Type-A samples and (b) Type-B samples.

## 3.3 Results and discussion

### 3.3.1 Results obtained by conventional defect analysis

The cross-sectional TEM images after PE [(b1) in Fig. 2.3] under the conditions of processes A and E, as listed in Table 2.3 are shown in Fig. 3.2. The thickness of the amorphous layer increased because of the increase in the peak-to-peak voltage ($V_{pp}$). After the plasma process, an oxidized layer is generally formed on the Si surface because the

plasma-damaged layer is easily oxidized by air exposure.[3,20,21] Consequently, a transition layer is formed underneath the SL. The thickness of the oxidized and transition layers can be determined using SE.[16]

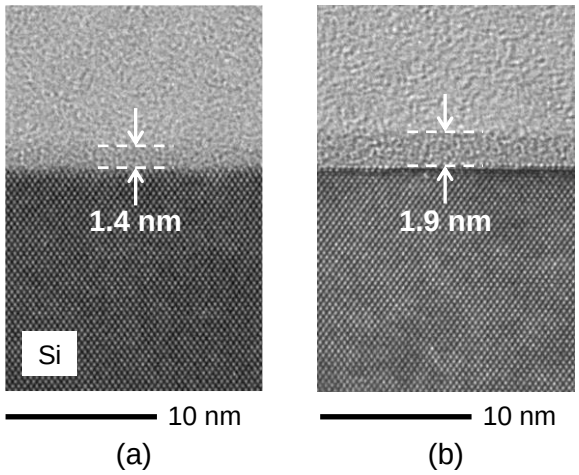



Figure 3.2 Cross-sectional TEM images of samples after PE [Type-A (b1) in Fig. 2.3] under the conditions of (a) Process A ($V_{pp}$ = 320 V) and (b) Process E ($V_{pp}$ = 700 V) in Table 2.3.

Two optical models were employed for comparison in which the transition layer comprised amorphous Si and crystalline Si (Model X) or amorphous Si and $SiO_2$ phases (Model Y), as shown in Fig. 2.12. The total thickness of SL and IL was defined as $d_{total}$ and that of IL and SL, as $d_{IL}$ and $d_{SL}$, respectively. $d_{total}$, $d_{SL}$, and $d_{IL}$ as a function of $V_{pp}$ for the optical models are shown in Fig. 3.3. The mean squared error (MSE)[22] was shown on the right *y*-axis. The MSE was used to quantify the difference between the experimental and model-predicted data, the goodness of fit. Both $d_{total}$ and $d_{IL}$ monotonically increased with an increase in $V_{pp}$. Based on these results, the thickness of the damaged layer increases with an increase in the energy of incident ions.

The thickness of an amorphized layer was also observed in the TEM images (Fig. 3.2). Notably, distinguishing the SL from the transition layers in the plasma-damaged samples using TEM observation is challenging. However, in the case of SE analysis, the surface oxidized and transition layers can be identified using the effective dielectric constants of each layer with a technique, such as effective medium approximation. The MSE value of Model Y was smaller than that of Model X. The estimated total thickness obtained by Model Y was in better agreement with the thickness obtained from the TEM observation compared with Model X. The fraction of $SiO_2$ in the IL gradually decreased with depth. Therefore, Model Y ($SiO_2$:a-Si/c-Si structure) should be employed in the SE analysis.

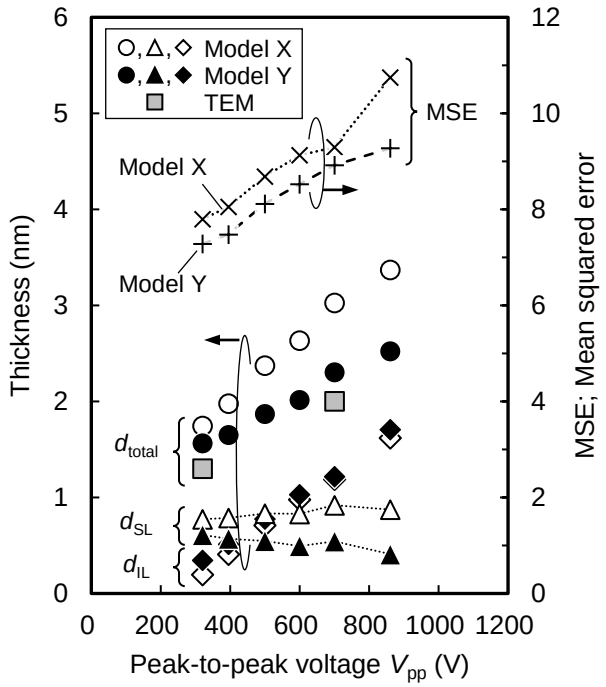



Figure 3.3 Estimated thicknesses ($d_{total}$, $d_{SL}$, and $d_{IL}$) as a function of $V_{pp}$. The MSE is shown on the right *y*-axis. The thickness of an amorphized layer by TEM observation is also shown.

The representative CL spectra of the samples after PE under the conditions listed in Table 2.3 are shown in Fig. 3.4. As mentioned, a 10 nm-thick passivation film was formed on the Si surface [(c) in Fig. 2.3]. A sample without plasma exposure served as the reference sample. Two emission lines, labeled TO and TO+$O^{\Gamma}$, were observed for all samples. These lines corresponded to the emission from the electrons in the band-to-band transition accompanied by the TO phonons and optical phonons at $k = 0$ ($O^{\Gamma}$).[23] The TO-line intensity of the damaged sample was normalized with that of the reference sample to eliminate the influence from the recombination center at the Si surface.

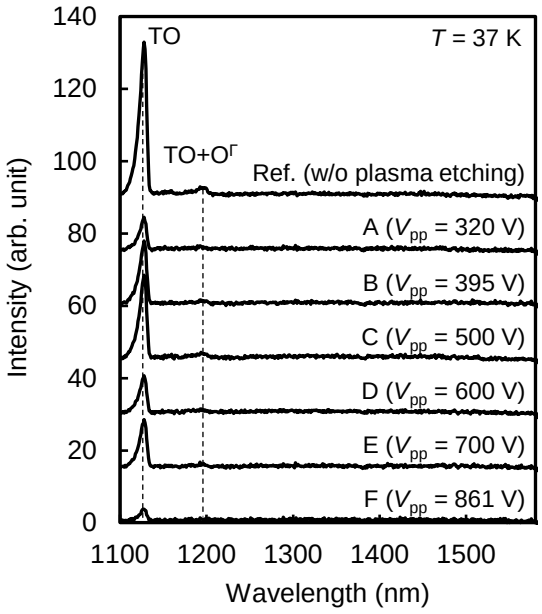



Figure 3.4 Representative CL spectra of the samples after PE under the conditions of processes A to F in Table 2.3. The acceleration voltage of the electron beam is 10 kV. Two characteristic emission peaks, labeled TO and TO+$O^{\Gamma}$, are observed for all samples.

The normalized TO-line peak intensity ratio as a function of $V_{pp}$ for the acceleration voltages of 10 and 25 kV is shown in Figs. 3.5(a) and 3.5(b), respectively. Four CL measurement data for each $V_{pp}$ were obtained. Notably, the electron beam penetration depths for the samples with a passivation film shown in Figs. 3.5(a) and 3.5(b) were shallower than those for the Si substrate without a passivation film. As shown, the TO-line intensity ratio was smaller than the reference in both cases, indicating that non-radiative recombination centers (defects) were formed in the damaged Si substrate.[14,24] The TO-line intensity ratio was lower in Fig. 3.5(a) than that in Fig. 3.5(b), implying that the density profile of non-radiative defects was maximum at the surface and decayed toward the deep region. Moreover, the $V_{pp}$ dependence of the TO-line intensity ratio was observed in Fig. 3.5(b), whereas no clear $V_{pp}$ dependence was observed in Fig. 3.5(a). For the lower acceleration voltage (10 kV), the recombination ratio of electron-hole pairs became saturated and the $V_{pp}$ dependence seemed difficult to identify because of the effects of the defects present in the vicinity of the Si surface. Meanwhile, for the higher acceleration voltage (25 kV), the intensity of the TO-line decreases with higher $V_{pp}$, inferring that more defects were created. The range of the TO-line intensity ratio is shown on the right $y$-axis in Figs. 3.5(a) and 3.5(b). The signal intensity was considerably smaller (1/50–1/100) at an accelerating voltage of 10 kV than that at 25 kV. Therefore, for 10 kV, the variation in the signal intensity relatively increased because of the effect of surface states. The normalized TO-line peak intensity ratio as a function of $d_{IL}$ for the acceleration voltages of 10 and 25 kV is shown in Fig. 3.5(c). This result implied that the amount of damage ($d_{IL}$) decreased with the lower $V_{pp}$, and the variation ratio increased. In summary, a higher acceleration voltage is required for the CL analysis of PPD even if the damaged layer thickness is in the range of several nanometers.

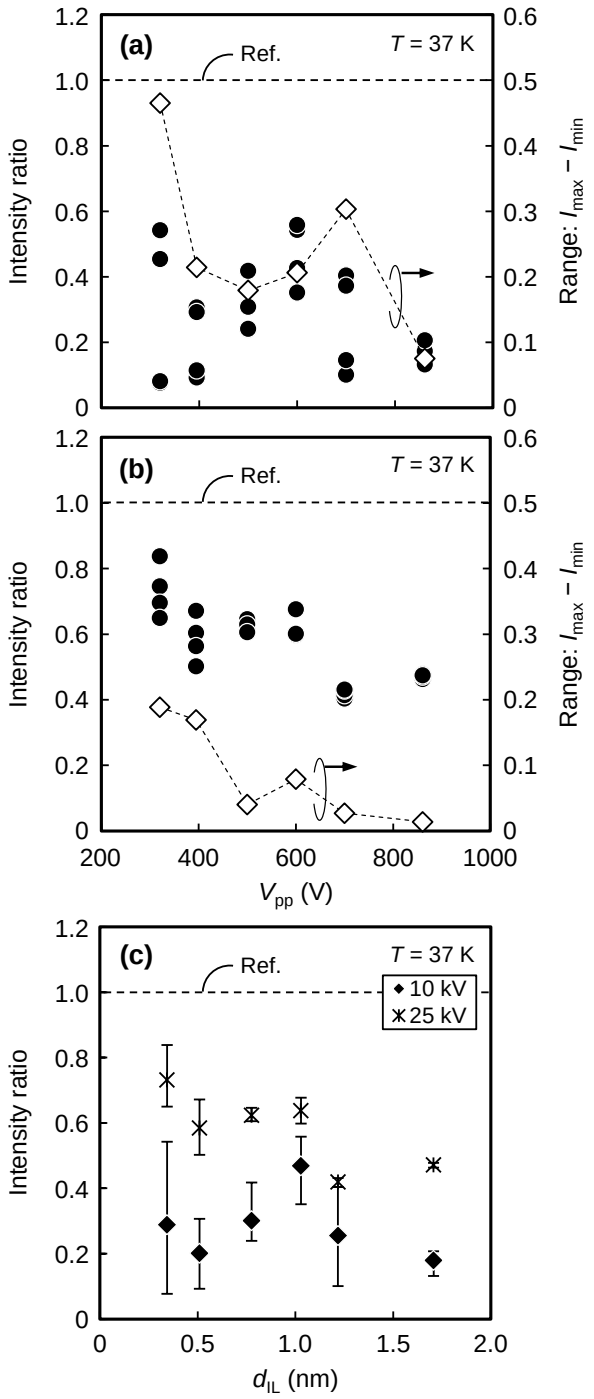



Figure 3.5 $V_{pp}$ dependence of the normalized TO-line peak intensity ratio at electron beam acceleration voltages of (a) 10 and (b) 25 kV. The range of the TO-line peak intensity ratio is shown on the right *y*-axis. (c) The normalized TO-line peak intensity ratio is shown as a function of $d_{IL}$ for acceleration voltages of 10 and 25 kV.

The depth profiles of O, C, and F atoms are shown in Figs. 3.6(a)–3.6(c), respectively, obtained using TOF−SIMS after PE under the conditions of processes A, B, and E. In these cases, a sample cleaned by an ammonium hydrogen-peroxide mixture served as the reference sample. A change was observed in the C and F profiles after PE, as shown in Figs. 3.6(b) and 3.6(c), respectively, whereas no significant change was observed for the O profile in Fig. 3.6(a). The C and F atomic concentrations significantly increased (by one or two orders of magnitude) as $V_{pp}$ increased, as shown in Figs. 3.6(b) and 3.6(c), respectively. The $CF_3$ radicals from plasma were adsorbed on the Si or $SiO_2$ surface and dissociated into C and F by the impact of the incident ions. The oxidation was suppressed by the presence of the $CF_x$ polymer on the surface; hence, the $V_{pp}$ dependence may not be identified with respect to the depth profile of the O atoms. In contrast, the C and F atoms diffused deeper with an increase in $V_{pp}$ because the projected range of the incident ions increased with the higher $V_{pp}$. The thicknesses of the C and F distribution regions ($> 10^{18}$ $cm^{-3}$) were assessed to be approximately 10 nm, which is significantly thicker than that assigned by the TEM and SE analyses. This finding suggested that these species function as latent defects (presumably interstitial or defect precursors, in this case) that are not identified by conventional physical and optical techniques. Thus, in modern manufacturing, C and F atoms are sensitive measures for the PPD analysis using TOF−SIMS.

The PAS analysis was performed to investigate the detailed structure and profile of defects. The *S* parameter obtained by the PAS analysis after PE under the condition of process E (as damaged samples) as a function of the incident positron energy $E_{PAS}$ is shown in Fig. 3.7. The projection range of the incident positron was estimated according to the energy and displayed on the upper *x*-axis. A comparison between the reference and

damaged samples is shown in Fig. 3.7. The *S* parameter in the PAS analysis assigns the presence of the positron recombination centers, generally vacancies in the Si substrate. These vacancies are believed to exist on the surface of the Si substrate leading to an increase in the *S* value.[25] The *S* value is almost constant at high $E_{PAS}$ (>10 keV), indicating that, in this energy range, almost all positrons annihilated in the substrate without diffusing back to the surface region. As shown, the *S* parameter of the damaged sample was lower than that of the reference, particularly near the surface. The difference was validated at a depth of approximately 200 nm. As previously mentioned,[26–29] the *S* value decreased when the impurities were introduced into a Si substrate because of the coupling between the impurity and the vacancy—in this case between F and the vacancy. The decrease in the *S* parameter might correspond to the creation of defects after PE. Based on this assumption, the present finding indicated that latent defects existed for a depth of up to 20 nm, at least.

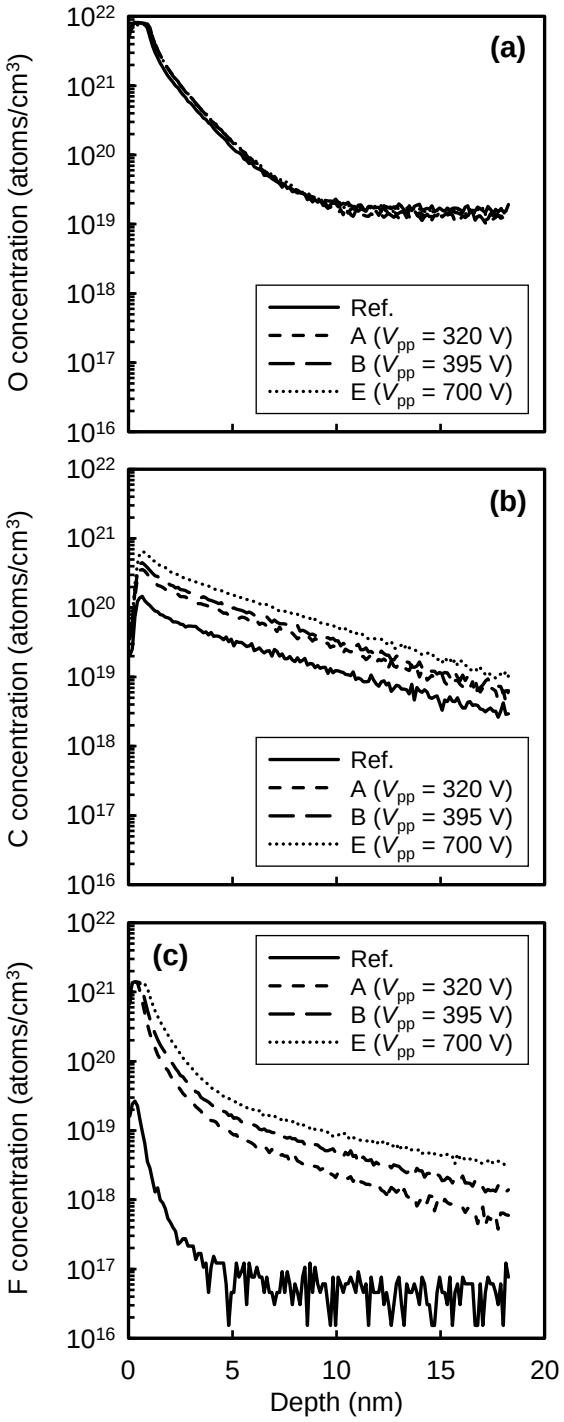



Figure 3.6 Impurity profiles obtained using TOF−SIMS after PE under the conditions of processes A, B, and E. Depth profiles of (a) O, (b) C, and (c) F atoms.

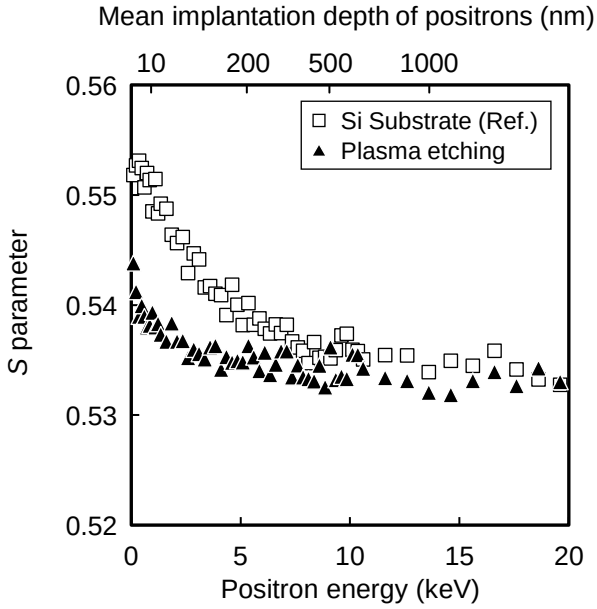


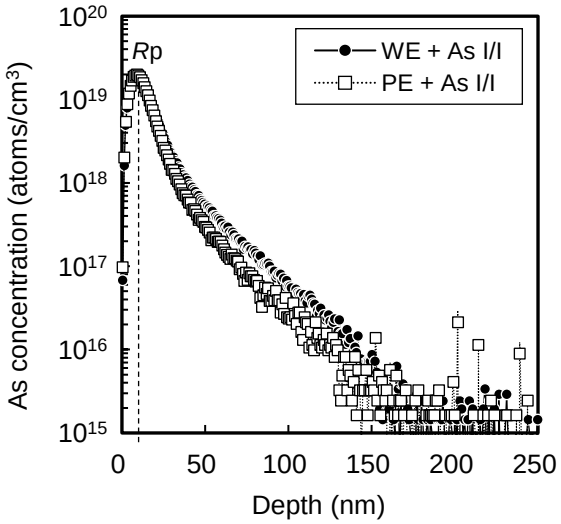

Figure 3.7 *S* parameter as a function of the incident positron energy $E_{PAS}$ for the reference and damaged samples under the condition of process E in Table 2.3. The *S* parameter near the Si surface decreases after PE.

### 3.3.2 Dechanneling behavior of As ions in the damaged layer

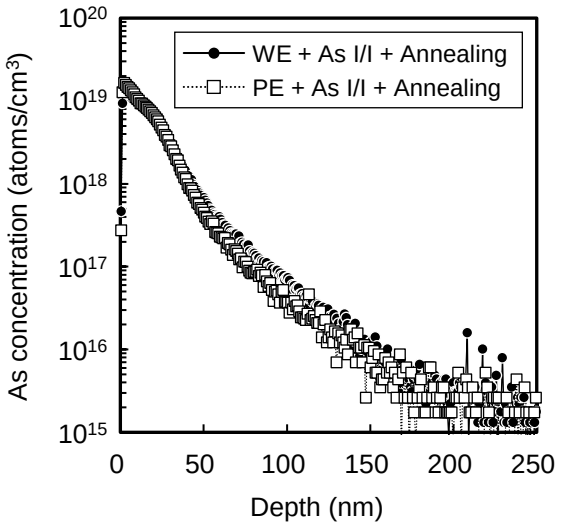
As previously mentioned, both CL and PAS analyses can be used to identify plasma-induced latent defects present underneath the surface oxidized and interface (transition) regions assigned by TEM and SE. In this chapter, the dechanneling mechanism of impurity was utilized and its dynamic behavior was investigated to validate the findings. Arsenic atoms were used as markers for the analysis. As shown in Fig. 2.3, As atoms were implanted after PE and thermal annealing was subsequently performed (Type-B samples in Fig. 2.3).

The As profiles after ion implantation [(d) in Fig. 2.3] and after annealing [(e) in Fig. 2.3] are shown in Figs. 3.8(a) and 3.8(b), respectively, obtained by TOF−SIMS. The As profiles of the samples with an oxide film removed by PE under the condition denoted by process E in Table 2.3 [(b2) in Fig. 2.3] and those with an oxide film removed by WE [(b3) in Fig. 2.3] were compared. The projected range ($R_p$) of As atoms was approximately 10 nm in this energy range. As shown in Fig. 3.8(a), the difference in the distribution edge of As atoms was obtained in the range from 50 to 200 nm in depth; the As profile in the plasma-damaged sample was steeper than that of the wet-etched sample. Therefore, the channeling of As ions was suppressed by defects created during PE. As shown in Fig. 3.8(b), the difference in the distribution edge was still observed even after annealing.

The *S* parameter as a function of the incident positron energy $E_{PAS}$ for the plasma-damaged and As-ion implanted (As I/I) samples is shown in Fig. 3.9. This figure shows (1) a comparison between the reference and damaged samples (□, ▲) and (2) a comparison between the plasma-damaged and wet-chemical-etched samples after annealing (●, ♦). Similar to the case in Fig. 3.7, the *S* value near the Si surface of the damaged sample was lower than that of the reference sample. The *S* parameter of the plasma-damaged sample significantly decreased near the Si surface compared with that of the wet-chemical-etched sample. Thus, annealing after As-ion implantation enhanced bonding between impurities (C, F, and As) and vacancies created by PE, consequently reducing the *S* parameter.




(a)




(b)

Figure 3.8 As profiles obtained using the SIMS analysis for plasma-damaged and wet-chemical-etched samples after (a) ion implantation [(d) in Fig. 2.3] and (b) thermal annealing [(e) in Fig. 2.3].

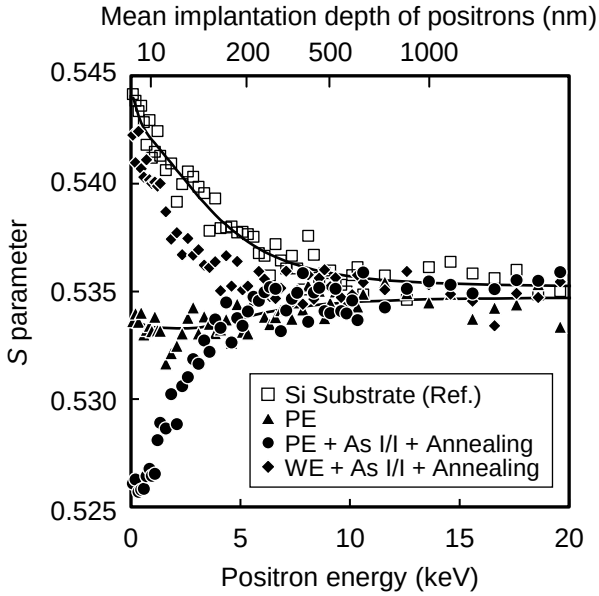



Figure 3.9 *S* parameter as a function of the incident positron energy for various samples. (□): Reference, (▲): after PE, (●): plasma-damaged and As-implanted sample after thermal annealing, and (♦): wet-chemical-etched and As-implanted sample after thermal annealing.

The impurity profiles before and after annealing are shown in Fig. 3.10. The depth profiles of the O, C, and F atoms are shown in Figs. 3.10(a)–3.10(c), respectively. These figures compare the results between the plasma-damaged and wet-chemical-etched samples. No significant difference was observed between the plasma- and wet-chemical-etched samples in the profile of the O atoms, as shown in Fig. 3.10(a). Conversely, the profiles of the C and F atoms showed considerable differences between the plasma- and wet-chemical-etched samples, as shown in Figs. 3.10(b) and 3.10(c), respectively. Notably, these species originated from the processing steps employed in this study. The

concentration of the C and F atoms near the surface of the plasma-etched sample was higher than that of the wet-chemical-etched sample. This result implied that the profiles of the C and F atoms after the PE—a typical defect structure—were further advanced into the sample and the diffusion of F atoms was more obvious after thermal annealing compared with C atoms in the plasma-damaged region. The profile of C atoms was almost identical before and after annealing, indicating that the impinged C atoms were more stable than F atoms during thermal annealing. F atoms were considered to diffuse back to the Si substrate surface during the annealing process. Two essential features were validated from the aforementioned results: (1) C and F atoms can be used as markers to analyze the profile of latent defects (by PPD) in SIMS analysis. (2) F atoms exhibit characteristic thermal diffusion in the region of ~100 nm and can be used as a marker to analyze the thermal behavior of the damaged region. The decrease in the *S* value may be primarily attributed to the presence of F atoms after PE, as shown in Figs. 3.7 and 3.9. The F atoms were considered to be trapped in vacancies and annealed with the vacancies during thermal annealing. These interactions decreased the *S* value (number of vacancies), which is consistent with the results of previous studies.[28] Finally, we focused on the impurity profiles obtained using the SIMS and PAS analyses.

The differential profile of As atoms (wet-chemical-etched–plasma-etched) calculated from the results in Fig. 3.8 is shown in Fig. 3.11, according to which the channeling behavior of As atoms was suppressed to be more than $10^{15}$ atoms/cm$^3$ at a region ~200 nm from the Si substrate surface. The difference in the profile is attributed to the original defect profile owing to PE. The defect distribution was predicted from the $S$–$E_{PAS}$ curve in the PAS measurement using VEPFIT—a computer program developed by van Veen *et al*.[30]—to validate the defect profile obtained using the SIMS analysis in

combination with As ion implantation. Generally, the peak of the damage profile is at the surface; hence, the defect density monotonically decreases along the depth. Therefore, the two-layer model was employed in the VEPFIT analysis, where the two effective diffusion lengths and *S* parameters were defined. The thickness of this region where the effective diffusion length and *S* parameter differ from the reference sample was obtained using this two-layer model. The estimated result from the sample after PE (▲) in Fig. 3.9 is indicated on the right *y*-axis. As shown in Fig. 3.11, an abrupt increase of approximately 130 nm was observed, indicating that PPD defects were present from the surface to this region and had a density of ~$10^{16}$ $cm^{-3}$ based on the detection limit of the PAS analysis [25,31]. This result was consistent with the differential profile obtained using SIMS, as shown in Fig. 3.11. In summary, latent defects were distributed to a depth of at least 130 nm after PE.

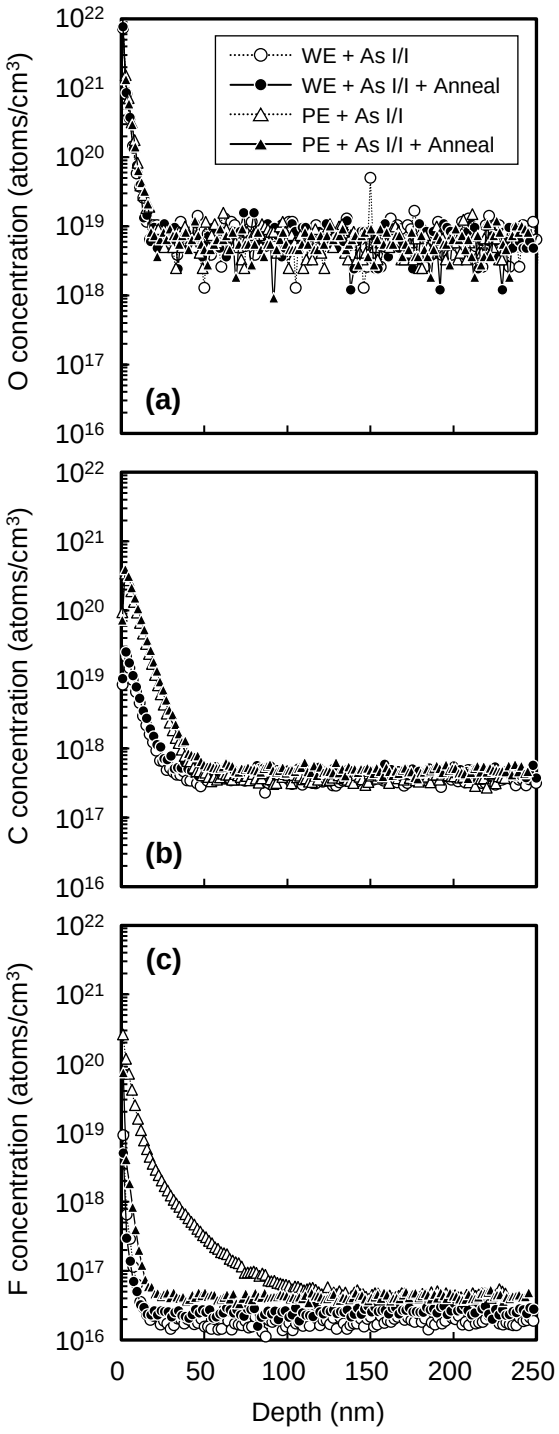



Figure 3.10 Impurity profiles obtained using SIMS before and after annealing. Depth profiles of (a) O, (b) C, and (c) F atoms.

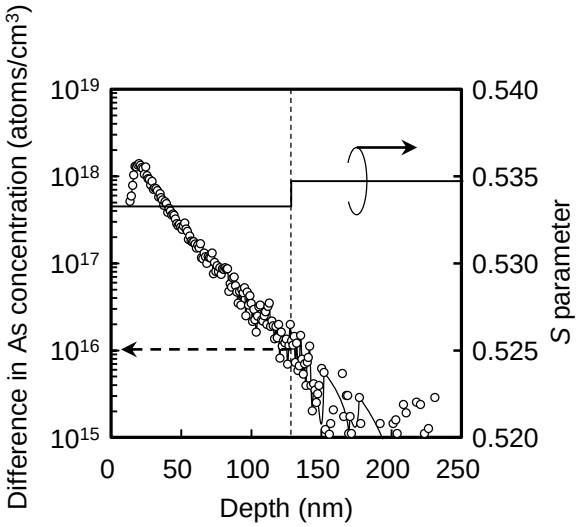



Figure 3.11 Differential profile of As-ions (wet-chemical-etched–plasma-etched). The *S* parameter is shown on the right *y*-axis.

The PPD evaluation techniques employed in this study with respect to the identified thicknesses of a damaged layer and defect density after PE is shown in Fig. 3.12. The profile of defects (solid line in Fig 3.12) was also obtained using a technique that utilizes PPD-enhanced dechanneling of As atoms implanted with a projection range of 10 nm.

The thickness of the damaged layer in the Si substrates was determined to be approximately 1–2 nm by TEM and SE analyses. Based on CL analysis, the density profile of non-radiative defects was maximum at the surface and decayed toward the deep region. TOF−SIMS analysis identified the presence of interstitial atoms (C and F) to a depth of ~20 nm. A decrease in the *S* value, suggesting the presence of defects from the surface to a depth of ~200 nm, was validated by PAS analysis.

The dechanneling mechanism of impurity (As atom) was utilized and its dynamic behavior was investigated to identify plasma-induced latent defects. In the SIMS measurements, the change in the distribution edge of As atoms owing to PPD was observed in depths ranging from 50 to 200 nm. Moreover, impinged F atoms were validated as a sensitive marker to characterize the defect behavior during thermal annealing. Based on PAS analysis, structural changes related to vacancies interacting with C and F atoms distributed from the surface reached a depth of approximately 130 nm in Si substrates. The technique that utilizes the PPD-induced dechanneling mechanism of As atoms assessed defects with a density of ~$10^{16}$ $cm^{-3}$.

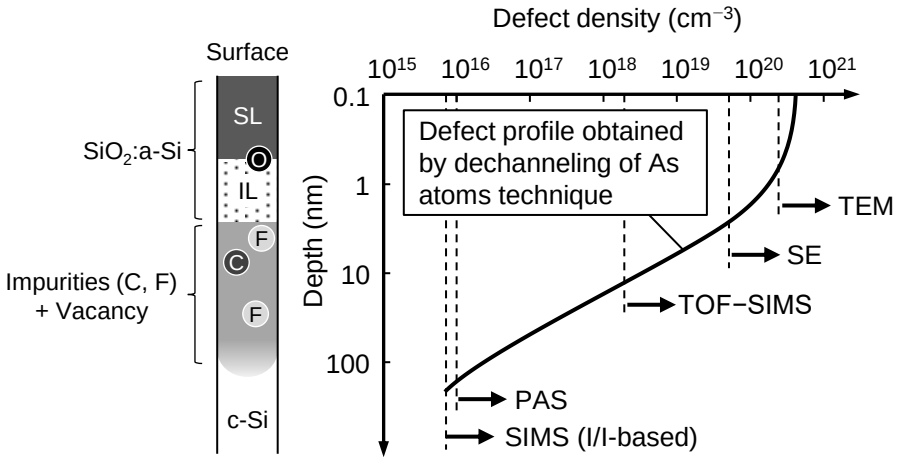



Figure 3.12 Summary of PPD evaluation techniques employed in this study with respect to the identified thicknesses of the "damaged" layer and defect density after PE.

## 3.4 Conclusion

The plasma-induced defect creation in the present manufacturing processes was comprehensively investigated using various techniques. We focused on low-density latent defects present underneath IL after PE. Surface-damaged structures were investigated using TEM and SE, assigning the presence of PPD. Based on CL analysis, the created defects (both on the Si surface and underneath the IL) function as carrier recombination centers. TOF−SIMS analysis assigned the presence of interstitial atoms (C and F) to a depth of ~20 nm. The change in the *S* value within the surface region of 200 nm thick (both on the Si surface and underneath the IL) was assessed using PAS analysis. F atoms introduced during PE were the key species to investigate the profile of defects.

SIMS analysis was employed to track the implanted As ions and reveal the dynamic behavior of created defects by PE. From the comparison of the profile of As atoms in the samples treated by plasma- and wet-etch processes, the channeling of As ions was suppressed because of the defects created by PPD. Based on PAS analysis, defects were distributed from the Si surface to a depth of 130 nm. The SIMS analysis combined with the PAS analysis validated the presence of PPD defects from the surface to 130 nm and the density to be ~$10^{16}$ $cm^{-3}$, which is lower than the previously reported densities. Furthermore, F atoms introduced during PE were the key species to investigate the dynamics (diffusion) of defects during thermal annealing. The profile of low-density defects performed herein is indispensable to understanding the PPD mechanism and designing future electronic devices that are sensitive to defect creation.

**References**

[1] J. F. Gibbons, Proc. IEEE **60**, 1062 (1972).

[2] K. S. Jones, S. Prussin, and E. R. Weber, Appl. Phys. A **45**, 1 (1988).

[3] T. Ohchi, S. Kobayashi, M. Fukasawa, K. Kugimiya, T. Kinoshita, T. Takizawa, S. Hamaguchi, Y. Kamide, and T. Tatsumi, Jpn. J. Appl. Phys. **47**, 5324 (2008).

[4] M. Fukasawa, Y. Nakakubo, A. Matsuda, Y. Takao, K. Eriguchi, K. Ono, M. Minami, F. Uesawa, and T. Tatsumi, J. Vac. Sci. Technol. A **29**, 041301 (2011).

[5] C. Petit-Etienne, E. Pargon, S. David, M. Darnon, L. Vallier, O. Joubert, and S. Banna, J. Vac. Sci. Technol. B **30**, 040604 (2012).

[6] T. Shigetoshi, M. Fukasawa, K. Nagahata, and T. Tatsumi, Jpn. J. Appl. Phys. **54**, 06GB05 (2015).

[7] S. Shibata, F. Kawase, A. Kitada, T. Kouzaki, and A. Kitamura, IEEE Trans. Semicond. Manuf. **23**, 545 (2010).

[8] B. de Mauduit, L. Laânab, C. Bergaud, M. M. Faye, A. Martinez, and A. Claverie, Nucl. Instrum. Methods Phys. Res. B **84**, 190 (1994).

[9] C. Bonafos, D. Mathiot, and A. Claverie, J. Appl. Phys. **83**, 3008 (1998).

[10] F. Cristiano, C. Bonafos, A. Nejim, S. Lombardo, M. Omri, D. Alquier, A. Martinez, S. U. Campisano, P. L. F. Hemment, and A. Claverie, Nucl. Instrum. Methods Phys. Res. B **127**, 22 (1997).

[11] J. F. Ziegler, *Ion Implantation: Science and Technology* (Academic Press, Orlando, 1984).

[12] R. Krause-Rehberg and H. S. Leipner, *Positron Annihilation in Semiconductors: Defect Studies* (Springer, Berlin, 1999).

[13] B. G. Yacobi and D. B. Holt, *Cathodoluminescence Microscopy of Inorganic Solids*

(Plenum, New York, 1990).

[14] A. Sagara, A. Uedono, and S. Shibata, IEEE Trans. Semicond. Manuf. **28**, 92 (2015).

[15] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing* (Wiley, New York, 2005).

[16] A. Matsuda, Y. Nakakubo, Y. Takao, K. Eriguchi, and K. Ono, Thin Solid Films **518**, 3481 (2010).

[17] K. Eriguchi, Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, H. Nakagawa, S. Hayashi, S. Noda, K. Ishikawa, M. Yoshimaru, and K. Ono, in *Proc. IEEE Int. Electron Devices Meeting*, 2008, pp. 1–4.

[18] Y. Nakakubo, K. Eriguchi, and K. Ono, ECS J. Solid State Sci. Technol. **4**, N5077 (2015).

[19] K. Eriguchi and Y. Okada, J. Phys. D: Appl. Phys. **50**, 26LT01 (2017).

[20] G. S. Oehrlein, Mater. Sci. Eng. B **4**, 441 (1989).

[21] S. A. Vitale and B. A. Smith, J. Vac. Sci. Technol. B **21**, 2205 (2003).

[22] J. A. Woollam, B. Johs, C. M. Herzinger, J. Hilfiker, R. Synowicki, and C. L. Bungay, in Proc. SPIE **10294**, 1029402 (1999).

[23] G. Davies, Phys. Rep. **176**, 83 (1989).

[24] R. Sugie, K. Inoue, and M. Yoshikawa, J. Appl. Phys. **112**, 033507 (2012).

[25] A. Uedono, Oyo Buturi **84**, 402 (2015) (in Japanese).

[26] A. Uedono, T. Kitano, M. Watanabe, T. Moriya, N. Komuro, T. Kawano, S. Tanigawa, R. Suzuki, T. Ohdaira, and T. Mikado, Jpn. J. Appl. Phys. **36**, 969 (1997).

[27] A. Uedono, T. Kitano, K. Hamada, T. Moriya, T. Kawano, S. Tanigawa, R. Suzuki, T. Ohdaira, and T. Mikado, Jpn. J. Appl. Phys. **36**, 2571 (1997).

[28] A. Uedono, S. Inumiya, T. Matsuki, T. Aoyama, Y. Nara, S. Ishibashi, T. Ohdaira, R.

Suzuki, S. Miyazaki, and K. Yamada, J. Appl. Phys. **102**, 054511 (2007).

[29] A. Uedono, K. Tsutsui, S. Ishibashi, H. Watanabe, S. Kubota, Y. Nakagawa, B. Mizuno, T. Hattori, and H. Iwai, Jpn. J. Appl. Phys. **49**, 051301 (2010).

[30] A. van Veen, H. Schut, J. de Vries, R. A. Hakvoort, and M. R. Ijpma, AIP Conf. Proc. **218**, 171 (1991).

[31] A. Uedono, L. Wei, C. Dosho, H. Kondo, S. Tanigawa, and M. Tamura, Jpn. J. Appl. Phys. **30**, 1597 (1991).

# Chapter 4

# Evaluation of latent defects using vertical and lateral p–n junctions

## 4.1 Introduction

The influence of PPD on device performance and reliability is critical when scaling devices in which an extremely low defect density is required. Our comprehension of PPD mechanisms is commonly limited by two issues: (1) the detection limits of PPD evaluation techniques and (2) the assessment of defect distribution in three-dimensional (3D) structures. The degradation of material properties using PPD was investigated using a wide variety of structural and electrical analyses, such as transmission electron microscopy (TEM), spectroscopic ellipsometry (SE),[1,2] electron spin resonance (ESR) analysis,[3] *I–V*,[4–9] and *C–V*[10] techniques. Although these methods can detect the presence of defects in Si substrates after PPD, quantifying the defects in the density range of $< 10^{18}$ $cm^{-3}$ and developing a detailed defect profile is challenging owing to the detection limits. In Chapter 3, the profile of low-density defects ($\sim 10^{16}$ $cm^{-3}$) was measured using secondary ion mass spectrometry (SIMS) combined with positron annihilation spectroscopy (PAS) and cathodoluminescence (CL), where generated vacancies and carrier recombination centers in damaged Si substrates were validated to be identified by PAS and CL, respectively. The combination technique was used to track the PPD-enhanced dechanneling of ion-implanted As atoms in damaged Si substrates.

In general, conventional PPD structural analyses determine the PPD depth profile and the density of permeated species in the damaged surface region. Spatially resolved structural analysis and/or electrical measurements using specifically designed devices should be employed to assign the lateral (spatial) distribution of defects created by PPD. In contrast to the physical analyses outlined in Chapter 3, electrical techniques are believed to be sufficiently sensitive in PPD analyses. *I–V* measurements using Schottky contact structures and *C–V* measurements of the change in damaged-layer capacitance are widely used. Exploration by electrical techniques may be a powerful tool to detailedly assess defect creation in advanced electronic devices. However, most of these methods only measure the effects of vertically distributed defects on electrical performance.[4–9] Thus, these conventional methods cannot be used to measure defects created by stochastic straggling of incident species in the lateral direction.

Here, defect creation in the vertical and lateral directions of Si substrates during plasma processing is investigated using devices with different p–n junction structures. (1) To evaluate PPD in the vertical direction, blanket wafers were used for physical and *C–V* analyses to evaluate the effects of plasma etching (PE) and subsequent furnace annealing (FA). A chemical dry etching (CDE)[11–13] process was performed after PE to evaluate the influence of residual species such as O, C, and F. (2) To evaluate PPD in the lateral direction, lateral p–n junction structures with different distances between the p-type and n-type regions ($D_{pn}$) were designed and tested. The electric field of lateral p–n junctions was varied by controlling the voltage applied to the p–n junction ($V_{rev}$), and *I–V* measurements for devices with various $D_{pn}$ were conducted to determine the distributions of latent defects in the vertical and lateral directions. Based on the results obtained, the PPD mechanisms in the vertical and lateral directions will be discussed in detail.

## 4.2 Experimental

### 4.2.1 Evaluation of the PPD scheme in the lateral direction

A schematic of defect creation during plasma processing for the manufacturing of devices is shown in Figure 4.1(a). Defects are distributed in the lateral direction underneath the $SiO_2$ mask in addition to the vertical direction because of lateral straggling. The setup used to measure the vertical leakage current ($I_V$) is shown in Fig. 4.1(b); wide p–n junctions were used to evaluate PPD in the vertical direction. The setup designed to measure the $I_V$ and lateral leakage current ($I_L$) is shown in Fig 4.1(c). Lateral p–n junction structures with varying lateral distances between the p- and n-type regions ($D_{pn}$) were prepared and the density of local defects was estimated from the changes in $I_V$ and $I_L$. Because defects act as carrier trap sites in the Si bandgap, the conduction of carriers via trap sites increases $I_V$ and $I_L$.

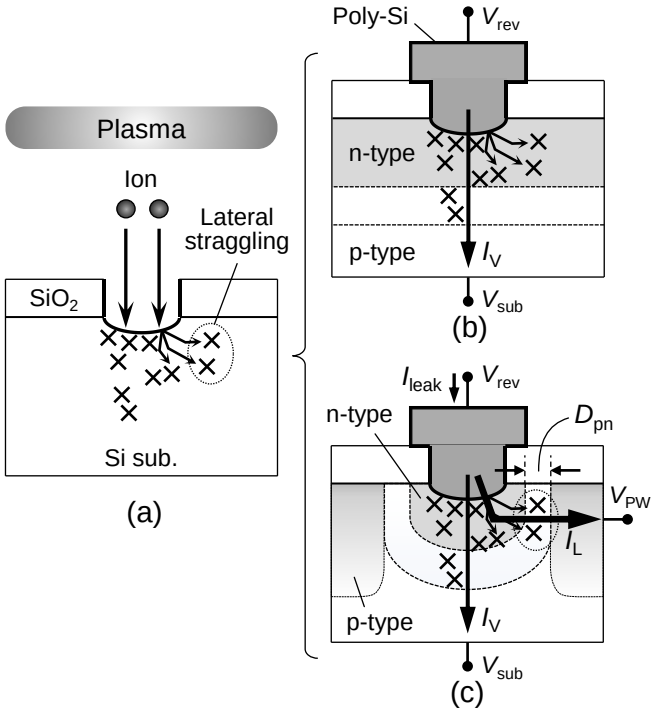



Figure 4.1 (a) Schematic of defect creation mechanisms during plasma processing. Setups to measure (b) the vertical leakage current ($I_V$) and (c) the $I_V$ and the lateral leakage current ($I_L$).

### 4.2.2 Methodology

Two types of samples—blanket wafers (Type-A) and p–n junction (Type-C) devices—were prepared to investigate PPD.

**Type-A samples**

The process conditions for Type-A samples (See Fig. 2.5 for the detailed process flow.) are listed in Table 4.1. An experimental procedure using Type-A samples to investigate the influence of residual species in the damaged layer is shown in Fig. 4.2.

Table 4.1 Preparation procedures for Type-A samples: low-temperature CDE (LT), high-temperature CDE with $O_2$ addition (HT1) and without $O_2$ (HT2).

| Sample ID (Type-A) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| Wet cleaning | ● | ● | ● | ● | ● | ● | ● | ● | ● |
| Plasma etching | – | ● | ● | ● | ● | ● | ● | ● | ● |
| Ashing | – | ● | ● | ● | ● | ● | ● | ● | ● |
| Wet cleaning | – | ● | ● | ● | ● | ● | ● | ● | ● |
| Chemical dry etching | – | – | – | LT | LT | HT1 | HT1 | HT2 | HT2 |
| Wet cleaning | – | ● | ● | ● | ● | ● | ● | ● | ● |
| Furnace annealing | – | – | ● | – | ● | – | ● | – | ● |

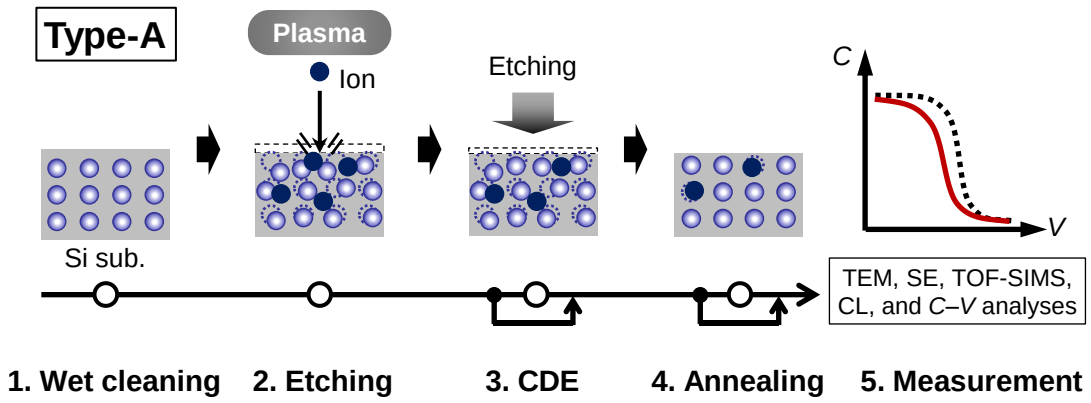



Figure 4.2 Experimental procedure to investigate the influence of residual species in the damaged layer using Type-A samples.

**Type-C devices**

Type-C devices were prepared based on the flowchart shown in Fig. 2.6. Cross-sectional schematics are also shown. The process conditions for Type-C devices are listed in Table 4.2. The dimensions and bias conditions of Type-C devices are shown in Fig. 4.3.

*I–V* measurements were performed using contact-hole array patterns with 504,000 contacts; the diameter of the bottom of the contacts was approximately 90 nm. The duration of a Si over-etching step was varied to investigate the relationship between Si recess ($d_R$) and junction leakage current. $D_{pn}$ was varied from 0 to 210 nm. The voltages applied to the deep n-well, p-well, and Si substrates were $V_{NW}$ = 0.5, $V_{PW}$ = 0, and $V_{sub}$ = 0 V, respectively. $V_{rev}$ was varied from 0 to 3 V.

Table 4.2 Preparation procedure for Type-C devices.

| Sample ID (Type-C) | I | II | III |
|---|---|---|---|
| Plasma etching | ● | ● | ● |
| Ashing | ● | ● | ● |
| Wet cleaning | ● | ● | ● |
| Chemical dry etching | – | HT1 | HT2 |
| Wet cleaning | ● | ● | ● |
| Poly-Si deposition and etching | ● | ● | ● |
| Furnace annealing | ● | ● | ● |

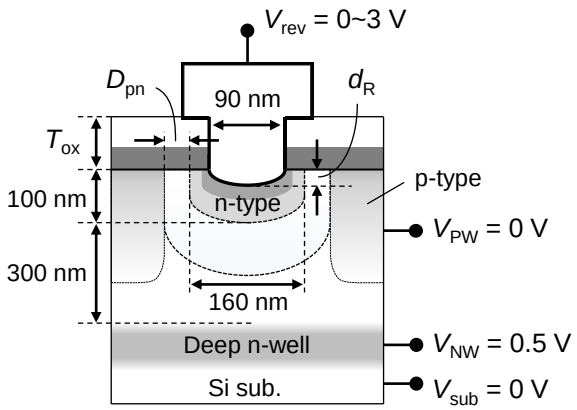



Figure 4.3 Detailed device dimension and bias condition.

## 4.3 Results and discussion

### 4.3.1 PPD assessment in the vertical direction

Cross-sectional TEM images of the reference sample (ID 1), the plasma-etched sample (ID 2), and the plasma-etched sample after HT2 CDE treatment (ID 8) are shown in Fig. 4.4. The amorphized layer thickness was measured using the image contrast after the cross-sectional TEM image processing.[14] The amorphous layers on the Si surface of samples 1 and 2 were each approximately 1.7 nm thick, indicating that the change in the thickness caused by the initial PE is challenging to measure using TEM. The amorphous layer on sample 8 was thicker and rougher than those on samples 1 and 2. Two mechanisms were proposed to explain the increased roughness of sample 8: (1) surface roughening induced by F radicals in the absence of $O_2$ under the HT2 CDE condition,[15] and (2) enhanced oxidation of the damaged layer by exposure to air,[16–18] which is supported by the increased thickness of sample 8 amorphous layer (1.9 nm).

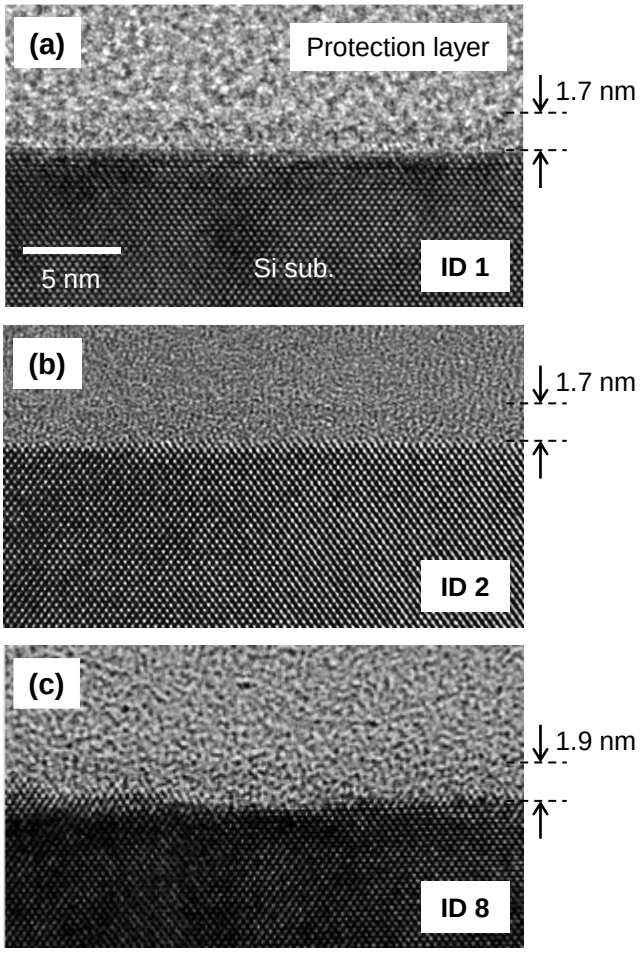



Figure 4.4 Cross-sectional TEM images of (a) the reference sample (ID 1), (b) the plasma-etched sample (ID 2), and (c) the plasma-etched sample after HT2 CDE treatment (ID 8).

The thicknesses of the surface oxidized layer (SL: $d_{SL}$) and interfacial transition layer (IL: $d_{IL}$) were determined using SE and an optical model in which the IL comprises amorphous Si and $SiO_2$ phases (Model Y in Fig. 2.12). The estimated $d_{SL}$ and $d_{IL}$ for

samples 1–9 are shown in Fig. 4.5. The mean squared error (MSE)[19] on the right *y*-axis in Fig. 4.5 was used to quantify the difference between the experimental and model-predicted data; that is, the goodness of fit. The overall MSE value increased with $d_{IL}$ as $d_{IL}$ is estimated using a simple optical model of amorphous Si and $SiO_2$ phases. In particular, because the PPD increases the $d_{IL}$ value,[20] treatments with the oxidation-based processes (ID 4 and 6) significantly increases $d_{SL}$. $d_{IL}$ was relatively large for samples 2 and 8. Therefore, the oxidation of samples 2 (plasma-etched) and 8 (plasma-etched and HT2-CDE treated) was suppressed compared with samples 4 and 6. The $d_{SL}$ increased for samples 4–9, particularly the samples treated by LT CDE (ID 4 and 5).

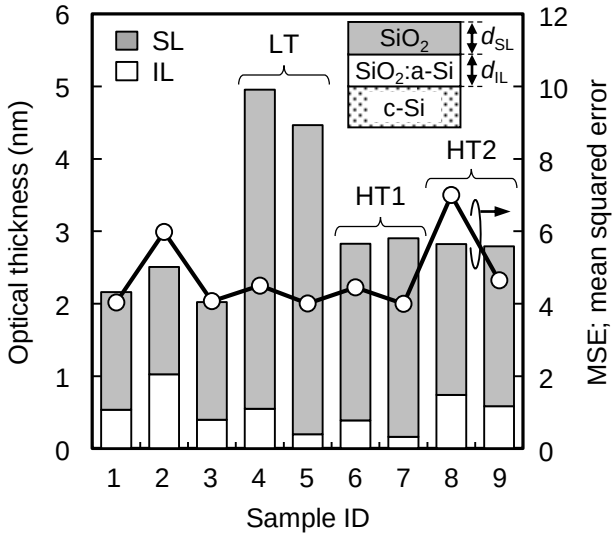



Figure 4.5 Estimated thicknesses ($d_{SL}$ and $d_{IL}$) of samples 1–9; an optical model used for the SE analysis is shown in the inset.

The O, C, and F depth profiles obtained using TOF–SIMS are shown in Figs 4.6(a)–4.6(c). The plasma processing steps introduced the detected impurities. The O atomic concentration profile varied depending on post-PE treatments; the number of O atoms near the Si substrate surface increased in samples 4–9, corresponding to the increased thickness of the oxidized layer. The increased O density was significant for the samples treated using LT CDE (ID 4 and 5); this result is consistent with the $d_{SL}$ increase determined using SE. Moreover, the C atomic concentration profile changed in response to post-PE treatments; overall, the number of C atoms near the Si substrate surfaces decreased in samples 4–9 and was substantial for samples 4–7.

No significant difference was observed in the O and C profiles of the samples with and without FA treatment. Conversely, significant differences were observed in the F atomic concentration profiles of samples that never underwent FA. The F atomic concentration increased substantially after PE and decreased after each post-PE treatment, in particular after FA (ID 3, 5, 7, and 9). As discussed in Chapter 3, the diffusion of F atoms in the damaged Si structure is anticipated to be primarily governed by the FA treatment. F atoms are considered to be diffused out from the Si surface or into Si substrate during the annealing process.[21] The reduction of C and F after CDE is consistent with previously reported data.[13]

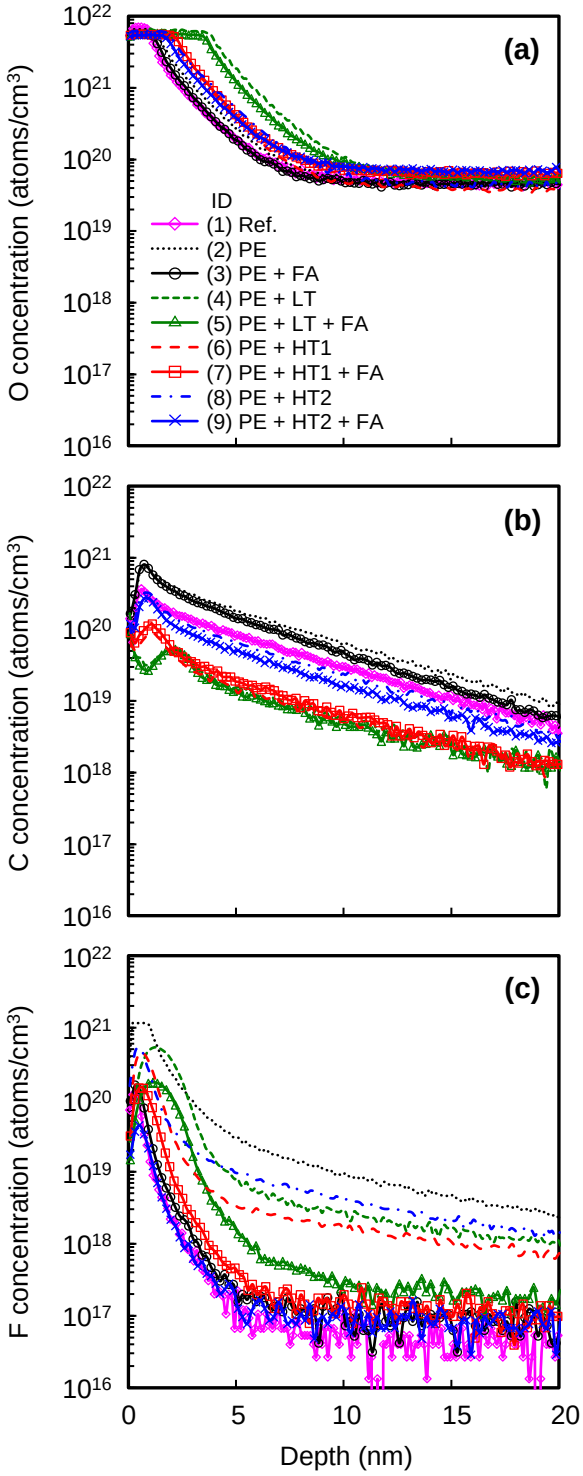



Figure 4.6 Impurity profiles obtained using TOF–SIMS after PE, CDE treatment, and FA treatment; depth profiles of (a) O, (b) C, and (c) F atoms.

The $C_p$–$V_b$ and $1/C_p^2$–$V_b$ curves for all Type-A samples are shown in Figs. 4.7(a) and 4.7(b), respectively; $C_p$ is the measured parallel capacitance and $V_b$ is the applied bias voltage. Flat-band voltage ($V_{FB}$)[22,23] shifts were observed in all etched samples, as shown in Fig. 4.7(a) and the $V_{FB}$ shift was not completely recovered after FA. Moreover, the capacitance in the accumulation region decreased for all CDE samples, corresponding to the increase in the $d_{SL}$ shown in Fig. 4.5. By introducing the density of defects, $n_{dam}$, the differential capacitance can be expressed as:

$$\frac{d}{dV_b}\left(\frac{1}{C_p^2}\right) = \frac{2}{q\varepsilon_0\varepsilon_{Si}(N_A + n_{dam})}, \tag{4.1}$$

where $\varepsilon_{Si}$ is the relative dielectric constant of the Si substrate, $\varepsilon_0$ is the permittivity in vacuum, and $N_A$ is the p-type doping density. The slope of $1/C_p^2$–$V_b$ defines $N_A + n_{dam}$.

In Fig. 4.7(b), changes in the slope correspond to the presence of defects site;[10] thus, the differences in the slopes of the reference sample (ID 1) and the other samples (ID 2–9) indicate the differences in the defect density of Si substrates. The slopes of $1/C_p^2$–$V_b$ are shown in Fig. 4.7(c). Without FA, the slope of the plasma-etched sample (ID 2) was slightly less than those of the CDE samples (ID 4, 6, and 8), implying that CDE influences the density of defects in damaged Si substrates. Therefore, the defects created by PE were removed and/or reconstructed by the CDE. When the samples underwent FA, the slope of the plasma-etched sample (ID 3) was less than those of the CDE samples (ID 5, 7, and 9). The slopes of the $1/C_p^2$–$V_b$ plot are correlated with the defect density in the IL region and the capacitance in the depletion layer; thus, it is anticipated that the defects in the IL region were reconstructed (recovered) by FA and resulted in a decrease in ($d_{IL}$ + $d_{SL}$). This decrease effectively induced an increase in leakage current, which modulated the $C_p$–$V_b$ characteristics.

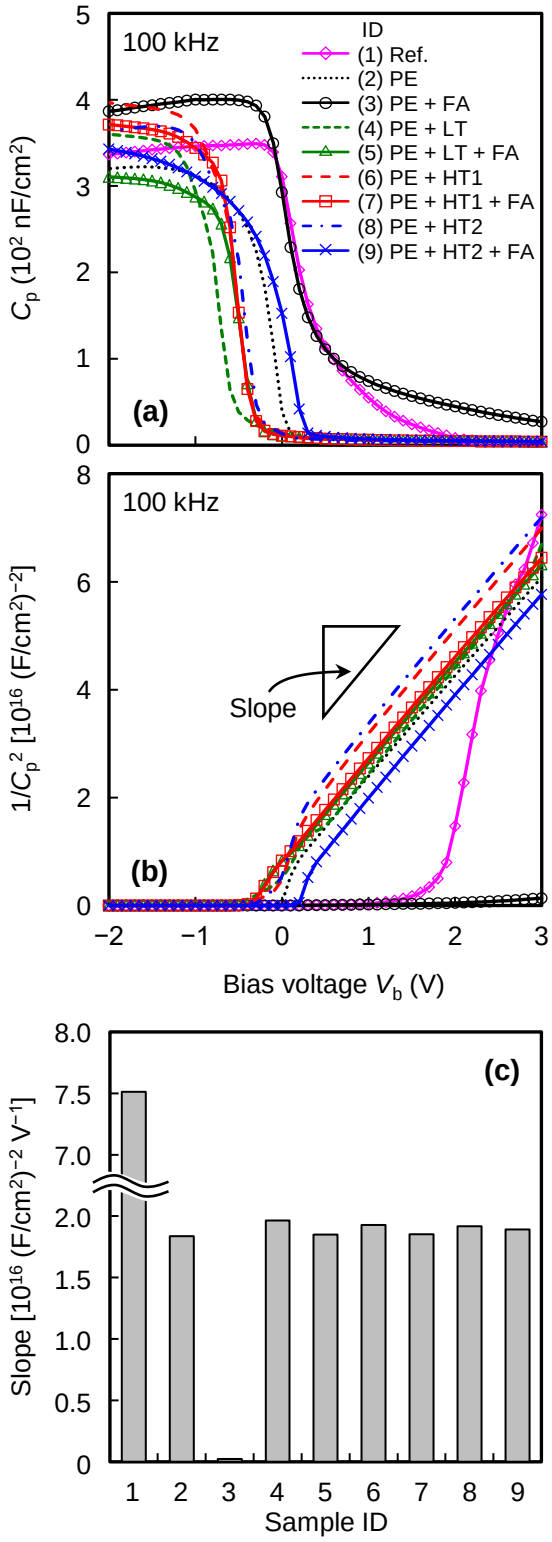



Figure 4.7 (a) $C_p$–$V_b$ curves for Type-A samples 1–9 obtained at a modulation frequency of 100 kHz. (b) $1/C_p^2$-$V_b$ curves. (c) Slopes of $1/C_p^2$–$V_b$.

The relationship between the O, C, and F atomic concentrations ($n_O$, $n_C$, and $n_F$) at a depth of 1 nm, measured using TOF–SIMS and the $V_{FB}$ shift are shown in Fig. 4.8. As the $V_{FB}$ shifted to negative voltages, $n_O$ and $n_F$ increased. The slope of $n_F$ versus $V_{FB}$ was larger than that of $n_O$ versus $V_{FB}$, which may indicate that the F atoms in the damaged region play a more dominant role in the $V_{FB}$ shift compared with the oxidation of the damaged layer surface by $n_O$. The Si–F bond energy is responsible for the $V_{FB}$ shift by $n_F$. Based on previous studies,[24,25] the presence of F-related defects significantly induces the shift of $V_{FB}$ because of the change in electron trapping and detrapping behaviors around F atoms. The $V_{FB}$ shift of the plasma-etched sample (ID 2) is only slightly negative, although the $n_F$ value was high. A possible mechanism may be attributed to a large number of carrier trapping and detrapping sites in the plasma-etched damaged layer of sample 2 without the CDE treatment or the FA. The Si surface in sample 2 is severely damaged compared with other samples. Therefore, the severely damaged region comprising F-related defects in sample 2 may modulate the electron trapping and detrapping mechanisms in the *C–V* measurement. Notably, the depth profile of $n_F$ modifies the capacitance of the damaged region in response to $V_b$. Further studies are required to understand the mechanisms controlling F retention by plasma-etched samples. Based on the results of this study, understanding the dynamic behavior of F atoms in the damaged region is extremely relevant to controlling and suppressing PPD in Si substrates.

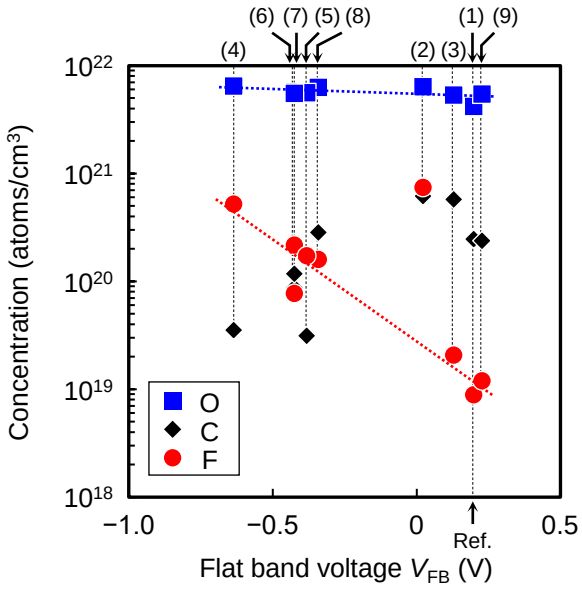



Figure 4.8 Relationship between O, C, and F atomic concentrations ($n_O$, $n_C$, and $n_F$) at a depth of 1 nm in the Si substrate, measured using TOF–SIMS and the $V_{FB}$ shift.

Representative CL spectra and TO-line peak intensity of samples 1–3, 5, and 9 are shown in Figs. 4.9(a) and 4.9(b), respectively. To investigate the effect of CDE, CL analyses were performed under two conditions with different gas mixtures, LT CDE and HT2 CDE. A 10-nm thick passivation film was formed on the Si substrate prior to the FA treatment for CL analyses; sample 1 was used as the reference. In general, the depth of electron beam penetration in samples with a passivation film was shallower than those in the Si substrate without a passivation film. Two emission lines, labeled TO and TO+O$^{\Gamma}$, were observed for all samples [Fig. 4.9(a)]. These lines correspond to the emissions of electrons in the band-to-band transition (TO) and optical phonons at $k = 0$ (O$^{\Gamma}$).[26] The TO-line intensity of the damaged samples was normalized to that of the reference sample (ID

1) to eliminate the effect of the recombination center at the Si surface. The normalized TO-line peak intensity ratios at electron beam acceleration voltages ($V_{CL}$) of 10 and 25 kV are shown in Fig. 4.9(b). The TO-line intensity ratio of sample 2 was significantly less than that of sample 1, indicating that non-radiative recombination centers (defects) were formed in the damaged Si substrate.[27–31] Moreover, the TO-line intensity ratio was lower at a $V_{CL}$ of 10 kV than at 25 kV. This indicates that the density of non-radiative defects was highest near the Si surface and decayed toward the interior. Thus, FA (ID 3) could not fully recover the TO-line intensity ratio.

The increase in TO-line intensity at a $V_{CL}$ of 25 kV was almost identical to that of sample 1 for CDE samples (ID 5 and 9). Furthermore, the TO-line intensity ratio of sample 9 was larger than that of sample 1 at a $V_{CL}$ of 10 kV. This result implies that the HT2 CDE treatment formed an HTO film on the Si substrate, which decreased the number of surface recombination centers at the $SiO_2$/Si interface. Thus, CDE after plasma exposure was expected to reconstruct the structures damaged by PPD.

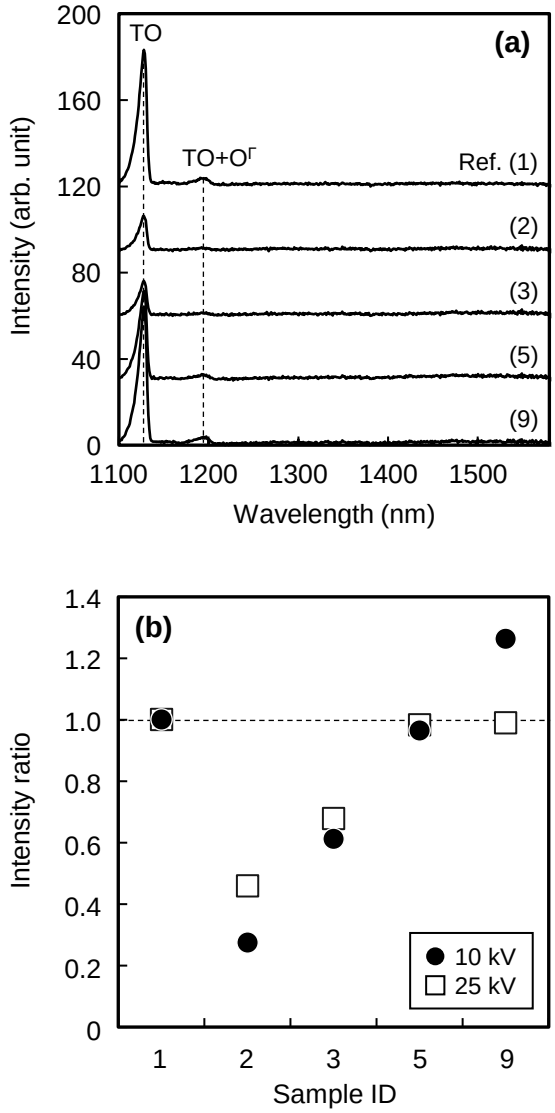



Figure 4.9 (a) Representative CL spectra of samples 1–3, 5, and 9 at an electron beam acceleration voltage ($V_{CL}$) of 10 kV. Two characteristic emission peaks, labeled TO and TO+O$^{\Gamma}$, are observed for all samples. (b) Normalized TO-line peak intensity ratios at $V_{CL}$ = 10 and 25 kV.

### 4.3.2 PPD assessment in the vertical and lateral directions

Three device structures with different oxide film thicknesses ($T_{ox}$) were designed to control the amount of PPD. Representative cross-sectional TEM images of the poly-Si–Si systems (Fig. 4.1) are shown in Figs. 4.10(a)–4.10(c); the $T_{ox}$ of the samples in Figs. 4.10(a)–4.10(c) are 60, 42, and 60 nm, respectively. The device with the thinnest oxide film exhibited the highest degree of PPD. The variation in $d_R$ after plasma etching is shown in Fig. 4.10(a) and 4.10(b) ($d_R$ = 11 and 22 nm, respectively). The TEM image of the sample that underwent HT2 CDE treatment ($d_R$ = 13 nm) is shown in Fig. 4.10(c). The morphology (roughness) at the interface between the poly-Si and the Si substrate increased in the sample with HT2 CDE treatment, which is similar to Type-A sample 8 [Fig. 4.4(c)].

The leakage current ($I_{leak}$) of p–n junctions as a function of $V_{rev}$ for Type-C devices I–III is shown in Fig. 4.11(a); *I–V* measurements were performed at 60 °C. $I_{leak}$ increased as $D_{pn}$ decreased and the differences in $I_{leak}$ were larger when $D_{pn}$ = 0 nm, postulating that increasing the number of defect sites ($n_{dam}$) increases $I_{leak}$ (= $I_L$). The $I_{leak}$ was lowest in device III, which agrees with the CL results [Fig. 4.9(b)].

$I_{leak}$ at $V_{rev}$ = 1 V as a function of $D_{pn}$ is shown in Fig. 4.11(b), which illustrates that $I_{leak}$ rapidly decreases as $D_{pn}$ approaches 90 nm. The dependence of $I_{leak}$ on $D_{pn}$ indicates that defects created in the lateral direction—presumably induced by stochastic straggling of impurities—can be quantitatively evaluated using the proposed devices. Thus, the implementation of the devices with different $D_{pn}$ is crucial to identify the PPD observed in the lateral direction. The aforementioned results regarding an increase in $I_L$ imply the presence of defects induced by plasma etching.

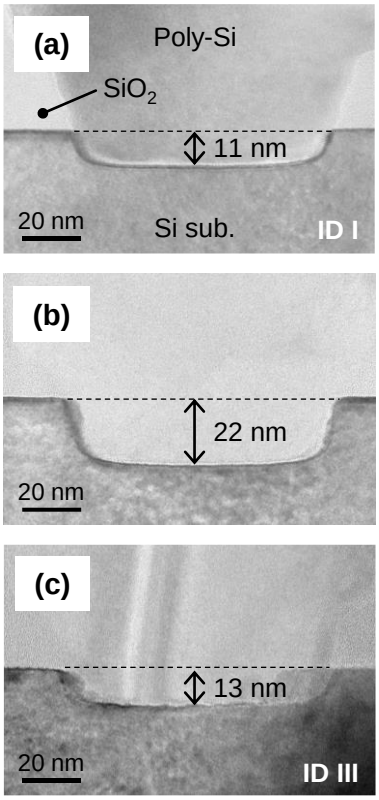



Figure 4.10 Representative cross-sectional TEM images of poly-Si–Si systems. The $T_{ox}$ of the samples are (a) 60 nm (without CDE treatment), (b) 42 nm (without CDE treatment), and (c) 60 nm (with HT2 CDE treatment).

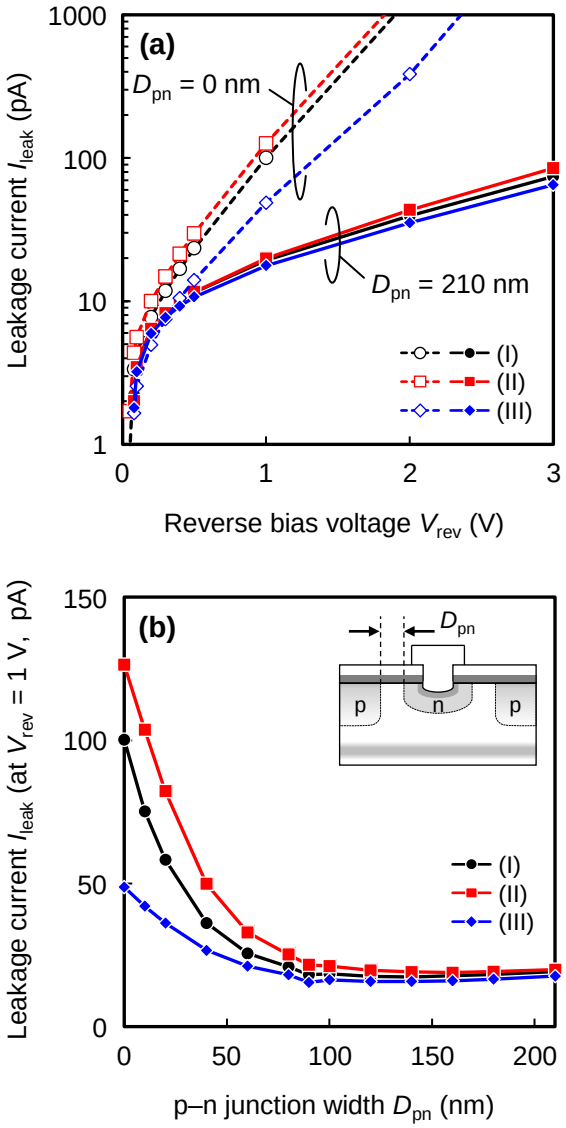



Figure 4.11 Leakage current of p–n junctions in Type-C devices I–III, as a function of (a) $V_{rev}$ at $D_{pn}$ = 0 and 210 nm, and (b) $D_{pn}$ at $V_{rev}$ = 1 V. *I–V* measurements were performed at 60 °C.

The temperature dependence of $I_{leak}$ was investigated to determine the nature of the defects, that is, the resultant conduction mechanism of damaged p–n junctions. The reverse-biased *I–V* curves of two p–n junction distances at temperatures ($T_{sub}$) ranging from 25 to 80 °C (ID I) are shown in Fig. 4.12(a). As $T_{sub}$ increases, $I_{leak}$ increases for $D_{pn}$ = 0 and 210 nm. The observed $T_{sub}$-dependence is attributed to carrier conduction (tunneling) through the p–n junction rather than along the $SiO_2$/Si interface.[32]

The activation energies ($E_a$) for $D_{pn}$ = 0 and 210 nm were determined to be 0.46–0.51 eV and 0.67 eV, respectively [Fig. 4.12(b)]. When $D_{pn}$ = 0 nm, the estimated $E_a$ of 0.46–0.51 eV is close to half of the Si bandgap energy ($E_g/2$ = 0.56 eV); therefore, the dominant conduction mechanism is the recombination of carriers in the depletion layer.[23,32] When $D_{pn}$ = 210 nm, the estimated $E_a$ of 0.67 eV is larger than $E_g/2$. This may imply that $I_{leak}$ comprises two conduction mechanisms, that is, the recombination and diffusion of carriers, although the observed $I_{leak}$ is small.

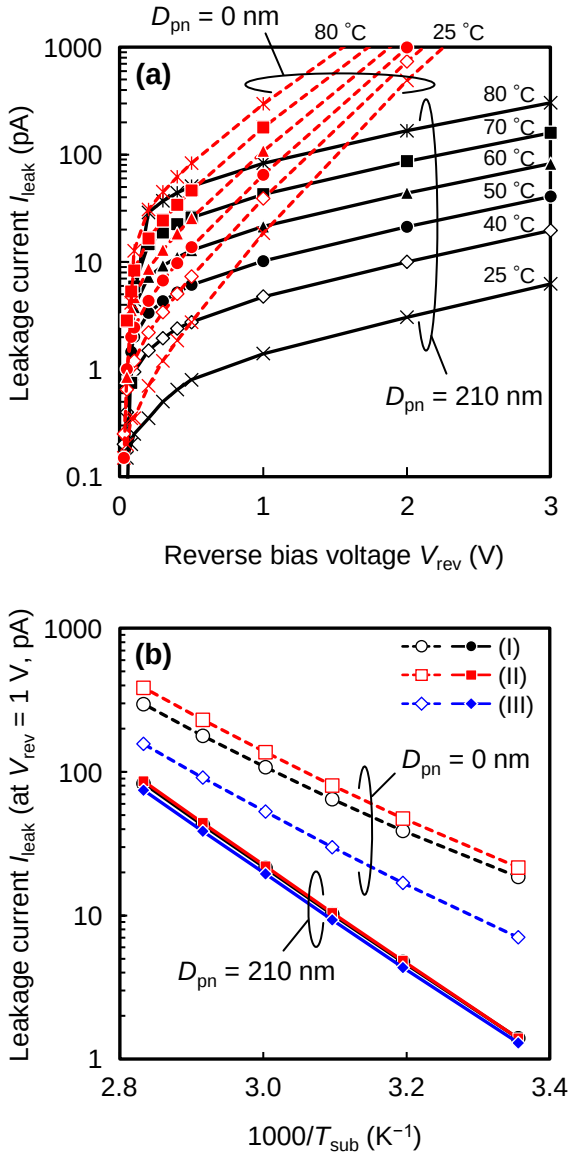



Figure 4.12 (a) Reverse-biased *I–V* curves of two p–n junction distances at temperatures ranging from 25 to 80 °C (ID I), and (b) Arrhenius plots for $D_{pn}$ = 0 nm and 210 nm (ID I–III).

As the defect profile is controlled by changing $d_R$, devices with different $d_R$ were fabricated to determine the effects of device structures on defect creation in the vertical and lateral directions. As shown in Figs. 4.10(a) and 4.10(b), the $d_R$ was varied from 11 to 22 nm. $I_V$ measurements were performed for the devices with $D_{pn}$ = 90 nm to suppress $I_L$. The $d_R$-dependence of $I_V$ at $V_{rev}$ = 1 V, normalized to that of the device with $d_R$ = 11 nm is shown in Fig. 4.13. In particular, $I_V$ increased with $d_R$ for device I; this suggests that the $d_R$-dependence of $I_V$ can be attributed to the reduced electrostatic barrier for electron conduction at the vertical p–n junction as $d_R$ increases. The increase in $I_V$ of devices II and III is relatively small compared with that of sample ID I. This difference is attributed to a decrease in the defect density caused by the CDE treatments of devices II and III.

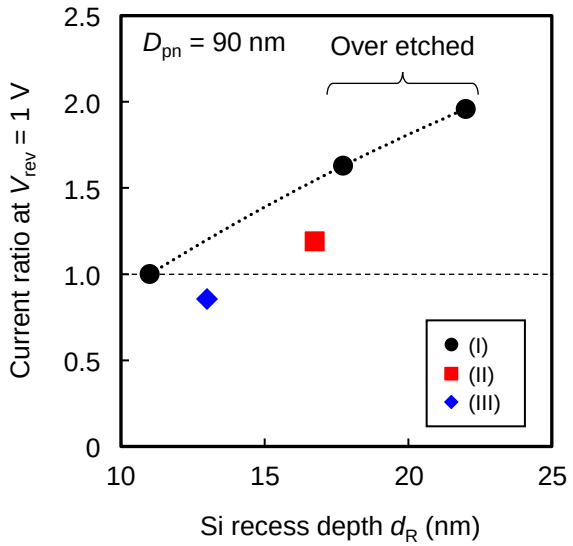



Figure 4.13 $d_R$-dependence of $I_V$ (at $V_{rev}$ = 1 V and $D_{pn}$ = 90 nm) normalized to that of the device with $d_R$ = 11 nm.

The summary of the results obtained in this chapter is shown in Fig. 4.14. As shown in Fig. 4.14(a), devices with different $d_R$ were prepared to evaluate PPD in the vertical direction. $I_V$ was dependent on $d_R$. Moreover, this chapter demonstrated that CDE decreased $I_V$ by either recovering the defect structures or removing the damaged layer; a detailed conduction mechanism for the vertical direction is shown on the right of Fig. 4.14(a). The observed $d_R$-dependence of $I_V$ results from the increase in defects, which reduces the electrostatic barrier.

Devices with different $D_{pn}$ were used to determine the mechanism for lateral defect creation, which is shown on the right in Fig. 4.14(b). Based on *I–V* measurements, $I_L$ increases with a decrease in $D_{pn}$ and the $T_{sub}$-dependence of $I_L$ was attributed to carrier conduction (tunneling) through the p–n junction. Thus, $I_L$ increases with $D_{pn}$, that is, the tunneling distance decreases.

The results suggest that PPD in the lateral direction, which is "unexposed" to plasma, results from stochastic straggling of impurity species, as predicted by molecular dynamics simulations.[33] Defects in the vertical and lateral directions serve as a source of leakage current in both directions. Defect creation and leakage current are considered critical problems for low-defect-density devices, such as image sensors. Devices with different lateral p–n junctions should be implemented to broaden our understanding of PPD mechanisms in future 3D devices.

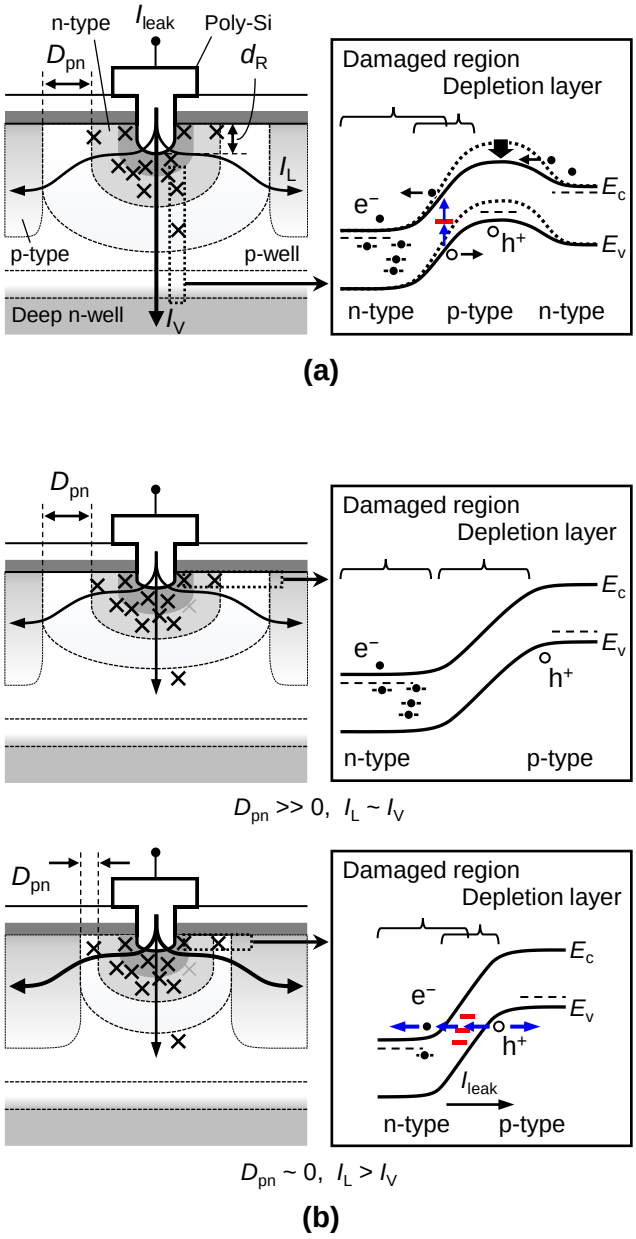



Figure 4.14 Summary of the detailed conduction mechanisms: (a) $I_V$ characterization scheme and (b) $I_V$ and $I_L$ characterization schemes.

## 4.4 Conclusion

Defect creation in the vertical and lateral directions of Si substrates during plasma processing was investigated using devices with different p–n junction structures. Analyses using SE, TOF–SIMS, and CL were conducted to characterize the damaged structures. Defects formation in Si substrates was validated using *C–V* measurements. Based on *I–V* measurements, $I_L$ increased as $D_{pn}$ decreased; the increase in $I_L$ implied the creation of defects in the lateral direction. The conduction mechanism of lateral defects was attributed to carrier tunneling at the p–n junction. Based on the experimental results, PPD occurred both in the vertical and lateral directions owing to the stochastic straggling of impurity species. Devices with lateral p–n junctions are indispensable to understanding PPD mechanisms and designing future electronic devices sensitive to the presence of latent defects.

**References**

[1] H. Fujiwara, *Spectroscopic Ellipsometry: Principles and Applications* (John Wiley & Sons, West Sussex, 2007).

[2] A. Matsuda, Y. Nakakubo, Y. Takao, K. Eriguchi, and K. Ono, Thin Solid Films **518**, 3481 (2010).

[3] Y. Ishikawa, Y. Ichihashi, S. Yamasaki, and S. Samukawa, J. Appl. Phys. **104**, 063308 (2008).

[4] X. C. Mu, S. J. Fonash, A. Rohatgi, and J. Rieger, Appl. Phys. Lett. **48**, 1147 (1986).

[5] K. T. Sung, S. W. Pang, M. W. Cole, and N. Pearce, J. Electrochem. Soc. **142**, 206 (1995).

[6] W. Wu and P. K. McLarty, J. Vac. Sci. Technol. A **13**, 67 (1995).

[7] M. Koyama, C. Cheong, K. Yokoyama, and I. Ohdomari, Jpn. J. Appl. Phys. **36**, 6682 (1997).

[8] K. Egashira, K. Eriguchi, and S. Hashimoto, in *Proc. IEEE Int. Electron Devices Meeting*, 1998, pp. 563–565.

[9] Y. Nakakubo, A. Matsuda, M. Fukasawa, Y. Takao, T. Tatsumi, K. Eriguchi, and K. Ono, Jpn. J. Appl. Phys. **49**, 08JD02 (2010).

[10] Y. Nakakubo, K. Eriguchi, and K. Ono, ECS J. Solid State Sci. Technol. **4**, N5077 (2015).

[11] N. Aoto, M. Nakamori, S. Yamasaki, H. Hada, N. Ikarashi, K. Ishida, Y. Teraoka, and I. Nishiyama, J. Appl. Phys. **77**, 3899 (1995).

[12] T. Nakahata, K. Yamamoto, J. Tanimura, T. Inagaki, T. Furukawa, S. Maruno, Y. Tokuda, A. Miyamoto, S. Satoh, and H. Kiyama, J. Cryst. Growth **226**, 443 (2001).

[13] C.-L. Cheng, K.-S. Chang-Liao, and T.-K. Wang, Solid-State Electron. **50**, 103 (2006).

[14] S. Shibata, F. Kawase, A. Kitada, T. Kouzaki, and A. Kitamura, IEEE Trans. Semicond. Manuf. **23**, 545 (2010).

[15] H. Nishino, N. Hayasaka, K. Horioka, J. Shiozawa, S. Nadahara, N. Shooda, Y. Akama, A. Sakai, and H. Okano, J. Appl. Phys. **74**, 1349 (1993).

[16] G. S. Oehrlein, Mater. Sci. Eng. B **4**, 441 (1989).

[17] T. Ohchi, S. Kobayashi, M. Fukasawa, K. Kugimiya, T. Kinoshita, T. Takizawa, S. Hamaguchi, Y. Kamide, and T. Tatsumi, Jpn. J. Appl. Phys. **47**, 5324 (2008).

[18] S. A. Vitale and B. A. Smith, J. Vac. Sci. Technol. B **21**, 2205 (2003).

[19] J. A. Woollam, B. Johs, C. M. Herzinger, J. Hilfiker, R. Synowicki, and C. L. Bungay, in Proc. SPIE **10294**, 1029402 (1999).

[20] Y. Sato, S. Shibata, A. Uedono, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. A **37**, 011304 (2018).

[21] S.-P. Jeng, T.-P. Ma, R. Canteri, M. Anderle, and G. W. Rubloff, Appl. Phys. Lett. **61**, 1310 (1992).

[22] R. Winter, J. Ahn, P. C. McIntyre, and M. Eizenberg, J. Vac. Sci. Technol. B **31**, 030604 (2013).

[23] S. M. Sze and M.-K. Lee, *Semiconductor Devices, Physics and Technology*, 3rd ed. (Wiley, New York, 2012).

[24] M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, and M. Yoneda, in *Proc. IEEE Int. Electron Devices Meeting*, 2005, pp. 413–416.

[25] T. Sasaki, F. Ootsuka, H. Ozaki, T. Hoshi, M. Tomikawa, M. Yasuhira, and T. Arikado, Jpn. J. Appl. Phys. **43**, 1837 (2004).

[26] G. Davies, Phys. Rep. **176**, 83 (1989).

[27] B. G. Yacobi and D. B. Holt, J. Appl. Phys. **59**, R1 (1986).

[28] R. Sugie, T. Mitani, M. Yoshikawa, Y. Iwata, and R. Satoh, Jpn. J. Appl. Phys. **49**, 04DP15 (2010).

[29] R. Sugie, K. Inoue, and M. Yoshikawa, J. Appl. Phys. **112**, 033507 (2012).

[30] A. Sagara, A. Uedono, and S. Shibata, IEEE Trans. Semicond. Manuf. **28**, 92 (2015).

[31] Y. Sato, S. Shibata, R. Sakaida, and K. Eriguchi, in *Ext. Abs. 17th Int. Workshop on Junction Technol.*, 2017, pp. 73–76.

[32] Y. Murakami and T. Shingyouji, J. Appl. Phys. **75**, 3548 (1994).

[33] K. Eriguchi, A. Matsuda, Y. Takao, and K. Ono, Jpn. J. Appl. Phys. **53**, 03DE02 (2014).

# Chapter 5

# Predicting the effect of plasma-induced damage on p–n junction leakage

## 5.1 Introduction

Electrical characterizations are more straightforward than structural analyses in terms of elucidating the effects of plasma-induced damage (PID) on the performance of electronic devices. Electrical analysis techniques, such as current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements, have been employed to characterize damaged structures after plasma etching (PE).[1–7] Historically, PID analyses focus on the creation of defects in the vertical direction. Morimoto et al. investigated the effects of PID on leakage current using device structures with a p–n junction wherein the presence of defects after $N_2/H_2$ PE was evaluated using a vertical p–n junction structure.[8] Similarly, Kuboi et al. investigated the effect of defects created by Si trench etching on the dark current of a CMOS image sensor (CIS).[9] These PID analyses were performed primarily by detecting changes in the leakage current owing to the presence of defects.

With the structural transition of advanced devices from two-dimensional (2D) to three-dimensional (3D), defect creation in the lateral and vertical directions has become crucial in ultra-low leakage devices. Defect creation in the lateral direction is attributed to the stochastic straggling of incident ions.[10–14] The density of defects created in the lateral direction is lower than that in the vertical direction owing to its characteristic

mechanism. The low defect density of lateral PID is a primary reason for the difficulty in its detection. Thus far, two approaches have been employed to assign lateral PIDs: molecular dynamics (MD) simulations and experiments with 3D device structures. In MD simulations, an impinging ion penetrates the crystalline Si region during the etching of a fin structure.[11,12] Based on previous studies, the defect density in the lateral direction is one-tenth that in the vertical or lower, resulting in difficulties in assessing the defect density. Experimentally, preliminary assessments of defects in the lateral direction using devices with a lateral p–n junction as described in Chapter 4 have been performed. The presence of the lateral defects was identified by the change in the leakage current depending on the lateral p–n junction width. However, to design low-leakage devices, such as CISs, a simplified model is required to predict the effect of low-density defects created by the lateral straggling of incident species on the leakage current. Modeling the junction leakage current of a device with PIDs and identifying the presence of defects is critical.

In this chapter, a model focusing on the effects of created defects on p–n junction leakage current density increase ($\Delta J_{pn}$) in combination with technology computer-aided design (TCAD) simulations is proposed. TCAD simulations were performed to precisely assign the profiles of impurity and carrier concentration in the p–n junction regions for various lateral p–n junction widths ($W_{p–n}$). Three defect spatial distributions, $n_{dam}(x)$, (linear, exponential, and Gaussian) were assumed and implemented to predict $\Delta J_{pn}$ by referring to defect distribution reports in the vertical (depth) direction.[6,15,16] $W_{p–n}$-dependence on p–n junction leakage current density ($J_{pn}$) was investigated to examine the effect of $n_{dam}(x)$ on $\Delta J_{pn}$. The prediction model was implemented to experimentally assign defect profiles in devices with lateral p–n junctions exposed to fluorocarbon-containing

plasma in a contact-opening step, that is, defects in Si substrates were created in the contact-opening step. The distribution of defects created in the lateral direction was obtained based on the experimental results of $\Delta J_{pn}$.

## 5.2 Modeling the effect of plasma-induced damage on p–n junction leakage

In this chapter, simulation parameters, which determine the doping profiles, were calibrated using the results of secondary ion mass spectrometry (SIMS) analysis of blanket wafers considering ion implantation and subsequent thermal processes. Synopsys Sentaurus TCAD simulations were performed using the parameters obtained to precisely assign the carrier concentration profiles in the p–n junction regions for various $W_{p–n}$. The impurity profiles of the p–n junction regions were obtained in advance using the TCAD simulation. Defects were introduced as impurities to induce carrier trapping and detrapping, with reference to a previous study.[6] The effects of $n_{dam}(x)$ on the depletion region width ($W_{dep}$) and maximum electric field ($F_m$) in p–n junctions were estimated. The relationship between $n_{dam}(x)$ and $J_{pn}$ was determined using $W_{dep}$ and $F_m$. $W_{p–n}$-dependence on $J_{pn}$ and $V_{pn}$-dependence on $J_{pn}$ for three defect spatial distributions and an increase in $J_{pn}$ owing to defects under the operating conditions were predicted.

### 5.2.1 Model scheme

The schematic of a device structure with the lateral $n^+$–p junction for the TCAD simulation and its energy band diagram are shown in Fig. 5.1(a). The $x$-axis represents the lateral direction along the p–n junction and the $z$-axis, the vertical (depth) direction from the substrate surface. The n-type region was formed by combining arsenic ion implantation and phosphorous diffusion from the poly-Si film in the contact hole, whereas

the p-type region was formed by boron ion implantation. The parameters employed in the TCAD simulation are listed in Table 5.1. The diameter ($\Phi$) at the bottom of the contact-opening area and the Si recess depth ($d_R$) were set to 80 and 15 nm, respectively. The detailed process flow employed for the TCAD simulation is shown in Fig. 2.4. An example of the carrier profile obtained using the TCAD simulation for a device structure with $W_{p-n}$ = 90 nm is shown in Fig. 5.1(b).

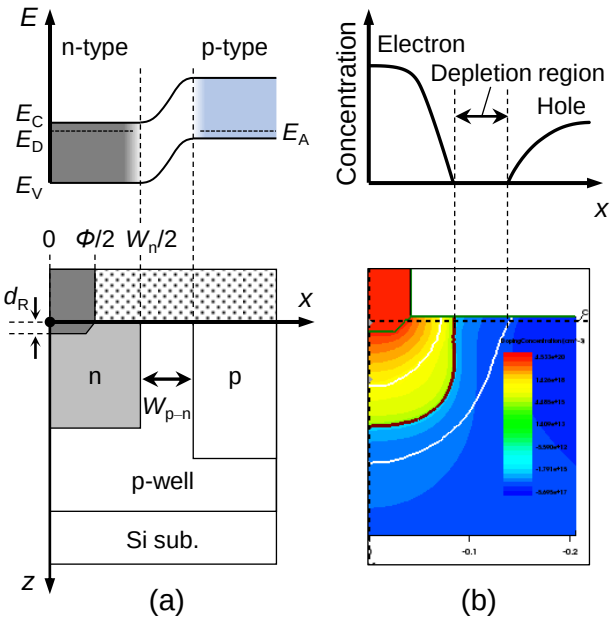



Figure 5.1 (a) Schematic of the device structure with $n^+$–p junction for the TCAD simulation and its energy band diagram. (b) Carrier profile obtained using the TCAD simulation for a device structure with $W_{p-n}$ = 90 nm.

Table 5.1 Parameters employed in the TCAD simulations.

| | |
|---|---|
| P-well ion implantation (I/I) | B 100 keV, $4 \times 10^{12}$ cm$^{-2}$, 7° tilt |
| N-type I/I | As 100 keV, $1 \times 10^{12}$ cm$^{-2}$, 0° tilt |
| P-type I/I (of two steps) | B 50 keV, $3 \times 10^{12}$ cm$^{-2}$, 0° tilt<br>B 10 keV, $6 \times 10^{12}$ cm$^{-2}$, 0° tilt |
| Annealing after I/I | 1050 °C rapid thermal annealing |
| N-type region width | $W_n$ = 160 nm |
| Contact hole diameter | $\Phi$ = 80 nm |
| Si recess depth | $d_R$ = 15 nm |
| Phosphorus concentration of poly-Si film | $7.0 \times 10^{20}$ cm$^{-3}$ |
| Annealing after poly-Si deposition | 850 °C, 10 min |

The implemented impurity (donor and acceptor) and estimated carrier (electron and hole) profiles at $z$ = 5 nm for various $W_{p–n}$ (0, 60, 90, 120, and 180 nm) in the TCAD simulations are shown in Fig. 5.2(a) and 5.2(b). A region of high electron concentration is formed at the bottom of the contact-opening area owing to phosphorus diffusion from the P-doped poly-Si film. The electron concentration ($\approx 2.5 \times 10^{20}$ cm$^{-3}$) at the bottom of the contact-opening area was considerably higher than the hole concentration ($\approx 4 \times 10^{17}$ cm$^{-3}$) in the p-type region. The hole concentration near the p–n junction decreased as $W_{p–n}$ increased. The distance between the electron and hole regions, that is, the depletion region width, increased with $W_{p–n}$. The depletion region extended to the p-type region as $W_{p–n}$ increased.

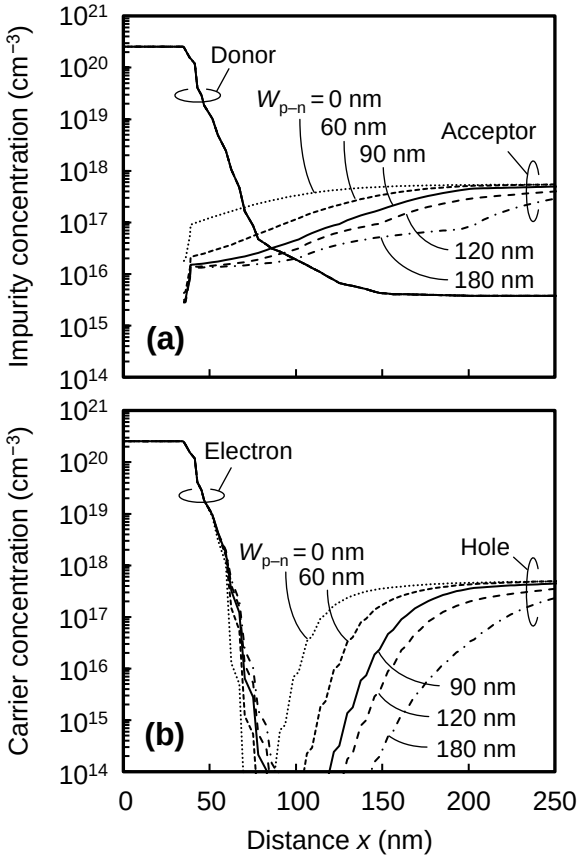



Figure 5.2 (a) Impurity (donor and acceptor) and (b) Carrier (electron and hole) profiles at $z$ = 5 nm in Si substrates for various $W_{p-n}$ (0, 60, 90, 120, and 180 nm) obtained using the TCAD simulation.

The creation of defects in Si substrates during plasma etching is shown in Fig. 5.3(a). As discussed in Chapter 4, the defects are assumed to be created both in the vertical direction and lateral direction underneath the mask through a stochastic process called the straggling of incident ions.[11,12] These defects create trap levels ($E_t$) in the energy band gap of Si. The presence of defects can be evaluated based on the change in the leakage current of the p–n junction structure with various defects located in the energy band gap.[13] The

carrier conduction mechanism via $E_t$ in the p–n junction was investigated based on the Shockley–Read–Hall (SRH) model.[17] A reverse bias voltage ($V_{pn}$) was applied to the p–n junction. The carrier recombination–generation process via $E_t$ was enhanced by $F_m$ in the p–n junction. The three types of spatial defect distribution assumed in this study: (I) linear distribution, (II) exponential distribution, and (III) Gaussian distribution are shown in Fig. 5.3(b). Each distribution of defects is expressed as follows:

$$n_{dam}(x) = n_0\left(1 - \frac{x}{\lambda}\right), \tag{5.1}$$

$$n_{dam}(x) = n_0 \exp\left(-\frac{x}{\lambda}\right), \tag{5.2}$$

$$n_{dam}(x) = \frac{N_{peak}}{\sqrt{2\pi}\sigma} \exp\left(-\frac{x^2}{2\sigma^2}\right) \equiv n_0 \exp\left(-\frac{x^2}{2\lambda^2}\right), \tag{5.3}$$

where $n_0$ [$cm^{-3}$] and $N_{peak}$ [$cm^{-2}$] represent the peak densities introduced in the respective distribution type. $\lambda$ and $\sigma$ are characteristic lengths that define the spatial distribution of defects. Notably, the peak density of defect distributions can be expressed as $n_0$ because a damaged layer is typically removed by WE following plasma exposure. The defect density near the Si substrate surface created by PE is approximately $10^{18}$ $cm^{-3}$.[6] Because the defect density in the lateral direction created by PE was expected to be lower than $10^{18}$ $cm^{-3}$, $1 \times 10^{17}$ $cm^{-3}$ was adopted as the value of $n_0$. The three types of spatial defect distribution $n_{dam}(x)$ in the Si substrate for various $\lambda$ (10, 20, 40, 100, and 1000 nm) are shown in Fig. 5.4. The impact of PPD on the development of the depletion region is discussed in the following subsection.

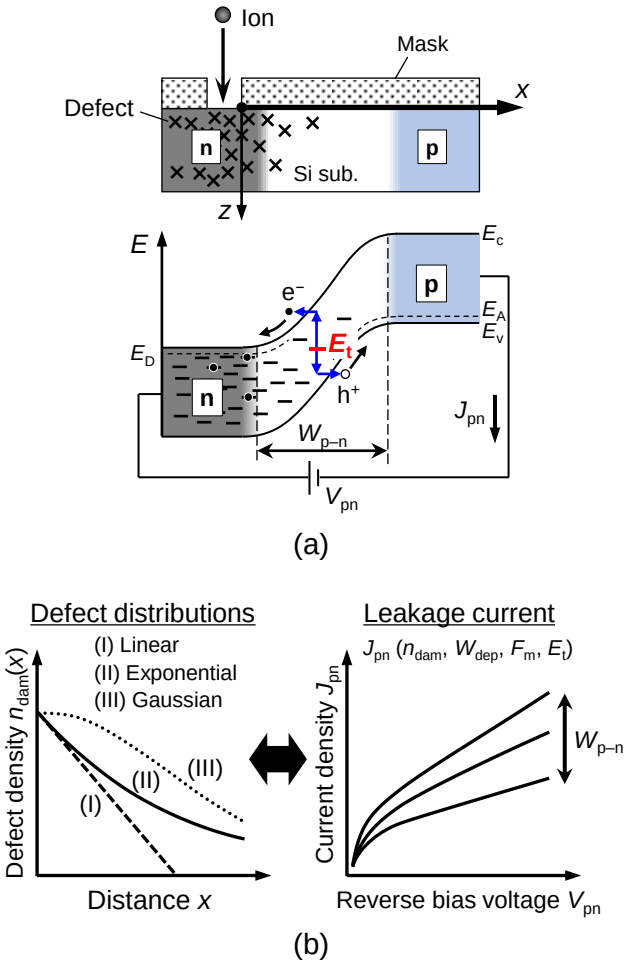



Figure 5.3 (a) Schematic of defect creation in a p–n junction structure by plasma exposure and its energy band diagram. Trap levels ($E_t$) are created in the energy bandgap of Si through plasma exposure. (b) Schematic to predict the effect of defect spatial distributions $n_{dam}(x)$ on $J_{pn}$. Three defect spatial distributions—(I) linear, (II) exponential, and (III) Gaussian—were assumed.

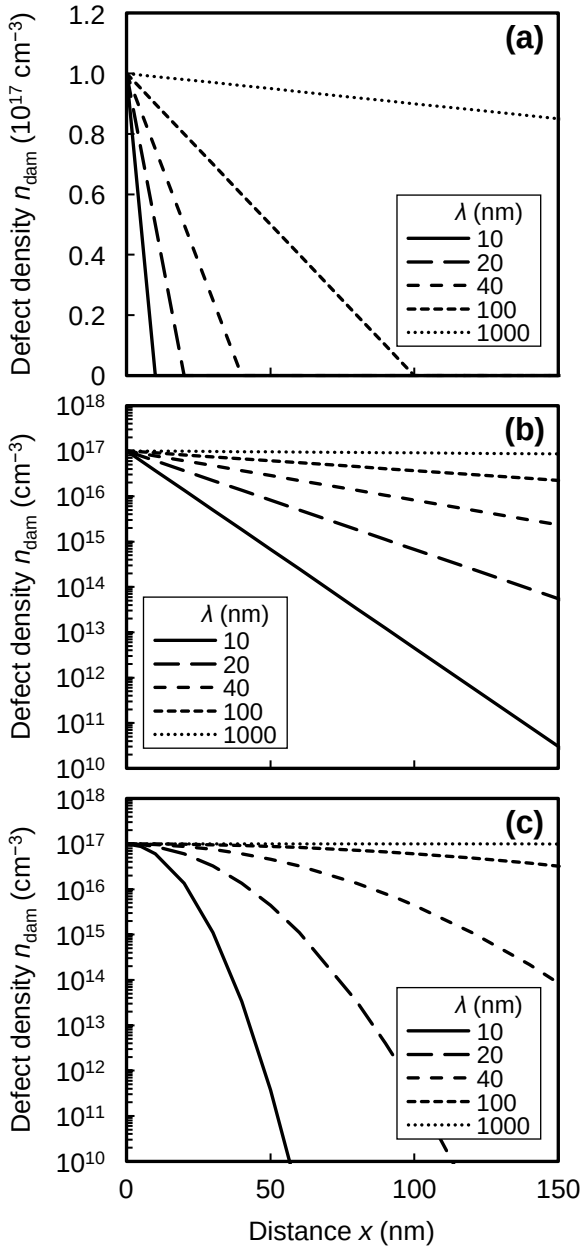



Figure 5.4 Three types of spatial defect distribution $n_{dam}(x)$ in the Si substrate assumed by (a) linear, (b) exponential, and (c) Gaussian.

### 5.2.2 PPD impact on the development of the depletion region

In this subsection, the impact of three defect spatial distributions on the development of depletion region was investigated. The impurity concentration near the p–n junction changed linearly rather than stepwise, as shown in Fig. 5.2(a). A linearly graded p–n junction was assumed to predict the impact of PPD on depletion region development. The reverse bias voltage ($V_{pn}$) dependence on $W_{dep}$ in a linearly graded p–n junction is expressed as follows:[18]

$$W_{dep} = \left[\frac{12\varepsilon_0\varepsilon_s\left(V_{bi}+V_{pn}\right)}{q\alpha}\right]^{\frac{1}{3}}, \tag{5.4}$$

where $\varepsilon_0$ is the permittivity in a vacuum, $\varepsilon_s$ is the relative dielectric constant of Si, $V_{bi}$ is the built-in potential, $q$ is the elementary charge, and $\alpha$ is the impurity gradient. The depletion region expands to the p-type region when the donor concentration ($N_D$) is considerably higher than the acceptor concentration ($N_A$). The impurity gradient in the p–n junction can be approximated as follows:

$$\alpha \approx \frac{dN_A(x)}{dx}. \tag{5.5}$$

Assuming that the defect site with a density of $n_{dam}(x)$ is created along the $x$-axis (lateral direction) by plasma exposure, the impurity gradient in a damaged region is expressed as

$$\alpha \approx \frac{d[N_A(x)+n_{dam}(x)]}{dx}. \tag{5.6}$$

$W_{dep}$ in the presence of defects can be calculated using Eqs. (5.4) and (5.6). The profile of the acceptor $N_A(x)$ in the p–n junction was investigated. The $N_A(x)$ profile for various $W_{p–n}$ (0, 60, 90, 120, and 180 nm) is shown in Fig. 5.5. The value of $N_A(x)$ represents the concentration at the right edge of the depletion region. The impurity gradient of $N_A(x)$ is shown on the right $y$-axis in Fig. 5.5.

$W_{dep}$ depends on both $W_{p–n}$ and $V_{pn}$ (dominantly on $V_{pn}$ under bias). $V_{pn}$ was

maintained at 1 V such that $F_m$ in the p–n junction was less than $10^6$ V/cm, even when $W_{p–n}$ was 0 nm. The estimated $W_{dep}$ as a function of $\lambda$ for various values of $W_{p–n}$ (0, 10, 20, 40, and 100 nm) for the three types of defect spatial distributions at $V_{pn}$ = 1 V is shown in Fig. 5.6. The defect distributions influence the development of the depletion region in the p–n junction. The impurity concentration in the p–n junction increases with $\lambda$, resulting in a decrease in $W_{dep}$. The difference in $W_{dep}$ for the three types of defect spatial distributions increases with an increase in $W_{p–n}$. The schematics of the three types of defect spatial distributions for small and large values of $\lambda$ are shown in Figs. 5.7(a) and 5.7(b), respectively. Note that $n_{dam}(x)$ is a function of $\lambda$ as expressed in Eqs. (5.1)–(5.3). As shown in Fig. 5.7(b), when the value of $\lambda$ is large (e.g., $\lambda$ = 100 nm), the difference in $n_{dam}(x)$ for each distribution is larger at $x_2$ than at $x_1$. An appropriate $W_{p–n}$ should be adopted based on the $\lambda$ value to discuss the effects of defect spatial distributions on $J_{pn}$. In this study, two cases—(1) $\lambda$ = 10 nm, $W_{p–n}$ = 10 nm and (2) $\lambda$ = 100 nm—for $W_{p–n}$ = 100 nm were considered.

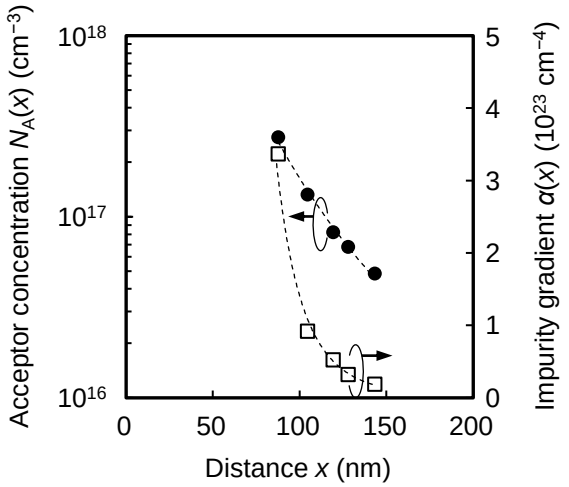



Figure 5.5 Acceptor profile $N_A(x)$ in the $n^+$–p junction for various $W_{p–n}$ (0, 60, 90, 120, and 180 nm). The impurity gradient ($\alpha$) of $N_A$ is shown on the right $y$-axis.

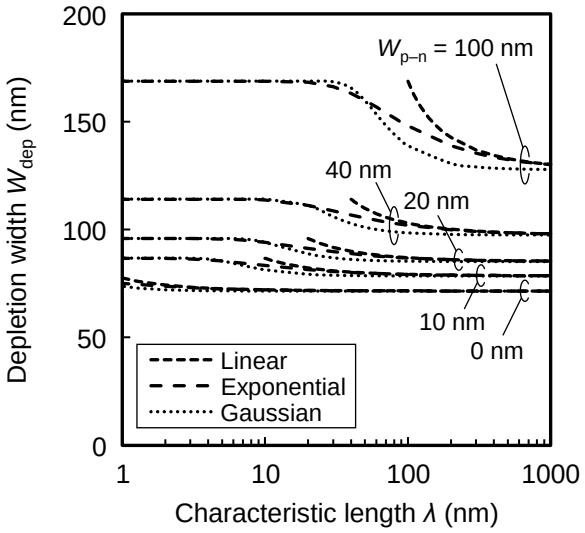



Figure 5.6 Predicted $W_{dep}$ as a function of $\lambda$ for various $W_{p–n}$ (0, 10, 20, 40, and 100 nm) at $V_{pn}$ = 1 V. The peak density $n_0$ was set to $1 \times 10^{17}$ cm$^{-3}$.

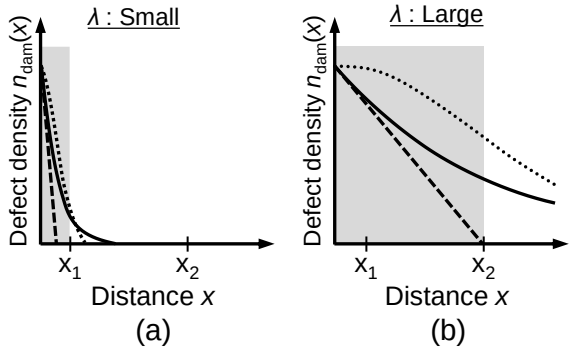



Figure 5.7 Schematics of the three types of defect spatial distributions for (a) small value of $\lambda$ (e.g., $\lambda$ = 10 nm) and (b) large value of $\lambda$ (e.g., $\lambda$ = 100 nm).

The estimated $W_{dep}$ as a function of $W_{p–n}$ and $V_{pn}$ are shown in Fig. 5.8(a) and 5.8(b), respectively, for the three types of defect spatial distributions as well as $W_{dep}$ without defects. In both cases: (1) λ = 10 nm and (2) 100 nm, $W_{dep}$ for the three defect

distributions was smaller than that for the case without defects. The decrease in $W_{dep}$ is attributed to an increase in impurity concentration in the p–n junction resulting from the presence of defects. $W_{dep}$ changes with defect spatial distributions along with the $\lambda$ values. $W_{dep}$ for the Gaussian distribution was the smallest among the three distributions owing to its larger half-width at half-maximum compared with other defect distributions.

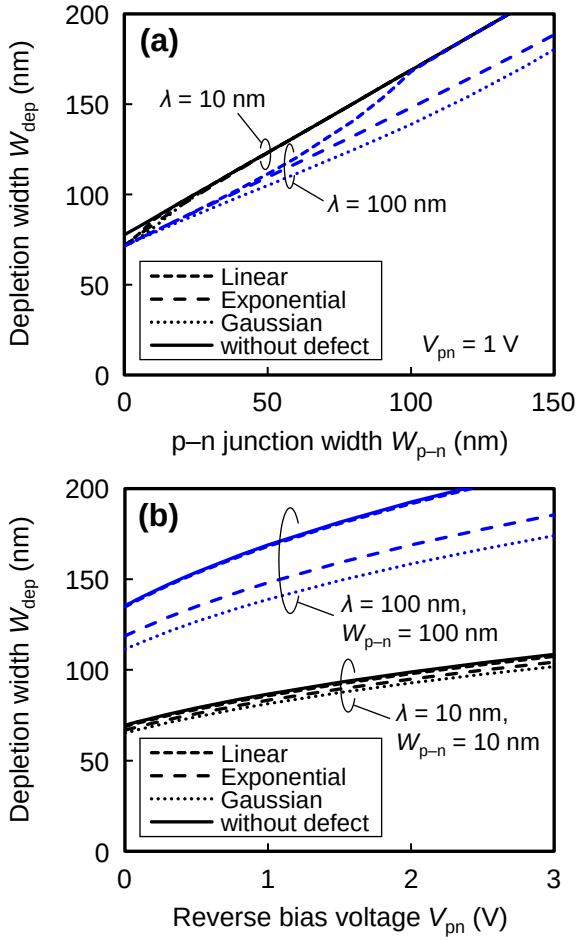



Figure 5.8 (a) Predicted $W_{dep}$–$W_{p–n}$ curves for two cases of $\lambda$ = 10 and 100 nm at $V_{pn}$ = 1 V. (b) Predicted $W_{dep}$–$V_{pn}$ curves for two cases of $\lambda = W_{p–n}$ = 10 and 100 nm. The peak density $n_0$ was set to $1 \times 10^{17}$ cm$^{-3}$.

### 5.2.3 Bias dependence of the leakage current

The effect of PPD on $J_{pn}$ was investigated by considering changes in $W_{dep}$ and $F_m$ of the p–n junction in the presence of defects. Assuming that $J_{pn}$ under the condition of $F_m < 10^5$–$10^6$ V/cm is composed of the SRH generation current density ($J_{SRH}$)[17,19–21] and trap-assisted tunneling (TAT) current density ($J_{TAT}$)[22,23], $J_{pn}$ is expressed as follows:[24–27]

$$J_{pn} \sim J_{SRH} + J_{TAT}. \tag{5.7}$$

For simplicity, we assumed that $n_t$ is equal to the defect density ($n_{dam}$) created by plasma exposure and capture cross-section ($\sigma_0$) in Eq. (2.16) is $1.0 \times 10^{-16}$ cm$^2$ as estimated from the atomic vacancy size of Si ($\approx 10^{-8}$ cm).[14,18] The approximation in Eq. (5.7) is validated below using experimental data.

The estimated Γ as a function of $\lambda$ for various $W_{p–n}$ (0, 10, 20, 40, and 100 nm) at $V_{pn}$ = 1 V is shown in Fig. 5.9(a). As $\lambda$ increases, $W_{dep}$ decreases, increasing Γ. An increase in Γ implies an increase in the ratio of $J_{TAT}$ to $J_{SRH}$ as expressed in Eq. (2.19). For $W_{p–n}$ = 100 nm, the value of Γ is less than 1 ($J_{TAT} < J_{SRH}$) in the range of $\lambda$ = 1–1000 nm. The estimated $J_{pn}$ as a function of $\lambda$ for various $W_{p–n}$ (0, 10, and 100 nm) at $V_{pn}$ = 1 V, with the value of $E_t$ set to 0.7 eV is shown in Fig. 5.9(b). The temperature was assumed to be 60 °C. The difference in $J_{pn}$ of the three defect distribution types originates from the difference in $W_{dep}$ and the corresponding difference in $F_m$. The value of $J_{pn}$ increases with a decrease in $W_{p–n}$ and an increase in $\lambda$. The estimated $J_{pn}$ as a function of $V_{pn}$ for two cases: (1) $\lambda = W_{p–n}$ = 10 nm and (2) $\lambda = W_{p–n}$ = 100 nm is shown in Fig. 5.10. In both cases, the value of $n_{dam}$ is smallest with a linear distribution. Therefore, the $J_{pn}$ in the case of linear distribution was the smallest among the three types of defect distributions.

The estimated $J_{pn}$ as a function of $W_{p–n}$ at $V_{pn}$ = 1 V and $E_t$ = 0.7 eV is shown in

Fig. 5.11. Three cases of $\lambda$ and $n_0$: (1) $\lambda$ = 10 nm, $n_0 = 1 \times 10^{17}$ cm$^{-3}$, (2) $\lambda$ = 100 nm, $n_0 = 1 \times 10^{17}$ cm$^{-3}$, and (3) $\lambda$ = 100 nm, $n_0 = 1 \times 10^{16}$ cm$^{-3}$, are shown. $J_{pn}$ decreases as $W_{p-n}$ increases. $J_{pn}$ in the case of a linear distribution decreases more rapidly with an increasing $W_{p-n}$ than in the other distributions. $W_{p-n}$ dependence of $J_{pn}$ is significantly influenced by the defect spatial distribution $n_{dam}(x)$ and $\lambda$ value. The defect profiles created in the Si substrate by plasma exposure are examined using experimental data.

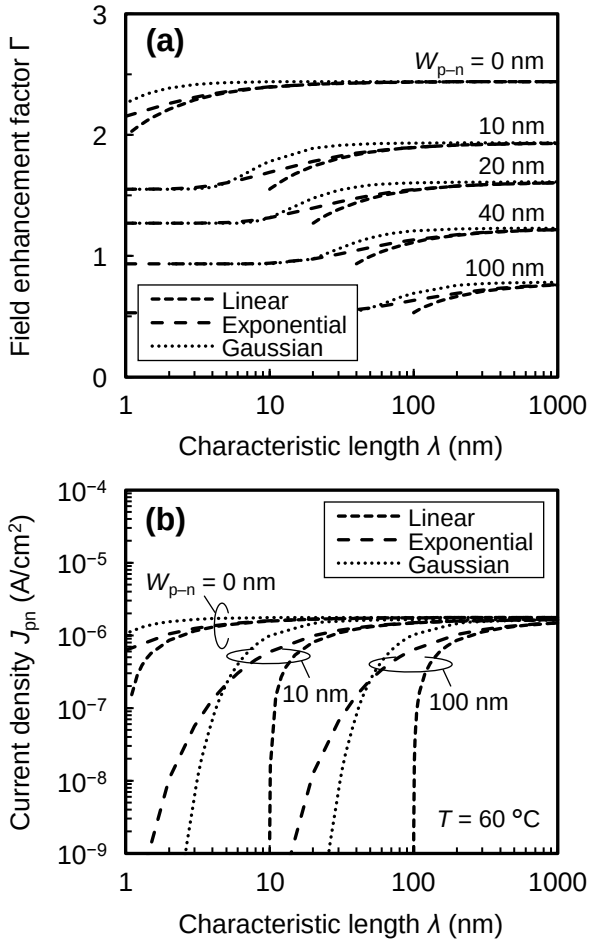



Figure 5.9 Predicted (a) $\Gamma$–$\lambda$ curves on $W_{p-n}$ = 0, 10, 20, 40, and 100 nm at $V_{pn}$ = 1 V ($n_0 = 1 \times 10^{17}$ cm$^{-3}$) and (b) $J_{pn}$–$\lambda$ curves on $W_{p-n}$ = 0, 10, and 100 nm at $V_{pn}$ = 1 V ($n_0 = 1 \times 10^{17}$ cm$^{-3}$, $E_t$ = 0.7 eV).

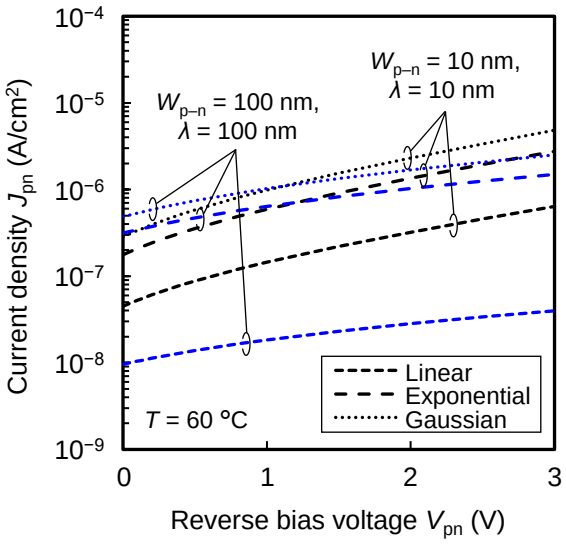



Figure 5.10 Predicted $J_{pn}$–$V_{pn}$ curves for two cases of $\lambda = W_{p-n}$ = 10 and 100 nm ($n_0$ = 1 × $10^{17}$ $cm^{-3}$, $E_t$ = 0.7 eV).

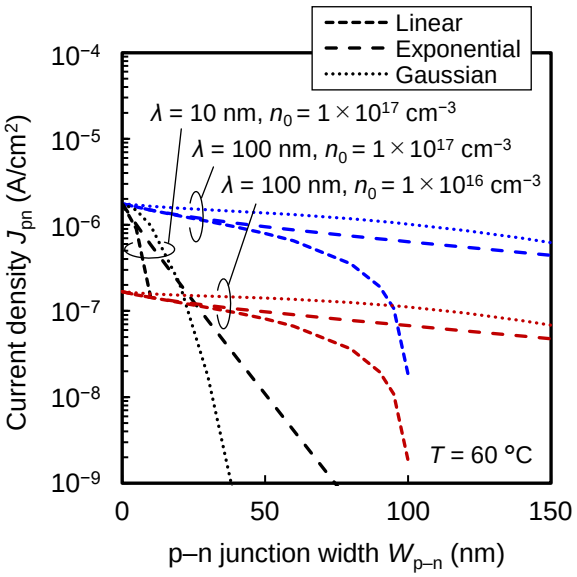



Figure 5.11 Predicted $J_{pn}$–$W_{p-n}$ curves at $V_{pn}$ = 1 V ($E_t$ = 0.7 eV) for three cases of $\lambda$ and $n_0$: (1) $\lambda$ = 10 nm, $n_0$ = 1 × $10^{17}$ $cm^{-3}$, (2) $\lambda$ = 100 nm, $n_0$ = 1 × $10^{17}$ $cm^{-3}$, and (3) $\lambda$ = 100 nm, $n_0$ = 1 × $10^{16}$ $cm^{-3}$.

### 5.2.4 Energy level dependence of the leakage current

The prediction model includes the effects of $E_t$ on $J_{pn}$ as well as the defect spatial distributions $n_{dam}(x)$. The relationship between $E_t$ and $J_{pn}$ ($n_0 = 1 \times 10^{17}$ cm$^{-3}$, $\lambda = W_{p-n} =$ 100 nm) at $V_{pn} = 1$ V for the three types of defect distributions is shown in Fig. 5.12. The value of $J_{SRH}$ is maximum when $E_t$ equals $E_i$ ($\approx 0.58$ eV at $T = 60$ °C) as expressed in Eq. (2.16). The difference in $J_{pn}$ among the three types of defect distributions is attributed to each spatial defect profile. Based on the result, $J_{pn}$ significantly depends on $E_t$ as well as $n_{dam}(x)$. The effect of $E_t$ on $J_{pn}$ and the lateral defect distribution should be predicted.

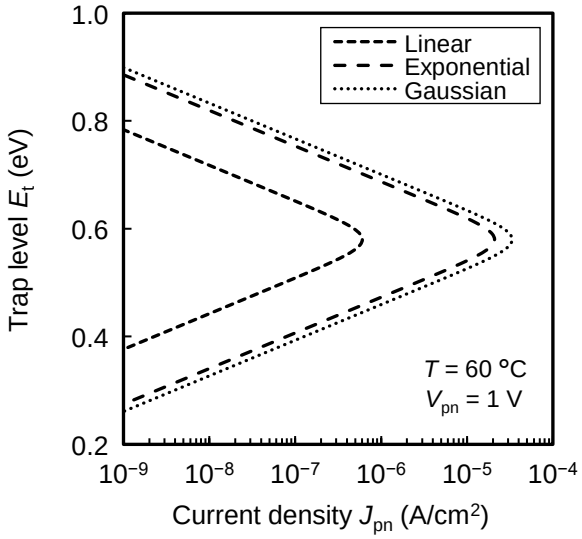



Figure 5.12 Relationship between $E_t$ and $J_{pn}$ at $V_{pn} = 1$ V ($n_0 = 1 \times 10^{17}$ cm$^{-3}$, $\lambda = W_{p-n}$ = 100 nm) for the three types of defect distributions. The temperature was assumed to be 60 °C.

## 5.3 Comparison with experimental results

### 5.3.1 Test structures to evaluate PPD in the lateral direction

The effects of PPD on p–n junction leakage current density ($J_{leak}$) were evaluated using devices with different lateral p–n junction widths ($D_{pn}$). The devices were designed similarly to the structure employed in the TCAD simulations. Defects were created in the lateral and vertical directions in the Si substrates during the contact-opening step. The prediction model was applied to reveal the profile of plasma process-induced defects in devices with lateral p–n junctions. The device structure with a lateral $n^+$–p junction is shown in Fig. 5.13. The process technology and device structures used in this chapter are the same as the Type-C device used in Chapter 4. The designed devices (samples I, II, and III) were exposed to $CF_4/CHF_3/Ar/O_2$-containing ECR plasma. The incident energy of ions was controlled by changing the peak-to-peak voltage ($V_{pp}$) at the wafer stage and 700 V was employed. The processing time was adjusted to remove an oxide film on Si substrates and to form contact holes. The contact opening process comprised $SiO_2$ etching and Si over-etching. Si over-etching results in the formation of a recess structure. Defects are anticipated to be created in the vertical and lateral (unexposed area) directions, during contact opening. Subsequently, CDE treatment was conducted for samples II and III. The CDE conditions are listed in Table 5.2. $CF_4/O_2$ discharge plasma was used for HT1 (sample II) and $CF_4$ discharge plasma, for HT2 (sample III). A 2.45-GHz microwave generated both plasmas; the exposure time was 18 s. After the removal of a native oxide layer at the bottom of contact opening areas, a phosphorus-doped poly-Si film with a dosage of $7.0 \times 10^{20}$ $cm^{-3}$ was deposited. The P-doped poly-Si film was electrically connected to the n-type region of the Si substrate. Furnace annealing (FA) was performed at 850 °C for 10 min under an $N_2$ atmosphere. The FA had two main purposes, to reduce

the contact resistance between the poly-Si film and the n-type region owing to the diffusion of P into the n-type region of the Si substrate and to prevent the depletion region from extending to the n-type region. The P concentration in the n-type region was designed to be higher than the boron concentration in the p-type region. The defect profile toward the p-type region can be investigated by extending the depletion region toward the p-type region.

The diameter ($\Phi$) at the bottom of the contact hole and depth of the Si recess ($d_R$) were measured using transmission electron microscopy (TEM). The *I–V* and *C–V* characteristics of the p–n junctions were evaluated using contact-hole array patterns with 504 k contacts; the measurement was performed in a dark environment. The voltages applied to the p-well and Si substrate were $V_{PW}$ = 0 and $V_{sub}$ = 0 V, respectively. The reverse bias voltage ($V_{rev}$) applied to p–n junctions ranging from 0 to 3 V. The lateral depletion region width ($W_{dep}$) was estimated using the *C–V* technique to precisely assess the distribution of defects in the lateral direction. The lateral distance from the sidewall surface of the contact hole to the center of the depletion region was defined as $D_{CJ}$. For simplicity, the area of the $n^+$–p junction ($S_j$) was approximated as a hemispherical surface: $S_j = 2\pi (\Phi/2 + D_{CJ})^2$. A change in $J_{leak}$ was evaluated in the devices for various $D_{pn}$ (0–140 nm).

The cross-sectional schematic of the poly-Si/Si system after poly-Si film deposition is shown in Fig. 5.14(a). Details of the cross-sectional TEM micrographs of poly-Si/Si systems of samples I, II, and III in Table 5.2 are shown in Figs. 5.14(b)–5.14(d), respectively. The values of $\Phi$ and $d_R$ for each sample are shown in these figures. Sample II treated with HT1 exhibited larger $\Phi$ and $d_R$ values than sample III treated with HT2. This is attributed to the difference in the etching rates between $CF_4/O_2$ and $CF_4$ plasmas.

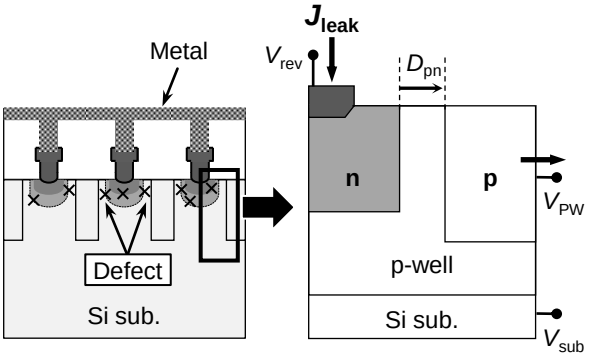



Figure 5.13 Device structure with a lateral $n^+$–p junction.

Table 5.2 Chemical dry etching (CDE) conditions.

| Sample ID | I | II | III |
|---|---|---|---|
| CDE Type | NA | HT1 | HT2 |
| $T_{sub}$ (°C) | — | 100 | 100 |
| $P_{MW}$ (W) | — | 400 | 400 |
| $CF_4$ (sccm) | — | 180 | 100 |
| $O_2$ (sccm) | — | 420 | — |

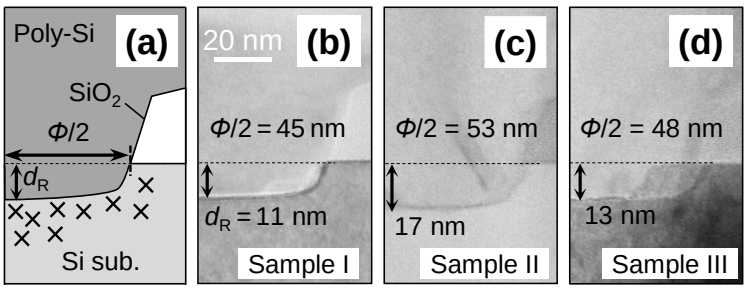



Figure 5.14 (a) Schematic of a poly-Si/Si system after poly-Si film deposition. Cross-sectional TEM micrographs of poly-Si/Si systems: (b) sample I, (c) sample II, and (d) sample III.

### 5.3.2 Assignment of defect distribution in the lateral direction

The profile of defects in the lateral direction was examined by applying the present prediction model to the experimental data. The $J_{leak}$ of samples I, II, and III was investigated based on the SRH model to identify the carrier conduction mechanism in the lateral direction. The measured $J_{leak}$–$V_{rev}$ characteristics (symbols) of the p–n junctions for samples I, II, and III with $D_{pn}$ = 0 and 140 nm are shown in Fig. 5.15. The measured $J_{leak}$–$V_{rev}$ curves were fitted using the SRH model expressed in Eq. (5.7) (solid lines in Fig. 5.15). The measured data were in good agreement with the model fitting curves. The fitting results supported the assumption that the $J_{leak}$ of the samples consisted mainly of $J_{SRH}$ and $J_{TAT}$.

$J_{TAT}$ and the activation energy ($E_a$) of $J_{TAT}$ depend on $F_m$ in the p–n junction; $E_a$ of $J_{TAT}$ can be calculated as follows:[28]

$$E_a = -\frac{\partial ln(J_{TAT})}{\partial\left(\frac{1}{kT}\right)} = E_t - \frac{3}{2}kT - 3kT\left(\frac{F_m}{F_\Gamma}\right)^2. \quad (5.8)$$

$E_t$ can be estimated from the value of $E_a$, when $F_m$ in the p–n junction is zero. $E_a$ as a function of $F_m^2$ for samples I, II, and III and $D_{pn}$ = 0, 60, 100, and 140 nm, wherein $E_a$ decreases as $F_m^2$ increases are shown in Fig. 5.16. The $E_t$ values for samples I, II, and III obtained from the values of $E_a$ at $F_m$ = 0 V/cm were 0.71, 0.72, and 0.70 eV, respectively. Various types of residual defects (trap levels) are present after PE and subsequent thermal processes.[24,29] The values of the trap level obtained from the evaluation of the parallel-connected hole array pattern represent the average of various trap levels.

Two typical leakage current mechanisms are governed by $F_m$ in the p–n junction: (1) TAT and (2) BBT.[30] TAT is relevant when $F_m$ in the p–n junction ranges from $10^5$ to $10^6$ V/cm, and BBT becomes relevant when $F_m$ exceeds $10^6$ V/cm.[30] The value of $E_a$ based on the BBT mechanism is smaller than 0.15 eV.[31,32] As shown in Fig. 5.16, the

value of $E_a$ is larger than 0.2 eV even at $V_{rev}$ = 3 V ($F_m^2$ = 0.89 [MV/cm]$^2$) with $D_{pn}$ = 0 nm. TAT is more dominant than BBT in the range of 0–3 V.

The measured $J_{leak}$ (symbols) as a function of $D_{pn}$ for samples I, II, and III at $V_{rev}$ = 1 V is shown in Fig. 5.17. $J_{leak}$ was fitted by curves predicted from the three types of defect spatial distributions (solid lines in Fig. 5.17). As shown, when $D_{pn}$ is smaller than 50 nm, the measured $J_{leak}$ properly fits with the curves predicted by the linear and exponential distributions. When $D_{pn}$ exceeds 50 nm, the measured $J_{leak}$ fits the curve of the exponential distribution better than that of the linear and Gaussian distributions. Therefore, the profile of defects in the lateral direction created by $CF_4/CHF_3/Ar/O_2$-containing plasma is exponential.

The characteristic lengths $\lambda$ of samples I, II, and III obtained from the fitting results were 85, 80, and 100 nm, respectively. The defect profile from the sidewall surface of the contact hole was estimated using the value of $\lambda$ obtained and the exponential distribution of defects. The defect distribution in the lateral direction estimated from the exponential distribution in Fig. 5.17 for samples I, II, and III is shown in Fig. 5.18, according to which $n_{dam}$ decreases along the lateral direction from the sidewall surface of the contact hole. $n_{dam}$ of sample III was the smallest, implying the number of defects decreased owing to HT2-CDE treatment in agreement with previous studies that suggest the residual species, such as F and C atoms in the Si substrate decreased owing to HT2-CDE treatment.[13] The model prediction with $J_{leak}$–$D_{pn}$ measurements revealed a spatial profile of defects with a width of ~100 nm and a density of $10^{15}$–$10^{16}$ cm$^{-3}$. This study both clarifies the presence of defects in the lateral direction and the impact of the defect profile on $J_{leak}$. Therefore, the prediction model, in combination with the $J_{leak}$ evaluation scheme using the designed structure, is beneficial in designing ultra-low leakage devices

by considering defect spatial distribution.

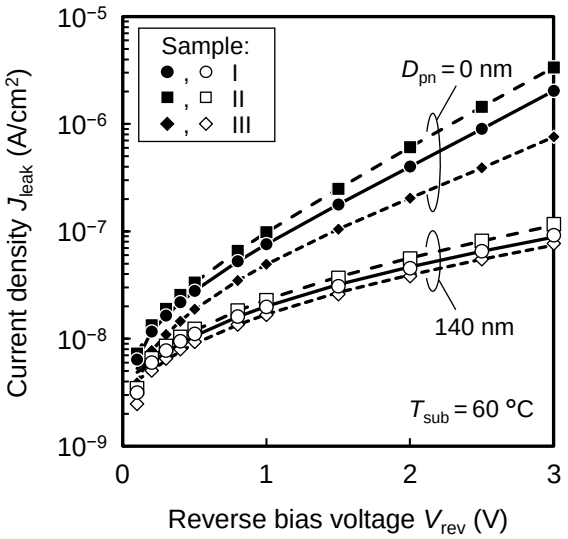



Figure 5.15 Measured $J_{leak}$–$V_{rev}$ characteristics of $n^+$–p junctions (symbols) with $D_{pn}$ = 0 and 140 nm for samples I, II, and III and the model fitting curves (lines) based on $J_{SRH}$ and $J_{TAT}$.

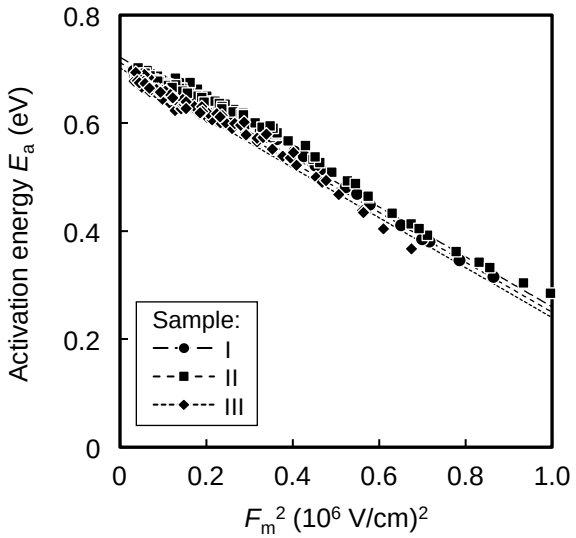



Figure 5.16 $F_m^2$-dependence of $E_a$ for samples I, II, and III with $D_{pn}$ = 0, 60, 100, and 140 nm.

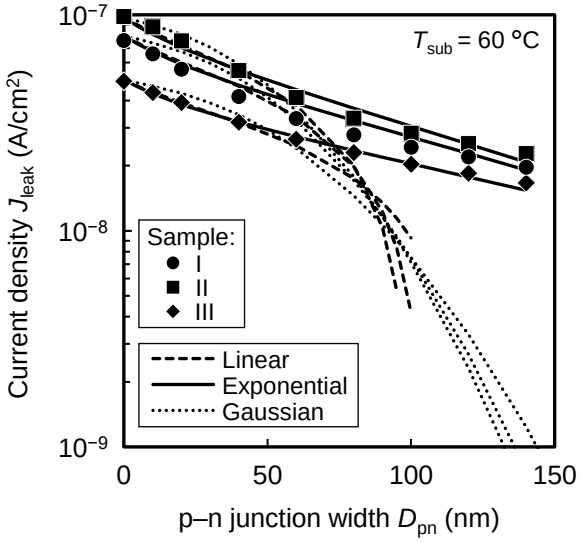



Figure 5.17 Measured $J_{leak}$–$D_{pn}$ characteristics of the $n^+$–p junctions for samples I, II, and III at $V_{rev}$ = 1 V (symbols) and model fitting curves (solid lines) based on the linear, exponential, and Gaussian distributions of defects.

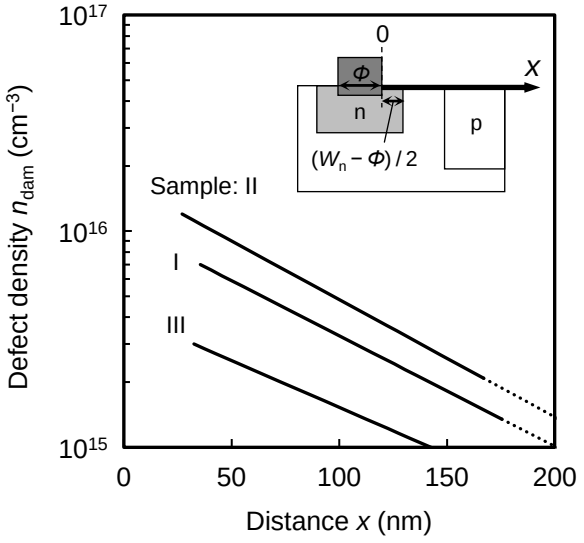



Figure 5.18 Defect density ($n_{dam}$) distributions in the lateral direction derived from $J_{leak}$ to $D_{pn}$ characteristics for samples I, II, and III.

## 5.4 Conclusion

We propose a model estimating the effects of created defects on p–n junction leakage current density increase ($\Delta J_{pn}$) in combination with TCAD simulations. Three defect spatial distributions, $n_{dam}(x)$, (linear, exponential, and Gaussian) were implemented to predict $\Delta J_{pn}$. $\Delta J_{pn}$ was strongly dependent on the $n_{dam}(x)$ profiles in addition to the total number of defects and energy level. The difference in $\Delta J_{pn}$ of the three defect distribution types resulted from the difference in $W_{dep}$ and the corresponding difference in $F_m$. The prediction model was implemented to experimentally assign the profile of defects in the devices with lateral p–n junction exposed to fluorocarbon-containing plasma. From the experimental results on $\Delta J_{pn}$, the distribution of defects was revealed to be exponential; the defects were distributed from the sidewall surface of the contact hole to a 100-nm distance with a density of $10^{15}$–$10^{16}$ $cm^{-3}$. The total number of defects and their distribution could be predicted from the p–n junction leakage current. The proposed model prediction scheme can be used to design plasma processes and circuit layouts when realizing future ultra-low leakage current devices.

**References**

[1] X. C. Mu, S. J. Fonash, A. Rohatgi, and J. Rieger, Appl. Phys. Lett. **48**, 1147 (1986).

[2] W. Wu and P. K. McLarty, J. Vac. Sci. Technol. A **13**, 67 (1995).

[3] K. T. Sung, S. W. Pang, M. W. Cole, and N. Pearce, J. Electrochem. Soc. **142**, 206 (1995).

[4] K. Egashira, K. Eriguchi, and S. Hashimoto, in *Proc. IEEE Int. Electron Devices Meeting*, 1998, pp. 563–565.

[5] Y. Nakakubo, A. Matsuda, M. Fukasawa, Y. Takao, T. Tatsumi, K. Eriguchi, and K. Ono, Jpn. J. Appl. Phys. **49**, 08JD02 (2010).

[6] Y. Nakakubo, K. Eriguchi, and K. Ono, ECS J. Solid State Sci. Technol. **4**, N5077 (2015).

[7] T. Hamano, K. Urabe, and K. Eriguchi, J. Phys. D: Appl. Phys. **52**, 455102 (2019).

[8] T. Morimoto, H. Ohtake, and T. Wanifuchi, J. Vac. Sci. Technol. B **33**, 051811 (2015).

[9] S. Kuboi, M. Yamage, and S. Ishikawa, in *Proc. IEEE Int. Symp. Semicond. Manuf.*, 2016, pp. 1–4.

[10] S. Furukawa, H. Matsumura, and H. Ishiwara, Jpn. J. Appl. Phys. **11**, 134 (1972).

[11] K. Eriguchi, A. Matsuda, Y. Takao, and K. Ono, Jpn. J. Appl. Phys. **53**, 03DE02 (2014).

[12] K. Eriguchi, J. Phys. D: Appl. Phys. **50**, 333001 (2017).

[13] Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. B **38**, 012205 (2019).

[14] Y. Sato, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, and K. Eriguchi, in *Proc. IEEE Int. Electron Devices Meeting*, 2020, pp. 9.4.1–9.4.4.

[15] Y. Okada, K. Ono, and K. Eriguchi, Jpn. J. Appl. Phys. **56**, 06HD04 (2017).

[16] Y. Sato, S. Shibata, A. Uedono, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. A **37**, 011304 (2018).

[17] W. Shockley and W. T. Read, Phys. Rev. **87**, 835 (1952).

[18] S. M. Sze and M.-K. Lee, *Semiconductor Devices, Physics and Technology*, 3rd ed. (Wiley, New York, 2012).

[19] R. N. Hall, Phys. Rev. **87**, 387 (1952).

[20] C. T. Sah, R. N. Noyce, and W. Shockley, Proc. IRE **45**, 1228 (1957).

[21] R. D. McGrath, J. Doty, G. Lupino, G. Ricker, and J. Vallerga, IEEE Trans. Electron Devices **34**, 2555 (1987).

[22] G. Vincent, A. Chantre, and D. Bois, J. Appl. Phys. **50**, 5484 (1979).

[23] P. A. Martin, B. G. Streetman, and K. Hess, J. Appl. Phys. **52**, 7409 (1981).

[24] Y. Sato, S. Shibata, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, and K. Eriguchi, IEEE J. Electron Devices Soc. **10**, 769 (2022).

[25] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 2090 (1992).

[26] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 331 (1992).

[27] G. Roll, M. Goldbach, and L. Frey, Microelectron. Reliab. **51**, 2081 (2011).

[28] A. Weber, A. Birner, and W. Krautschneider, Solid-State Electron. **51**, 1534 (2007).

[29] Y. Yoshikawa and K. Eriguchi, Jpn. J. Appl. Phys. **57**, 06JD04 (2018).

[30] E. Simoen, G. Eneman, M. B. Gonzalez, D. Kobayashi, A. L. Rodríguez, J.-A. J. Tejada, and C. Claeys, J. Electrochem. Soc. **158**, R27 (2011).

[31] Q. Rafhay, C. Xu, P. Batude, M. Mouis, M. Vinet, and G. Ghibaudo, Solid-State Electron. **71**, 37 (2012).

[32] A. Alnuaimi, A. Nayfeh, and V. Koldyaev, J. Appl. Phys. **113**, 044513 (2013).

# Chapter 6

# Characterization of plasma process-induced low-density defect creation by lateral junction leakage

## 6.1 Introduction

Plasma-induced damage (PID) is crucial in the design of leading-edge devices, as they are not inherently scalable in accordance with the device's feature size. Advanced ultralow leakage devices, such as CMOS image sensors (CISs), require precisely controlled defect creation dynamics because the residual defects in Si substrates after plasma etching (PE) act as carrier conduction sites and induce an increase in dark current ($I_{dark}$).[1–3] $I_{dark}$ limits the performance factors of CISs, such as the signal-to-noise ratio under low illumination. Thus, high-quality CISs require extremely low-dark currents (several electrons per second). Characterization of low-density defects in improving CIS performance is becoming increasingly relevant.

The effects of lateral defects by PPD on device performance are enhanced in three-dimensional device structures. Latent defects in the lateral direction were investigated through molecular dynamics simulations[4,5] and leakage current analysis using device structures with p–n junctions.[6] In planar-type MOSFETs, current flows laterally from a contact hole on the source or drain. Therefore, the impact of defects in

the lateral direction created by plasma processing should be precisely assessed to realize low-leakage devices. From Chapters 4 and 5, the employment of devices with p–n junctions formed in the lateral direction and leakage current ($I_{leak}$) was proven useful for the characterization of defects present in the lateral direction. The presence of defects created in the lateral direction (lateral PPD) was identified using device structures with various p–n junction widths in the lateral direction.

Defects created in the Si substrate during plasma processing act as electron hopping or recombination/generation sites for conduction. The trap energy levels and densities of these defects considerably influence the junction leakage current. Various test structures for PPD evaluation have been proposed.[6–13] A single device structure with various p–n junction widths to assess the lateral PPD in a short turnaround time was proposed.[6] In addition, a CIS structure to clarify the influence of the lateral PPD on the increase in $I_{dark}$ structure was employed.[14] After confirming the relationship between the change in $I_{leak}$ in single devices and that in $I_{dark}$ in a CIS circuit, the results from single devices can be used as a guideline to suppress the extent of PPD to CISs with ultralow leakage. Therefore, determining the relationship between the performance change in a simple structure and that in large-scale devices, such as ultra-large-scale integration and CIS circuits is crucial. However, a comprehensive comparison of parameters, such as $I_{leak}$ and $I_{dark}$, has not been performed extensively.

In this chapter, two test structures, that is, a single device with a p–n junction (Type-C) and a CIS device (Type-D) were prepared to examine the relationship between the obtained performance changes in response to PPD. The nature of defects in the lateral direction was evaluated using principal parameters of the Shockley–Read–Hall (SRH) model, such as defects density and trap energy levels ($E_t$).[15] The leakage current increase

in the single device (= $I_{leak}$) and the dark current increase in the CIS circuit (= $I_{dark}$), were evaluated. The contact-opening diameter ($\Phi$) was varied for these devices to examine the lateral PPD.

## 6.2 Designed devices for PPD assessments

The device with various p–n junction structures was proposed to assess low-density defects in the lateral direction in Chapter 4. This chapter focuses on low-density defects created by lateral PPD and the clarification of their influence on the leakage current increase using a single device (Type-C) and a CIS-based circuit (Type-D). The two test structures are shown in Figs. 2.1(c) and 2.1(d). Single devices were employed because the number of required fabrication steps is smaller than that required for CIS devices. Moreover, the process conditions and device layout designs can be optimized within a short turnaround time based on the results obtained. In contrast, the results obtained from CIS devices reveal the statistical features of defects created by PE. A schematic of defect creation in the lateral direction during PE is shown in Fig. 6.1. Defects are created in the lateral direction owing to the stochastic lateral straggling of the incident ions as well as the vertical direction. Hence, the defect density in the lateral direction is significantly smaller than that in the vertical direction.

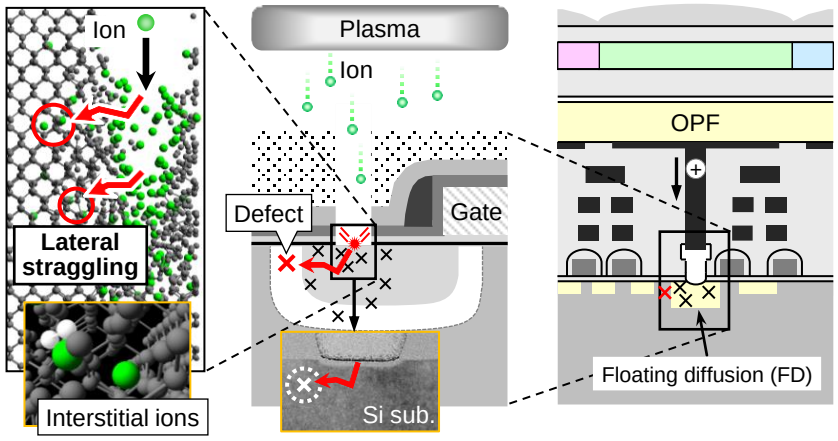



Figure 6.1 Schematic of defect creation in the lateral direction in a Si substrate during plasma processing.

## 6.3 Characterization scheme

The cross-sectional device structures with p–n junctions of the process test element group (PTEG) and device TEG (DTEG) are shown in Figs. 6.2(a) and 6.2(c), respectively. The layouts of the two test structures are shown in Fig. 2.2. The lateral distance between the p- and n-type regions ($D_{pn}$) was set at 90 nm. The n-type region located at the bottom of a contact hole in the PTEG was set to 160 × 160 nm. The number of contact holes for each PTEG and DTEG is 504000 and 3000, respectively. The 504000 contact-hole arrays in the PTEG were connected in parallel with the measured low-leakage current (several pA). The pixel area of the DTEG was composed of 3000 pixels and a single floating diffusion (FD) contact hole was connected to each pixel. The $\Phi$ of PTEG and DTEG are summarized in Table 2.1. The distance between the sidewall surface of the contact hole and the edge of the n-type region is defined as $D_{edge}$ (= 80 – $\Phi$/2 nm). The equivalent circuits of the PTEG and DTEG are shown in Figs. 6.2(b) and 6.2(d),

respectively. In the case of the DTEG, a reverse bias voltage ($V_{rev}$) was applied to the p–n junction (that is FD) via a reset transistor.[16] Notably, the leakage current through the p–n junctions ($I_{leak}$ and $I_{dark}$) comprises lateral and vertical leakage currents ($I_L$ and $I_V$, respectively). The impurity profile for the p–n junction was designed such that $I_L >> I_V$. Therefore, the following can be assumed: ($I_{leak}$, $I_{dark}$) ≈ $I_L >> I_V$. The voltages applied to the p-well and the Si substrate were $V_{PW}$ = 0 V and $V_{sub}$ = 0 V, respectively. $V_{rev}$ was applied to the p–n junction in the range of 0–3 V. $I_{leak}$ and $I_{dark}$ were measured at 333 K (60 °C), considering the operating temperature range of electronic devices.[17,18] The sample preparation flowchart for the PTEG and DTEG is shown in Fig. 2.4.

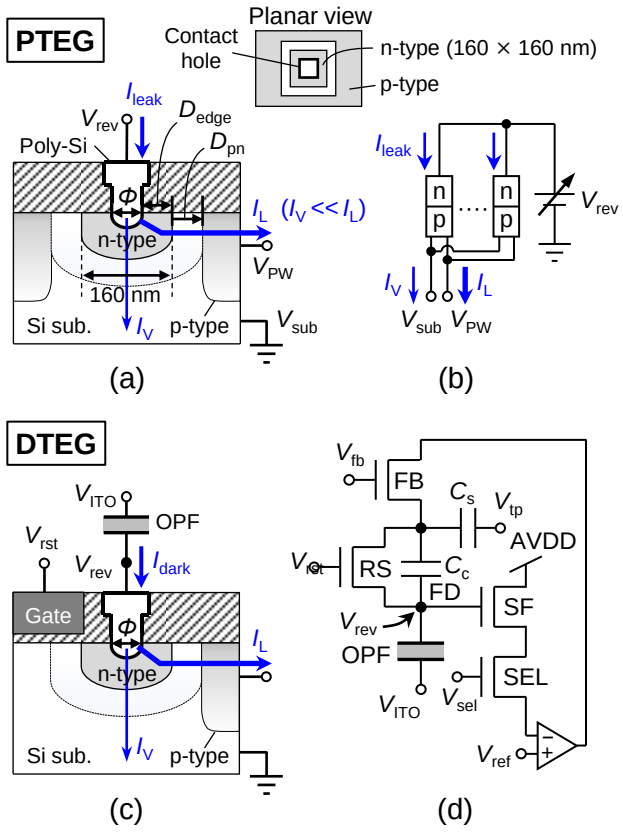



Figure 6.2 Cross-sectional illustrations of the (a) PTEG and (c) DTEG. Equivalent circuits of the (b) PTEG and (d) DTEG.

## 6.4 Results and discussion

### 6.4.1 Impacts of PPD on junction leakage and dark current

Cross-sectional TEM images of P1 and P2 listed in Table 2.1, with the contact holes filled with poly-Si are shown in Figs. 6.3(a) and 6.3(b), respectively. A Si recess structure with a depth of approximately 10 nm was formed in both samples by Si over-etching, followed by wet etching (WE). The formation of the Si recess structures implies the presence of PPD in Si substrates subject to PE conditions.

The cumulative probability of $I_{leak}$ at $V_{rev}$ = 0.5 V and $T_{sub}$ = 333 K for P0–P4 are shown in Fig. 6.4(a). At least 30 devices were measured. As shown, the distribution of $I_{leak}$ (slope) was not significantly dependent on $\Phi$. This can probably be because the $I_{leak}$ measured in the PTEG corresponds to the mean value of the currents of 504000 contacts connected in parallel. $I_{leak}$ increased with $\Phi$. The cumulative probability of $I_{dark}$ at $V_{rev}$ = 0.5 V for D1 and D2 is shown in Fig. 6.4(b). As observed, $I_{dark}$ of approximately 3000 pixels was distributed over a range of three orders of magnitude. The difference in the distribution of $I_{leak}$ and $I_{dark}$ [$S_{PTEG}$ and $S_{DTEG}$ in Figs. 6.4(a) and 6.4(b), respectively] might be attributed to the number of contact holes and difference in the sample structure and the number of process steps. The results suggest the necessity to suppress process variations, such as critical dimension controls in photolithography and PE to improve the variation in $I_{dark}$. An increase in $I_{dark}$ increases the number of white pixels in dark and fixed pattern noise. This is crucial for CISs in which the diffusion region cannot be reset during signal integration.[18–20] $I_{dark}$ differed between D1 ($\Phi$ = 80 nm) and D2 ($\Phi$ = 90 nm). Moreover, $\Phi$ dependence mechanisms of $I_{leak}$ and $I_{dark}$ are discussed in the following sections.

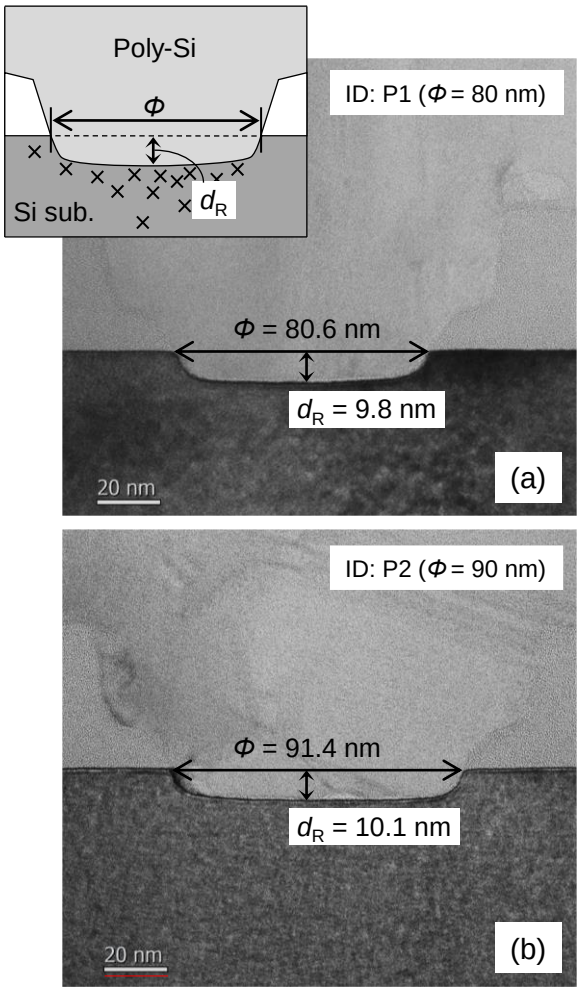



Figure 6.3 Representative cross-sectional TEM images of poly-Si/Si systems for (a) the P1 ($\Phi$ = 80 nm) and (b) P2 ($\Phi$ = 90 nm) samples of the PTEG.

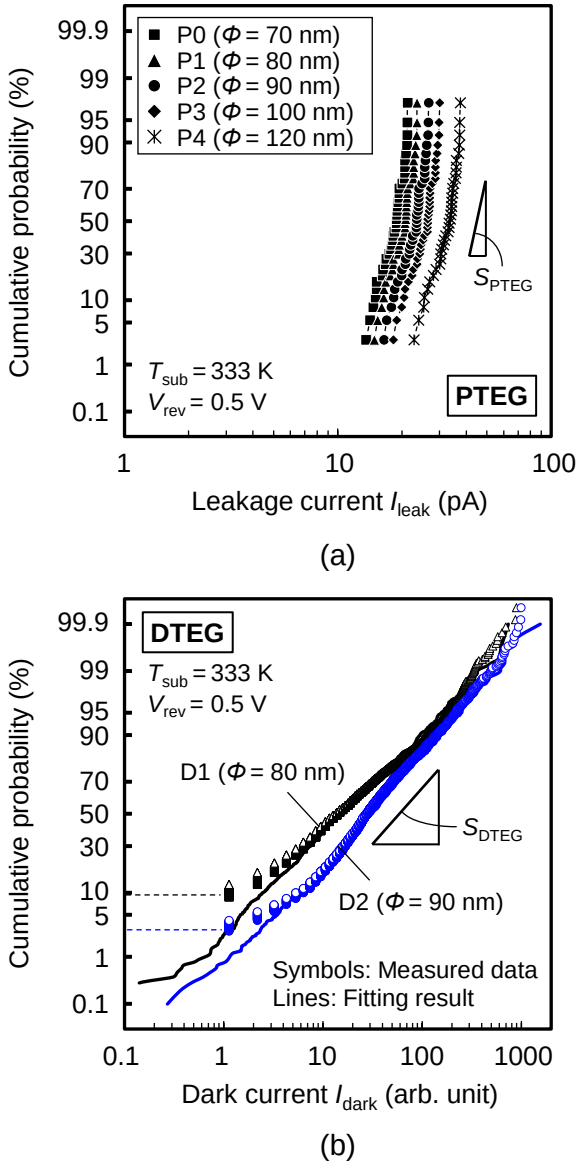



Figure 6.4 (a) Cumulative probability of $I_{leak}$ at $V_{rev}$ = 0.5 V and $T_{sub}$ = 333 K for P0–P4 ($\Phi$ = 70, 80, 90, 100, and 120 nm). (b) Cumulative probability of $I_{dark}$ at $V_{rev}$ = 0.5 V and $T_{sub}$ = 333 K for D1 ($\Phi$ = 80 nm) and D2 ($\Phi$ = 90 nm).

### 6.4.2 Carrier conduction in p–n junctions via defects

The representative temperature dependence of $I_{leak}$ for five $V_{rev}$ values (0.2, 0.5, 1, 2, and 3 V) for P2 ($\Phi$ = 90 nm) is shown in Fig. 6.5(a). The slope of $I_{leak}$ versus $1000/T_{sub}$ corresponds to the activation energy ($E_a$). Generally, the leakage current at the p–n junction comprises the diffusion current ($I_{diff}$), SRH generation current ($I_{SRH}$), trap-assisted tunneling current ($I_{TAT}$), and BBT current ($I_{BBT}$).[17,21–23] As explained in Chapter 2, $I_{diff}$ is proportional to $\exp(-E_g/kT)$ and $I_{SRH}$, to $\exp(-E_g/2kT)$.[24–26] $E_a$ of $I_{SRH}$ is assumed to be equal to the $E_t$ created by PE. $E_a$ is approximately $E_g/2$ at $V_{rev} \leq 1$ V and smaller than $E_g/2$ at $V_{rev} \geq 2$ V. This result implies the following: (1) $I_{diff}$ is not dominant in the samples and (2) $I_{SRH}$ is dominant when the electric field across the p–n junction is weak. Thus, $I_{diff}$ is considerably smaller than $I_{SRH}$ in the present case, that is, $I_{diff} << I_{SRH}$.

As shown in Chapter 2, two leakage current mechanisms are caused by the electric field ($F_m$) across the p–n junction, TAT and BBT. We focus on the $F_m$ across the p–n junction and the activation energy of the leakage current (carrier conduction) to identify the main mechanism. TAT dominates when $F_m$ across the p–n junction ranges from 0.1 to 1.0 MV/cm and BBT dominates when $F_m$ exceeds 1.0 MV/cm. The $V_{rev}$-dependence of $F_m$ for P0–P4 is shown in Fig. 6.5(b). The $F_m$ was estimated through $C$–$V$ measurements. As shown, $F_m$ is smaller than 1.0 MV/cm at the maximum voltage $V_{rev}$ = 3 V. This result suggests that TAT is dominant under the aforementioned applied voltage conditions.[23] Assuming the leakage current caused by the BBT mechanism is negligible ($I_{BBT} << I_{TAT}$), $I_{leak}$ can be approximated as $I_{leak} \sim I_{SRH} + I_{TAT}$.

This subsection focuses on $I_{SRH}$ and $I_{TAT}$ for the PTEG. The same trend was observed in the DTEG analysis. The presence of defects in the p–n junction influences the effective carrier concentration at the p–n junction owing to the ionization of defects.

The carrier concentration in the p–n junction influences the width of the depletion region. Thus, $I_{leak}$ in the p–n junction is influenced by the PPD-induced defect creation resulting from the change in $F_m$ across the junction. In the presence of an electric field ($F_m$ < 1.0 MV/cm), $I_{TAT}$ can be expressed using the field enhancement factor Γ as $I_{TAT} = \Gamma(F_m) \cdot I_{SRH}$.[27–29] The measured $I_{leak}$ of p–n junctions (symbols) as a function of $V_{rev}$ at $T_{sub}$ = 333 K for P0–P4 is shown in Fig. 6.5(c). Measured *I–V* curves for each *Φ* were fitted using the SRH model [solid lines in Fig. 6.5(c)]. The measured data and model fitting results were in good agreement. An increase in $I_{leak}$ by the lateral PPD could be modeled using $I_{SRH}$ and $I_{TAT}$. The measured $I_{dark}$ for each pixel was predicted using the SRH model, where each trap level was assumed to exhibit a normal distribution. As shown in Fig. 6.4(b), a good agreement was observed between $I_{dark}$ and the model fitting results based on $I_{SRH}$ and $I_{TAT}$.

Notably, $I_{SRH}$ and $I_{TAT}$ depend on $E_t$. The $E_a$ of $I_{TAT}$ was calculated from Eq. (5.8). $E_a$ depends on the temperature and $F_m$ at the p–n junction. For simplicity, we assume that 3/2 $kT$ << $E_t$. Thus, $E_t$ under $F_m$ = 0 V/cm, the density of traps ($n_t$) was estimated from the measured $E_t$ and $I_{SRH}$ values as follows,

$$n_t = \frac{2\cosh\left(\frac{|E_t - E_i|}{kT}\right)}{qn_i W_{dep} S\sigma_0 v_{th}} \cdot I_{SRH} \quad . \tag{6.1}$$

$I_{SRH}$ depends on $E_t$ and $n_t$ as expressed using Eq. (2.16). From Eq. (6.1), $n_t$ can be estimated by measuring the leakage current, that is, $I_{SRH}$. Based on the model of carrier conduction, the effects of lateral PPD on $E_t$ and $n_t$ were quantitatively evaluated from the change in leakage current. The PTEG and DTEG evaluation results are detailedly examined in the following sections.

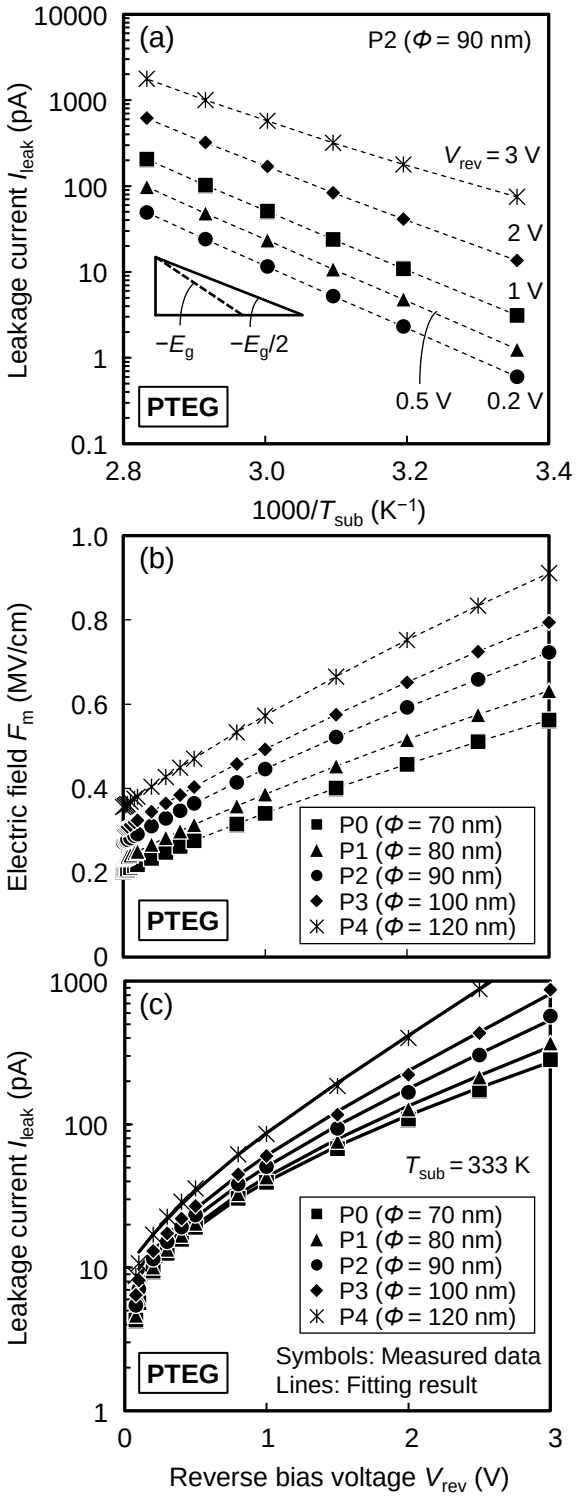



Figure 6.5 (a) Representative temperature dependence of the $I_{leak}$ for five $V_{rev}$ values (0.2, 0.5, 1, 2, and 3 V) for P2 ($\Phi$ = 90 nm). (b) $V_{rev}$-dependence of $F_m$ for P0–P4. (c) Measured $I_{leak}$ of p–n junctions as a function of $V_{rev}$ at $T_{sub}$ = 333 K for P0–P4.

### 6.4.3 Assignment of the energy level of defects

This subsection focuses on $E_t$, which is independent of the bias conditions. As previously mentioned, $E_t$ can be predicted from $E_a$ by measuring the temperature dependencies of $I_{leak}$ or $I_{dark}$ under different bias conditions. Subsequently, the energy profile of defects was determined from the temperature dependence of $I_{dark}$, that is, $E_a$, for all pixels in the case of DTEG. The relationship between the derived $E_a$ and $I_{dark}$ values at 293 K for D1 and D2 is shown in Fig. 6.6(a). The extracted $E_a$ values are distributed extensively, implying that various defect structures were formed in both D1 and D2. As shown, pixels with smaller $E_a$ values yielded larger $I_{dark}$ values regardless of $\Phi$. This indicated that a significantly damaged pixel (exhibiting a larger $I_{dark}$) contained a shallow trap site. $E_a$ distributions of D1 ($\Phi$ = 80 nm) and D2 ($\Phi$ = 90 nm) at $V_{rev}$ = 0.5 V are shown in Fig. 6.6(b). The mean value of $E_a$ for D2 is slightly larger than that for D1. The distribution of D2 extends to a lower $E_a$ region compared with that of D1. The number of pixels with small $E_a$ is larger in D2 than in D1. The defects created by PPD have an energy distribution. That is, the profile of trap energy levels depends on the amount of lateral PPD. The defects created by PPD are in the form of broken bonds, vacancies, and interstitials. These defect structures in the Si substrate generate trap levels to conduct carriers within the energy bandgap of Si. The creation of these trap levels was predicted theoretically.[5,30] The presence of various trap levels formed by PPD was proposed experimentally by cathodoluminescence analysis.[6,31] Using DTEG, statistical features could be assigned, such as the energy profile of the created defects. As previously measured, the extracted $E_a$ values were extensively distributed, implying that various defect structures were formed. A key advantage of using the DTEG is its ability to statistically and quantitatively assess the effects of lateral PPD on the leakage current.

The $\Phi$ dependencies of $E_a$ and $E_t$ derived from $I_{leak}$ for P0–P4 and the average of $E_a$ ($\overline{E}_a$) derived from $I_{dark}$ for D1 and D2 are shown in Fig. 6.7. The average activation energy calculated from Fig. 6.6(b) was used for $E_a$ in the DTEG. The $E_a$ and $E_t$ values were slightly dependent on $\Phi$. An increase in $\Phi$ indicates a decrease in the distance between the sidewall surface of the contact hole and the p–n junction, which corresponds to an increase in the lateral PPD as the number of defects decreases with increasing distance from the sidewall surface. As shown in Fig. 6.7, $E_a$ and $E_t$ slightly increase as a function of $\Phi$. The lateral PPD had a slight influence on $E_a$ and $E_t$ in the devices.

In addition, $E_a$ of the PTEG was consistent with $\overline{E}_a$ of the DTEG. This consistency indicates that the features of the trap energy levels in a CIS structure can be estimated using the PTEG. Complementary analyses using the PTEG and DTEG are indispensable to optimize the process conditions and device structures by considering the effects of the tail distribution of the trap level on the leakage current.

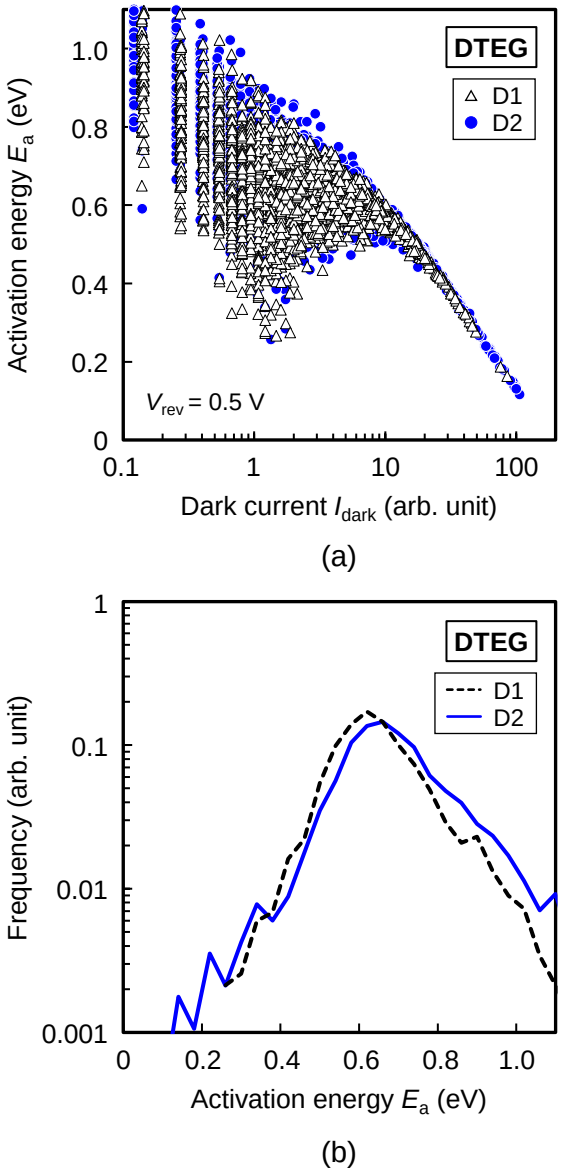



Figure 6.6 (a) Relationship between derived $E_a$ and $I_{dark}$ ($T_{sub}$ = 293 K) for D1 and D2 at $V_{rev}$ = 0.5 V and (b) $E_a$ distribution of each pixel for D1 and D2 at $V_{rev}$ = 0.5 V.

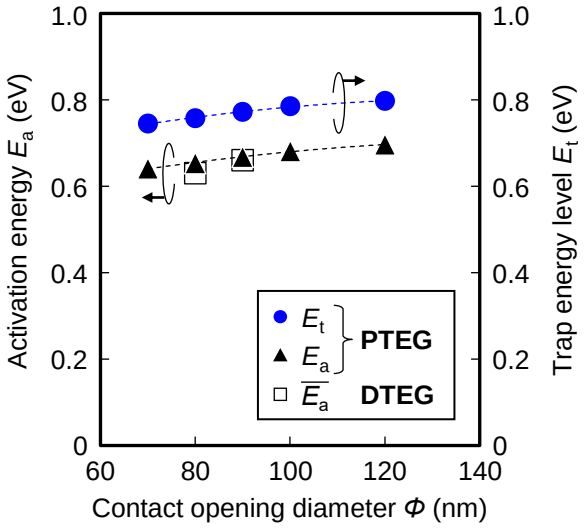



Figure 6.7 Comparison of $\Phi$ dependencies of $E_a$ and $E_t$ in the case of PTEG and $\overline{E}_a$ in the case of DTEG. The values of $E_a$ and $E_t$ were estimated from the temperature dependencies of $I_{leak}$ of P0–P4 in the case of PTEG and $\overline{E}_a$ [as shown in Fig. 6.6(b)] in the case of DTEG.

### 6.4.4 Assignment of the density of defects

Here, we investigated the density of created traps. Using the SRH model, $n_t$ can be estimated in the PTEG and DTEG from $I_{leak}$ to $I_{dark}$, as shown in Figs. 6.5(c) and 6.4(b), respectively. A comparison of the estimated $n_t$ derived from the $I_{SRH}$ as a function of $\Phi$ and $D_{edge}$ for the PTEG and DTEG is shown in Fig. 6.8. The $n_t$ value in Fig. 6.8 is the average density for the DTEG, which was derived from $\overline{E}_a$ and the mean value of $I_{dark}$. $n_t$ increases as $\Phi$ increases. As discussed in the previous subsection, the density of defects $n_t$ created in the p–n junction (= the amount of lateral PPD) increased as a function of $\Phi$. In addition, the dependence of $n_t$ on $D_{edge}$ validates that $n_t$ has a distribution that decreases in the lateral direction from the contact hole to the p–n junction. Overall, the $n_t$ values

estimated for the PTEG were consistent with those derived for the DTEG. Thus, the average defect density created by lateral PPD in a CIS circuit can be estimated using the PTEG data. The device and process conditions can be efficiently optimized by employing the PTEG.

A DTEG-based characterization scheme is advantageous in that it can predict the statistical distribution of trap levels created by the lateral PPD, thus leading to the statistical deviation of $I_{dark}$. In contrast, the PTEG is a powerful tool to assign $E_t$ and $n_t$ for various device structures under various bias conditions compared with the DTEG. Therefore, comprehensive and complementary analyses using PTEG and DTEG are extremely handy to identify the lateral PPD and optimize the device structures and process conditions required to realize future ultralow leakage devices.

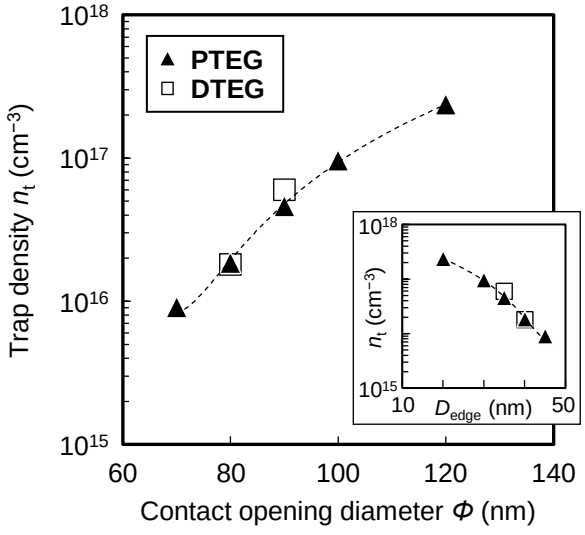



Figure. 6.8 Comparison of $n_t$ dependence on $\Phi$ in the cases of PTEG and DTEG. $n_t$ values were estimated from each $I_{SRH}$ for the PTEG and DTEG.

## 6.5 Conclusion

The effects of lateral PPD on the junction leakage current were comprehensively investigated using a single device and CIS circuit. The contact-opening diameter ($\Phi$) dependencies of $I_{leak}$ and $I_{dark}$ were extensively investigated. As observed, $I_{leak}$ and $I_{dark}$ increased with an increase in $\Phi$, implying an increase in the lateral PPD at the junction. The trap (defect) energy level and density were quantified using the SRH model. The derived trap level estimated for the PTEG was consistent with that of the DTEG. From the relationships of $\Phi$ and $n_t$, $n_t$ had a spatial distribution profile that decreases in the lateral direction from the sidewall surface of a contact hole to the p–n junction. The defect density and energy level depend on the amount of the lateral PPD. The characterization scheme using the PTEG and DTEG demonstrated in this study can be used to evaluate low-density PPD, thus optimizing the plasma process and device design.

**References**

[1] N. Teranishi, in *Proc. Int. Symp. VLSI Technol.*, 2013, pp. 1–4.

[2] J.-P Carrère, S. Place, J.-P Oddou, D. Benoit, and F. Roy, in *2014 IEEE Int. Reliab. Phys. Symp.*, 2014, pp. 3C.1.1–3C.1.6.

[3] S. Kuboi, M. Yamage, and S. Ishikawa, in *Proc. IEEE Int. Symp. Semicond. Manuf.*, 2016, pp. 1–4.

[4] K. Eriguchi, A. Matsuda, Y. Takao, and K. Ono, Jpn. J. Appl. Phys. **53**, 03DE02 (2014).

[5] K. Eriguchi, J. Phys. D: Appl. Phys. **50**, 333001 (2017).

[6] Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. B **38**, 012205 (2019).

[7] K. Egashira, K. Eriguchi, and S. Hashimoto, in *Proc. IEEE Int. Electron Devices Meeting*, 1998, pp. 563–565.

[8] X. C. Mu, S. J. Fonash, A. Rohatgi, and J. Rieger, Appl. Phys. Lett. **48**, 1147 (1986).

[9] K. T. Sung, S. W. Pang, M. W. Cole, and N. Pearce, J. Electrochem. Soc. **142**, 206 (1995).

[10] Y. Nakakubo, K. Eriguchi, and K. Ono, ECS J. Solid State Sci. Technol. **4**, N5077 (2015).

[11] W. Wu and P. K. McLarty, J. Vac. Sci. Technol. A **13**, 67 (1995).

[12] T. Morimoto, H. Ohtake, and T. Wanifuchi, J. Vac. Sci. Technol. B **33**, 051811 (2015).

[13] G.-H. Kim, Y.-R. Kang, W.-J. Kim, S.-Y. Kim, and C.-I. Kim, Thin Solid Films **515**, 4892 (2007).

[14] Y. Sato, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, and K. Eriguchi, in *Proc. IEEE Int. Electron Devices Meeting*, 2020, pp. 9.4.1–9.4.4.

[15] W. Shockley and W. T. Read, Phys. Rev. **87**, 835 (1952).

[16] K. Nishimura, Y. Sato, J. Hirase, R. Sakaida, M. Yanagida, T. Tamaki, M. Takase, H.

Kanehara, M. Murakami, and Y. Inoue, in *Proc. IEEE Int. Solid-State Circuits Conference*, 2016, pp. 110–111.

[17] N. V. Loukianova, H. O. Folkerts, J. P. V. Maas, D. W. E. Verbugt, A. J. Mierop, W. Hoekstra, E. Roks, and A. J. P. Theuwissen, IEEE Trans. Electron Devices **50**, 77 (2003).

[18] P. Centen, S. Lehr, S. Roth, J. Rotte, F. Heizmann, A. Momin, R. Dohmen, K.-H. Schaaf, K. J. Damstra, R. Ree, and M. Schreiber, in *Proc. Int. Image Sensor Workshop*, 2013, pp. 409–412.

[19] K. Nishimura, S. Shishido, Y. Miyake, H. Kanehara, Y. Sato, J. Hirase, Y. Sato, Y. Tomekawa, M. Yamasaki, M. Murakami, M. Harada, and Y. Inoue, Jpn. J. Appl. Phys. **57**, 1002B4 (2018).

[20] M. Guidash M. Oh, D. Collins, R. Mauritzson, D. Tekleab, W. Xu, and S. Nicholes, in *Proc. Int. Image Sensor Workshop*, 2019, p. P06.

[21] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 2090 (1992).

[22] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 331 (1992).

[23] E. Simoen, G. Eneman, M. B. Gonzalez, D. Kobayashi, A. L. Rodríguez, J.-A. J. Tejada, and C. Claeys, J. Electrochem. Soc. **158**, R27 (2011).

[24] W. Shockley, Bell Syst. Tech. J. **28**, 435 (1949).

[25] D. K. Schroder, Solid-State Electron. **27**, 247 (1984).

[26] S. M. Sze and M.-K. Lee, *Semiconductor Devices, Physics and Technology*, 3rd ed. (Wiley, New York, 2012).

[27] G. Vincent, A. Chantre, and D. Bois, J. Appl. Phys. **50**, 5484 (1979).

[28] Y. Mori, S. Kamohara, M. Moniwa, K. Ohyu, T. Yamanaka, and R. Yamada, IEEE Trans.

Electron Devices **53**, 398 (2006).

[29] A. Weber, A. Birner, and W. Krautschneider, Solid-State Electron. **51**, 1534 (2007).

[30] Y. Yoshikawa and K. Eriguchi, Jpn. J. Appl. Phys. **57**, 06JD04 (2018).

[31] Y. Sato, S. Shibata, A. Uedono, K. Urabe, and K. Eriguchi, J. Vac. Sci. Technol. A **37**, 011304 (2018).

# Chapter 7

# Conclusion

This study examined defect creation mechanisms (PPD) near the surface region caused by the physical interaction between a crystalline Si substrate and incident ions from the plasma. The effects of PPD on ultra-low leakage current devices were examined by identifying the defect distribution and the density in the Si substrate and detailedly evaluating its effect on the p–n junction leakage current. The following concluding remarks can be drawn.

1. PPD to Si substrates in the vertical (depth) direction were investigated using various analysis techniques. Time-of-flight SIMS identified the presence of interstitial atoms to a depth of ~20 nm. CL and PAS analyses could assign defects both on the Si substrate surface and underneath the IL after PE. Based on CL analysis, the created defects (both on the Si surface and underneath the IL) function as carrier recombination centers. Based on PAS analysis, the structural changes assigned by the extracted *S* value extended to a depth of approximately 200 nm. Moreover, the depth and density of defects ($10^{16}$ $cm^{-3}$) were validated by a technique using the PPD-enhanced dechanneling of As atoms implanted with a projection range of 10 nm combined with detailed SIMS analysis. From the decrease in *S* value by the PAS analysis, defects in the form of vacancies and fluorine (residual species) were distributed from the substrate surface to a depth of approximately 130 nm with a

density of $10^{16}$ $cm^{-3}$ (much lower than the detection limits of conventional analysis techniques, ~$10^{18}$ $cm^{-3}$). Moreover, this distribution was promoted by annealing processes.

2. Defect creation in the vertical and lateral directions of Si substrates during PE was investigated using devices with different p–n junction structures. Based on current–voltage measurements of devices with different p–n junction distances, leakage currents in the vertical and lateral directions increased with decreasing p–n junction distance. PPD created defects in the vertical and lateral directions because of the stochastic straggling of impurity species, as theoretically predicted by molecular dynamics simulations.
3. A model that focused on the effects of created defects on the p–n junction leakage current increase ($\Delta J_{pn}$) in combination with TCAD simulations was proposed. The prediction model was implemented to experimentally assign defect profiles in the devices with lateral p–n junction exposed to fluorocarbon-containing plasma. The distribution of defects was exponential from the experimental results on $\Delta J_{pn}$. Defects created during a contact-opening step were distributed from the outer edge of the contact hole to a distance of 100 nm with a density of $10^{15}$–$10^{16}$ $cm^{-3}$.
4. Two test structures—a single device with a leakage current ($I_{leak}$) and a CIS circuit with a dark current ($I_{dark}$)—were designed to examine the relationship between the obtained performance changes in response to PPD. Both $I_{leak}$ and $I_{dark}$ were dependent on the diameter of the contact fabricated by PE, implying the presence of defects in the lateral direction via lateral PPD. From the analysis of the temperature dependence of $I_{leak}$ and $I_{dark}$, the lateral PPD influenced the mean value of the activation energy $E_a$. The derived trap site density ($n_t$) in the CIS circuit was consistent with that of a single

device. An increase in $I_{dark}$ indicated an increase in the number of trap sites and an increase in defects at shallow levels in particular.

This study revealed the presence and distribution of ultra-low-density plasma-induced defects in Si substrates by tracking As atoms in Si substrates. The lateral PPD was revealed by focusing on the change in leakage current using device structures with lateral p–n junctions. Furthermore, we experimentally demonstrated using a single device and a CIS that the presence of ultra-low-density plasma-induced defects created in the lateral direction increased the leakage current. The comprehensive defect profiling and characterization scheme performed in this study could be used to evaluate low-density PPD, resulting in the optimization of plasma processes and the design of future electronic devices that are sensitive to defect creation.

***A brief outlook***

(1) The optimization of gas chemistry can effectively suppress PPD. Stochastic straggling (scattering) is more obvious for light mass ions, such as H and F, which are widely used in current mass production. This mechanism was also predicted through molecular dynamics simulations.

(2) The implementation of the PPD proximity effect, that is, lateral-PPD-aware layout designs, is an alternative approach to suppress an increase in $I_{dark}$ induced by the lateral straggling of incident species.

(3) Plasma processes and devices can be designed by considering the effect of defect distribution on device performance with the implementation of a defect distribution model in TCAD simulations. This approach is expected to realize future low-leakage devices.

# Appendix

## A.1 Leakage current by the Poole–Frenkel effect and band-to-band tunneling

The junction leakage current can be described using the Poole–Frenkel model in the case of a weak electric field ($F_m \sim 10^4$ V/cm).[1–4] In the Poole–Frenkel model, electrons are thermally emitted over the top of a potential energy barrier lowered by the presence of the electric field. The electric-field dependence of the junction leakage current density ($J_{PF}$) is expressed as[3,4]

$$J_{PF} \sim F_m \exp\left(\frac{q}{kT}\sqrt{\frac{qF_m}{\pi\varepsilon_{Si}}}\right), \tag{A1}$$

where $\varepsilon_{Si}$ is the permittivity of Si.

BBT becomes obvious in an electric field over $10^6$ V/cm. BBT current density ($J_{BBT}$) is expressed as[5,6]

$$J_{BBT} \sim V\left(\frac{F_m}{F_0}\right)^{\frac{3}{2}} \exp\left(-\frac{F_0}{F_m}\right), \tag{A2}$$

where $F_0$ is a material-dependent constant depending on the tunneling effective mass and band gap of the semiconductor material.

## References

[1] J. Frenkel, Phys. Rev. **54**, 647 (1938).

[2] M. J. J. Theunissen and F. J. List, Solid-State Electron. **28**, 417 (1985).

[3] J. Lin, S. Banerjee, J. Lee, and C. Teng, IEEE Electron Device Lett. **11**, 191 (1990).

[4] H. D. Lee, IEEE Trans. Electron Devices **47**, 762 (2000).

[5] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 2090 (1992).

[6] E. Simoen, G. Eneman, M. B. Gonzalez, D. Kobayashi, A. L. Rodríguez, J.-A. J. Tejada, and C. Claeys, J. Electrochem. Soc. **158**, R27 (2011).

# Acknowledgments

First, I would like to express my sincere gratitude to Professor Koji Eriguchi for the continuous support of my research, helpful discussions, and insightful guidance. I could think about and learn what is relevant not only in research but also in life through discussions. Assistant professor Keiichiro Urabe provided many helpful comments, warm encouragement, and considerate concern.

I am sincerely grateful to Professor Akira Uedono of the University of Tsukuba for fruitful discussions on PAS measurement data. I would like to thank Dr. Satoshi Shibata at Panasonic Operational Excellence for his insightful comments and encouragement. Furthermore, I would like to thank Dr. Kazuko Nishimura, Mr. Takayoshi Yamada, Mr. Ryota Sakaida, Mr. Masayuki Yamasaki, and Mr. Masashi Murakami of Panasonic Holdings Corporation for their support and encouragement.

I would like to thank Mr. Tomohiro Kuyama (Tokyo Electron Ltd.), Mr. Takashi Hamano, and Mr. Takayuki Matsuda for their support. Further, I would like to thank all the members of the Propulsion Engineering Laboratory in the Department of Aeronautics and Astronautics, Kyoto University.

Finally, I am grateful to my wife, Hiromi, for her constant support. I am grateful to my parents for their words of encouragement and generous kindness.

I dedicate this study to my wife and parents.

January 2023

# List of Publications

## Journal Articles

1. Y. Sato, S. Shibata, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, and K. Eriguchi, "Predicting the effects of plasma-induced damage on p–n junction leakage and its application in the characterization of defect distribution," J. Vac. Sci. Technol. B **40**, 062209 (2022).
   [**Chapter 5** of the dissertation is reproduced from this paper, with the permission of AIP Publishing. Copyright (2022), American Vacuum Society. DOI: 10.1116/6.0002181.]

2. Y. Sato, S. Shibata, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, and K. Eriguchi, "Characterization of Plasma Process-induced Low-density Defect Creation by Lateral Junction Leakage," IEEE J. Electron Devices Soc., **10**, 769 (2022).
   [**Chapter 6** of the dissertation is reproduced from this paper, with the permission of IEEE. Copyright (2022), IEEE. DOI: 10.1109/JEDS.2022.3176321.]

3. Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, "Evaluation of residual defects created by plasma exposure of Si substrates using vertical and lateral pn junctions," J. Vac. Sci. Technol. B **38** 012205 (2019).
   [**Chapter 4** of the dissertation is reproduced from this paper, with the permission of AIP Publishing. Copyright (2019), American Vacuum Society. DOI: 10.1116/1.5126344.]

4. Y. Sato, S. Shibata, A. Uedono, K. Urabe, and K. Eriguchi, "Characterization of the distribution of defects introduced by plasma exposure in Si substrate," J. Vac. Sci. Technol. A **37**, 011304 (2019).
   [**Chapter 3** of the dissertation is reproduced from this paper, with the permission of AIP Publishing. Copyright (2019), American Vacuum Society. DOI: 10.1116/1.5048027.]

5. K. Nishimura, S. Shishido, Y. Miyake, H. Kanehara, Y. Sato, J. Hirase, Y. Sato, Y. Tomekawa, M. Yamasaki, M. Murakami, M. Harada and Y. Inoue, "Advanced features of layered-structure organic-photoconductive-film CMOS image sensor: Over 120 dB wide dynamic range function and photoelectric-conversion-controlled global shutter function," Jpn. J. Appl. Phys., **57**, 1002B4 (2018).

## International conference contributions

1. [Invited] Y. Sato, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, K. Eriguchi, “Evaluation of Plasma-Induced Stochastic Damage Creation in the Lateral Direction Using pn Junction Structures,” *20th International Workshop on Junction Technology 2021*, pp. 21–24 (Kyoto, Japan, June 10–11, 2021).
2. Y. Sato, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, K. Eriguchi, “Characterization Scheme for Plasma-Induced Defect Creation due to Stochastic Lateral Straggling in Si Substrates for Ultra-low Leakage Devices,” *66th IEEE International Electron Devices Meetin*g (IEDM 2020), December 12–16, 2020, IEEE Electron Devices Society.
3. [Invited] Y. Sato, S. Shibata, A. Uedono, K. Urabe, and K. Eriguchi, “Characterization of residual defects created in Si substrates,” *The Forum on the Science and Technology of Silicon Materials 2018*, November 18–21, 2018, Okayama University 50th Anniversary Hall, Okayama, Japan.
4. T. Kuyama, Y. Sato, K. Urabe, and K. Eriguchi, “Effects of Microwave Annealing on the Recovery of Microscopic Defects in Silicon Nitride Films,” *40th International Symposium on Dry Process*: DPS2018, November 13–15, 2018, Toyoda Auditorium, Nagoya University, Aichi, Japan. Proc. 40th International Symposium on Dry Process (DPS), 299–300 (2018).
5. Y. Sato, S. Shibata, R. Sakaida, and K. Eriguchi, “Characterization of Residual Defects in Plasma-exposed Si Substrates using Cathodoluminescence and Positron Annihilation Spectroscopy,” *17th International Workshop on Junction Technology 2017*, pp. 73–76 (Kyoto, Japan, June 2nd, 2017).

## Domestic conference contributions

1. [招待講演] Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, “pn接合構造を用いたシリコン基板へのプラズマ誘起ダメージの評価 (Evaluation of plasma-induced damage in Si substrate using pn junction structures),” 第82回応用物理学会秋季学術講演会 (82nd JSAP Autumn Meeting), Nagoya, Japan, Sep. 10–13, 2021.
2. [招待講演] 佐藤好弘, 山田隆善, 西村佳壽子, 山崎雅之, 村上雅史, 占部継一郎, 江利口浩二:「プラズマプロセスにより形成される3次元欠陥分布が暗電流特性に及ぼす影響評価」, (映像情報メディア学会 情報センシング研究会(IST), 「固体撮像技術および

一般」, 2021年3月26日（金）, オンライン）

3. [招待講演] 佐藤好弘, 山田隆善, 西村佳壽子, 山崎雅之, 村上雅史, 占部継一郎, 江利口浩二:「プラズマ曝露中に確率的ラテラル散乱によって導入されるシリコン中の欠陥が超低リーク電流デバイスに与える影響の評価」, 先端 CMOS デバイス・プロセス技術（IEDM 特集）, 2021 年 1 月 28 日, シリコン材料・デバイス研究会（SDM）:オンライン開催
4. [招待講演] 佐藤好弘:「プラズマと固体表面における欠陥生成機構の高感度解析」, 第34回プラズマ新領域研究会,「プラズマプロセスにおける欠陥生成に関する新生面」, 2020年10月21日, 応用物理学会プラズマエレクトロニクス分科会:オンライン開催
5. 久山智弘, 吉川侑汰, 佐藤好弘, 占部継一郎, 江利口浩二:「プラズマ曝露によりシリコン窒化膜中に形成された欠陥構造の窒素雰囲気アニールに関する検討」, 第 79 回応用物理学会秋季学術講演会 (79th JSAP Autumn Meeting), Nagoya, Japan, Sep. 18–21, 2018.

## Award

1. IEEE EDS Kansai Chapter of the Year Award

   Y. Sato, T. Yamada, K. Nishimura, M. Yamasaki, M. Murakami, K. Urabe, and K. Eriguchi: “Characterization Scheme for Plasma-Induced Defect due to Stochastic Lateral Straggling in Si Substrates for Ultra-Low Leakage Devices,” IEEE International Electron Devices Meeting (IEDM).

   2021年9月28日
2. 第19回プラズマエレクトロニクス賞 (Plasma Electronics Award)

   Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, “Evaluation of residual defects created by plasma exposure of Si substrates using vertical and lateral pn junctions.”

   2021年3月10日
3. IEEE ISSCC 2016 Demonstration Session Award

   K. Nishimura, Y. Sato, J. Hirase, R. Sakaida, M. Yanagida, T. Tamaki, M. Takase, H. Kanehara, M. Murakami, and Y. Inoue, “An Over 120dB Simultaneous-Capture Wide-Dynamic-Range 1.6e- Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor.”

   2016年2月6日

## Misc

1. 佐藤好弘，柴田聡，占部継一郎，江利口浩二:「プラズマエレクトロニクス賞を受賞して」，応用物理学会プラズマエレクトロニクス分科会会報, 74, 25–27, 2021 年 6 月

## Other publications

1. K. Yamamoto, S. Sakashita, Y. Sato, M. Inoue, M. Anma, T. Oosuka, and J. Yugami, “Phase and Composition Control of Ni Fully Silicided Gates by Nitrogen Ion Implantation and Double Ni Silicidation,” Jpn. J. Appl. Phys., vol. 47, no. 4S, p. 2398, (2008).
2. Y. Satoh, H. Okada, K. Jinushi, H. Fujikura, and H. Hasegawa, “Voltage Gain in GaAs-Based Lateral Single-Electron Transistors Having Schottky Wrap Gates,” Jpn. J. Appl. Phys., vol. 38, no. 1S, p. 410, (1999).
3. S. Kasai, Y. Satoh, and H. Hasegawa, “Conductance oscillation characteristics of GaAs Schottky wrap-gate single-electron transistors,” Physica B: Condensed Matter, vol. 272, no. 1, pp. 88–91, (1999).
4. Y. Satoh, S. Kasai, K. Jinushi, and H. Hasegawa, “Computer Simulation and Experimental Characterization of Single Electron Transistors Based on Schottky Wrap Gate Control of 2DEG,” Jpn. J. Appl. Phys., vol. 37, no. 3S, p. 1584, (1998).
5. H. Hasegawa, T. Sato, H. Okada, K. Jinushi, S. Kasai, and Y. Satoh, “Electrochemical formation and characterization of Schottky in-plane and wrap gate structures for realization of GaAs- and InP-based quantum wires and dots,” Applied Surface Science, vol. 123–124, pp. 335–338, (1998).