Study on Electron Trapping and Transport in SiC MOSFETs

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Abstract

In the present day, the reduction of power loss in semiconductor power devices is important to solve the energy problems in the world. The performance of conventional silicon (Si)-based power devices is approaching the theoretical limit determined by its physical properties. In order to overcome it, silicon carbide (SiC) is currently regarded as a new material for power device applications owing to its wide band gap and high critical electric field. Consequently, the conduction loss of SiC devices can be reduced to 1/500 compared to Si ones.

The donor and acceptor concentrations ($N_{\mathrm{D,A}}$) of SiC are widely controllable in the range 10^{14} cm^{-3} $\leq N_{\mathrm{D,A}} \leq 10^{20}$ cm^{-3} both by epitaxial growth and by ion implantation. In addition, the SiC/silicon dioxide ($\mathrm{SiO_2}$) interfaces have both high conduction and valence band offsets. For these reasons, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) have been researched and developed for several decades. However, in the case of 600–1200 V class devices (most marketable devices), the channel resistance accounts for most of the specific on-resistance. As a result, the drain current of SiC power MOSFETs is unpredictable even though the basic device parameters (e.g., p-body doping concentration and gate oxide thickness) are given. This abnormally high channel resistance originates from a high density of SiC/$\mathrm{SiO_2}$ interface states. The lack of information on the relationship between channel resistance and interface state density (i.e., influences of electron trapping and scattering) makes it difficult to predict the drain current of MOSFETs, which is a major challenge at the present stage.

The most important parameter for the drain current, effective channel mobility, can be obtained from the electrical characteristics of MOSFETs. The effective channel mobility can be expressed as a product of (i) the ratio of free electrons to total electrons and (ii) the free electron mobility. Because the interface states capture the electrons in the inversion layers and the trapped electrons act as Coulomb scattering centers, (i) and (ii) change simultaneously as the gate voltage changes. In order to understand these phenomena, accurate separation of free and trapped electrons and elucidation of the electron scattering mechanism are required. From the above background, the present study aims to extract the energy distribution of interface state density near the conduction band edge based on the gate characteristics of MOSFETs and to clarify the electron scattering mechanism in SiC/$\mathrm{SiO_2}$ inversion layers by using MOS-Hall effect measurements and numerical calculations.

In Chapter 1, the reason why SiC is superior for power device applications is explained. On the other hand, the challenges of SiC MOSFETs and the current status of previous studies are detailed. After that, two objectives of the present study and the methods to accomplish them are proposed.

In Chapter 2, gate characteristics of MOSFETs are focused to extract the energy distribution of interface state density near the conduction band edge. The interface state density plotted with respect to the bottom edge of the two-dimensional density of states shows that the interface state density is uniquely determined by the interface treatments regardless of p-body doping concentration. This result indicates that the defect states are generated not at SiC/SiO_2 but in SiC. Furthermore, the author finds that the ratio of free electrons to total electrons is independent of the p-body doping concentration.

In Chapter 3, to discuss the behavior of free electron mobility, the effective channel mobility of SiC MOSFETs annealed in phosphoryl chloride ($POCl_3$) is quantified. MOS-Hall effect measurements reveal that the electron trapping effect is extremely small in the case of $POCl_3$-annealed MOSFETs. In the low effective normal field region, the effective channel mobility of $POCl_3$-annealed MOSFETs is higher than the phonon-limited mobility reported in the previous study on Hall effect measurement for MOSFETs annealed in nitric oxide (NO). On the other hand, in the high effective normal field region, the effective channel mobility decreases sharply due to strong surface roughness scattering.

In Chapter 4, MOS-Hall effect measurements are conducted to clarify the electron scattering mechanism in SiC (0001)/SiO_2 inversion layers. As a result, the Hall mobility of $POCl_3$-annealed MOSFETs is about 1.9–2.9 times higher than that of NO-annealed MOSFETs in the high effective normal field region. The theoretically calculated free electron mobility is increased by reducing trapped electron density, especially in the high effective normal field region. In addition, Hall mobility at 77 K is much lower than that at room temperature (RT), regardless of interface treatment.

In Chapter 5, the electron scattering mechanism in SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO_2 inversion layers, which is essential for trench-type vertical MOSFETs, is discussed. The trapped electron density of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs is 1.8 times higher than that of $POCl_3$-annealed (0001) MOSFETs, whereas it is 3.9 times lower than that of NO-annealed (0001) MOSFETs. Then, the Hall mobility of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs is 1.5 times higher than that of NO-annealed (0001) MOSFETs and is 1.4 times lower than that of $POCl_3$-annealed (0001) MOSFETs. Moreover, the ratio of Hall mobility at 77 K to that at RT is smaller for MOSFETs with higher trapped electron density. Therefore, Coulomb scattering due to trapped electrons is possibly dominant in SiC MOSFETs. In theoretical calculations, the Hall mobility of $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs can be reproduced by considering strong Coulomb scattering due to fixed charges.

In Chapter 6, the author summarizes the important findings on the electron trapping and scattering in SiC MOSFETs obtained from the present study and suggests future work.

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Contents

Chapter 1

Introduction

1.1 Background

The dawn of the semiconductor industry has realized a society where people can live affluently. The first transistor was invented by William Shockley, John Bardeen, and Walter Brattain at Bell Laboratories in Murray Hill, New Jersey, in 1947–1948. Nowadays, semiconductors play an important role in numerous electronic devices, such as integrated circuits (ICs), optical devices, microwave devices, sensors, and power devices.

In the present day, environmental conservation and dealing with the depletion of natural resources are necessary to create a sustainable society in the future. For example, electric vehicles will gradually replace gas-powered vehicles due to the exhaustion of crude oil. As a result, the demand for electric power will increase, and saving electricity must be urgent. In order to use electricity efficiently, reducing electric power loss is one of the most critical issues from the perspective of semiconductor devices.

The electricity used in our society comes from power plants. Its voltage is as high as several hundreds of thousand volts. Therefore, electric power substations and transformers have to regulate and convert the electricity into the proper form [i.e., suitable alternating current (AC)/direct current (DC), voltage, and frequency] by using power devices to be available in our homes and workplaces. However, approximately 10% of the electricity is lost as Joule heat at every electric conversion [1–4]. Thus, further improvement of the power devices is strongly required to reduce the electric power loss.

These days, power devices are almost exclusively fabricated on silicon (Si) owing to its low cost, deep understanding of device physics, and long history of technology. Si-based power devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs), gate turn-off thyristors (GTOs), and insulated-gate bipolar transistors (IGBTs) are practically used as switching devices for power device applications. The extensive studies on Si device physics and processing lead to the highly efficient control of electric power in the present era. However, Si technology is mature, and the performance of Si devices is close to the limit, which is determined by the physical properties of Si.

For further performance enhancement, other materials with superior physical properties for power device applications should be focused.

The specific on-resistance ($R_{\mathrm{on\_sp}}$) and the breakdown voltage (V_{B}) are important parameters in a trade-off relationship to understand the performance of power devices. The $R_{\mathrm{on\_sp}}$ of unipolar devices, such as Schottky barrier diodes (SBDs), MOSFETs, and junction field-effect transistors (JFETs) with non-punch-through structures is given by [5]

$$R_{\mathrm{on\_sp}} = \frac{4V_{\mathrm{B}}^2}{\varepsilon_{\mathrm{s}}\mu_{\mathrm{bulk}}E_{\mathrm{cr}}^3}, \tag{1.1}$$

where ε_{s} is the permittivity of the semiconductor, μ_{bulk} is the bulk mobility, and E_{cr} is the critical electric field. Here, wide-bandgap (E_{g}) semiconductors, such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide ($\mathrm{Ga_2O_3}$), and diamond are expected as the materials for next-generation power devices. The physical properties of these semiconductors are shown in Table 1.1 [1, 6–10]. Wide-E_{g} semiconductors tend to have a high E_{cr}, and thus, they have a lower $R_{\mathrm{on\_sp}}$ compared to that of Si devices. In particular, SiC and its devices are deeply explained in the following Sec. 1.2.

1.2 Silicon Carbide (SiC) Power Devices

SiC is a IV-IV compound semiconductor containing 88% covalent bond and 12% ionic bond. It has superior physical properties for highly efficient power device applications such as a 3 times wider E_{g} and 10 times higher E_{cr} compared to Si [1, 2, 11–18]. SiC devices can be operated at high temperatures owing to its wide E_{g}, and thus extremely low intrinsic carrier concentration at room temperature (RT). Hence, $R_{\mathrm{on\_sp}}$ of SiC unipolar devices can be reduced to 1/500 compared to Si ones owing to its high E_{cr}. Recently, the unipolar limit of SiC was updated based on the latest electron mobility [19] and impact ionization coefficient [20] along the *c*-axis data. The updated unipolar limit is shown in Fig. 1.1 [21]. Note that the unipolar limit in Fig. 1.1 is calculated by considering the punch-through structures. The updated unipolar limit of SiC based on the experimental data overcomes that of Si.

SiC has a lot of polytypes, such as 3C-, 4H-, and 6H-SiC. 4H-SiC, which owns a higher electron mobility (1020 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ for $\perp c$ and 1200 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ for $\parallel c$) compared to 6H-SiC (450 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ for $\perp c$ and 100 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ for $\parallel c$) and higher E_{cr} (2.5–2.8 $\mathrm{MV\ cm^{-1}}$) compared to 3C-SiC (1.4 $\mathrm{MV\ cm^{-1}}$), is particularly suitable for power device applications [1, 13, 15, 16, 22–33]. Therefore, the physical properties of 4H-SiC are written as representative parameters of SiC in Table 1.1.

SiC technology such as crystal growth, defect engineering, and device processing has advanced in the last 2–3 decades and is mature compared to the other wide-E_{g} semiconductors. For example, the high-quality wafers with high-purity epitaxial layers of 150 mm diameter can be fabricated [1, 34, 35], both n- and p-type doping concentrations (N_{D} and

Table 1.1: Physical properties of Si, 4H-SiC, GaN, β-Ga$_2$O$_3$, and diamond at room temperature [1, 6–10].

Property	Si	4H-SiC	GaN	β-Ga$_2$O$_3$	Diamond
Bandgap / eV	1.12	3.26	3.42	4.9	5.5
Electron Mobility / cm^2 V^{-1} s^{-1}	1350	1020 ($\perp c$) 1200 ($\parallel c$)	1400 (Bulk) 2000 (2DEG)	300	4000
Hole Mobility / cm^2 V^{-1} s^{-1}	450	120	30	-	3800
Critical Electric Field / MV cm^{-1}	0.3	2.5–2.8	2.5–2.8	8?	10?
Relative Permittivity	11.9	9.76 ($\perp c$) 10.32 ($\parallel c$)	9.5 ($\perp c$) 10.4 ($\parallel c$)	10	5.7
Thermal Conductivity / W cm^{-1} K^{-1}	1.5	4.9	2.0	0.2	20

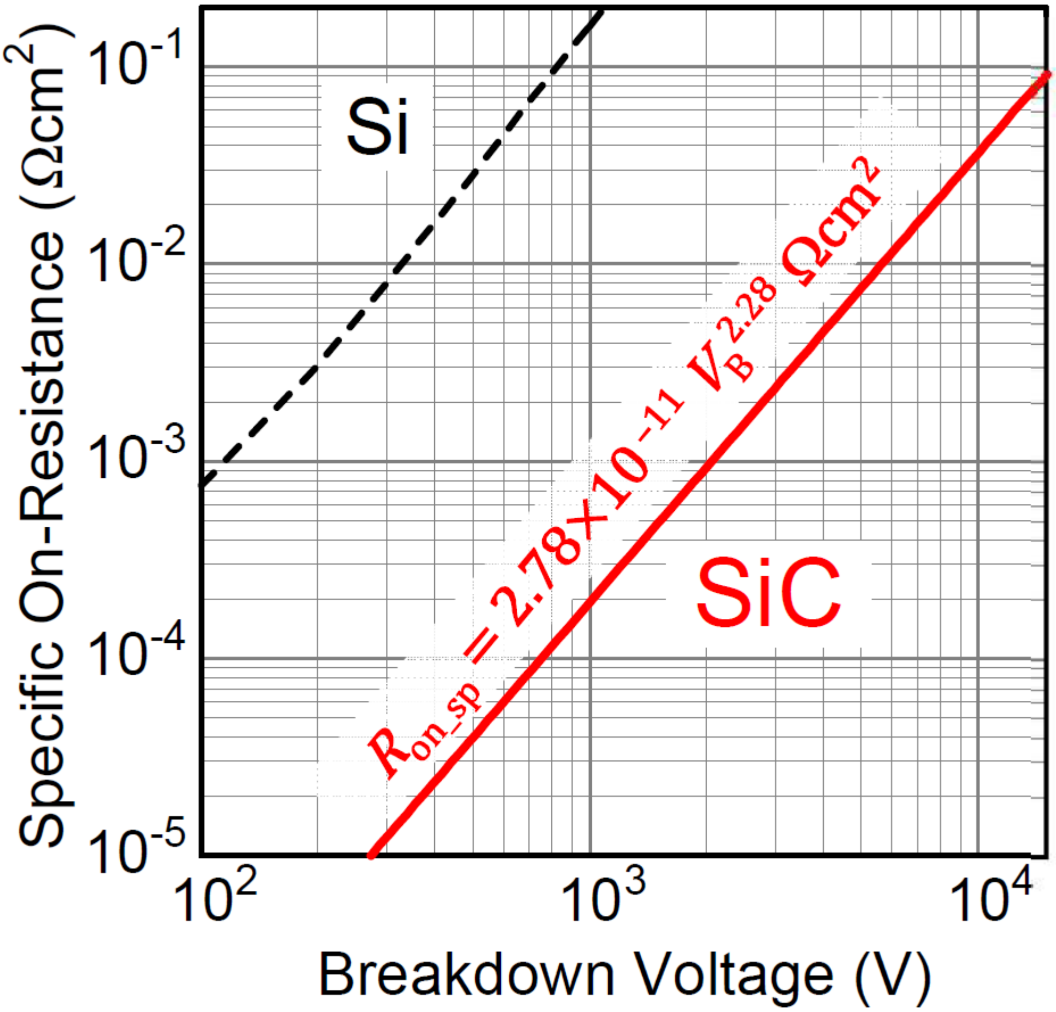

Figure 1.1: Recently updated unipolar limit of SiC based on the latest electron mobility [19] and impact ionization coefficient [20] along the c-axis data [21]. Here, $R_{\mathrm{on\_sp}}$ and V_{B} are the specific on-resistance and the breakdown voltage of the device, respectively.

N_A, respectively) are controllable in a wide range ($10^{14} \leq N_{D,A} \leq 10^{20}$ cm^{-3}) by either epitaxial growth or impurity ion implantation [1, 36, 37]. In addition, SiC is an indirect semiconductor, and thus has a long minority carrier lifetime, which is needed for bipolar devices, such as pin diodes, BJTs, and IGBTs [1]. Furthermore, regarding SiC MOS devices, silicon dioxide (SiO_2), the possible candidate as a gate dielectric for its large E_g, can be formed by either thermal oxidation or deposition. SiC/SiO_2 interfaces have both high conduction and valence band offsets despite the wide-E_g of SiC. For this advantage, the Fowler-Nordheim tunneling current, which directly reflects the reliability of the insulator, can be suppressed in SiC MOSFETs.

Based on the above background, SiC MOSFETs are promising power switching devices for low-loss, high-speed, and high-temperature operations and can replace conventional Si IGBTs. In the present era, SiC MOSFETs are commercially used for many applications, such as traction, vehicles, and home appliances.

1.3 Key Issues of SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

SiC MOSFETs are expected as high-efficiency switching devices. However, critical issues remain in SiC MOSFETs. That is, a high density of interface states limits the drain current of the MOSFETs. As a result, the channel resistance increases and accounts for most of the specific on-resistance. Figure 1.2 shows the specific on-resistance and its components of 600, 1200, and 3300 V class SiC power MOSFETs. Regarding the 3300 V class SiC MOSFETs, the drift resistance is dominant. As for the 600–1200 V class SiC MOSFETs, however, the channel resistance is dominant. The relationship between the channel resistance and interface state density (D_{it}) is unclear. Therefore, predicting SiC MOSFET characteristics is difficult even if the MOSFET structure (e.g., p-body doping concentration and gate oxide thickness) is given. Modeling the drain current has yet to progress for the following reasons.

- Information on energy distribution of D_{it} at SiC/SiO_2 interfaces is lacking.
- Carrier scattering mechanism in SiC MOSFETs is not well understood.

The D_{it} at SiC/SiO_2 interfaces is abnormally high ($D_{it} \sim 10^{13}$ cm^{-2} eV^{-1}) compared to Si/SiO_2 interfaces ($D_{it} \sim 10^{10}$ cm^{-2} eV^{-1}) and a lot of electrons are trapped at the interface states (i.e., electron trapping effect). Then, the effective channel mobility (μ_{eff}), which can be obtained by assuming that all of the electrons induced by applying gate bias are mobile, deviates from the free electron mobility (μ_{free}), which is the true mobility contributed only by mobile electrons. Here, the relationship between μ_{eff} and μ_{free} is expressed by [1]

$$\mu_{\mathrm{eff}} = \frac{n_{\mathrm{free}}}{n_{\mathrm{free}} + n_{\mathrm{trap}}} \mu_{\mathrm{free}}, \tag{1.2}$$

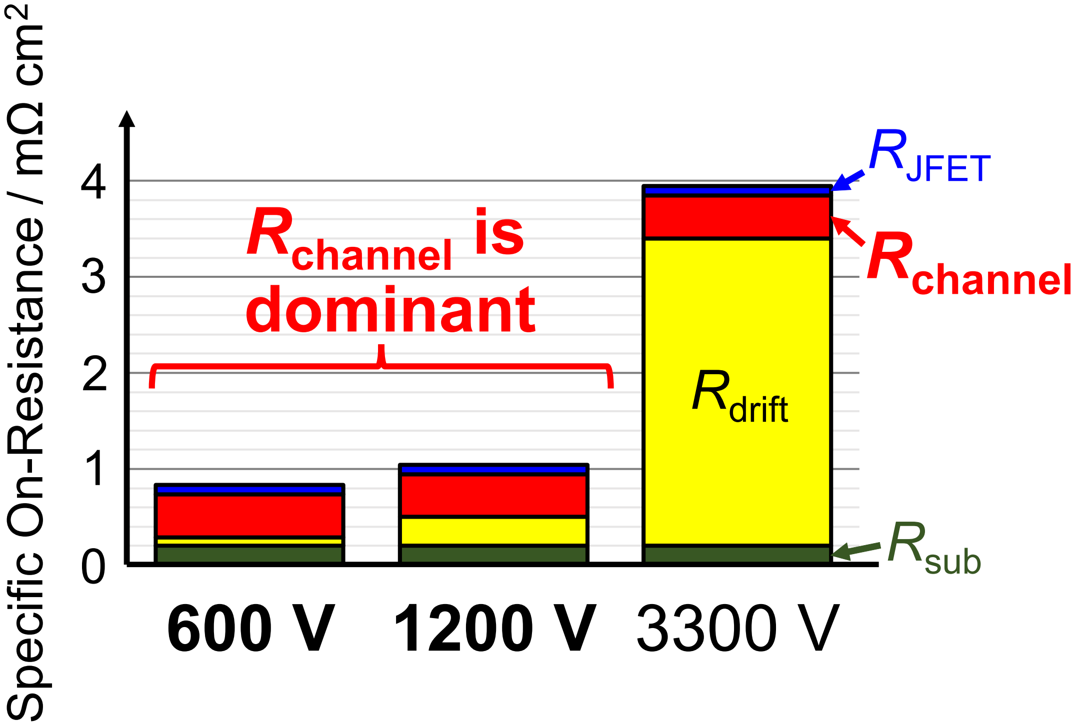

Figure 1.2: Specific on-resistance and its components of 600, 1200, and 3300 V class SiC power MOSFETs. Here, R_{channel} is the channel resistance, R_{drift} is the drift resistance, R_{JFET} is the JFET resistance, and R_{sub} is the substrate resistance. The R_{channel} is dominant for 600–1200 V class SiC MOSFETs.

where n_{free} is the free electron density and n_{trap} is the trapped electron density. Fig. 1.3 shows the schematic illustration of an energy band diagram of a SiC/SiO$_2$ interface. The free electrons can contribute to conduction, and the trapped electrons are immobile. Note that D_{it} has an energy dependence, and the D_{it} in the vicinities of both conduction and valence band edges (E_{C} and E_{V}, respectively) is particularly high. Thus, the D_{it} near E_{C} is very important for the on-state of MOSFETs. The μ_{eff} is given by [1, 38]

$$\mu_{\mathrm{eff}} = \frac{L I_{\mathrm{D}}}{W C_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{T}}) V_{\mathrm{DS}}}, \tag{1.3}$$

where L is the channel length, I_{D} is the drain current, W is the channel width, C_{ox} is the oxide capacitance, V_{GS} is the gate-source voltage, V_{T} is the threshold voltage, and V_{DS} is the drain-source voltage. When μ_{eff} is extracted from the gate characteristics of MOSFETs, the density of total electrons (n_{total}) induced by applying V_{GS} is calculated by [1, 38]

$$n_{\mathrm{total}} = n_{\mathrm{free}} + n_{\mathrm{trap}} \simeq \frac{C_{\mathrm{ox}}}{e} (V_{\mathrm{GS}} - V_{\mathrm{T}}), \tag{1.4}$$

where e is the elementary charge. Therefore, μ_{eff} is extracted by assuming that all of the electrons contribute to conduction even if a lot of electrons are trapped and immobile. As a result, as shown in Eq. 1.2, if the n_{trap} increases, μ_{eff} cannot be assumed to be μ_{free}. Thus, μ_{eff} contains two physical parameters: the ratio of free electrons to total electrons ($n_{\mathrm{free}}/n_{\mathrm{total}}$) and μ_{free}. This complexity makes the modeling of MOSFET characteristics difficult. The modeling of these two parameters is described in detail in the following Sec. 1.3.1 and Sec. 1.3.2.

1.3.1 Interface State Density at SiC/Silicon Dioxide (SiO$_2$) Interfaces

To understand the $n_{\mathrm{free}}/n_{\mathrm{total}}$ in a wide range of V_{GS}, the energy distribution of D_{it}, especially near E_{C}, must be considered. Figure 1.4 shows the schematic illustration of D_{it} distribution. The surface Fermi level (E_{F}) is near E_{C} in the on-state of MOSFETs. Therefore, D_{it} near E_{C} is the crucial parameter for the calculation of n_{trap}. However, D_{it}, which is extracted by the conventional technique [i.e., capacitance (C)–voltage (V) characteristics of MOS capacitors at RT] such as a high-low method [38–40], is obtained only in a deeper energy range ($0.2\ \mathrm{eV} \leq E_{\mathrm{C}} - E_{\mathrm{T}} \leq 0.5\ \mathrm{eV}$) due to the limitation of the measurements at RT [1, 41]. In addition, D_{it} increases exponentially toward E_{C} [42–47]. Thus, other extraction methods of D_{it} near E_{C} should be focused.

In previous studies, conductance [48] and constant-capacitance deep level transient spectroscopy (CC-DLTS) [49, 50] methods were used to extract D_{it} near E_{C} by using MOS capacitors. On the other hand, by using MOSFETs, D_{it} near E_{C} was extracted by MOS-Hall effect measurements [51–53] and by low-temperature subthreshold slopes [46, 54]. In a MOS-Hall effect measurement, n_{trap} is directly obtained by combining split gate-channel

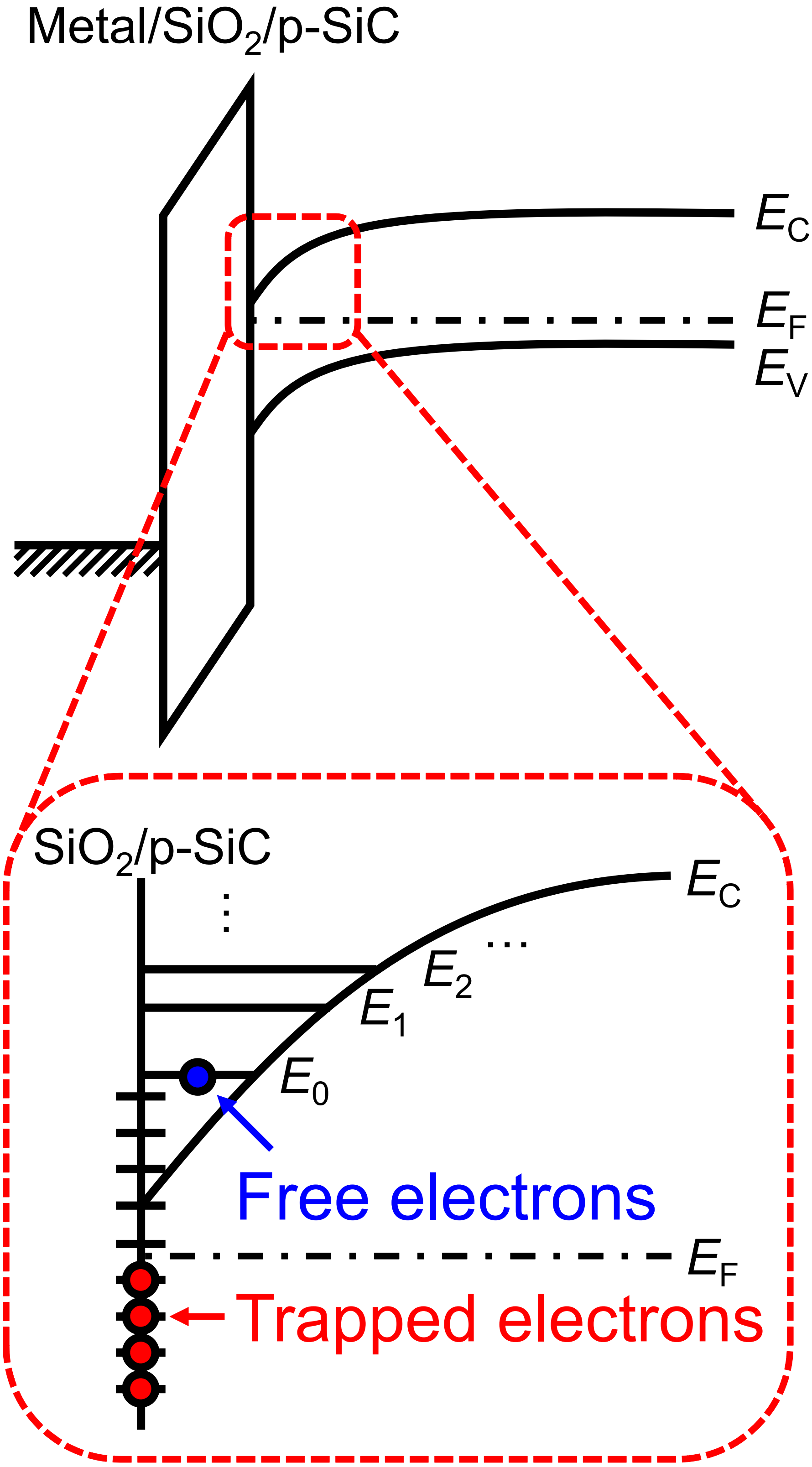

Figure 1.3: Conceptual band diagram of a SiC/SiO$_2$ interface. Here, E_C is the conduction band edge, E_F is the Fermi level, and E_V is the valence band edge. Most of the electrons induced by applying gate bias are trapped at the interface states and do not contribute to conduction.

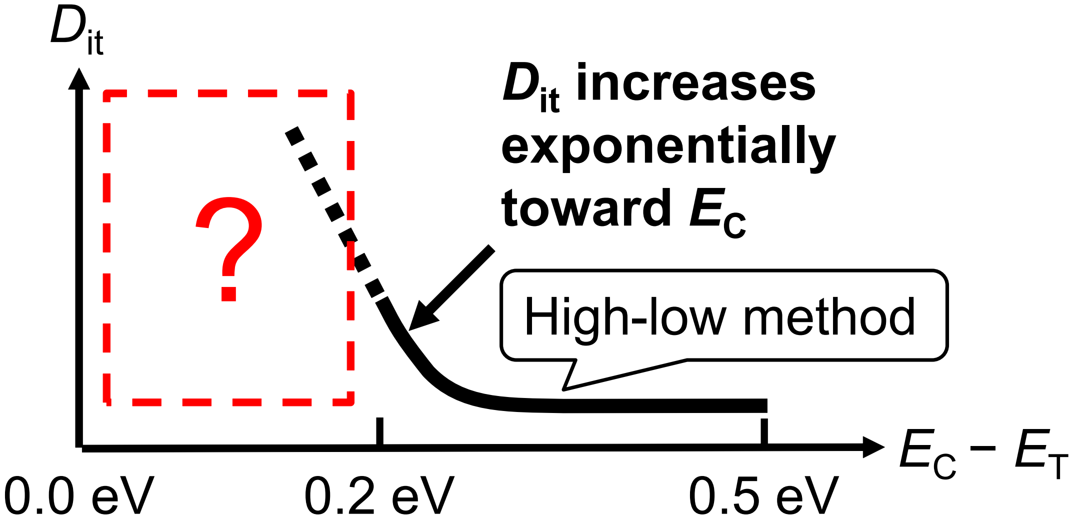

Figure 1.4: Schematic drawing of interface state density ($D_{\rm it}$) distribution. $D_{\rm it}$ in the limited energy range ($0.2\ {\rm eV} \leq E_{\rm C} - E_{\rm T} \leq 0.5\ {\rm eV}$) is accessible by a high-low method of MOS capacitors at room temperature. Here, $E_{\rm C}$ is the conduction band edge. However, $D_{\rm it}$ increases exponentially toward $E_{\rm C}$, and the surface Fermi level ($E_{\rm F}$) is located near $E_{\rm C}$ at on-state of MOSFETs. Therefore, $D_{\rm it}$ near $E_{\rm C}$ is important to determine the trapped electron density.

(C_{GC})–V_{GS} measurement, and D_{it} is given as the differential of n_{trap} with respect to E_{F} [47]. As for the subthreshold slopes, they are directly converted to D_{it}.

Refs. 46, 54, 55 reported that the channel mobility is inversely proportional to the interface state density (D_{it}). Besides, Ref. 47 reported that Hall mobility (μ_{Hall}), which can be assumed to be μ_{free}, does not strongly depend on the gate oxide formation condition. Therefore, a lot of interface states at SiC/SiO$_2$ behave as electron capture centers rather than Coulomb scattering centers. However, the influence of D_{it} at higher energy on mobility is poorly understood (e.g., doping concentration dependence).

Note that the difference in gate oxide formation condition reflects the difference in D_{it}. Figure 1.5 shows the summary of gate oxide formation conditions for Si and SiC MOS structures. As for Si MOS, the gate oxide is formed by dry oxidation followed by forming gas annealing. The D_{it} at Si/SiO$_2$ interfaces is $\sim 1 \times 10^{10}$ cm^{-2} eV^{-1} [39]. In contrast, abnormally high D_{it} ($\sim 10^{13}$ cm^{-2} eV^{-1}) is generated at SiC/SiO$_2$ interfaces after dry oxidation. To reduce the D_{it}, post-oxidation-annealing (POA) such as annealing in nitric oxide (NO) [56–59] or nitrous oxide (N$_2$O) [56, 60, 61] is carried out in many institutions. In the industries, annealing in NO is the current standard process for the production of SiC power MOSFETs. Annealing in NO can reduce D_{it} ($< 10^{12}$ cm^{-2} eV^{-1}) and improve the μ_{eff} to some extent ($\sim$ 30–40 cm^2 V^{-1} s^{-1} for $N_{\mathrm{A}} \sim 10^{15}$ cm^{-3}). Moreover, although phosphoryl chloride (POCl$_3$) annealing [i.e., annealing in a gas mixture of POCl$_3$, oxygen (O$_2$), and nitrogen (N$_2$)] can substantially reduce the D_{it} ($< 10^{11}$ cm^{-2} eV^{-1}) and improve the μ_{eff} ($\sim$ 90–100 cm^2 V^{-1} s^{-1} for $N_{\mathrm{A}} \sim 10^{15}$ cm^{-3}) [62, 63], the POCl$_3$ annealing has some problems [64–66], especially for the oxide reliability.

1.3.2 Carrier Scattering Mechanism in SiC/SiO$_2$ Inversion Layers

In order to predict the MOSFET characteristics, in addition to the $n_{\mathrm{free}}/n_{\mathrm{total}}$ as mentioned in Sec. 1.3.1, the N_{A} of p-body, gate oxide formation process, surface orientation, and temperature dependences of μ_{free}, and thus carrier scattering mechanism in SiC MOSFETs must be clarified. The carrier scattering mechanism is mainly discussed by considering the effective normal field (E_{eff}) dependence of μ_{free}. In Si MOSFETs, the μ_{free}–E_{eff} relationship can be directly obtained from gate characteristics because the μ_{eff} is very close to μ_{free} owing to extremely low n_{trap} in Eq. 1.2. As a result, it was found that the μ_{eff} in Si MOSFETs is limited by Coulomb scattering due to substrate impurities, phonon scattering, and surface roughness scattering [67, 68] as shown in Fig. 1.6. The μ_{free} (and thus, μ_{eff}) can be expressed using Matthiessen's rule as

$$\frac{1}{\mu_{\mathrm{free}}} = \frac{1}{\mu_{\mathrm{C}}} + \frac{1}{\mu_{\mathrm{ph}}} + \frac{1}{\mu_{\mathrm{sr}}}, \tag{1.5}$$

where μ_{C}, μ_{ph}, and μ_{sr} are mobilities limited by Coulomb, phonon, and surface roughness scattering, respectively.

Si

Dry Oxidation + Forming Gas Annealing
D_{it} ~ 1×10^{10} cm^{-2} eV^{-1}

SiC

As-Ox.	Ox.+NO	Ox.+$POCl_3$
D_{it} ~ 10^{13} cm^{-2} eV^{-1}	$D_{\mathrm{it}} < 10^{12}$ cm^{-2} eV^{-1}	$D_{\mathrm{it}} < 10^{11}$ cm^{-2} eV^{-1}
μ_{eff} ~ 5 cm^{2} V^{-1} s^{-1}	μ_{eff} ~ 30–40 cm^{2} V^{-1} s^{-1}	μ_{eff} ~ 90–100 cm^{2} V^{-1} s^{-1}
Low μ_{eff}	Standard used for MOSFET production	V_{T} instability

Figure 1.5: Summary of gate oxide formation conditions for Si and SiC (0001) MOS structures.

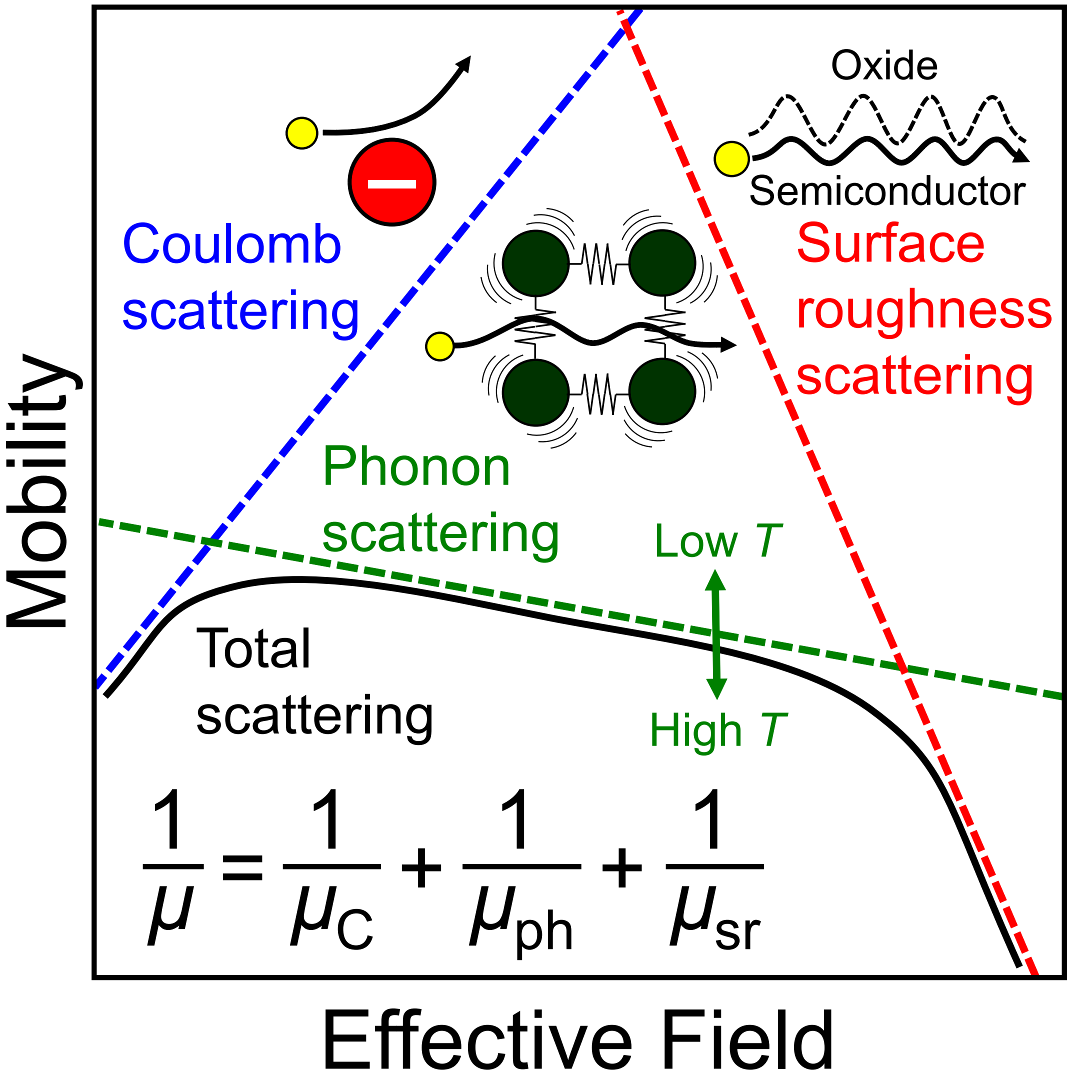

Figure 1.6: Schematic illustration of carrier scattering mechanism in Si MOSFETs. Here, μ is the total mobility, μ_C, μ_{ph}, and μ_{sr} are mobilities limited by Coulomb, phonon, and surface roughness scattering.

However, extraction of μ_{free} from gate characteristics is not easy in SiC MOSFETs because the n_{trap} is not negligible. In addition, the impact of Coulomb scattering due to trapped electrons becomes strong nonlinearly in the high-E_{eff} region because the n_{trap} is increased by applying gate bias in SiC MOSFETs. In contrast, the interface charge density does not change in Si MOSFETs. In order to address this problem, MOS-Hall effect measurements were performed in many institutions [47, 51, 52, 69–102]. Hall effect measurements can detect the free electrons affected by Lorentz force, and μ_{Hall} can be obtained. The μ_{Hall} is equal to μ_{free} if the Hall scattering factor is assumed to be unity. Theoretical studies on carrier scattering mechanism in SiC MOSFETs were also investigated in detail [103–111]. However, the carrier scattering mechanism in SiC MOSFETs is not well understood due to the abnormally low μ_{free}.

Although some essential information on the scattering mechanism was obtained, the scattering mechanism itself is unclear. In particular, MOSFETs annealed in NO, which has a high density of trapped electrons [47], were mainly focused in the previous studies. The electrons trapped at the interface states probably become Coulomb scattering centers and degrade μ_{free}, especially in the high-E_{eff} region because the free electrons are localized very near the interfaces. Therefore, μ_{Hall} of MOSFETs with extremely low D_{it} may be higher than that of MOSFETs with high D_{it}.

Furthermore, the surface orientation dependence of μ_{free} [93, 98, 100] is essential for power device applications. Figure 1.7 shows the schematic device structures of planar- and trench-types vertical MOSFETs [1–4]. Trench-type vertical MOSFETs have some advantages over planar-type vertical MOSFETs, such as no JFET resistance, smaller cell pitch size owing to the vertical channel and no JFET region, and higher μ_{eff}. Figure 1.8(a) shows the schematic drawing of a SiC wafer. SiC (0001) (Si-face) is almost exclusively used for studies on mobility-limiting factors in SiC MOSFETs. Figure 1.8(b) shows the schematic illustration of a primitive cell for 4H-SiC. SiC $(11\bar{2}0)$ (a-face) and $(1\bar{1}00)$ (m-face) are representative orientations for non-polar faces. Figure 1.8(c) shows the schematic device structure of a trench-type vertical MOSFET from the bird's eye view. The channel of a trench-type vertical MOSFET is formed on the trench sidewalls [i.e., $(11\bar{2}0)$ or $(1\bar{1}00)$]. The μ_{eff} of NO-annealed lightly-doped SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs is three times higher than that of MOSFETs on (0001) [55]. However, the scattering mechanism in SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs is hardly investigated. Investigation of similarities and differences in μ_{Hall} of MOSFETs fabricated on various crystal faces is a key to obtaining insight into the scattering mechanism.

1.4 Purpose and Outline of This Study

In this study, the author investigates the energy distribution of D_{it} in the vicinity of E_{C} to understand the effect of carrier trapping at SiC/SiO$_2$ interfaces. Moreover, the author

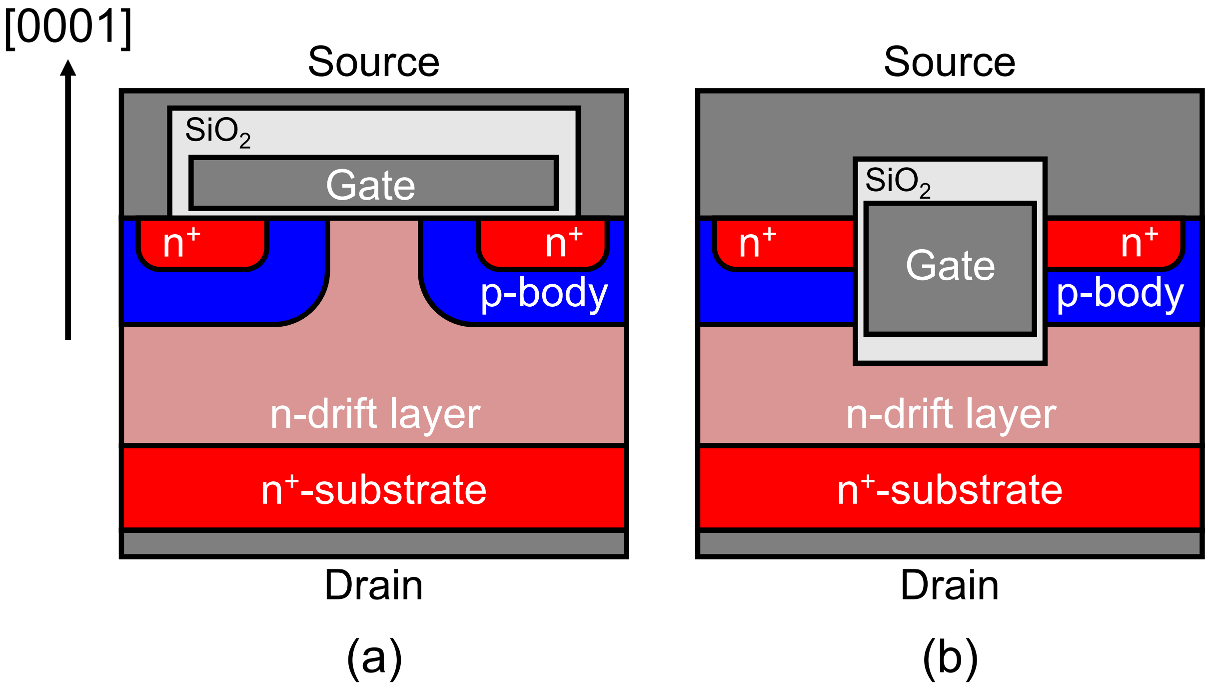

Figure 1.7: Schematic device structures of (a) planar- and (b) trench-types vertical MOSFETs.

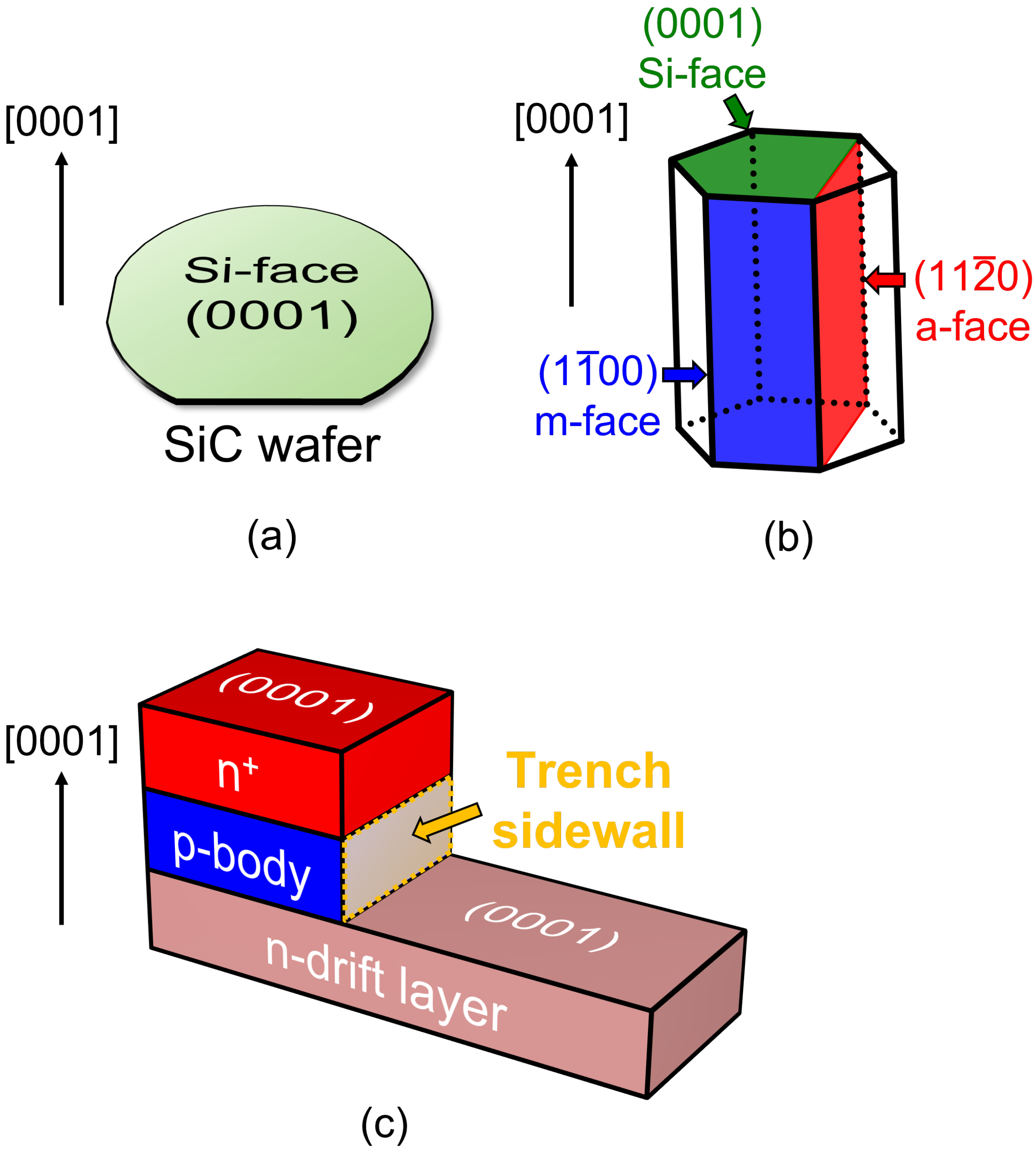

Figure 1.8: (a) Schematic drawing of a SiC wafer. Si-face is almost exclusively used surface orientation for the investigation and production of SiC MOSFETs. (b) Schematic illustration of a primitive cell for 4H-SiC. (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ are known as Si-, a- and m-faces, respectively. (c) Schematic device structure of a trench-type vertical MOSFET from the bird's eye view. Trench sidewalls correspond to non-polar faces, such as $(11\bar{2}0)$ and $(1\bar{1}00)$.

conducts MOS-Hall effect measurements and discusses the carrier scattering mechanism in SiC/SiO$_2$ inversion layers.

In Chapter 2, $D_{\rm it}$ near $E_{\rm C}$ is extracted from gate characteristics of SiC (0001) MOSFETs without POA or annealed in NO with various $N_{\rm A}$ of p-body. The possible origin of $D_{\rm it}$ is discussed by considering inversion layer quantization. Furthermore, the abnormal $\mu_{\rm eff}$ drop for heavily-doped MOSFETs is also investigated.

Next, the author focuses on MOSFETs annealed in POCl$_3$ to obtain extremely low $D_{\rm it}$ and to discuss Coulomb scattering due to trapped electrons.

In Chapter 3, the author extracts $\mu_{\rm eff}$ of SiC (0001) MOSFETs annealed in POCl$_3$ with various $N_{\rm A}$ of p-body and briefly discusses the scattering mechanism. Then, POCl$_3$-annealed MOSFETs with high-purity semi-insulating (HPSI) substrate are also prepared. The author compares the $\mu_{\rm eff}$ of MOSFETs annealed in POCl$_3$ to the phonon-limited mobility reported in the previous study on $\mu_{\rm Hall}$ for MOSFETs annealed in NO. In addition, a body bias technique is adopted, and the author investigates the $\mu_{\rm eff}$ of POCl$_3$-annealed MOSFETs in the high-$E_{\rm eff}$ region.

In Chapter 4, $\mu_{\rm Hall}$ of SiC (0001) MOSFETs without POA, annealed in NO, and annealed in POCl$_3$ with various p-body doping concentrations is investigated. The $n_{\rm total}$ is extracted by split $C_{\rm GC}$–$V_{\rm GS}$ measurements, and $D_{\rm it}$ near $E_{\rm C}$ is obtained for various $N_{\rm A}$. The difference in $\mu_{\rm Hall}$ of MOSFETs annealed in between NO and POCl$_3$ is also discussed. In addition, the $\mu_{\rm Hall}$ at 77 K is investigated to understand the impact of Coulomb scattering due to the trapped electrons. Furthermore, theoretical $\mu_{\rm free}$ is calculated to reproduce the Hall effect results.

In Chapter 5, $\mu_{\rm Hall}$ of SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs annealed in NO with various p-body doping concentrations at RT and 77 K is quantified. In analyses, the $n_{\rm trap}$ and $\mu_{\rm Hall}$ of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs are compared to that of NO- and POCl$_3$-annealed (0001) MOSFETs. The author tries to explain the $\mu_{\rm Hall}$ of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs by using numerical calculation.

In Chapter 6, the summary and future prospects of this study are shown.

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Chapter 2

Energy Distribution of Interface State Density near The Conduction Band Edge

2.1 Introduction

The D_{it} in the vicinity of E_{C} is particularly important to predict the gate characteristics because the surface E_{F} is located near E_{C} in the on-state of MOSFETs. In addition, the D_{it} increases exponentially toward E_{C}. Ref. 1 focused on the nature of interface states (i.e., the drain current is dominantly limited by carrier trapping rather than carrier scattering) and proposed a unique technique to extract D_{it} near E_{C}. In the calculation, the authors assumed the constant μ_{free} because μ_{free} is not changed significantly by applying V_{GS} and determined the D_{it} function by using some fitting parameters to reproduce the gate characteristics of MOSFETs. They confirmed that the D_{it} was not significantly different from the results obtained from MOS-Hall effect measurements.

However, N_{A} dependence of D_{it} near E_{C} is unclear. Actual power MOSFETs have a heavily-doped p-body ($\sim 10^{17}$ cm^{-3}) to avoid short-channel effects. In general, the channel mobility of MOSFETs decreases when N_{A} of p-body increases. For example, in the case of Si MOSFETs, Coulomb scattering by substrate impurities, phonon scattering, and surface roughness scattering are strong in heavily-doped MOSFETs, and the channel mobility gradually decreases [2, 3]. On the other hand, in the case of SiC MOSFETs, the channel mobility sharply drops when N_{A} increases [4]. For this phenomenon, Ref. 5 suggested that the bottom edge of the two-dimensional density of states (2D-DOS) [6] is located at higher energy due to the inversion layer quantization, and D_{it} at higher energy dominantly limits μ_{eff} in MOSFETs with heavily-doped p-body. Ref. 7 investigated D_{it} for various N_{A} by using Hall effect measurements. Nevertheless, the D_{it} was calculated by ignoring the quantum confinement effect. Ref. 8 also reported the results of Hall effect measurements for MOSFETs with various N_{A} of p-body. However, D_{it} of only lightly-doped MOSFETs was obtained. If D_{it} at higher energy is needed for modeling of heavily-doped MOSFETs, D_{it} extracted from lightly-doped MOSFETs does not have a wide enough energy range. Thus, to establish the modeling of $n_{\mathrm{free}}/n_{\mathrm{total}}$, D_{it} in a wide energy range is strongly required.

In this study, to obtain the D_{it} distributions near E_{C}, D_{it} distribution of SiC (0001) MOS structures is determined by reproducing the experimental gate characteristics of as-oxidized and NO-annealed SiC MOSFETs with various N_{A} of p-body on the basis of the numerical calculations considering inversion layer quantization. Thus, potential distributions and energy sub-bands in the inversion layer are calculated by solving Poisson's and Schrödinger equations, respectively [9–11]. This self-consistent calculation is described in detail in Appendix A. The mobility-limiting factors of SiC MOSFETs are discussed based on the obtained results.

In addition to the above, this experiment is a unique attempt to reveal where most of the interface states are located (i.e., in SiO_2, at SiC/SiO_2 interfaces, or in SiC) by analyzing the electrical characteristics of MOSFETs. Figure 2.1 shows the schematic band diagrams of lightly- and heavily-doped MOS interfaces. The quantization effect is weak in the lightly-doped MOSFETs because the density of charges in the depletion layer is small. In the heavily-doped MOSFETs, however, the quantization effect is strong, and the bottom edge of 2D-DOS [E_{C}(2D-DOS)] is located at higher energy due to the high surface electric field. Next, the locations of interface states are focused. The energy of D_{it} at the SiC/SiO_2 interfaces is not varied by inversion layer quantization. In contrast, comparing to D_{it} at SiC/SiO_2 interfaces, D_{it} in SiO_2 shifts to lower energy due to the higher oxide field. In other words, the D_{it} distribution is expected to shift to lower energy by increasing N_{A} if the most of the interface states are formed in SiO_2. On the other hand, D_{it} in SiC shifts to higher energy due to the quantum confinement effect in SiC. Then, the D_{it} distribution is expected to shift to higher energy by increasing N_{A}.

The locations of interface defects were investigated in the previous studies. In general, interface defects created by residual carbon (C) atoms are regarded as the possible origin of interface states [12]. In fact, a high density of C atoms was detected by performing high-temperature annealing in a high-purity argon (Ar) atmosphere [13]. The interface states in SiO_2 are called near-interface traps (NITs) [14]. NITs are possibly generated by C defects [14] such as $C_O{=}C_O$ [15] and $Si_2{-}C{-}O$ [16] and intrinsic oxide defects. The interface defects at the SiC/SiO_2 interfaces are caused by C defects such as C clusters [14, 15] and $C{-}C$ [17] and dangling bonds [18]. More recent studies also considered the interface states in SiC. One of the possible origins is the fluctuation of the conduction band edge of SiC [19–21]. Recently, Ref. 22 reported that $(C_2)_{\mathrm{Si}}$ in SiC, which creates the interface states near E_{C}, is one of the possible candidates of mobility-limiting factors. However, the origin of D_{it} is unclear at the present stage.

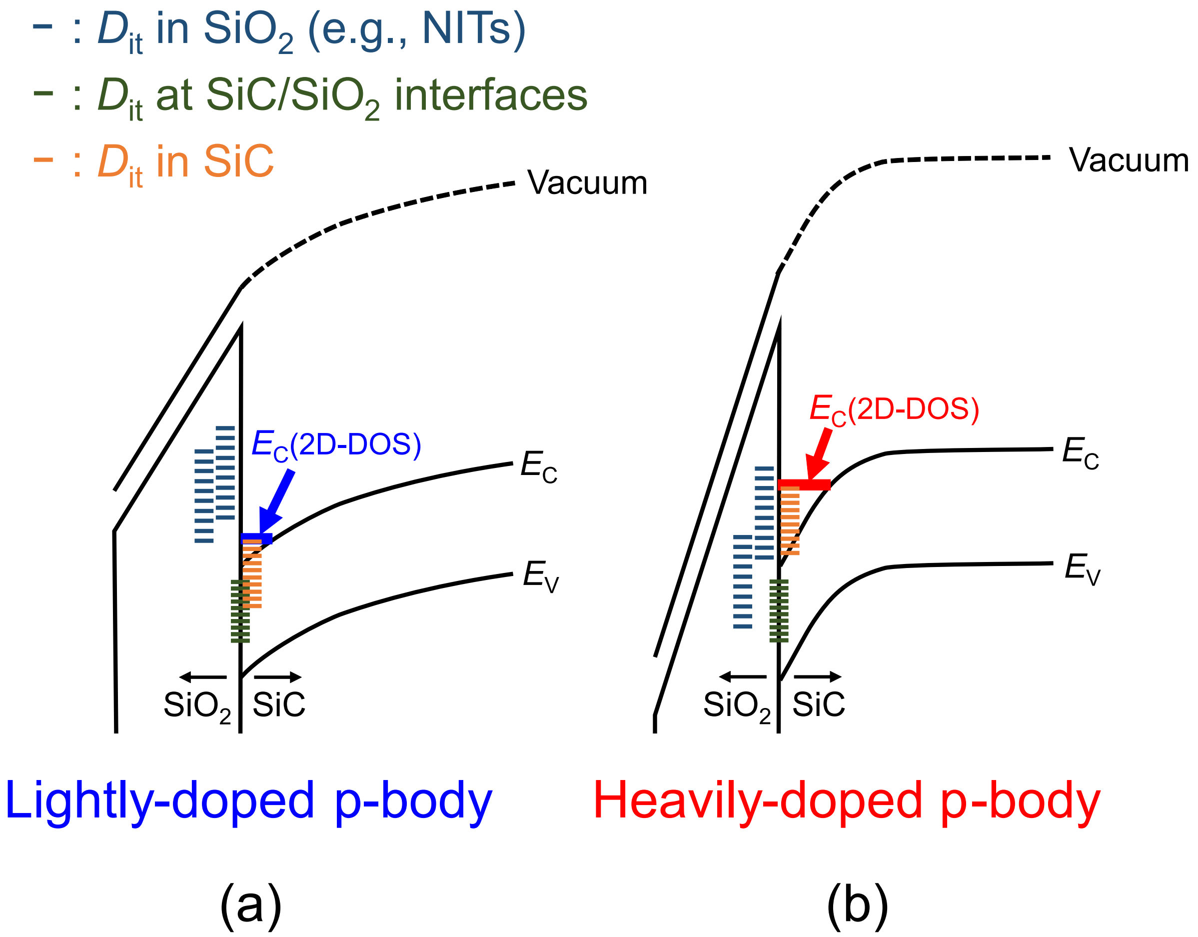

Figure 2.1: Schematic band diagrams of (a) lightly- and (b) heavily-doped SiC MOS interfaces. Three types of D_{it} (i.e., in SiO$_2$, at SiC/SiO$_2$ interfaces, and in SiC) are also shown. In these diagrams, the energy is fixed at the SiC/SiO$_2$ interfaces.

2.2 Device Fabrication

In this study, MOSFETs without POA (As-Ox.) and annealed in NO (Ox.+NO) were prepared. In addition, N_A of p-body was varied from 3×10^{15} cm^{-3} to 1×10^{18} cm^{-3}. Figure 2.2(a) shows the process flow of the fabricated MOSFETs. First of all, aluminum (Al) ions (Al$^+$) were implanted into 8° off-axis p-type 4H-SiC (0001) epitaxial layers ($N_\mathrm{A} = 3 \times 10^{15}$ cm^{-3}) to obtain several p-body doping concentrations ($N_\mathrm{A} = 3 \times 10^{16}$, 1×10^{17}, 3×10^{17}, and 1×10^{18} cm^{-3}). Phosphorus (P) ion (P$^+$) implantation was performed to form source/drain regions ($N_\mathrm{D} = 1 \times 10^{20}$ cm^{-3}). After ion implantation, activation annealing was carried out at 1650°C for 20 min in Ar atmosphere. After sacrificial oxidation, the gate oxides were formed by dry oxidation at 1300°C for 30 min or by dry oxidation with subsequent annealing in NO (10% diluted in N_2) at 1250°C for 70 min. The gate oxide thickness measured by using spectroscopic ellipsometry was about 42 nm. The channel length and width of the MOSFETs were 50 or 100 μm and 200 μm, respectively. All of the measurements were conducted at RT.

2.3 Extraction of Interface State Density from Gate Characteristics

In order to extract the D_it distribution, the gate characteristics of MOSFETs should be calculated [1]. For this reason, how to calculate I_D and V_GS is described in Sec. 2.3.1 and the obtained D_it distribution is discussed in Sec. 2.3.2.

2.3.1 Modeling of Gate Characteristics Considering Carrier Trapping Effect

In general, I_D and V_GS are expressed by [23]

$$I_\mathrm{D} = \frac{W}{L} e n_\mathrm{free} \mu_\mathrm{free} V_\mathrm{DS}, \tag{2.1}$$

$$V_\mathrm{GS} = V_\mathrm{FB} + \psi_\mathrm{S} + \frac{-Q_\mathrm{fix} + e(N_\mathrm{A} - N_\mathrm{D}) z_\mathrm{depl} + e n_\mathrm{free} + e n_\mathrm{trap}}{C_\mathrm{ox}}, \tag{2.2}$$

where V_FB is the flatband voltage, ψ_S is the surface potential, Q_fix is the fixed charge density, z_depl is the depletion layer width. In this study, N_D is negligibly small.

The key to calculating the above equations is how to determine n_free and n_trap. Figure 2.3 shows the conceptual band diagram of a MOS interface for calculating n_free and n_trap. In the calculation, it is assumed that all of the electrons in the inversion layer contribute to conduction with constant μ_free and that all of the electrons trapped at the interface states are immobile.

The n_free is calculated by self-consistently solving Poisson's and Schrödinger equations [9–11]. The calculation procedure is explained in Appendix A. Then, E_F and the energy of

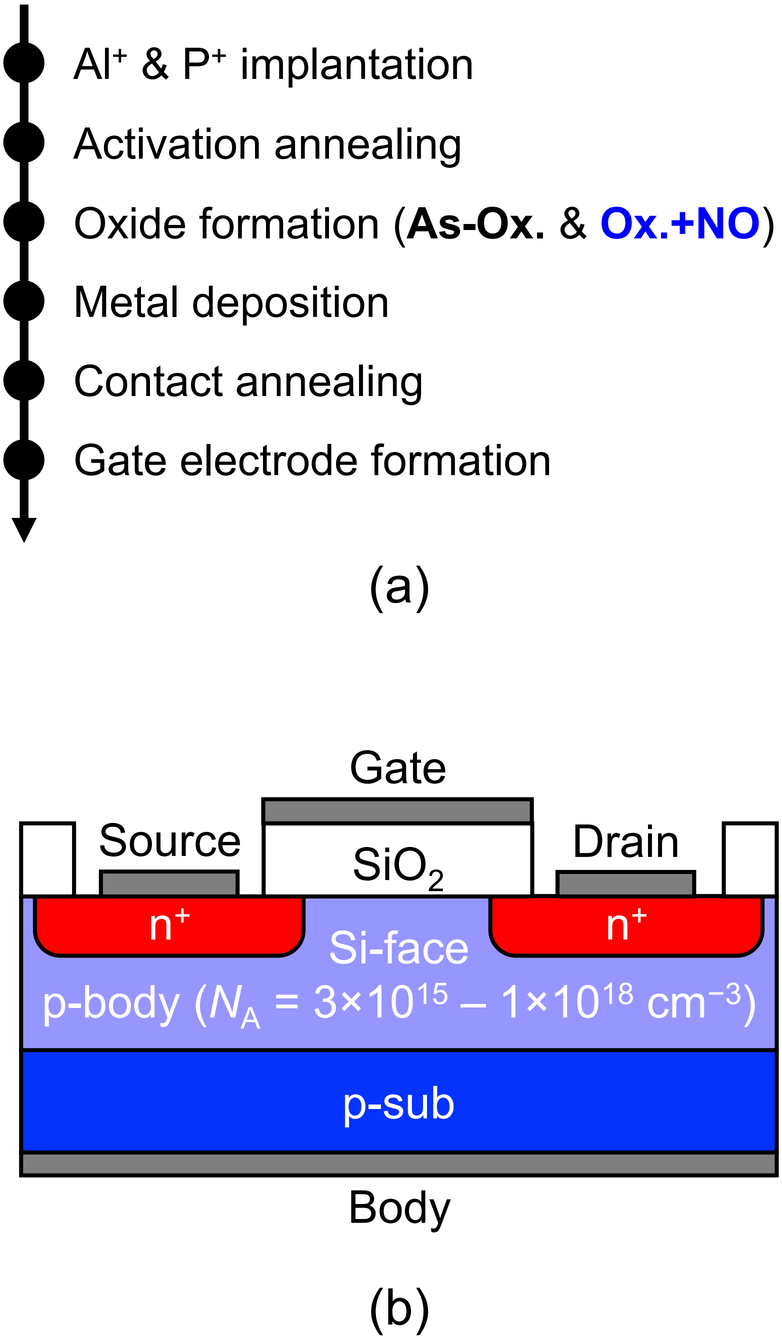

Figure 2.2: (a) Process flow of the fabricated SiC (0001) MOSFETs in this study. (b) Schematic device structure of the fabricated MOSFETs from the cross-sectional view.

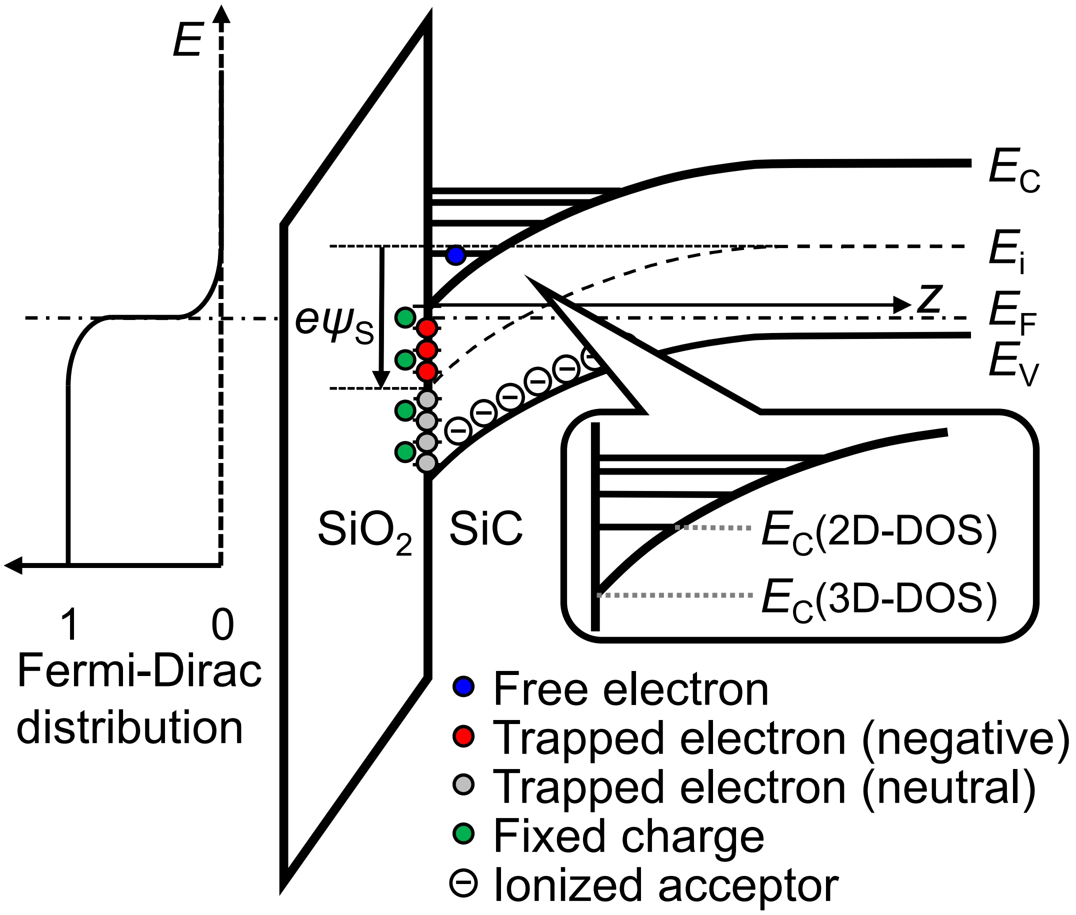

Figure 2.3: Conceptual band diagram of a SiC MOS interface for the calculation of n_{free} and n_{trap}. n_{free} is calculated by self-consistently solving Poisson's and Schrödinger equations. n_{trap} is calculated by integrating the product of D_{it} and Fermi-Dirac distribution with respect to the energy.

the lowest sub-band (E_0) for the lowest conduction band valley (E_0^{1st}) at a given n_{free} are essential parameters to extract D_{it}.

Based on the previously reported Hall mobility of NO-annealed MOSFETs [24], μ_{free} of MOSFETs with p-body doping concentrations of 3×10^{15}, 3×10^{16}, 1×10^{17}, 3×10^{17}, and 1×10^{18} cm^{-3} are assumed to be 100, 35, 25, 15, and 5 cm^2 V^{-1} s^{-1}, respectively, regardless of oxide formation process. Refs. 25, 26 indicated that the Hall mobilities of as-oxidized and NO-annealed MOSFETs are almost the same, making such an assumption reasonable.

Finally, n_{trap} is calculated by [27]

$$n_{\mathrm{trap}} = \int_{E_{\mathrm{i}}}^{\infty} \frac{D_{\mathrm{it}}}{1 + \exp\left(\dfrac{E - E_{\mathrm{F}}}{k_{\mathrm{B}}T}\right)} \, \mathrm{d}E, \tag{2.3}$$

where E_{i} is the intrinsic level of SiC, E is the energy, k_{B} is the Boltzmann constant, and T is the absolute temperature. The interface states below E_{i} and above E_{i} are donor- and acceptor-like states, respectively, as shown in Fig. 2.3. The D_{it} distribution is assumed to be expressed by [28, 29]

$$D_{\mathrm{it}} = D_0 + D_1 \exp\left[\frac{E - E_{\mathrm{C}}(\text{3D-DOS})}{E_1}\right] + D_2 \exp\left[\frac{E - E_{\mathrm{C}}(\text{3D-DOS})}{E_2}\right], \tag{2.4}$$

where E_{C}(3D-DOS) is the bottom edge of the three-dimensional density of states (3D-DOS), D_0, D_1, D_2, E_1, E_2, and Q_{fix} in Eq. 2.2 are fitting parameters to reproduce the experimental gate characteristics of MOSFETs.

Figure 2.4 shows the experimental and calculated gate characteristics for as-oxidized and NO-annealed MOSFETs with lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{15}$ cm^{-3}) and heavily-doped ($N_{\mathrm{A}} = 1 \times 10^{18}$ cm^{-3}) p-bodies. The calculated I_{D}–V_{GS} curves can reproduce the experimental ones in the range of $0 \text{ V} \leq V_{\mathrm{GS}} \leq 15$ V, which corresponds to the energy range of $E_{\mathrm{C}}(\text{3D-DOS}) - 0.38 \text{ eV} \leq E_{\mathrm{T}} \leq E_{\mathrm{C}}(\text{3D-DOS}) + 0.18$ eV.

2.3.2 Energy Distribution of Interface State Density

Figure 2.5(a) shows the energy distribution of D_{it} plotted with respect to E_{C}(3D-DOS) obtained from the gate characteristics in Fig. 2.4. The D_{it} in Fig. 2.5(a) strongly depends on N_{A}. In addition, the D_{it} decreases when the N_{A} increases. For example, the D_{it} of the lightly-doped MOSFET is five times higher than that of the heavily-doped MOSFET. In Sec. 2.1, the dependence of D_{it} distribution on the location of interface states is discussed. In this case, it can be seen that the D_{it} distribution shifts to higher energy by increasing N_{A}. Here, the D_{it} plotted with respect to E_{C}(2D-DOS) [$= E_{\mathrm{C}}(\text{3D-DOS}) + E_0^{\mathrm{1st}}$] is shown in Fig. 2.5(b). The 2D-DOS (D_{2D}) was calculated by [6] $D_{\mathrm{2D}} = n_v m_{\mathrm{d}} k_{\mathrm{B}} T / \pi \hbar^2$, where n_v is the number of the equivalent valley, m_{d} is the density-of-states effective mass, and $\hbar$ is the Dirac constant. In contrast to the D_{it} in Fig. 2.5(a), the D_{it} in Fig. 2.5(b) is uniquely

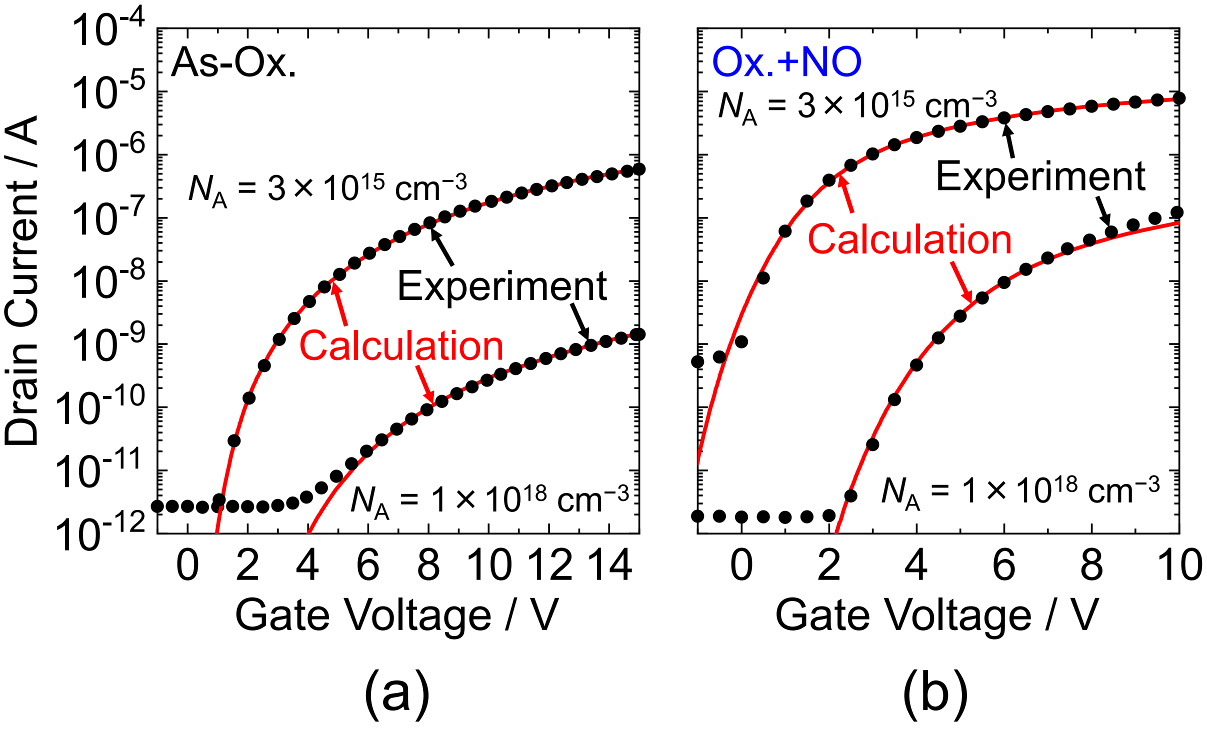

Figure 2.4: Experimental and calculated gate characteristics for (a) as-oxidized and (b) NO-annealed SiC (0001) MOSFETs with lightly-doped ($N_A = 3 \times 10^{15}$ cm^{-3}) and heavily-doped ($N_A = 1 \times 10^{18}$ cm^{-3}) p-bodies.

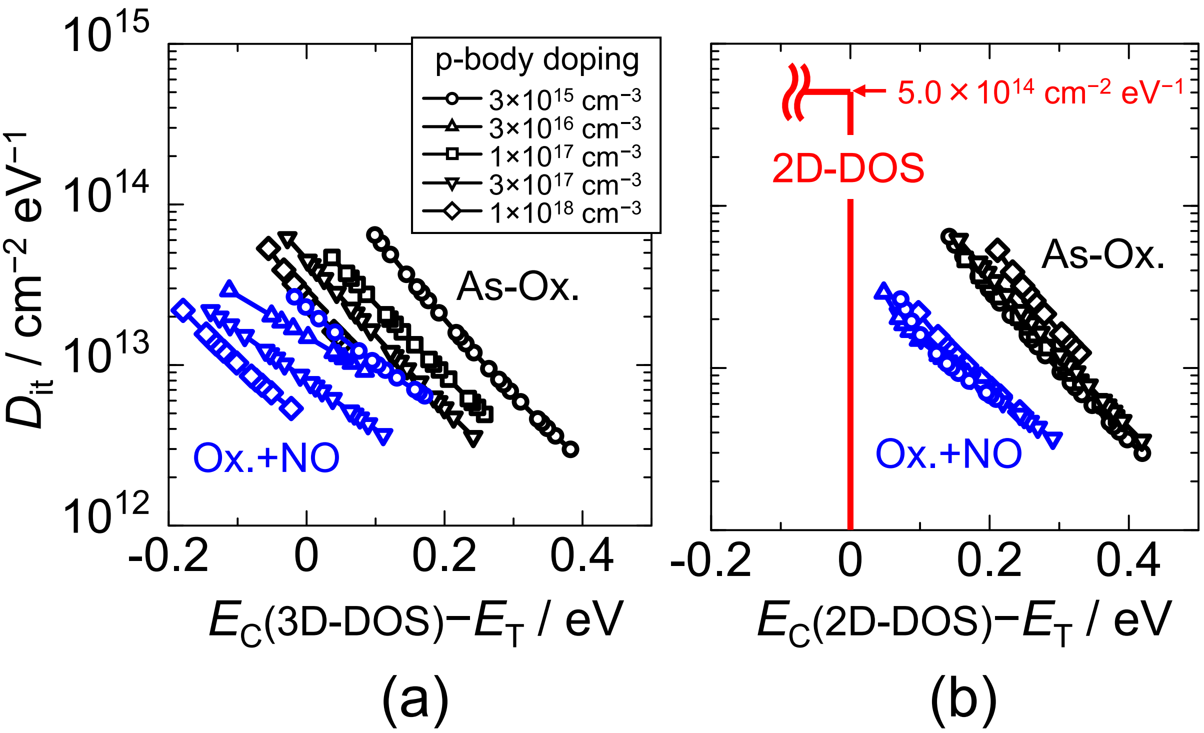

Figure 2.5: Interface state density ($D_{\rm it}$) distributions plotted with respect to the bottom edge of (a) three-dimensional density of states (3D-DOS) and (b) two-dimensional density of states (2D-DOS) obtained from the gate characteristics of as-oxidized and NO-annealed SiC (0001) MOSFETs with various p-body acceptor concentrations.

determined by the gate oxide formation condition and independent of N_A. In other words, the D_it follows the energy shift of E_C(2D-DOS), and therefore D_it originates from the SiC side.

Here, the validity of D_it for the assumption of constant μ_free should be discussed. In Ref. 24, μ_Hall of the lightly-doped ($N_\mathrm{A} = 2 \times 10^{15}$ cm^{-3}) MOSFETs is varied in the range of 80–120 cm^2 V^{-1} s^{-1}, and that of the heavily-doped MOSFETs ($N_\mathrm{A} = 4 \times 10^{17}$ cm^{-3}) is varied in the range of 10–20 cm^2 V^{-1} s^{-1}. Then, the D_it is also extracted by assuming different constant μ_free in Fig. 2.6. Figure 2.6(a) shows the D_it plotted with respect to E_C(2D-DOS) by assuming three different constant μ_free (80, 100, 120 cm^2 V^{-1} s^{-1}) for the lightly-doped ($N_\mathrm{A} = 3 \times 10^{15}$ cm^{-3}) MOSFETs, and Fig. 2.6(b) shows the D_it plotted with respect to E_C(2D-DOS) by assuming three different constant μ_free (10, 15, 20 cm^2 V^{-1} s^{-1}) for the heavily-doped ($N_\mathrm{A} = 3 \times 10^{17}$ cm^{-3}) MOSFETs. The D_it is slightly affected by the assumption of Hall mobility for the following reason. If the μ_free is varied in ±20%, the n_free is varied in -17%–$+25\%$ to reproduce the same I_D. However, the n_trap of SiC MOSFETs is abnormally high even after NO annealing. Thus, to reproduce the same V_GS (i.e., $n_\mathrm{free}+n_\mathrm{trap}$), the n_trap (i.e., D_it) is not strongly affected by changing n_free (i.e., μ_free). In addition, μ_free is not changed significantly by applying the gate bias [24]. Therefore, using the constant μ_free is a reasonable assumption.

2.4 Discussion

Figure 2.7 shows the $n_\mathrm{free}/n_\mathrm{total}$ as a function of n_free for as-oxidized and NO-annealed MOSFETs with various N_A of p-body. The difference in $n_\mathrm{free}/n_\mathrm{total}$ between as-oxidized and NO-annealed MOSFETs reflects the difference in D_it. On the other hand, the p-body doping dependence of D_it is quite small. Therefore, the same $n_\mathrm{free}/n_\mathrm{total}$ in lightly-doped MOSFETs can be used for modeling of the electron trapping effect in heavily-doped MOSFETs. In this case, it can be explained that the sharp mobility drop, which is observed in the heavily-doped MOSFETs [4], is attributed to the influence of electron scattering [24] rather than that of electron trapping. Hence, further investigation of Hall effect measurements is required to understand why the sharp μ_free drop occurs.

Recently, Refs. 20, 21 suggested that the interface states originate from the tail of 2D-DOS by characterizing wet-oxidized MOSFETs at cryogenic temperatures and concluded that variable-range hopping (VRH) [30, 31] is the main conduction mechanism in the tail states. However, the VRH is only dominant at extremely low temperatures (≤ 50 K) [20]. In addition, the D_it obtained in this study is extracted by assuming that all of the electrons trapped at the interfaces are immobile and do not contribute to conduction. Therefore, the nature of D_it in the present study is different from that in the previous studies [20, 21].

Ref. 19 suggested that 4H-SiC (0001) (k-site)/SiO$_2$ and 4H-SiC (0001) (h-site)/SiO$_2$ have different conduction band edges revealed by a density-functional theory (DFT) [32, 33]

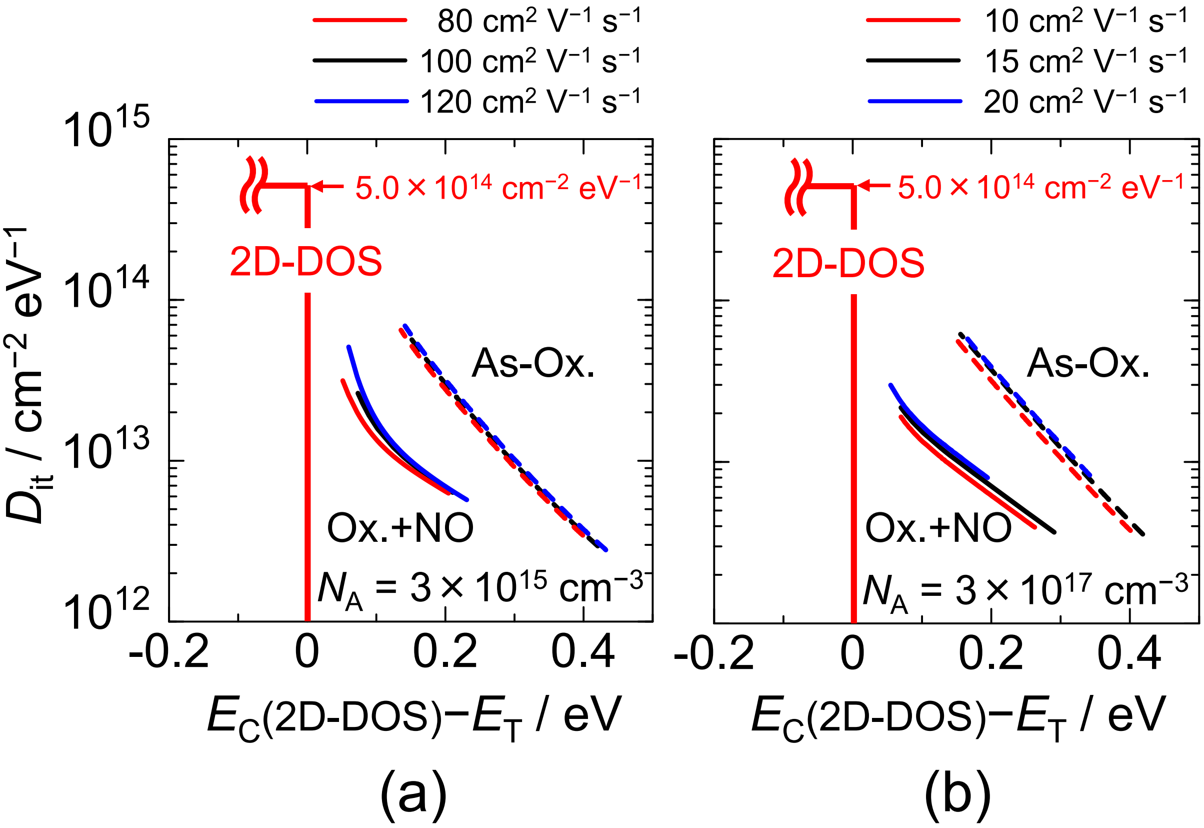

Figure 2.6: Interface state density (D_{it}) distributions plotted with respect to the bottom edge of the two-dimensional density of states (2D-DOS) extracted by assuming different constant free electron mobilities for (a) lightly- ($N_{\mathrm{A}} = 3 \times 10^{15}$ cm^{-3}) and (b) heavily-doped ($N_{\mathrm{A}} = 3 \times 10^{17}$ cm^{-3}) SiC (0001) MOSFETs.

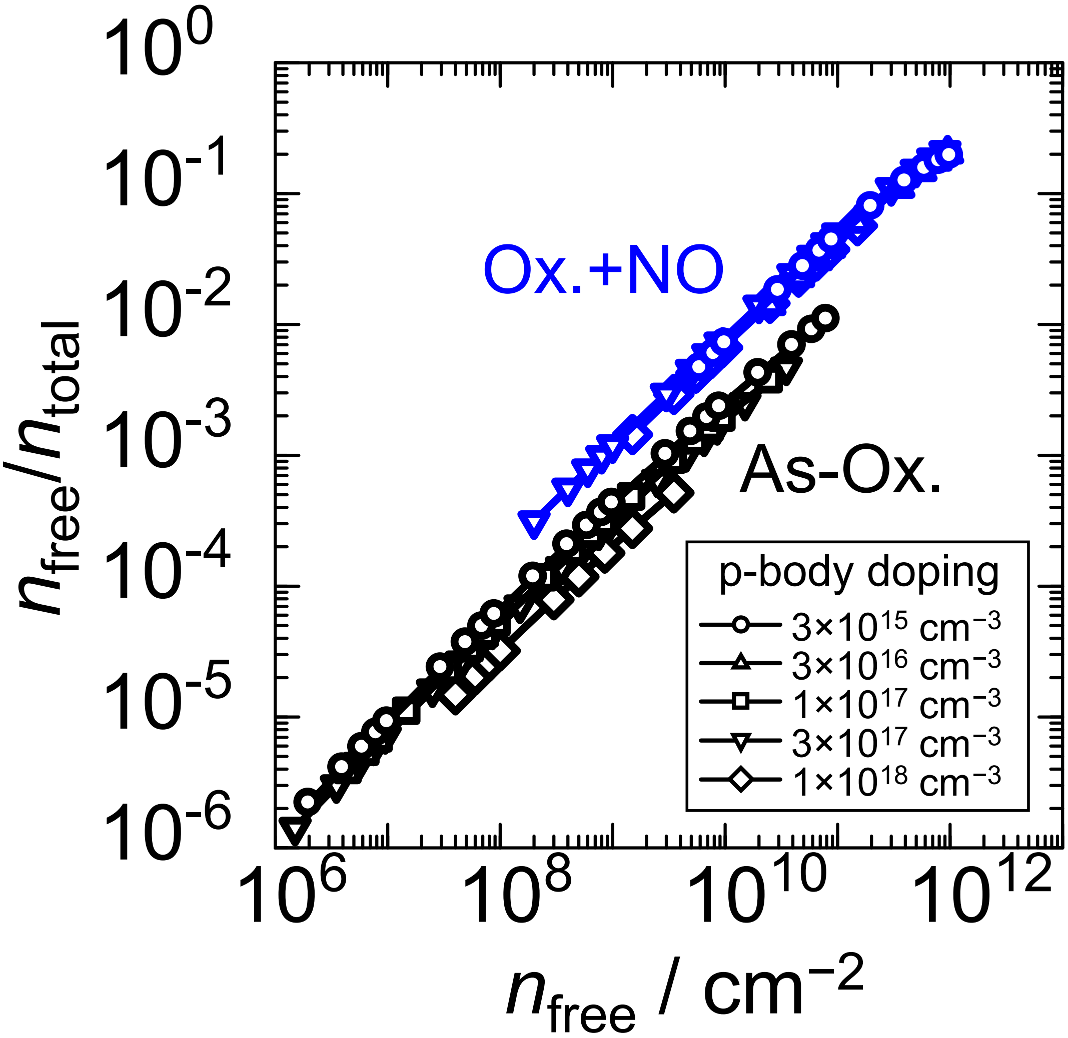

Figure 2.7: Ratio of free electrons to total electrons ($n_{\text{free}}/n_{\text{total}}$) as a function of the free electron density (n_{free}) for as-oxidized and NO-annealed SiC (0001) MOSFETs with various p-body acceptor concentrations (3×10^{15} cm^{-3} $\leq N_{\text{A}} \leq 1 \times 10^{18}$ cm^{-3}).

calculation. Therefore, the conduction band edge of SiC is not determined as a certain energy, which implies that the fluctuation of the conduction band edge may occur. By contrast, as for the non-polar orientation, such as a- and m-faces, this phenomenon does not occur [19]. Thus, D_{it} at SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ with various p-body doping/SiO_2 interfaces should be investigated in the future.

The D_{it} of SiC MOS structures formed by oxidation-minimizing processes, which suppress the oxidation of SiC [34–37], is significantly small. From these results, it can be concluded that at least the D_{it} in SiC is the dominant mobility-limiting factors of MOSFETs.

2.5 Summary

In summary, the D_{it} distribution near the conduction band edge in 4H-SiC (0001)/SiO_2 systems is extracted by reproducing the experimental I_{D}–V_{GS} characteristics of MOSFETs with a numerical calculation. In the calculation, energy sub-bands in the inversion layer are calculated by self-consistently solving Poisson's and Schrödinger equations. The obtained D_{it} distribution is uniquely determined by the oxide formation process (As-Ox. or Ox.+NO) and independent of the acceptor concentration (3×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{18}$ cm^{-3}). In addition, the ratio of the free electrons to the total electrons increases by annealing in NO, which can be seen that the drain current increases in the NO-annealed MOSFETs owing to the increase in the free electron density. In contrast, the $n_{\mathrm{free}}/n_{\mathrm{total}}$ is almost identical among MOSFETs with various N_{A}. This result implies that the drain current decrease observed in heavily-doped MOSFETs is mainly ascribed to the decrease in the free electron mobility rather than the decrease in the free electron density.

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Chapter 3

Effective Channel Mobility in SiC MOSFETs Annealed in Phosphoryl Chloride with Adopting Body Bias Technique

3.1 Introduction

In Chapter 2, the author revealed that μ_{eff} of as-oxidized and NO-annealed MOSFETs with high N_{A} of p-body is abnormally low due to the decrease in μ_{free}. Therefore, the reason why the abnormal decrease in μ_{free} occurs in heavily-doped MOSFETs should be clarified.

Recently, Refs. 1, 2 reported that Hall mobility does not strongly depend on the oxide formation process comparing two types of MOSFETs (i.e., MOSFETs formed by dry oxidation only and by dry oxidation followed by NO annealing). This result implies that the influence of interface states on μ_{free} is small. In addition, Refs. 3, 4 reported that μ_{Hall} sharply drops in the high-E_{eff} region, which is a similar tendency of μ_{eff} in heavily-doped MOSFETs. In particular, Ref. 4 determined the phonon-limited mobility, the highest mobility limit in SiC MOSFETs. However, the phonon-limited mobility (e.g., 163 cm^2 V^{-1} s^{-1} at $E_{\mathrm{eff}} = 0.1$ MV cm^{-1}) is much lower than that in Si MOSFETs, comparing the ratio of μ_{bulk}. The ratio of bulk mobility for SiC [μ_{bulk}(SiC) $\sim$ 1000 cm^2 V^{-1} s^{-1} [5]] to that for Si [μ_{bulk}(Si) $\sim$ 1500 cm^2 V^{-1} s^{-1} [6]] is $\sim$0.67. Although it should be close to the ratio of phonon-limited mobility [μ_{ph}(SiC)] for SiC to that for Si [μ_{ph}(Si)] in the low-E_{eff} region, the μ_{ph}(SiC)/μ_{ph}(Si) obtained by Ref. 4 is 0.25 at $E_{\mathrm{eff}} = 0.05$ MV cm^{-1}. In contrast, Ref. 7 reported that SiC MOSFETs with an extremely low doping concentration obtained by counter doping show very high Hall mobility of 800 cm^2 V^{-1} s^{-1} compared to the reported phonon-limited mobility [4]. The theoretical study [8] also found that the experimentally determined phonon-limited mobility [4] cannot be reproduced by considering only phonon scattering. One of the most important findings is that the N_{A} of p-body does not strongly influence μ_{free}, which is revealed by adopting a body bias technique [9–11]. In other words, the impact of Coulomb scattering by ionized acceptors on μ_{free} is small in SiC MOSFETs.

In the previous studies, the μ_{free} in SiC MOSFETs has been investigated using MOSFETs annealed in NO and without POA [1, 3, 4]. However, Ref. 1 reported that the $n_{\mathrm{free}}/n_{\mathrm{total}}$ was quite low even after NO annealing. Therefore, Coulomb scattering by electrons trapped at the interface states is probably strong in NO-annealed MOSFETs. The trapped electrons are localized at the SiC/SiO$_2$ interfaces. Then, free electrons in the heavily-doped MOSFETs approach the MOS interfaces in the high-E_{eff} region and can be strongly affected by Coulomb scattering due to the trapped electrons. Thus, the μ_{Hall} of NO-annealed MOSFETs reported in the previous study [4] may not be dominantly limited by the phonon scattering.

In this chapter, the author focuses on annealing in POCl$_3$ [12, 13], which can substantially reduce n_{trap}. As already mentioned in Chapter 1, POCl$_3$ annealing can achieve extremely low D_{it} ($< 10^{11}$ cm^{-2} eV^{-1}). Therefore, Coulomb scattering due to trapped electrons is possibly small in POCl$_3$-annealed MOSFETs. In addition, POCl$_3$-annealed lightly-doped MOSFETs show a high μ_{eff} ($\sim$ 90 cm^2 V^{-1} s^{-1}) [13], which is close to the reported μ_{Hall} ($\sim$ 100 cm^2 V^{-1} s^{-1}) of NO-annealed MOSFETs [1, 4]. This result suggests that the n_{trap} of POCl$_3$-annealed MOSFETs is negligibly small, indicating that μ_{eff} can be assumed to be μ_{free} in POCl$_3$-annealed MOSFETs as shown in Eq. 1.2. Therefore, to briefly discuss the scattering mechanism in SiC MOSFETs, μ_{eff} of POCl$_3$-annealed MOSFETs is investigated in this study.

First, MOS-Hall effect measurements are performed to investigate the carrier trapping effect in POCl$_3$-annealed MOSFETs. MOSFETs annealed in NO or POCl$_3$ are prepared to compare the carrier trapping effect. Next, field-effect mobility and subthreshold slope for MOSFETs with various N_{A} obtained from gate characteristics are discussed. The μ_{eff} of POCl$_3$-annealed MOSFETs in the low-E_{eff} region is obtained using high-purity semi-insulating (HPSI) substrates. MOS structures fabricated on HPSI substrates can realize minimal band bending because the Fermi level is located near the midgap of SiC. As a result, POCl$_3$-annealed MOSFETs on HPSI substrates are expected to show very high mobility. Therefore, MOSFETs on HPSI substrates are useful for investigating the validity of the reported phonon-limited mobility [4]. On the other hand, the μ_{eff} in the high-E_{eff} region is extracted by applying negative body-source voltage (V_{BS}) [9–11]. The body bias technique, which can vary the depletion charge density (N_{depl}), is explained in Sec. 3.3.

3.2 Device Fabrication

Figure 3.1(a) shows the process flow of the fabricated MOSFETs. In this study, p-type 4H-SiC (0001) epitaxial layers (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{15}$ cm^{-3}) and HPSI substrates were used. To vary the p-body doping concentrations ($N_{\mathrm{A}} = 3 \times 10^{16}$, 1×10^{17}, 3×10^{17}, 1×10^{18}, and 3×10^{18} cm^{-3}), Al$^+$ ion implantation was performed. The source/drain

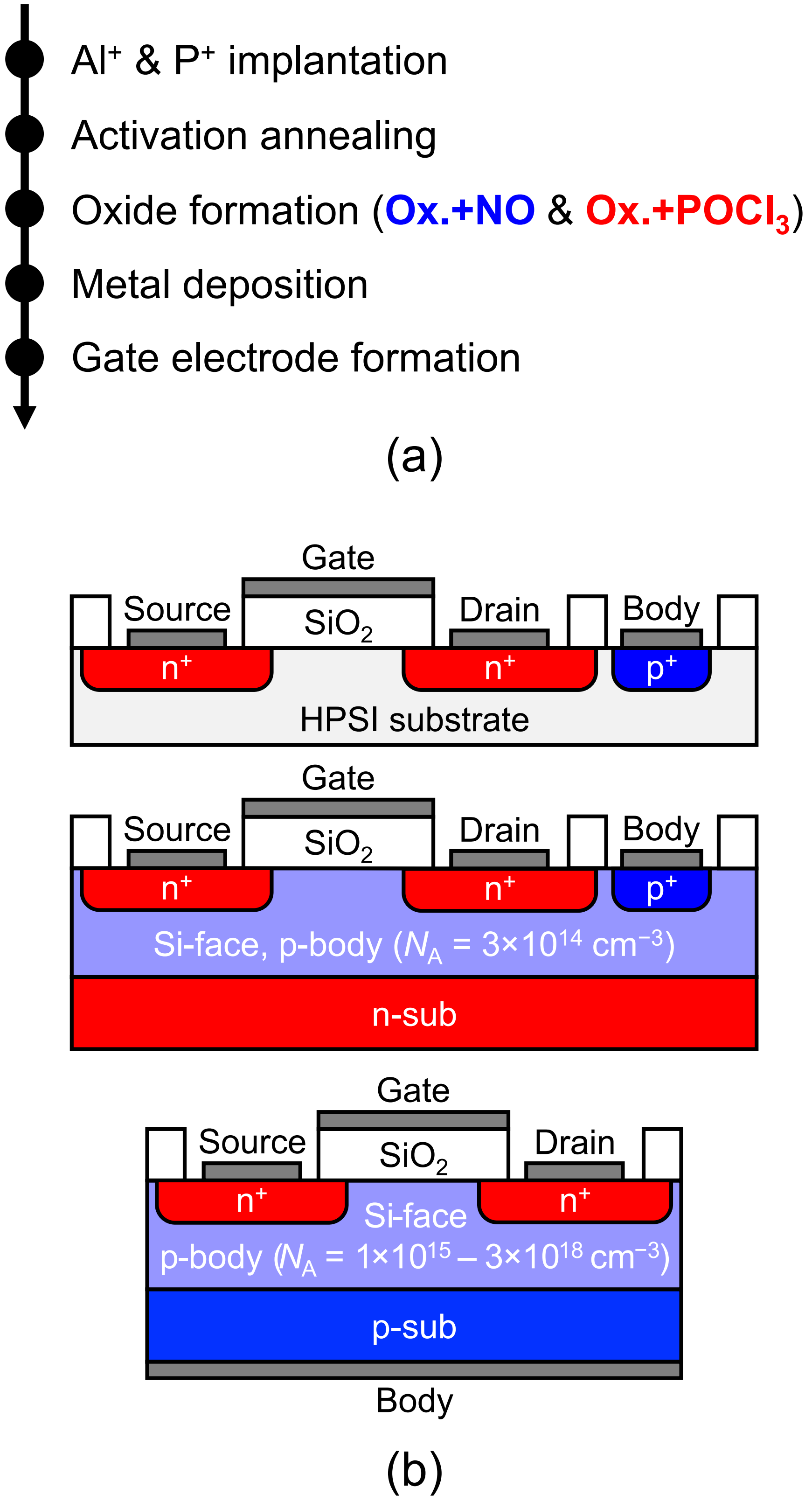

Figure 3.1: (a) Process flow of the fabricated SiC (0001) MOSFETs in this study. (b) Schematic device structures of the fabricated MOSFETs from the cross-sectional view.

regions ($N_\mathrm{D} = 1.0 \times 10^{20}$ cm^{-3}) and body regions ($N_\mathrm{A} = 1.6 \times 10^{20}$ cm^{-3}) were formed by P$^+$ and Al$^+$ ions implantation, respectively. After ion implantation, activation annealing was carried out at 1750°C for 20 min in an Ar atmosphere. The gate oxides were formed by dry oxidation at 1300°C for 30 min with subsequent annealing in NO (10% diluted in N$_2$) at 1250°C for 70 min or by dry oxidation with subsequent annealing in POCl$_3$ (annealing in a gas mixture of POCl$_3$, O$_2$, and N$_2$) at 1000°C for 10 min. After the POCl$_3$ annealing, N$_2$ annealing was also performed at 1000°C for 30 min. The gate oxide thicknesses were about 42 nm and 58 nm for NO- and POCl$_3$-annealed MOS structures. The channel length and width of the MOSFETs were 500 μm and 100 μm, respectively. The schematic resultant device structures are described in Fig. 3.1(b). All of the measurements were conducted at RT.

3.3 Body Bias Technique

In this section, how to control the E_eff by changing V_BS is explained in detail. Figure 3.2(a) shows the schematic measurement system when the body bias technique is adopted. When V_BS is applied, the N_depl is given by [9, 11]

$$N_\mathrm{depl} = \sqrt{\frac{2\varepsilon_\mathrm{SiC}(N_\mathrm{A} - N_\mathrm{D})(\psi_\mathrm{S} - V_\mathrm{BS})}{e}}, \tag{3.1}$$

where ε_SiC is the permittivity of SiC. In this study, ψ_S is assumed to be $2\psi_\mathrm{B}$, where ψ_B is the bulk potential. The above equation shows that the N_depl is increased by applying negative V_BS. Here, the E_eff is expressed by [14]

$$E_\mathrm{eff} = \frac{e(N_\mathrm{depl} + \eta n_\mathrm{free})}{\varepsilon_\mathrm{SiC}}, \tag{3.2}$$

where η is a parameter that indicates how much the electrons contribute to the E_eff. In general, η is assumed to be 1/3 when most of the electrons are localized at the lowest sub-band [15]. As a result, as shown in Eq. 3.2 and Fig. 3.2(b), the E_eff is controllable by V_BS.

3.4 Basic Characteristics of Fabricated SiC MOSFETs

3.4.1 Hall Electron Density

First, the influence of carrier trapping is investigated by Hall effect measurements. Figure 3.3 shows the gate voltage dependences of Hall electron density for lightly-doped (N_A = 3×10^{14} cm^{-3}) SiC MOSFETs annealed in NO and POCl$_3$. In this study, the

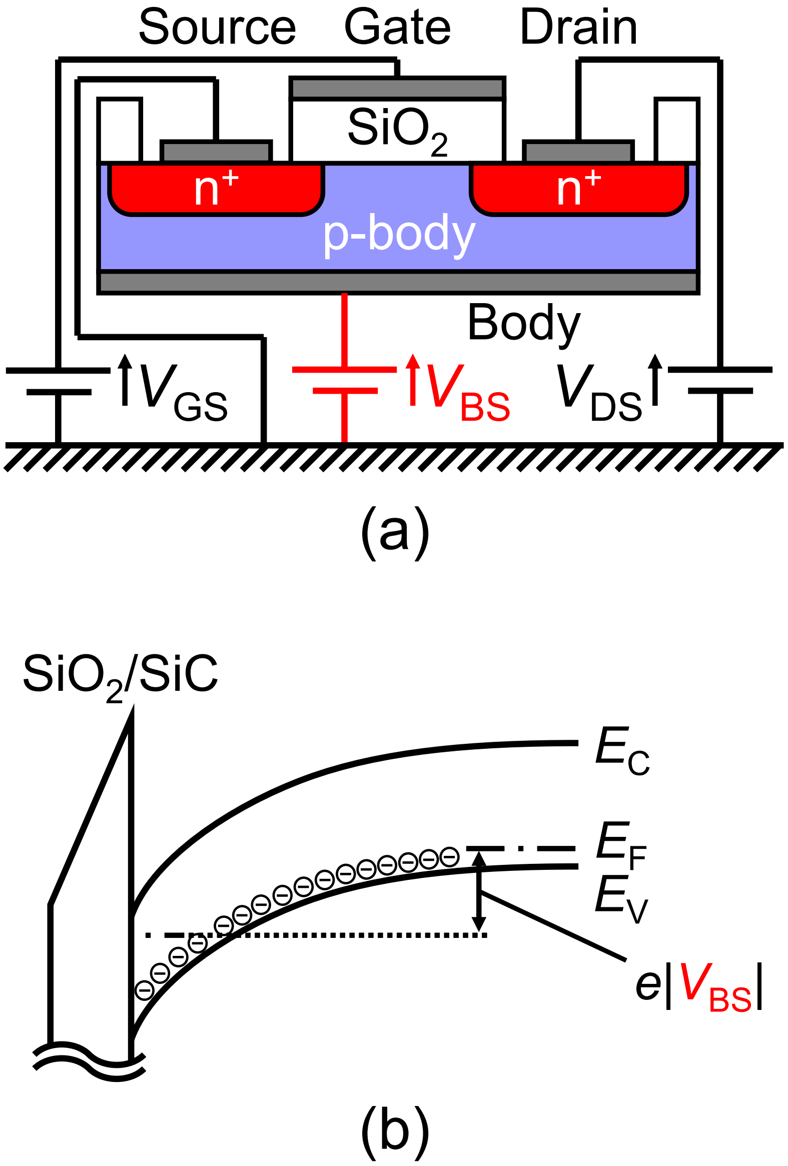

Figure 3.2: (a) Schematic measurement system when a body bias technique is adopted. (b) Schematic band diagram of a SiO_2/SiC interface when a negative body bias is applied.

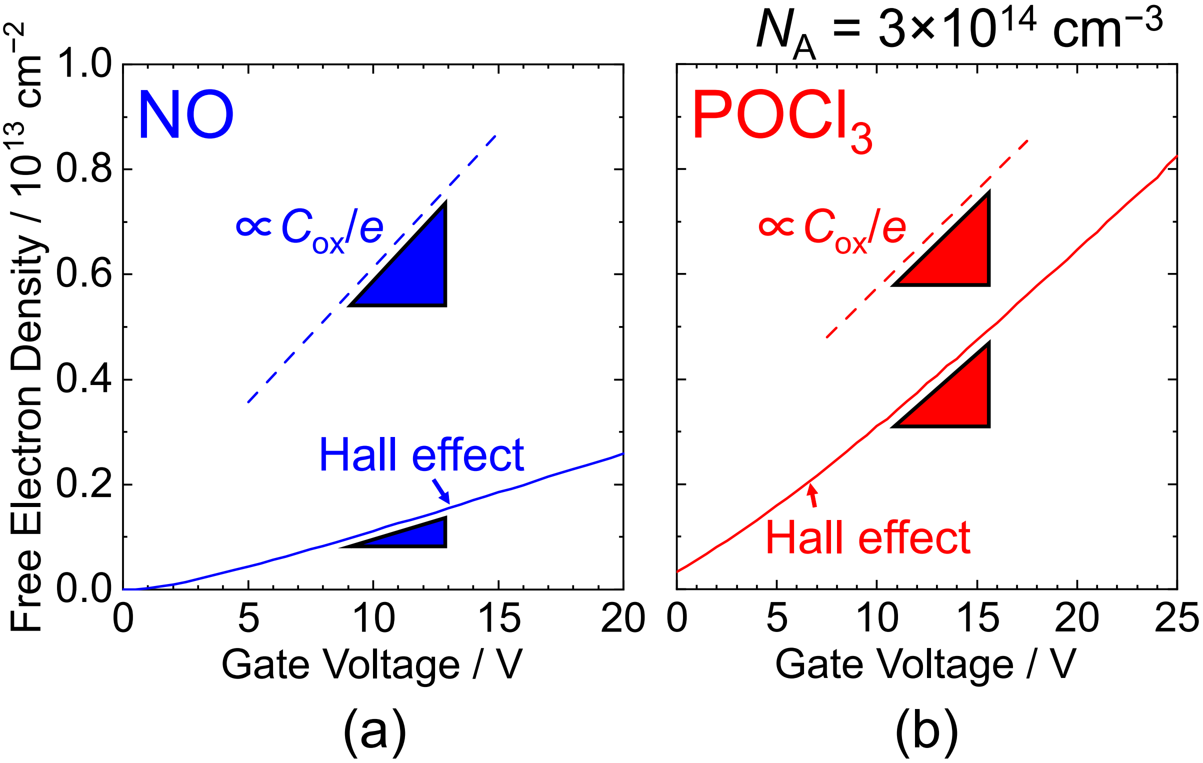

Figure 3.3: Gate voltage dependences of the free electron density for lightly-doped ($N_A = 3 \times 10^{14}$ cm^{-3}) SiC (0001) MOSFETs annealed in (a) NO and (b) POCl$_3$ obtained by Hall effect measurements. The ideal slope of dividing the oxide capacitance by the elementary charge (C_{ox}/e) is also shown.

Hall scattering factor is assumed to be unity; the Hall electron density is equal to n_{free}. In the case of the NO-annealed MOSFETs, the slope of the n_{free}–V_{GS} plot is substantially smaller than the ideal slope of dividing the oxide capacitance by the elementary charge (C_{ox}/e). As shown in Eq. 1.4, the slope of n_{total}–V_{GS} is C_{ox}/e for $V_{\mathrm{GS}} > V_{\mathrm{T}}$. However, in the case of the POCl$_3$-annealed MOSFETs, the slope is nearly identical (~98%) to the ideal one. On the basis of these results, it is assumed that the carrier trapping effect is negligible in POCl$_3$-annealed MOSFETs ($n_{\mathrm{free}} \sim n_{\mathrm{free}} + n_{\mathrm{trap}}$ and $\mu_{\mathrm{free}} \sim \mu_{\mathrm{eff}}$). In the following Sec. 3.4.2 and Sec. 3.4.3, the carrier trapping effect is discussed from the perspective of I_{D}–V_{GS} characteristics.

3.4.2 Field-Effect Mobility

Figure 3.4 shows the gate voltage dependences of field-effect mobility (μ_{FE}) for NO- and POCl$_3$-annealed MOSFETs fabricated on HPSI substrates and various N_{A} of p-body (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}). The field-effect mobilities for the POCl$_3$-annealed MOSFETs are much higher than those for the NO-annealed ones irrespective of the acceptor concentration. In the MOSFETs annealed in NO, the peak value of the field-effect mobility ($\mu_{\mathrm{FE,peak}}$) is approximately 18 cm^2 V^{-1} s^{-1} for heavily-doped ($N_{\mathrm{A}} = 3 \times 10^{17}$ cm^{-3}) MOSFETs. In the case of phosphorus treatment, however, $\mu_{\mathrm{FE,peak}}$ is as high as $\sim$ 66 cm^2 V^{-1} s^{-1} for heavily-doped ($N_{\mathrm{A}} = 3 \times 10^{17}$ cm^{-3}) MOSFETs. In addition, the peak values of μ_{FE} for the POCl$_3$-annealed MOSFETs on a HPSI substrate and on a lightly-doped p-body ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}) are approximately 147 cm^2 V^{-1} s^{-1} and 112 cm^2 V^{-1} s^{-1}, respectively.

The μ_{FE} is given by [5]

$$\mu_{\mathrm{FE}} = \frac{\mathrm{d}I_{\mathrm{D}}}{\mathrm{d}V_{\mathrm{GS}}}\frac{L}{WC_{\mathrm{ox}}V_{\mathrm{DS}}}. \tag{3.3}$$

Note that μ_{FE} has been mainly reported by many institutions because the μ_{eff} in Eq. 1.3 needs the V_{T}, which is arbitrarily determined. The influence of D_{it} can be discussed by μ_{FE} to some extent. However, μ_{FE} is strictly different from μ_{eff} because μ_{FE} can be obtained on the assumption that μ_{eff} does not depend on V_{GS}. Therefore, to discuss the scattering mechanism, μ_{eff} should be evaluated. In Sec. 3.4.4, μ_{eff} is extracted by split C_{GC}–V_{GS} measurements, which can directly quantify the $en_{\mathrm{total}} \simeq C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{T}})$.

3.4.3 Subthreshold Slope

Figure 3.5 shows the subthreshold slopes (SS) of NO- and POCl$_3$-annealed SiC MOSFETs fabricated on HPSI substrates and various N_{A} of p-body (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) as a function of the drain current normalized by channel length and width

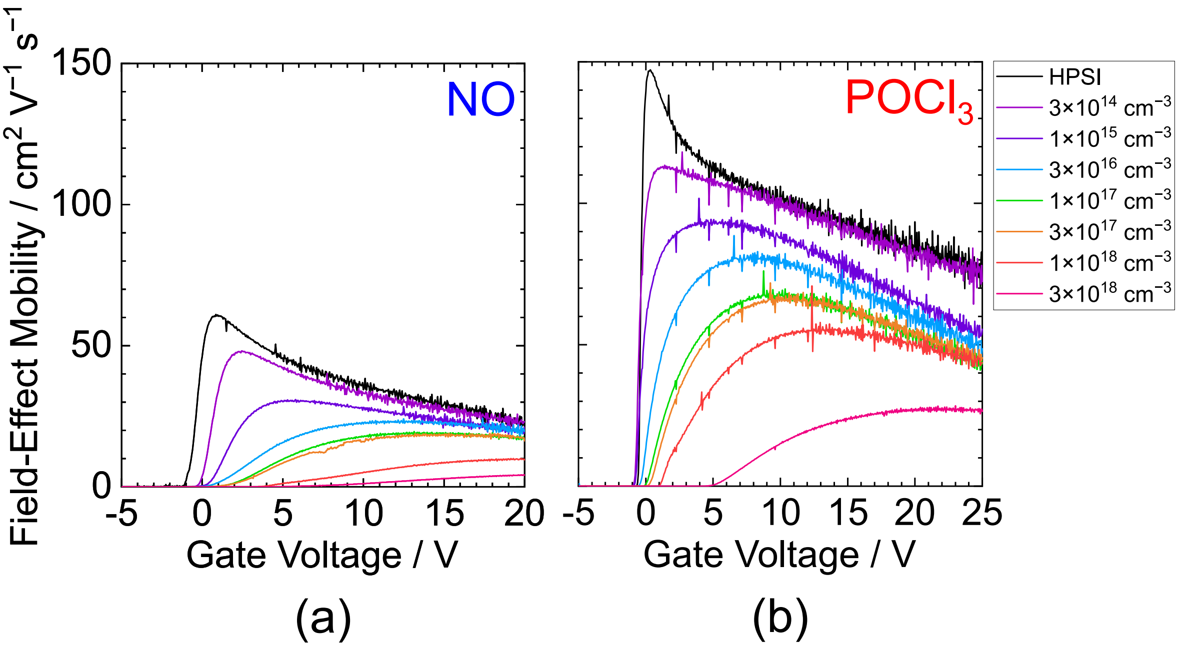

Figure 3.4: Gate voltage dependences of the field-effect mobility for (a) NO- and (b) POCl$_3$-annealed SiC (0001) MOSFETs fabricated on HPSI substrates and various N_{A} of p-body (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}).

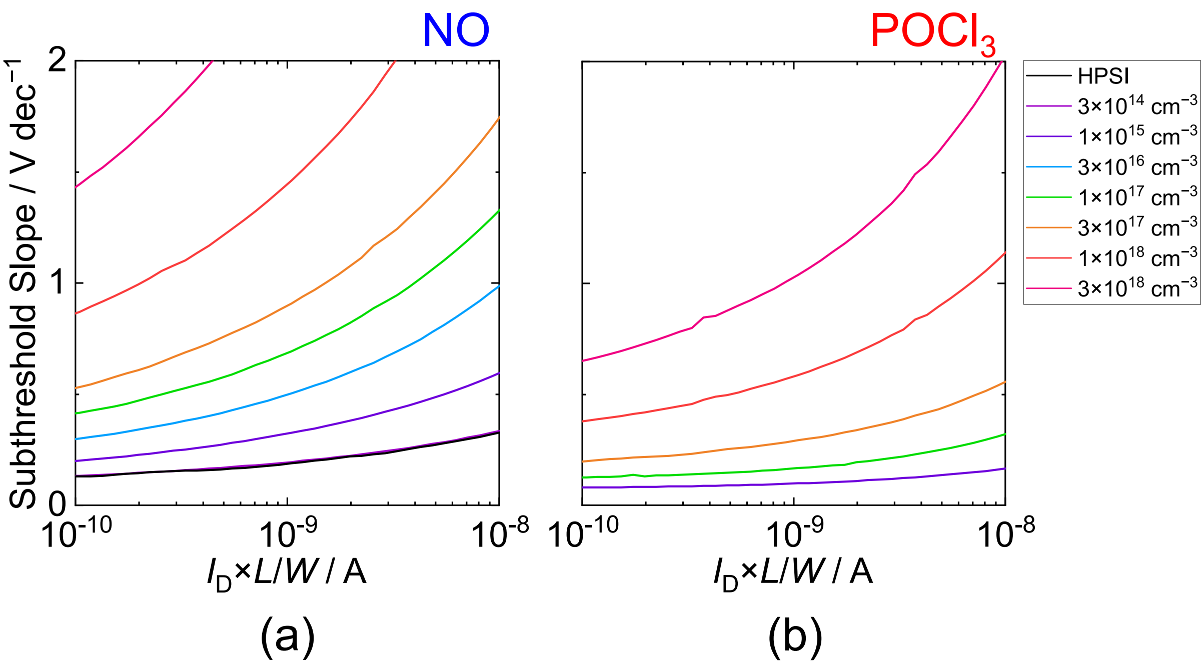

Figure 3.5: Subthreshold slopes of (a) NO- and (b) POCl$_3$-annealed SiC (0001) MOSFETs fabricated on HPSI substrates and various N_{A} of p-body (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) as a function of the drain current normalized by channel length and width ($I_{\mathrm{D}} \times L/W$).

($I_D \times L/W$). The SS is represented by [6]

$$SS = (\ln 10)\left(\frac{k_B T}{e}\right)\left(\frac{C_{ox} + C_{depl} + e^2 D_{it}}{C_{ox}}\right), \tag{3.4}$$

where C_{depl} is the depletion-layer capacitance. Note that μ_{free} strongly depends on N_A; therefore, the surface Fermi level is varied even at a given drain current for different N_A. The SS in Fig. 3.5(a) is much higher than that in Fig. 3.5(b). For example, in the case of the NO-annealed MOSFETs, the SS (at 1×10^{-10} A, $N_A = 3 \times 10^{18}$ cm^{-3}) is 1.4 V dec^{-1}. However, the SS (at 1×10^{-10} A, $N_A = 3 \times 10^{18}$ cm^{-3}) is 0.65 V dec^{-1} in the case of the $POCl_3$-annealed MOSFETs. Thus, the SS value for a $POCl_3$-annealed heavily-doped MOSFET is approximately 2.2 times lower than that of a NO-annealed heavily-doped MOSFET, which is a consequence of the difference in D_{it} resulting from the NO and $POCl_3$ annealing.

3.4.4 Effective Channel Mobility

The μ_{eff} as already shown in Eq. 1.3 is strictly given by [16]

$$\mu_{eff} = \frac{L I_D}{W e n_{total} V_{DS}}. \tag{3.5}$$

Here, n_{total} can be obtained by the following equation [16].

$$n_{total} = \frac{1}{e}\int_{-\infty}^{V_{GS}} C_{GC}\, dV_{GS}. \tag{3.6}$$

The C_{GC} is determined by split C_{GC}–V_{GS} measurements. In this study, a quasi-static C–V measurement system is used.

Figure 3.6 shows the effective channel mobility of $POCl_3$-annealed MOSFETs fabricated on HPSI substrates and various N_A of p-body (3×10^{14} cm^{-3} $\leq N_A \leq 3 \times 10^{18}$ cm^{-3}) as a function of the effective normal filed. In the present study, n_{trap} is assumed to be 0 cm^{-2} on the basis of the results in Fig. 3.3. The N_A is set as 0 cm^{-3} for the HPSI MOSFETs, and η is assumed to be 1/3 [15]. Here, the E_{eff} range extracted for the MOSFET on a HPSI substrate is not affected by the assumed N_A value as far as N_A is lower than 10^{13} cm^{-3}, which is naturally expected for a SiC HPSI substrate.

Next, the author focuses on the reported phonon-limited mobility [4] to discuss the scattering mechanism in SiC MOSFETs. In this study, it is assumed that the phonon-limited mobility is independent of the gate oxide formation process according to its definition. In the previous study [4], the phonon-limited mobility obtained by Hall effect measurements of NO-annealed MOSFETs with extremely low N_A of 3×10^{14} cm^{-3} was found to be given by $\mu/\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1} = 66.5 \times (E_{eff}/\text{MV cm}^{-1})^{-0.39}$ at room temperature. In the present study, however, μ_{eff} of $POCl_3$-annealed MOSFETs on a HPSI substrate is higher than the reported phonon-limited mobility [4]. At $E_{eff} = 0.57$ MV cm^{-1}, the phonon-limited mobility reported

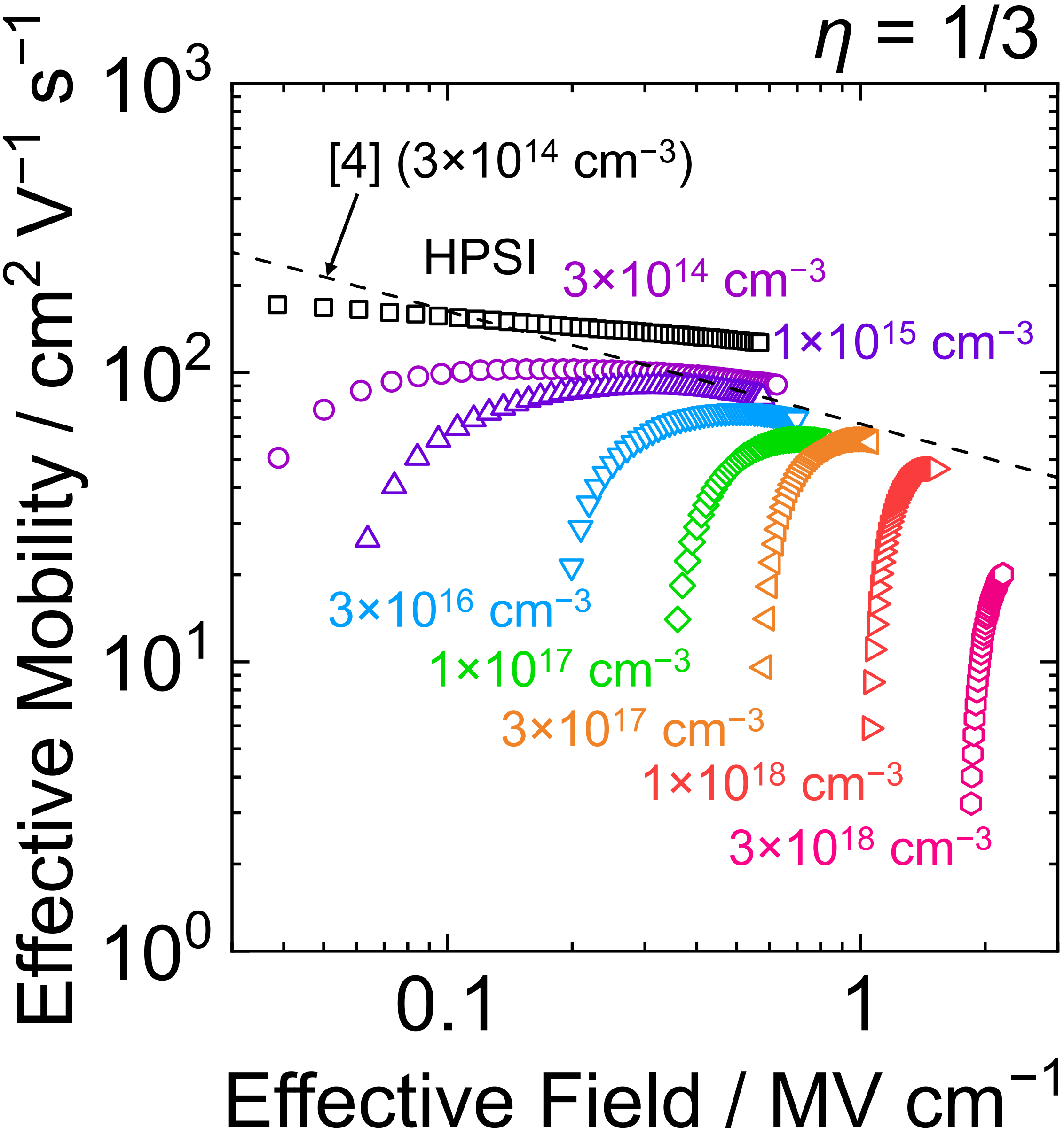

Figure 3.6: Effective normal field (E_{eff}) dependence of effective channel mobility (μ_{eff}) for SiC (0001) MOSFETs subjected to POCl$_3$ annealing. The MOSFETs were fabricated using p-bodies with various dopant concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) and on HPSI substrates. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The black broken line is the phonon-limited mobility line reported in the previous study [4].

in Ref. 4 is 83 cm^2 V^{-1} s^{-1}. On the other hand, μ_{eff} of POCl$_3$-annealed MOSFETs on a HPSI substrate is 126 cm^2 V^{-1} s^{-1}. Thus, μ_{eff} of POCl$_3$-annealed MOSFETs, which should be smaller than μ_{Hall} of the devices, is higher than μ_{Hall} of NO-annealed MOSFETs, which suggests that the true phonon-limited mobility is probably higher compared to the reported one. This result implies that the influence of Coulomb scattering due to the interface charges may remain in NO-annealed MOSFETs.

In addition, in the high-E_{eff} region, μ_{eff} of 46 cm^2 V^{-1} s^{-1} is obtained for the heavily-doped ($N_{\mathrm{A}} = 1 \times 10^{18}$ cm^{-3}) MOSFETs, which is much higher than the reported Hall mobility of < 20 cm^2 V^{-1} s^{-1} for heavily-doped ($N_{\mathrm{A}} = 4 \times 10^{17}$ cm^{-3}) MOSFETs annealed in NO. In general, free electrons are localized very close to the SiC/SiO$_2$ interface in the high-E_{eff} region. Thus, this mobility enhancement can be interpreted by the lower density of trapped electrons.

To extensively discuss the μ_{eff} in the high-E_{eff} region, I_{D}–V_{GS} with applying negative body bias is needed. In the following section, the μ_{eff} in the high-E_{eff} region is focused.

3.5 Characteristics of Fabricated SiC MOSFETs with Applying Negative Body Bias

In previous reports on SiC MOS-Hall effect measurements, the Hall mobility of NO-annealed MOSFETs is substantially degraded under a high E_{eff} [3, 4]. This phenomenon cannot be interpreted simply on the basis of Coulomb scattering from acceptors in a p-type body [10, 17]. Furthermore, the influence of scattering by trapped electrons is inevitable [8] since numerous trapped electrons remain even after NO annealing. Therefore, Coulomb scattering due to the trapped electrons and surface-roughness scattering, which are dominant in the high-E_{eff} region, are indistinguishable. According to Ref. 4, surface roughness scattering was reported not dominantly to affect the Hall mobility of NO-annealed (0001) MOSFETs even in the high-E_{eff} region. Note that the Hall mobility in Ref. 4 was measured in the relatively low E_{eff} range (< 1.0 MV cm^{-1}), and Coulomb scattering due to the trapped electrons is possibly dominant (the maximum trapped electron density: $\sim 5.7 \times 10^{12}$ cm^{-2} [1]). According to Ref. 11, it is suggested that the Hall mobility of NO-annealed ($0\bar{3}3\bar{8}$) MOSFETs is limited by strong surface roughness scattering. The n_{trap} of MOSFETs on ($0\bar{3}3\bar{8}$) (the maximum trapped electron density: $\sim 1.5 \times 10^{12}$ cm^{-2} [18]) is much lower than that of MOSFETs on (0001). However, the measured data was in the relatively low E_{eff} range (< 1.5 MV cm^{-1}). As a result, the Hall mobility was proportional to $E_{\mathrm{eff}}^{-1.7}$ (in theory, E_{eff}^{-2}). Thus, surface roughness scattering in the high-E_{eff} region (1.0 MV cm^{-1} $< E_{\mathrm{eff}} <$ 2.0 MV cm^{-1}) should be more extensively investigated. In the present study, a negative body bias (0 V $\geq V_{\mathrm{BS}} \geq -40$ V) is applied to control E_{eff} for a given N_{A} by using MOSFETs on (0001) with a D_{it} as low as that on ($0\bar{3}3\bar{8}$).

Figure 3.7 shows the atomic force microscope (AFM) images (2×2 μm^2 scan), and

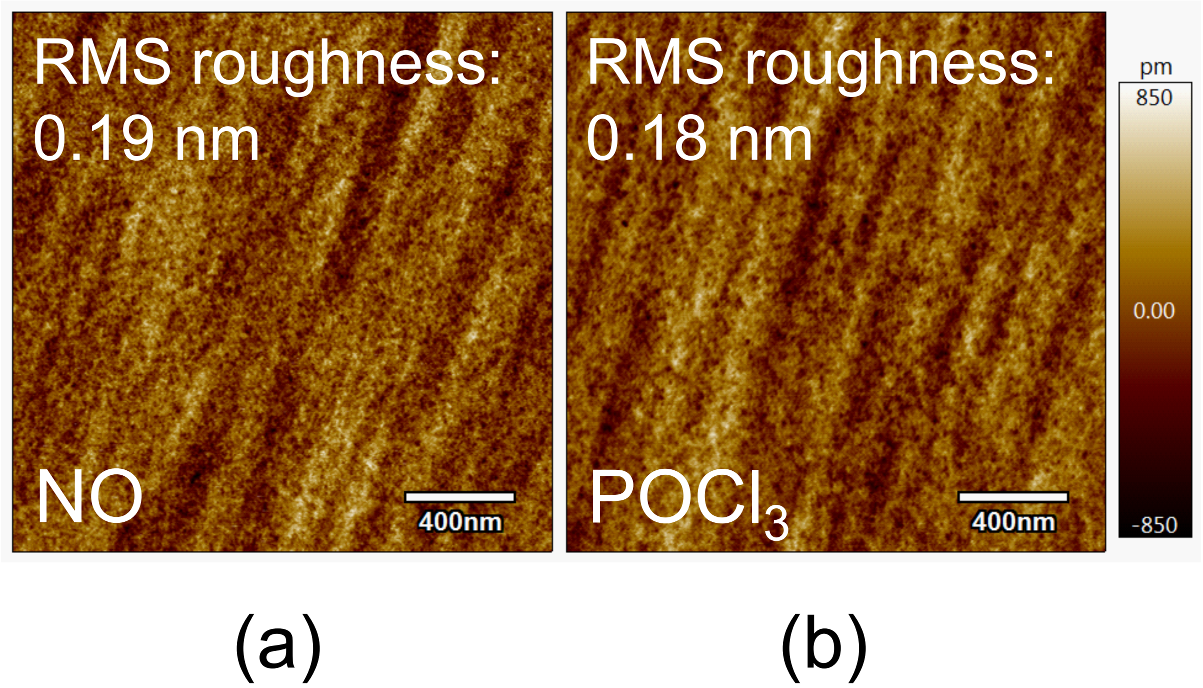

Figure 3.7: Atomic force microscope (AFM) images ($2 \times 2\ \mu\text{m}^2$ scan), and the root mean square (RMS) roughness of SiC (0001) substrates after removing the gate oxides annealed in (a) NO and (b) POCl$_3$ by dilute hydrofluoric acid.

the root mean square (RMS) roughness of SiC substrates after removing the gate oxides annealed in NO and $POCl_3$ by dilute hydrofluoric acid. In Fig. 3.7, the RMS roughness is 0.19 nm and 0.18 nm for NO- and $POCl_3$-annealed SiC substrates, respectively. This result implies that the influence of surface roughness scattering can be regarded as almost the same.

Next, Fig. 3.8 shows the typical I_D–V_{GS} characteristics, the gate voltage dependence of electron density obtained by split C_{GC}–V_{GS} measurements, and the gate voltage dependence of effective channel mobility. When a negative body bias is applied, the threshold voltage shifts toward the positive direction.

Figure 3.9 shows the effective normal field dependences of the effective channel mobility for lightly- ($N_A = 3 \times 10^{14}$ cm^{-3}) and heavily-doped ($N_A = 3 \times 10^{17}$ cm^{-3}) MOSFETs after $POCl_3$ annealing. The body bias is applied in the range from 0 V to -40 V. The μ_{eff} for lightly-doped MOSFETs is high, approximately 103 cm^2 V^{-1} s^{-1} in the case of $V_{BS} =$ 0 V. When a negative body bias is applied, E_{eff} increases, and μ_{eff} decreases irrespective of N_A for the MOSFETs. The decrease in μ_{eff} is especially sharp for the heavily-doped MOSFETs ($N_A = 3 \times 10^{17}$ cm^{-3}). For example, μ_{eff} decreases from 58 cm^2 V^{-1} s^{-1} ($E_{eff} =$ 1.0 MV cm^{-1}) to 8.5 cm^2 V^{-1} s^{-1} ($E_{eff} =$ 2.3 MV cm^{-1}) for heavily-doped ($N_A = 3 \times 10^{17}$ cm^{-3}) MOSFETs with increasing V_{BS} to -40 V. In addition, when a gate voltage increases, μ_{eff} increases sharply for each p-body doping.

3.6 Discussion

In this section, μ_{eff} in the high-E_{eff} region is discussed in detail. To compare to the previous results of μ_{Hall} for NO-annealed MOSFETs [10], μ_{eff} as a function of the average distance of electrons from the MOS interface (z_{avg}) is considered. Figure 3.10 shows the effective channel mobility as a function of z_{avg} at n_{total} of 1.5×10^{12} cm^{-2}. The reported μ_{Hall} of NO-annealed MOSFETs at n_{free} of 1.5×10^{12} cm^{-2} [10] is also shown by a dashed line. Here, how to calculate z_{avg} is described in Appendix A. In Fig. 3.10, μ_{eff} sharply decreases as z_{avg} decreases (especially, $z_{avg} < 2.0$ nm), irrespective of the acceptor concentration of the p-type body. Therefore, this mobility degradation in the high-E_{eff} region may not be caused by Coulomb scattering from ionized acceptors. This speculation is consistent with the study in Chapter 2 that the carrier trapping effect does not depend on N_A by comparing D_{it} of MOSFETs with various p-body doping concentrations because the acceptors do not dominantly limit μ_{eff}. Compared to the z_{avg} dependence of μ_{Hall} for NO-annealed MOSFETs, the behavior of mobility degradation in the high-E_{eff} region ($z_{avg} < 2.0$ nm corresponding to $E_{eff} > 0.5$ MV cm^{-1}) is very close. In addition, it is revealed that μ_{eff} of $POCl_3$-annealed MOSFETs strongly decreases in the very high-E_{eff} region ($z_{avg} < 1.6$ nm corresponding to $E_{eff} > 1.0$ MV cm^{-1}). The sharp mobility drop is observed in the range $z_{avg} < 2.0$ nm.

The RMS roughness of SiC substrates after chemical mechanical polishing is 0.037 nm

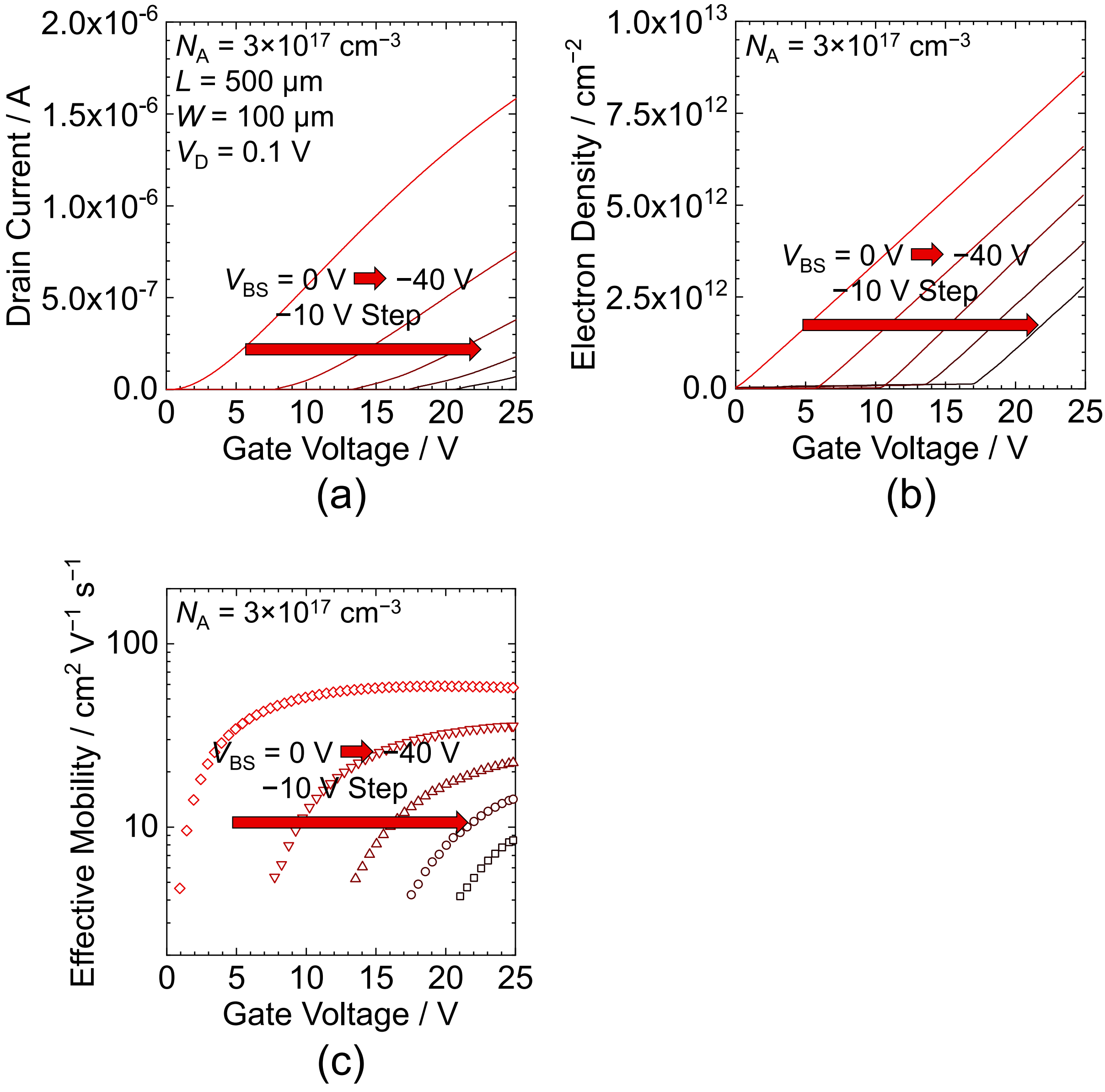

Figure 3.8: Typical (a) drain current, (b) electron density, and (c) effective channel mobility as a function of the gate voltage for POCl$_3$-annealed SiC (0001) MOSFETs when the negative body bias is applied in the range from 0 V to −40 V. In the calculation of the electron density, the gate-channel capacitance is obtained by quasi-static capacitance–voltage measurements.

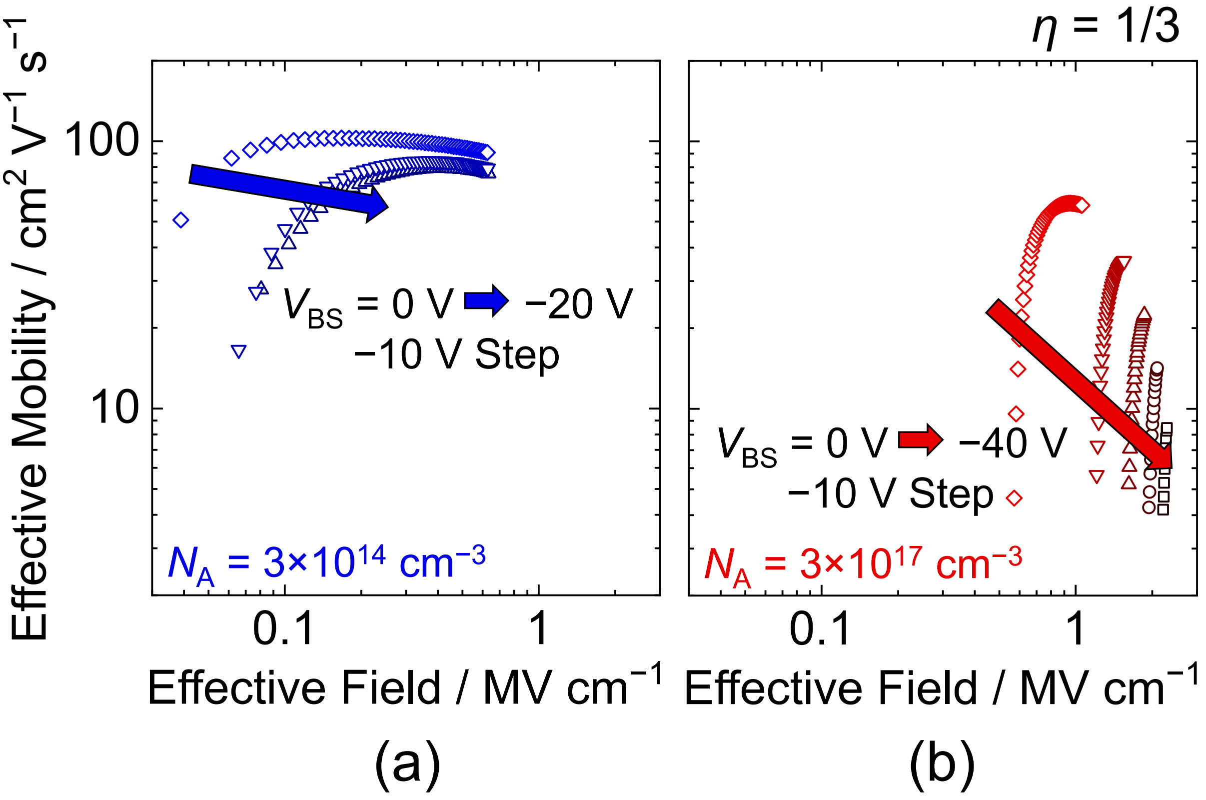

Figure 3.9: Effective normal field (E_{eff}) dependences of the effective channel mobility (μ_{eff}) for POCl$_3$-annealed (a) lightly- ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}) and (b) heavily-doped ($N_{\mathrm{A}} = 3 \times 10^{17}$ cm^{-3}) SiC (0001) MOSFETs when the body bias is applied in the ranges from 0 V to -20 V and from 0 V to -40 V, respectively. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}.

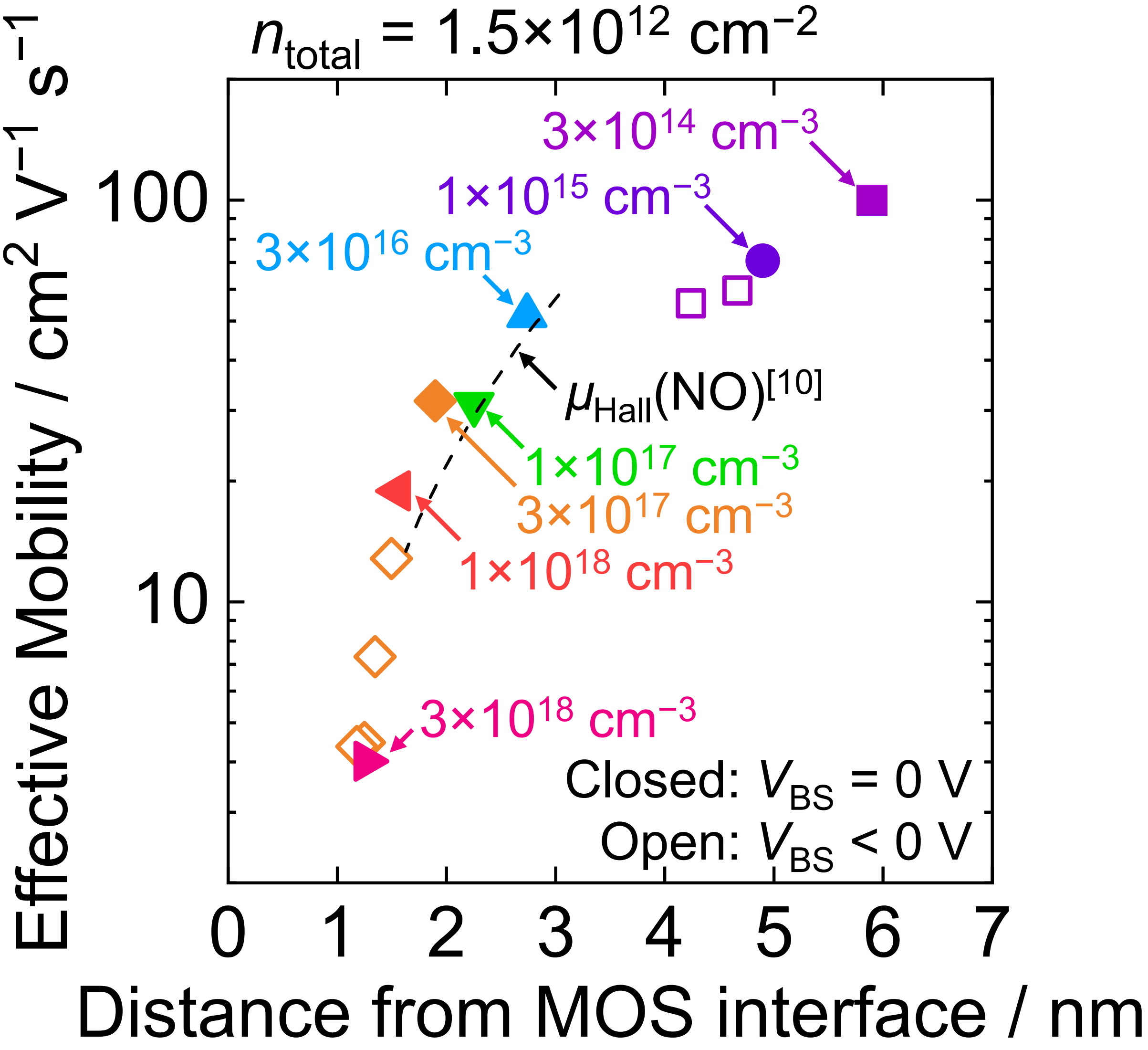

Figure 3.10: Effective channel mobility as a function of the average distance of electrons from the MOS interface for POCl$_3$-annealed SiC (0001) MOSFETs when the total electron density (n_{total}) is 1.5×10^{12} cm^{-2} with and without applying negative body bias (V_{BS}). The data for various p-body doping concentrations are shown in the figure. The closed symbols and open symbols represent the data of $V_{BS} = 0$ V and $V_{BS} < 0$ V, respectively. The reported Hall mobility of MOSFETs annealed in NO [10] is also shown.

(20×20 μm^2 scan) [19]. After epitaxial growth or high-temperature annealing, however, the RMS roughness increases to a few nanometers. In particular, SiC (0001) substrates originally have an off-angle of several degrees to ensure polytype replication [20]. For this reason, the (0001) substrates have a high density of steps. On the other hand, the above phenomena are not observed in the case of Si/SiO$_2$ interfaces. Therefore, the height of surface roughness (Δ_{sr}) at SiC/SiO$_2$ interfaces is possibly higher than that at Si/SiO$_2$ interfaces. As a result, the surface roughness-limited mobility (μ_{sr}) of SiC MOSFETs substantially decreases because the μ_{sr} is proportional to $\Delta_{\mathrm{sr}}^{-2}$ [15].

The sharp decrease in μ_{eff} in $z_{\mathrm{avg}} < 2.0$ nm is observed even if D_{it} is reduced by POCl$_3$ annealing, which is unusual because it is not caused in Si MOSFETs. One of the possible origins of the abnormal mobility drop is the strong surface roughness scattering at the SiC/SiO$_2$ interfaces, as already mentioned above. A power function of E_{eff} for the obtained μ_{eff} is considered to discuss the surface roughness scattering. Figure 3.11 shows the μ_{eff} as a function of E_{eff} ($E_{\mathrm{eff}} > 1.0$ MV cm^{-1}) for several n_{total} of 1.0×10^{12}–3.0×10^{12} cm^{-2}. In Fig. 3.11(b), μ_{eff} follows a slope of -2.3–-2.2 regardless of n_{total}. However, the slope for the lowest n_{total} condition ($n_{\mathrm{total}} = 1.0 \times 10^{12}$ cm^{-2}) is -1.8, which may be influenced by another scattering such as Coulomb scattering due to acceptors, fixed charges, and trapped electrons. In addition, the data of the lowest n_{total} condition is at most at E_{eff} of 1.6 MV cm^{-1}. Thus, the obtained result is consistent with the previous report [11]. These strong E_{eff} dependences are attributable to lower D_{it} and higher E_{eff} compared to the previous studies [4, 11]. According to the previous study on Si MOSFETs, μ_{eff} is proportional to E_{eff}^{-2} in the range $E_{\mathrm{eff}} > 0.5$ MV cm^{-1} at 77 K, and this is ascribed to surface roughness scattering [14]. In general, the surface roughness scattering rate is known to be proportional to E_{eff}^{2} [21], and thus the surface roughness-limited mobility should be proportional to E_{eff}^{-2}. Note that an experimentally obtained absolute value of μ_{eff}–E_{eff} slope is sometimes larger than 2 (maximum: 2.8) according to the previous studies [9, 15]. In addition, the increase in μ_{eff} by increasing n_{total}, which is not observed in conventional Si MOSFETs, can be explained by screening μ_{sr} by surface carriers [8, 22]. Based on the obtained results, the substantial decrease in mobility of MOSFETs with low D_{it} in the very high-E_{eff} region (1.0 MV cm^{-1} $< E_{\mathrm{eff}} <$ 2.0 MV cm^{-1}) obtained in this study may be mainly caused by surface roughness scattering.

3.7 Summary

In summary, the μ_{eff} of POCl$_3$-annealed 4H-SiC (0001) MOSFETs with various dopant concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) in the p-type body is investigated in detail. The μ_{eff} of POCl$_3$-annealed MOSFETs on HPSI substrates is higher than the phonon-limited mobility reported in the previous study on μ_{Hall} for NO-annealed MOSFETs, which have a high density of trapped electrons. Thus, the reported phonon-limited mobility

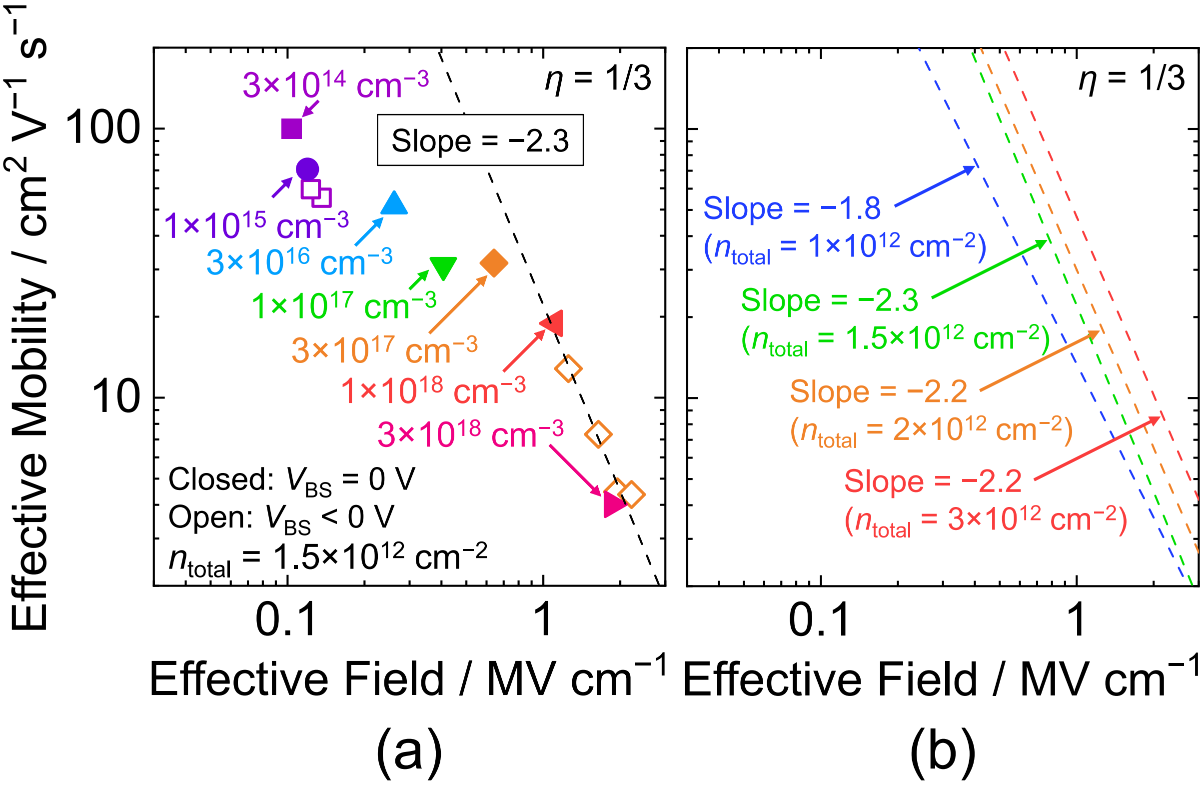

Figure 3.11: (a) Effective normal field (E_{eff}) dependence of the effective channel mobility (μ_{eff}) when the total electron density (n_{total}) is 1.5×10^{12} cm^{-2} for POCl$_3$-annealed SiC (0001) MOSFETs with and without applying negative body bias (V_{BS}). Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}. The slope of −2.3 is indicated by a dashed line. The data for various p-body doping concentrations are shown in the figure. The closed symbols and open symbols represent the data of $V_{\mathrm{BS}} = 0$ V and $V_{\mathrm{BS}} < 0$ V, respectively. (b) The μ_{eff} as a function of E_{eff} in the high E_{eff}-region ($E_{\mathrm{eff}} > 1.0$ MV cm^{-1}) of MOSFETs at $n_{\mathrm{total}} = 1.0 \times 10^{12}$, 1.5×10^{12}, 2.0×10^{12}, and 3.0×10^{12} cm^{-2}.

is probably affected by the influence of trapped electrons. Next, a negative body bias technique is used to investigate μ_{eff} of POCl$_3$-annealed MOSFETs in the high-E_{eff} region. As a result, the considerable mobility degradation in the high-E_{eff} region (1.2 nm $< z_{\mathrm{avg}} <$ 1.5 nm corresponding to 1.2 MV cm^{-1} $< E_{\mathrm{eff}} <$ 2MV cm^{-1}) is observed in the range 1.5×10^{12} cm^{-2} $< n_{\mathrm{total}} <$ 3.0×10^{12} cm^{-2} even though MOSFETs with low D_{it} are used. It may be caused by surface roughness scattering because the μ_{eff} follows a $E_{\mathrm{eff}}^{-2.3--2.2}$ dependence in the range 1.0 MV cm^{-1} $< E_{\mathrm{eff}} <$ 2.0 MV cm^{-1}.

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Chapter 4

Electron Scattering Mechanism in SiC (0001) MOSFETs

4.1 Introduction

In Chapter 3, the μ_{eff} of $\mathrm{POCl_3}$-annealed MOSFETs was compared to the μ_{Hall} of NO-annealed MOSFETs reported in the previous study [1]. To accurately discuss the Coulomb scattering by trapped electrons, however, the comparison of μ_{Hall} for between NO- and $\mathrm{POCl_3}$-annealed MOSFETs fabricated on the same substrates is needed. In this chapter, Hall effect measurements for SiC (0001) MOSFETs are performed, and the electron scattering mechanism is discussed with numerical calculations.

In the present study, the author focuses on the N_{A} of p-body dependence of μ_{Hall}. Although some previous studies reported the N_{A} dependence of μ_{Hall} [1–4], the electron scattering mechanism itself is not clarified. The μ_{Hall} of SiC MOSFETs especially in the high-E_{eff} region is approximately ten times lower than that of Si MOSFETs. Due to this, separation of the scattering processes is very difficult at the present stage.

To address this problem, the author also focuses on the interface treatment and temperature dependences of μ_{Hall}. The μ_{Hall} of as-oxidized and NO-annealed MOSFETs has been discussed in the previous studies [4–8]. However, NO-annealed MOSFETs are probably influenced by a high density of trapped electrons as already explained in Chapter 3. Therefore, μ_{Hall} of $\mathrm{POCl_3}$-annealed MOSFETs is obtained in this study. In addition, only a few studies on the temperature dependence of μ_{Hall} were reported [1, 4, 8–10]. Temperature is one of the most important parameters for understanding and formulating the scattering mechanism. In particular, phonon scattering is suppressed at low temperatures, and Coulomb scattering is dominant. Thus, the impact of Coulomb scattering due to trapped electrons on μ_{free} can be discussed at low temperatures.

To begin with, the n_{trap} of MOSFETs without POA, annealed in NO, or annealed in $\mathrm{POCl_3}$ is quantified by combining MOS-Hall effect and split C_{GC}–V_{GS} measurements. In the analyses, the energy distribution of D_{it} plotted with respect to E_{C}(2D-DOS) is also extracted considering inversion layer quantization. Next, the author compares the measured μ_{Hall} of $\mathrm{POCl_3}$-annealed MOSFETs to that of NO-annealed ones at room and low temperatures. After that, the dominant scattering processes for electrons in the SiC (0001)/$\mathrm{SiO_2}$ inversion layers are explained using computed μ_{free}.

4.2 Experimental Details

Figure 4.1(a) shows the process flow of the fabricated MOSFETs in this chapter. In this study, p-type 4H-SiC (0001) body layers (3×10^{14} $\mathrm{cm^{-3}} \leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ $\mathrm{cm^{-3}}$) were prepared. The p-body doping concentration was varied by $\mathrm{Al^+}$ ion implantation. The source/drain regions ($N_{\mathrm{D}} = 1.0 \times 10^{20}$ $\mathrm{cm^{-3}}$) and body regions ($N_{\mathrm{A}} = 1.6 \times 10^{20}$ $\mathrm{cm^{-3}}$) were formed by $\mathrm{P^+}$ and $\mathrm{Al^+}$ ion implantation, respectively. After that, Ar annealing was carried out at 1750°C for 20 min to activate implanted ions. The gate oxides were formed by three different conditions: (1) dry oxidation at 1300°C for 30 min without POA (As-Ox.), (2) dry oxidation with subsequent annealing in NO (10% diluted in $\mathrm{N_2}$) at 1250°C for 70 min (NO), (3) dry oxidation with subsequent annealing in $\mathrm{POCl_3}$ (a gas mixture of $\mathrm{POCl_3}$, $\mathrm{O_2}$, and $\mathrm{N_2}$) at 1000°C for 10 min ($\mathrm{POCl_3}$). Regarding $\mathrm{POCl_3}$ annealing, $\mathrm{N_2}$ annealing at 1000°C for 30 min was also performed after the gate oxide formation. The resultant oxide thicknesses were 42 nm for as-oxidized and NO-annealed MOSFETs and 58 nm for $\mathrm{POCl_3}$-annealed MOSFETs. The channel length and width of the eight-terminal MOS-Hall bar devices were 500 μm and 100 μm, respectively. The schematic device structures are described in Fig. 4.1(b). The measurements were conducted at RT (296 K) and 77 K.

Figure 4.2(a) shows the schematic device structure and circuit of split C_{GC}–V_{GS} measurements from the cross-sectional view. The measurement was performed using the quasi-static C–V measurement system. The n_{total} was quantified by Eq. 3.6. Moreover, Fig. 4.2(b) shows the schematic illustration of a MOS-Hall bar from the top view. In this study, the Hall scattering factor is assumed to be unity. Therefore, the measured Hall electron density and μ_{Hall} are assumed to be the n_{free} and μ_{free}. MOS-Hall effect measurements were conducted under an AC (100 Hz) magnetic field (0.219–0.376 T). To extract the μ_{Hall} accurately, the resistivity and the Hall voltage of the inversion channel were measured continuously when the same V_{GS} was applied.

4.3 Energy Distribution of Interface State Density Extracted from MOS-Hall Effect Measurements

4.3.1 Densities of Free and Trapped Electrons

Figure 4.3 shows the gate voltage dependences of the n_{free}, n_{trap}, and n_{total} for as-oxidized, NO-annealed, and $\mathrm{POCl_3}$-annealed lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{14}$ $\mathrm{cm^{-3}}$) and heavily-doped

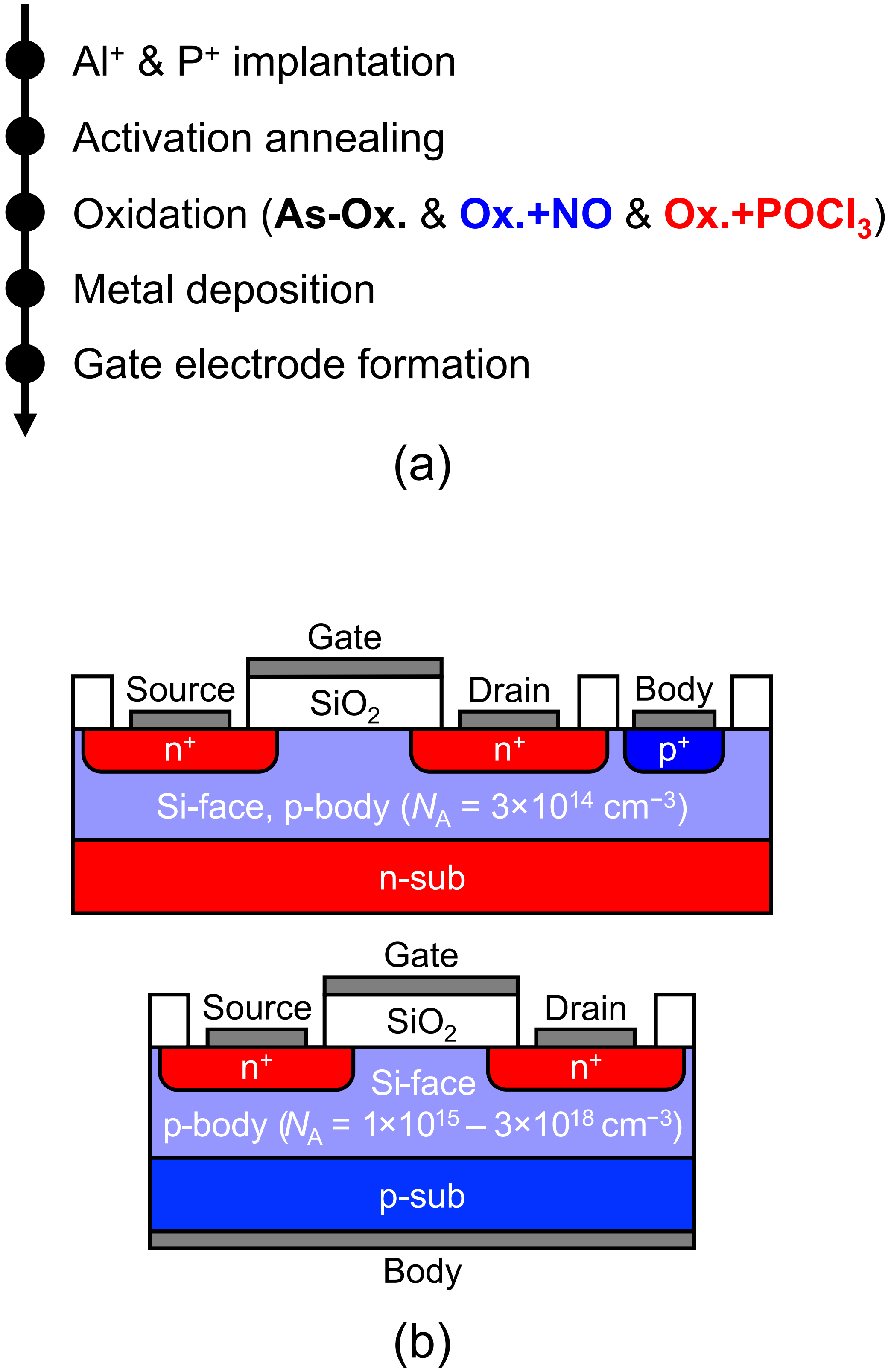
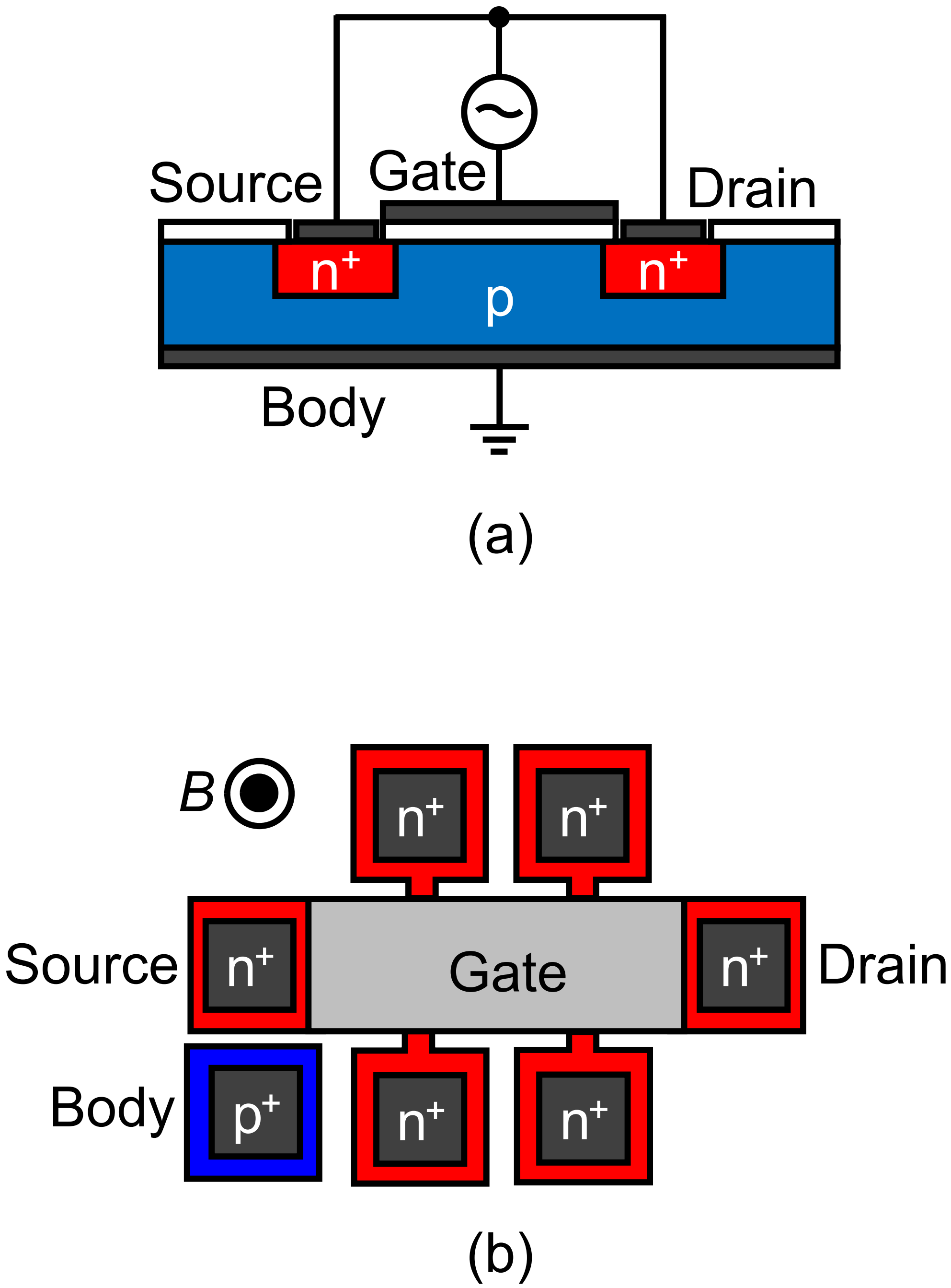


Figure 4.1: (a) Process flow of the fabricated SiC (0001) MOSFETs for MOS-Hall effect measurements. (b) Schematic device structures of the fabricated MOSFETs from the cross-sectional view.



(a)

(b)

Figure 4.2: (a) Schematic device structure and circuit of split gate-channel (C_{GC})–gate-source voltage (V_{GS}) measurements from the cross-sectional view and (b) schematic illustration of a MOS-Hall bar from the top view. For this structure, the resistivity and the Hall voltage of the inversion channel can be measured continuously when the same V_{GS} is applied.

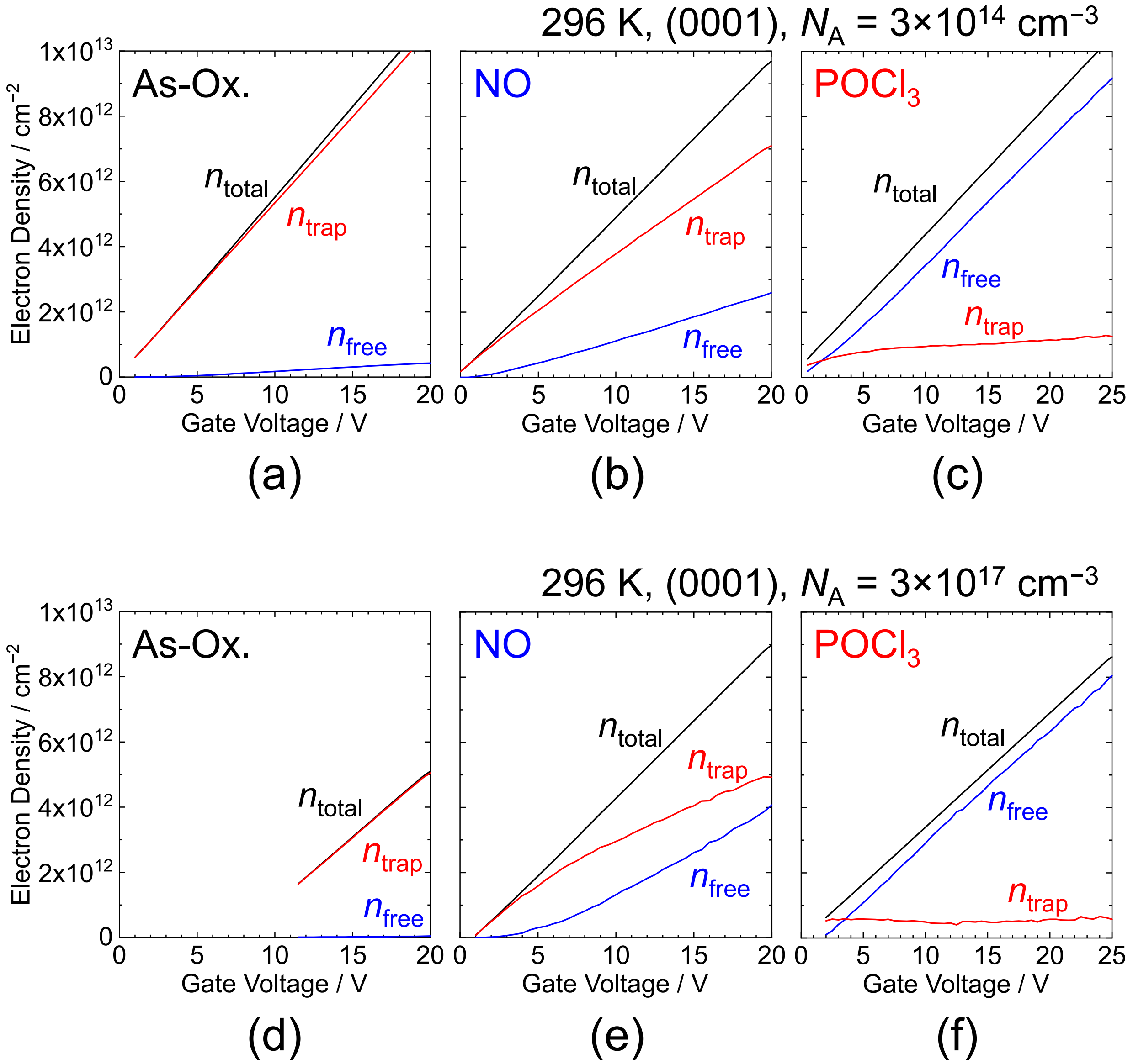


Figure 4.3: Gate voltage dependences of the densities of free electrons (n_{free}), trapped electrons (n_{trap}), and total electrons (n_{total}) for (a) as-oxidized, (b) NO-annealed, and (c) POCl$_3$-annealed lightly-doped ($N_A = 3 \times 10^{14}$ cm^{-3}) SiC (0001) MOSFETs and for (d) as-oxidized, (e) NO-annealed, and (f) POCl$_3$-annealed heavily-doped ($N_A = 3 \times 10^{17}$ cm^{-3}) ones at 296 K.

($N_\mathrm{A} = 3 \times 10^{17}$ cm^{-3}) (0001) MOSFETs at 296 K. In as-oxidized and NO-annealed lightly-doped MOSFETs, n_trap is higher than n_free even at high V_GS, which is consistent with previous results [5]. In the case of POCl$_3$-annealed MOSFETs, the n_free is close to the n_total. For example, $n_\mathrm{free} = 9.2 \times 10^{12}$ cm^{-2} and $n_\mathrm{total} = 1.0 \times 10^{13}$ cm^{-2} at $V_\mathrm{GS} = 25$ V for lightly-doped MOSFETs. Similarly, $n_\mathrm{free} = 8.1 \times 10^{12}$cm^{-2} and $n_\mathrm{total} = 8.6 \times 10^{12}$ cm^{-2} at $V_\mathrm{GS} = 25$ V for heavily-doped MOSFETs. From the perspective of $n_\mathrm{free}/n_\mathrm{total}$, the $n_\mathrm{free}/n_\mathrm{total}$ at n_total of 5×10^{12} cm^{-2} is about 3% and 23% for as-oxidized and NO-annealed lightly-doped MOSFETs, respectively. In contrast, the ratio is about 80% for POCl$_3$-annealed ones. As for the heavily-doped MOSFETs, the $n_\mathrm{free}/n_\mathrm{total}$ at n_total of 5×10^{12} cm^{-2} is 1%, 31%, and 91% for as-oxidized, NO-annealed, and POCl$_3$-annealed MOSFETs, respectively. Thus, the n_trap is considerably smaller compared to the other MOSFETs, especially at high V_GS for both lightly- and heavily-doped MOSFETs. Note that the influence of the Hall scattering factor is neglected in the above discussion.

4.3.2 Energy Distribution of Interface State Density

In this chapter, the energy distribution of D_it was extracted by [5]

$$D_\mathrm{it} \approx \frac{\mathrm{d}n_\mathrm{trap}}{\mathrm{d}E_\mathrm{F}(n_\mathrm{free})}. \tag{4.1}$$

Here, the E_F was calculated by self-consistently solving the Schrödinger and Poisson's equations [11–13].

Figure 4.4 shows the energy distributions of D_it plotted with respect to E_C(2D-DOS) for as-oxidized, NO-annealed, and POCl$_3$-annealed (0001) MOSFETs with various N_A of p-body. In the case of as-oxidized and NO-annealed MOSFETs, the D_it increases exponentially toward E_C(2D-DOS). For example, $D_\mathrm{it} > 10^{14}$ cm^{-2} eV^{-1} for as-oxidized MOSFETs and $D_\mathrm{it} > 10^{13}$ cm^{-2} eV^{-1} for NO-annealed MOSFETs when E_T is higher than E_C(2D-DOS) $-$ 0.1 eV. In contrast, the D_it obtained from POCl$_3$-annealed MOSFETs in Fig. 4.4(c) does not increase exponentially toward E_C(2D-DOS). Furthermore, D_it of POCl$_3$-annealed MOSFETs is much lower compared to the other MOSFETs (As-Ox. and NO) and close to the detection limit because the n_trap does not strongly depend on V_GS, and thus E_F. In Chapter 2, the D_it was obtained by assuming that the μ_Hall is constant. On the other hand, in this chapter, D_it distributions in Fig. 4.4 are extracted taking account of the gate voltage dependence of Hall mobility. Thus, the results in Fig. 4.4 are more accurate than those in Chapter 2. In this study, D_it very near E_C(2D-DOS) can be extracted especially for POCl$_3$-annealed MOSFETs because the n_free and n_trap in the wide energy range can be obtained.

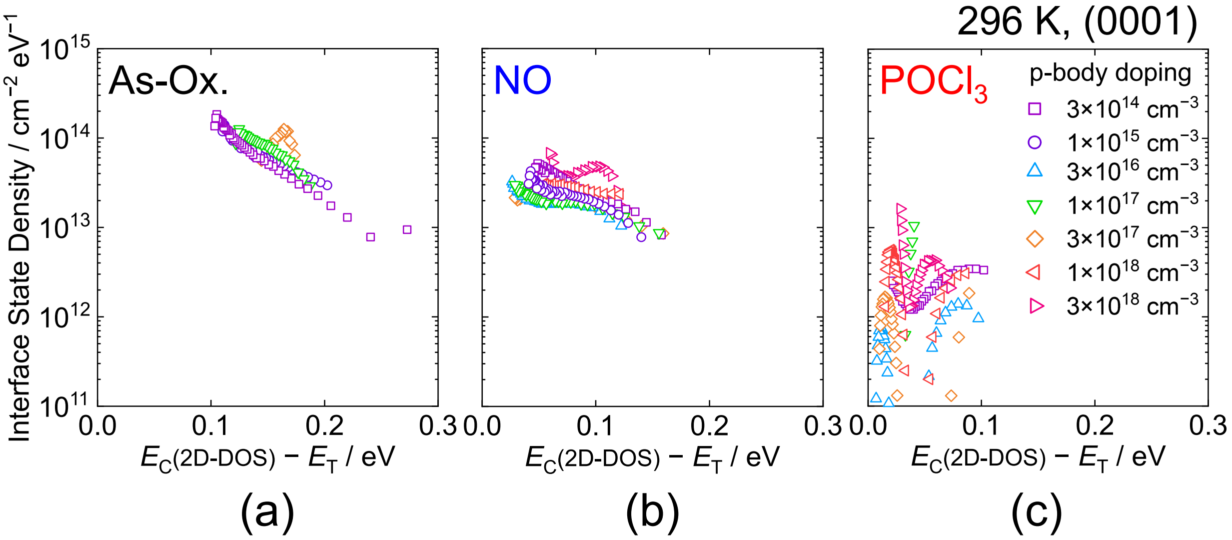


Figure 4.4: Energy distributions of interface state density plotted with respect to the bottom edge of the two-dimensional density of states [E_C(2D-DOS)] for (a) as-oxidized, (b) NO-annealed, and (c) POCl$_3$-annealed (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_A \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K.

4.4 Hall Mobility

4.4.1 Experimental Results

Figure 4.5 shows the effective normal field dependences of μ_{Hall} for as-oxidized, NO-annealed, and $\mathrm{POCl_3}$-annealed (0001) MOSFETs with various N_{A} of p-body at 296 K. In this study, the η is set as 1/3 [1, 14]. Here, the phonon-limited mobility (μ_{ph}) reported in the previous study on μ_{Hall} for NO-annealed MOSFETs [1] is also shown. The μ_{Hall} of as-oxidized MOSFETs is similar to that of NO-annealed ones, being consistent with the results of previous reports [5, 6]. In contrast, the μ_{Hall} of $\mathrm{POCl_3}$-annealed MOSFETs is higher than that of NO-annealed ones in the wide E_{eff} range. Moreover, the μ_{Hall} degradation in the high-E_{eff} region, which is observed in NO-annealed MOSFETs [1, 3], is suppressed in the case of $\mathrm{POCl_3}$-annealed MOSFETs. For comparison of μ_{Hall} between NO- and $\mathrm{POCl_3}$-annealed MOSFETs, the results are also plotted in the same figure (Fig. 4.6). For example, the Hall mobilities of NO- and $\mathrm{POCl_3}$-annealed MOSFETs are 14 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ and 41 $\mathrm{cm^2\ V^{-1}\ s^{-1}}$ ($E_{\mathrm{eff}} = 1.1$ MV $\mathrm{cm^{-1}}$), respectively. In addition, the μ_{ph} reported in the previous study on μ_{Hall} of NO-annealed MOSFETs [1] shown by a dotted black line in Fig. 4.5 follows both results of as-oxidized and NO-annealed lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{14}$ $\mathrm{cm^{-3}}$) MOSFETs. On the other hand, the μ_{Hall} of $\mathrm{POCl_3}$-annealed MOSFETs exceeds the μ_{ph} reported in the previous study [1]. The μ_{Hall} enhancement observed in $\mathrm{POCl_3}$-annealed MOSFETs can be explained by suppressing the influence of Coulomb scattering due to trapped electrons. If the Coulomb scattering is dominant in SiC MOSFETs at RT, μ_{Hall} at low temperatures should be severely affected by the Coulomb scattering and be lower than that at RT. Therefore, MOS-Hall effect measurements are also conducted at 77 K to demonstrate the strong influence of Coulomb scattering.

Figure 4.7 shows the effective normal field dependences of μ_{Hall} for NO- and $\mathrm{POCl_3}$-annealed (0001) MOSFETs with various N_{A} of p-body. The open and closed symbols represent the results at 296 K and 77 K, respectively. The Hall mobilities of both NO- and $\mathrm{POCl_3}$-annealed MOSFETs at 77 K are lower than those at 296 K. In the case of Si MOSFETs, μ_{eff} ($\simeq \mu_{\mathrm{free}}$) is dominantly limited by phonon scattering at RT. As a result, μ_{free} at 77 K is higher than that at RT in the wide E_{eff} range because phonon scattering is suppressed at low temperatures. Therefore, it can be concluded that the μ_{Hall} degradation observed in SiC MOSFETs even after $\mathrm{POCl_3}$ annealing is caused by strong Coulomb scattering. Furthermore, the μ_{Hall} of NO-annealed MOSFETs is substantially decreased by lowering the temperature, whereas the μ_{Hall} of $\mathrm{POCl_3}$-annealed MOSFETs is not significantly decreased. For instance, $\mu_{\mathrm{Hall}}(77\mathrm{K})/\mu_{\mathrm{Hall}}(296\mathrm{K})$ is about 40% for $\mathrm{POCl_3}$-annealed MOSFETs at n_{free} of 2.5×10^{12} $\mathrm{cm^{-2}}$, whereas $\mu_{\mathrm{Hall}}(77\mathrm{K})/\mu_{\mathrm{Hall}}(296\mathrm{K})$ is about 19% for NO-annealed MOSFETs. This result implies that the trapped electrons tend to be strong Coulomb scattering centers especially at low temperatures.

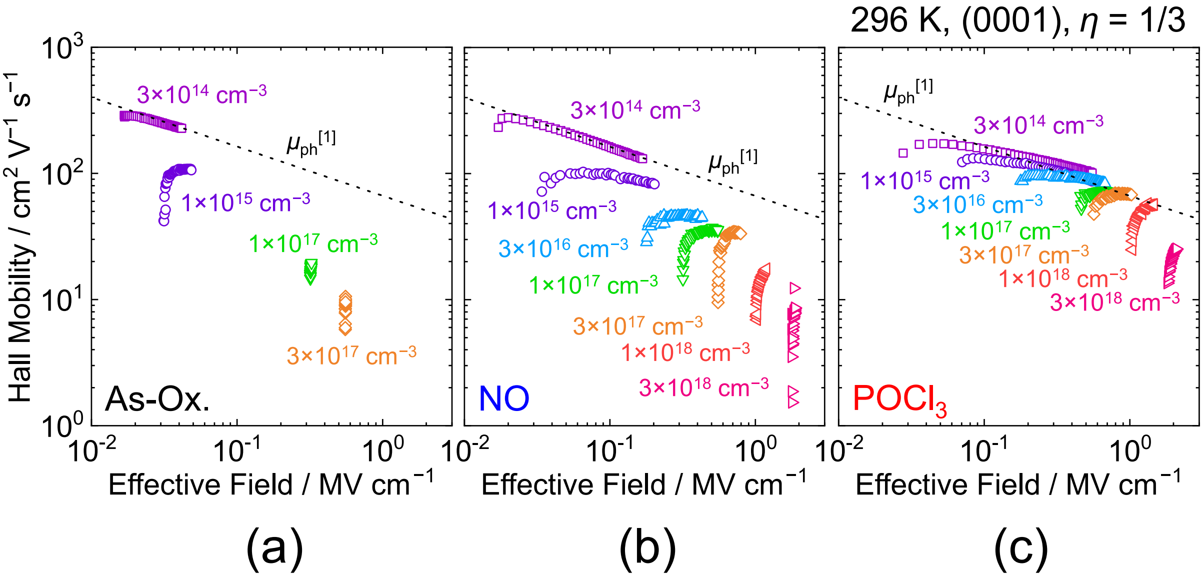


Figure 4.5: Effective normal field (E_{eff}) dependences of Hall mobility (μ_{Hall}) for (a) as-oxidized, (b) NO-annealed, and (c) POCl$_3$-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The phonon-limited mobility (μ_{ph}) reported in the previous study on μ_{Hall} for NO-annealed MOSFETs [1] is also shown.

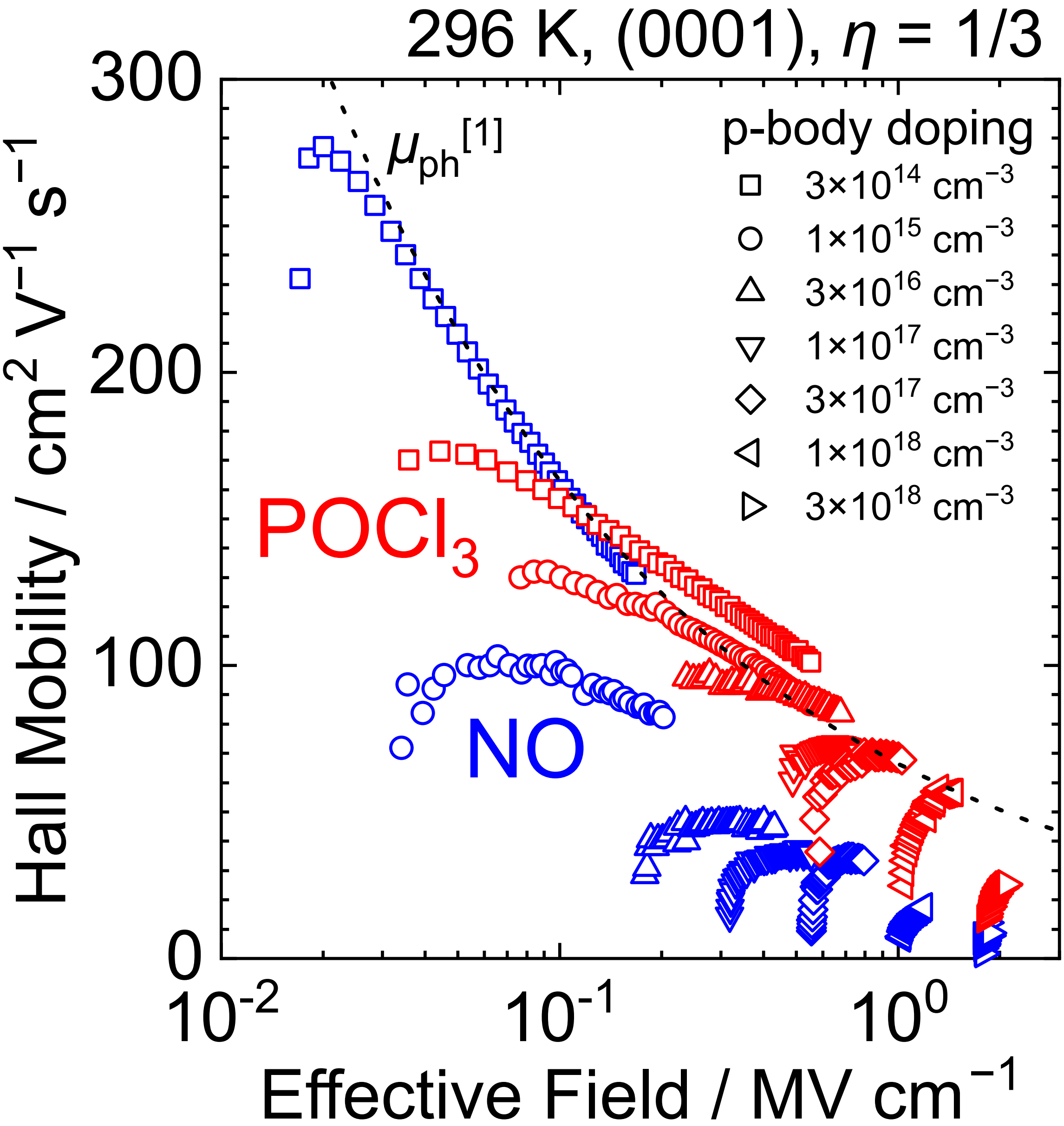


Figure 4.6: Effective normal field (E_{eff}) dependence of Hall mobility (μ_{Hall}) for NO- and POCl$_3$-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\text{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The phonon-limited mobility (μ_{ph}) reported in the previous study on μ_{Hall} for NO-annealed MOSFETs [1] is also shown.

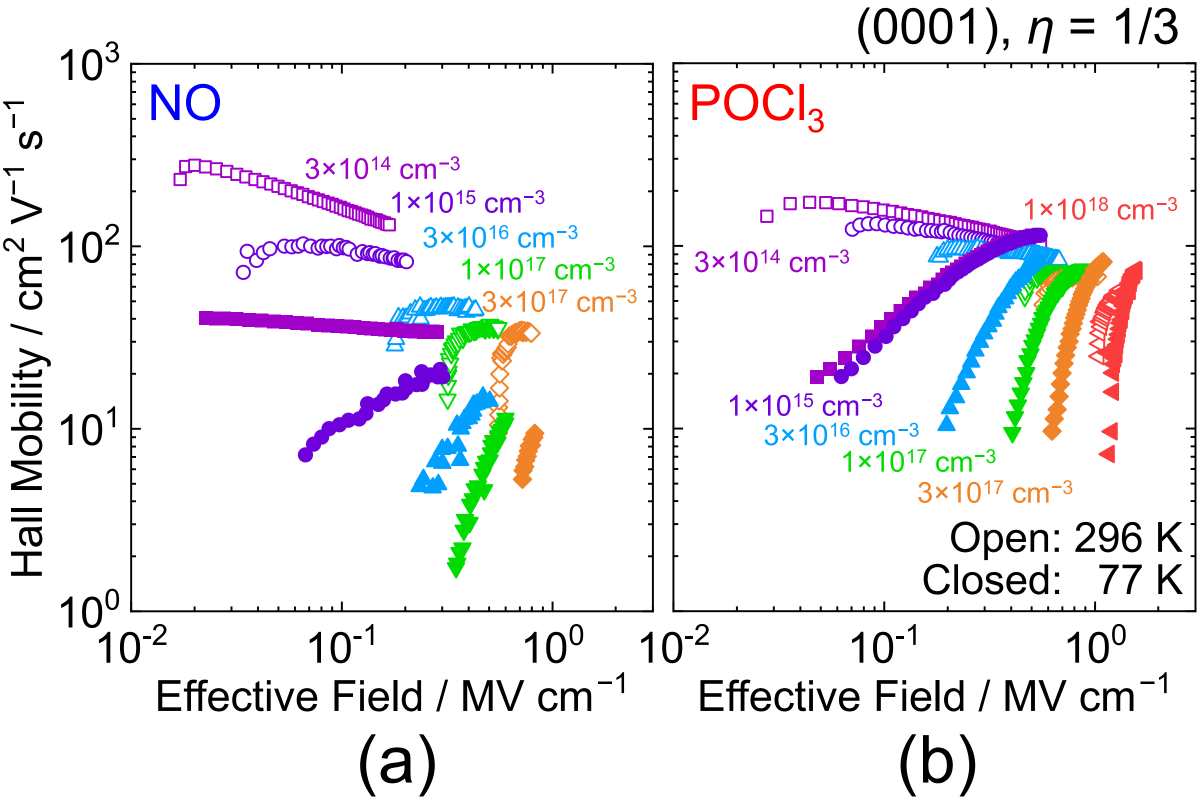


Figure 4.7: Effective normal field (E_{eff}) dependences of Hall mobility (μ_{Hall}) for (a) NO- and (b) POCl$_3$-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{18}$ cm^{-3}) of p-body. The open and closed symbols represent the results at 296 K and 77 K, respectively. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}.

4.4.2 Theoretical Analyses

In this section, to model the electron scattering in SiC/SiO$_2$ inversion layers, μ_{free} in SiC MOSFETs is calculated based on the theoretical studies [15, 16]. First, phonon scattering and Coulomb scattering due to substrate impurities are focused. The phonon scattering can be calculated because the previous study on bulk mobility [17] determined the deformation potential and energy of phonons. The impact of substrate impurities on free electrons can also be calculated by using a parameter of N_{A}. The momentum relaxation time and free electron density in the sub-bands are computed to calculate the mobilities. How to calculate momentum relaxation times of acoustic phonon scattering, non-polar optical phonon scattering, and Coulomb scattering due to substrate impurities is described in Appendix A. Note that the n_{free} and n_{trap} of lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs are used to calculate μ_{free} for all of the MOSFETs.

The μ_{free} of POCl$_3$-annealed MOSFETs is firstly calculated because the influence of Coulomb scattering due to trapped electrons is probably small. Figure 4.8 shows the effective normal field dependence of experimental μ_{Hall} and calculated μ_{free} for POCl$_3$-annealed (0001) MOSFETs with various N_{A} of p-body at 296 K. The symbols represent the results of MOS-Hall effect measurements. Calculated acoustic phonon-limited (ac), non-polar optical phonon-limited (nop), substrate impurities-limited (imp), and total (ac+nop+imp) mobilities are shown by dashed, dotted, dashed-dotted, and solid lines, respectively. In Fig. 4.8, the total mobility (ac+nop+imp) is about 4 times higher than the experimental μ_{Hall} of POCl$_3$-annealed MOSFETs. Thus, the other scattering processes should be considered to reproduce the experimental results.

Next, mobilities limited by Coulomb scattering due to fixed charges and trapped electrons and surface roughness scattering are calculated. The impact of Coulomb scattering due to fixed charges depends on the fixed charge density (N_{fix}). However, the N_{fix} is unknown because the fixed charge density obtained by threshold voltage shift is estimated as the net fixed charge density. Therefore, N_{fix} is determined as a fitting parameter in the present study. Besides, the influence of Coulomb scattering due to trapped electrons depends on n_{trap}. In this study, the n_{trap} experimentally obtained from MOS-Hall and split C_{GC}–V_{GS} measurements is used to calculate the mobility. The n_{trap} is increased by applying V_{GS}; thus, the influence of Coulomb scattering due to trapped electrons is gradually stronger. The surface roughness scattering at SiC/SiO$_2$ interfaces is possibly stronger than that at Si/SiO$_2$ interfaces. From the perspective of the AFM, the typical RMS roughness of the Si surface is < 0.1 nm before the fabrication of the MOSFETs. On the other hand, the RMS roughness of the SiC surface is increased to a few nanometers by performing epitaxial growth or high-temperature annealing [18]. In particular, a SiC (0001) surface has a large surface roughness due to an off-angle of several degrees. In general, SiC (0001)/SiO$_2$ interfaces observed by transmission electron microscope (TEM) have steps, whereas SiC ($11\bar{2}0$) and ($1\bar{1}00$)/SiO$_2$ interfaces are atomically flat. Based on the above discussion, these mobilities

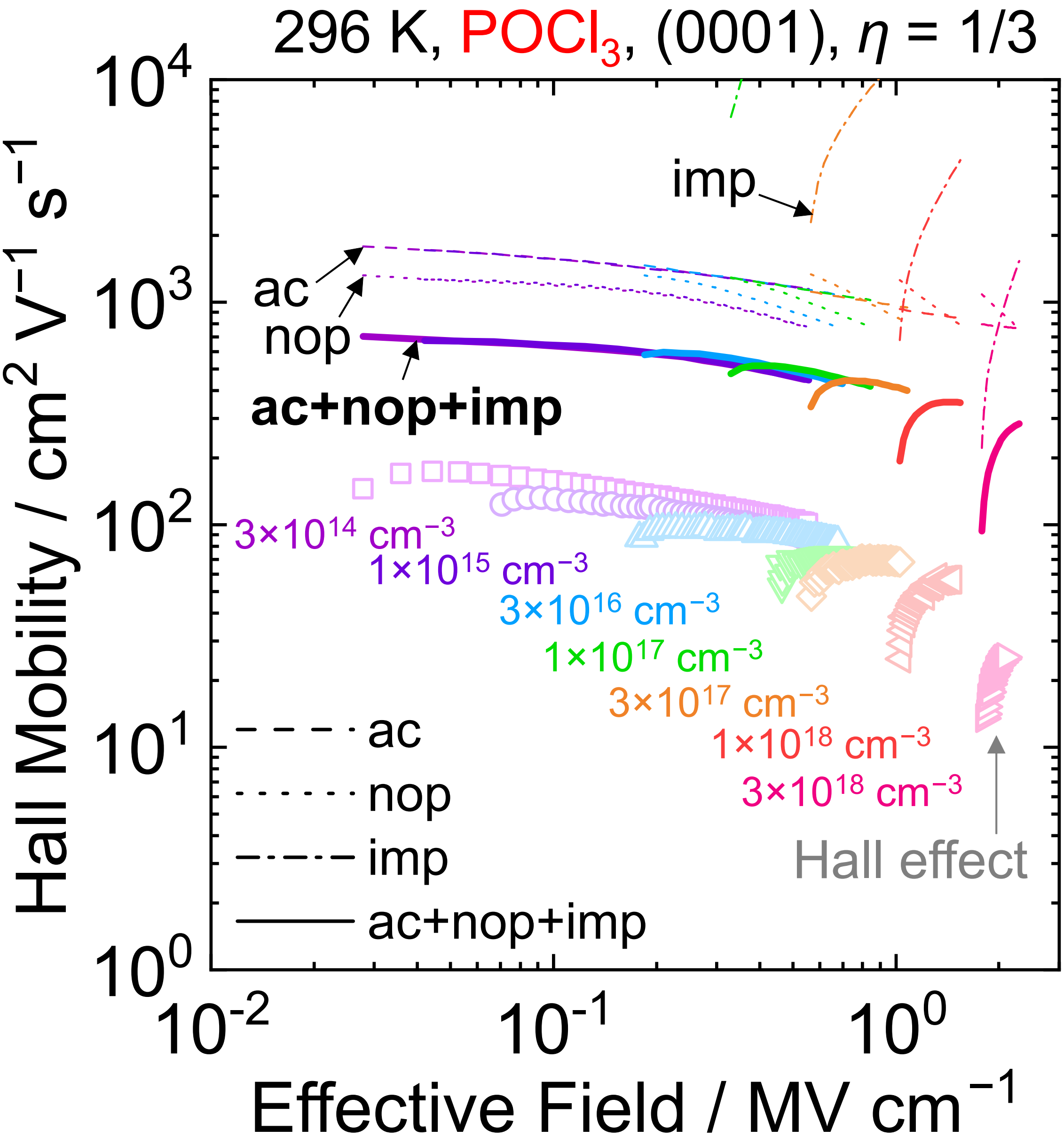


Figure 4.8: Effective normal field (E_{eff}) dependence of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for POCl$_3$-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\text{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Experimental results are represented by symbols. Calculated acoustic phonon-limited (ac), non-polar optical phonon-limited (nop), substrate impurities-limited (imp), and total (ac+nop+imp) mobilities are shown by dashed, dotted, dashed-dotted, and solid lines, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}.

are calculated using the theory explained in Appendix A.

Figure 4.9 shows the effective normal field dependence of experimental μ_{Hall} and calculated μ_{free} for POCl$_3$-annealed (0001) MOSFETs with various N_{A} of p-body at 296 K. The various colored symbols represent experimental data, and calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. The N_{fix} is set as 7.5×10^{12} cm^{-2} in the calculation. As can be seen, Coulomb scattering due to the fixed charges is dominant in a wide E_{eff} range. In addition, the $\varDelta_{\mathrm{sr}}$ and correlation length of surface roughness (L_{sr}) are set as 1.0 nm and 5.0 nm, respectively. The surface roughness scattering is also dominant in the high-E_{eff} region. These parameters can be determined independently because the influence of fixed charges is only dominant in the low-E_{eff} region ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}). In the case of Si MOSFETs, the $\varDelta_{\mathrm{sr}}$ and L_{sr} are typically in the range 0.2 nm $\leq \varDelta_{\mathrm{sr}} \leq$ 0.4 nm and 1.0 nm $\leq L_{\mathrm{sr}} \leq$ 3.0 nm, respectively [19]. Ref. 20 reported that the μ_{Hall} of MOSFETs on $(0\bar{3}3\bar{8})$ with applying negative body bias is also limited by fixed charges and surface roughness scattering. At least, N_{fix} reported in Ref. 20 is 4×10^{13} cm^{-2}, which is much higher than that in MOSFETs on (0001) obtained in this study. On the other hand, the $\varDelta_{\mathrm{sr}}$ reported in Ref. 20 is 1.2 nm, which is close to the value determined in the present study. As for the L_{sr}, the impact of L_{sr} on μ_{sr} is more negligible than the other parameters. Therefore, the L_{sr} value cannot be deeply discussed at the present stage.

Here, the effective normal field dependence of experimental μ_{Hall} and calculated μ_{free} for NO-annealed MOSFETs is shown in Fig. 4.10. In NO-annealed MOSFETs, the trapped electrons-limited mobility decreases at high V_{GS} because the n_{trap} is increased by applying gate bias. As a result, the μ_{Hall} degradation for NO-annealed MOSFETs can be demonstrated by considering strong Coulomb scattering due to trapped electrons. In Chapter 2, however, it was revealed that the trapped electrons are localized not at SiC/SiO$_2$ but in SiC. Therefore, the actual influence of Coulomb scattering due to trapped electrons differs from the above model. In order to discuss the impact of the location of trapped electrons, the author also calculates the Coulomb-limited mobility when trapped electrons are distributed in the SiC side.

Figures 4.11 and 4.12 show the experimental μ_{Hall} and μ_{free} calculated by considering depth profiles of trapped electrons as a function of E_{eff} for POCl$_3$- and NO-annealed (0001) MOSFETs with various N_{A} of p-body at 296 K. The symbols and lines are the same meaning as those in Fig. 4.10. In Figs. 4.11 and 4.12, the trapped electrons are distributed in the range 0 nm $\leq z \leq$ 1 nm and 0 nm $\leq z \leq$ 2 nm, respectively. In the present study, the trapped electrons are distributed from the interface to the SiC side as a box profile. Note that the potential distribution affected by the trapped electrons in SiC is also considered in the calculation of Poisson's equation. As can be seen, the calculated μ_{free} is not significantly decreased by changing the distribution of trapped electrons in the case

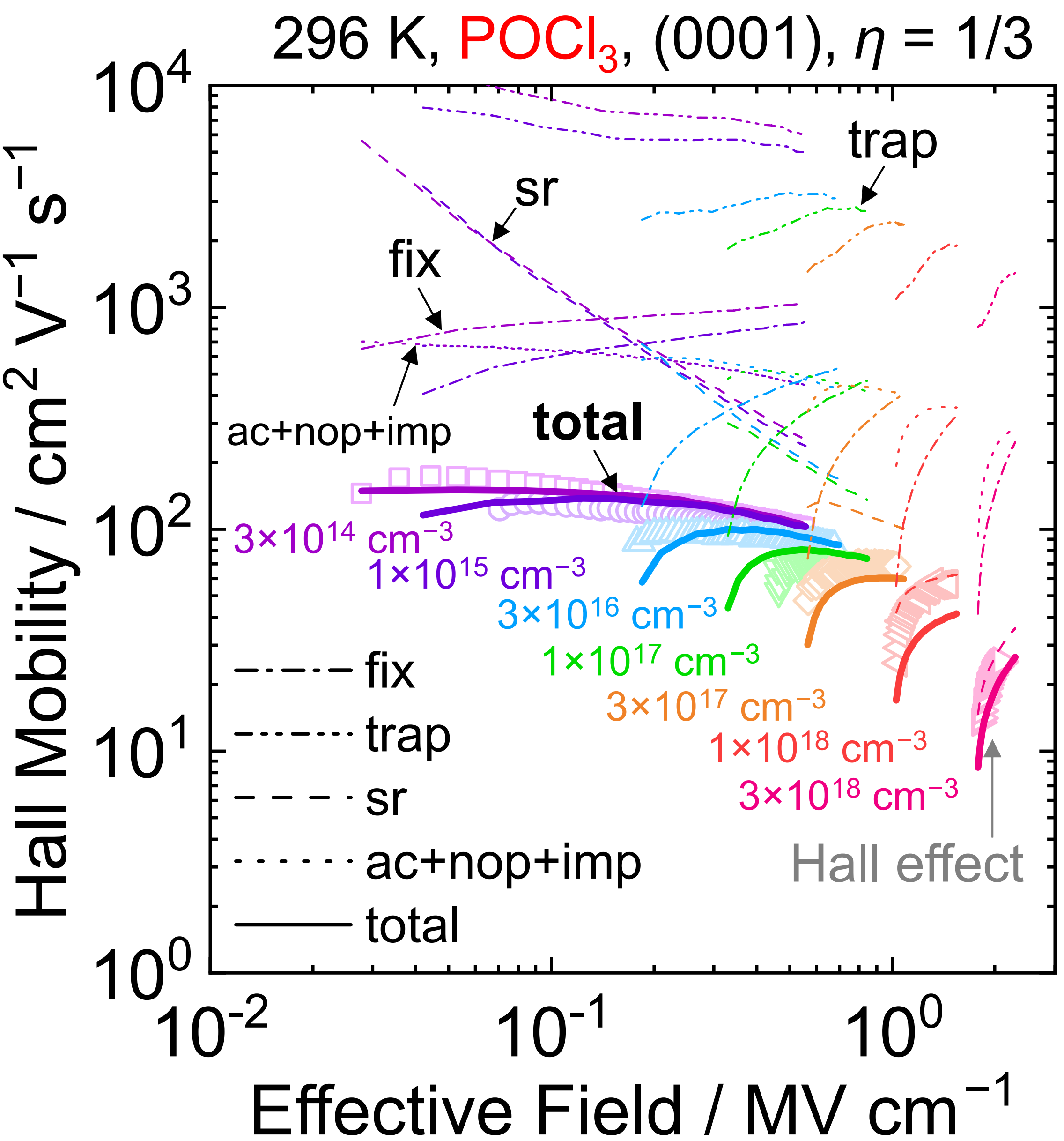


Figure 4.9: Effective normal field (E_{eff}) dependence of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for POCl$_3$-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\text{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height (Δ_{sr}), and surface roughness correlation length (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

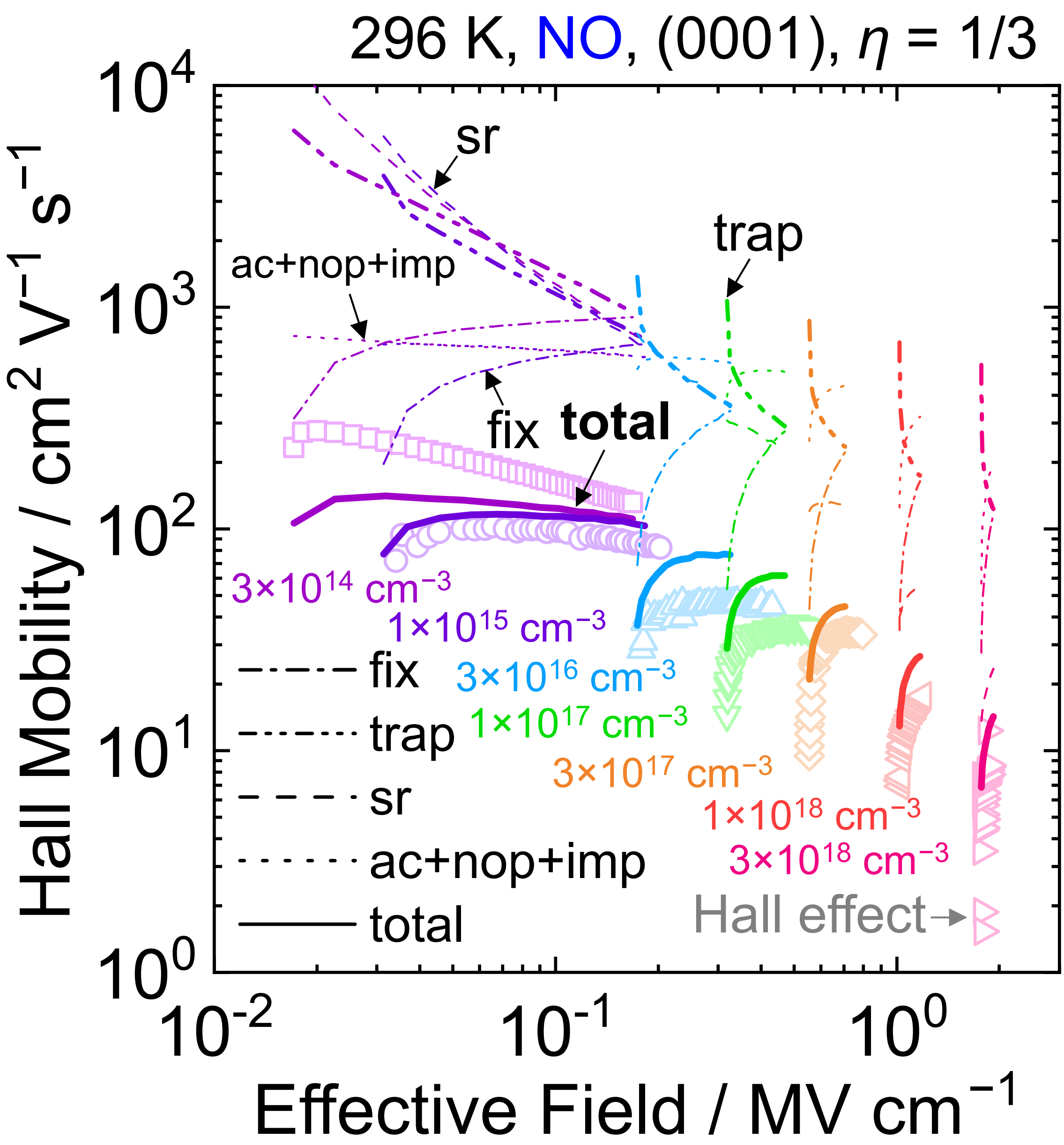


Figure 4.10: Effective normal field (E_{eff}) dependence of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for NO-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are also shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height (Δ_{sr}), and surface roughness correlation length (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

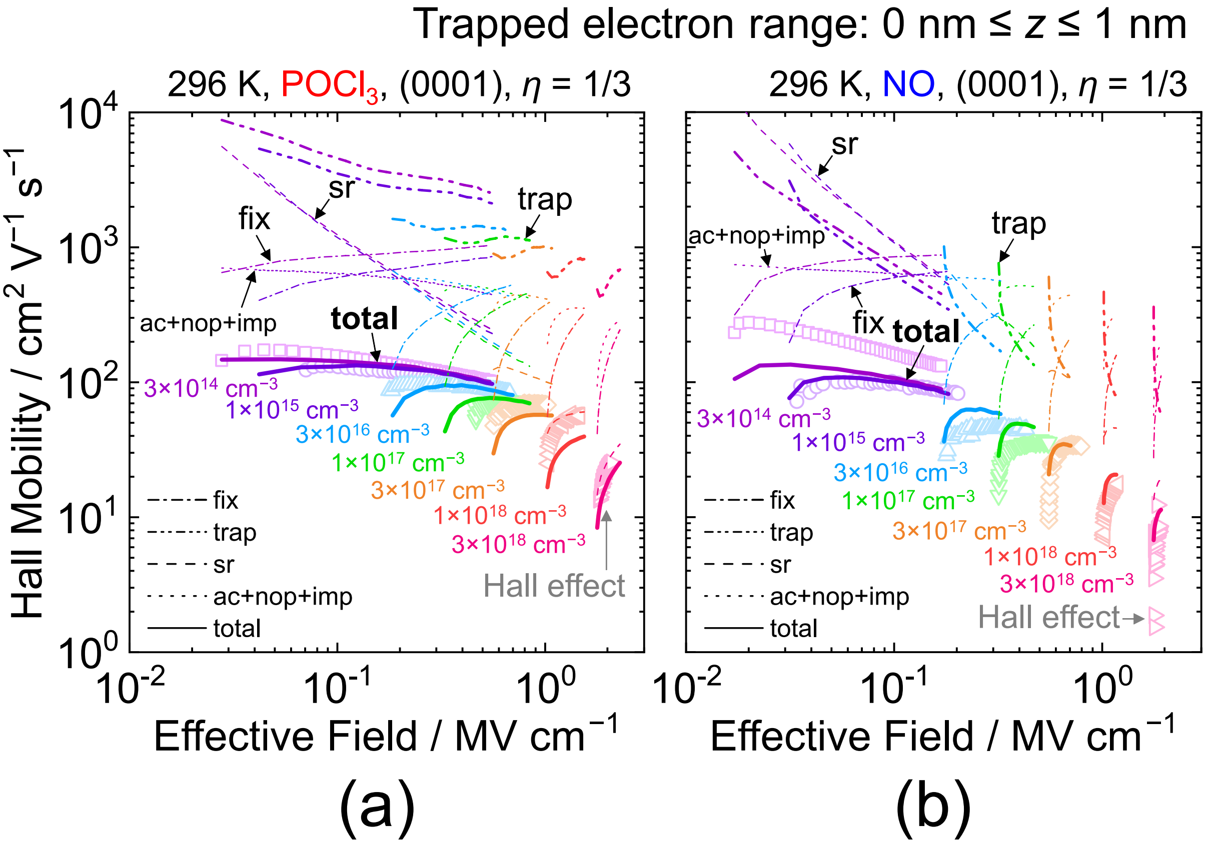


Figure 4.11: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for (a) POCl_3- and (b) NO-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\text{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. In the calculation, the trapped electron density distribution is considered to be a box profile in the range 0 nm $\leq z \leq$ 1 nm. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height (Δ_{sr}), and surface roughness correlation length (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

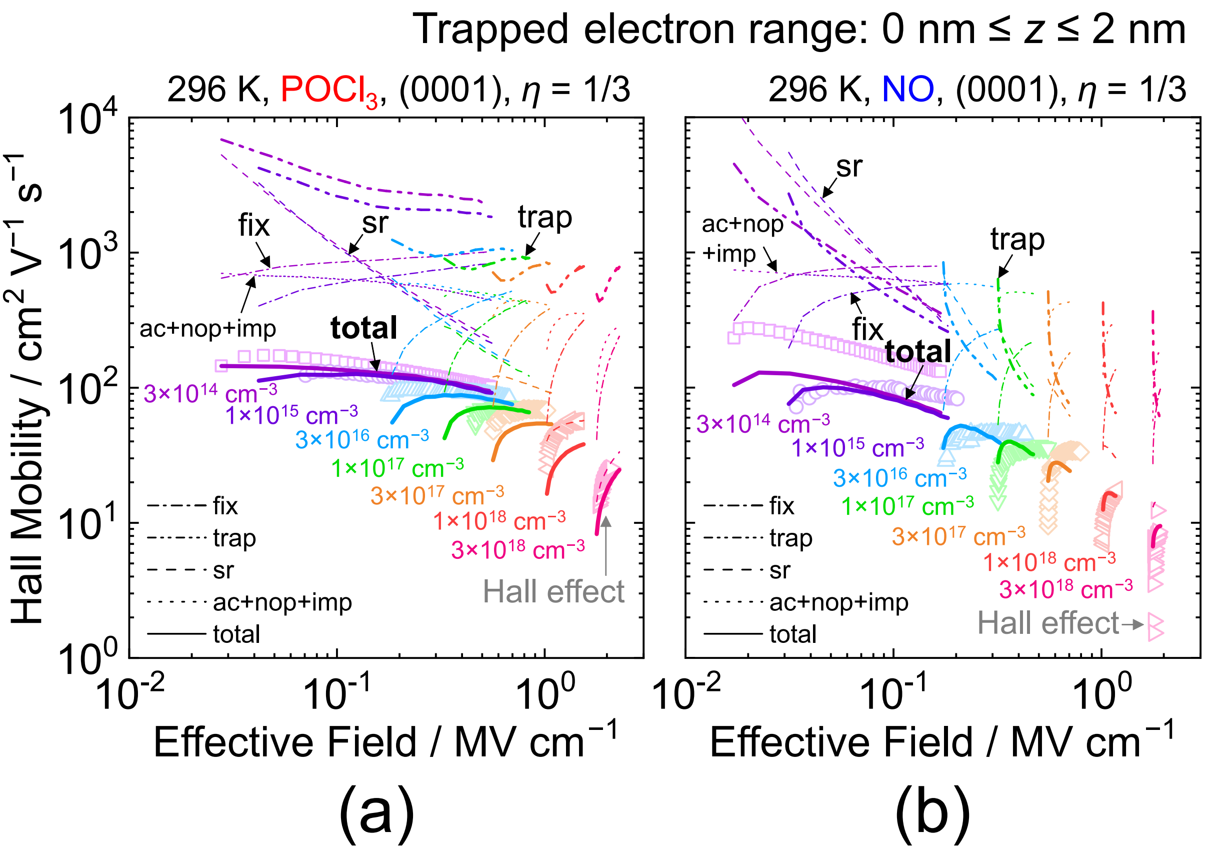


Figure 4.12: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for (a) POCl_3- and (b) NO-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\text{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. In the calculation, the trapped electron density distribution is considered to be a box profile in the range 0 nm $\leq z \leq$ 2 nm. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height ($\mathit{\Delta}_{\text{sr}}$), and surface roughness correlation length (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

of POCl_3-annealed MOSFETs [Fig. 4.11(a) and Fig. 4.12(a)]. In contrast, in the case of NO-annealed MOSFETs, the Coulomb scattering due to the trapped electrons is severely affected by the depth profiles of trapped electrons [Fig. 4.11(b) and Fig. 4.12(b)]. If the trapped electrons are localized in the range 0 nm $\leq z \leq$ 2 nm, the calculated μ_{free} is much lower than the experimental μ_{Hall}. Thus, the trapped electrons are probably localized near the MOS interfaces (0 nm $\leq z \leq$ 1 nm). However, the depth profile of trapped electrons is unknown at the present stage. The trapped electrons-limited mobility strongly depends on the position and density of trapped electrons. Therefore, to calculate the accurate μ_{free} determined by trapped electrons, the distribution of trapped electron density should be clarified in the future.

Next, calculated μ_{free} at 77 K is discussed by comparing to the μ_{Hall} in Fig. 4.7. Note that the n_{free} and n_{trap} at 296 K are used in the calculation. Figure 4.13 shows the experimental μ_{Hall} and μ_{free} calculated by considering depth profiles of trapped electrons as a function of E_{eff} for POCl_3- and NO-annealed (0001) MOSFETs with various N_{A} of p-body at 77 K. The symbols and lines are the same meaning as those in Fig. 4.10. In Fig. 4.13, the trapped electrons are distributed in the range 0 nm $\leq z \leq$ 1 nm. As for the POCl_3-annealed MOSFETs, the calculated μ_{free} is still higher than the experimental μ_{Hall}, especially for lightly-doped ($N_{\text{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs, whereas the calculated mobility is very close to the experimental one for heavily-doped (N_{A} = 1–3 $\times 10^{18}$ cm^{-3}) MOSFETs. Regarding the NO-annealed MOSFETs, the calculated μ_{free} is still higher than the μ_{Hall} for all of the MOSFETs. The impact of Coulomb scattering due to trapped electrons is probably underestimated because the depth profile (i.e., position and volume density) of trapped electrons is not yet understood. However, the phonon-limited mobility is high, and surface roughness-limited mobility does not enormously change at low temperatures from the calculation results. Therefore, although the influence of trapped electrons is not accurately modeled, strong Coulomb scattering is the most promising candidate to explain the abnormal μ_{Hall} degradation at low temperatures.

4.5 Discussion

First, the $n_{\text{free}}/n_{\text{total}}$, also discussed in Chapter 2, is summarized in Fig. 4.14. In Chapter 2, the μ_{free} was assumed to be a constant value. Therefore, the assumption influenced the $n_{\text{free}}/n_{\text{total}}$ calculated in Chapter 2. In this chapter, however, the $n_{\text{free}}/n_{\text{total}}$ is experimentally determined by MOS-Hall and split C_{GC}–V_{GS} measurements. In Fig. 4.14, although the $n_{\text{free}}/n_{\text{total}}$ especially for NO-annealed MOSFETs slightly depends on the process and measurement conditions, the $n_{\text{free}}/n_{\text{total}}$ is not decreased by increasing N_{A}. Thus, the $n_{\text{free}}/n_{\text{total}}$ does not correlate with N_{A}. This result is consistent with one of the conclusions in Chapter 2 that the abnormal μ_{eff} drop observed in NO-annealed heavily-doped MOSFETs reported in the previous study [21] is caused not by the decrease in $n_{\text{free}}/n_{\text{total}}$ but rather by the

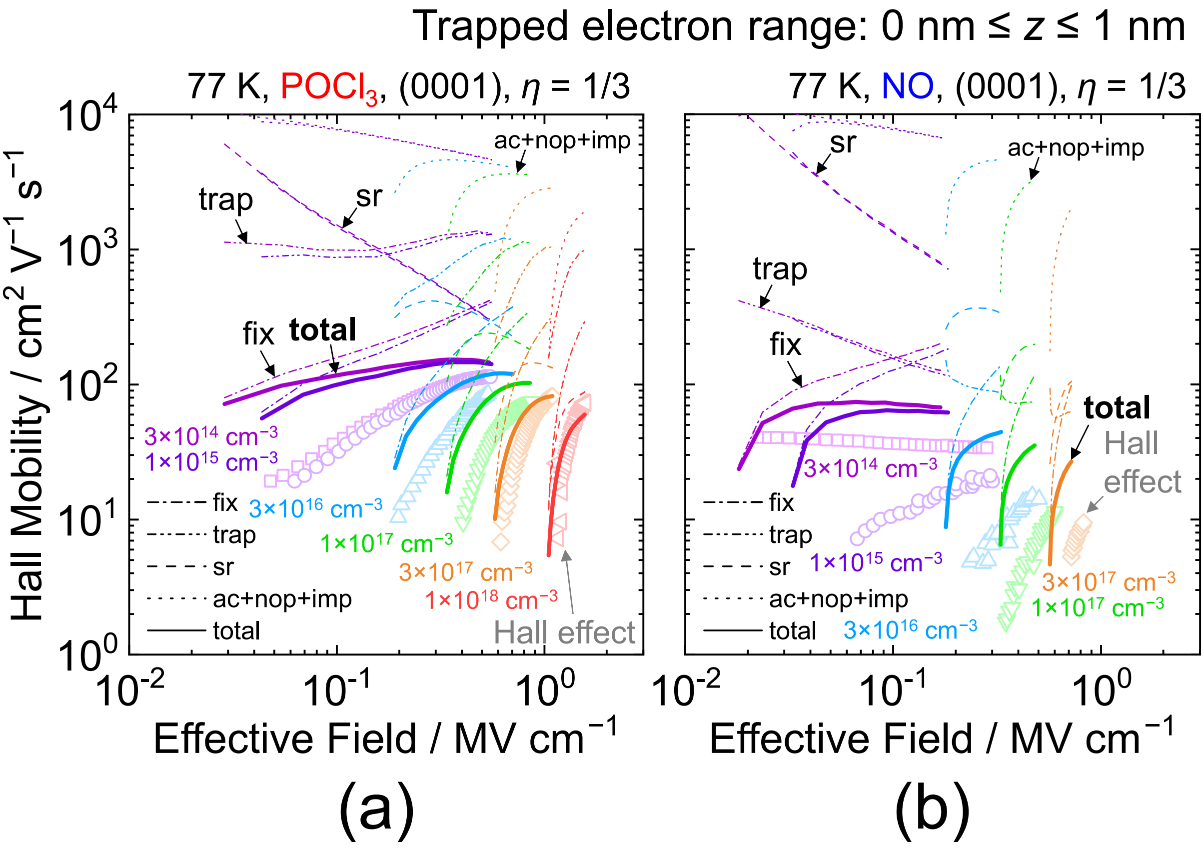


Figure 4.13: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for (a) POCl$_3$- and (b) NO-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{18}$ cm^{-3}) of p-body at 77 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. In the calculation, the trapped electron density distribution is considered to be a box profile in the range 0 nm $\leq z \leq$ 1 nm. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height (Δ_{sr}), and surface roughness correlation length (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

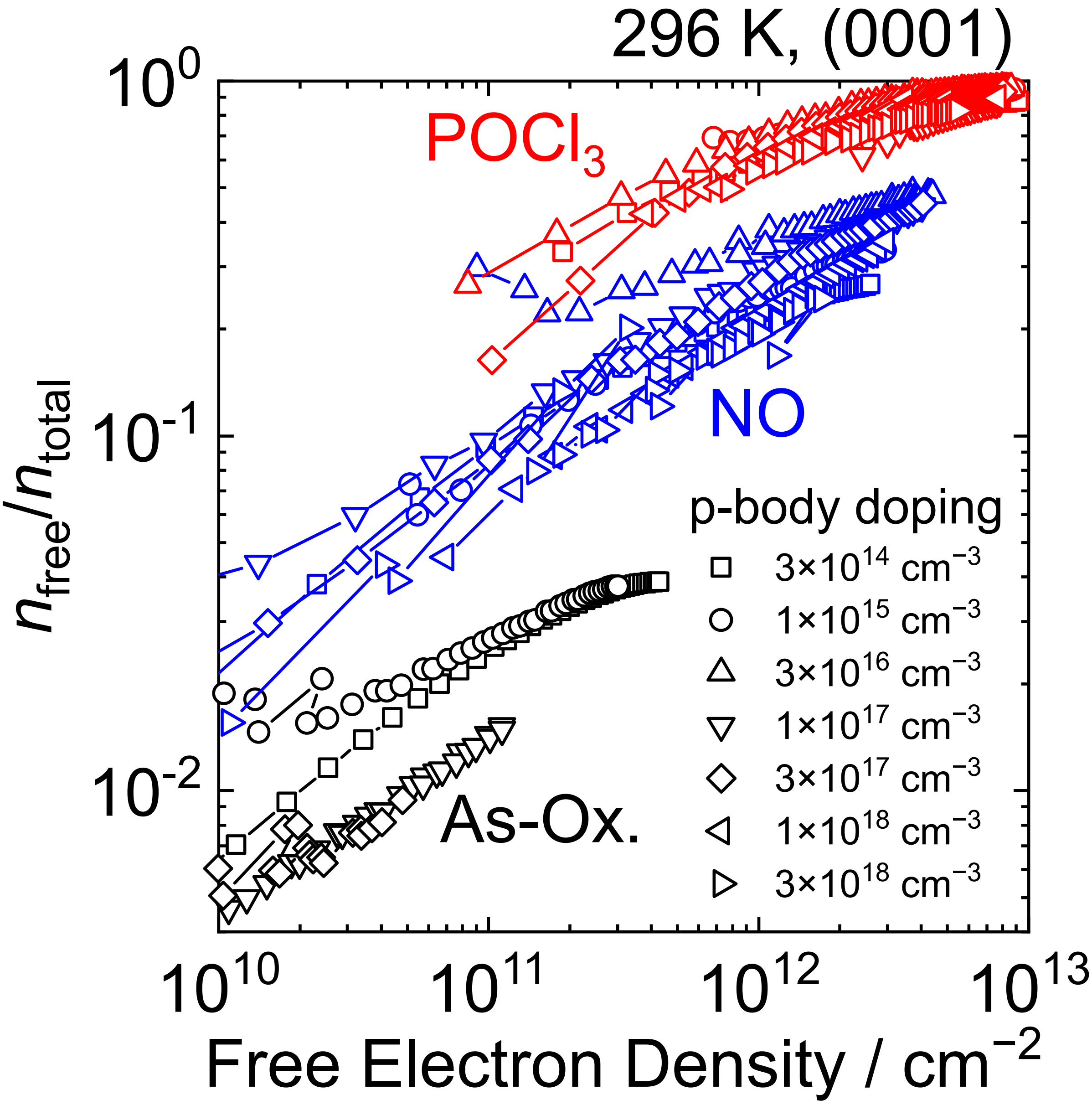


Figure 4.14: Ratio of free electrons to total electrons ($n_{\mathrm{free}}/n_{\mathrm{total}}$) as a function of the free electron density (n_{free}) for as-oxidized, NO-annealed, and POCl$_3$-annealed SiC (0001) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K.

decrease in μ_{free}.

The reason why the μ_{Hall} of POCl$_3$-annealed MOSFETs is higher compared to the other MOSFETs can be explained by the difference in trapped electron density. Figure 4.15 shows the schematic band diagrams of as-oxidized and NO-annealed MOS interfaces and POCl$_3$-annealed ones. As for the as-oxidized and NO-annealed MOS interfaces, the n_{trap} is high ($n_{\mathrm{trap}} \sim 2.5$–$11 \times 10^{12}$ cm^{-2} at V_{GS} of 25 V). On the other hand, the n_{trap} at POCl$_3$-annealed MOS interfaces is low ($n_{\mathrm{trap}} \sim 4.9 \times 10^{11}$ cm^{-2} at V_{GS} of 25 V). As a result, the density of Coulomb scattering centers at POCl$_3$-annealed MOS interfaces is reduced to 1/10 compared to that at as-oxidized and NO-annealed ones. In addition, a previous study on μ_{Hall} of MOSFETs fabricated on various crystal faces implies that the MOSFETs with low n_{trap} tend to record high μ_{Hall} [22]. These high μ_{Hall} data on the $(11\bar{2}0)$ and $(0\bar{3}3\bar{8})$ faces can be interpreted by the much lower n_{trap}, as in the case of POCl$_3$-annealed MOSFETs. Furthermore, to consider the mobility improvement under the high-E_{eff} region, the distance from Coulomb scattering centers is essential. When the E_{eff} increases, the free electrons approach the SiC/SiO$_2$ interfaces and must be more strongly affected by the Coulomb scattering centers originating from the trapped electrons. Thus, the degradation of μ_{Hall} is considerably small for POCl$_3$-annealed MOSFETs in the high-E_{eff} region owing to much smaller n_{trap}.

However, the μ_{Hall} of NO-annealed MOSFETs is very close to as-oxidized ones in the wide N_{A} range (3×10^{14} cm$^{-3} \leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}) in Fig. 4.5. In addition to that, the μ_{Hall} of POCl$_3$-annealed lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs is lower than that of NO-annealed ones in Fig. 4.6. For example, μ_{Hall} is 172 cm^2 V^{-1} s^{-1} and 207 cm^2 V^{-1} s^{-1} at $E_{\mathrm{eff}} = 0.053$ MV cm^{-1} for POCl$_3$- and NO-annealed MOSFETs, respectively. Thus, this result contradicts the above mobility enhancement model in Fig. 4.15. In actual, the calculated μ_{free} of NO-annealed lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs is underestimated in Fig. 4.11. Ref. 16 reported that the difference in μ_{Hall} of between as-oxidized and NO-annealed MOSFETs can be explained if Coulomb and surface roughness scattering is considered to be screened by both free and trapped electrons. In the case of POCl$_3$-annealed MOSFETs, the influence of screening by trapped electrons is smaller compared to the as-oxidized and NO-annealed MOSFETs. As a result, the μ_{Hall} of POCl$_3$-annealed lightly-doped ($N_{\mathrm{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs is smaller than that of NO-annealed ones. As another possibility, the density and correlation effect of fixed charges at NO-annealed SiC/SiO$_2$ interfaces may be different from those at POCl$_3$-annealed ones. In particular, the correlation effect of fixed charges is discussed in Appendix A.

4.6 Summary

In summary, μ_{Hall} of POCl$_3$-annealed MOSFETs with various p-body doping concentrations (3×10^{14} cm$^{-3} \leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) at RT and 77 K is investigated. At RT, in the

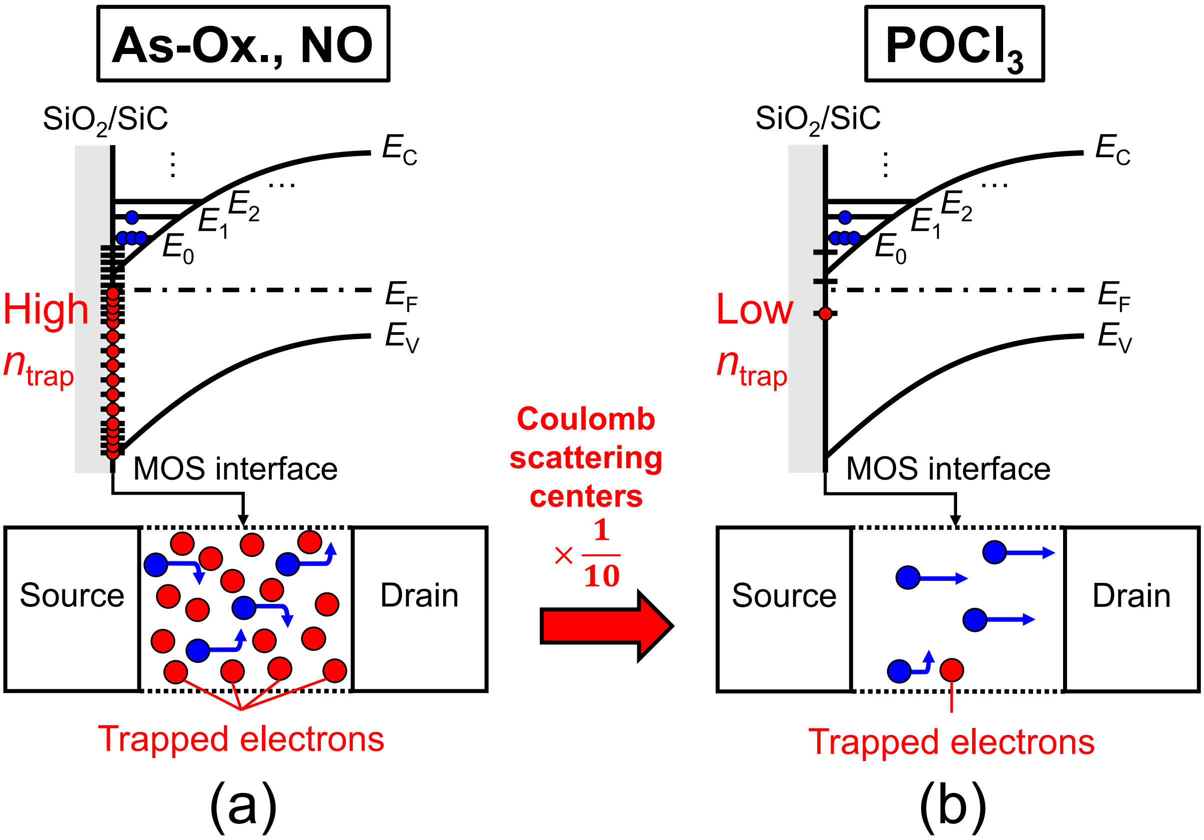


Figure 4.15: Schematic band diagrams of (a) as-oxidized and NO-annealed and (b) POCl$_3$-annealed SiC MOS interfaces. Here, E_C is the conduction band edge, E_F is the Fermi level, and E_V is the valence band edge.

lightly-doped ($N_\mathrm{A} = 3 \times 10^{14}$ cm^{-3}) POCl$_3$-annealed MOSFETs, n_free (9.2×10^{12} cm^{-2}) is close to n_total (1.0×10^{13} cm^{-2}) at $V_\mathrm{GS} = 25$ V. The D_it near the band edge extracted from the MOS-Hall effect measurements on the POCl$_3$-annealed MOSFETs is significantly lower than that of as-oxidized and NO-annealed MOSFETs ($D_\mathrm{it} > 10^{13}$ cm^{-2} eV^{-1} at $E_\mathrm{C}(\mathrm{2D\text{-}DOS}) - 0.075$ eV). The μ_Hall of POCl$_3$-annealed MOSFETs is much higher than that of as-oxidized and NO-annealed MOSFETs for almost all p-body doping concentrations. In the high-E_eff region ($E_\mathrm{eff} = 1.1$ MV cm^{-1}), the μ_Hall is 14 cm^2 V^{-1} s^{-1} for NO-annealed MOSFETs, whereas the μ_Hall is 41 cm^2 V^{-1} s^{-1} for POCl$_3$-annealed ones. At 77 K, the μ_Hall is degraded by lowering the temperature for both NO- and POCl$_3$-annealed MOSFETs. In particular, the μ_Hall of NO-annealed MOSFETs significantly decreases compared to that at RT. The above-obtained results can be considered that the μ_Hall enhancement and the suppression of μ_Hall degradation in POCl$_3$-annealed MOSFETs are caused by lower n_trap. The influence of Coulomb scattering due to trapped electrons is also investigated based on the theoretical mobility calculation. As a result, the μ_Hall of POCl$_3$-annealed MOSFETs can be mainly explained by Coulomb scattering due to fixed charges and surface roughness scattering. In addition to the scattering processes, the μ_Hall of NO-annealed MOSFETs is limited by Coulomb scattering due to trapped electrons.

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Chapter 5

Electron Scattering Mechanism in SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs

5.1 Introduction

In Chapter 4, the electron scattering mechanism in SiC (0001)/SiO_2 inversion layers was discussed. In actual trench-type vertical power MOSFETs, however, an inversion channel is typically formed at SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO_2 interfaces. Therefore, the electron scattering mechanism in SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO_2 inversion layers is also needed to clarify. In addition, the N_A dependence of μ_Hall is critical to prevent short-channel effects, which was not sufficiently investigated in the previous studies on μ_Hall for MOSFETs on non-polar faces [1–3]. Moreover, the temperature dependence of μ_Hall for MOSFETs on non-polar faces [2] was rarely reported.

Ref. 1 reported that the D_it of MOSFETs on $(0\bar{3}3\bar{8})$ and $(11\bar{2}0)$ is lower than that of MOSFETs on (0001) and $(000\bar{1})$. The results also show that MOSFETs with lower n_trap tend to have higher μ_Hall [1]. Recently, Ref. 3 reported that the μ_Hall of MOSFETs on polar faces is lower than that of MOSFETs on $(0\bar{3}3\bar{8})$ and non-polar faces. However, the electron scattering mechanism in SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO_2 inversion layers, especially Coulomb scattering due to trapped electrons, is not extensively discussed at the present stage. In this chapter, MOS-Hall effect measurements are performed for MOSFETs with various N_A of p-body on the $(11\bar{2}0)$ and $(1\bar{1}00)$ substrates at RT and 77 K.

First, the densities of free and trapped electrons for SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs are measured by MOS-Hall effect and split C_GC–V_GS measurements. Then, the D_it distribution of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs is also extracted and compared to that of the (0001) ones. After that, the electron scattering mechanism in NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs is discussed comparing the experimental μ_Hall to calculated μ_free.

5.2 Experimental Details

Figure 5.1(a) shows the process flow of the MOSFETs fabricated on non-polar faces. The p-type 4H-SiC (11$\bar{2}$0) and (1$\bar{1}$00) epitaxial layers (4×10^{15} cm^{-3} $\leq N_\mathrm{A} \leq 1 \times 10^{17}$ cm^{-3} and 1×10^{16} cm^{-3} $\leq N_\mathrm{A} \leq 3 \times 10^{17}$ cm^{-3}, respectively) were used in this chapter. The source/drain ($N_\mathrm{D} = 1.0 \times 10^{20}$ cm^{-3}) and body regions ($N_\mathrm{A} = 1.6 \times 10^{20}$ cm^{-3}) were formed by P$^+$ and Al$^+$ ion implantation, respectively. After ion implantation, activation annealing was performed at 1750°C for 20 min. The gate oxides were formed by dry oxidation at 1300°C for 5 min with subsequent annealing in NO (10% diluted in N$_2$) at 1250°C for 70 min. The resultant oxide thickness was 55 nm for both NO-annealed (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs. The channel length and width of the eight-terminal MOS-Hall bar devices were 500 μm and 100 μm, respectively. The schematic device structures are described in Fig. 5.1(b). The measurements were conducted at RT (296 K) and 77 K.

5.3 Energy Distribution of Interface State Density Extracted from MOS-Hall Effect Measurements

5.3.1 Densities of Free and Trapped Electrons

Figure 5.2 shows the gate voltage dependences of n_free, n_trap, and n_total for NO-annealed lightly- ($N_\mathrm{A} = 4 \times 10^{15}$ cm^{-3}) and heavily-doped ($N_\mathrm{A} = 1 \times 10^{17}$ cm^{-3}) (11$\bar{2}$0) MOSFETs and for lightly- ($N_\mathrm{A} = 1 \times 10^{16}$ cm^{-3}) and heavily-doped ($N_\mathrm{A} = 3 \times 10^{17}$ cm^{-3}) (1$\bar{1}$00) ones at 296 K. As for the lightly-doped MOSFETs, the n_trap of NO-annealed (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs is 1.8 times higher than that of POCl$_3$-annealed (0001) ones and is 3.9 times lower than that of NO-annealed (0001) ones at $n_\mathrm{free} = 2.0 \times 10^{12}$ cm^{-2}. Thus, the n_trap of MOSFETs on non-polar faces is relatively small, which is consistent with the previous results of MOS-Hall effect measurements for NO-annealed lightly-doped (11$\bar{2}$0) MOSFETs [1]. The $n_\mathrm{free}/n_\mathrm{total}$ at n_total of 5×10^{12} cm^{-2} is about 64% and 66% for the lightly-doped (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs, respectively. On the other hand, the ratio is about 60% and 45% for the heavily-doped (11$\bar{2}$0) and (1$\bar{1}$00) ones, respectively. Although the $n_\mathrm{free}/n_\mathrm{total}$ slightly depends on the process and measurement conditions, the n_free of NO-annealed MOSFETs on non-polar faces is higher than that of the MOSFETs on (0001).

5.3.2 Energy Distribution of Interface State Density

Figure 5.3 shows the energy distributions of D_it plotted with respect to E_C(2D-DOS) for NO-annealed (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs with various N_A of p-body. The energy distribution of D_it was extracted by Eq. 4.1. In Fig. 5.3, the D_it of MOSFETs on non-polar faces does not strongly depend on N_A, and the D_it is not significantly changed by increasing the energy. In contrast, the D_it of NO-annealed MOSFETs on (0001) increases exponentially

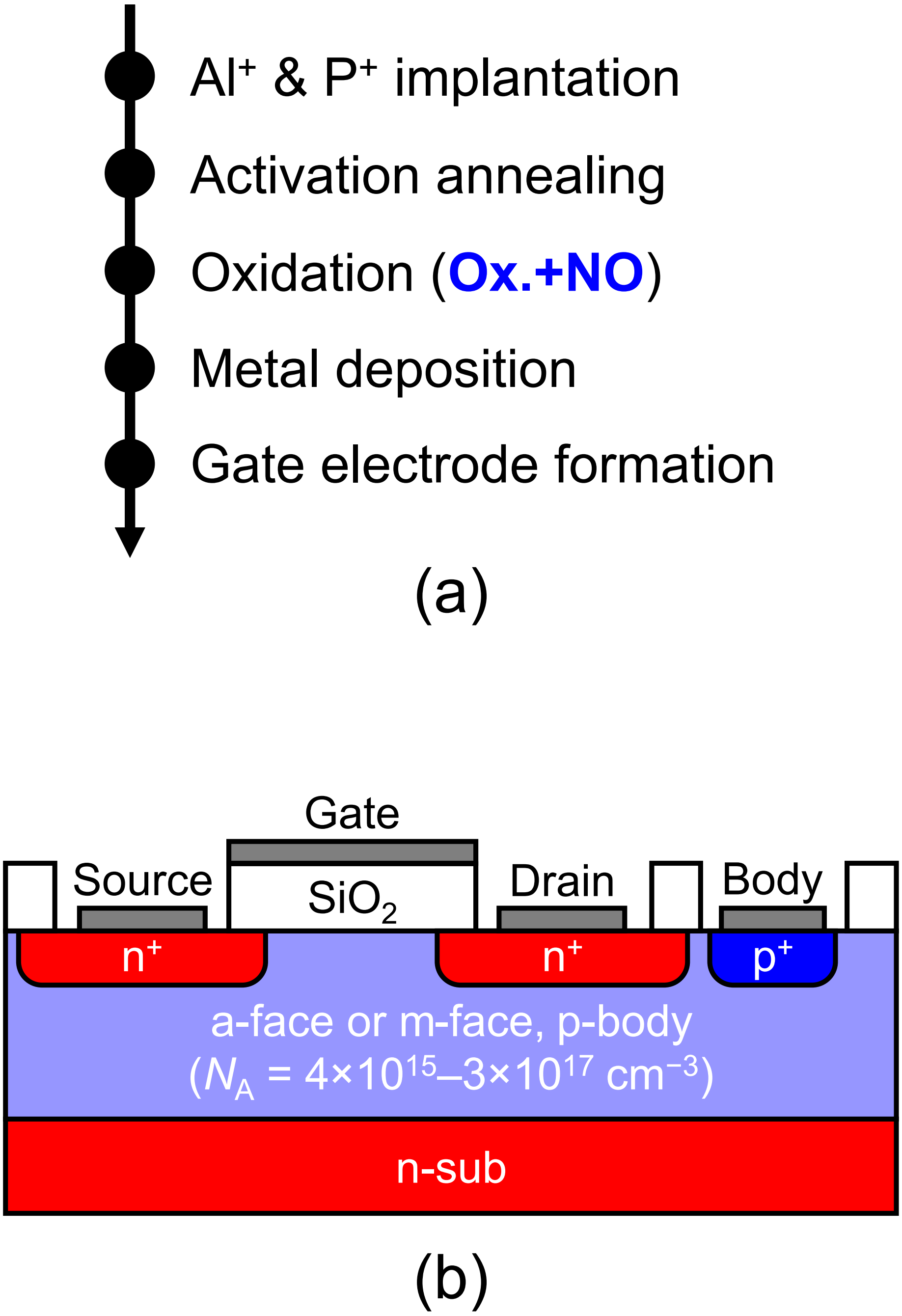

Figure 5.1: (a) Process flow of the fabricated SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs for MOS-Hall effect measurements. (b) Schematic device structure of the fabricated MOSFETs from the cross-sectional view.

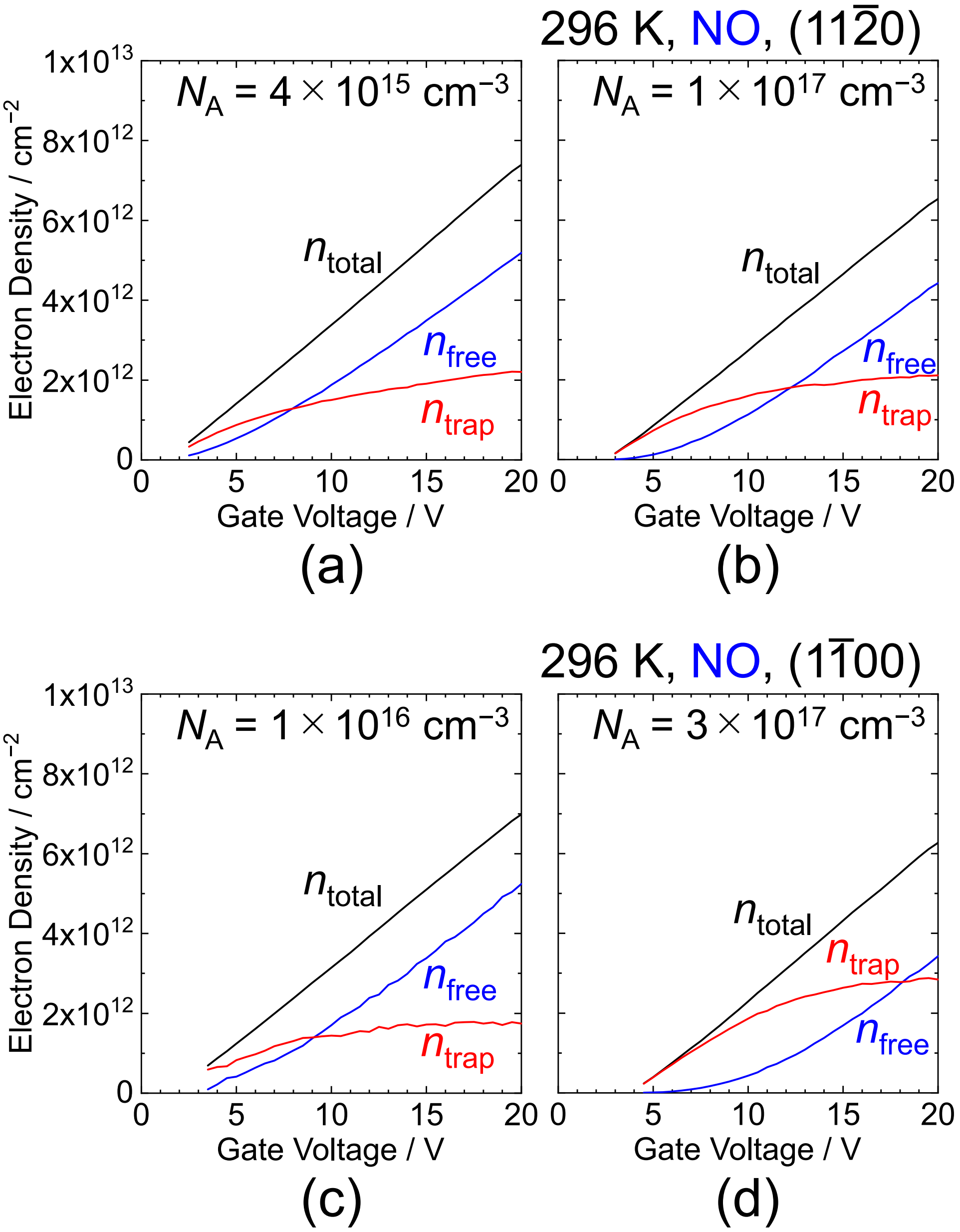

Figure 5.2: Gate voltage dependences of the densities of free electrons (n_{free}), trapped electrons (n_{trap}), and total electrons (n_{total}) for NO-annealed (a) lightly- ($N_{\text{A}} = 4 \times 10^{15}$ cm^{-3}) and (b) heavily-doped ($N_{\text{A}} = 1 \times 10^{17}$ cm^{-3}) SiC (11$\bar{2}$0) MOSFETs and for NO-annealed (c) lightly- ($N_{\text{A}} = 1 \times 10^{16}$ cm^{-3}) and (d) heavily-doped ($N_{\text{A}} = 3 \times 10^{17}$ cm^{-3}) (1$\bar{1}$00) ones at 296 K.

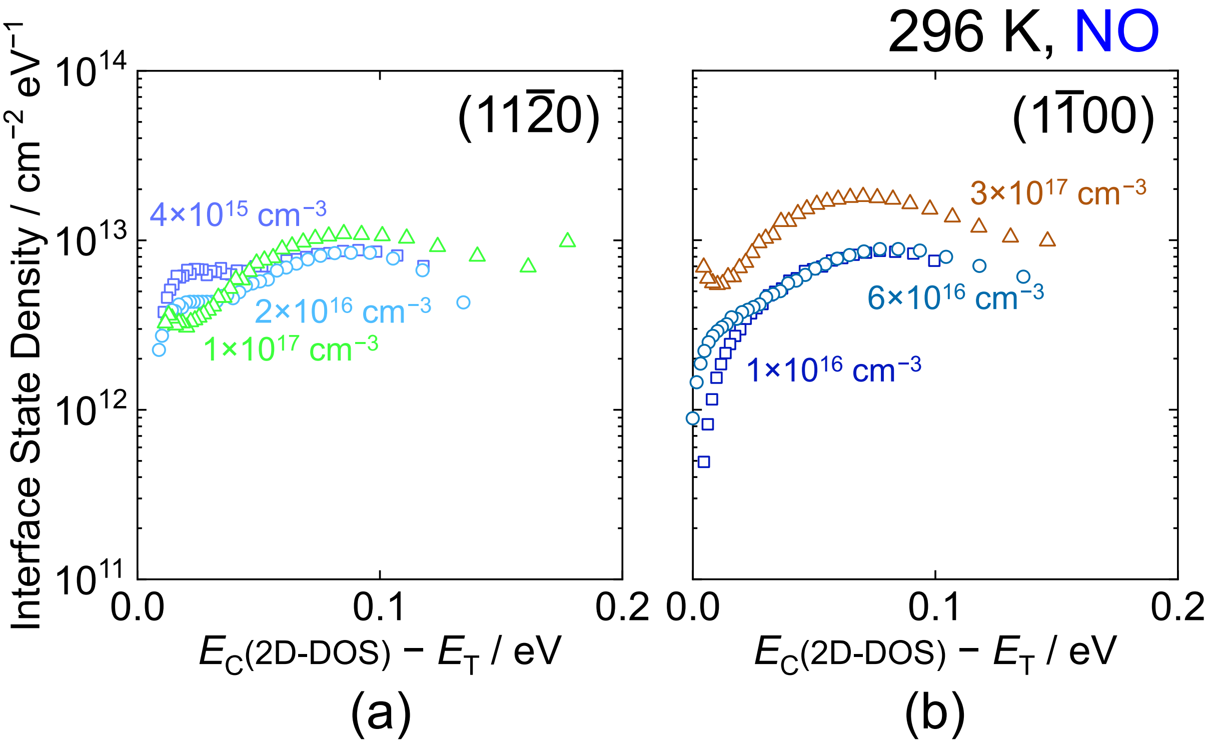

Figure 5.3: Energy distributions of interface state density plotted with respect to the bottom edge of the two-dimensional density of states [E_C(2D-DOS)] for NO-annealed SiC (a) (11$\bar{2}$0) and (b) (1$\bar{1}$00) MOSFETs with various acceptor concentrations (4×10^{15} cm^{-3} $\leq N_A \leq 1 \times 10^{17}$ cm^{-3} and 1×10^{16} cm^{-3} $\leq N_A \leq 3 \times 10^{17}$ cm^{-3}, respectively) of p-body at 296 K.

toward E_{C}(2D-DOS) [Fig. 4.2(b)]. For example, D_{it} is approximately 10^{13} cm^{-2} eV^{-1} for NO-annealed MOSFETs on non-polar faces in the range 0.0 eV $\leq E_{\mathrm{C}}(\text{2D-DOS}) - E_{\mathrm{T}} \leq 0.2$ eV. In this study, D_{it} very near E_{C}(2D-DOS) can be obtained owing to lower n_{trap}, and thus higher n_{free}.

5.4 Hall Mobility

5.4.1 Experimental Results

Figure 5.4 shows the effective normal field dependences of μ_{Hall} for NO-annealed (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ MOSFETs with various N_{A} of p-body at 296 K. The μ_{ph} reported in the previous study on μ_{Hall} for NO-annealed (0001) MOSFETs [4] is also shown in Fig. 5.4. The μ_{Hall} for MOSFETs on between (0001) and non-polar faces are plotted in Fig. 5.5 for comparison. The μ_{Hall} of NO-annealed MOSFETs on non-polar faces is 1.5 times higher than that of MOSFETs on (0001). On the other hand, the n_{trap} of NO-annealed MOSFETs on non-polar faces is 3.9 times lower than that of MOSFETs on (0001) at n_{free} of 2.0×10^{12} cm^{-2}. This result suggests that the μ_{Hall} enhancement observed in NO-annealed MOSFETs on non-polar faces can be explained by lower n_{trap} compared to NO-annealed (0001) MOSFETs.

The results of μ_{Hall} for NO-annealed (0001), $(11\bar{2}0)$, and $(1\bar{1}00)$ MOSFETs with various N_{A} of p-body at 296 K and 77 K are shown in Fig. 5.6. The open and closed symbols represent the results at 296 K and 77 K, respectively. As can be seen, the μ_{Hall} for all of the MOSFETs is decreased by lowering the temperature. The cause of μ_{Hall} degradation at low temperatures is probably strong Coulomb scattering. As already mentioned in Chapter 4, the μ_{free} in Si/SiO$_2$ inversion layers increases at low temperatures because the impact of phonon scattering is suppressed [5]. Thus, the μ_{Hall} degradation due to low temperature is peculiar to SiC MOSFETs on both polar and non-polar faces. In particular, μ_{Hall} of MOSFETs on (0001) markedly decreases compared to the results of MOSFETs on non-polar faces. The μ_{Hall} of NO-annealed MOSFETs on non-polar faces is 3.0 times higher than that of MOSFETs on (0001) at 77 K. This result implies that the trapped electrons act as strong Coulomb scattering centers at 77 K.

5.4.2 Theoretical Analyses

In this section, the electron scattering in SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO$_2$ inversion layers is explained based on theoretical calculation. The μ_{free} is calculated using the same procedure as for the SiC (0001) MOSFETs in Chapter 4 [6, 7]. First, phonon scattering and Coulomb scattering due to substrate impurities are focused. How to calculate momentum relaxation times of acoustic phonon scattering, non-polar optical phonon scattering, and Coulomb scattering due to the substrate impurities is described in Appendix A. In the calculation, the experimentally obtained n_{free} and n_{trap} at 296 K of lightly-doped [$N_{\mathrm{A}} = 4\times10^{15}$ cm^{-3}

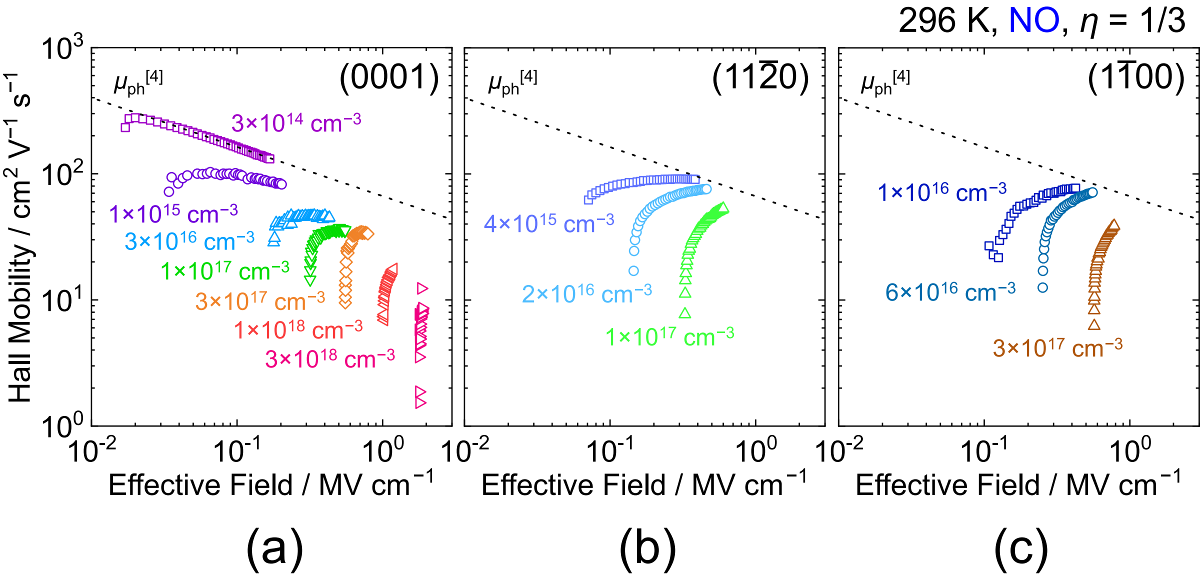

Figure 5.4: Effective normal field (E_{eff}) dependences of Hall mobility (μ_{Hall}) for NO-annealed SiC (a) (0001), (b) $(11\bar{2}0)$, and (c) $(1\bar{1}00)$ MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3\times10^{18}$ cm^{-3}, 4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1\times10^{17}$ cm^{-3}, and 1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3\times10^{17}$ cm^{-3}, respectively) of p-body at 296 K. Here, η $(= 1/3)$ is a parameter that indicates how much the electrons contribute to the E_{eff}. The phonon-limited mobility (μ_{ph}) reported in the previous study on μ_{Hall} for NO-annealed (0001) MOSFETs [4] is also shown.

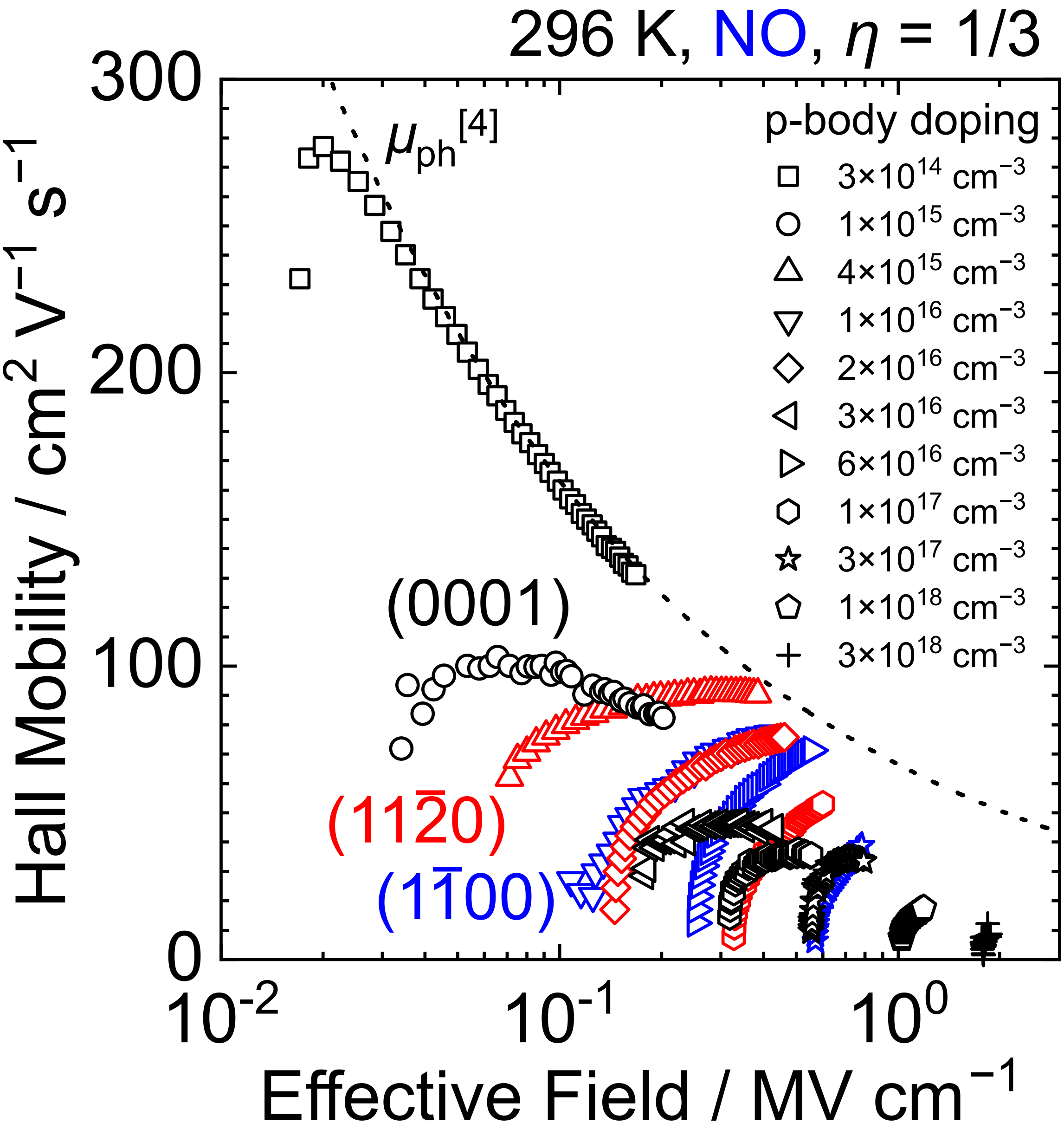

Figure 5.5: Effective normal field (E_{eff}) dependence of Hall mobility (μ_{Hall}) for NO-annealed SiC (0001), (11$\bar{2}$0), and (1$\bar{1}$00) MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) of p-body at 296 K. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The phonon-limited mobility (μ_{ph}) reported in the previous study on μ_{Hall} for NO-annealed (0001) MOSFETs [4] is also shown.

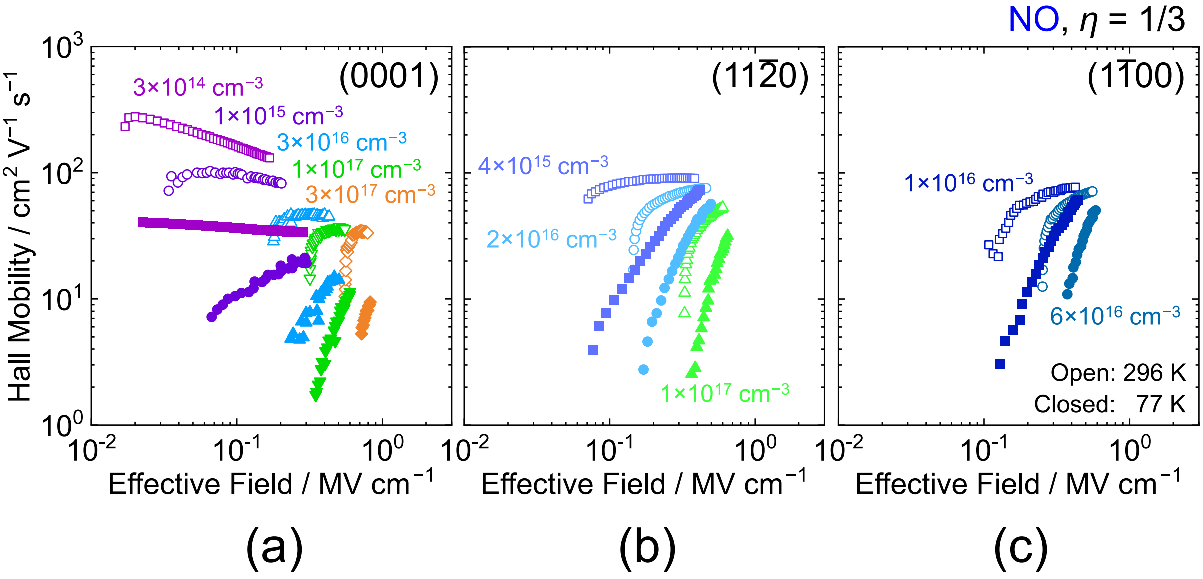

Figure 5.6: Effective normal field (E_{eff}) dependences of Hall mobility (μ_{Hall}) for NO-annealed SiC (a) (0001), (b) $(11\bar{2}0)$, and (c) $(1\bar{1}00)$ MOSFETs with various acceptor concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3\times10^{18}$ cm^{-3}, 4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1\times10^{17}$ cm^{-3}, and 1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3\times10^{17}$ cm^{-3}, respectively) of p-body. The open and closed symbols represent the results at 296 K and 77 K, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}.

for $(11\bar{2}0)$ and $N_\mathrm{A} = 1 \times 10^{16}$ cm^{-3} for $(1\bar{1}00)$] MOSFETs are used to calculate μ_free for all of the MOSFETs.

Figure 5.7 shows the effective normal field dependences of experimental μ_Hall and calculated μ_free for NO-annealed SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs with various N_A of p-body at 296 K. Here, the various symbols represent the experimental data. The calculated acoustic phonon-limited (ac), non-polar optical phonon-limited (nop), substrate impurities-limited (imp), and total (ac+nop+imp) mobilities are shown by dashed, dotted, dashed-dotted, and solid lines, respectively. The calculated μ_free is at least 4 times higher than the experimental μ_Hall regardless of surface orientation. Therefore, the other scattering processes should be considered to reproduce the experimental results for MOSFETs on non-polar faces.

Figure 5.8 shows the effective normal field dependences of experimental μ_Hall and calculated μ_free for NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs with various N_A of p-body at 296 K. Here, the symbols represent the experimental data. The calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. As for the fitting parameters, N_fix, $\varDelta_\mathrm{sr}$, and L_sr are 1.5×10^{13} cm^{-2}, 0.5 nm, 5.0 nm, respectively. In this chapter, the N_fix of MOSFETs on non-polar faces is set as 2 times higher than that of MOSFETs on (0001) in Chapter 4. In general, a nitrogen (N) concentration at NO-annealed SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO$_2$ interfaces is higher than that at NO-annealed SiC (0001)/SiO$_2$ ones [8]. Therefore, N_fix of MOSFETs on $(11\bar{2}0)$ and $(1\bar{1}00)$ should be set as higher than 7.5×10^{12} cm^{-2}. Consequently, the μ_Hall of MOSFETs on both $(11\bar{2}0)$ and $(1\bar{1}00)$ can be explained by strong Coulomb scattering due to fixed charges. In addition, the impact of surface roughness at SiC $(11\bar{2}0)$ and $(1\bar{1}00)$/SiO$_2$ interfaces must be smaller than that at SiC (0001)/SiO$_2$ ones because SiC $(11\bar{2}0)$ and $(1\bar{1}00)$ surfaces do not have an off angle of several degrees. Therefore, in the present study, the $\varDelta_\mathrm{sr}$ of MOSFETs on non-polar faces is set as 0.5 nm, 2 times lower than that of MOSFETs on (0001) in Chapter 4. However, the surface roughness-limited mobility is not strongly changed by increasing L_sr. Hence, the L_sr of MOSFETs on non-polar faces is assumed to be the same as (0001) in Chapter 4. As a result, the influences of Coulomb scattering due to trapped electrons and surface roughness scattering are very small (~ 1000 cm^2 V^{-1} s^{-1}) in this E_eff range.

In the above calculation, the trapped electrons are considered to be located at SiC/SiO$_2$ interfaces. Next, μ_free is calculated by considering a depth profile of trapped electrons in SiC. Figure 5.9 shows the experimental μ_Hall and μ_free calculated by considering a depth profile of trapped electrons in the range 0 nm $\leq z \leq$ 1 nm as a function of E_eff for NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs with various N_A of p-body at 296 K. The symbols and lines are the same meaning as those in Fig. 5.8. The μ_free at 296 K is not significantly varied by changing the distribution of trapped electron density because the μ_free is strongly limited by Coulomb scattering due to fixed charges rather than trapped electrons.

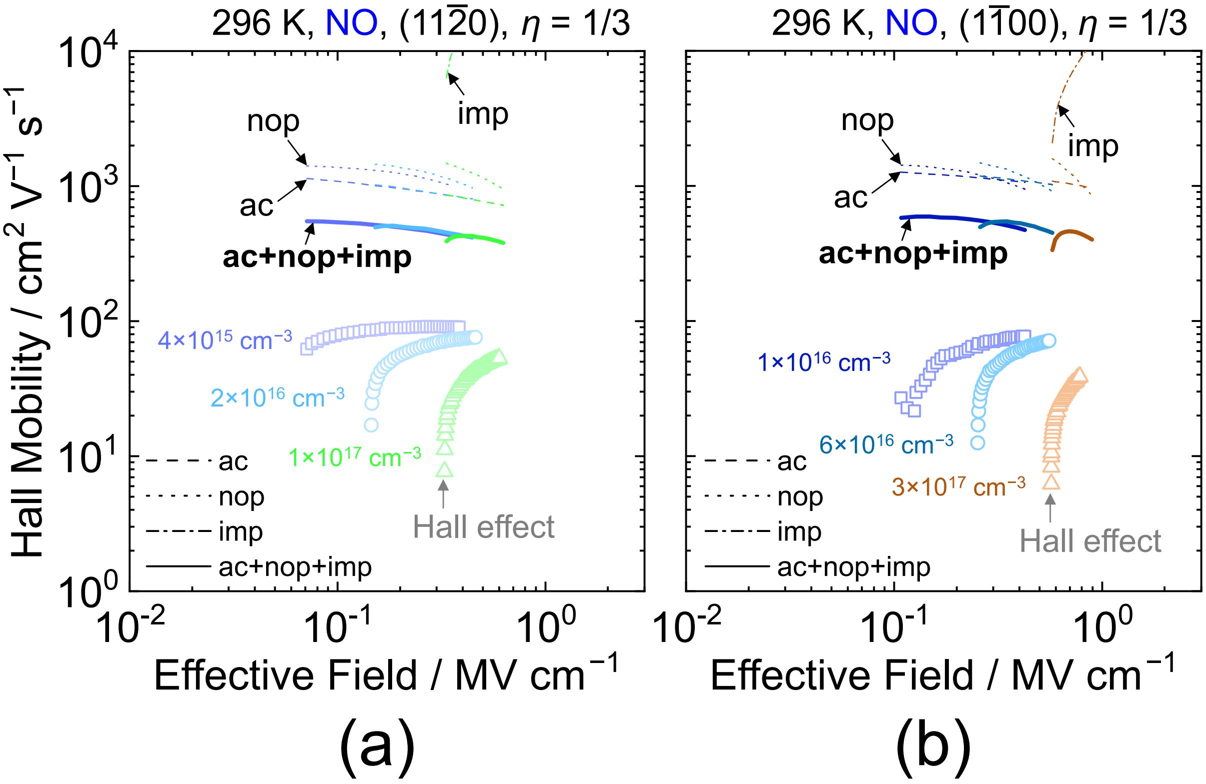

Figure 5.7: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for NO-annealed SiC (a) (11$\bar{2}$0) and (b) (1$\bar{1}$00) MOSFETs with various acceptor concentrations (4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{17}$ cm^{-3} and 1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}, respectively) of p-body at 296 K. Experimental results are represented by symbols. Calculated acoustic phonon-limited (ac), non-polar optical phonon-limited (nop), substrate impurities-limited (imp), and total (ac+nop+imp) mobilities are shown by dashed, dotted, dashed-dotted, and solid lines, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}.

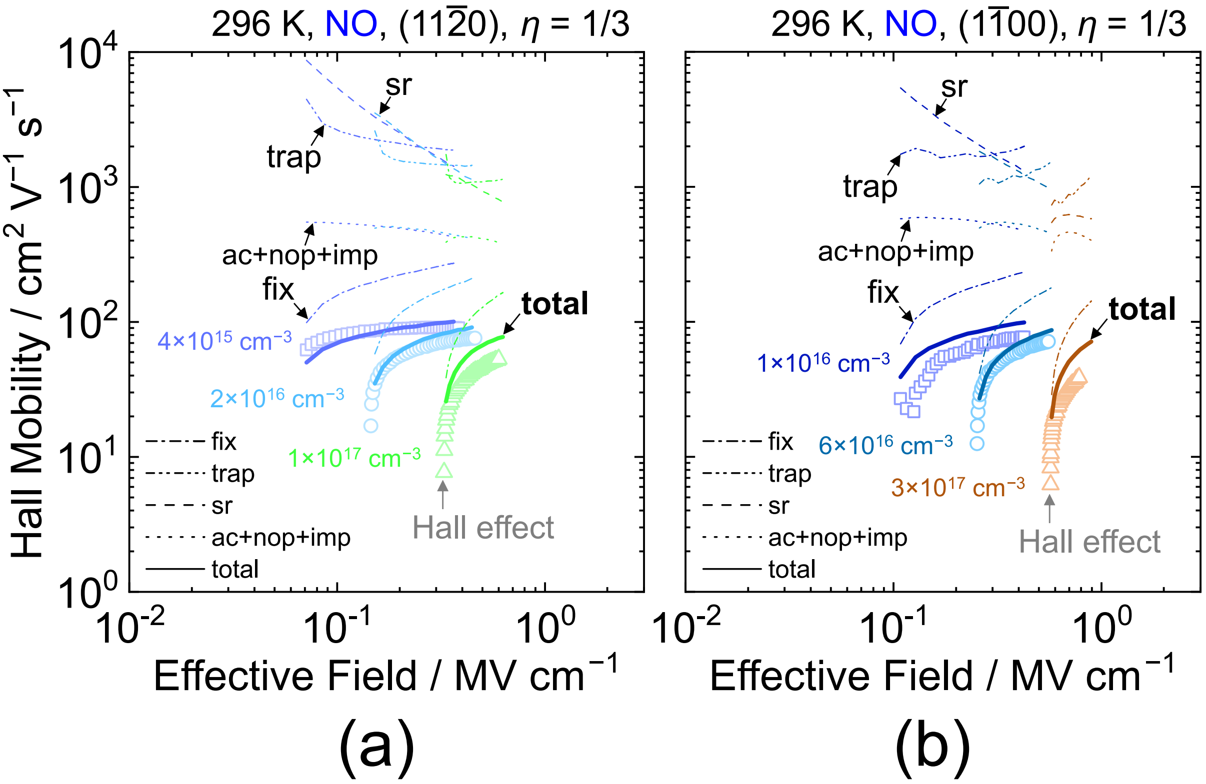

Figure 5.8: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for NO-annealed SiC (a) (11$\bar{2}$0) and (b) (1$\bar{1}$00) MOSFETs with various acceptor concentrations (4×10^{15} cm^{-3} $\leq N_{\text{A}} \leq$ 1×10^{17} cm^{-3} and 1×10^{16} cm^{-3} $\leq N_{\text{A}} \leq$ 3×10^{17} cm^{-3}, respectively) of p-body at 296 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height ($\varDelta_{\text{sr}}$), and surface roughness correlation length (L_{sr}) are 1.5×10^{13} cm^{-2}, 0.5 nm, and 5.0 nm, respectively.

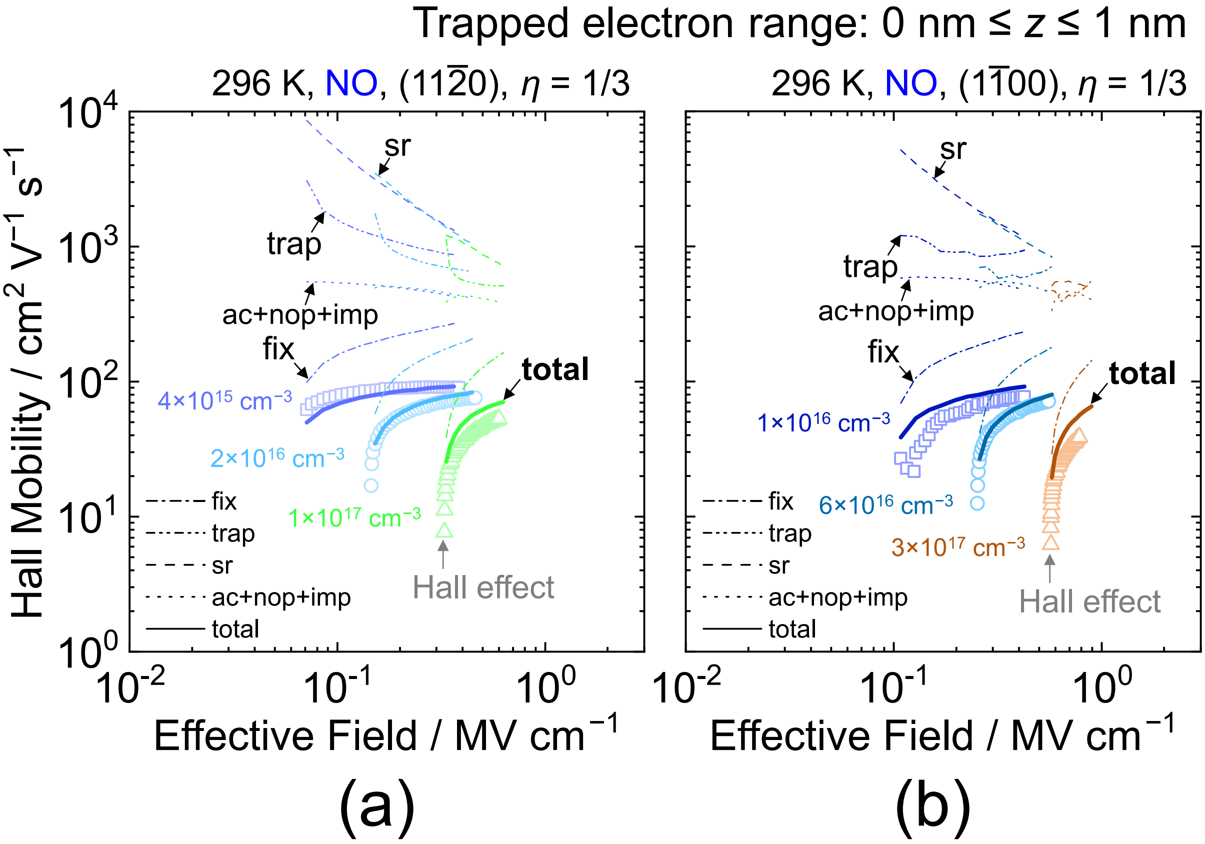

Figure 5.9: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for NO-annealed SiC (a) (11$\bar{2}$0) and (b) (1$\bar{1}$00) MOSFETs with various acceptor concentrations (4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{17}$ cm^{-3} and 1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}, respectively) of p-body at 296 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. In the calculation, the trapped electron density distribution is considered to be a box profile in the range 0 nm $\leq z \leq$ 1 nm. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height (Δ_{sr}), and surface roughness correlation length (L_{sr}) are 1.5×10^{13} cm^{-2}, 0.5 nm, and 5.0 nm, respectively.

Besides, μ_{free} at 77 K calculated by considering a depth profile of trapped electrons ($0\ \mathrm{nm} \leq z \leq 1\ \mathrm{nm}$) and experimental μ_{Hall} at 77 K in Fig. 5.6 are shown in Fig. 5.10. In the calculation, n_{free} and n_{trap} at 296 K are used, which is a large assumption. The symbols and lines are the same meaning as those in Fig. 5.8. In Fig. 5.10, the calculated μ_{free} is overestimated compared to the experimental μ_{Hall} because the expected depth profile and density of trapped electrons are probably different from the true ones, as already mentioned in Chapter 4.

5.5 Discussion

The relationship between n_{trap} and μ_{Hall} is summarized in the following discussion. Figure 5.11 shows the n_{trap} as a function of n_{free} for lightly-doped MOSFETs annealed in NO or $\mathrm{POCl_3}$ on various crystal faces. The blue, orange, green, and red symbols represent the results of NO-annealed ($N_{\mathrm{A}} = 3 \times 10^{14}\ \mathrm{cm^{-3}}$) (0001), ($N_{\mathrm{A}} = 4 \times 10^{15}\ \mathrm{cm^{-3}}$) ($11\bar{2}0$), ($N_{\mathrm{A}} = 1 \times 10^{16}\ \mathrm{cm^{-3}}$) ($1\bar{1}00$), and $\mathrm{POCl_3}$-annealed ($N_{\mathrm{A}} = 3 \times 10^{14}\ \mathrm{cm^{-3}}$) (0001) MOSFETs, respectively. The n_{trap} of NO-annealed MOSFETs on non-polar faces is 1.8 times higher than that of $\mathrm{POCl_3}$-annealed (0001) MOSFETs and is 3.9 times lower than that of NO-annealed ones. Note that the n_{trap} quantified at 296 K is used in the following discussion.

Next, the effective normal field dependences of μ_{Hall} for MOSFETs annealed in NO or $\mathrm{POCl_3}$ on various crystal faces at 296 K and 77 K are shown in Fig. 5.12. In these figures, the μ_{Hall} is extracted from MOSFETs with various N_{A} of p-body when the n_{free} is $2.5 \times 10^{12}\ \mathrm{cm^{-2}}$. In Fig. 5.12(a), the μ_{Hall} of NO-annealed MOSFETs on non-polar faces is 1.5 times higher than that of NO-annealed (0001) MOSFETs and 1.4 times lower than that of $\mathrm{POCl_3}$-annealed ones. This result implies that the effective mass dependence of μ_{Hall} is smaller than the n_{trap} dependence of μ_{Hall}. In contrast, the difference in μ_{Hall} among the MOSFETs is apparent at 77 K as shown in Fig. 5.12(b). In Fig. 5.12(b), the μ_{Hall} of NO-annealed MOSFETs on non-polar faces is 3.0 times higher than that of NO-annealed (0001) MOSFETs and is 1.6 times lower than that of $\mathrm{POCl_3}$-annealed ones. To discuss the mobility degradation due to lowering the temperature, the ratio of μ_{Hall} at 77 K [μ_{Hall}(77 K)] to that at RT [μ_{Hall}(296 K)] is extracted in Fig. 5.13.

Figure 5.13 shows the μ_{Hall}(77 K)/μ_{Hall}(296 K) for MOSFETs annealed in NO or $\mathrm{POCl_3}$ on various crystal faces. The symbols represent the data averaged among the MOSFETs with various N_{A} of p-body, and the error bars show the fluctuation of the data. The μ_{Hall}(77 K)/μ_{Hall}(296 K) of $\mathrm{POCl_3}$-annealed (0001) MOSFETs is around 40%. Thus, the μ_{Hall} is decreased by lowering the temperature even though MOSFETs annealed in $\mathrm{POCl_3}$, which can substantially reduce n_{trap}. Besides, the μ_{Hall}(77 K)/μ_{Hall}(296 K) of NO-annealed MOSFETs on non-polar faces is around 32%. Moreover, the ratio of NO-annealed (0001) MOSFETs is around 19%. Therefore, MOSFETs with higher n_{trap} tend to show lower μ_{Hall}

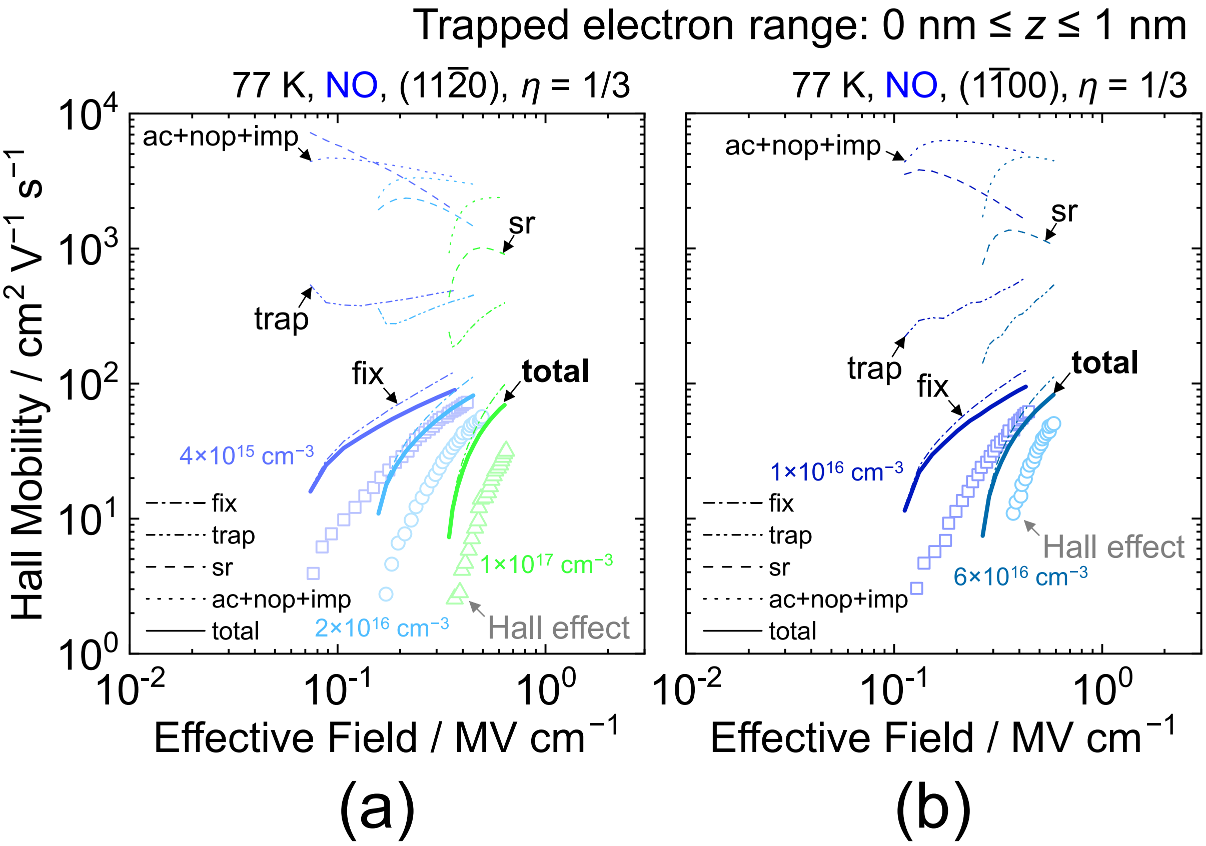

Figure 5.10: Effective normal field (E_{eff}) dependences of experimental Hall mobility (μ_{Hall}) and calculated free electron mobility (μ_{free}) for NO-annealed SiC (a) (11$\bar{2}$0) and (b) (1$\bar{1}$00) MOSFETs with various acceptor concentrations (4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{17}$ cm^{-3} and 1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}, respectively) of p-body at 77 K. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. In the calculation, the trapped electron density distribution is considered to be a box profile in the range 0 nm $\leq z \leq$ 1 nm. Here, η ($= 1/3$) is a parameter that indicates how much the electrons contribute to the E_{eff}. The fixed charge density (N_{fix}), surface roughness height (Δ_{sr}), and surface roughness correlation length (L_{sr}) are 1.5×10^{13} cm^{-2}, 0.5 nm, and 5.0 nm, respectively.

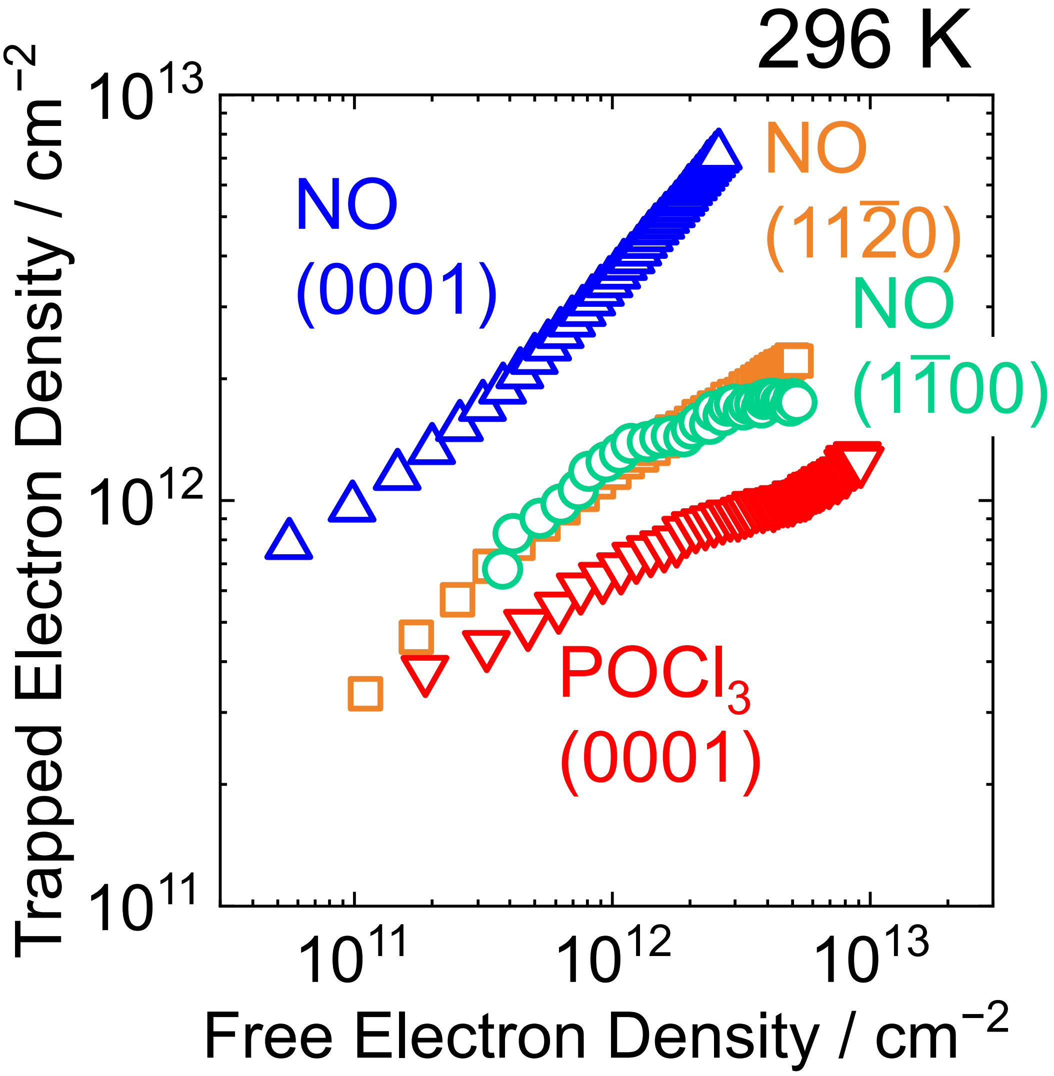

Figure 5.11: Trapped electron density as a function of the free electron density for lightly-doped SiC MOSFETs annealed in NO or POCl$_3$ on various crystal faces. The blue, orange, green, and red symbols represent the results of NO-annealed ($N_\mathrm{A} = 3 \times 10^{14}$ cm^{-3}) (0001), ($N_\mathrm{A} = 4 \times 10^{15}$ cm^{-3}) (11$\bar{2}$0), ($N_\mathrm{A} = 1 \times 10^{16}$ cm^{-3}) (1$\bar{1}$00), and POCl$_3$-annealed ($N_\mathrm{A} = 3 \times 10^{14}$ cm^{-3}) (0001) MOSFETs, respectively.

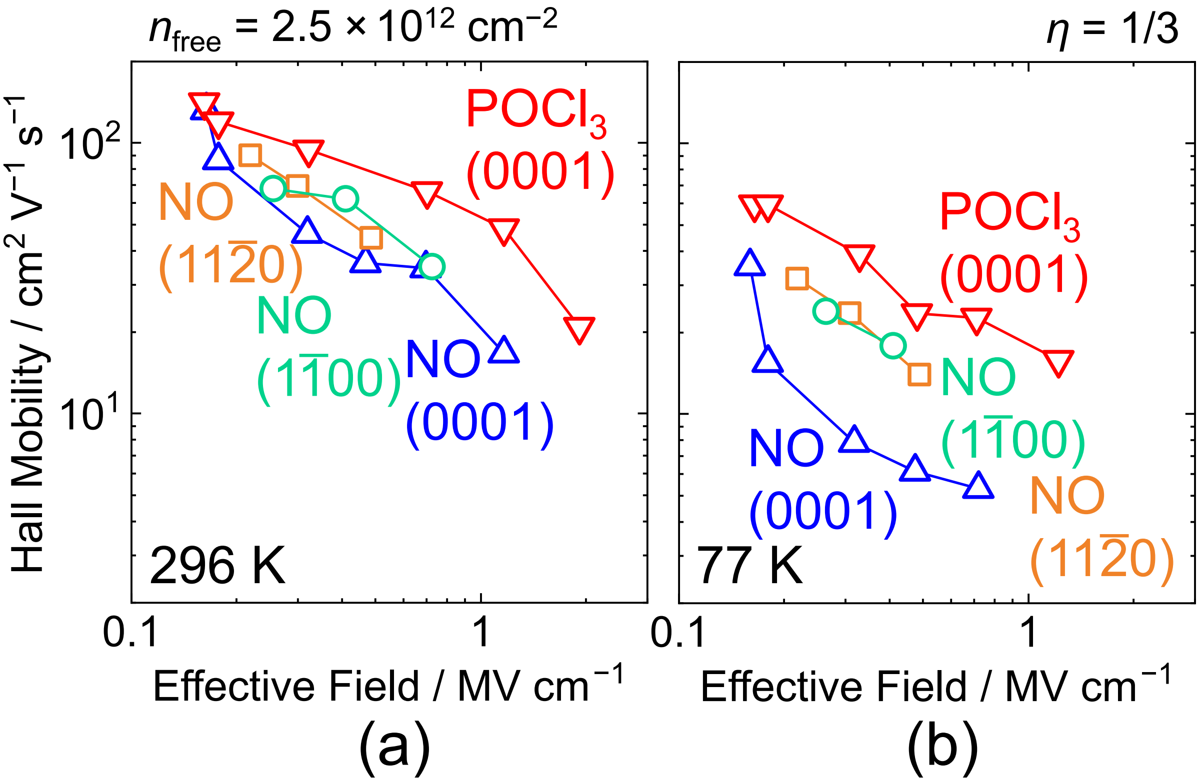

Figure 5.12: Effective normal field (E_{eff}) dependences of Hall mobility (μ_{Hall}) for SiC MOSFETs annealed in NO or POCl$_3$ on various crystal faces with various acceptor concentrations (N_{A}) of p-body at (a) 296 K and (b) 77 K when the free electron density (n_{free}) is 2.5×10^{12} cm^{-2}. The blue, orange, green, and red symbols represent the results of NO-annealed (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{18}$ cm^{-3}) (0001), (4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{17}$ cm^{-3}) (11$\bar{2}$0), (1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}) (1$\bar{1}$00), and POCl$_3$-annealed (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) (0001) MOSFETs, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the E_{eff}.

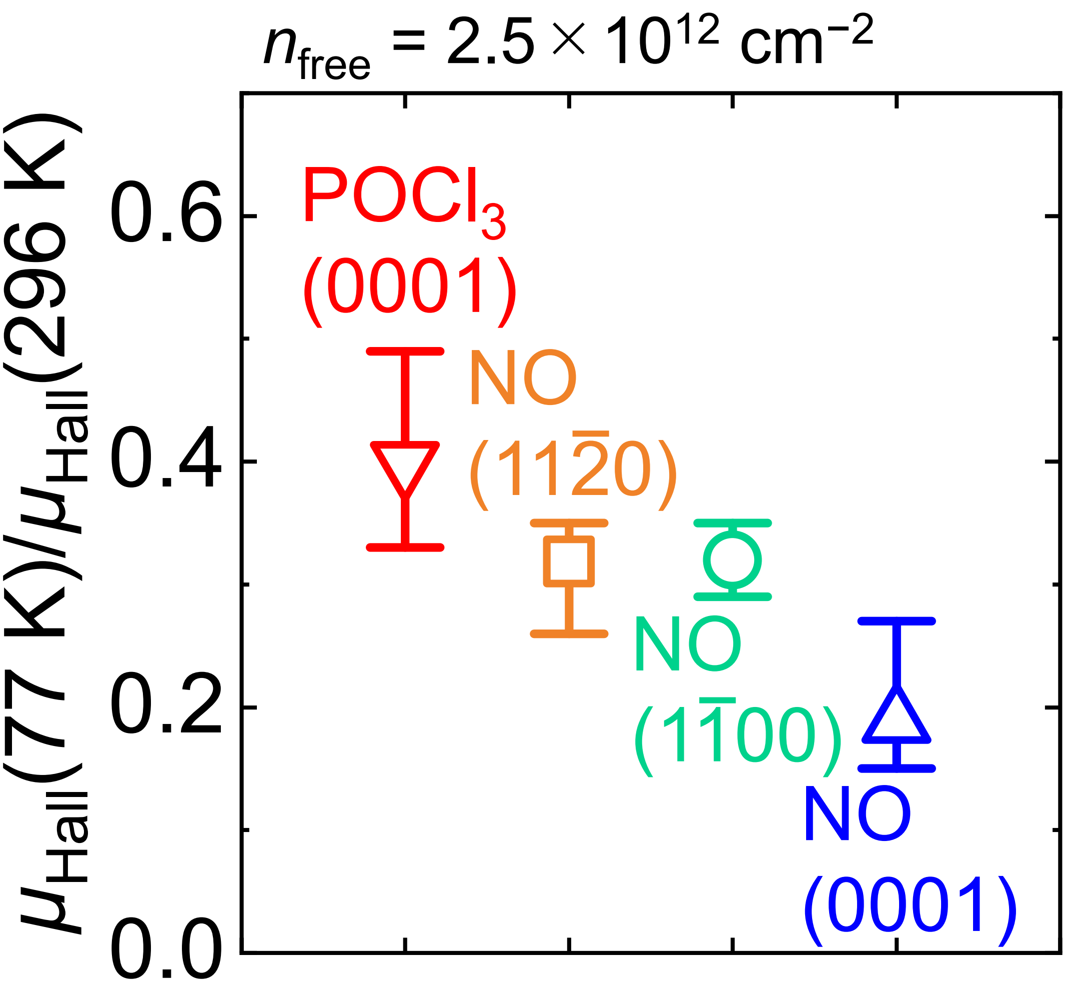

Figure 5.13: The ratio of Hall mobility (μ_{Hall}) at 77 K to that at 296 K for SiC MOSFETs annealed in NO or POCl$_3$ on various crystal faces with various acceptor concentrations (N_{A}) of p-body when the free electron density (n_{free}) is 2.5×10^{12} cm^{-2}. The blue, orange, green, and red symbols represent the results of NO-annealed (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{18}$ cm^{-3}) (0001), (4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 1 \times 10^{17}$ cm^{-3}) (11$\bar{2}$0), (1×10^{16} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}) (1$\bar{1}$00), and POCl$_3$-annealed (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) (0001) MOSFETs, respectively. The symbols and error bars are determined by the average and variation of the data among the MOSFETs with various p-bodies, respectively.

at 77 K compared to that at RT.

To discuss the n_{trap} dependence of μ_{Hall}, the μ_{Hall} at E_{eff} of 0.3 MV cm^{-1} and 0.4 MV cm^{-1} is extracted by adopting linear interpolation. Figure 5.14 shows the trapped electron density dependences of μ_{Hall} when the E_{eff} is 0.3 MV cm^{-1} and 0.4 MV cm^{-1} at 296 K and 77 K. The blue, orange, green, and red symbols represent the results of NO-annealed (0001), (11$\bar{2}$0), (1$\bar{1}$00), and POCl$_3$-annealed (0001) MOSFETs, respectively. The open and closed symbols represent the results at the E_{eff} of 0.3 MV cm^{-1} and 0.4 MV cm^{-1}, respectively. As can be seen, the μ_{Hall} has a negative correlation with n_{trap} at both RT and 77 K. In Fig. 5.14(a), the μ_{Hall}–E_{eff} slope is in the range -0.35–-0.28. On the other hand, the μ_{Hall}–E_{eff} slope is in the range -0.74–-0.72 at 77 K as shown in Fig. 5.14(b). This result indicates that the μ_{Hall} at low temperatures is significantly affected by n_{trap}.

5.6 Summary

In summary, μ_{Hall} of NO-annealed MOSFETs on non-polar faces with various acceptor concentrations (4×10^{15} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{17}$ cm^{-3}) of p-body at RT and 77 K is investigated in this chapter. The n_{trap} of NO-annealed (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs is 1.8 times higher than that of POCl$_3$-annealed (0001) ones and is 3.9 times lower than that of NO-annealed (0001) ones at n_{free} of 2.0×10^{12} cm^{-2}. The D_{it} near E_{C}(2D-DOS) extracted from the MOS-Hall effect measurements on the NO-annealed (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs is much lower than that of (0001) ones ($D_{\mathrm{it}} \sim 10^{13}$ cm^{-2} eV^{-1} in the wide energy range 0.0 eV $\leq E_{\mathrm{C}}(\text{2D-DOS}) - E_{\mathrm{T}} \leq$ 0.2 eV). As a result, the μ_{Hall} of NO-annealed MOSFETs on non-polar faces is 1.5 times higher than that of NO-annealed (0001) ones and 1.4 times lower than that of POCl$_3$-annealed ones. At 77 K, the μ_{Hall} of NO-annealed MOSFETs on (0001) substantially decreases compared to MOSFETs on non-polar faces. The μ_{Hall} of NO-annealed MOSFETs on non-polar faces is 3.0 times higher than that of MOSFETs on (0001) at 77 K. Based on the theoretical calculation, the μ_{Hall} of NO-annealed MOSFETs on non-polar faces is limited by Coulomb scattering due to fixed charges. The influence of Coulomb scattering due to fixed charges is more significant than those of Coulomb scattering due to trapped electrons and surface roughness scattering.

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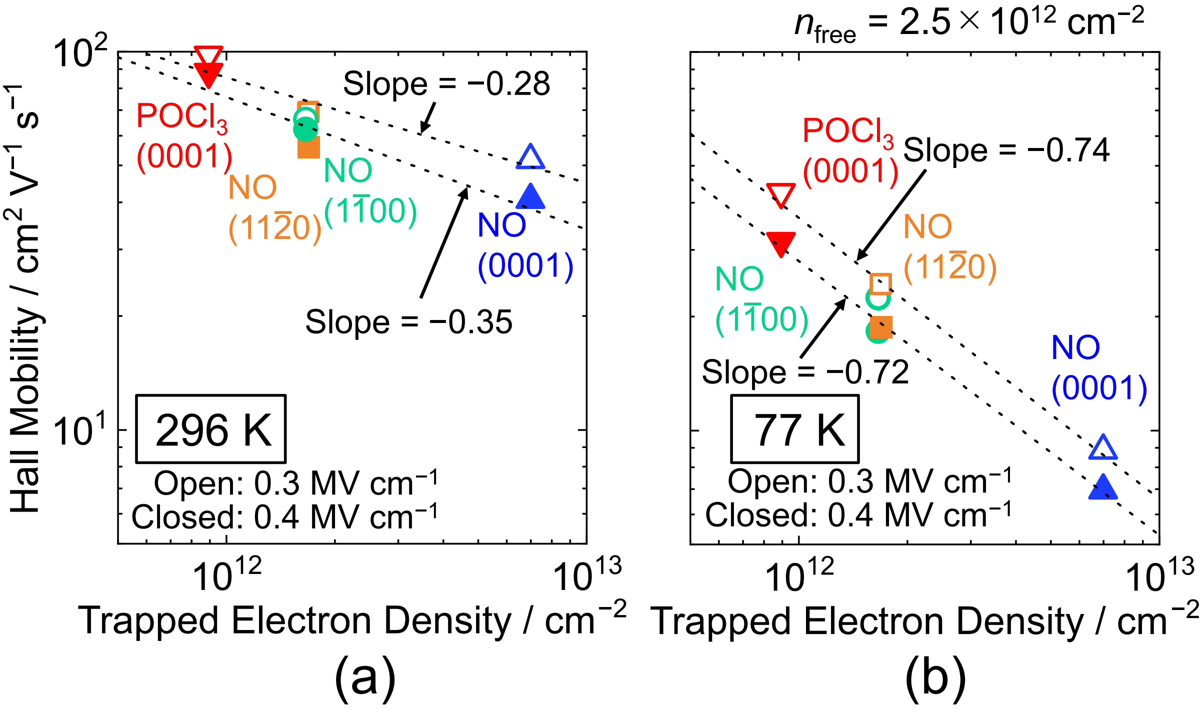

Figure 5.14: Trapped electron density (n_{trap}) dependences of Hall mobility (μ_{Hall}) at (a) 296 K and (b) 77 K when the free electron density (n_{free}) is 2.5×10^{12} cm^{-2}. The blue, orange, green, and red symbols represent the results of NO-annealed (0001), (11$\bar{2}$0), (1$\bar{1}$00), and POCl$_3$-annealed (0001) MOSFETs, respectively. The open and closed symbols are the results at the effective normal field (E_{eff}) of 0.3 MV cm^{-1} and 0.4 MV cm^{-1}, respectively.

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Chapter 6

Conclusions

6.1 Conclusions

In the present study, to predict SiC MOSFET characteristics, the author investigated the impact of the p-body doping concentration of MOSFETs on the electron trapping effect, discussed the effective channel mobility of phosphoryl chloride ($POCl_3$)-annealed MOSFETs, and analyzed Hall mobility in SiC MOSFETs with various surface orientation by combining numerical calculations. The major conclusions obtained in this study are summarized as follows.

In Chapter 2, the author extracted interface state density (D_{it}) near the conduction band edge (E_{C}) from gate characteristics of as-oxidized and nitric oxide (NO)-annealed SiC (0001) MOSFETs with various acceptor concentration (N_{A}) of p-body at room temperature (RT). The D_{it} plotted with respect to the conventional E_{C} (i.e., the bottom edge of the three-dimensional density of states) showed strange results that D_{it} at a given energy decreased when N_{A} increased. On the other hand, D_{it} plotted with respect to the bottom edge of the two-dimensional density of states was uniquely determined by the gate oxide formation process and independent of N_{A} of p-body. In addition, the author found that the interface states may be generated in the SiC side because the energy of interface states followed the conduction band edge of SiC. This result implies that the effective channel mobility (μ_{eff}) of heavily-doped MOSFETs is not affected by D_{it} at higher energy and that the ratio of free electrons to total electrons ($n_{\mathrm{free}}/n_{\mathrm{total}}$) does not decrease in heavily-doped MOSFETs. Based on the above results, the μ_{eff} degradation in heavily-doped MOSFETs is caused by electron scattering rather than electron trapping.

In Chapter 3, to clarify the scattering mechanism in SiC (0001) MOSFETs, the author focused on $POCl_3$-annealed MOSFETs to obtain extremely low D_{it}. In this chapter, μ_{eff} of $POCl_3$-annealed SiC (0001) MOSFETs with various N_{A} of p-body was extracted, and the scattering mechanism was briefly discussed. $POCl_3$-annealed MOSFETs with high-purity semi-insulating (HPSI) substrates were also prepared. From MOS-Hall effect measurement results, the electron trapping effect in $POCl_3$-annealed MOSFETs is extremely small in the on-state of MOSFETs because the free electron density (n_{free})–gate-source voltage (V_{GS}) slope was nearly equal to the ideal one. In addition, the author compared the field-effect mobility (μ_{FE}) of POCl$_3$-annealed MOSFETs to that of NO-annealed ones. As a result, μ_{FE} of POCl$_3$-annealed MOSFETs was 3.7 times higher than that of NO-annealed MOSFETs in the case of heavily-doped ($N_{\mathrm{A}} = 3 \times 10^{17}$ cm^{-3}) MOSFETs. In addition, the author also focused on the difference in the subthreshold slope (SS) of MOSFETs annealed in between NO and POCl$_3$. The SS of POCl$_3$-annealed MOSFETs was lower in the wide N_{A} range 3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}. Based on the obtained results, the μ_{eff} was assumed to be free electron mobility (μ_{free}). The μ_{eff} of POCl$_3$-annealed MOSFETs can be discussed for electron scattering mechanism. As a result, the μ_{eff} extracted from MOSFETs annealed in POCl$_3$ fabricated on HPSI substrates was higher than the phonon-limited mobility reported in the previous study on Hall mobility (μ_{Hall}) of NO-annealed MOSFETs, which can be interpreted that the influence of Coulomb scattering due to trapped electrons remains in the NO-annealed MOSFETs. In addition, a body bias technique was adopted to clarify the mobility degradation under a high effective normal field (E_{eff}). Then, the author demonstrated that the abnormal mobility drop occurs even after POCl$_3$ annealing. From the results of μ_{eff}–E_{eff} slope, the author suggested that strong surface roughness scattering is dominant in the high-E_{eff} region (1.0 MV cm^{-1} $\leq E_{\mathrm{eff}} \leq$ 2.0 MV cm^{-1}).

In Chapter 4, μ_{Hall} of SiC (0001) MOSFETs without POA, annealed in NO, and annealed in POCl$_3$ with various p-body doping concentrations (3×10^{14} cm^{-3} $\leq N_{\mathrm{A}} \leq 3 \times 10^{18}$ cm^{-3}) was extensively investigated. The n_{free} and the total electron density (n_{total}) were obtained from MOS-Hall effect and split gate-channel capacitance (C_{GC})–V_{GS} measurements, and D_{it} near E_{C} was obtained from MOSFETs with various N_{A}. The trapped electron density (n_{trap}) of POCl$_3$-annealed MOSFETs was much lower compared to the other MOSFETs (at least, $< 10^{12}$ cm^{-2}). The D_{it} near E_{C} does not depend on N_{A} even if D_{it} is extracted by Hall effect measurements, being consistent with the results in Chapter 2. The μ_{Hall} of MOSFETs annealed in POCl$_3$ was higher than that of MOSFETs annealed in NO and exceeded the phonon-limited mobility reported in the previous study. In addition, the μ_{Hall} at 77 K was much lower than that at RT, regardless of interface treatment. Moreover, the μ_{Hall} of NO-annealed MOSFETs was significantly decreased by lowering the temperature. Furthermore, theoretical μ_{free} was calculated to understand the electron scattering mechanism in SiC (0001) MOSFETs. The author demonstrated that the difference in μ_{Hall} of MOSFETs annealed in between NO and POCl$_3$ is explained by the influence of Coulomb scattering by trapped electrons. Consequently, the author suggested that the μ_{Hall} of SiC MOSFETs annealed in NO is limited by Coulomb scattering due to interface fixed charges and trapped electrons and surface roughness scattering. The obtained interface fixed charge density (N_{fix}), surface roughness height ($\mathit{\Delta}_{\mathrm{sr}}$), and surface roughness correlation length (L_{sr}) were 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

In Chapter 5, μ_{Hall} of SiC (11$\bar{2}$0) and (1$\bar{1}$00) MOSFETs annealed in NO with various N_{A} of p-body was investigated. The author focused on the n_{trap} of MOSFETs with various surface orientations and interface treatments. The n_{trap} of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs was 3.9 times lower than that of NO-annealed (0001) MOSFETs and was 1.8 times higher than that of $\mathrm{POCl_3}$-annealed (0001) MOSFETs. On the other hand, the μ_{Hall} of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs was 1.5 times higher than that of NO-annealed (0001) MOSFETs and was 1.4 times lower than that of $\mathrm{POCl_3}$-annealed (0001) MOSFETs. In particular, the $\mu_{\mathrm{Hall}}(77\mathrm{K})/\mu_{\mathrm{Hall}}(296\mathrm{K})$ of NO-annealed (0001) MOSFETs (the highest n_{trap}) was the lowest ($\sim$ 19%). This result implies that the electrons trapped at the interface states severely affect μ_{free}. Furthermore, the μ_{Hall} of NO-annealed $(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs could be explained by strong Coulomb scattering due to fixed charges ($N_{\mathrm{fix}} = 1.5 \times 10^{13}$ cm^{-2}).

6.2 Future Outlook

The author investigated the electron transport mechanism in SiC MOSFETs from various aspects in this thesis. However, several issues remain to be solved as follows.

- **MOS-Hall effect measurements at high temperatures**
  In the present study, the author focused on μ_{Hall} at RT and 77 K. Thus, the information on μ_{Hall} at high temperatures is unknown at the present stage. The μ_{Hall} at high temperatures is also important for separating the scattering processes. It can be inferred that the influence of strong Coulomb scattering is suppressed at high temperatures. In contrast, phonon scattering is dominant at high temperatures. In fact, Ref. 1 reported that the μ_{Hall} of $\mathrm{POCl_3}$-annealed MOSFETs is close to that of NO-annealed MOSFETs at 473 K.

- **Elucidation of the origin of the interface fixed charges**
  As described in Chapters 4 and 5, Coulomb scattering due to interface fixed charge is probably dominant. The N_{fix} is as high as 0.75–1.5 × 10^{13} cm^{-2}, which is even higher compared to the surface electron density ($\sim$ 10^{12}–10^{13} cm^{-2}). As a result, μ_{Hall} is decreased by lowering the temperature due to the strong Coulomb scattering. After increasing $n_{\mathrm{free}}/n_{\mathrm{total}}$ by finding a new technique of reducing D_{it}, the abnormally high density of interface charges should be reduced to improve μ_{free} itself. Recently, for instance, oxidation-minimizing processes [2–5] have been investigated. The μ_{Hall} of these interface-treated MOSFETs should be extensively discussed to understand the behavior of interface fixed charges.

- **Understanding of hole scattering mechanism in SiC/SiO$_2$ inversion layers**
  For SiC power MOSFET applications, the electron scattering mechanism in n-channel MOSFETs has been mainly focused. SiC MOSFETs can also be used for complementary MOS (CMOS) at high temperatures owing to its wide bandgap (i.e., low intrinsic carrier concentration). For SiC CMOS applications, modeling of both n- and p-channel

MOSFETs is important. However, few studies reported p-channel MOSFET characteristics. Recently, Ref. 6 reported that the mobility degradation in the high-E_{eff} region for NO-annealed p-channel MOSFETs is smaller than that for NO-annealed n-channel MOSFETs. Thus, from the perspective of the present study, either trapped electron density or interface fixed charge density in NO-annealed p-channel MOSFETs is likely smaller than that of NO-annealed n-channel MOSFETs.

- **Modeling of free electron mobility in a wide temperature range**
  The μ_{free} calculated by the present model could not reproduce the μ_{Hall} at low temperatures. The calculated μ_{free} of MOSFETs with higher n_{trap} at 77 K tends to be overestimated compared to μ_{Hall}. Therefore, the present model of Coulomb scattering by trapped electrons is probably underestimated. In order to predict the electron scattering in a wide temperature range, the impact of trapped electrons on μ_{Hall} should be clarified. Ref. 7 reported that the μ_{Hall} degradation can be explained by considering neutral defect scattering. Recently, Ref. 8 reported that dipole scattering is a possible candidate for the dominant mobility-limiting factors. The other scattering reported in the previous studies, which is considered to be peculiar to SiC MOS systems, should also be discussed in detail.

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Appendix A

Theory of Electronic States and Mobility in Inversion Layers

A.1 Wave Functions and Energies of Electrons in Sub-Bands

Information on electronic states in a MOS inversion layer is essential to discuss the possible origin of mobility-limiting factors in MOSFETs [1, 2]. For example, the Fermi level (E_{F}) at the MOS interface is determined by the free electron density (n_{free}). In calculating theoretical mobility, the wave functions (ξ_m) and energies of electrons in sub-bands (E_m) are also needed. Here, m is the number of sub-bands ($m = 0, 1, 2, \cdots$).

In the present study, energy (E)–wave vector (k) dispersion is calculated by assuming effective mass approximation and considering the lowest and second lowest conduction band valleys in 4H-SiC. The conduction band edge of the second lowest valley is higher than that of the lowest valley by 0.12 eV. The E is given by [1]

$$E = \frac{\hbar^2 k_x^2}{2m_x} + \frac{\hbar^2 k_y^2}{2m_y} + E_m = \frac{\hbar^2 (k_x'^2 + k_y'^2)}{2m_{\mathrm{avg}}} + E_m, \tag{A.1}$$

where $\hbar$ is the Dirac constant, which is obtained from dividing Plank constant ($h = 6.62607015 \times 10^{-34}$ J s) by 2π (i.e., $\hbar = h/2\pi$). Here, k_x and k_y satisfy the following equation [2]: $\hbar^2 k_x^2/2m_x = \hbar^2 k_y^2/2m_y = [E - E_{\mathrm{C}}(\text{2D-DOS})]/2$. The x and y directions are parallel to the MOS interface, and the z direction is perpendicular to the MOS interface. The m_{avg} is defined as $m_{\mathrm{avg}} = 2/(1/m_x + 1/m_y)$. For simplicity, the k_x' and k_y' are defined as $k_x' = k_x \times \sqrt{m_{\mathrm{avg}}/m_x}$ and $k_y' = k_y \times \sqrt{m_{\mathrm{avg}}/m_y}$, respectively. In Table A.1, the effective masses for various surface orientations are summarized [3, 4]. In the calculation, the surface orientation dependence of conduction band valleys should also be considered [5–7].

In general, ξ_m and E_m can be obtained by solving Schrödinger equation as [4, 5, 8]

$$\left[-\frac{\hbar^2}{2m_z}\frac{\mathrm{d}^2}{\mathrm{d}z^2} - e\phi(z)\right]\xi_m(z) = E_m \xi_m(z), \tag{A.2}$$

where z is the distance from the MOS interface to SiC, e is the elementary charge ($e = 1.602176634 \times 10^{-19}$ C), and $\phi(z)$ is the potential distribution of SiC. The $\phi(z)$ can be obtained by solving Poisson's equation as [4, 5, 8]

$$\frac{\mathrm{d}^2\phi(z)}{\mathrm{d}z^2} = -\frac{\rho_{\mathrm{depl}}(z) - e\sum\limits_{m=0}^{\infty} n_m |\xi_m(z)|^2}{\kappa_{\mathrm{SiC}}\varepsilon_0}, \tag{A.3}$$

where $\rho_{\mathrm{depl}}(z)$ is the depletion charge density, n_m is the electron density of mth sub-band, κ_{SiC} is the relative permittivity of SiC [c-axis ($c_{\parallel}$): 10.32, perpendicular to c-axis ($c_{\perp}$): 9.76] [9], and ε_0 is the permittivity of vacuum ($\varepsilon_0 = 8.8541878128 \cdots \times 10^{-12}$ F m^{-1}). The $\rho_{\mathrm{depl}}(z)$ is given by [4, 5, 8]

$$\rho_{\mathrm{depl}}(z) = \begin{cases} -e(N_{\mathrm{A}} - N_{\mathrm{D}}) & (0 \leq z \leq z_{\mathrm{depl}}) \\ 0 & (z_{\mathrm{depl}} < z), \end{cases} \tag{A.4}$$

where N_{A} and N_{D} are the acceptor and donor concentrations, respectively, and z_{depl} is the depletion layer width of SiC. The z_{depl} and the depletion charge density (N_{depl}) are given by [4, 5, 8]

$$z_{\mathrm{depl}} = \sqrt{\frac{2\kappa_{\mathrm{SiC}}\varepsilon_0(\psi_{\mathrm{S}} - V_{\mathrm{BS}})}{e(N_{\mathrm{A}} - N_{\mathrm{D}})}}, \tag{A.5}$$

$$N_{\mathrm{depl}} = (N_{\mathrm{A}} - N_{\mathrm{D}})\, z_{\mathrm{depl}}, \tag{A.6}$$

where ψ_{S} is the surface potential and V_{BS} is the body-source voltage. The ψ_{S} is obtained by [4, 5, 8]

$$\psi_{\mathrm{S}} = \frac{(E_{\mathrm{C}} - E_{\mathrm{F}})_{\mathrm{bulk}} + E_{\mathrm{F}}}{e} - \frac{e n_{\mathrm{free}} z_{\mathrm{avg}}}{\kappa_{\mathrm{SiC}}\varepsilon_0}, \tag{A.7}$$

where z_{avg} is the average distance of electrons from the MOS interface. Here, z_{avg} is calculated by [4, 5, 8]

$$z_{\mathrm{avg}} = \frac{1}{n_{\mathrm{free}}}\sum_m n_m z_m, \tag{A.8}$$

$$z_m = \frac{\int_0^{\infty} z|\xi_m(z)|^2 \,\mathrm{d}z}{\int_0^{\infty} |\xi_m(z)|^2 \,\mathrm{d}z}, \tag{A.9}$$

where z_m is the average distance of electrons in the mth sub-band from the MOS interface. The n_m satisfies the following equations [4, 5, 8]:

$$n_m = \frac{n_v m_{\mathrm{d}} k_{\mathrm{B}} T}{\pi\hbar^2} \ln\left[1 + \exp\left(\frac{E_{\mathrm{F}} - E_m}{k_{\mathrm{B}}T}\right)\right], \tag{A.10}$$

$$n_{\mathrm{free}} = \sum_{m=0}^{\infty} n_m, \tag{A.11}$$

where n_v is the number of equivalent valley, m_{d} is the density-of-states effective mass, which is expressed as $m_{\mathrm{d}} = \sqrt{m_x m_y}$, k_{B} is the Boltzmann constant ($k_{\mathrm{B}} = 1.380649 \times 10^{-23}$ J K^{-1}), and T is the absolute temperature. In the calculation procedure, Schrödinger and Poisson's equations are solved self-consistently [4, 8].

Table A.1: Effective masses for various surface orientations [3, 4]. Note that the degeneracy factor of the conduction band valleys of non-polar faces is different from that of polar faces. m_e is the electron mass ($m_\mathrm{e} = 9.1093837015 \cdots \times 10^{-31}$ kg).

Surface	$\{0001\}$	$\{11\bar{2}0\}$		$\{1\bar{1}00\}$	
Valleys	All	Lower	Higher	Lower	Higher
1st Conduction Band	3	2	1	1	2
Longitudinal Mass m_x / m_e	0.28	0.31	0.31	0.31	0.31
Longitudinal Mass m_y / m_e	0.57	0.35	0.57	0.28	0.50
Normal Mass m_z / m_e	0.31	0.45	0.28	0.57	0.32
Conductivity Mass m_avg / m_e	0.38	0.33	0.40	0.29	0.38
Density-of-States Mass m_d / m_e	0.40	0.33	0.42	0.29	0.39
2nd Conduction Band	3	2	1	1	2
Longitudinal Mass m_x / m_e	0.16	0.71	0.71	0.71	0.71
Longitudinal Mass m_y / m_e	0.78	0.32	0.78	0.16	0.63
Normal Mass m_z / m_e	0.71	0.40	0.16	0.78	0.20
Conductivity Mass m_avg / m_e	0.27	0.44	0.74	0.26	0.67
Density-of-States Mass m_d / m_e	0.35	0.48	0.74	0.34	0.67

A.2 Momentum Relaxation Rate

In order to calculate the MOS inversion layer mobility, the momentum relaxation rate ($1/\tau$), which is limited by scattering, such as phonon, Coulomb, and surface roughness scattering, is needed. In this section, how to determine $1/\tau$ is introduced based on theoretical studies. The calculation of theoretical inversion layer mobility is explained in the next section.

A.2.1 Phonon Scattering

The phonon scattering rate is determined by summating the probability in two situations (i.e., absorption and emission of a lattice phonon).

The acoustic phonon scattering rate of mth sub-band [$1/\tau_m^{\mathrm{ac}}(E)$] can be calculated by following equation [1, 2]:

$$\frac{1}{\tau_m^{\mathrm{ac}}(E)} = \sum_{n=0}^{\infty} \frac{m_{\mathrm{d}} D_{\mathrm{ac}}^2 k_{\mathrm{B}} T}{\hbar^3 \rho v_{\mathrm{SiC}}} \int_0^{\infty} |\xi_n(z)|^2 |\xi_m(z)|^2 \mathrm{d}z \times u\left(E - E_n\right), \tag{A.12}$$

where D_{ac} is the deformation potential of acoustic phonons (D_{ac} is assumed to be 11.6 eV $\times$ $12/9 = 15.5$ eV [2, 10, 11]), ρ is the density of SiC ($\rho = 3211$ kg m^{-3} [12]), v_{SiC} is the sound velocity of SiC ($v_{\mathrm{SiC}} = 13730$ m s^{-1} [12]), $u(x)$ is the step function [$u(x) = 1$ for $x \geq 0$ and $u(x) = 0$ for $x < 0$].

The intra- and inter-valley non-polar optical phonon scattering rate of mth sub-band ($1/\tau_m^{\mathrm{nop}}$) is expressed by [1, 2]

$$\frac{1}{\tau_m^{\mathrm{nop}}} = \sum_{n=0}^{\infty} \frac{Z_{\mathrm{nop}} D_{\mathrm{nop}}^2 m_{\mathrm{d}}}{2\rho_{\mathrm{SiC}} \hbar^2 \omega_{\mathrm{nop}}} \left[N(\hbar\omega_{\mathrm{nop}}) + \frac{1}{2} \mp \frac{1}{2} \right] \int_0^{\infty} |\xi_n(z)|^2 |\xi_m(z)|^2 \mathrm{d}z \\ \times u\left(E - E_n \pm \hbar\omega_{\mathrm{nop}}\right) \times \frac{1 - F_{\mathrm{FD}}(E_m \pm \hbar\omega_{\mathrm{nop}})}{1 - F_{\mathrm{FD}}(E_m)}, \tag{A.13}$$

where Z_{nop} [$= 3$ (intra-valley: 1, inter-valley: 2)] is the number of valleys to which electrons transition as a result of intra- and inter-valley non-polar optical phonon scattering, D_{nop} is the deformation potential of non-polar optical phonons ($D_{\mathrm{nop}} = 2.3 \times 10^9 \times \sqrt{4/3}$ eV cm^{-1}), $\hbar\omega_{\mathrm{nop}}$ is the energy of non-polar optical phonons ($\hbar\omega_{\mathrm{nop}} = 85$ meV), $N(E)$ is the Bose-Einstein distribution function [$N(E) = [\exp(E/k_{\mathrm{B}}T) - 1]^{-1}$], and $F_{\mathrm{FD}}(E) = [1 + \exp(E - E_{\mathrm{F}}/k_{\mathrm{B}}T)]^{-1}$ is the Fermi-Dirac distribution function. Regarding the D_{nop}, the D_{nop} reported in bulk 4H-SiC [D_{nop}(bulk)] is 2.3×10^9 eV cm^{-1} obtained by considering four conduction band valleys [11]. Therefore, D_{nop} is assumed by multiplying D_{nop}(bulk) with $\sqrt{4/3}$ because three conduction band valleys are considered in the present study.

A.2.2 Coulomb Scattering

First of all, the two-dimensional Fourier transform of the Coulomb potential $[\phi_{\mathrm{pc}}(z, z_0, q)]$ is considered. Here, z_0 is the position of a point charge (irrespective of positive/negative) which produces Coulomb potential, and q is the wave vector variation defined as the difference in the wave vector between the initial and end states. In the initial state, the electrons are in the mth sub-band, and the wave vector is $k' = \sqrt{k_x'^2 + k_y'^2}$. In the end state, the electrons are in the nth sub-band, and the wave vector is $k' + q$ with a scattering angle (θ). The q is given by [1]

$$q(\theta) = \sqrt{k'^2 + D - 2k'\sqrt{D}\cos\theta}, \tag{A.14}$$

where the D is given by [1]

$$D = k'^2 - \frac{2m_{\mathrm{avg}}}{\hbar^2}(E_n - E_m). \tag{A.15}$$

The $\phi_{\mathrm{pc}}(q(\theta), z, z_0)$ is obtained by solving Poisson's equation and is expressed by [2, 6]

$$\phi_{\mathrm{pc}}(q(\theta), z, z_0) = \frac{e}{2q\varepsilon_{\mathrm{SiC}}}\phi_{\mathrm{N}}(q(\theta), z, z_0), \tag{A.16}$$

$$\phi_{\mathrm{N}}(q(\theta), z, z_0) = \exp\left[-q(\theta)|z - z_0|\right] + \frac{\kappa_{\mathrm{SiC}} - \kappa_{\mathrm{SiO_2}}}{\kappa_{\mathrm{SiC}} + \kappa_{\mathrm{SiO_2}}}\exp\left[-q(\theta)(z + |z_0|)\right], \tag{A.17}$$

where $\kappa_{\mathrm{SiO_2}}$ is the relative permittivity of SiO$_2$ (= 3.9).

Here, the Coulomb scattering rate derived from substrate impurities of mth sub-band $(1/\tau_m^{\mathrm{imp}})$ is calculated by [1, 2]

$$\frac{1}{\tau_m^{\mathrm{imp}}} = \sum_{n=0}^{\infty}\left(\frac{m_{\mathrm{d}}e^4}{8\pi\hbar^3\kappa_{\mathrm{SiC}}\varepsilon_0}\right)\int_0^{2\pi}\frac{\int_0^{\infty}|I_{mn}(q(\theta), z_0)|^2 g_{\mathrm{imp}}(z_0)\,\mathrm{d}z_0(1 - \cos\theta)}{[q(\theta) + P(q)H_{00}(q(\theta))]^2}\,\mathrm{d}\theta\cdot u(D), \tag{A.18}$$

where $I_{mn}(q(\theta), z_0)$ is given by [1, 2]

$$I_{mn}(q(\theta), z_0) = \int_0^{\infty}\xi_n^*(z)\xi_m(z)\phi_{\mathrm{N}}(q(\theta), z, z_0)\,\mathrm{d}z, \tag{A.19}$$

$g_{\mathrm{imp}}(z)$ is the volume density of substrate impurities, assuming that $g_{\mathrm{imp}}(z) = N_{\mathrm{A}}$ for $z \le z_{\mathrm{depl}}$ and $g_{\mathrm{imp}}(z) = 0$ for $z_{\mathrm{depl}} < z$, $P(q)$ is one of the screening parameters, which is given by [2, 6]

$$P(q) = -\sum_{l=0}^{\infty}\frac{e^2 n_v m_{\mathrm{d}}}{4\kappa_{\mathrm{SiC}}\varepsilon_0\pi^2\hbar^2}\int_0^{\infty}\int_0^{2\pi}\frac{F_{\mathrm{FD}}(E_l(\boldsymbol{k}+\boldsymbol{q})) - F_{\mathrm{FD}}(E_l(\boldsymbol{k}))}{E_l(\boldsymbol{k}+\boldsymbol{q}) - E_l(\boldsymbol{k})}\,\mathrm{d}\theta\,\mathrm{d}E, \tag{A.20}$$

where E_l is the energy of electrons in lth sub-band. In the $P(q)$ calculation, the $\sum_{l=0}^{\infty}$ means summation for all of the sub-bands of six conduction band valleys. In this study, the $P(q)$

is calculated by assuming parabolic circular bands. In addition, H_{00} is the other screening parameter, which is given by [1, 2]

$$H_{mn} = \int_0^\infty \int_0^\infty \xi_n^*(z_1)\xi_m(z_1)\xi_n^*(z_2)\xi_m(z_2)\phi_{\mathrm{N}}(q(\theta), z_1, z_2)\ \mathrm{d}z_1\mathrm{d}z_2, \tag{A.21}$$

$$\simeq H_{00} = \int_0^\infty \int_0^\infty |\xi_0(z_1)|^2|\xi_0(z_2)|^2\phi_{\mathrm{N}}(q(\theta), z_1, z_2)\ \mathrm{d}z_1\mathrm{d}z_2. \tag{A.22}$$

The assumption of $m = 0$ and $n = 0$ is reasonable because most of the electrons are located at the lowest sub-band.

Next, the Coulomb scattering rate derived from interface fixed charges of mth sub-band ($1/\tau_m^{\mathrm{fix}}$) is considered. The equation of $1/\tau_m^{\mathrm{fix}}$ is very similar to that of $1/\tau_m^{\mathrm{imp}}$. The difference is only the integration of the substrate impurity density with respect to z_0. Accordingly, the fixed charge density (N_{fix}) is assumed to be distributed only at $z = z_{\mathrm{it}} = 0$ [i.e., $N_{\mathrm{fix}}\delta(z - z_{\mathrm{it}})$ instead of $g_{\mathrm{imp}}(z)$, where $\delta(x) = \infty$ for $x = 0$, $\delta(x) = 0$ for $x \neq 0$, and $\int_{-\infty}^{\infty} \delta(x)\ \mathrm{d}x = 1$]. Then, $1/\tau_m^{\mathrm{fix}}$ is expressed by [2]

$$\frac{1}{\tau_m^{\mathrm{fix}}} = \sum_{n=0}^{\infty} \left(\frac{m_{\mathrm{d}} e^4}{8\pi\hbar^3\kappa_{\mathrm{SiC}}\varepsilon_0} \right) \int_0^{2\pi} \frac{|I_{mn}(q(\theta), z_{\mathrm{it}})|^2 N_{\mathrm{fix}}(1 - \cos\theta)}{[q(\theta) + P(q)H_{00}(q(\theta))]^2}\ \mathrm{d}\theta \cdot u(D), \tag{A.23}$$

where $I_{mn}(q(\theta), z_{\mathrm{it}})$ is given by [2]

$$I_{mn}(q(\theta), z_{\mathrm{it}}) = \int_0^\infty \xi_n^*(z)\xi_m(z)\phi_{\mathrm{N}}(q(\theta), z, z_{\mathrm{it}})\ \mathrm{d}z, \tag{A.24}$$

$$= \int_0^\infty \xi_n^*(z)\xi_m(z)\frac{2\kappa_{\mathrm{SiC}}}{\kappa_{\mathrm{SiC}} + \kappa_{\mathrm{SiO_2}}} \exp\left[-q(\theta)z\right]\ \mathrm{d}z. \tag{A.25}$$

If the position of the fixed charges is correlated, the influence of Coulomb scattering will be small. The $1/\tau_m^{\mathrm{fix}}$ considering the correlation of fixed charges is expressed by [6]

$$\frac{1}{\tau_m^{\mathrm{fix}}} = \sum_{n=0}^{\infty} \left(\frac{m_{\mathrm{d}} e^4}{8\pi\hbar^3\kappa_{\mathrm{SiC}}\varepsilon_0} \right) \int_0^{2\pi} \frac{|I_{mn}(q(\theta), z_{\mathrm{it}})|^2 N_{\mathrm{fix}} \left[1 - \dfrac{2CJ_1(qR_{\mathrm{c}})}{qR_{\mathrm{c}}} \right] (1 - \cos\theta)}{[q(\theta) + P(q)H_{00}(q(\theta))]^2}\ \mathrm{d}\theta \cdot u(D), \tag{A.26}$$

where C_{fix} is the correlation factor and J_1 is the Bessel function of the first order. The C_{fix} is defined as $C_{\mathrm{fix}} = \pi R_{\mathrm{c}}^2 N_{\mathrm{fix}}$, where R_{c} is the critical radius, and thus πR_{c}^2 is the critical area. Figure A.1 shows the experimental Hall mobility and free electron mobility calculated by considering the correlation of the position of fixed charges as a function of the effective normal field for SiC (0001) MOSFETs annealed in NO with various N_{A} of p-body at room temperature. The symbols represent the experimental results. The calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the effective

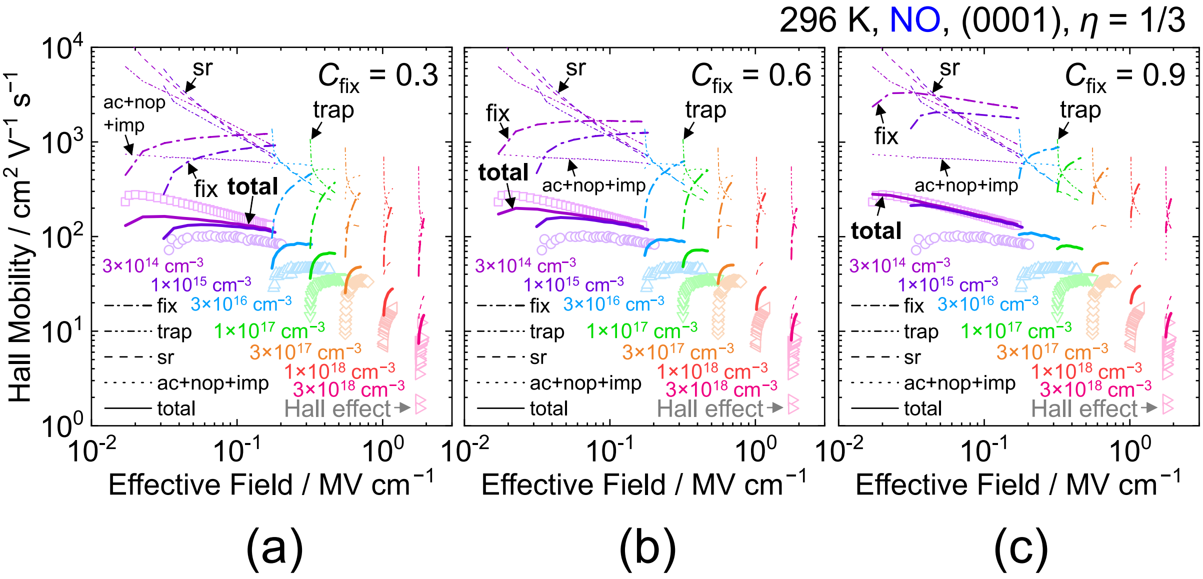

Figure A.1: Experimental Hall mobility and free electron mobility calculated by considering the correlation of the position of fixed charges as a function of the effective normal field for SiC (0001) MOSFETs annealed in NO with various acceptor concentrations of p-body (3×10^{14} cm$^{-3} \le N_\mathrm{A} \le 3\times10^{18}$ cm^{-3}) at room temperature. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. The correlation factor (C_fix) is set as (a) 0.3, (b) 0.6, and (c) 0.9 in the calculation. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the effective normal field. The fixed charge density (N_fix), surface roughness height ($\mathit{\Delta}_\mathrm{sr}$), and surface roughness correlation length (L_sr) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

normal field. The N_{fix}, the height of surface roughness (Δ_{sr}), and the correlation length of surface roughness (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively. The C_{fix} is set as 0.3, 0.6, and 0.9 in the calculation. The fixed charges are uniformly distributed when C_{fix} is close to 1. In the case of lightly-doped ($N_{\text{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs, the fixed charges-limited mobility is more than 2000 cm^2 V^{-1} s^{-1} in the wide effective normal field range when C_{fix} is 0.9 [Fig. A.1(c)]. As a result, the calculated free electron mobility is close to the experimental Hall mobility. Therefore, to explain the high Hall mobility observed in NO-annealed lightly-doped ($N_{\text{A}} = 3 \times 10^{14}$ cm^{-3}) MOSFETs, the correlation of the position of fixed charges should be considered.

Similarly, the Coulomb scattering rate derived from interface trapped charges of mth sub-band ($1/\tau_m^{\text{trap}}$) can be expressed by [2]

$$\frac{1}{\tau_m^{\text{trap}}} = \sum_{n=0}^{\infty} \left(\frac{m_{\text{d}} e^4}{8\pi\hbar^3 \kappa_{\text{SiC}} \varepsilon_0} \right) \int_0^{2\pi} \frac{|I_{mn}(q(\theta), z_{\text{it}})|^2 n_{\text{trap}} (1 - \cos\theta)}{[q(\theta) + P(q) H_{00}(q(\theta))]^2} \, \mathrm{d}\theta \cdot u(D), \tag{A.27}$$

where n_{trap} is the trapped electron density, which can be calculated by Eq. 2.3.

If the trapped electrons are localized not at SiC/SiO$_2$ but in SiC, the $1/\tau_m^{\text{trap}}$ is calculated by

$$\frac{1}{\tau_m^{\text{trap}}} = \sum_{n=0}^{\infty} \left(\frac{m_{\text{d}} e^4}{8\pi\hbar^3 \kappa_{\text{SiC}} \varepsilon_0} \right) \int_0^{2\pi} \frac{\int_0^{\infty} |I_{mn}(q(\theta), z_0)|^2 g_{\text{trap}}(z_0) \, \mathrm{d}z_0 (1 - \cos\theta)}{[q(\theta) + P(q) H_{00}(q(\theta))]^2} \, \mathrm{d}\theta \cdot u(D), \tag{A.28}$$

where g_{trap} is the volume density of trapped electrons and satisfies the following equation:

$$n_{\text{trap}} = \int_0^{\infty} g_{\text{trap}}(z) \, \mathrm{d}z. \tag{A.29}$$

A.2.3 Surface Roughness Scattering

The surface roughness scattering rate is expressed by [2]

$$\frac{1}{\tau_m^{\text{sr}}} = \sum_{n=0}^{\infty} \left[\frac{m_{\text{d}} (eE_{\text{eff},mn})^2 (\Delta_{\text{sr}} L_{\text{sr}})^2}{2\hbar^3} \right] \int_0^{2\pi} \frac{\left(1 + \dfrac{q(\theta)^2 L_{\text{sr}}^2}{2} \right)^{-3/2} (1 - \cos\theta)}{\left[1 + \dfrac{P(q) H_{00}(q(\theta))}{q(\theta)} \right]^2} \, \mathrm{d}\theta \cdot u(D), \tag{A.30}$$

where $eE_{\text{eff},mn}$ is expressed by [2, 6]

$$eE_{\text{eff},mn} = \left| \frac{\hbar^2}{2m_z} \frac{\mathrm{d}\xi_n^*(z)}{\mathrm{d}z} \frac{\mathrm{d}\xi_m(z)}{\mathrm{d}z} \right|. \tag{A.31}$$

In the present study, the correlation function is assumed to be exponential [6, 13] because the experimental mobility can be reproduced by using the exponential function in the case of Si MOSFETs [1, 13, 14].

The surface roughness scattering rate by assuming that the correlation function is Gaussian is given by [6, 13]

$$\frac{1}{\tau_m^{\mathrm{sr}}} = \sum_{n=0}^{\infty} \left[\frac{m_{\mathrm{d}} (eE_{\mathrm{eff},mn})^2 (\Delta_{\mathrm{sr}} L_{\mathrm{sr}})^2}{2\hbar^3} \right] \int_0^{2\pi} \frac{\exp\left(-\frac{q(\theta)^2 L_{\mathrm{sr}}^2}{4} \right) (1 - \cos\theta)}{\left[1 + \frac{P(q) H_{00}(q(\theta))}{q(\theta)} \right]^2} \mathrm{d}\theta \cdot u(D). \quad \text{(A.32)}$$

Figure A.2 shows the experimental Hall mobility and free electron mobility calculated by assuming that the correlation function is exponential or Gaussian as a function of the effective normal field for SiC (0001) MOSFETs annealed in $\mathrm{POCl_3}$ with various N_{A} of p-body at room temperature. The symbols and lines are the same meaning as those in Fig. A.1. In the calculation, N_{fix}, Δ_{sr}, and L_{sr} are 7.5×10^{12} $\mathrm{cm^{-2}}$, 1.0 nm, and 5.0 nm, respectively. In Fig. A.2(a), the correlation function is assumed to be exponential. Then, the surface roughness-limited mobility strongly decreases at a high gate bias. On the other hand, the correlation function is assumed to be Gaussian in Fig. A.2(b). In this case, the influence of surface roughness scattering significantly changes, especially at a high gate bias. Therefore, the impact of the correlation function at $\mathrm{SiC/SiO_2}$ interfaces on mobility should be extensively investigated from both experimental and theoretical studies.

A.3 Inversion Layer Mobility

The momentum relaxation time for the total scattering of mth sub-band ($1/\tau_m$) is calculated by $1/\tau_m = 1/\tau_m^{\mathrm{ac}} + 1/\tau_m^{\mathrm{nop}} + 1/\tau_m^{\mathrm{imp}} + \cdots$. Then, the average momentum relaxation time of mth sub-band ($\langle \tau_m \rangle$) is needed to obtain the inversion layer mobility. $\langle \tau_m \rangle$ can be expressed by using τ_m as [1]

$$\langle \tau_m \rangle = \frac{\int_{E_m}^{\infty} \tau_m (E - E_m) F_{\mathrm{FD}}(E)[1 - F_{\mathrm{FD}}(E)]}{\int_{E_m}^{\infty} (E - E_m) F_{\mathrm{FD}}(E)[1 - F_{\mathrm{FD}}(E)]} \mathrm{d}E. \quad \text{(A.33)}$$

As a result, the mobility (μ) is obtained by [1]

$$\mu = \sum_{m=0}^{\infty} \frac{n_m}{n_{\mathrm{free}}} \frac{e \langle \tau_m \rangle}{m_{\mathrm{avg}}}. \quad \text{(A.34)}$$

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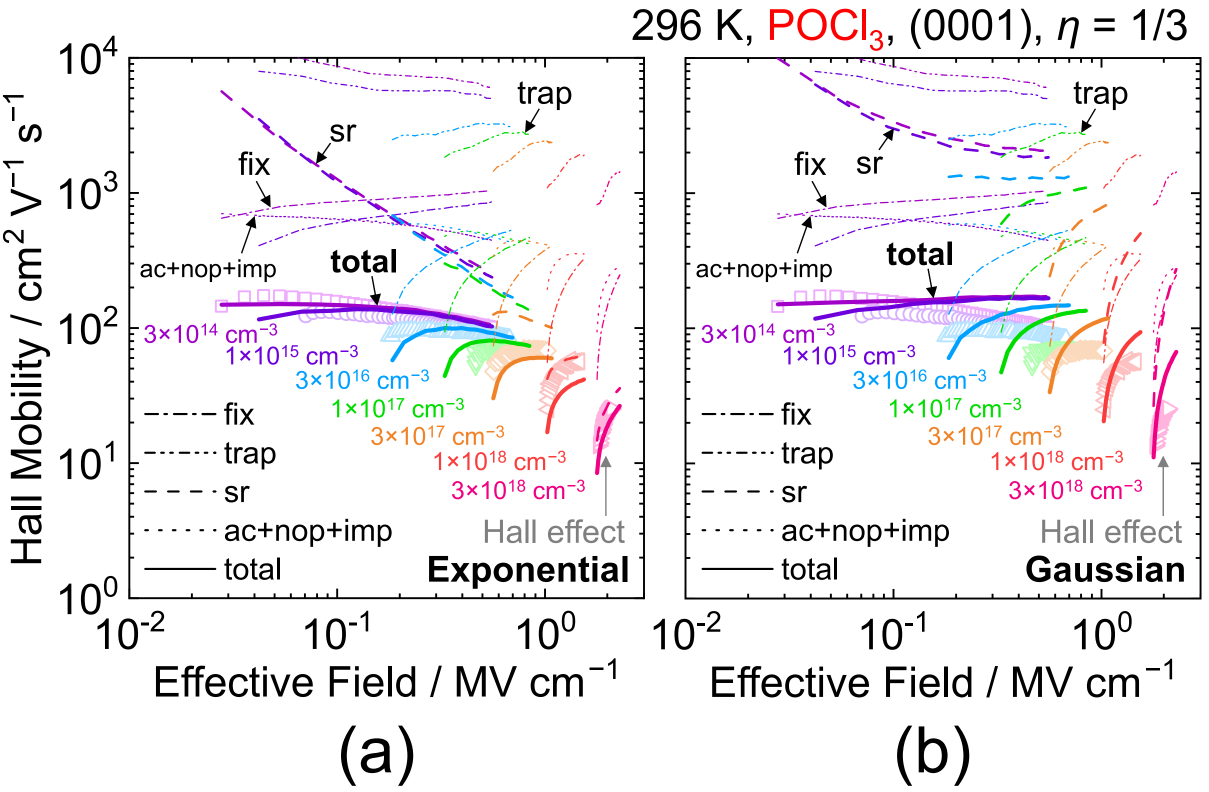

Figure A.2: Experimental Hall mobility and free electron mobility calculated by assuming that the correlation function is (a) exponential or (b) Gaussian as a function of the effective normal field for SiC (0001) MOSFETs annealed in $POCl_3$ with various acceptor concentrations of p-body (3×10^{14} cm^{-3} $\leq N_A \leq 3 \times 10^{18}$ cm^{-3}) at room temperature. Experimental results are represented by symbols. Calculated phonon and substrate impurities-limited (ac+nop+imp), fixed charges-limited (fix), trapped electrons-limited (trap), surface roughness-limited (sr), and total (total) mobilities are shown by dotted, dashed-dotted, dashed double-dotted, dashed, and solid lines, respectively. Here, η (= 1/3) is a parameter that indicates how much the electrons contribute to the effective normal field. The fixed charge density (N_{fix}), surface roughness height ($\mathit{\Delta}_{sr}$), and surface roughness correlation length (L_{sr}) are 7.5×10^{12} cm^{-2}, 1.0 nm, and 5.0 nm, respectively.

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List of Publications

A. Full Length Papers and Letters

1. T. Kobayashi, K. Tachiki, K. Ito, and T. Kimoto,
   "Reduction of interface state density in SiC (0001) MOS structures by low-oxygen-partial-pressure annealing,"
   Applied Physics Express **12**, 031001 (2019).

2. K. Ito, T. Kobayashi, and T. Kimoto,
   "Influence of vacuum annealing on interface properties of SiC (0001) MOS structures,"
   Japanese Journal of Applied Physics **58**, 078001 (2019).

3. T. Kobayashi, T. Okuda, K. Tachiki, K. Ito, Y. Matsushita, and T. Kimoto,
   "Design and formation of SiC (0001)/SiO_2 interfaces via Si deposition followed by low-temperature oxidation and high-temperature nitridation,"
   Applied Physics Express **13**, 091003 (2020).

4. K. Ito, T. Kobayashi, and T. Kimoto,
   "Effect of quantum confinement on the defect-induced localized levels in 4H-SiC(0001)/SiO_2 systems,"
   Journal of Applied Physics **128**, 095702 (2020).

5. K. Mikami, K. Tachiki, K. Ito, and T. Kimoto,
   "Body doping dependence of field-effect mobility in both n- and p-channel 4H-SiC metal-oxide-semiconductor field-effect transistors with nitrided gate oxides,"
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6. T. Hosoi, M. Ohsako, K. Moges, K. Ito, T. Kimoto, M. Sometani, M. Okamoto, A. Yoshigoe, T. Shimura, and H. Watanabe,
   "Impact of post-nitridation annealing in CO_2 ambient on threshold voltage stability in 4H-SiC metal-oxide-semiconductor field-effect transistors,"
   Applied Physics Express **15**, 061003 (2022).

7. K. Tachiki, K. Mikami, K. Ito, M. Kaneko, and T. Kimoto,
   "Mobility enhancement in heavily doped 4H-SiC (0001), ($11\bar{2}0$), and ($1\bar{1}00$) MOSFETs via an oxidation-minimizing process" (Spotlights 2022),
   Applied Physics Express **15**, 071001 (2022).

8. K. Ito, M. Horita, J. Suda, and T. Kimoto,
   "Effective channel mobility in phosphorus-treated 4H-SiC (0001) metal-oxide-semiconductor field-effect transistors with various p-body doping concentrations,"
   Japanese Journal of Applied Physics **61**, 098001 (2022).

9. K. Ito and T. Kimoto,
   "Mobility degradation under a high effective normal field in an inversion layer of 4H-SiC (0001) metal-oxide-semiconductor structures annealed in $POCl_3$,"
   Applied Physics Express **15**, 121006 (2022).

10. K. Ito, M. Horita, J. Suda, and T. Kimoto,
    "High Hall electron mobility in the inversion layer of 4H-SiC (0001)/SiO_2 interfaces annealed in $POCl_3$,"
    in preparation.

11. K. Ito, H. Tanaka, M. Horita, J. Suda, and T. Kimoto,
    "Experimental and theoretical analysis of Hall electron mobility in 4H-SiC (0001), ($11\bar{2}0$), and ($1\bar{1}00$)/SiO_2 inversion layers,"
    in preparation.

B. Conference Proceedings

1. T. Kimoto, M. Kaneko, K. Tachiki, K. Ito, R. Ishikawa, X. Chi, D. Stefanakis, T. Kobayashi, and H. Tanaka,
   "Physics and Innovative Technologies in SiC Power Devices,"
   Technical Digest of 67th IEEE International Electron Devices Meeting (2021) p. 761.

C. International Conferences

1. K. Ito, T. Kobayashi, M. Horita, J. Suda, and T. Kimoto,
   "Modeling of Electron Trapping in SiC MOSFETs Considering Interface-State-Density Distribution Extracted from Gate Characteristics,"
   European Conference on Silicon Carbide and Related Materials 2018 (Birmingham, UK, 2018), MO.P.MI6, Poster.

2. T. Kobayashi, K. Tachiki, K. Ito, Y. Matsushita, and T. Kimoto,
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   European Conference on Silicon Carbide and Related Materials 2018 (Birmingham, UK, 2018), TU.01a.05, Oral.

3. K. Ito, T. Kobayashi, M. Horita, J. Suda, and T. Kimoto,
   "Estimation of interface-state-density distribution of SiC MOS structures from gate characteristics of MOSFETs,"
   International Symposium on Photonics and Electronics Science and Engineering 2019 (Kyoto, Japan, 2019), P-15, Poster.

4. T. Kimoto, T. Kobayashi, K. Tachiki, and K. Ito,
   "Promise and Future Challenges of SiC Power MOSFETs" (Invited),
   21st International Conference on Insulating Films on Semiconductors (Cambridge, UK, 2019), 4.1, Oral.

5. K. Ito, T. Kobayashi, and T. Kimoto,
   "Interface State Density Distributions near The Conduction Band Edge Originating from The Conduction Band Fluctuation in SiO_2/SiC Systems" (Invited),
   International Conference on Silicon Carbide and Related Materials 2019 (Kyoto, Japan, 2019), Tu-3A-01, Oral.

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   "Energy distributions of interface state density originating from tail states of the conduction band in SiC MOS structures,"
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11. K. Mikami, K. Ito, K. Tachiki, and T. Kimoto,
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European Conference on Silicon Carbide and Related Materials 2020·2021 (Tours, France/Online, 2021), TU-1B-01, Oral.

12. K. Ito, M. Horita, J. Suda, and T. Kimoto,
“Universal Mobility in SiC MOSFETs with Very Low Interface State Density,”
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13. K. Tachiki, K. Ito, M. Kaneko, and T. Kimoto,
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