Robust Design of Low-voltage OTFT Circuits for Flexible Electronic Systems

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Abstract

Flexible electronics have attracted significant attention as an emerging technology for use in a wide range of internet-of-things (IoT) applications. In particular, organic thin-film transistors (OTFTs) have attracted great attention and are the subject of intense research due to their appealing properties such as flexibility, biocompatibility, and low supply voltage. In addition, OTFTs can be fabricated through low-cost and low-temperature printing processes. With the printing process, OTFT circuits can be fabricated on various substrates, such as flexible plastic film. As a result of intensive research efforts, considerable improvements have been made to the performance of OTFTs. Various applications that use OTFTs as principal active device components have been reported.

Although OTFT applications such as flexible sensors or smart labels are being studied, most of the current researches focus on the materials and the structure of the sensors that perform signal detection. Meanwhile, how to treat the data in these systems is also an essential issue. For instance, in a flexible sensor, after the data are detected, memory is needed to save these data. It should also be considered how to protect these data. Thus, the circuits used to control and compute the data in these systems are required. At present, most of these functions rely on external silicon devices. However, the data transmission between the OTFTs and silicon devices requires additional time and power. Implementing a OTFTs and silicon hybrid system also decreases the advantage of OTFTs low-cost fabrication process. Therefore, the OTFT circuitry considering treatments of local signal data is required.

This dissertation is devoted to use OTFT circuits to realize the local treatments of data in organic systems from three aspects, security, storage, and processing. However, being fundamentally different from silicon technologies, traditional silicon circuit design topology is not suitable for OTFTs. The OTFTs are unipolar, in which p-type transistors are much stronger than n-type transistors. In addition, OTFTs, especially n-type transistors, are sensitive to bias-stress and humidity in the air, resulting in a temporal reduction of mobility. Hence, in this dissertation, several circuit design typologies are also proposed to deal with these intrinsic detects of OTFTs.

In the first part of this dissertation, an OTFT physical unclonable function (PUF) is proposed for hardware security. The OTFT PUF can be used for privacy protection for the information collected by flexible sensors, or smart packaging to ensure the authenticity of products. A current mirror array is used for the proposed OTFT PUF. The current mirror can achieve self-compensation for the unavoidable degradation of OTFTs. In this part, two types of PUFs are proposed; one pursues area efficiency and the other aims for improved robustness. Through fabrication and measurement of the two OTFT PUFs, it demonstrates that the fabricated OCM-PUFs achieved 95% reliability, showing that the proposed PUFs achieve a high tolerance against response changes caused by device aging.

The second part of this dissertation focuses on an OTFT SRAM used for data storage. In traditional silicon CMOS SRAM construction, the pull down n-type transistors need to be designed strongest to sustain a stable operation, which is difficult for unipolar OTFTs. The general OTFT-based SRAM construction uses a pseudo-CMOS structure with only p-type transistors. However, the pseudo-CMOS topology decreases the stability and area efficiency of circuits. In this part, a CMOS design using p-type access transistors is adapted for SRAM cells to gain high stability and area efficiency. Then, the periphery circuits, decoder, and sense amplifier, for the SRAM array are designed. Moreover, to extend retention time, a degradation-mitigation circuit, based on a pseudo-CMOS design, is proposed. This circuit can self-detect degradation and automatically perform a process to mitigate device degradation at the necessary time periods. Through test chip measurements, the proposed SRAM cell achieves 50% area reduction and 2.5x static noise margin improvement compared to existing OTFT SRAM cells. The retention time of SRAM memory can be extended to at least 3x via the proposed degradation-mitigation circuit.

The ability of data processing is discussed in the last part of this dissertation. As demonstrated above, for general logic circuits, traditional CMOS design is not suitable for OTFTs, due to the unbalance of n-type transistors and p-type transistors. An alternative design topology, pass transistor logic (PTL), is proposed in this part. The PTL decreases the transistor counts and mainly depends on the strong p-type transistors. A full adder, which is the essential unit in logic circuits, is used as an example to demonstrate the construction of a PTL circuits. Compared to a traditional CMOS full adder, the transistor counts of PTL adder can be reduced by 50%. Furthermore, for full data processing, a processor based on PTL is discussed in this part. The processor uses one instruction set computer (OISC) architecture. The OISC uses only one instruction to execute all operations, hence the circuit is extremely simple and lightweight. The operation of each component in the OISC processor is

confirmed through test chip measurements, presenting the feasibility of the OTFT OISC processor.

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Chapter 1

Introduction

1.1 Flexible Electronics

With the development of IoT society, the amount of information being processed is exploding. The IoT device has emerged as an indispensable infrastructure for our daily lives. As these IoT devices are used in various situations, the demand for a wide range of materials, from traditional hard silicon to soft materials, is required according to the IoT applications. In response to such requirements, organic thin-film transistors (OTFTs) have attracted great attention and are the subject of intense research due to their appealing properties, such as flexibility, lightness, and biocompatibility [3–5]. Owing to their low cost and low temperature process, the OTFTs can be fabricated on various materials, such as flexible plastic films [6, 7]. Additionally, OTFTs can operate at a low supply voltage. Furthermore, in recent years, intensive research efforts significantly improved the performance of OTFTs [8–11]. As a result, various applications that use OTFTs as principal active device components have been reported. Examples include analog-to-digital (A/D) [12] or digital-to-analog (D/A) converters [13], RFID tags [4], microprocessors [14, 15], and flexible sensors [5].

Compared to other flexible thin-film transistors, such as IGZO TFT or ZnO TFT which need high supply voltage, such as 20 V [16, 17], the OTFTs used in this dissertation are driven by a low voltage of 3 V or lower. A simple external power supply such as coin batteries can be the energy source of the OTFTs. Thus, OTFT-based applications can be integrated more easily and safely. Moreover, through the printing process in the fabrication of OTFTs, it is possible to manufacture integrated circuits on a variety of objects. Consequently, everything around us has the ability to process information. For example, a smart label could be printed on a product package with an organic

sensor circuit. Smart labels not only store product information but also detect and store information of surrounding environments during transportation and storage. They also can be disposable with the product package due to the low fabrication cost of the organic circuits. Additionally, in the medical healthcare field, the organic flexible sensor can be used as an active sensor that adheres to the skin to improve sensitivity in detecting biometric information. The sensor can be easily customized by adjusting the position of the electrodes and printing on-demand according to the patient's body shape.

1.2 Motivation

At present, researches on organic transistors focus on the materials or structures of sensors for signal detection [8–11]. The processing or control of the signal generally relies on conventional silicon circuits. This results in the loss of the greatest advantage of organic transistors, which is that the entire system can be fabricated in a low cost printing process. Moreover, the power and time required to transmit the sensor signal to the silicon circuitry reduce energy efficiency [18, 19]. For a practical application of organic electronics, circuitry considering treatments of local signal data is required.

In an example of smart labels, owing to the low cost fabrication process, the smart label can be easily fabricated on the packaging material of merchandise, typically on plastic films. The smart label has the ability to store the information about the merchandise, including production date, place of production, lot number, serial number, etc. Additionally, for environmentally sensitive products, such as fresh vegetables, fish, meat, or wines, the recording of the environmental conditions is significantly useful. By storing environmental information such as temperature, humidity, and sunlight exposure, the products can be protected during delivery and storage. In addition, security functions are also important, such as authenticating the products or protecting stored information from malicious attacks. Then, a microprocessor is required to perform simple data processing and control data flow in those systems.

However, OTFT technology is fundamentally different from conventional silicon technology. There are several challenges that OTFT circuits are encountering. The OTFTs are unipolar devices, in which p-type transistors are much stronger than n-type. Compared with n-type transistors, p-type transistors exhibit more than 10x higher on-current and a significantly better on-off current ratio. Device degradation is also a negative feature of OTFTs. The OTFTs are sensitive to bias-stress and the reaction of organic semiconductor and humidity in the air reduces the mobility and on-current [20]. Furthermore, although OTFTs derive benefits from low cost fabrication processes, the defective rate of

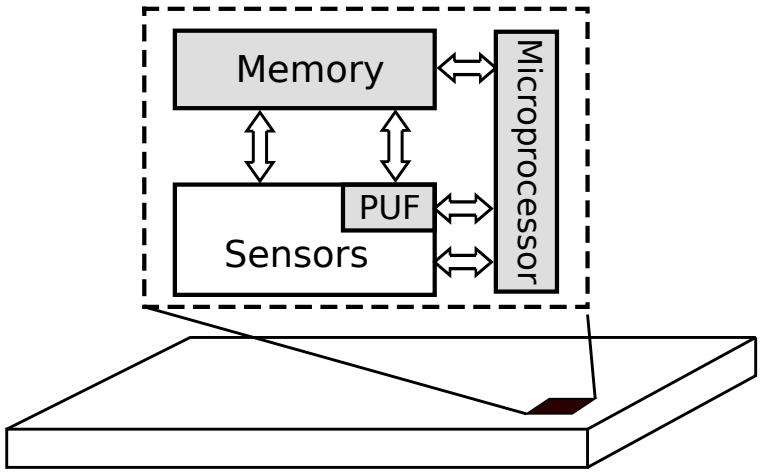


Figure 1.1: Conceptual illustration of a flexible system.

OTFTs is relatively high. Thus, traditional silicon circuit design is not suitable for designing OTFT circuits. For example, the performance of the circuits designed using the conventional CMOS style is considered to be low in the case of OTFTs, due to the performance unbalance between p-type and n-type transistors. The topology used to mitigate the effect of device degradation is required and additional efforts are required to enhance the operation of the OTFT circuits.

In this dissertation, the local treatments of data in organic systems are discussed from three aspects: security, storage, and processing. Additionally, several circuit design typologies are proposed to deal with the above-mentioned challenges in OTFTs. The conceptual illustration of the flexible system considered in this study is shown in Fig. 1.1. First, a hardware security circuit called physically unclonable functions (PUF) used for data security is proposed. OTFT PUF can be implemented in flexible sensors to improve the security of the communication that those devices establish. Moreover, it can also be printed on the packaging of merchandise for authenticating the merchandise. The proposed PUF achieves self-compensation against device degradation for a stable operation. Second, an OTFT memory is proposed for data storage. The OTFT memory can store data generated from the OTFT sensor shown in Fig 1.1 or the security data from PUF. The proposed memory achieves high stability and area efficiency. Based on a traditional memory architecture, a degradation-mitigation circuit is added to extend the retention time of the OTFT memory. Finally, the arithmetic circuits suitable for OTFT implementation are presented. These circuits enable the entire OTFT system to have the ability to compute and control the data. A feasibility of a Turning complete OTFT processor is presented in this dissertation.

1.3 Approaches

In this section, details of the aforementioned issues and the methods proposed to counterpart the issues in this dissertation are provided.

1.3.1 OTFT PUF for Data Security

As applications for OTFTs, such as flexible sensors or smart labels are developed, information leakage from these IoT devices has become a serious problem. In particular, attacks on medical equipment or social infrastructure devices pose a major threat to social systems. The information security and authorization of hardware devices have become crucial. For that reason, PUFs used to enhance hardware security are of high interest [21–24]. Based on physical variations caused during the manufacturing process, PUFs generate random, unclonable, unique identification information for each chip. The traditional silicon PUFs are generally used for authentication of the hardware devices. Through the implementation of OTFTs, the application of PUFs can be broadened, such as smart packaging to the authenticity of products or privacy protection for the information collected by organic sensors.

However, compared with silicon devices that can typically operate stably for more than ten years, degradation of OTFTs is observed on the scale of a few days. The reaction of moisture and organic semiconductor, as well as bias-voltage stress, increase the threshold voltage of the device and decrease the carrier mobility, resulting in a decrease in source-drain current. In PUF circuits, it is difficult to use it for authentication if PUF output change over time due to the degradation of OTFTs. Considering applications such as the authenticity of products for smart packaging, circuit life should be at least several weeks.

In this dissertation, organic current mirror PUF (OCM-PUF), a PUF structure resistant to the degradation of OTFTs is proposed. In the current mirror, the reference current is copied to obtain the output current. However, due to device variations, there are slight differences in the output current. This difference is used to generate a unique response. The circuit structure of the proposed PUF is simple, hence a stable circuit operation is expected even if the circuit is designed using OTFTs. Despite its simplicity, the proposed PUF achieves self-compensation against device degradation by utilizing the current mirror structure. Moreover, two types of OCM-PUF are proposed. One pursues area efficiency and the other aims for improved robustness. The PUF metrics of the two proposed PUFs are evaluated and compared through measurement.

1.3.2 OTFT SRAM for Data Storage

In order to implement more advanced functions into flexible IoT systems, local data storage is also indispensable. As the concept of the Turing machine suggests, the essence of computing is the operation on the memory value. Accordingly, for data processing in flexible systems, such as wearable sensors, it is desirable to integrate a flexible memory using the same process as the sensors. Storing the data locally can save transmit power and time [18]. Moreover, the manufacturing cost can be reduced significantly if the fabrication process of the memory is fully compatible with that of the sensors. To guarantee the access speed and stability of data storage, static random access memory (SRAM) is adopted in this dissertation, which can achieve stable operation with fast access time.

Different from traditional silicon technology, OTFTs are unipolar devices. P-type is much stronger than n-type and OTFTs are sensitive to bias stress degradation. Hence traditional silicon SRAM using CMOS structure is not suitable for the OTFTs. In conventional SRAM construction using OTFTs, a pseudo CMOS design that uses only p-type transistors is adopted. However, compared with the traditional CMOS designs, the circuits based on pseudo-CMOS design occupy a larger area and full swing outputs are hardly possible.

In this dissertation, a CMOS and pseudo-CMOS hybrid organic SRAM with enhanced stability is proposed. A CMOS design is utilized in SRAM cell to achieve high area efficiency and stable operation. The proposed SRAM cell using p-type access transistors realizes sufficient static noise margin (SNM) for stable operation despite the use of weak n-type transistors. Along with the SRAM cell, the specific implementation of the periphery circuit used in the SRAM array is explained. Moreover, a degradation-mitigation circuit using a pseudo-CMOS design is proposed. The pseudo-CMOS design is used for the purpose of stable performance and reliability for a long period. This circuit can self detect degradation and automatically perform a process to mitigate device degradation at required time periods.

1.3.3 OTFT Arithmetic Circuits for Data Processing

Besides data security and storage, the ability of data processing is indispensable for organic systems. Similar to the OTFTs memory, the near-sensor computing of the system data can also reduce the integration cost. As mentioned above, the OTFTs are unipolar and tend to degrade fast. The current low cost fabrication process leads to a relatively high defective rate. Several design typologies for data processing circuits are discussed to solve these issues of OTFTs [25, 26].

In this dissertation, OTFT circuit design based on pass transistor logic

(PTL) is proposed. PTL is a widely discussed logic family used as an alternative design topology to traditional CMOS [27]. The PTL proposed in this dissertation is designed to reduce the number of required transistors, leading to a high area efficiency. PTL also relies on strong p-type transistors, avoiding the use of n-type as much as possible. The p-type based circuitry guarantees high stability. Two types of PTL circuits are discussed and compared through simulation. A full adder, which is the most widely used logic circuit, is used as an example to confirm the operation of a PTL-based arithmetic circuit.

Furthermore, as an example of a PTL circuit, a PTL-based OTFT processor is studied in this dissertation. The proposed processor is based on one instruction set computer (OISC) architecture and it is Turning complete. OISC structure uses only one instruction to execute any program at the expense of operation time and memory space. The architecture is extremely simple and lightweight since it only has one instruction. The component circuits mainly depend on PTL, which is suitable for OTFTs implementation. To confirm the feasibility of the proposed OISC processor, typical operations in an organic system are performed by the proposed processors.

1.4 Organization

The organization of this dissertation is summarized as follows. In Chapter 2, preliminaries of OTFTs are provided. The device structure, specific fabrication process, and device model used for the simulations are presented. The chip fabrication, circuit simulation, and degradation evaluation discussed in this dissertation are based on the preliminaries in this chapter.

In Chapter 3, the implementation of OTFT PUFs for hardware authentication is discussed. To achieve self-compensation of the device performance degradation, OTFT PUFs use the current mirror structure. Then, two types of current mirror PUFs are demonstrated; one aiming for area efficiency and the other pursuing improved robustness. Through test chip measurements, the metrics of two proposed OTFT PUFs are compared and evaluated. The ability to resist device degradation is also confirmed through a long period of measurement.

Chapter 4 proposes OTFT SRAM circuits. Firstly, the architecture of the SRAM array is introduced. A degradation mitigation circuit is added to extend retention time. A new design topology in SRAM cell is proposed to increase the stability and area efficiency. Then, specific circuit structures in the SRAM array are designed. The transistor sizes of the SRAM cell are optimized through simulation. Finally, the operations of the SRAM cell, periphery circuits, and SRAM array are confirmed through test chip measurements. Additionally, the

effectiveness of the degradation mitigation circuit is verified.

Chapter 5 discusses the data processing in the OTFT system. For the logic circuit, a design topology using PTL is proposed. A full adder using PTL is used as an example. Through simulation and measurements, this design topology is proven to be suitable for logic circuit implementation using OTFTs. Based on the PTL, Chapter 5 also demonstrates an OTFT processor. The proposed processor using OISC simplifies architecture and the construction is lightweight. The OISC processor intensively uses the pass transistors and mainly depends on the proposed PTL adder. A feasibility of the proposed processor is again confirmed through simulation and measurements.

In Chapter 6, a summary of this dissertation and future works are discussed.

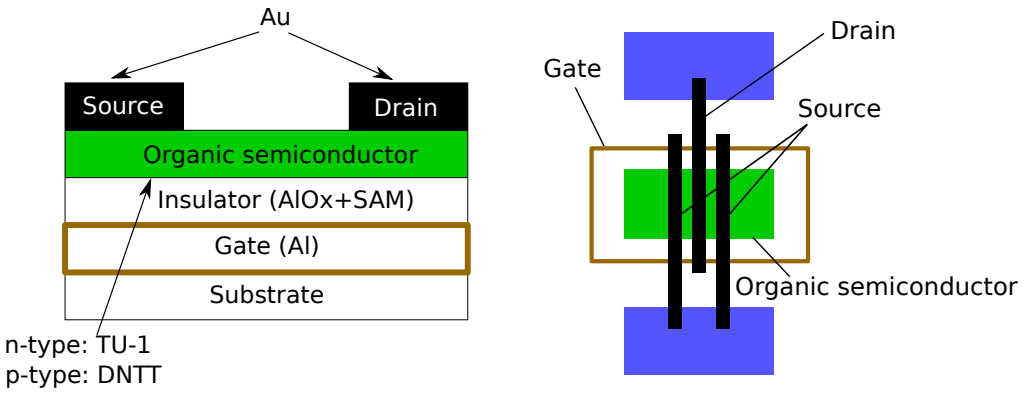
Chapter 2

Preliminaries of Organic thin film transistors

The OTFTs are a type of thin-film transistors (TFTs) in which the semiconductor is made of organic materials. Similar to silicon transistors, OTFTs have three terminals, gate, source, and drain and they operate as switches in logic circuits. While their fabrication processes are much less complex than conventional silicon technology. OTFTs can be fabricated in low temperature and low cost deposition or printing processes. In addition, the mechanical flexibility of organic materials enables OTFTs compatible with flexible substrates. In this chapter, detailed background knowledge about OTFTs used in this dissertation is provided. The device structure and fabrication process are introduced in Section 2.1 and Section 2.2. Section 2.3 provides the device model for OTFTs used for SPICE simulation. The OTFTs characteristic, especially device degradation, is explained in Section 2.4

2.1 OTFTs structure

The OTFTs considered in this dissertation exhibit a top contact and bottom gate structure with a minimum feature size of $50\,\mu$m. A simplified cross-sectional structure showing a film layer stack is illustrated in Fig. 2.1(a). Depending on the relative position (top/bottom) of contact, gate electrodes, and organic semiconductor, there are four types of device structures which are shown in Fig. 2.2. The structure in which the gate electrode is located below the semiconductor layer is called the "bottom gate" type and the structure in which the gate electrode is placed above the semiconductor layer is called the "top gate." Similarly, by the position of contact and semiconductor, there are "top contact" and "bottom contact" structures.



(a) Film layer stack.

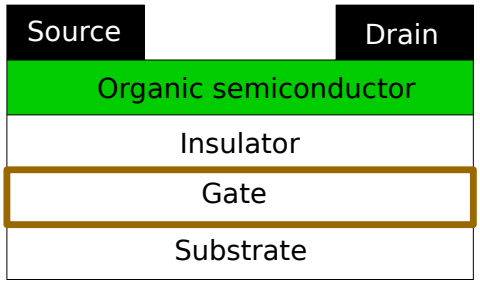
(b) Example transistor layout.

Figure 2.1: Structure of low voltage organic thin-film transistor. © IEEE 2020

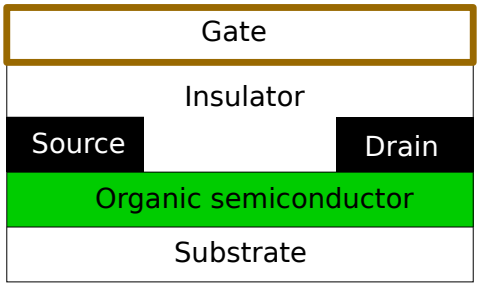
In the bottom contact structure, the contact electrode is fabricated first, and then the organic semiconductor is fabricated on the contact electrode. It is hard for the organic semiconductor to form a uniform surface between the contact layer and the organic semiconductor layer. Hence, the bottom contact structure shows higher contact resistance than the top contact structure [28,29]. Regarding the gate position, in the bottom gate structure, the gate insulator layer is formed before the organic semiconductor. Metal oxides with high dielectric constant, such as aluminum oxide that can be formed by treatment such as oxygen plasma, can be used for forming an insulator film [30–32]. Moreover, by adding additional surface treatments on insulator film such as self-assembled monolayer (SAM) [29], the characteristics and stability of OTFTs can be further improved.

The stacking of film layers, from the bottom to top, for fabricating an OTFT is as follows: gate metal (Al), insulator (AlO_x) and self-assembled monolayer (SAM), organic semiconductor, source-drain metal (Au), and passivation on a substrate material. The semiconductor materials are dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [33, 34] for p-type and 4,8-Bis[5-[3-(trifluoromethoxy)phenyl]-2-thienyl]-2$\lambda^4\delta^2$-benzo[1, 2-c:4,5-c']bis[1,2,5]thiadiazole (TU-1) [35] for n-type.

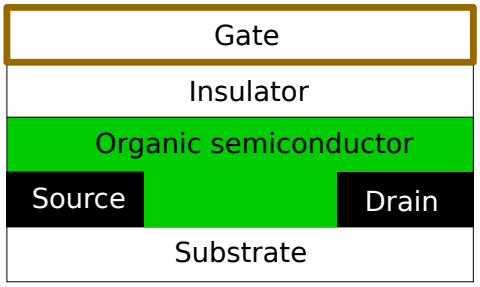
The OTFTs with the multifinger layout shown in Fig. 2.1(b) are used in this work. Since the feature size of OTFTs is relatively large, the transistor area should be as small as possible. Compared with the one finger layout, the transistor area and diffusion capacitance are reduced while maintaining the dimensions (channel width/ channel length) of the transistor [27,36]. Moreover, the channel width can be easily increased by adding the drain and source electrodes.



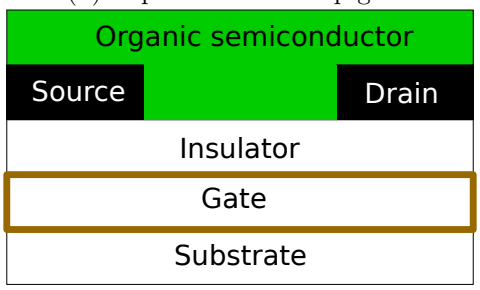
(a) Top contact and bottom gate.



(b) Top contact and top gate.



(a) Bottom contact and top gate.



(b) Bottom contact and bottom gate.

Figure 2.2: Structures of low voltage organic thin-film transistors.

2.2 Fabrication process of OTFTs

The fabrication process of the OTFTs used in this dissertation is introduced below, and a cross-sectional view of a device in each step is shown in Fig. 2.3. Although a printing process can be used for OTFTs fabrication, to maximize the performance of OTFTs circuits, more stable processes mainly depending on physical vapor deposition (PVD) are currently used. It takes about three days to complete the process.

Step-1 Gate electrode (Al) deposition

In a vacuum of about 5×10^{-4} Pa, Tungsten is used for the support of solid Al, and solid Al is heated and deposited by applying a 25 A current to Tungsten. After the deposition is finished, the Al is cooled in a vacuum for 30 minutes. The thickness of the deposited Al film is about 20 nm.

Step-2 Contact layer (Cr and Au) deposition

Since the gate electrode is at the bottom of the OTFTs, a contact layer is needed to connect the gate with the upper layer. Cr is used to improve the contact between Al and Au. In a vacuum of about 5×10^{-4} Pa, Cr and Au are deposited in that order with a current of 7 A. The thickness of the contact layer is about 40 nm.

Step-3 O_2 plasma oxidation of Al

Oxidation treatment with oxygen plasma for 30 minutes while supplying 0.2 L/min of oxygen. The gate electrode (Al) other than Via is oxidized to form AlO_x, which will be the insulator of the OTFTs.

Step-4 Self-assembled monolayer (SAM) generation

SAM is used to modify the dielectric interfaces to improve the characteristics of OTFTs. It can be produced by immersing the substrate in a solution of 33.4 mg Octadecylphosphonic acid (ODPA) [37] dissolved in 20 ml propanol for 2 hours. SAM is formed only on AlO_x by neutralization reaction. After SAM generation, the substrate is washed with propanol to remove excess ODPA and then heated to 120 °C to evaporate the moisture produced by the neutralization reaction during the SAM generation. The AlO_x and SAM operate as the insulator of OTFTs which is extremely thin, about 5 nm in total.

Step-5 Organic semiconductor deposition.

In a vacuum of about 1×10^{-3} Pa, semiconductor materials contained in the test cube are gradually heated and deposited. The deposition rate of semiconductors is important because it involves the formation of crystals, and is performed at a rate of about 0.3 Å/s. The deposition is terminated when the film reaches 30 nm thickness and then cooled in a vacuum for 30 minutes.

Step-6 Source/Drain, metal wire (Au) deposition

In a vacuum of about 5×10^{-4} Pa, Au is deposited with a current of 7 A. The thickness of all Au layers is about 30 nm.

Step-7 Parylene protective film formation

The parylene film is used to protect the OTFTs from environment-induced degradation. It is formed by the chemical vapor deposition (CVD) process. First, the furnace is heated to 690 °C and evacuated to 7 Pa. Then, 1 g parylene is set and heated to 175 °C to vaporize. Parylene in gaseous form at 175 °C is decomposed in the furnace at 690 °C and polymerized to form a film on an OTFT chip. Since the Parylene layer is used to protect OTFTs, it is relatively thick at about 600 nm.

Step-8 Hole opening for via

Holes are drilled on the parylene to connect the metal wire to the upper layer. The holes are generated by oxygen plasma for 30 minutes while supplying 0.2 L/min of oxygen.

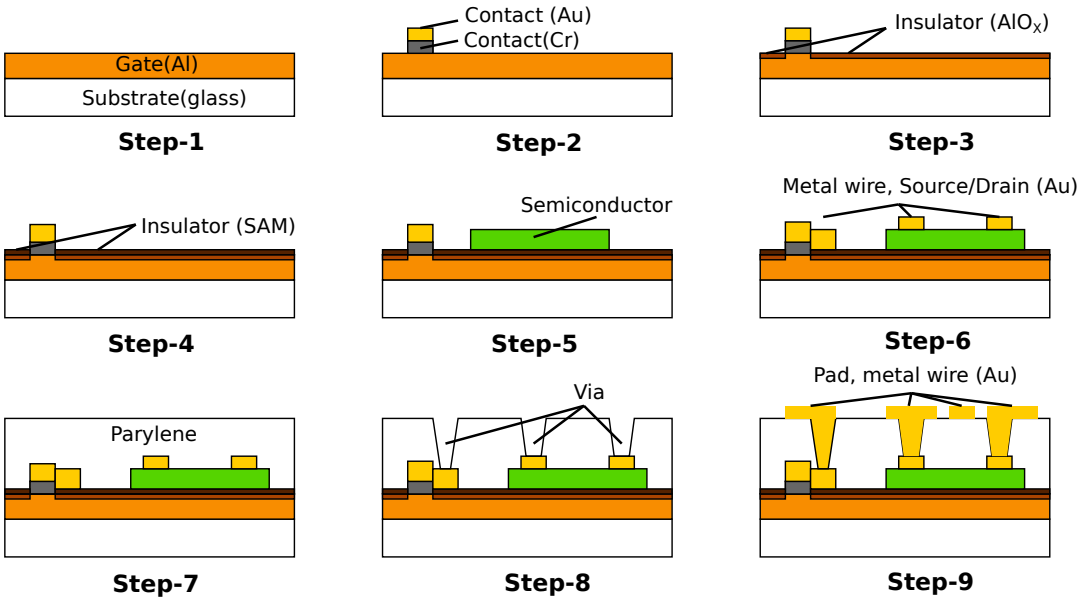
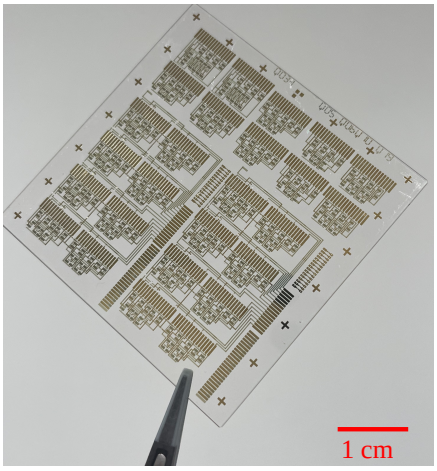


Figure 2.3: Fabrication process of OTFTs.

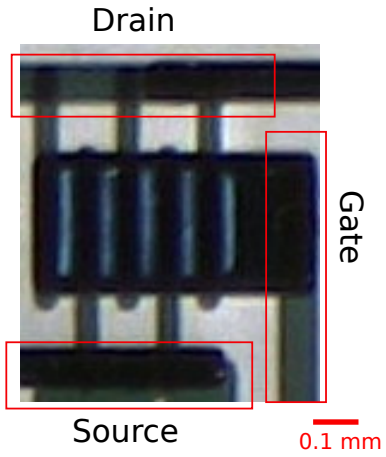
Step-9 Pad metal (Au) deposition

The pad metal is the top layer of the device. Probes contact the pad for measurement. In addition, for complex OTFT circuits, only one layer of metal wire is generally insufficient. The pad metal is also used for wiring purpose.

The OTFT chips in this dissertation are fabricated on a 5 cm× 5 cm glass substrate. By replacing the glass substrate with a plastic film, the OTFT circuits can also be fabricated on flexible film substrates. A photo of an entire chip and one OTFT is shown in Fig. 2.4. Thanks to an extremely thin insulator layer, which is about several nm, the OTFTs can be driven by a low supply voltage. However, it is inevitable that the thin insulator tends to have a problem of gate dielectric breakdown, decreasing the chip yield. To mitigate this problem, the use of the gate electrode layer is minimized and this layer is used only for the OTFTs gate, i.e., this layer is not used for wiring purpose. Most of the metal wires in circuits use the Au layer deposited in Step-6 and Step-9. The parylene layer with several hundred nm thickness has better insulation properties.



(a) Chip entire.



(b) Single OTFTs device.

Figure 2.4: Photo of a fabricated OTFTs chip. Substrate is a 5 cm×5 cm glass. A flexible film substrate can also be used.

2.3 Operation principle and device model of OTFTs

The OTFTs have a metal-insulator-semiconductor (MIS) structure and the operation principle is similar to Si MOSFET. For example, in n-type transistors, when the gate-to-source voltage (V_{gs}) is larger than the threshold voltage (V_{th}), the transistor turns ON and a channel is formed at the interface of the organic semiconductor and insulator. By applying a positive drain-to-source voltage (V_{ds}), carriers are injected from the drain and current begins to flow through the channel. When increasing V_{ds} to $V_{\mathrm{gs}} - V_{\mathrm{th}}$, the potential between the gate and the source is eliminated, the channel disappears and becomes pinched off. Above this voltage, the current is saturated and only controlled by V_{gs} regardless of V_{ds}. A simple Shockley model shown in Eq. 2.1 can express this operation [38] as,

$$
\begin{aligned}
I_{\mathrm{SAT}} =& \frac{\mu W C_i}{2L}(V_{\mathrm{gs}} - V_{\mathrm{th}})^2 \\
I_\alpha =& \begin{cases} I_{\mathrm{SAT}} & (V_{\mathrm{ds}} > V_{\mathrm{SAT}}) \\ I_{\mathrm{SAT}} \left(2 - \dfrac{V_{\mathrm{ds}}}{V_{\mathrm{SAT}}}\right) \dfrac{V_{\mathrm{ds}}}{V_{\mathrm{SAT}}} & (V_{\mathrm{ds}} \leqq V_{\mathrm{SAT}}) \end{cases}
\end{aligned}
\tag{2.1}
$$

where, the I_{SAT} and V_{SAT} are the pinch off current and voltage. On the other hand, Si MOSFETs and OTFTs use different electrodes, leading to differences

Table 2.1: Explanation of each parameter in OTFTs device model

Parameter	Explanation
$V_{\mathrm{SAT}}, I_{\mathrm{SAT}}$	Pinched off voltage, current
$W, L,$	Channel width, Channel length
C_{I}	Gate dielectric capacitance
$B, V_{\mathrm{B}}, K_\alpha, m_\alpha, n_\alpha, \lambda_\alpha, I_0, S$	Fitting parameters

in operation in the transistor OFF state. In Si MOSFETs, the leakage current is very small because a reverse electric field is applied to the pn junction between the drain and the source. In OTFTs, there are carriers with potentials exceeding the injection barrier of source metal to organic semiconductor. These carriers can inject into the organic semiconductor, resulting in a relatively large leakage current.

For accurate SPICE simulation, a high accuracy model is required. As described above, the operation of OTFTs can be explained by a similar principle as that of Si MOSFETs. A device model on the basis of Si MOSFET models has been proposed to describe the characteristics of OTFTs [39]. In this model, the on-current (I_α) model shown in Eq. 2.3 is represented by the alpha-power law [40], which is more accurate than the Shockley model. The current in the subthreshold region (I_{sub}), shown in Eq. 2.6, is expressed by the exponential function of V_{gs}. I_{sub} is caused by the diffusion current due to the charge density gradient between the source and the drain. I_α and I_{sub} are smoothly connected by the tanh function. The gate leakage current is expressed by I_{leak}. The explanation of each model parameter is shown in Table 2.1.

$$
\begin{aligned}
I_{\mathrm{D}} =& I_\alpha \frac{1}{2}\left[1+\tanh\left[B\left\{V_{\mathrm{gs}}-\left(V_{\mathrm{th}}(t)-V_{\mathrm{B}}\right)\right\}\right]\right] \\
&+ I_{\mathrm{sub}} \frac{1}{2}\left[1-\tanh\left[B\left\{V_{\mathrm{gs}}-\left(V_{\mathrm{th}}(t)-V_{\mathrm{B}}\right)\right\}\right]\right] + I_{\mathrm{leak}} \qquad (2.2)
\end{aligned}
$$

$$
I_\alpha = \begin{cases} I_{\mathrm{SAT}} & (V_{\mathrm{ds}} > V_{\mathrm{SAT}}) \\ I_{\mathrm{SAT}}\left(2-\frac{V_{\mathrm{ds}}}{V_{\mathrm{SAT}}}\right)\frac{V_{\mathrm{ds}}}{V_{\mathrm{SAT}}} & (V_{\mathrm{ds}} \le V_{\mathrm{SAT}}) \end{cases} \qquad (2.3)
$$

$$
V_{\mathrm{SAT}} = K_\alpha \left(V_{\mathrm{gs}}-V_{\mathrm{th}}(t)\right)^{m_\alpha} \qquad (2.4)
$$

$$
I_{\mathrm{SAT}} = \frac{W}{L} C_{\mathrm{I}} \mu \left(V_{\mathrm{gs}}-V_{\mathrm{th}}(t)\right)^{n_\alpha}\left(1+\lambda_\alpha V_{\mathrm{ds}}\right) \qquad (2.5)
$$

$$
I_{\mathrm{sub}} = I_0 \exp\left\{-\frac{\ln(10)}{S}\left(V_{\mathrm{gs}}-V_{\mathrm{th}}(t)\right)\right\} \qquad (2.6)
$$

2.4 Electronic characteristic of OTFTs

Generally, the OTFTs are almost unipolar that p-type is much stronger than n-type. Unlike Si MOSFETs using pnp or npn structure to form a channel, the OTFTs use n/p-type semiconductor materials. The carriers are produced by the energy level between the organic semiconductor and the source/drain. The highest occupied molecular orbital (HOMO) is used for p-type organic semiconductor and the lowest occupied molecular orbital (LOMO) is used for n-type organic semiconductor. The metals typically used for the source/drain, such as Au or Ag, have high work functions better suited for injection of holes into the HOMO than of electrons into the LUMO. Low-work-function metals such as Al or Mg, oxidize easily and readily form reactive complexes with the organic semiconductor, resulting in the degradation of both metal and organic semiconductor [38].

An example of the measured $I_\mathrm{d} - V_\mathrm{g}$ characteristics of the p-type and n-type OTFTs used in this thesis is shown in Fig. 2.5. These devices can be driven by a supply voltage of 3 V or lower [41]. The p-type transistors exhibit better performance than the n-type with more than 10x higher on-current and a significantly better on-off current ratio.

When compared to Si devices, OTFTs are relatively easier to degrade the performance due to bias-stress voltages and reactions with air humidity or oxygen [42–44]. Moisture diffuses into the organic semiconductor, capturing the carriers generated in the channel. This reduces the on-current and mobility. In addition, oxygen molecules oxidize the semiconductor, degrading the characteristic of OTFTs. The degradation affects the threshold voltage and mobility. The degradation model is expressed as shown in Eq. 2.7 [44]:

$$p(t) = \mathbf{P0} + \mathbf{A_P}\,(t - \mathbf{t_0})^{\mathbf{n_P}}\,, \tag{2.7}$$

where p denotes a model parameter that represents degradation, either threshold voltage (V_th) or mobility (μ). $\mathbf{P0}$ denotes the initial value, $\mathbf{A_P}$ and $\mathbf{n_P}$ denote degradation rate. Once degraded, it is difficult to fully recover to the original characteristic. In recent years, numerous efforts have been made to enhance the stability of OTFTs [9,10,45]. The environment-induced degradation can be suppressed via protection methods such as the application of an encapsulant on the top of the circuit. With the advancement of device materials and structures, the recent OTFTs can reportedly operate for approximately one year [46].

The bias-stress degradation is also a serious issue for low voltage OTFTs, under the conditions where devices are in static bias conditions. The degradation mechanism is considered as the trap of mobile charge carriers in the semiconductor channel formed on the gate dielectric. The trapped carriers lead to increased threshold voltage and decreased mobility, thereby, degrading

Table 2.2: Parameters of the degradation model of OTFTs in Eq. 2.8, Eq. 2.9, and Eq. 2.10

Parameter	Explanation
p	Model parameter for V_{th} or μ
δ_1	Degradation term
δ_2	Recovery term
$-A_{\mathrm{p}}, m$	Degradation rate
$-B_{\mathrm{p}}, n$	Recovery rate

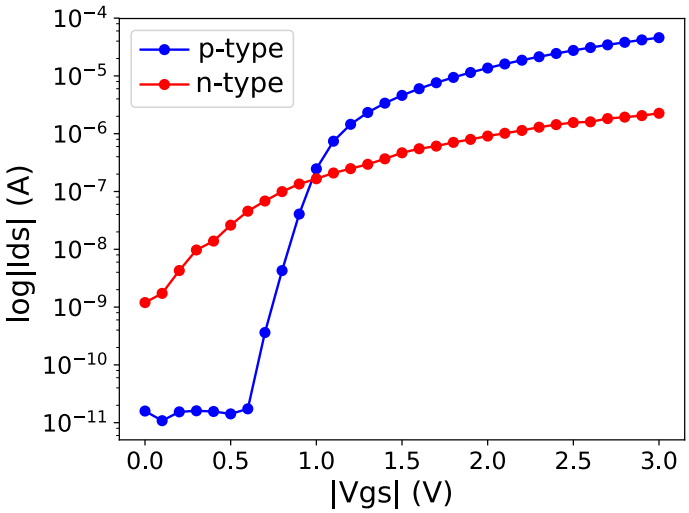


Figure 2.5: Drain current characteristics of p- and n-type OTFTs with a size of W/L=1200 μm/50 μm. V_{ds}=3.0 V. © IEEE 2022

the performance of the device [47]. The performance of the OTFTs is reported to recover when stress voltage is removed. The degradation and recovery model for the bias stress is represented as follows [20], and the explanation of each model parameter is shown in Table 2.2.

$$\Delta p(t+t_0) = \delta_1+\delta_2, \tag{2.8}$$

$$\delta_1 = \phi_{\mathrm{p}} \left(1-\exp\left(-A_{\mathrm{p}} t^m\right)\right), \tag{2.9}$$

$$\delta_2 = \Delta p(t_0) \left(1-\left(\frac{1-\exp\left[-B_{\mathrm{p}} t\right]}{1-\exp\left[-B_{\mathrm{p}}\left(t+t_0\right)\right]}\right)^n\right), \tag{2.10}$$

Chapter 3

Physical Unclonable Function using OTFTs

3.1 Introduction

With the advancement of IoT society, various IoT devices can now be connected to the internet. Securing data generated by IoT devices has become crucial. Among the vast areas of information security, authorization of hardware devices is one of the most important topics. For that reason, physically unclonable functions (PUFs) are attracting attention in the field of hardware security [21–24]. On the basis of physical variation during the manufacturing process, PUF generates identification information, which is random, unclonable, and unique to each chip. The challenge-response (input and output) of the PUFs can be used for authentication, encryption, etc [48–50].

Physically unclonable function circuits using OTFTs [1, 2] are the prospective candidates for use with IoT sensors. Moreover, OTFT PUFs can be implemented in RFID tags or with flexible sensors to improve the security of the communications that those devices establish. Besides hardware devices, OTFT-based PUFs can also be used for the packaging of merchandise. By printing on the surface of packaging materials, OTFT PUFs can be used for various purposes, such as delivery tracking or expiration date control.

In this chapter, we propose a new PUF circuit, organic current mirror PUF (OCM-PUF), which is suitable for fabricating using OTFTs. In recent years, numerous efforts have been made to enhance OTFT stability and considerable progress has been achieved [9–11]. However, the deterioration of organic devices leading to the degradation of circuit performance is still a serious issue in OTFTs [39, 46, 51]. Considering the performance and the stability of OTFTs available today, we take the simplest approach to construct the organic PUF.

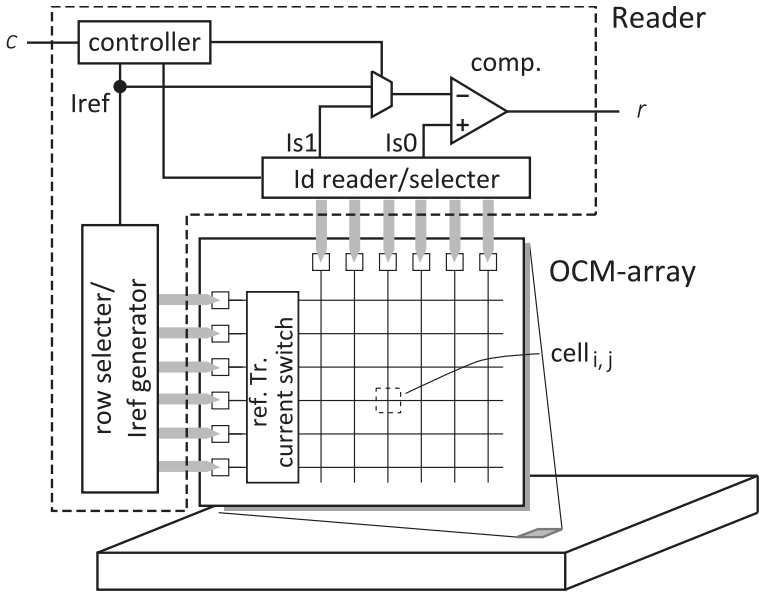


Figure 3.1: OCM-array as an OCM-PUF, and its use model. © IEEE 2020

The conceptual illustration and the usage model of the proposed OCM-PUF are shown in Fig. 3.1. In this example, the PUF is printed as an organic current mirror array (OCM-array) on the surface of merchandise, such as a smartphone or grocery packaging. The printed array serves as a serial number and/or expiry date associated with it [52]. When in use, a reader device first accepts challenge c to apply for the OCM-array. The OCM-array outputs the corresponding response r. The challenge and response pairs are then compared with those taken at the time of packaging and stored in the database. We fabricate the proposed PUF to experimentally evaluate its performance [53].

Compared with the existing PUFs that use OTFTs such as SRAM PUF [54] or Arbiter PUF [55] the circuit structure of the proposed PUF is simpler. Therefore, a stable circuit operation is expected even if the circuit is fabricated using OTFTs. The response of the proposed OCM-PUF is determined by the current variation of each device. Moreover, the salient feature of the proposed PUF is its resilience against device degradation. As described in Chapter 2, device degradation is an unavoidable problem of OTFTs. In PUF circuits, since the short actual operating time, the degradation over time is dominant rather than bias-stress degradation. The proposed PUF achieves self-compensation against device degradation by utilizing the current mirror structure.

In this chapter, two types of OCM-PUFs are proposed and thoroughly evaluated: one that aims for area efficiency [56] and one that pursues improved robustness in the systematic variation. Through the test-chip fabrication and measurements, the advantages and disadvantages of the two proposed

PUFs were compared, and the PUF metrics of the proposed OCM-PUFs were quantitatively evaluated.

The rest of this chapter is organized as follows. In Sec. 3.2, preliminaries of PUFs, and organic PUFs are introduced. Then, in Sec. 3.3, the circuit structure and its operation of the proposed OCM-PUF are presented. The proposed circuit is evaluated through test chip measurements as presented in Sec. 3.4. Finally, we conclude this chapter in Sec. 3.6.

3.2 Background

3.2.1 Physically unclonable function

The PUFs exploit the manufacturing process variation to generate unique information for each instance. The PUFs are expected to be widely used in the authentication and key generation for common key cryptosystems [57]. It can be embodied in physical structure and is easy to evaluate, however, difficult to predict and duplicate.

The general operation of the PUF is pictorially illustrated in Fig. 3.2. A PUF works as a function f that returns a response $r = f(c)$ for a challenge input c. Here, the function f of a PUF is non-deterministic and chip-dependent because it depends on the physical variation of the hardware circuit. This property is achieved by simply using the same usual layout and fabrication. However, each PUF acquires its own unique challenge-response pairs (CRPs) because they are determined by physical variations that are beyond the control of manufacturing equipment. Because manufacturing variation is the source of the random response, cloning the function f is impossible even by the manufacturer of the PUF. In other words, the PUF circuit is designed, so that the chip-dependent manufacturing variability is enlarged and becomes observable. At present, authentication and secure key generation are the two primary applications of PUFs. Two categories of PUFs exist: *strong* PUF and *weak* PUF [58]. The strong PUFs own an exponentially large number of CRPs and are typically used for authentication. The weak PUFs have a limited number of CRPs and are typically used for key generation.

In conventional common-key cryptosystems, keys are stored in non-volatile memory within a chip. However, safely managing keys in memory is difficult and expensive. The invasive attack can extract the digital key stored in the memory. In order to achieve a higher level of security, additional tamper-sensing circuitry has been required to protect memory [57], which may become costly. By using PUFs, secret keys can be derived from the physical characteristics of the circuit at a lower cost than storing keys in memory [59].

In addition, PUFs can be used in the authentication process. As shown in Fig. 3.3, we may consider the authentication between Alice and Bob. In the PUF-based authentication, a large number of CRPs were collected and stored in a secure database and then the PUF was securely passed to Bob before communication. After this setup, Alice chose a CRP(c,r) from the CRP database and sent the challenge to Bob. When Bob received the challenge, a response r_α obtained from the PUF was returned to Alice. Bob will verify the response r by whether it matches r_α or not.

The performance of PUF can be evaluated using randomness and reliability metrics [60]. The randomness represents the balance of 0's and 1's in the response. It can be defined as follows:

$$\text{Randomness} = -\log_2\left(\frac{1}{2} + \left|\frac{1}{C}\sum_{c=1}^{C} r_c - \frac{1}{2}\right|\right), \tag{3.1}$$

where r_c and C are the responses to challenge c and the maximum number of challenge c, respectively. The reliability is a metric that indicates whether a PUF always returns the same response to the same challenge. The reliability can be estimated by calculating the ratio of the response change as follows:

$$\text{Reliability} = \frac{\text{Changed bits}}{\text{Total bits}}. \tag{3.2}$$

The reliability metric can be used for the evaluation of the effectiveness of the aging compensation. Both metrics assume a value between 0 and 1, where 0 is the worst, and 1 is the best.

A changing response is considered an error response. Decreasing the error rate is critical in designing PUFs using organic devices. The responses of a PUF can change with the change in environmental conditions. Typically, the error, observed as a bit-flip, can be corrected by an error-correction code (ECC) [57]. However, a PUF with a very high error rate will result in an impractically large ECC. In the worst-case scenario of observing considerable randomly occurring errors, the generation of ECC becomes infeasible. It has been reported in [61] that an error rate higher than 25% can make using ECC entirely impractical.

3.2.2 Organic thin-film transistor PUF

Thus far, several PUFs using OTFT devices have been proposed. These techniques have successfully realized the functionality of PUFs. However, there remains room for improvement before their practical application, particularly in terms of the stability of the responses.

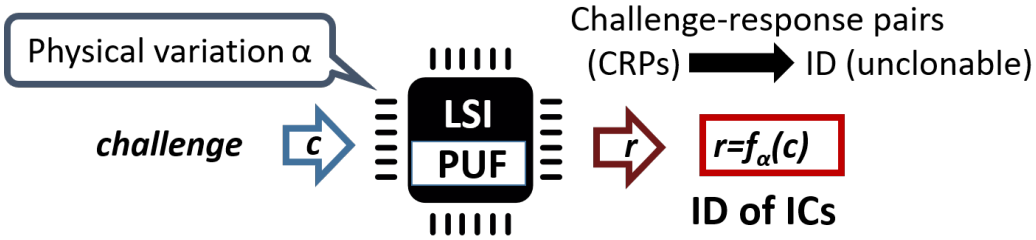


Figure 3.2: Typical use of PUFs. © IEEE 2020

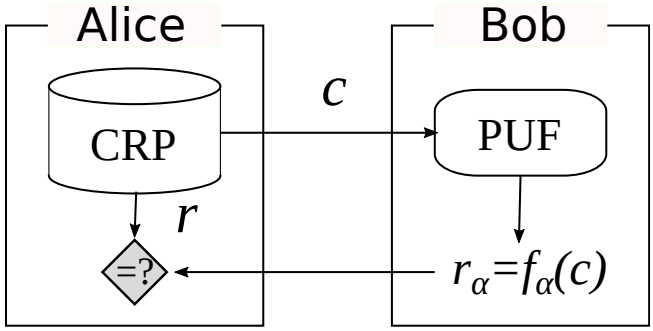


Figure 3.3: Example PUF-based authentication. © IEEE 2020

The ring oscillator (RO) PUF [1] shown in Fig. 3.4 utilizes the frequencies of ROs. The frequencies of two selected ROs have been compared to generate a response. Due to the variation in transistors, each RO has different frequency. Hence, the response is unique. Fig. 3.5 shows the construction of the buskeeper PUF [2] which uses a pair of cross-coupled inverters to generate a response. After applying supply voltage, the value of cross-coupled invert is random mainly depending on the threshold voltage of internal transistors. The Buskeeper PUF in [2] is reported to be more tolerant to environmental changes than RO PUFs. However, the responses of the PUF are easily affected by the temporal degradation of the OTFT, decreasing the reliability of the PUF.

In these PUF implementations, several transistors have been used to generate a response bit. In the case of the buskeeper PUF, without considering the access transistors, four OTFTs are used to construct one cell. A RO PUF requires an even larger number of transistors than the buskeeper PUF. As the area of the PUF becomes larger, there will be a greater chance of observing device failure. The large area may also lead to non-uniformity of the device performance. Since the size of the OTFT devices is much larger than that of silicon devices, it would be desirable to shrink the circuit area to as small as possible. For assumed applications of organic PUF, such as smart packaging or authentication of organic IoT sensors, the desirable circuit area would be

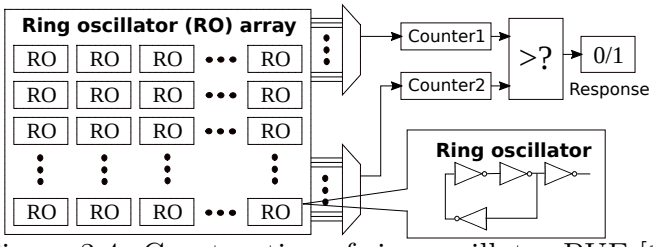


Figure 3.4: Construction of ring oscillator PUF [1]

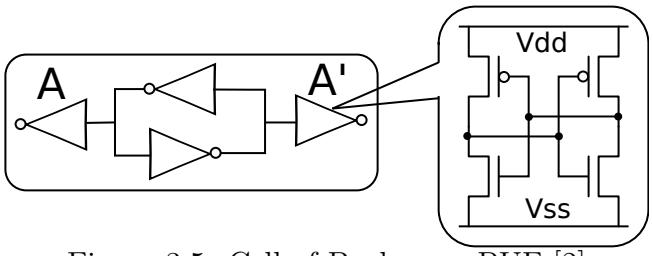


Figure 3.5: Cell of Buskeeper-PUF [2]

less than a few square centimeters. Moreover, higher cell density increases the available number of PUF bits for a given area. This leads to a higher security level [53]. In our organic PUF design, area efficiency and stable performance against aging are the two main objectives.

3.3 Organic current mirror array

3.3.1 Circuit architecture

Here, we propose two designs of current mirror arrays (CMAs): CMA1 and CMA2. The CMA is the integral component of the OCM-PUF.

The schematic diagram of CMA1 is depicted in Fig. 3.6. The construction of the circuit is simple and area-efficient. An elementary cell contains only one transistor, each of which is paired with the reference transistor. The transistors in the same row share a common gate-source voltage V_{g} that is generated using the reference transistor with the current input at the reference electrode, I_{ref}. Here, the reference transistor is the leftmost one in each row. In the example in Fig. 3.6, the entire PUF contains n rows. The current applied to the reference transistor was copied to all transistors in the same row, which shared the same gate voltage. The reference current and that of the cell will be compared to generate an output bit. The drain terminals of the transistors in the same column share the output electrode, $I_{\mathrm{d}i}$ at the top. In the measurement, the current is applied to a selected row, and the currents from all cells are measured

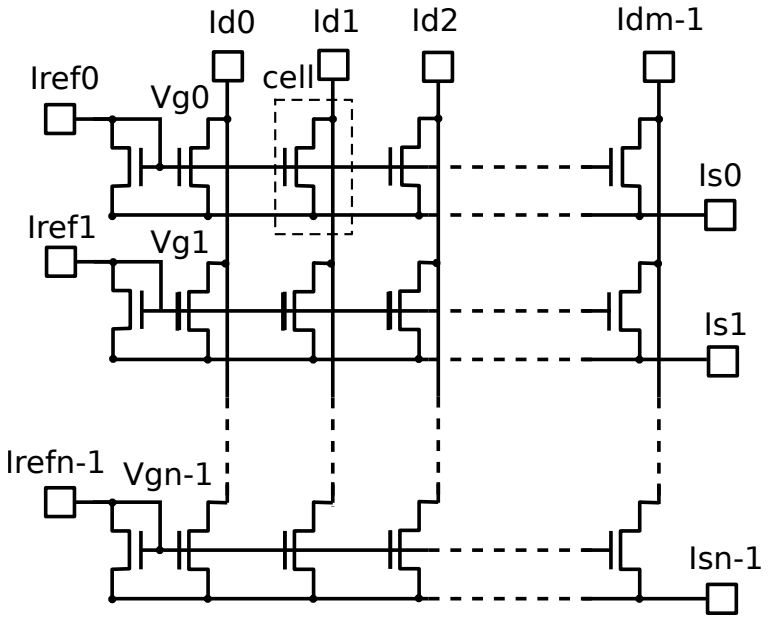


Figure 3.6: Schematic diagram of OCM-PUF1. © IEEE 2020

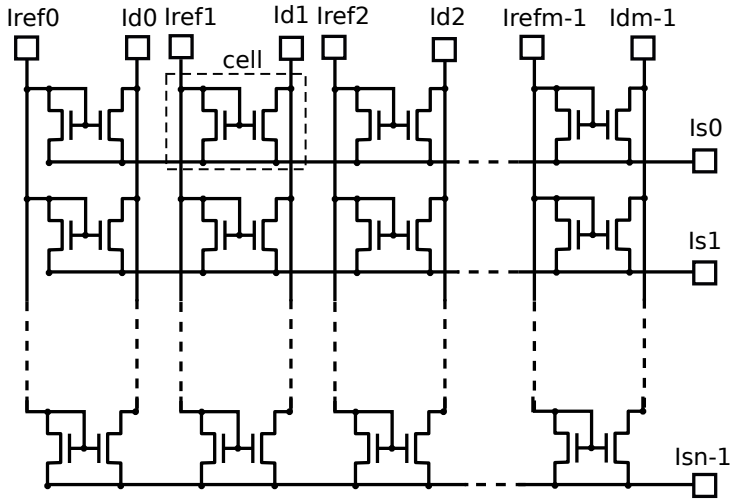


Figure 3.7: Schematic diagram of OCM-PUF2. © IEEE 2020

in parallel. In this construction, the size of the reference transistor should be designed using a large area so that its threshold voltage approaches the mean value through the averaging effect. The deviation of the threshold voltage from the mean value will lead to bias in the row responses.

In order to reduce bias in the response distribution, we propose another circuit, CMA2, depicted in Fig. 3.7. This circuit is robust for the systematic variation as one cell in the array consists of one current mirror pair. The

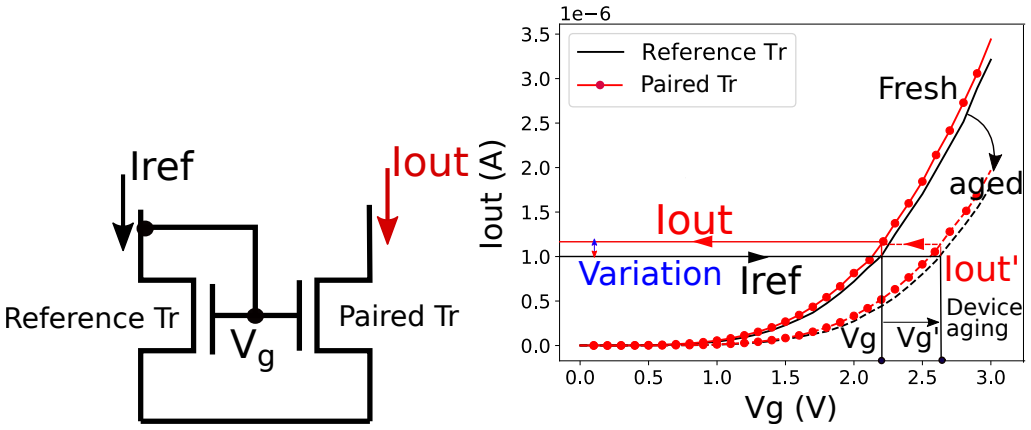
voltage and reference current had been given to the gate and source electrode of the selected cell, and we measured the drain electrode, which gave the output current of the array.

CMA2 occupies a larger area because a cell contains two transistors; however, CMA1 contains only one, which is set aside a shared reference transistor. However, CMA2 may avoid the issue of bias and be expected to generate more balanced outputs than CMA1. In CMA1, the transistors in the same row share the gate voltage of the reference transistor. If the reference transistor suffers a failure, which occurs in a fixed probability in proportion to the area and is unavoidable in the current state of organic transistors, all the outputs in that row may become unavailable. Similarly, any faults, such as the gate leakage of the transistors in the cell, may change the shared voltage, which may cause bias in the row response, even if it does not kill the entire row. In the case of CMA2, the reference transistor is distributed inside each cell, and all the cells in CMA2 are independent. Thus, CMA2 is expected to be robust for random faults in any of the transistors.

We measured the currents for both CMA1 and CMA2 at the drain electrode, which provided the output current of the array. If all transistors in the array are equal, meaning I-V characteristics are completely identical, the output currents become exactly equal to the reference current. In practice, due to unavoidable manufacturing variability, the output current varies from transistor to transistor. Since the current is unique for each OTFT, this difference can be utilized as the chip signature. In order to obtain a response bit, the output current of a transistor was compared with the reference current, or the output currents of two transistors were compared.

Owing to the adoption of the current mirror structure, both CMA1 and CMA2 should compensate for the temporal degradation of organic devices. The OTFTs are known to age fast [46]. Air moisture penetrated into the organic semiconductor gradually increases the threshold voltage of the device and then decreases the drain current. In other PUF circuits, decreased drain current deteriorates the circuit performance, changing the response of the PUF. In the proposed current mirror structure, the threshold voltage degradation in the reference transistor was compensated by an increase in the gate voltage, V_{gs}. Because the reference transistor and those in the OCM-array age at a similar speed, the response of the PUF shall not change.

Fig. 3.8 depicts how compensation is achieved in the current mirror circuits. When a current I_{ref} is given to a reference transistor, the output current I_{out} is determined by the paired transistor at a gate voltage V_{g} that is generated by the given I_{ref}. If the characteristics of the paired transistors are identical, the output becomes a copy of the reference current. Practically, because of the variation during the manufacturing process, a slight difference will exist between I_{out} and



(a) Current mirror (b) Current compensation

Figure 3.8: Current compensation in the current mirror circuit. © IEEE 2020

I_{ref}. As time passes, because of the aging of the transistors, the gate voltage changes from V_{g} to V_{g}'. Since the device ages at a similar rate in two transistors, the relative current magnitude of the output I_{out}' to the reference current will remain the same as that when the transistors are fresh. This compensation can be externally observed as the increase of the shared gate voltage.

3.3.2 Operation as a PUF

The OCM-array can be used as a PUF of different configurations. By changing the setting in the reader circuit, it can operate as either a weak PUF or a strong PUF.

In the weak PUF mode, an OTFT cell is selected according to a given challenge. The current of a selected OTFT is measured to compare with its reference current within the reader circuit, as shown in Fig. 3.1. Due to the threshold voltage variation of the OTFT, the output current distributes about the given reference current. The comparator output then becomes a random bit. The whole array circuit will show a digital signature based on the digital response in each cell. This digital signature can be seen as the response of PUF.

By changing the configuration of the reader, the OCM-array can be used as another type of PUF, having larger CRP space than the weak PUF mode. In this mode, two transistors are selected, and the currents of the two transistors, I_{s0} and I_{s1} were compared to generate a response bit. Though the CRP space was not exponentially large, this mode expanded the challenge space to the number of transistors squared.

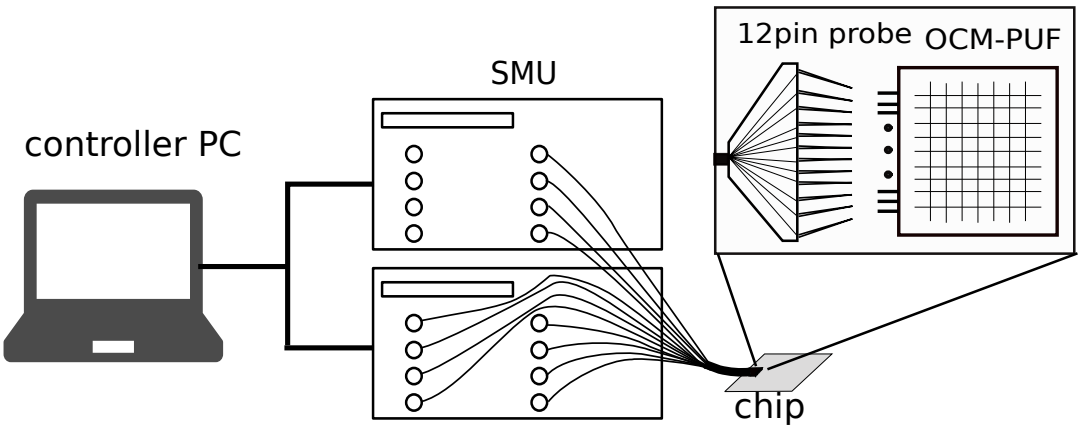


Figure 3.9: The measurement environment. © IEEE 2020

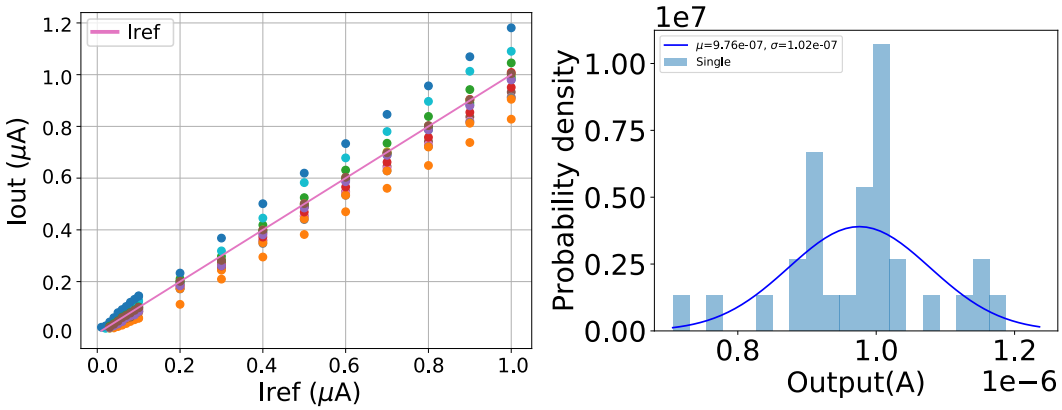
3.4 Experimental Results of OCM-array

The proposed two OCM-PUFs were evaluated through the fabrication and measurement of test-chips. The measurement setup is depicted in Fig. 3.9. We used a 12-pin probe to connect the electrodes of the array circuit to the semiconductor parameter analyzers. The bias-voltage adjustment, reference current application, and output current measurements were automated by a controller PC. Each terminal was controlled independently by an SMU channel.

3.4.1 Current mirror

Adequate amount of literature has not reported on the actual operation of OTFT-based analog circuits [12, 62] such as a current mirror. Hence, before evaluating the operation of the OCM-arrays, we first evaluated the characteristics of the stand-alone current mirror transistor pairs. The number of current mirror circuits measured was 16 for the n-type. The channel length and width of the OTFTs were 50 μm and 1200 μm, respectively. The reference current was altered from 0 A to 1 μA, while the drain-source voltage was fixed at 3 V for the n-type transistor.

The measured current mirror characteristics are shown in Fig. 3.10(a). The output currents were distributed per the given reference current, demonstrating that the OTFT-based current mirror copies the reference current. Fig. 3.10(b) shows the output current distribution when the reference current is $I_{\mathrm{ref}} = 1\,\mu$A. Although the number of OTFTs is small, it shows that outputs follow a normal distribution. Therefore, the current mirrors operated as expected and the variation can be used for PUF.



(a) Transfer characteristics of current mirror pairs.

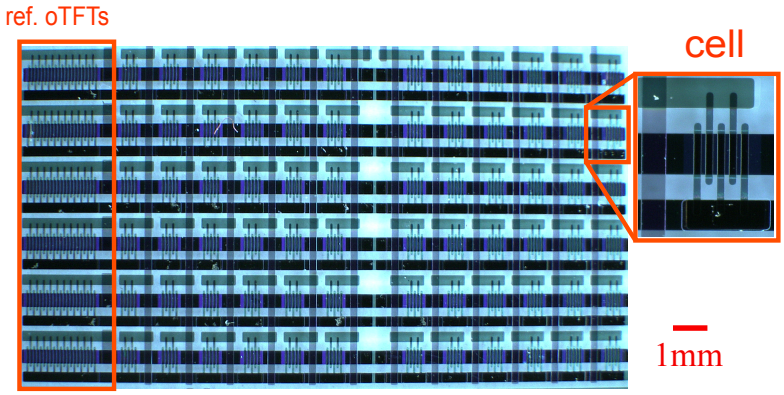
(b) Variations of the output currents at $I_{\mathrm{ref}} = 1\,\mu\mathrm{A}$.

Figure 3.10: Measurement results of n-type current mirrors. © IEEE 2020

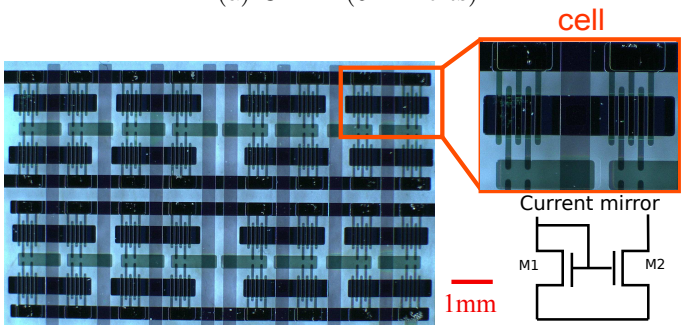
3.4.2 OCM-array

We then fabricated the two types of the proposed OCM-PUF arrays. The microphotographs of CMA1 and CMA2 are shown in Fig. 3.11. The channel length and width of the OTFT in the array were $50\,\mu$m and $1600\,\mu$m, respectively. Considering the circuit area and the measurement equipment, we fabricated one CMA1 that contained 6×12 cells and two CMA2s, each of which contained 4×4 cells. The reference transistor in CMA1 was designed to be five times the width of the transistors in the cells to ensure that its threshold voltage approached the mean value. In our fabricated devices, defects, mostly pinholes, were often found in the dielectric layer of the devices. They caused short circuits between the gate and drain or the source electrodes. In the case of CMA1, since the OTFT in the same row shared a common reference transistor, the existence of such a defect mode made the other cells in that row inoperable as the short circuit changed the shared gate voltage. On the other hand, in the case of CMA2, because all the cells were independently designed, such defects could only affect a paired transistor within a cell. Eventually, the CMA1 contained 3×12 measurable cells and CMA2 contained 30 measurable cells. The areas of CMA1 and CMA2 were $2.43\,\mathrm{mm}^2$/cell and $3.58\,\mathrm{mm}^2$/cell, respectively. In the unit area calculation of CMA1, the area of the shared reference transistors was included.

Fig. 3.12 plots the measured output of the two types of OCM-arrays. For both types of OCM-arrays, the drain-source voltage of the selected row is set to 3 V, while the reference current is swept from 0 A to $1\,\mu$A. Through this experiment, we can see that the cell in the array can operate as the current

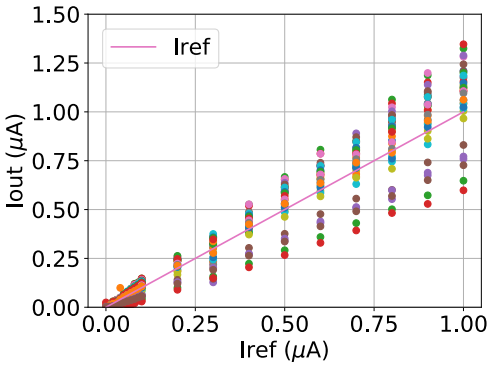


(a) CMA1 (6×12 bits)

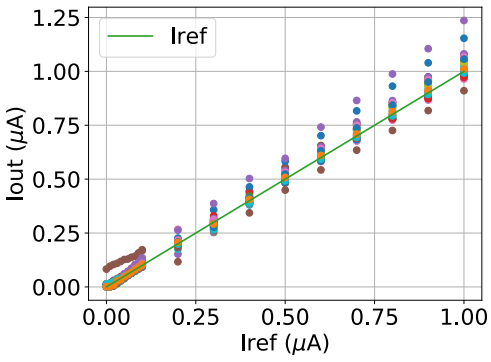


(b) CMA2 (4×4 bits)

Figure 3.11: Microphotographs of the two types of OCM-PUF fabricated. © IEEE 2020



(a) CMA1



(b) CMA2

Figure 3.12: Transfer characteristics of OCM-PUF. © IEEE 2020

mirror.

When operating the proposed OCM-array in the Weak PUF mode described in 3.3.2 it is necessary to determine the reference current for the response by

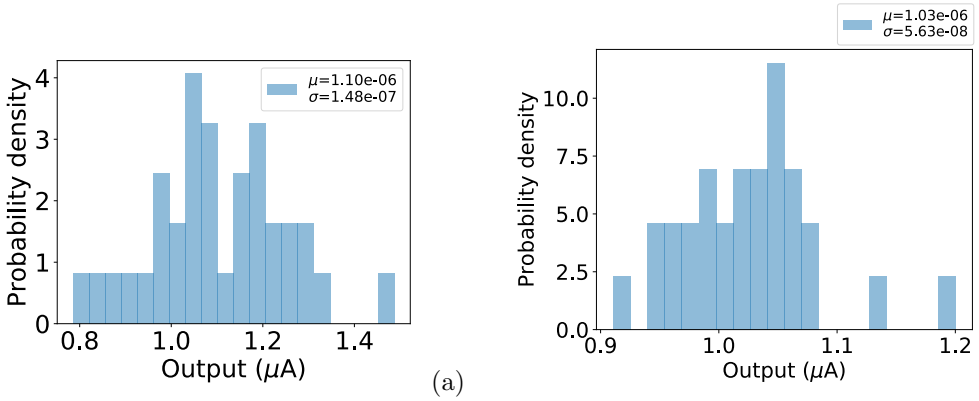


Figure 3.13: Variation of output current when$I_{\text{ref}} = 1\,\mu$A. © IEEE 2020

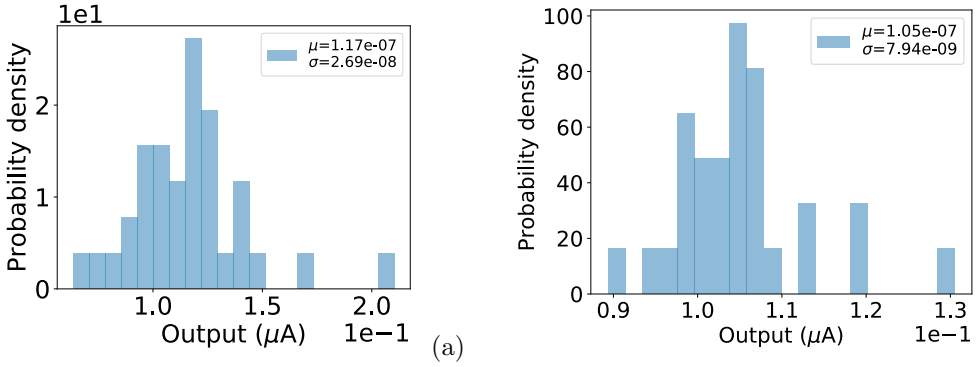


Figure 3.14: Variation of output current when$I_{\text{ref}} = 0.1\,\mu$A.

comparing the output current with the reference current. The output distributions are shown in Fig. 3.13 and Fig. 3.14 when the reference currents(I_{ref}) are $1\,\mu$A and $0.1\,\mu$A. For both conditions, the output currents follow a normal distribution. When the $I_{\text{ref}} = 1\,\mu$A, the average current output is relatively close to the reference current. The reason that the average current is slightly larger than the reference current is considered to be due to the leakage current between the gate and drain of the current mirror. There is a potential difference between the gate and drain, where a small leakage current is generated. Therefore, when using the current mirror as a PUF, the reference current to generate the response must be large enough to mitigate the effect of small gate leakage currents. Hereafter, this work use $I_{\text{ref}} = 1\,\mu$A to generate the response.

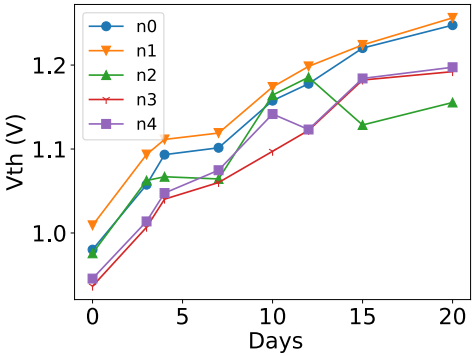


Figure 3.15: Temporal threshold voltage change of OTFTs in CMA1. © IEEE 2020

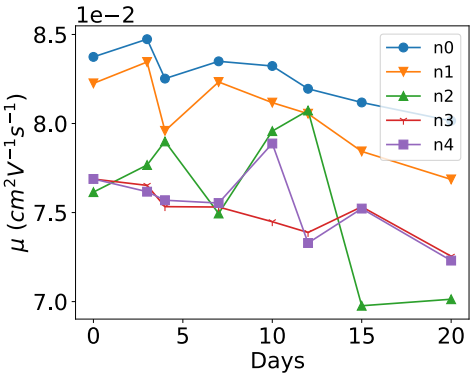


Figure 3.16: Temporal mobility change of OTFTs in CMA1. © IEEE 2020

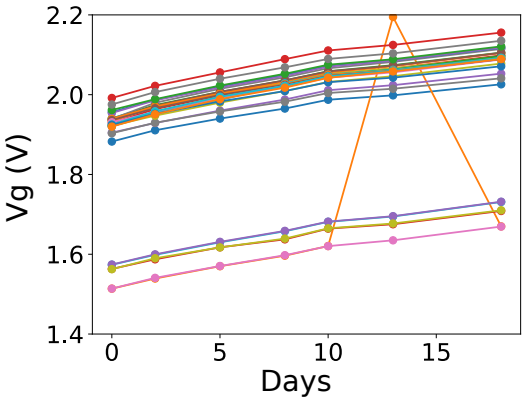


Figure 3.17: Temporal gate voltage change of current mirrors in CMA2. © IEEE 2020

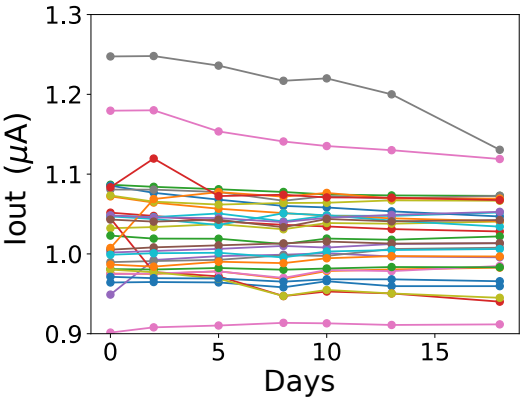


Figure 3.18: Temporal output current change of current mirrors in CMA2. © IEEE 2020

3.4.3 Resistance to degradation

As explained in Sec. 3.3.1, the current mirror structure may compensate for aging if paired devices age at a similar rate. To determine the degradation rate, we measured the temporal changes of the threshold voltage and the mobility of the randomly selected OTFTs, as shown in Figs. 3.15 and 3.16. Through direct probing, I_{di}-V_g characteristics of the OTFTs in CMA1 were measured. For better visibility of the figures, we have limited ourselves to present the results for only five OTFTs. However, a similar trend was observed for other OTFTs. The threshold voltage was derived through a constant current method at 0.1 μA, while mobility was calculated through extracting the gain factor. Both threshold voltage and mobility shifted temporally.

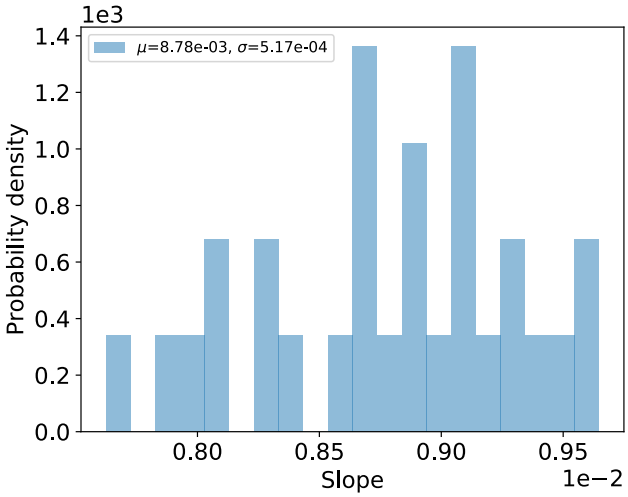


Figure 3.19: Variation of threshold voltage change.

In addition, to confirm the degradation rate of the device, we measured the temporal changes of the gate voltage in CMA2 as shown in Fig. 3.17. For simplicity, we use the simple Shockley model Eq. 2.1 in Sec. 2.3 to represent the device's characteristic

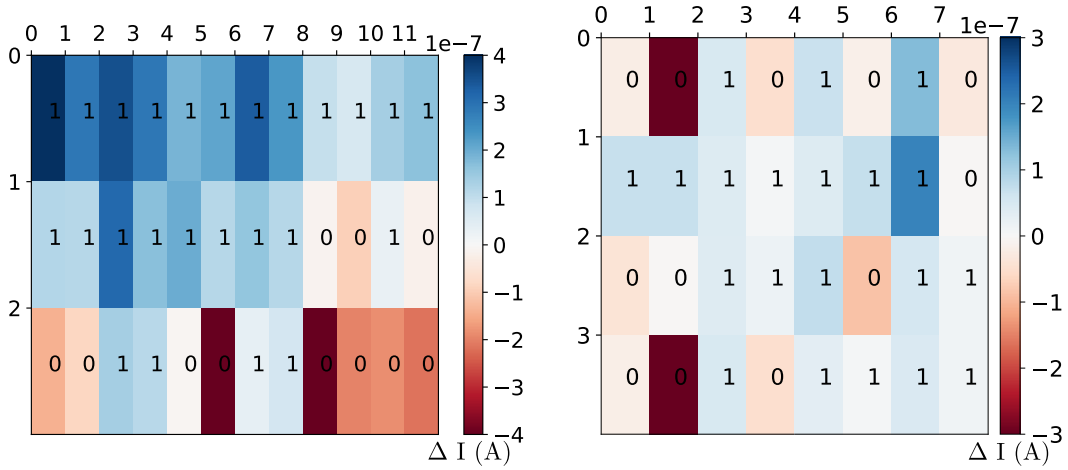
$$I_{\mathrm{d}} = \frac{\mu W C_i}{2L}(V_{\mathrm{gs}} - V_{\mathrm{th}})^2 \tag{3.3}$$

The gate-source voltage V_{gs} is obtained as

$$V_{\mathrm{gs}} = \sqrt{\frac{2LI_{\mathrm{d}}}{\mu W C_i}} + V_{\mathrm{th}} \tag{3.4}$$

As can be seen from the equation, V_{gs} reflects the degradation of threshold voltage and mobility of the reference transistor. Fig. 3.18 shows that most of the reference transistors age at a similar rate.

To quantify this rate, the slope of the V_{gs} change was determined for all devices, and a histogram is shown in Fig. 3.19. The average and standard deviation of the data are $8.78{\times}10^{-3}$ V/day and $5.17{\times}10^{-4}$ V/day respectively. Hence, V_{gs} changes only $5.17{\times}10^{-4}$ V compared to the average value. From the simulation results, the output current changes only 0.67% when V_{gs} changes by $5.17{\times}10^{-4}$ V at the operating voltage of in the current mirror. As shown in Fig. 3.14, which shows the variation of the CMA2 output, the difference between the output current and the average is within 5.63×10^{-8} A. This is about 5% of the average value. The amount of change due to variation in V_{gs} increase rate is 0.67%, which is sufficiently small compared to the 5% change due to device



(a) CMA1 (b) CMA2

Figure 3.20: Digital signatures and current difference ΔI. © IEEE 2020

Table 3.1: Randomness of the digital signature © IEEE 2020

	CMA1	CMA2
Overall	0.53	0.75
Ave of rows	0.33	0.74

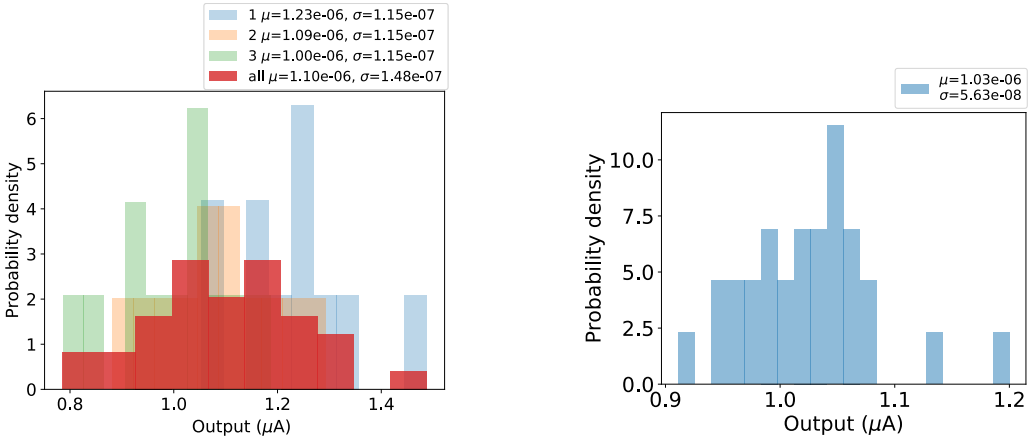
variation. These results indicate that the organic transistors degrade at about the same rate and the change in current is small.

Furthermore, to highlight the effectiveness of applying a current mirror structure, we plotted the output currents of the current mirror in Fig. 3.18 with the same axes as Fig. 3.17. By comparing the two figures, we noticed that even with the performance degradation of the transistors, which can be recognized by the gradual increase of the gate voltage, all of the output currents maintained about the same value. This also indicates that the current magnitude relative to the reference current was unchanged. From these results, the proposed OTFT-based current mirror array successfully compensates, to a large extent, for the effect of device aging.

3.5 The evaluation of OCM-PUF

3.5.1 Randomness

This section evaluates the metrics of the proposed OCM-array used as OCM-PUF. Firstly, Randomness is evaluated, which is the ratio of 0's and 1's in the response. If the ratio of 0's and 1's is exactly, Randomness is 1.



(a) CMA1 (b) CMA2

Figure 3.21: Variations of the output currents at $I_{\mathrm{ref}} = 1\,\mu$A. © IEEE 2020

We used $I_{\mathrm{ref}} = 1\,\mu$A as the reference current to generate responses, at which, the effect of the gate leakage current was ignorable. The response was determined as 0 when the current of the selected cell was larger than I_{ref}, and otherwise 1. For CMA1 in Fig. 3.6, a digital signature, or a response map, was obtained as shown in Fig. 3.20. The current difference between the reference and the output was indicated in the same figure using the color of the cells. In Fig. 3.20(a), we see runs of 1's or 0's in the first and the third rows. In these rows, the respective reference transistors happened to be strong and weak, compared with the reference transistors in other rows. We calculated randomness using Eq. (3.1) of two digital signatures. In order to evaluate the runs of 1's or 0's, we also calculated the average randomness of each row. The result is shown in Table 3.1. The table shows that the signature of Fig. 3.20(b) shows higher randomness than Fig. 3.20(a). The randomness was further backed up by Fig. 3.21, which shows the output current distribution at $I_{\mathrm{ref}} = 1\,\mu$A. Moreover, the output currents mostly follow a normal distribution. In Fig. 3.21(a), besides the distribution of all outputs, we also presented the distribution of each row. It demonstrated that each row had the same variation and a different average, meaning that the rows' output was strongly affected by the reference transistors. However, in CMA2, the reference transistors were distributed in each cell. The cells in CMA2 were independent so that CMA2 showed higher randomness.

3.5.2 Reliability

We evaluated the reliability metric using Eq. (3.2) in Sec. 3.2.1 of the proposed OCM-arrays as a stronger PUF. Reliability is an important metric in our PUF,

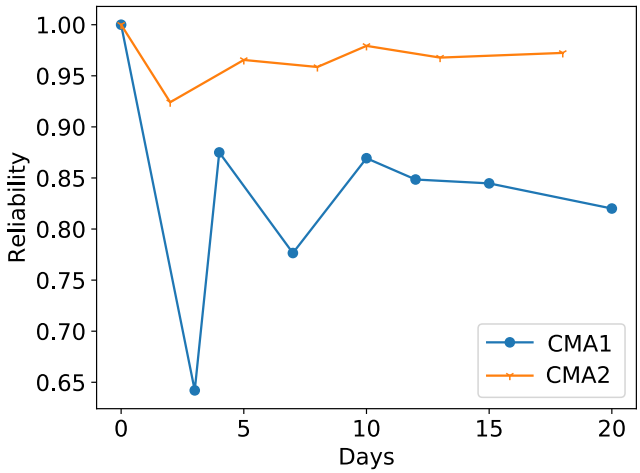
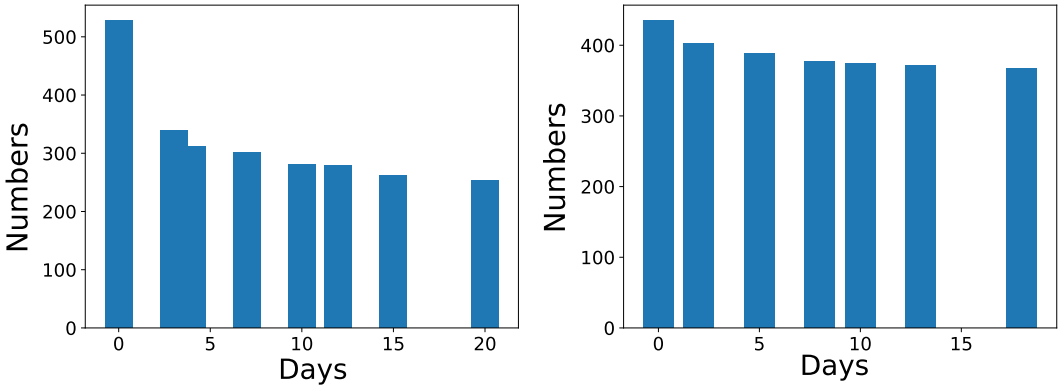


Figure 3.22: Temporal changes of reliability. © IEEE 2020

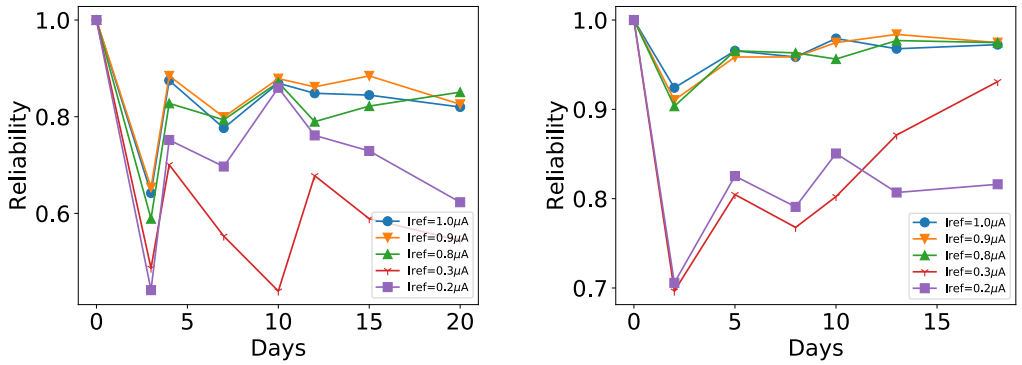


(a) CMA1 (b) CMA2

Figure 3.23: Number of unchanged responses. © IEEE 2020

as it indirectly indicates the effectiveness of aging compensation. Furthermore, we calculated the change in metrics over time. The change in reliability is shown in Fig. 3.22. Even with the degradation of the device, the metric of the reliability maintained a high level, and the reliability of CMA2 remained above 90%.

Fig. 3.23 shows the number of unchanged responses for approximately three weeks. From the results, we can see that only half of the responses in CMA1 could be used over time. By contrast, in CMA2, nearly 85% of the responses could be used. As described in Sec. 3.2.1, although the changing responses can be corrected by the error correction code (ECC), the low reliability of CMA1 will cause too large of an ECC circuit. Therefore, CMA2 is more practical for



(a) CMA1 (b) CMA2

Figure 3.24: Reliability change due to differences in reference current.

implementation.

3.5.3 Reference current

From the single current mirror measurement in Sec. 3.4.1, it is found that the output is affected by a small gate-drain leakage current, when the reference current is small. The reference current I_{ref} is set to 1 μA, which is the maximum reference current in this measurement. Considering other factors such as power consumption, I_{ref} can be set freely. In this section, we discuss the best I_{ref} in terms of reliability.

We measure output current by changing the input currents from 0 μA to 1 μA in increments of 0.1 μA. Several input currents (1 μA, 0.9 μA, 0.8 μA, 0.3 μA, 0.2 μA) are selected as reference currents to obtain the response and to calculate the reliability with the pass of time. The results are compared with the reliability at I_{ref}=1 μA to determine a proper reference current.

The results are shown in Fig. 3.24. When the reference current is relatively high (I_{ref}=0.9 μA/0.8 μA), the change in reliability is almost the same as I_{ref}=1 μA. However, when I_{ref}=0.2 μA/0.3 μA, there is a clear decrease in reliability. We consider that this is because the output is affected not only by the device degradation but also by the variation of the gate-drain leakage current. Therefore, when selecting the reference current, it is not necessary to select a current as high as possible, but be large enough to ignore the effect of leakage current. In addition, the reliability seems to stabilize over time. It can be predicted that better results will be obtained if the system has been stabilized such as using a burn-in experiment.

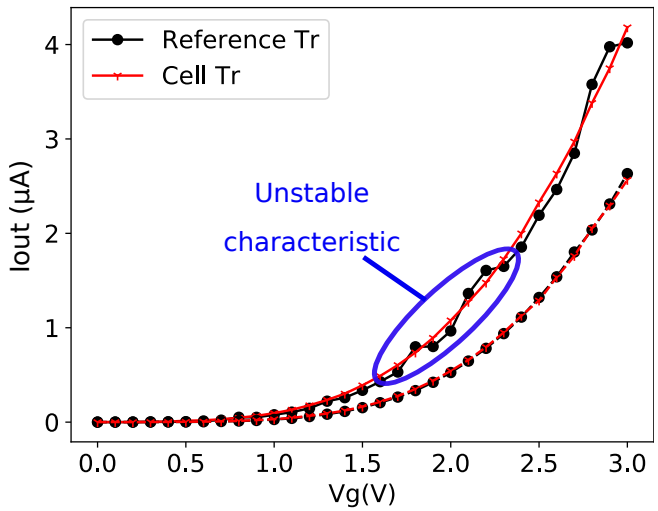


Figure 3.25: I-V characteristics of the unstable device. © IEEE 2020

3.5.4 Comparison

Thus far, in the evaluation, CMA2 achieved a better performance than CMA1. This is due to CMA1 containing some unstable cells. In our measurement, we found that the current characteristics of some transistors were not smooth against V_{gs}, as shown in Fig. 3.25. In CMA1, since those unstable devices work as reference transistors, all outputs of that row will be affected, resulting in the degradation of reliability. On the other hand, even if some unstable transistors exist, their influences were confined to the respective cells and CMA2 maintained better performance from the fourth day and the period that followed.

There is clearly a trade-off between the circuit area and the reliability. Hence, we here define a new figure of merit (FOM) that evaluates the performance of the different circuit designs of PUFs. We define the FOM as follows:

$$\text{FOM} = \frac{\text{Percentage of unchanged responses}}{\text{Area per unit cell}}. \tag{3.5}$$

Fig. 3.26 shows the FOMs of CMA1 and CMA2 as functions of time. In addition, CMA2 shows a higher FOM than CMA1 as time passed. Therefore, CMA2 still demonstrates better performance, even though it occupies a larger area.

We now consider the practical usage of the proposed OCM-PUF as being fabricated on the package to authenticate the product. Assuming that a 64-bit PUF is required for specification, additional bits are required for the design of safe operation, as unstable cells will be included. Though CMA1 has a high area-efficiency, additional bits will enlarge the entire circuit area. From

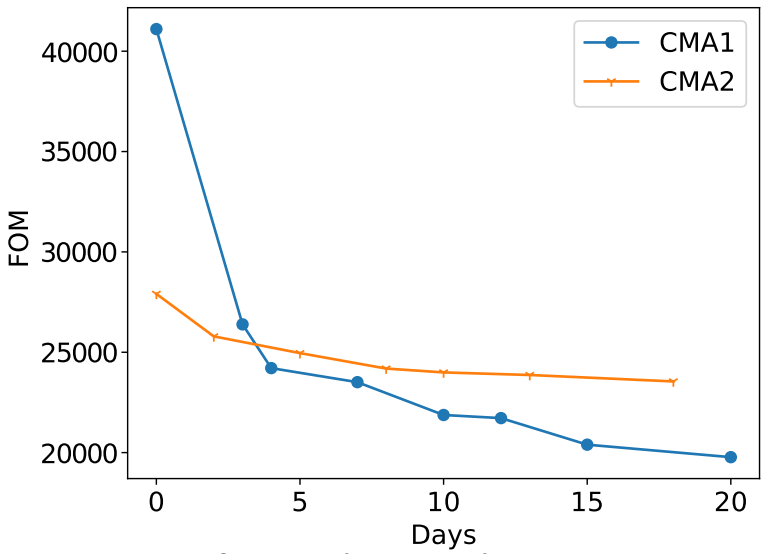


Figure 3.26: FOM as a function of aging. © IEEE 2020

Table 3.2: Required bit and area for different sizes of PUFs. © IEEE 2020

		32-bit	64-bit	128-bit
CMA1	ideal area (mm^2)	77.76	155.52	311.04
	required bit	67	133	266
	real area (mm^2)	162.81	323.19	646.48
CMA2	ideal area (mm^2)	114.56	229.12	458.24
	required bit	38	76	152
	real area (mm^2)	136.04	272.08	544.16

Fig. 3.23, we can see that the number of unchanged responses becomes constant as time passes. We used the percentage of the unchanged responses from the last day to calculate the number of additional bits. For different sizes of PUF, Table 3.2 summarizes the circuit area of the ideal case (all devices were stable), the number of required bits, and the circuit area of the real case based on our measurement. From the table, in current technology, the area-efficiency of CMA2 is higher than CMA1. However, with further development of organic devices, the stability of devices is expected to improve. Hence, the performance of CMA1 may also improve through the use of more stable devices.

3.6 Summary

In this work, an organic PUF circuit using a current mirror structure, called OCM-PUF, is proposed and evaluated its performance through a test chip

fabrication. The proposed PUF circuit was resilient against the deterioration of organic devices, which was considered unavoidable. Two types of OCM-PUFs were proposed by taking into account area efficiency and PUF performance. Through fabrication and measurement of the two OCM-PUFs, it demonstrated that the fabricated OCM-PUFs achieved 95% reliability, thereby exhibiting considerable high tolerance against degradation of the fabricated devices.

Chapter 4

Static Random Access Memory using OTFTs

4.1 Introduction

For implementing truly flexible systems, local data storage is essential to store and to post-process the signals generated by the sensors. Flexible NFC tags, smart labels, and other systems can be combined with sensors to enable environmental monitoring. For example, smart labels can monitor the temperature and other environmental conditions of goods that are being transported or stored. In such systems, it is necessary to store the data first in order to process the data, which the sensors acquire intermittently, in an energy efficient manner. Currently, most of the systems use external silicon-based memories as the local data storage media [18]. However, in actual implementation, mounting silicon dies on a flexible substrate and reducing the number of interface signals between them is considered as a key challenge [63,64]. The data transmission between silicon and OTFT devices costs extra power and time [18, 19]. By manufacturing flexible memory with flexible sensors using the same process, system reliability can be improved and fabrication costs can be significantly reduced.

There are many advantages to building an entire circuit solely using organic technology, which is fundamentally different from silicon technology. However, current OTFTs are mostly unipolar, i.e., p-type transistors are much stronger than n-type. Furthermore, n-type OTFTs are susceptible to degradation due to bias stress [20]. It is challenging to implement complex OTFT circuits via traditional design methodologies that have been developed primarily targeting conventional silicon-based circuits. Hence, the pseudo-CMOS design using only p-type transistors has often been adopted in designing OTFT circuits [25, 26].

When compared to the traditional CMOS designs, the circuits based on pseudo-CMOS design occupy a larger area. Additionally, rail-to-rail outputs are hardly possible. The power consumption tends to be high due to the static leakage current [65, 66]. Therefore, it is important to select the suitable design styles between CMOS and pseudo-CMOS circuits, based on the characteristics of the OTFT circuit under consideration.

In this chapter, an organic static random access memory (SRAM) with CMOS and pseudo-CMOS hybrid design style for enhancing stability is proposed as a flexible memory for IoT applications. Generally, the memory array occupies a large area and consumes high power in the system. In existing works [19,67], the pseudo-CMOS SRAM with large area and power consumption further makes the memory array difficult to be integrated into flexible memory. Hence, we utilize the CMOS design to alleviate the problem of circuit area and power consumption. We show via the simulation and test-chip measurements that the proposed organic CMOS SRAM, which uses p-type access transistors can realize sufficient static noise margin (SNM) for stable operation despite the use of n-type transistors that are originally weak and degradation-prone. In addition, to overcome the short lifetime of the CMOS memory cells due to the fast degradation of n-type devices, we propose to implement an area-efficient, low power, and robust degradation-mitigation circuit suitable for the organic memory arrays. Unlike OTFT PUFs discussed in Chapter 3, the SRAM is considered to operate for a long time, hence the bias-stress degradation especially for n-type transistors is a dominant issue. With the proposed circuit, the SRAM circuit can self-detect bias-stress degradation and automatically perform a process to mitigate device degradation at the required time periods. In designing the detection-mitigation circuit, the pseudo-CMOS design style is adopted for the purpose of stable performance and reliability for a long time period.

The rest of this chapter is organized as follows. Section 4.2 introduces the background and prior art and OTFT-based SRAM circuit design. In Section 4.3, we present the proposed memory architecture and specific circuit implementations. The proposed circuit is evaluated through simulation in Sec. 4.4. In Section 4.5 the performance and robustness of the proposed circuit are experimentally verified via test chip measurements and simulations. Finally, in Section 4.6, we conclude this chapter.

4.2 Background and prior art

4.2.1 Memory in sensor systems

4.2.2 Standard SRAM cell

The standard 6-transistor (6T) SRAM cell shown in Fig. 4.2(a) consists of a pair of cross-coupled inverters holding a state, and a pair of access transistors to read or write the state.

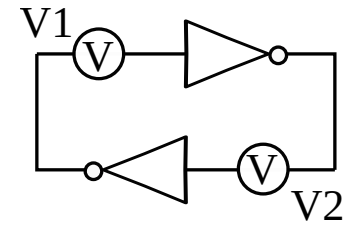
In the read operation, the bitlines are initially precharged as floating logical "1." Assume Q is initially "0" and thus Q_b is initially "1." When the bitline is raised, $bit1$ should be pulled down by the driver and access transistors, D1 and A1. At the same time, Q tends to rise due to change sharing. The charge stored in the bitline flows in through A1. Hence, to keep holding Q at "0" state, D1 must be stronger than A1.

In the write operation, we again assume Q is initially "0" and wish to write "1" to node Q. On account of the read stability constraint, it is unable to force Q high through A1. The cell must be written by forcing Q_b low through A2. Therefore, to maintain the stability of write operation, the P2 must be weaker than A2 [27].

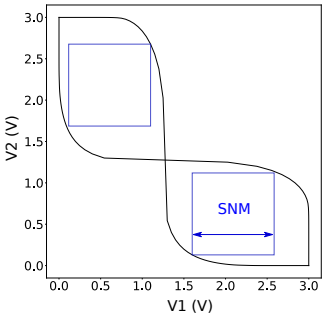
4.2.3 Cell stability

The stability of SRAM cells in different operation mode is quantified by the static noise margin (SNM). The test circuits for determining SNM are shown in Fig. 4.1. The SNM in hold and read state is defined by the length of the side of the largest inscribed square, and SNM in write state is the smallest inscribed square in the butterfly diagram [27, 68]. As shown in Fig. 4.1, read state SNM is the smallest and write state SNM is the biggest. Generally, the writing stability is not a design challenge and addtional attention needs to be paid in read operation [69, 70].

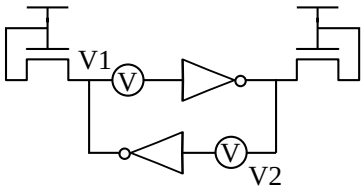
According to the above read and write stability constraints, In the standard SRAM cells, the n-type pull down transistors in the cross-coupled inverters must be the strongest among all. The n-type are of intermediate strength, and p-type pull up transistors must be the weakest. However, in the case of OTFTs, the n-type OTFTs are generally much weaker than p-type. What is worse, n-type OTFTs tend to deteriorate fast during operation. To ensure stable operation, the size of n-type transistors have to be extremely larger than p-type transistors, which significantly increases the cell area.



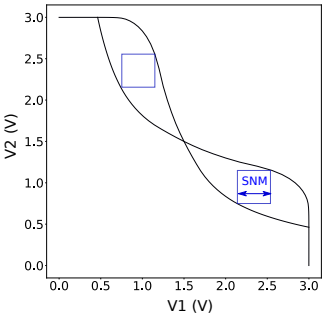
(a) Hold margin circuit



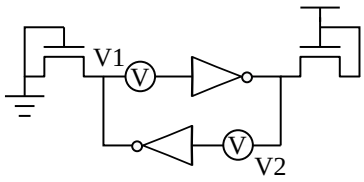
(b) Hold margin



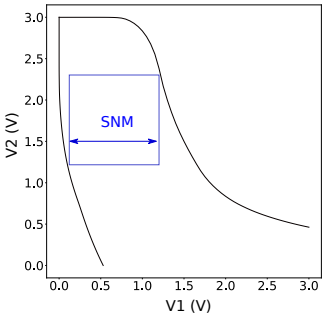
(c) Read margin circuit



(d) Read margin



(e) Write state

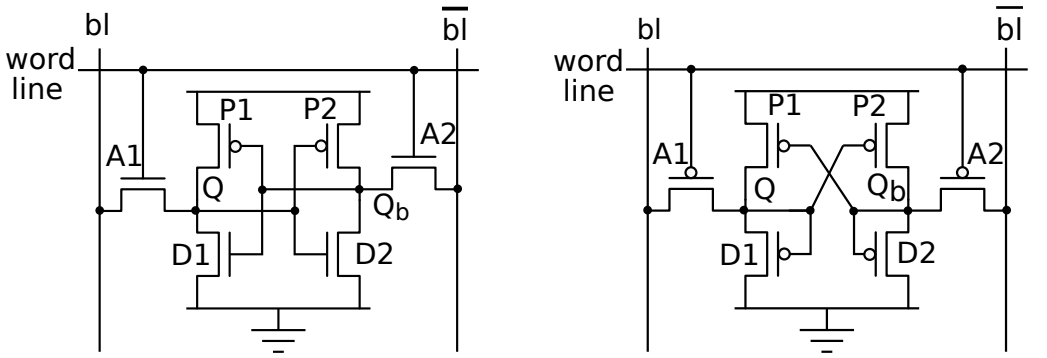


(f) Read margin

Figure 4.1: The test circuits and bufferfly diagram indicating static noise margin (SNM).

4.2.4 Conventional SRAM circuits

As explained in 4.2.2, in order to achieve stable operations of the conventional SRAM cell, the strengths of the transistors comprising the SRAM cell must



(a) Standard SRAM cell.

(b) OTFTs SRAM cell with pseudo-CMOS design.

Figure 4.2: Schematic of conventional SRAM cells. © IEEE 2022

satisfy a specific order. The n-type pull down must be the strongest and is followed by the p-type access. The p-type pull up transistors must be the weakest [27]. The application of inherently weak n-type OTFTs as pull down transistors makes it evidently difficult to satisfy the constraint.

In order to alleviate the issue, the pseudo-CMOS OTFT-based SRAM designs that only use p-type transistors shown in Fig 4.2(b) are proposed. The SRAM cells using pseudo-CMOS designs are reported in [19, 67]. [19] also confirms the operation of a 16b SRAM array circuit. However, in pseudo-CMOS design, the pull down transistors are realized by using transistors with a diode connection. Hence, circuits require significantly large size pull down devices to achieve full swing operation. [66] evaluates the stability of SRAM cells via simulation. This indicates that the pull down devices must be at least 10x larger than the pull up devices to obtain sufficient stability, which further deteriorates the area and power efficiency. Moreover, a 128b SRAM array with periphery read/write circuit using a-IGZO TFTs is proposed in [18]. The a-IGZO OTFTs should be driven by a relatively high voltage, such as 15 V, and this device is also a unipolar device with only n-type transistors. Hence, the pseudo-CMOS design with large pull down devices is adopted in this study.

4.3 Hybrid CMOS and pseudo-CMOS Organic Memory Architecture

The architecture of the proposed CMOS and pseudo-CMOS hybrid organic memory is shown in Fig. 5.4. Based on the conventional SRAM architecture, the proposed memory consists of a memory array, a sense amplifier for data readout, and address decoders. The address decoder specifies the place of the

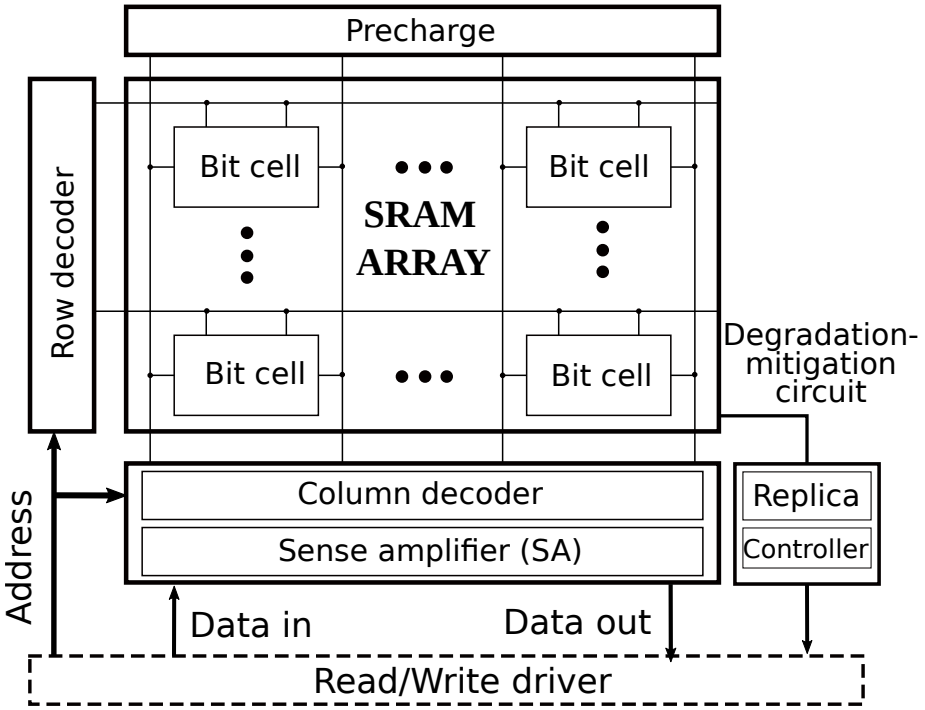


Figure 4.3: Architecture of the proposed memory. Degradation mitigation circuit is added to enhance lifetime of the memory array. © IEEE 2022

memory cell for reading and writing signal data. In the read operation, the cell specified by the address decoder is read through sense amplifiers. The sense amplifiers increase the magnitude of the readout signal appearing in bitlines and can accelerate the reading speed.

In addition to these regular circuit blocks, we propose a degradation-mitigation circuit that senses and mitigates the bias-stress degradation of the transistors composing memory cells to extend the lifetime of the memory. The salient feature of the degradation-mitigation circuit is self-detection of the degradation and self-mitigation, with a simple circuit structure that requires very small resources to implement. When the data is stored for only several hours, the degradation is not significant and the memory operates exactly in a manner identical to conventional memories. Only when the memory is required to store data for a long time, the degradation-mitigation circuit is required to operate to enhance the retention of stored data.

4.3.1 Memory cell

The schematic of the proposed organic SRAM memory cell is shown in Fig. 4.4. The SRAM cell contains cross-coupled inverters that hold data and a pair of

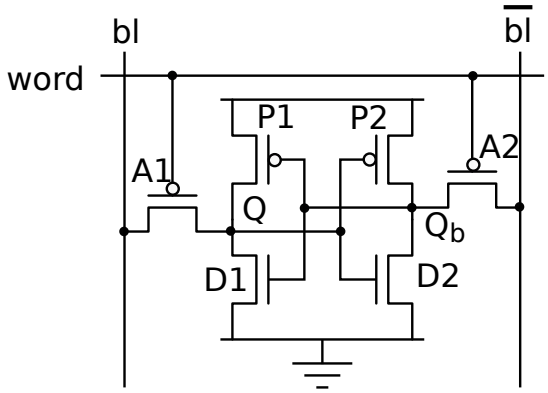
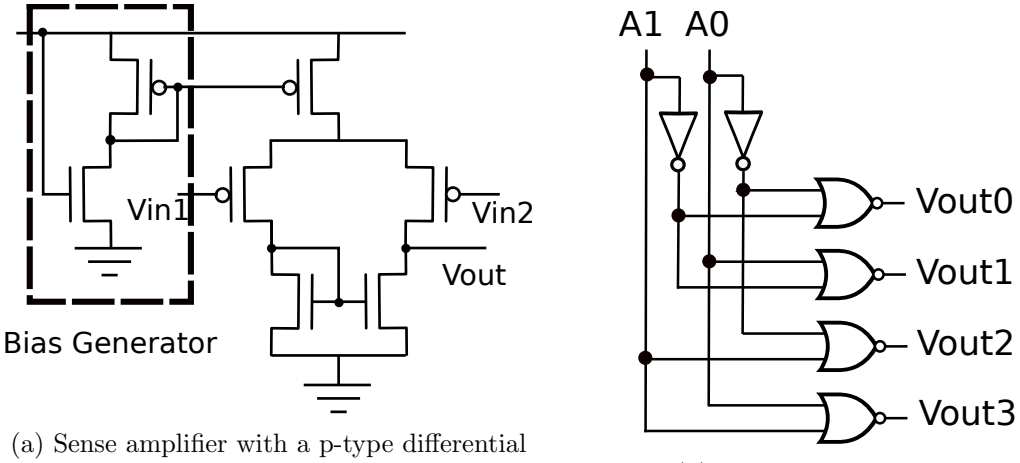


Figure 4.4: Proposed SRAM cell with p-type access transistors. © IEEE 2022

access transistors for read and write operations. In the proposed memory cell, we use p-type access transistors in contrast to conventional n-type transistors. The access transistors are controlled by wordline. When the wordline turns on, the SRAM cell begins read and write operation. The read and write data is transmitted via bitlines. The strength of each device must satisfy specific constraints for stable operation.

With the switching of the type of transistors, the memory cell operation and device constraints are described as follows. Before the read operation, the bitlines are initially precharged to "0" level. Here, we assume node Q is "1" and Q_b is "0." The wordline turns on when the read operation begins. The voltage of node Q tends to fall due to the "0" precharge. In order to maintain the voltage of node Q at "1" level, the pull up transistor P1 should be stronger than the access transistor A1. In the write operation, we again assume Q is initially "1" and wish to write "0" to the same node. Given the read-stability constraint, the voltage of node Q is not allowed to drop to a "0" level, through A1. The cell must be written by forcing Q_b high via A2. Thus, the access transistor A2 should be stronger than the pull down transistor D2 to achieve stable write operations.

As previously described, the strength constraints of the transistors in this circuit differ from those of the conventional SRAM cell in Sec. 4.2.1. The pull up transistor should be the strongest, and then access and pull down transistors should be the weakest. The requirement of the weakest pull down transistor perfectly matches the characteristic of n-type OTFTs. Thus, given the memory cell construction, it is easy to satisfy the necessary constraint without increasing the size of any transistors.



(a) Sense amplifier with a p-type differential pair.

(b) NOR-based decoder.

Figure 4.5: Implementation of periphery circuits. © IEEE 2022

4.3.2 Periphery circuits

In addition to the memory cell, periphery circuits also should be improved to mitigate the weak driving strength of n-type OTFTs. In the study, we design a sense amplifier (SA) circuit using a common-source differential amplifier, as shown in Fig. 4.5(a) [12]. An n-type current mirror load is adopted to achieve a high gain. The gain of the amplifier is given as follows:

$$A_v = g_{\mathrm{mp}}(r_{\mathrm{on}} \parallel r_{\mathrm{op}}), \tag{4.1}$$

where g_{mp} denotes the transconductance of the paired p-type transistors, and r_{on}, r_{op} denote load resistance determined by the channel length modulation of n-type and p-type OTFTs. In the circuit, the significantly higher transconductance of the p-type OTFT is used as opposed to n-type OTFT such that the gain is determined by p-type OTFTs and less dependent on n-type OTFTs.

An example of a circuit implementation of a four-word address decoder is shown in Fig. 4.5(b). The circuit uses NOR and NOT logic gates. The n-type devices are connected in parallel in typical NOR gate implementation. The parallel connection in NOR gates is more suitable than the series connection that exists in NAND gates given the weaker n-type device strengths.

4.3.3 Degradation mitigation circuit

Based on the aforementioned device-type assignments, the proposed memory circuit can write, store, and read data in a stable manner. However, it is reported that the current OTFT cannot avoid degradation, and this is

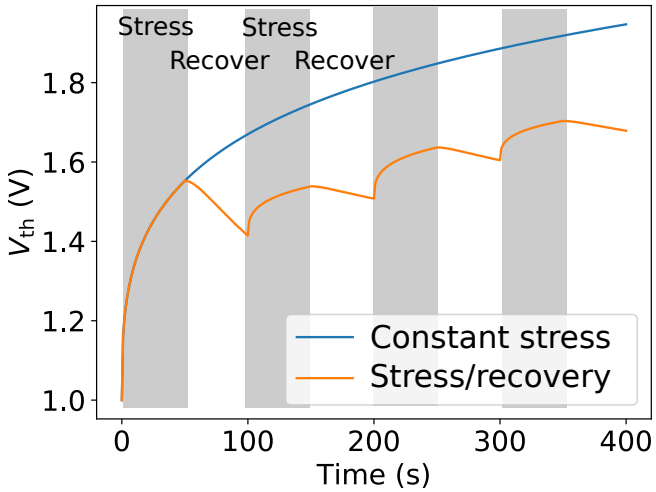


Figure 4.6: Example of the simulation on degradation and recovery of V_{th}. © IEEE 2022

particularly due to voltage stress. When the memory is required to keep storing the same value for a long time, the stored data can be flipped due to device degradation. In this study, we utilize the symmetric structure of the SRAM memory cell and propose a simple circuit that senses and mitigates the device degradation due to bias stress.

Let us assume that node Q in Fig. 4.4 holds data "1" and Q_{b} holds "0." In this condition, device D2 suffers from a constant voltage stress. Thus, the voltage level of node Q_{b} increases gradually due to device degradation. The on-conductance of an n-type transistor can be lower than the off-conductance of the p-type transistor that forms an inverter in the memory cell. In the worst case, the voltage level of Q_{b} can exceed the logical threshold of the memory cell, thereby causing the stored data to be inverted. We propose preventing the constant stress of D2 by deliberately inverting the stored value. Once the stored value is inverted, D1 is stressed and D2 starts to recover. By occasionally inverting the stored values of the entire memory array while bookkeeping the current state of the memory, i.e., whether the stored values in the array are inverted, we extend the retention time of the memory cell.

The performance of the OTFTs is reported to recover when stress voltage is removed. The degradation and recovery model for the bias stress is represented by Eq. 2.8 in Sec. 2.4. Based on the model, a simple simulation of the temporal change of V_{th} in a memory cell is performed as shown in Fig. 4.6. We observe that the change in V_{th} significantly decreases via occasionally inverting stored values.

Fig. 4.8 illustrates the architecture of the proposed degradation mitigation

circuit. The replica cell monitors the degradation of the memory cells as a surrogate. The voltage level of logic "0" of the memory cell replica is continuously monitored by the detector circuit. The detector circuit outputs two signals: Y and $Sigflip$. Signal Y is used to control the inverting operation. Signal $Sigflip$ is used to inform the read/write driver that the stored data in the memory array is inverted ("1") or not ("0"). In the read operation, the memory value is inverted (or not) via the read/write driver to restore the correct data based on the value of $Sigflip$. The replica cell can be implemented in each column of the memory array. Considering the device variability, it is more reliable to use one replica cell monitoring one column than monitoring the entire memory array. Moreover, since the replica cell shares the bitlines with memory cells in the same column, the flip operation can be easily implemented.

The operation of the degradation-mitigation circuit is explained using a simplified timing chart shown in Fig. 4.8. Typically, the proposed memory array acts as a traditional memory. The read address (r_addr) and write address (w_addr) are provided by the system. The memory keeps storing the same value, and thus the node voltage of Q_{b}, which initially stores "0," gradually increases due to the faster stress-degradation of the n-type device. When the voltage exceeds a logic threshold of the NAND gate whose inputs are connected to the internal nodes of the replica cell, the output of the NAND gate switches from "1" to "0," and thus the signal Y changes to "1." The change in Y triggers the inverting operation of the memory array. All word addresses of the memory array are sequentially generated. The words in each address are read out, inverted, and written back to the original word addresses. These operations can be carried out using a simple asynchronous counter circuit. After inverting the last word, the value of the replica cell is inverted, and then Y returns to 0. At this time, the bias conditions are entirely switched for the two inverters in the replica cell. The "0" voltage at node Q becomes very close to zero, and $Sigflip$ is "1," thereby indicating that the memory array contains inverted values.

Similar to the previous cycle, the voltage of node Q, which stores "0" gradually increases due to the degradation of the n-type OTFT. When the voltage at node Q exceeds the logical threshold of the NAND gate, the memory contents are inverted again and return to the initial state. The time that the memory cell is in a single state corresponds to several hours in our device. Thus the time of the inverting operation is in the order of seconds and is significantly shorter than the hold time although it varies with the size of the array. It should be emphasized here that the circuit is self-operating, and thus all processes are autonomously executed as degradation of the memory cell progresses, without any external clock or control signals.

Furthermore, it is noted that the most of the circuit components for the circuit operation described above are already contained in ordinary SRAMs. The

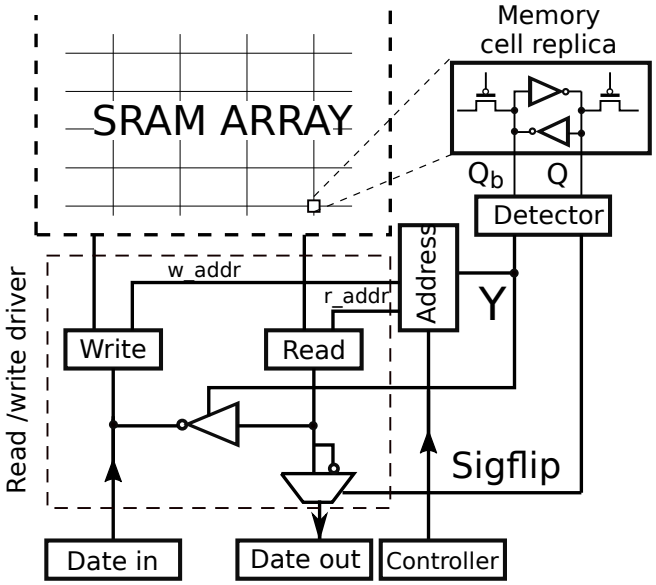


Figure 4.7: Architecture of degradation-mitigation circuit. © IEEE 2022

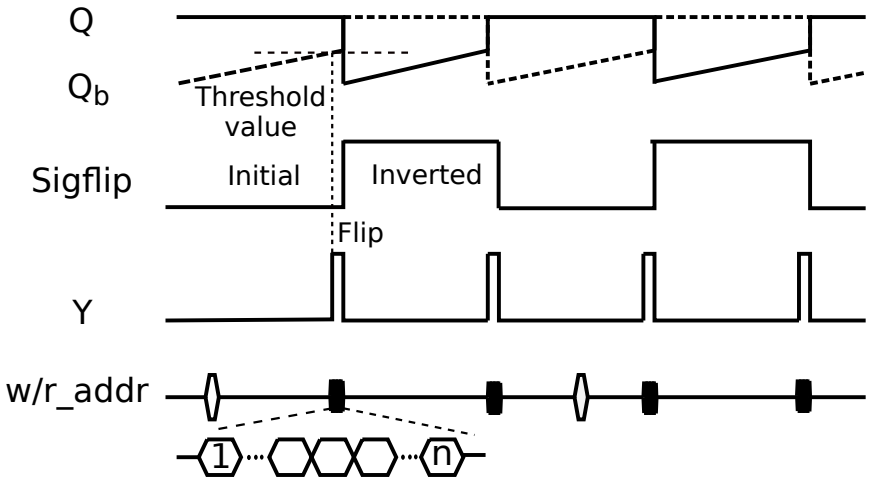


Figure 4.8: Time chart of the operation of degradation-mitigation circuit for a memory array containing n words. © IEEE 2022

important and new component for realizing self-detection and self-mitigation functions corresponds to the degradation-mitigation circuit.

An example of the implementation of the degradation-mitigation circuit is shown in Fig. 4.9. Stability and long-time operation are prerequisites given that the circuit must function appropriately without any significant degradation. Hence, we use the pseudo-CMOS design for the circuit to realize long term reliability. When compared to the CMOS memory array, circuits designed using only p-type OTFTs are hardly affected by degradation due to bias stress.

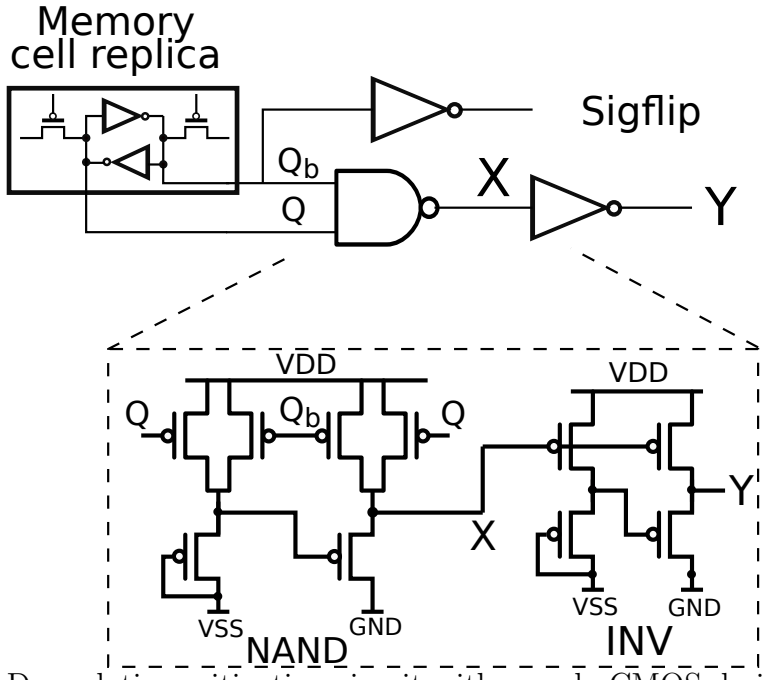
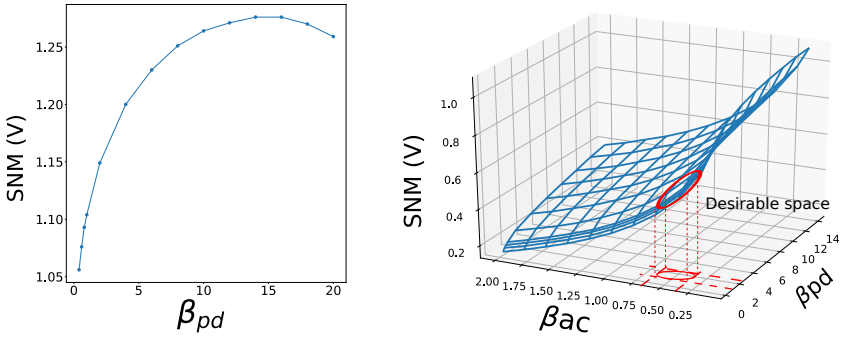


Figure 4.9: Degradation mitigation circuit with pseudo-CMOS design. © IEEE 2022

The degradation detector can be realized by a NAND gate. The two inputs of the NAND gate are connected to the memory cell replica, and thus one of the inputs should always be "0" and the other should be "1." However, the voltage level of "0" input gradually increases due to the degradation of the device. The NAND circuit operates as a comparator to capture the increase of "0" level to "1." The output of the NAND gate X is connected to the INV gate to amplify the signal. The bit stored in the memory cell replica is also used to indicate the state of the memory as $Sigflip$. We use an INV gate to isolate the internal node from outside of this circuit. The voltage levels of VDD, LIND, and VS are 3 V, 0 V, and -1 V, respectively. The construction of the degradation mitigation circuit is simple and its operation is fully autonomous. An additional controller circuit is not required, and thus both the power and area penalty are minimal.

4.4 Transistor Size Optimization through Simulation

In this section, we verify the operation of the proposed SRAM cell through SPICE [71] simulations. Since the writability is not a design challenge, the SNM in hold and read state are simulated by sweeping the transistors sizes:



(a) hold state (b) Read state

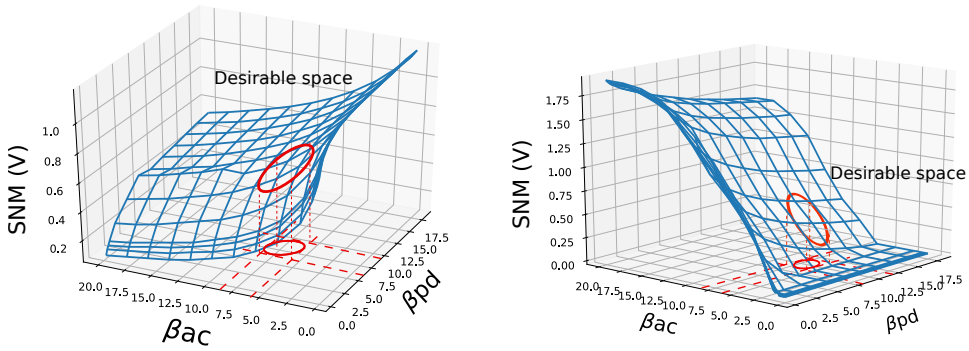
Figure 4.10: Simulation results of SNM in hold and read states at 3 V supply voltage. (*Copyright* (2021) *The Japan Society of Applied Physics*)

the ratio of pull down to pull up transistor size ($\beta_{\mathrm{pd}} = W_{\mathrm{D}}/W_{\mathrm{P}}$ where W_{X} is the channel width of transistor X), and that of access to pull-up transistor sizes ($\beta_{\mathrm{ac}} = W_{\mathrm{A}}/W_{\mathrm{P}}$). The OTFT models used in the simulation [20, 44] are fitted to the device used in this work. A design constraint in this work is assumed that the minimum SNM among different states is above 0.2 V and SRAM cell area is as small as possible.

Considering the weak n-type device, the size of n-type pull down transistors (β_{pd}) is varied from 0.4 to 20, and the size of pull up transistors (β_{ac}) is varied from 0.2 to 2. The results in hold and read states at 3 V supply voltage are shown in Fig. 4.10. The SNM is constantly positive showing that the proposed SRAM can operate stably. In hold state, the SNM is above 1 V and increases as β_{pd} increases. In read state, a small β_{pd} is required for a stable read operation. In terms of stability and transistor sizes, the design space that satisfies the constraint is calculated as β_{ac} is about 0.5 and β_{pd} is about 1.

As a comparison, we also simulate the existing SRAM cells, i.e., conventional SRAM cell and all p-type SRAM cell. In the case of a conventional SRAM cell that is with n-type access transistors, it is necessary to consider writability. β_{pd} and β_{ac} are swept from 0.4 to 20. The results of SNM in read and write operations are shown in Fig. 4.11. The SNM in hold state is the same as Fig. 4.10(a) since the cross-coupled inverter is identical. The SNM in write state reduces to 0 V with the decrease of β_{pd} and increase of β_{ac}. The large SNMs in read and write states lie in conflicting locations, hence the desirable space is considered in between the middle. $\beta_{\mathrm{ac}} = 6{\sim}8$ and $\beta_{\mathrm{ac}} = 8{\sim}12$ are considered desirable.

The simulation results of all p-type SRAM cells are shown in Fig. 4.12.



(a) Read state (b) Write state

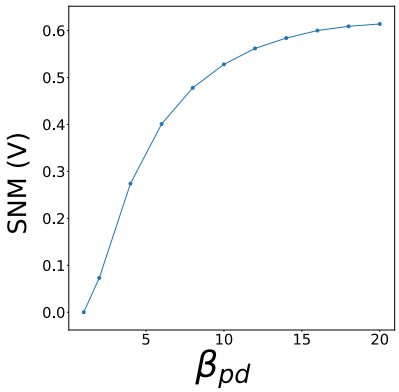
Figure 4.11: Simulation results for conventional SRAM structure for finding optimal transistor sizes in read and write SNM at 3 V supply voltage. (*Copyright* (2021) *The Japan Society of Applied Physics*)

Since the cross-coupled inverter is made of a pseudo topology, the hold SNM is naturally low and pull down transistors have to be large to achieve large SNM. For stable read operation, the access transistors need to be small. In the range of β_{ac} and β_{pd} used in this work, the writability is not a problem. Therefore, the desirable space is where β_{ac} is about 0.3 and β_{pd} is about 7.

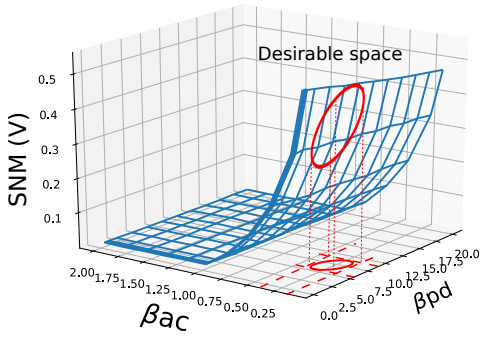
The desirable spaces for each type of cell have been depicted in the respective figures. For a stable operation, under the condition that the minimum transistor size is the same, the conventional SRAM cell and all p-type SRAM cell have similar size. Meanwhile, the device sizes of the proposed SRAM cell can be reduced by 80% compared to the conventional and all p-type SRAM cell. The proposed SRAM structure with β_{pb}=1, β_{ac} = 0.5 and smallest transistor size of W/L = 300/50 μm is chosen for the fabrication and measurement. For comparison, the all p-type SRAM cell with β_{pd}=7, β_{ac} = 0.3 is also fabricated in this work.

4.5 Experimental Validation

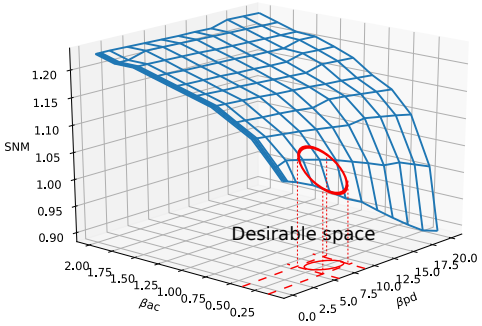
The building blocks of the proposed memory circuit are implemented as a test chip and evaluated via measurements. The microphotograph of the test chip is shown in Fig. 4.13. We use a 16-pin probe card to connect to electrodes of memory array circuit and a source measurement unit (SMU) as voltage sources. A host PC controls SMU channels that generate input signals and measure output voltages.



(a) Read state



(b) Read state



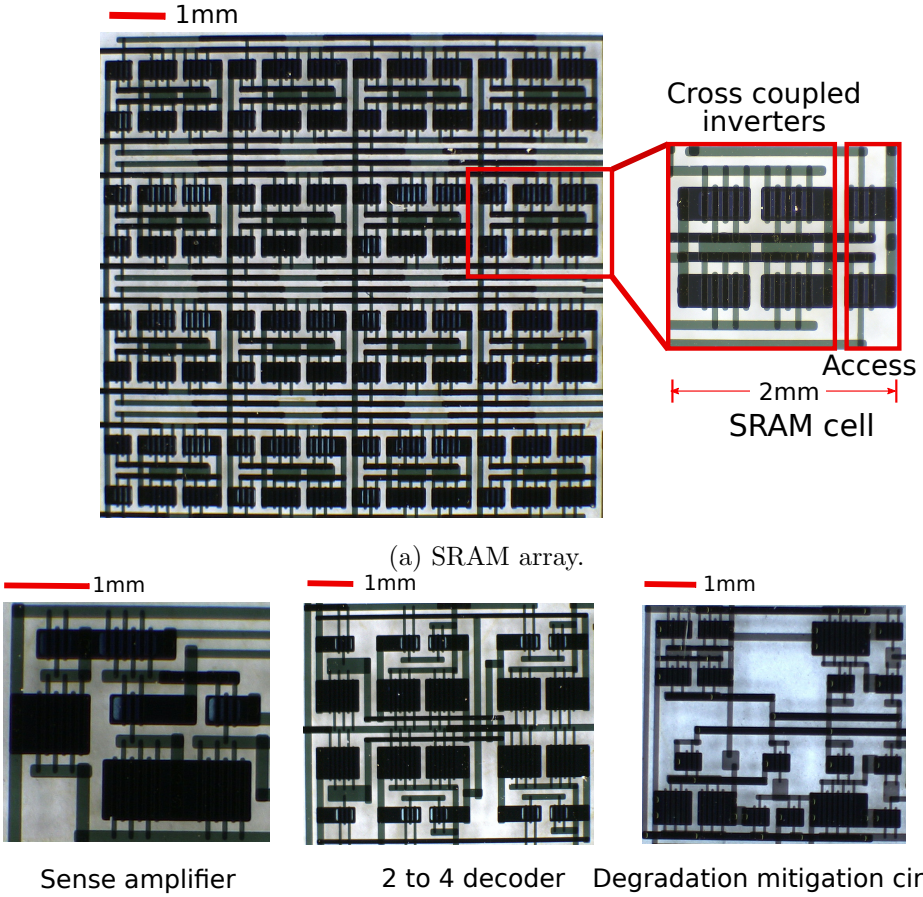
(c) Write state

Figure 4.12: Simulation results for All-p SRAM structure for finding optimal transistor sizes in read and write SNM at 3 V supply voltage. (*Copyright* (2021) *The Japan Society of Applied Physics*)

4.5.1 SRAM memory cell

We first measure the operation of the SRAM memory cell. The dimensions (channel width/channel length) of pull-up, pull-down, and access transistors are 1200 μm/50 μm, 1200 μm/50 μm, and 600 μm/50 μm, respectively, which are optimized via simulation. In our optimized layout, the cell size of the proposed SRAM cell can be reduced by 50%.

The SNM in hold, read, write state of two types of SRAM cells is depicted in Fig. 4.14. In Access-p SRAM cell, the hold SNM is 2.5x, write SNM is 2x and write SNM is 1.4x larger than All-p SRAM. All SNMs in three operation states in Access-p SRAM cell are higher than those of All-p SRAM, meaning that the operation of the proposed SRAM is more stable than All-p SRAM.



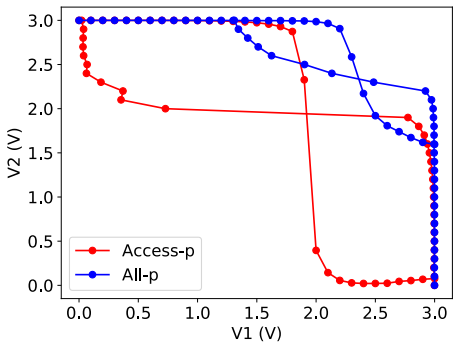
(a) SRAM array.

(b) Periphery circuits.

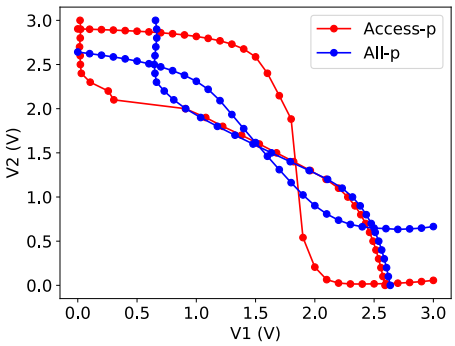
Figure 4.13: Proposed SRAM on test chip. © IEEE 2022

In pseudo-CMOS topology, the pull down transistors are almost close to the off state of p-type transistors even though they are designed with a large size. Hence, the output hardly reaches 0 V when the input is high. In the proposed circuit, though n-type OTFTs are weak, large SNM has been observed owing to the relatively small off-current of p-type OTFTs.

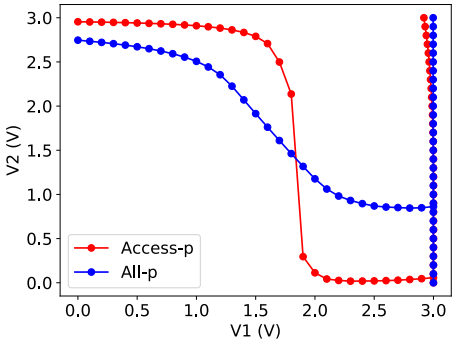
The comparison of the two cells in write operation is also depicted in Fig. 4.15. At first, the access transistors are turned off while pulse signals are applied to bitlines. Nodes Q and Q_b in SRAM should be isolated from the bitlines, and the fabricated cell successfully keeps holding the initial state. Then, after the wordline is activated, the node voltages of Q and Q_b should be overwritten by the values of the bitlines. As the wordline turns off the access transistors again, the internal nodes can hold the signals written before. Although both cells can operate successfully, due to the weak pull down ability in All-p cell, the node cannot reach 0 V when the input signal is low.



(a) Hold state



(b) Read state



(c) Write state

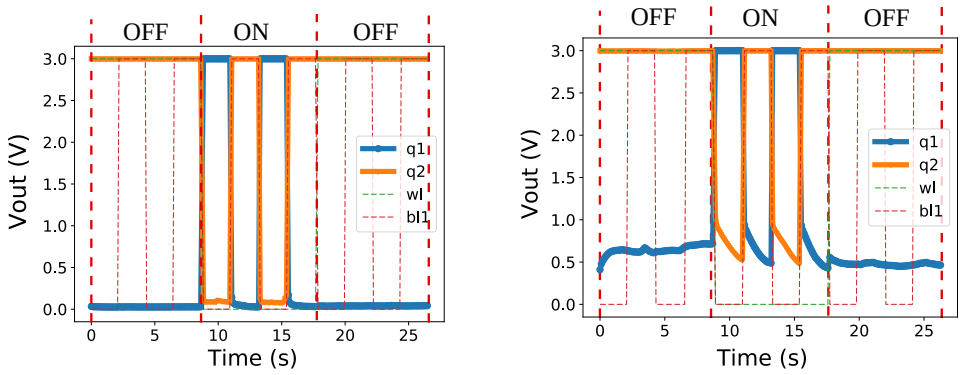
Figure 4.14: The measurement results of SNM in Access-p and All-p SRAM cells at 3 V supply voltage. (*Copyright* (2021) *The Japan Society of Applied Physics*)

Furthermore, the write speed of All-p is also slower than Access-p SRAM cell.

The read and write operation of the proposed SRAM cell is also confirmed in Fig. 4.16. To confirm the read operation clearly, each bitline is connected to a 0.1 μF capacitor. In each operation, the access transistors are first turned off and then turned on. We see that as the access transistors turn on, the write/read operations are activated. The signals written in the previous phase can be read out successfully. With these results, we can verify the correct write/read operation of the proposed SRAM cell.

4.5.2 SRAM array operation

We implement a four-bit word, four-word memory array with periphery circuits on a test chip to confirm its operation. The measured voltage transfer curve of



(a) Access-p (b) All-p

Figure 4.15: The write operation of Access-p and All-p SRAM cells. (*Copyright* (2021) *The Japan Society of Applied Physics*)

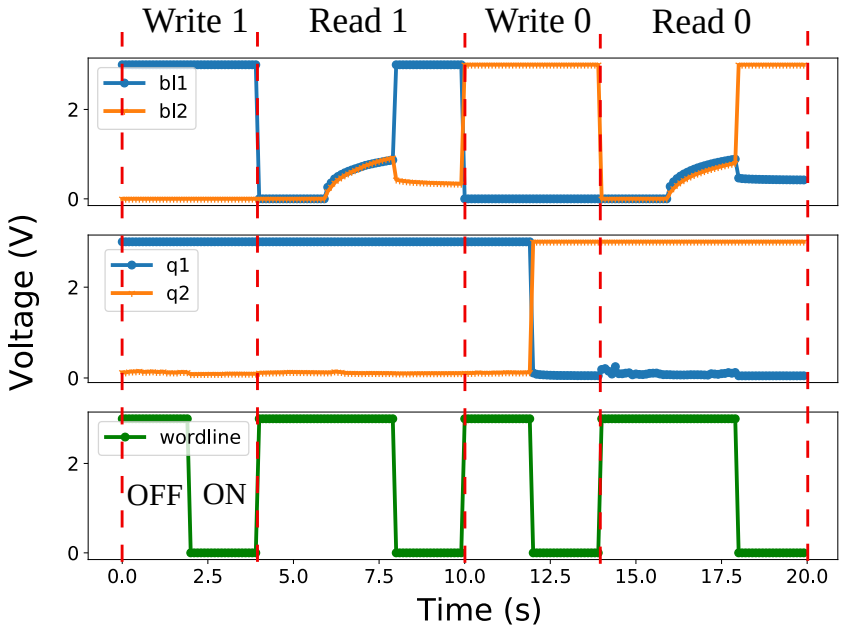


Figure 4.16: Write and read operations of the proposed SRAM cell. (*Copyright* (2021) *The Japan Society of Applied Physics*)

a SA is shown in Fig. 4.17(a). In the measurement, both bitlines are precharged to "0", i.e., 0 V prior to the read operation. When the reading bit is "1", one of the bitlines (bl in this example) begins to increase from "0" level to "1" level, while $\overline{\text{bl}}$ remains as "0." During this period, the output of SA changes from a level about halfway between "0" and "1" toward "1." Similarly, when the

reading bit is "0," $\overline{\text{bl}}$ becomes "1" and bl remains "0," and the output of SA decreases to "0." As shown in Fig. 4.17(a), the fabricated SA is highly sensitive to the change in bitlines. The correct output signals are derived for both "0" and "1" read operations. The transition from the halfway voltage to either "0" and "1" output level requires less than 1.0 V and realizes a fast read operation.

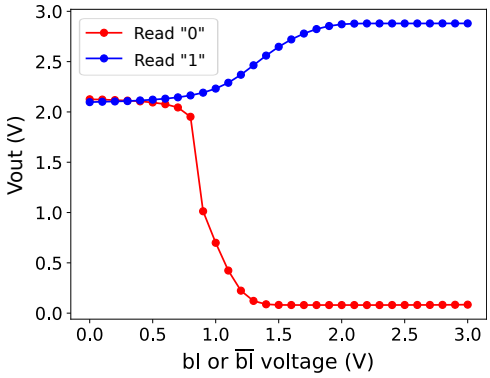
Fig. 4.17(b) shows the measured output signals for the four-bit decoder for all combinations of address inputs. The result indicates that the decoder based on the NOR gate is fully functional. The stable and fast operation of the NOR-based decoder is confirmed based on input signals.

The operation of a memory cell is confirmed as shown in Fig. 4.18. The figure shows bitlines and an output voltage of the SA. When verifying the read operation, each bitline is connected to a 1 μF capacitor, and thus signal transition time is significantly slower than regular operating conditions. When successive write and read operations are issued, the data written in the previous cycle is correctly retrieved in the next read cycle. The stored bit is read after the wordline is turned on, thereby indicating that the wordline also successfully controls read/write operation via p-type OTFT switches. Additionally, the read time is accelerated by approximately 50% with SA.

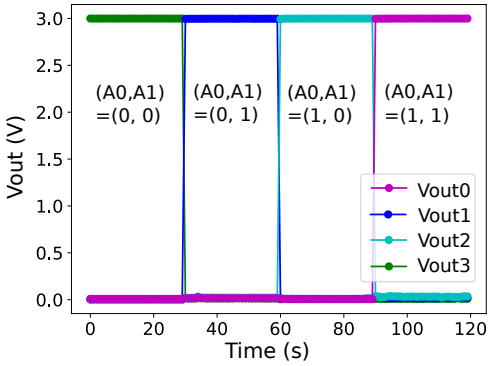
Fig. 4.19 shows the read and write operations of the memory array. In the measurement, we first write four words in sequence, and then read the written four words in the same sequence. A bitline pair is continuously monitored during the series of write and read operations. We first write "1" and "0" alternatively for the word 0, 1, 2, and 3. Subsequently, all the bits stored in the memory cells correctly appear on the bitlines in the subsequent read operations for the four words in the written order. In the read operation, a selected wordline is turned on after the bitlines are precharged in the first half of a read cycle. We can confirm that all the bits corresponding to words correctly appear on bitlines. A comparison between the proposed SRAM and the state of art can be found in Table 4.1.

4.5.3 Degradation-mitigation circuit

We then confirm the effectiveness of the proposed degradation-mitigation circuit. The microphotograph of the circuit is shown in Fig. 4.13. The circuit size is equivalent to the area of only four memory cells, and this is typically sufficiently small when compared to the area of the entire memory array. Fig. 4.20 compares the observation of internal node voltages of a memory cell with and without a degradation-mitigation circuit. In the conventional architecture where no mitigation is performed, just storing the data changes the internal voltage level and worsens the voltage margin. The node voltage storing "0" increases gradually due to the degradation of the pull down n-type



(a) Transfer characteristic of the sense amplifier.



(b) 2 to 4 decoder.

Figure 4.17: Measurement results of periphery circuits. © IEEE 2022

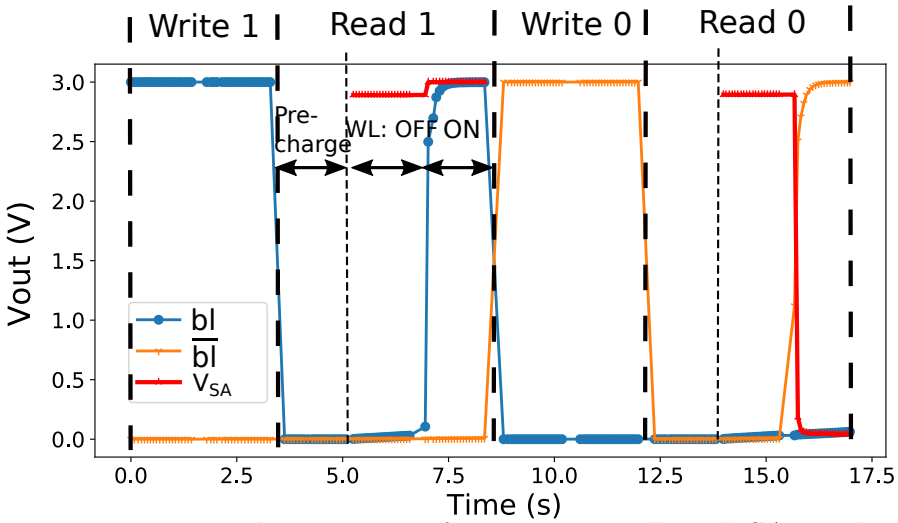


Figure 4.18: Measured operation of a memory cell and SA in the memory array. © IEEE 2022

OTFT. The stored value is corrupted after approximately 5h. It is noted that the memory cell is intensively used before starting the measurement. Although the "0" level increases slightly faster than the fresh memory cell, the proposed memory cell can operate for many hours even after stress-recovery cycles. The measurements of several memory arrays indicate that the retention time of our memory cells can be considered as several hours. This indicates that the proposed mitigation circuit is necessary when the required retention time exceeds this.

Fig. 4.20 also shows the time change of the internal node voltages of a memory cell when the proposed mitigation circuit is applied. A fresh memory

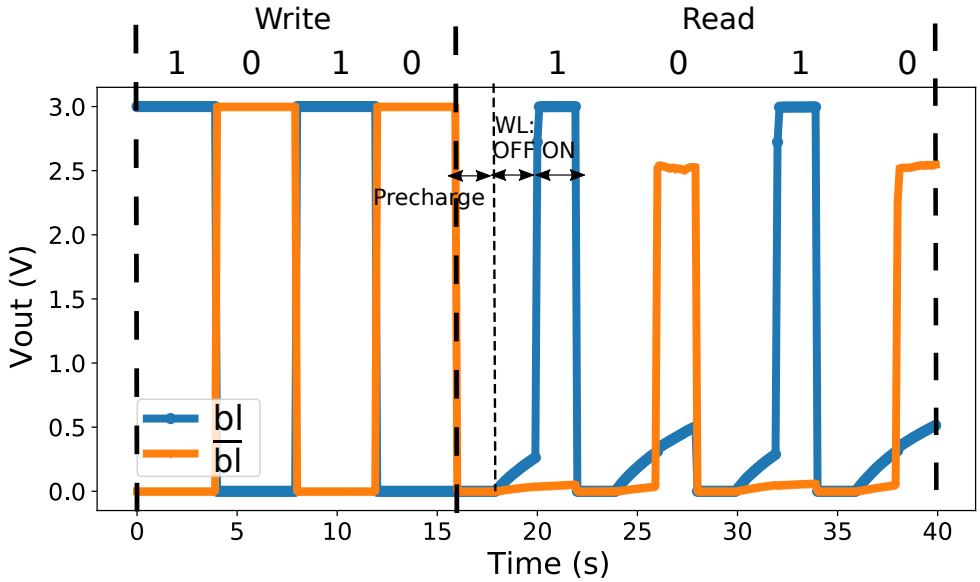


Figure 4.19: Measured read and write operation of the memory array. © IEEE 2022

Table 4.1: Comparison table for thin-film SRAM designs

	This work	Roose et al., 2019 [18]	Avila et al., 2016 [19]	Fukuda et al., 2011 [41]
Technology	Organic	a-IGZO	Organic	Organic
Logic style for SRAM cell	CMOS	Pseudo CMOS	Pseudo CMOS	Pseudo CMOS
Matrix size	4×4 bits	8×64 bits	1 bit	1bit
Supply voltage	3 V	10 V	40 V	4 V
Hold SNM	0.75 V	Not available	2.5 V	0.44 V
Integrated with periphery circuits	Yes	Yes	No	No

cell is used in this measurement. The inverting operation is performed when the voltage of "0" exceeds 1.5 V. As shown in Fig. 4.4, D2 is constantly stressed when node Q is "1." Subsequently, the node voltage at Q_b begins to increase from ground level due to the degradation of D2. The Q_b corresponds to "1," after the inversion of the stored bit, D1 begins to degrade while D2 recovers in this period. After several hours, D2 recovers substantially and can operate for extended hours.

The application of the proposed circuit extends the retention time to at least 35h in this measurement. The measurement results also indicate that the period between bit-inverting is several hours, and the period is adaptively

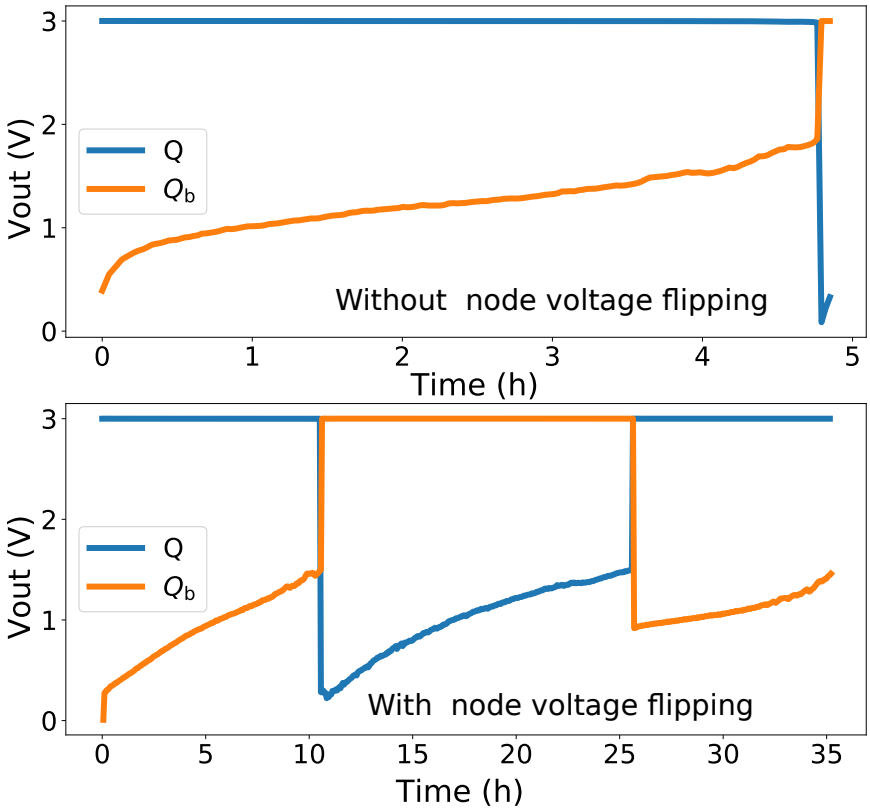


Figure 4.20: Temporal change in internal node voltages of a memory cell. The stored value flips due to device degradation (top). The retention time can be extended significantly through the preventive node flipping (bottom). © IEEE 2022

altered based on changes in the threshold voltage. Although inverting the bits in memory array costs extra power, the period of several hours indicates that the power consumption due to the inverting operation is negligible when compared to the static power consumed by the memory. Fig. 4.21 shows the measured transfer curve of the degradation mitigation circuit in Fig. 4.9. When the "0" voltage of the node, Q or Q_b, increases due to device degradation, the NAND output X gradually changes from "1" to "0." After the amplification by the INV gate, signal Y provides the correct signal to trigger the inverting operation when "0" level increases beyond 1.5 V due to device degradation.

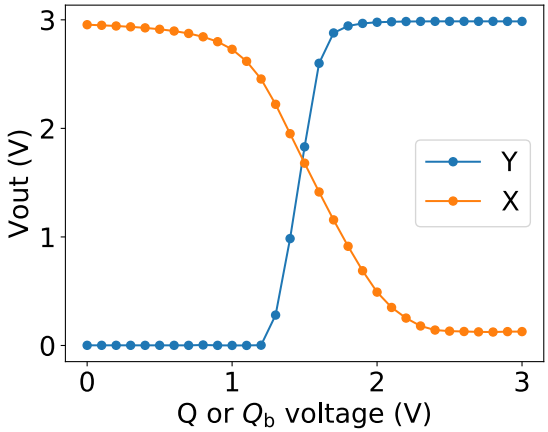


Figure 4.21: Measured voltage transfer curve of the proposed degradation-mitigation circuit shown in Fig. 4.9. © IEEE 2022

4.6 Summary

In this chapter, an SRAM-based memory for flexible electronic systems using low voltage OTFTs is proposed. The application of the proposed memory circuit extends data storage capacity to the flexible sensor systems, thereby enabling efficient data processing and transfer possible. The memory is designed using a combination of CMOS and pseudo-CMOS design styles to enhance its robustness. The SRAM cells utilize CMOS design with p-type access transistors, and this improves area efficiency, power consumption, and stability. Flexible sensors are easier to implement because of the proposed memory with a small area. Its low power consumption can alleviate the problem of energy harvesting in a flexible system. A pseudo-CMOS-based degradation-mitigation circuit is also proposed for the memory array. The proposed circuit can self-detect and automatically mitigate device degradation. Test chip measurements indicated that the memory array and periphery circuits demonstrate correct operation at 3 V. Additionally, the proposed degradation-mitigation circuit significantly extends the retention time of the memory.

Chapter 5

Pass Transistor Logic using OTFTs

5.1 Introduction

In order to implement flexible organic systems, the ability of data processing is an essential requirement. However, as mentioned previously, the OTFTs are unipolar with p-type much stronger than n-type and sensitive to degradation. It is lacking the benefit of using complementary transistor type in circuit design. In Chapter. 4, to achieve higher area efficiency, a CMOS OTFT SRAM is proposed with a p-type only degradation mitigation circuit to enhance stability. However, for more complex data processing systems, it is unrealistic to consider degradation mitigation for every part of the circuits. Hence, the circuits mainly based on the p-type are required. Moreover, the inherent defects due to current OTFT fabrication technologies are the main obstacles to the implementation of robust and complex OTFT circuits. The manufacturing imperfections, such as gate insulator defects described in Sec. 2.2, result in a device failure. It is still a challenge to build large scale OTFT circuits [72,73]. There are several efforts on improving transistor characteristics and circuit topologies [25,26]. However, the transistor characteristic improvements generally involve a high cost fabrication process. The new circuit topologies also tend to use additional transistors to improve performance, resulting in low area efficiency.

In this chapter, an alternative design topology, pass transistor logic (PTL), is adopted for organic circuit design. The proposed topology is applied to reduce the number of transistors required in building logic circuits, especially that of the weak n-type transistors. It achieves high area efficiency and stability since the logical functions mainly depend on strong p-type transistors. PTL is a well-studied logic family with various types of structures [27] and has been

implemented in some emerging devices such as carbon nanotube [74] but seldom in OTFTs. In this chapter, based on conventional PTL structures, two types of the PTL structure suitable for OTFTs implementation are discussed. These two types are different in amplification method. A full adder, which is one of the most essential units in logic circuits, is used as an example to confirm the performance of PTL circuits. Through SPICE simulation and test chip measurement, the two proposed circuits are evaluated.

Additionally, as an application example of PTL circuits, an OTFT processor for data processing is proposed. Processors are at the heart of every electronic device, which is capable of interpreting and executing program instructions and performing arithmetic operations. The microprocessor can make the organic systems smarter since it is programmable. It executes a variety of computational tasks through proper sequencing of instructions without modifying the underlying hardware. At present, several processors using thin-film technology have been reported [15, 75]. However, these processors are based on the similar circuitry and architecture with conventional silicon devices, which requires an extremely high transistor yield. Additional cost and efforts have to be made in fabrication to increase the transistor yield. In this chapter, the improvements on circuits and architecture level are discussed.

The proposed microprocessor uses the one-instruction-set computer (OISC) architecture, implementing the subleq (subtract and branch if less than or equal to zero) instruction. The subleq instruction is Turing complete and can execute any function given sufficient execution time and memory space [76]. Since the OISC can perform only one instruction, the implementation is extraordinarily simple, and it is expected to mitigate the effect of the intrinsic OTFT defects. The execution of the instuction mainly depends on the subtract operation, which can be executed by the proposed PTL full adder. The operation of each component in the architecture is confirmed through test chip measurements and the operation of the OISC processor is confirmed by verilog simulation, showing the feasibility of the PTL-based OTFTs processor.

The rest of the chapter is organized as follows. In Sec. 5.2, the basics of PTL logic family are introduced. Then, in Sec. 5.3 the structure of the proposed PTL circuits is presented. The PTL-based OISC processor is introduced in Sec. 5.4. The transistor sizes of proposed PTL full adder are optimized through simulation in Sec. 5.5 and experiments on full adder and an OISC processor are presented in Sec. 5.6. Finally, this chapter is concluded in Sec. 5.7.

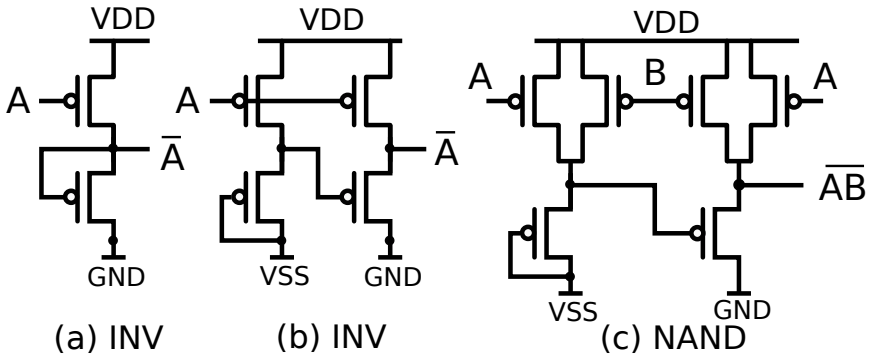


Figure 5.1: Logic gate using pseudo-CMOS structure.

5.2 Background

5.2.1 Conventional OTFT logic gate

In traditional silicon devices, the CMOS structure is one of the most widely used logic families. However, the imbalance of n-type and p-type transistors in OTFTs puts the CMOS structure at disadvantage in many aspects, such as area and gain. The pull down n-type transistors have to be designed using an extremely large size to balance the drivability with much stronger pull up p-type transistors. To overcome these problems, different styles such as pseudo-CMOS structure using only p-type transistors have been generally suggested [26].

Several simple logic gates using pseudo-CMOS structures are shown in Fig. 5.1. Fig. 5.1(a) shows the most basic inverter gate. It is not capable of providing full-swing output signals since the pull down transistors are the diode-connected load. To fully amplify the signals, the addition of multistage logic gates, such as Fig. 5.1(b) or Fig. 5.1(c), is suggested. However, a large number of transistors and multiple DC supply voltages (VSS and VDD) negatively impact to the implementation of organic circuits.

Other topologies have also been investigated. Kim et al. [77] proposed to use a dynamic gate to decrease the area and to increase speed. However, the dynamic gate has the difficulty of monotonicity requirement, in which the input signals must be monotonically rising to ensure the correct operation. The dynamic gates require careful clocking, consume significant dynamic power, and are sensitive to noise during evaluation. Qing et al. [78] used a bootstrapped feedback network to provide full swing signals. However, this topology also uses five transistors per inverter and an additional capacitor which complexes the manufacturing process.

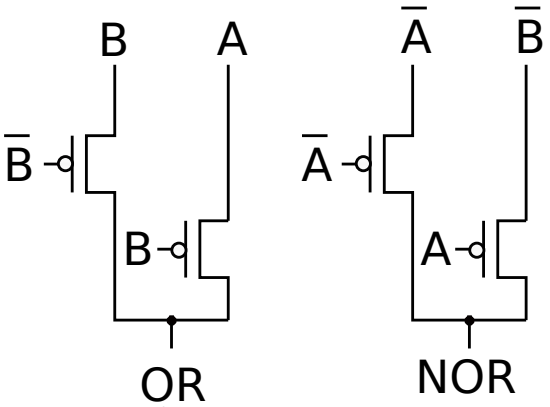
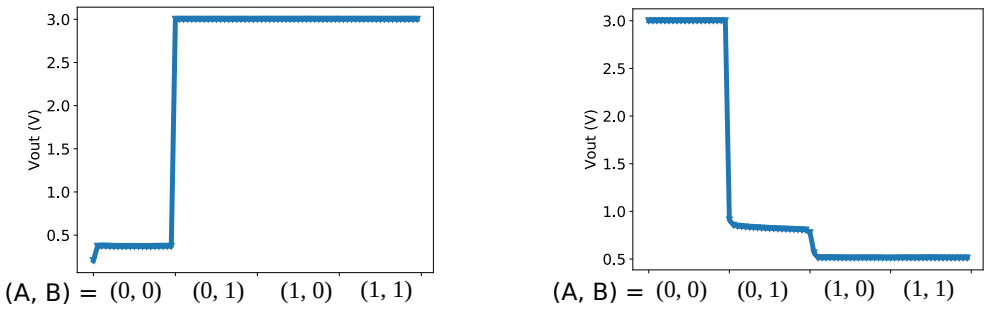


Figure 5.2: Basic logic circuits using pass transistor.

5.2.2 Pass transistor logic

The PTL is a popular and widely used alternative to traditional CMOS logic configuration [79, 80]. Unlike CMOS logic whose inputs are applied only to gate terminals, in pass transistor logic, inputs are also applied to source/drain terminals. For a p-type pass transistor, when a low voltage is applied to the gate, the transistor is in "ON" state. It can pass the input signal from the source to the drain. When a high voltage is applied to the gate, it is in the "OFF" state and the input cannot be transmitted. Hence, the pass transistors can be used as switches to propagate the logic levels between circuits. One major drawback of pass transistors is the threshold voltage drop. For a p-type transistor, it produces a "strong one" but a "weak zero" by raising the output above threshold voltage when the input is logical zero. Generally, complementary pass transistors or adding a gain stage to the output are used to mitigate this problem.

The PTL uses either single type transistors or parallel pairs of nMOS and pMOS transistors as the switches to implement a logic circuit. PTL can significantly reduce the number of transistors and is expected to improve area, speed and power compared to CMOS logic in some cases. For example, Fig. 5.2 shows the NOR and OR pass transistor logic using only p-type transistors. The P-type only transistor networks are less complex, resulting in lower signal capacitance and smaller area. Fig. 5.3 shows an example of measured characteristic NOR and OR pass transistor logic. The pass transistors realize a correct logic function. However, a degraded "low" level output can also be confirmed. Since Fig. 5.2 only contains p-type transistors, a 0.5 V is treated as logic "0" owing to the intrinsic threshold voltage drop.



(a) OR gate. (b) NOR gate.

Figure 5.3: Output levels of basic pass transistor logic in Fig. 5.2.

5.2.3 One Instruction Set Computer

OISC is the ultimate form of reduced instruction set computer (RISC), where the number of instructions is reduced to one. This architecture relies on only a single instruction to implement a Turing complete machine. The only instruction eliminates the necessity of opcode and permits simpler computational elements. Due to its simplicity, the simplest processor cores with minimum hardware resources can construct a multicore processor system with parallel processing. It is reported that OISC architecture has been used in various applications such as data streaming [81], lightweight cryptography algorithm, and microcontroller [82, 83].

A variety of OISC instructions have been proposed, among which subleq instruction is the most popular one and has been used in lots of literature [76, 84,85]. Moreover, the compiler that translates the programs written in a C-style language to subleq has been reported [76]. Hence, subleq is compatible with the normal high-level programing.

The instruction subleq refers to "Subtract and branch if less than or equal to zero". This instruction is composed of three operands: two data addresses and a third next instruction address. Since subleq has only one instruction, the opcode can be omitted. Each instruction is only three addresses long. The semantic of "subleq A, B, C" is as follows:

$$\begin{aligned} Res &\leftarrow Mem[B] - Mem[A] \\ Mem[B] &\leftarrow Res \\ PC &\leftarrow \begin{cases} C, & \text{if } Res \leq 0 \\ PC + 1, & \text{otherwise} \end{cases} \end{aligned}$$

Firstly, the result Res is calculated by subtracting the value stored in memory address A from the value in memory address B. The result is written back in memory B and the next program counter (PC) depends on the value of Res. If Res is smaller or equal to 0, PC jumps to address C, else the PC is incremented by 1. As an example, the addition operation "Mem[b] = Mem[a] + Mem[b]" can be realized as follows.

```
# Mem[Z] = -Mem[A]
 subleq a, Z, 1
# Mem[b] = Mem[b]-(-Mem[a])
 subleq Z, b, 2
# Mem[Z] = 0
 subleq Z, Z, 3
```

Here, "Z" represents a fixed memory location which holds the value zero. Although the subleq only provides a subtraction operation, the *addition* operation is performed by negating the first operand at first. Then subtracting the result value from the second operand. Finally, address "Z" is reset to zero.

5.3 Pass Transistor Logic Architecture

The proposed PTL architecture for OTFTs is shown in Fig. 5.4. It is composed of two main elements: a pass transistor logic tree and a gain stage. The logic computation is performed in the pass transistor tree that uses only p-type transistors. As shown in Fig. 5.2, the pass transistor logic usually uses complementary inputs. To easily interface with the next stage, the output signals are also designed to be complementary. However, the p-type only logic tree suffers from rise of low level logic voltages so-called threshold voltage rise and loss of gain when a low voltage signal is transmitted. Thus, a gain stage is used to amplify output signals.

PTL is a big logic family with various constructions. In terms of the logic tree, the construction in this chapter minimizes the transistor count. Then, two types of gain stages suitable for OTFTs are designed and compared. In this section, we use the full adder, which is the most fundamental and most frequently used logic in digital arithmetic circuits, as an example to explain the implementation of PTL.

5.3.1 Pass transistor logic tree

Compared to basic logic gates, such as OR or NOR, the full adder is a more complex circuit, which needs an additional method to configure the logic tree.

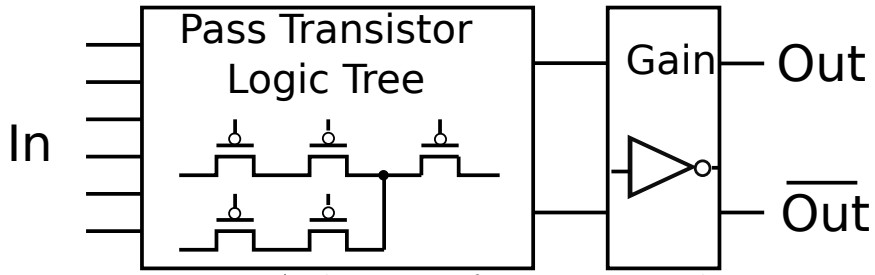


Figure 5.4: Architecture of pass transistor logic.

The sum and carry-out function of a full adder can be expressed as

$$S = \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC, \quad (5.1)$$

$$CO = AB + BC + AC, \quad (5.2)$$

where A and B denote the input bits, C denotes the carry-in bit, S denotes the sum and CO denotes the carry-out.

Fig. 5.5 shows a straightforward approach to designing a full adder using CMOS structure. We first design a half adder and then use two half adders and some logic gates to implement a full adder. Most existing approaches use a large number of transistors resulting in low area efficiency. Furthermore, the heavy use of weak n-type transistors also decreases the stability of OTFT circuits.

Fig. 5.6 shows a schematic of a full adder using pass transistor logic. To minimize the transistor count, a Karnaugh map (K-map) [86] technique is used to generate a logic tree. This technique reduces the transistor count by sharing the path as much as possible. This simplification significantly reduces the layout size and energy consumption.

5.3.2 Gain stage

The p-type only logic tree is purely passive and thus it does not regenerate the input level without buffers, such as an inverter or a pull-up/pull-down circuitry. It cannot produce complete "0" logic. Hence a gain stage is added at the end of the logic tree to provide full swing output.

In this work, two designs of the gain stage are discussed. The first design is shown in Fig. 5.7 based on swing restored pass transistor logic (SRPL) [87]. A cross-coupled inverter (latch) is used to amplify the output. It minimizes the number of n-type transistors to enhance stability. It is also compatible with the pseudo-CMOS logic discussed in Sec. 4.2, which can completely eliminate the use of n-type transistors. The large size pseudo-CMOS logic is used only in the gain stage so that its effect on the entire circuit is small.

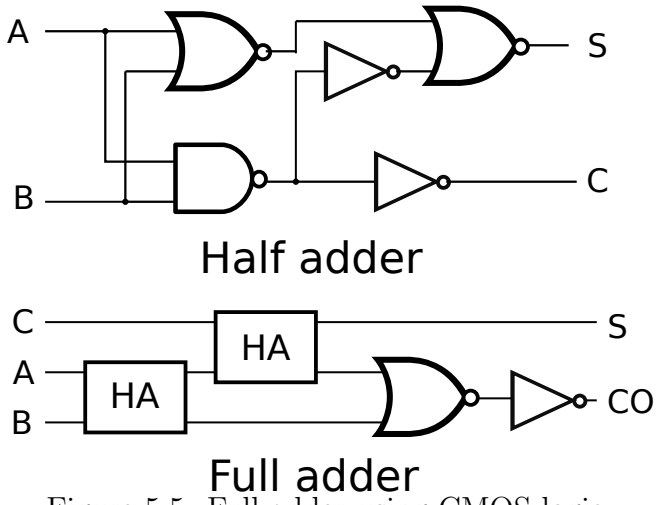
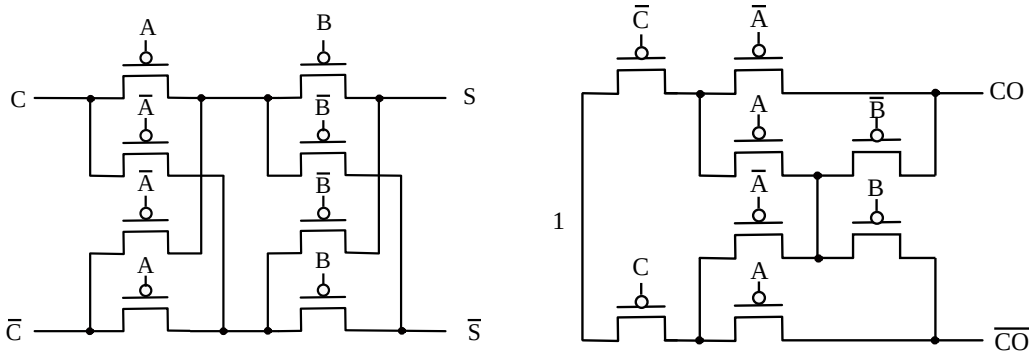


Figure 5.5: Full adder using CMOS logic.



(a) Sum circuit.

(b) Carry circuit.

Figure 5.6: Full adder using pass transistors logic.

The other design is shown in Fig. 5.8, which is based on differential cascade voltage switch circuits with pass gate logic (DCVSPG) [88]. Since the p-type pass transistor can provide complete "1" output but suffers from threshold voltage rise on the "0" output, we use only two n-type transistors to pull-down the signals. This design further reduces the transistor count. However, compared with gain stage using latches, the ability of pull down using n-type transistors is considered to be weak. Table 5.1 summarizes the transistor numbers used in full adder of each logic type, traditional CMOS, gain stage with latch, and gain stage with n-type transistors. Compared to the traditional CMOS structure, the PTL logic can reduce the transistor counts by 50%. Furthermore, the number of n-type is reduced to only 1/10, leading to higher area efficiency and stability. To further compare the types of PTL, the circuit operation speed will be evaluated in Sec. 5.5.

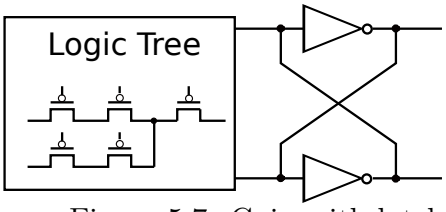


Figure 5.7: Gain with latch.

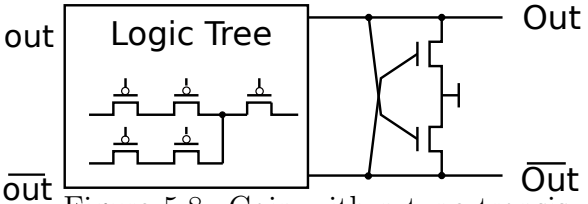


Figure 5.8: Gain with n-type transistors.

Table 5.1: Device counts of full adder.

Logic type / Count	Traditional CMOS	Gain with latch	Gain with N-type
P-type	19	18	16
N-type	19	2	2
All	38	20	18

5.4 PTL-based OISC Processor

In this section, as an example of the PTL-based OTFT circuit design, a processor using OISC architecture is discussed. The OISC processor is extremely lightweight mainly based on the PTL adder proposed in previous section. Despite its simplicity, the proposed processor is Turning complete and can execute specified operations for OTFT system. The OISC architecture and a simple example operation considered to be used in OTFT system are introduced in Sec. 5.4.1. Then, the specific circuits in the architecture of OISC are explained in Sec. 5.4.2.

5.4.1 Architecture

The architecture of subleq based OISC processor is shown in Fig. 5.9. This architecture contains three main components, an instruction memory, a data memory, and an arithmetic unit. For simplicity, we assume one subleq operation is performed in one clock cycle. The specific operation is characterized below:

1. Instruction memory: the instruction memory stores the instruction to be executed. At the rising edge of a clock signal, it receives the next instruction address generated by arithmetic units and supplies the next instruction to system. It can be implemented by SRAM memory described in Chapter 4. Since the instructions are generally large in OISC architecture, for complex programs, they can also be implemented off-chip, combined with silicon technology.

2. Data memory: the data memory stores the data in system and the results of computation. Based on the data address in the instruction, the data is sent to arithmetic unit for computation. At the rising edge of a clock signal, the result is written back to the second data address (B).

3. Arithmetic unit: the arithmetic unit contains a subtractor, which computes a difference between the two inputs. If the result is negative or equal to 0, the next instruction address gets updated by the jump address, specified in the instruction. Otherwise, the instruction address gets updated by the immediate next instruction. At the rising edge of a clock signal, it sends the computation result to data memory and the next instruction address to instruction memory. A multiplexer (MUX) circuit is required to perform this branch operation and a flip-flop is used to synchronize the data.

The above-described architecture is extraordinarily simple and lightweight, thus the operation is expected to be possible when implemented in OTFT systems. As an example, for an organic sensor with an array structure or an organic PUF discussed in Chapter 3, an operation that reads out row/column signals in order in an array is needed. The operation that sends a signal to decoder of array system can be represented by a loop program,

```
for (i=0;i<N;i=i+1){
      p = p+1;
      output(p);
}
```

Here, an implementation is shown on how to translate this program to subleq. The instruction memory and data memory are designed as follows. Here, the architecture is designed to output data when the second address is -1 and stop operation when the third address is -1. The instruction opcode (subleq) is omitted.

```
Instruction memory:
  # mov p to a
   a a 1; p Z 2; Z a 3; Z Z 4;
  # output p
   a -1 5;
  # p = p+1
   M p 6;
  # Check if p<N
   a a 7; E Z 8; Z a 9; p a -1; Z Z 0
Data memory:
  a:0; Z:0; M:-1; E:N
```

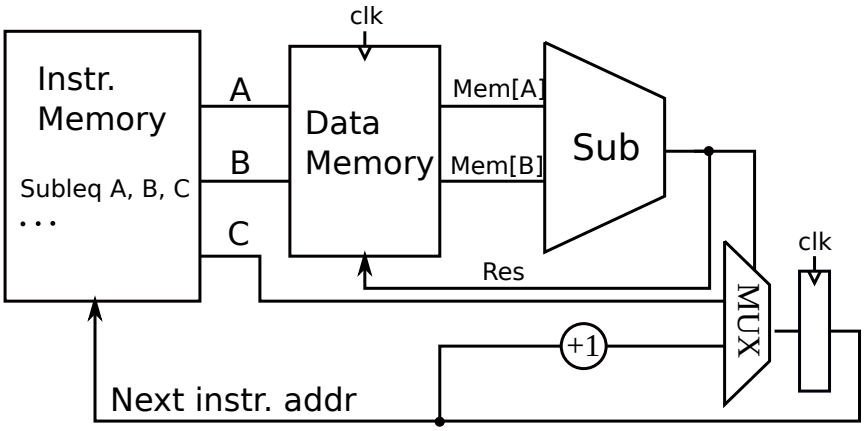


Figure 5.9: Simple architecture of OISC.

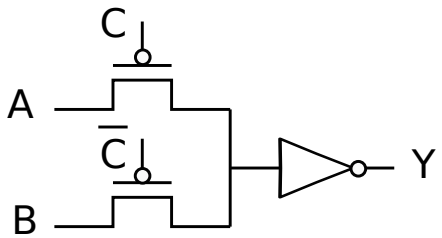


Figure 5.10: Multiplexer based on pass transistors.

Here address "Z" points a fixed memory location saving the value zero and address "a" is used to output the data or save temporary results. As discussed above, the OISC OTFTs processor has the ability to execute basic operations required in OTFT sensors or OTFT PUF.

5.4.2 Circuit construction

As shown in Fig. 5.9, the architecture is mainly based on the arithmetic unit, a subtractor. It can be easily realized with a slightly modified adder proposed in the previous chapter. According to two's complement, to perform B − A, each bit of A is inverted with NOT gate then add one. In the previous section, a full adder using pass transistor logic has been proposed. The subtractor in the proposed processor is based on the proposed full adder.

Other small scale circuits in the proposed architecture are introduced next. Considering the area efficiency, most of them are also constructed by pass transistors. Fig. 5.10 shows the MUX used to branch instruction address. To reduce transistor count, pass transistors are used in this circuit. Since p-type transistors cannot produce full swing output, an invert is added to the end to amplify the output signal.

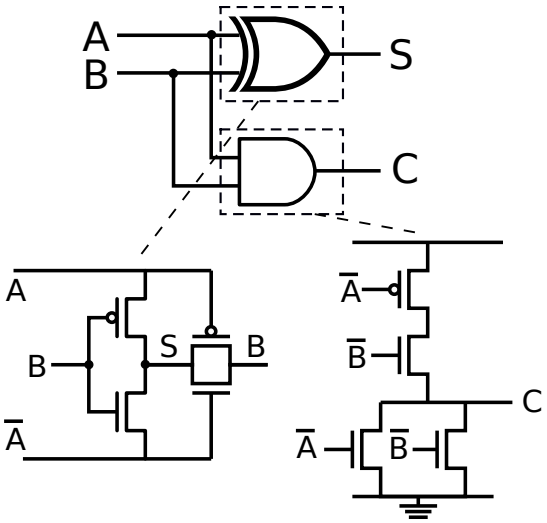


Figure 5.11: Construction of half adder.

When the result is positive, the instruction address is incremented by one, which is referred to as a "+1" operation. Although this operation can be easily realized by a full adder, it can also be simplified to a half adder. Fig. 5.11 shows the specific construction of the half adder. It contains a NAND gate and an XOR gate. In this work, a NOR gate is used to replace the NAND gate, since the parallel connection of n-type transistors in the NOR gate can enhance the device strengths. In the structure of the XOR gate, pass transistor topology is also adopted. This structure minimizes the gate area.

Fig. 5.12 shows the D-flip flop (DFF) used to synchronize the system data. D-FF is one of the most essential units in digital circuits. At present, several types of flipflops using OTFTs have been discussed. Takeda et al. [89] proposed a NAND-based flipflop which can afford low voltage operation. Hayasaka et al. [90] demonstrate a latch-based flipflop. It is reported that latch-based flipflop saves 60% of the occupied area and a shorter propagation delay time when compared to NAND-based flipflop. Hence, a latch-based flipflop is utilized in this work. In this DFF, two D-latches are used to form a flipflop. Noting that the transistor sizes in D-latches need to be designed carefully to guarantee a correct operation. Since p-type transistors are much stronger than n-type, the pull up p-type transistors in feedback invert may affect the internal node. For example, the node "Q" tends to be "1" due to feedback inverter. This abnormal node "Q" also has an influence on former nodes, destroying the values stored in the D-FF. Hence, in order to maintain a stable operation, feedback inverters, especially the pull up p-type transistors, are designed weak strength with a small size.

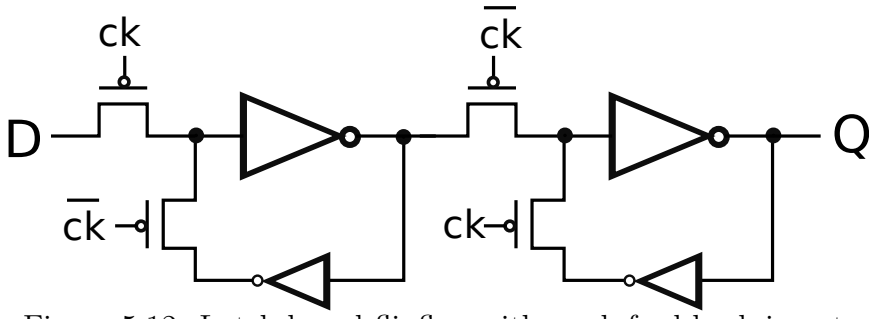


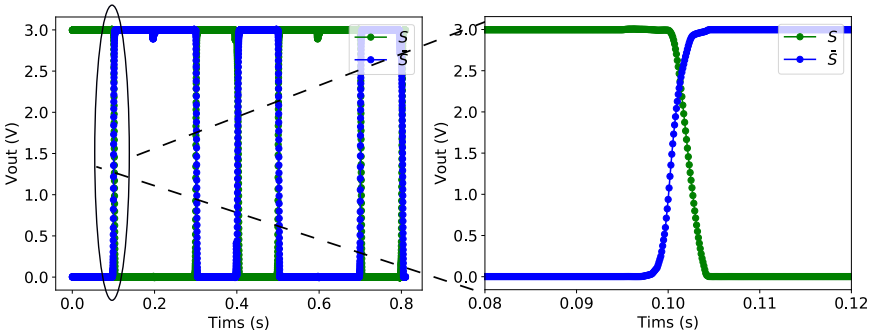
Figure 5.12: Latch based flipflop with weak feed back invert.

5.5 Transistor Size Optimization

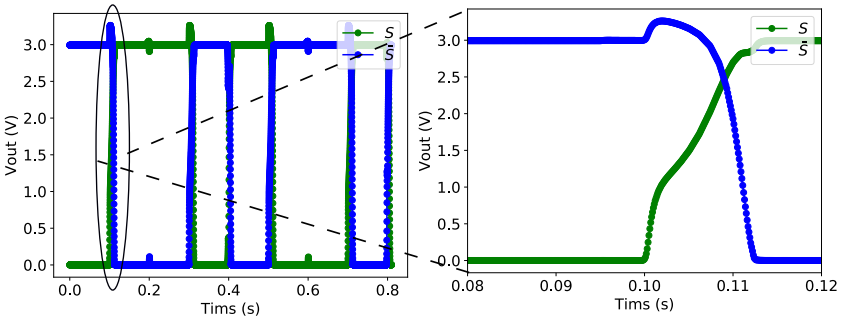
Prior to the test-chip measurement, the operation of the proposed full adder circuit is first verified through SPICE simulations. Since full adder is a major component of the OISC, it needs to be designed carefully. In the two proposed gain stages, both latches and n-type transistors use a cross-coupled structure. For pull-down n-type transistors, there is a trade-off between a large transistor that pulls down the signal quickly on one side while pulling up the signal slowly on the other side. Hence, the sizes of the cross-coupled device need to be determined carefully to reduce the circuit delay. In this section, besides the operation verification, we optimize the transistor sizes to minimize circuit delay. Then, we evaluate and compare the performance of two proposed gain stages at the optimal size through simulation.

Fig. 5.13 shows an example of the transient simulation waveform of the proposed sum circuit in the full adder. The input signals change all combinations from (0,0,0) to (1,1,1). For both of the proposed gain stages, the pass transistor tree can output the correct sum and carry results and both of the proposed gain styles can generate full-swing output. Meanwhile, the latch type gain stage shows better stability and faster operation speed. To evaluate delay and compare the two types of gain stages, the rise and fall time of output signals are simulated by sweeping the sizes of transistors. The channel length of all transistors is fixed to 50 μm, the channel width of n-type pull-down transistors (W_{N}) is also fixed to 1200 μm and the channel width of p-type transistors (W_{P}) is swept from 100 μm to 1600 μm.

The results of the timing simulation of the proposed gain stage with different transistor sizes are shown in Fig. 5.14. In general, enlarging the transistor sizes leads to a faster operation, while fall time increases as the size becomes too large. Owing to the cross-coupled structure, n-type pull-down transistors cannot provide sufficient current against large pull-up p-type to pull down the signals. From the results, $W_{\mathrm{P}}/\ W_{\mathrm{N}} = 0.3$ is considered as a desirable size. A



(a) Gain with latch.



(b) Gain with n-type transistors.

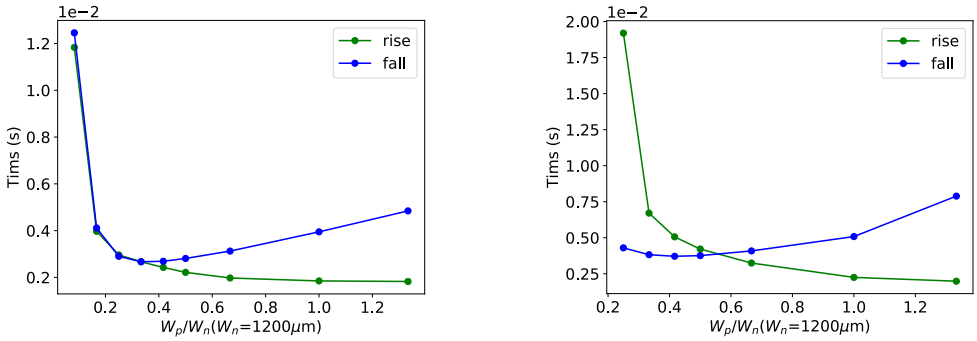
Figure 5.13: Transient simulation waveform of sum circuits.

similar simulation is done to the gain stage using n-type and its results are shown in Fig. 5.15. The trend of the results is also similar to the former one.

The comparison of the two gain stages is shown in Fig. 5.16. The rise and fall time are from the operations at optimal transistor sizes. Overall, the latch type gain stage is faster than the n-type gain stage, since the latch has a better amplification ability. From Table 5.1, the transistor counts of latch type gain stage are only two more than n-type gain stage. The occupied areas of the two circuits are almost the same. However, the operation speed can be significantly accelerated with latch gain stage. In some cases, the delay of circuits with latch gain stage can be reduced to half. Thus, the gain stage using latch is considered as a better topology for PTL-based OTFT circuits.

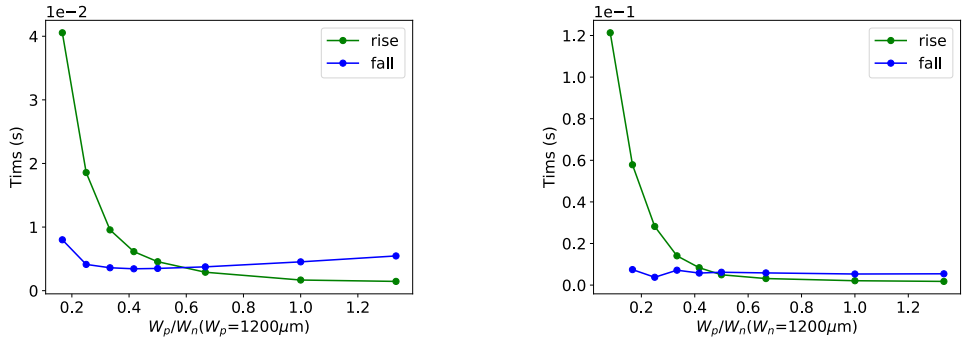
5.6 Experimental results

In this section, as the main component of the OISC processor, the PTL-based full adder with the optimal size is first verified through test chip measurement. Then, to execute the example loop program described in Section. 5.4.1, an OISC



(a) Sum circuit. (b) Carry circuit.

Figure 5.14: Simulation results of rise and fall time with latch gain stage.



(a) Sum circuit. (b) Carry circuit.

Figure 5.15: Simulation results of rise and fall time with n-type gain stage.

processor is designed. Unfortunately, it is still a challenge to make the whole system operable on the current OTFTs yield. The components of the processor are verified through measurements and the operation of the OISC processor is verified through verilog simulation. In test chip measurements, We use a 16-pin probe card to connect the electrodes of each circuit. A host PC controls source measurement unit (SMU) channels to generate input signals. The output voltages are measured by the SMU and an oscilloscope. The supply voltage of all measurements is set to 2.5 V.

5.6.1 PTL-based full adder

Based on the simulation results, p-type transistor sizes of the proposed full adder is W/L = (600/100) μm and n-type transistors whose layout size of (1200/50) μm are chosen for fabrication. The microphotographs of the fabricated full adder are shown in Fig. 5.17.

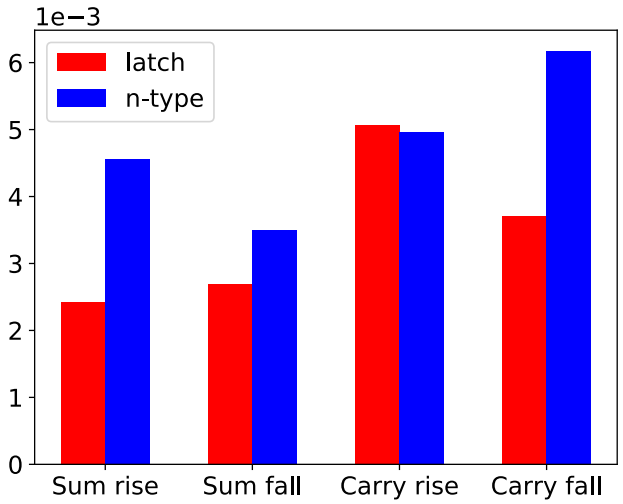


Figure 5.16: Comparison of operation time at optimal size.

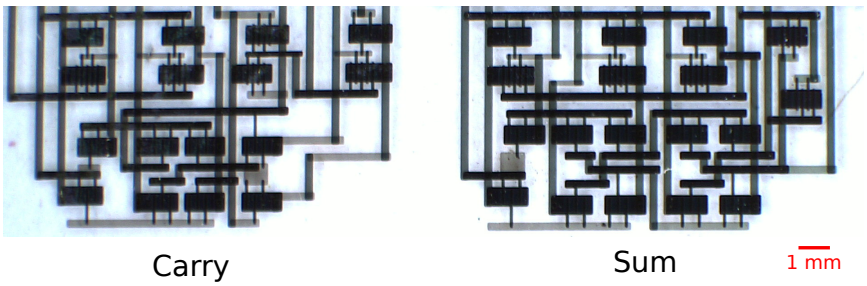


Figure 5.17: Microphoto of proposed full adder on test chip

The measured waveform of the full adder is shown in Fig. 5.18. Input signals, A, B, and C are swept from (0,0,0) to (1,1,1). The calculation results of the full adder are confirmed to be correct for all combinations of the input signals. Fig. 5.19 and Fig 5.20 show the specific transient waveform of the output signal changing from "0" to "1" and "1" to "0". The rise time and fall time of the sum signal are about 5.2 ms and 8.1 ms. For the carry signal, the rise time and fall time are about 11.2 ms and 15.1 ms respectively. For both signals, the relatively long fall time is considered due to the degradation of n-type OTFTs.

5.6.2 OISC processor

To execute the example loop program described in the previous section, an OISC processor is discussed in this section. For simplicity the processor is designed to be 2 bits with a signed 3 bits subtractor. Fig. 5.21(a) shows an example

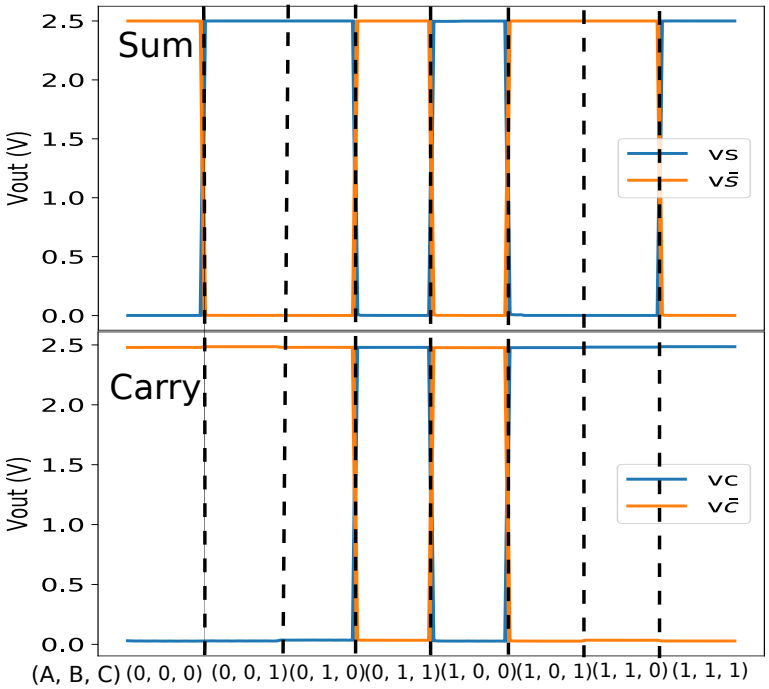
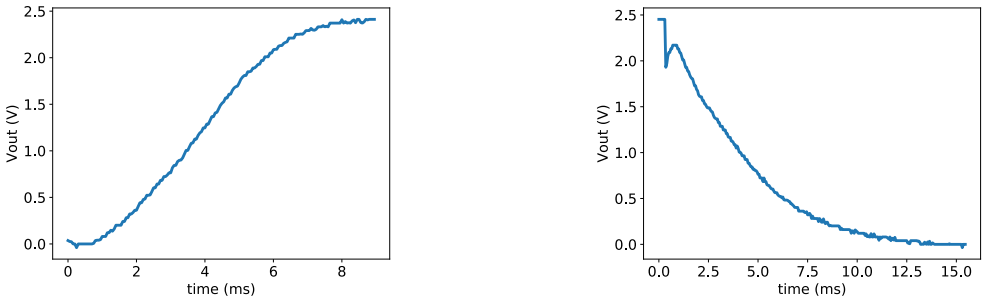


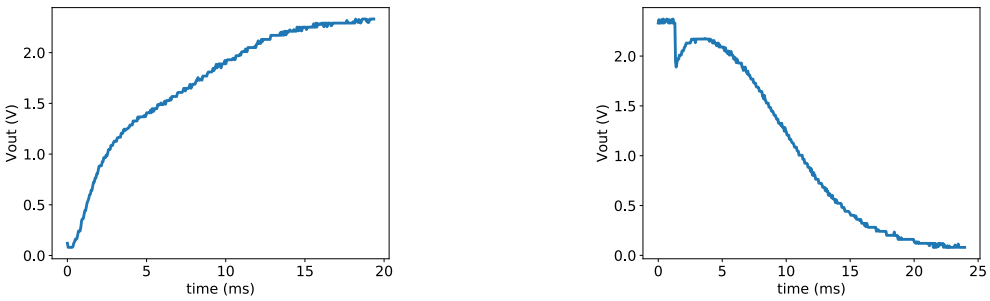
Figure 5.18: Measurement result of PTL full adder.



(a) Signal sum rise. (b) Signal sum fall.

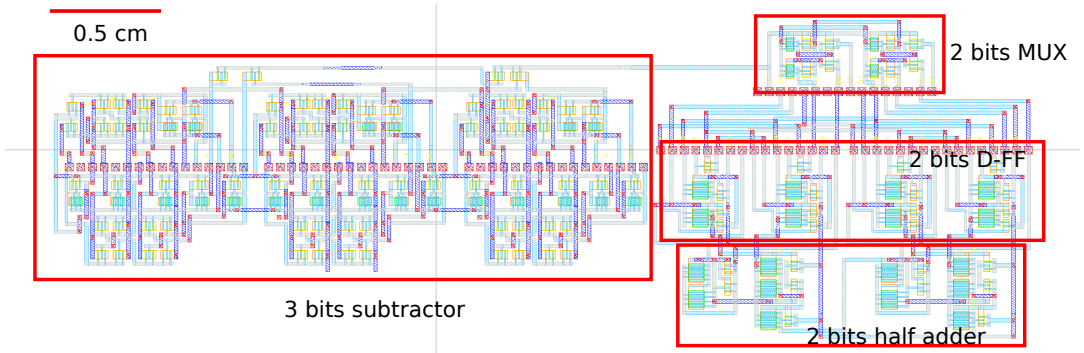
Figure 5.19: Transient waveform of output sum signal.

layout of this processor without memory implementation. It is comprised of 152 transistors. However, the current yield of OTFTs used in this dissertation is about 95%, the current OTFTs cannot guarantee a correct operation of the entire system. The operation of the entire system is confirmed through verilog simulation instead and each component used in the OISC processor is

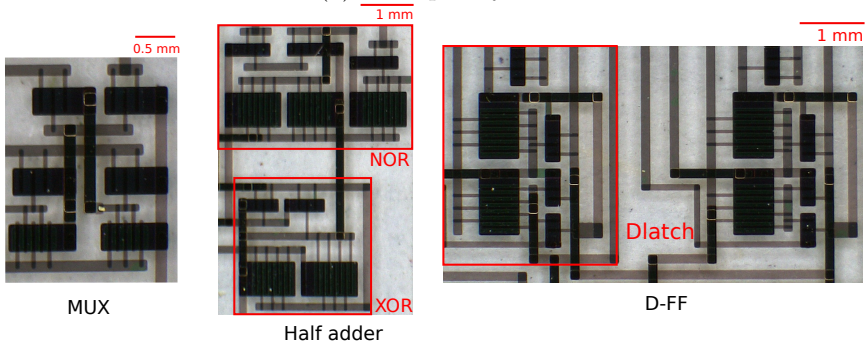


(a) Signal carry rise. (b) Signal carry fall.

Figure 5.20: Transient waveform of output carry signal.



(a) Example layout.



(b) Microphotographs for each component.

Figure 5.21: A proposed 2 bits OISC processor.

confirmed through measurements. Fig. 5.21(b) shows the microphotographs of these components.

Fig. 5.22 shows the measurement result of the multiplexer. The inverted signal of input A ($\bar{A}$) is selected as an output when $C = 0$, whereas $\bar{B}$ is selected when $C = 1$. Fig. 5.23 shows the measured output voltages of half adder for all four input combinations. The sum is the output of the XOR gate and the carry

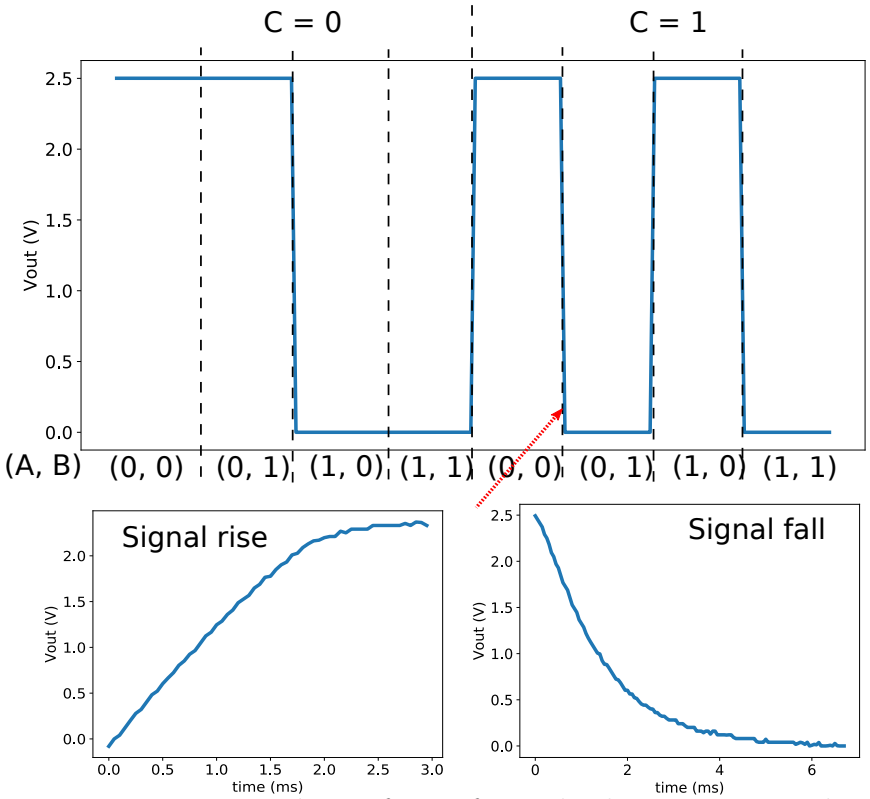


Figure 5.22: Measured waveform of a multiplexer on a test-chip.

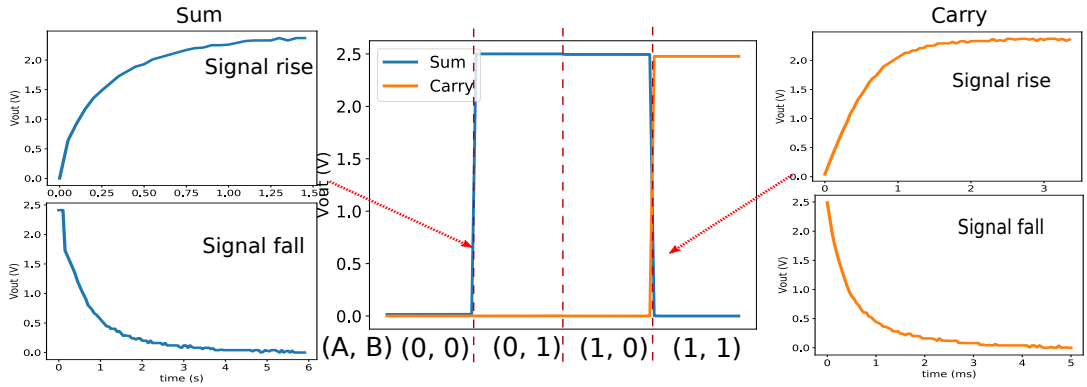


Figure 5.23: Measured waveform of a half adder on a test-chip.

is the output of the NOR gate. These outputs show the correct and ideal logic levels. Table 5.2 summarizes the rise time and fall time of output signals in each OISC processor component. The delays of these circuits are shorter than the delay in the full adder since the constructions are significantly simple. Hence, the speed of the OISC processor is mainly restricted by the full adder.

Table 5.2: Rise and fall times of each component in OISC processor.

Time (ms) / Circuit	Rise time	Fall time
MUX	1.6	2.8
Sum	0.75	1.65
Carry	1.2	1.7

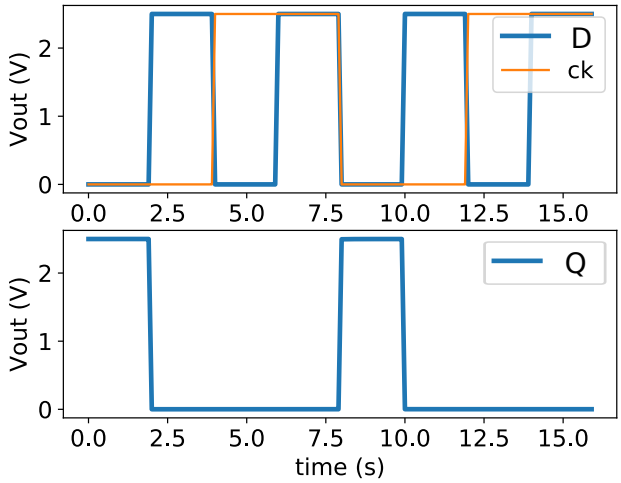
The D-FF used in this work comprises two D-latch with inverted clock input. The dynamic characteristics of D-latch and D-FF are shown in Fig. 5.24. In the D-latch circuit, the input value (D) passes to the output value (Q) when the clock (ck) is low. The output (Q) maintains the input D when the ck is high. In D-FF, Q is set to the value of input D when ck switches from low to high.

Fig. 5.25 shows the verilog simulation output of gtkwave while running a loop program. For simplicity, the loop condition N is set to 3. The "outreg" is the register for the output signal and the "stop" signal is added to inform the suspension of operation. The approximate clock frequency can be calculated from the above measurement results. From Table 5.2, the delay of the full adder is obviously longer than other logic circuits. Hence, the critical path presents in the full adder, considered as the carry signal from the first bit to the last bit. For a 3 bits adder, the worst case is supposed to be 3×15.1 ms (carry fall time) = 45.3 ms. A clock with a 20 Hz frequency can guarantee the correct operation of the OISC processor.

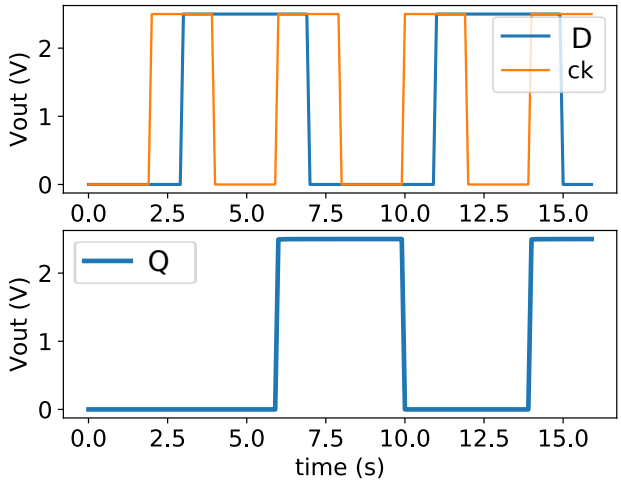
Fig. 5.25 shows the correct operation of the loop program, presenting the feasibility of an OTFT OISC processor based on PTL. While the result also shows that the operation speed is slow. The slow operation is mainly caused by characteristic of the OTFTs since the delay for even a simple OTFTs logic gate is several ms. With the further development of OTFTs, the performance can be expected to boost to an intermediate speed. Moreover, compared with architecture in current use, the OISC architecture also slows down the speed. The extremely lightweight architecture is at the expense of execution time. Some topologies which are supposed to improve the OISC architecture will be discussed in future works in Chapter 6.

5.7 Summary

In this chapter, the circuits based on PTL used for data computing are proposed. The proposed PTL circuits reduce transistor numbers and are mainly constructed by strong p-type OTFTs, leading to a decrease in occupied area and a stable operation. A full adder is used as an example to explain the construction



(a) D-latch.



(b) D-FF.

Figure 5.24: Dynamic characteristics of D-latch and D-FF.

of PTL. Compared to transitional CMOS full adder, the PTL-based full adder reduces the transistor counts by 50%. Based on the gain stage, two types of PTL are proposed. The performances of two PTL circuits are confirmed and the delay of two circuits are compared through simulation. Then as an application of PTL, a lightweight OISC microprocessor based on PTL is discussed. Although the processor is extremely simple, it is Turning complete and can execute any instructions. Through experiments, the feasibility of the PTL-based OISC processor is verified. Each component in the processor is evaluated through

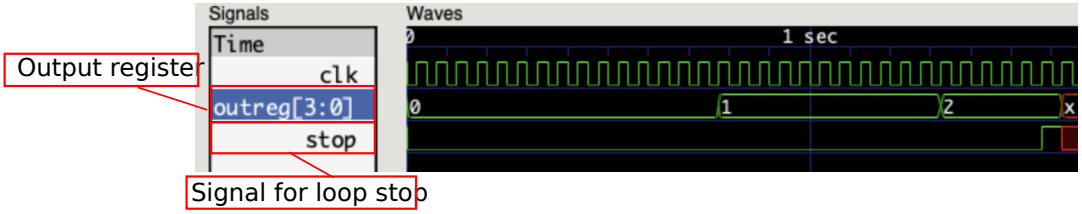


Figure 5.25: Example OISC simulation output of loop program.

test chip measurements. Since the yield of current OTFTs yield is relatively low, the operation of the entire system is confirmed by simulation. While, with the development of OTFT devices, the performance of the OISC processor can be expected to be improved.

Chapter 6

Conclusion

6.1 Summary of this dissertation

The emergence of organic thin-film transistors (OTFTs) enables the development of intelligent IoT products that enrich our lives. The OTFTs offer attractive benefits, such as flexibility, lightness, and decomposability. In addition, OTFTs can be fabricated through low-cost and low-temperature printing processes. In the printing process, circuits can be fabricated on various materials, such as flexible plastic films. As a result of intensive research efforts, considerable improvements have been recently made to both the mobility and on/off current ratio. Therefore, various applications that use OTFTs as principal active device components have been reported.

Meanwhile, besides the improvement of device performance, the periphery circuit of the organic systems used to process or control system data is also a key challenge. At present, most periphery circuits rely on traditional silicon transistors. Although silicon integration offers a short-term solution, this approach requires a high cost manufacturing process, resulting in the loss of the greatest advantage of organic transistors. The transmission between organic and silicon systems reduces efficiency. Therefore, the OTFT-based circuitry regarding the treatment of system local data is required. However, OTFTs are different from traditional silicon devices. OTFTs are unipolar devices and easy to be degraded. Traditional silicon design topology is not suitable for OTFTs circuits. Additional efforts are required to construct stable OTFT circuits.

For example, in a specific flexible application such as smart label fabricated on the packaging of environmentally sensitive products such as wine or vegetables. The environmental condition can be recorded by flexible sensors. At the same time, the information of sensor data and products need to be stored. The security of these data also has to be protected. Moreover, a processor is

required to control and process the data in these systems. In this dissertation, the treatments of local data are considered from three aspects, security, storage, and processing. Firstly. an OTFT PUF circuit used for hardware security is proposed in Chapter. 3. It can be used for smart labels to authenticate the products or protect the information in OTFTs systems. The proposed OTFT PUF adapts a current mirror to achieve self-compensation of unavoidable degradation of OTFTs. Two types of OTFT PUFs are designed to evaluate and compare the metrics as a PUF. Through test-chip measurements, the fabricated PUFs maintain high reliability, showing that the proposed PUF achieves high tolerance response changes caused by device aging.

Secondly, a SRAM used for local data storage of the signals generated by OTFT systems is proposed. The memory cells based on a CMOS design style utilize p-type access transistors to improve area efficiency and stability. A degradation-mitigation circuit, based on a pseudo-CMOS design style, extends retention time. The proposed circuit, which is comprised of a few basic logic gates, is easy to implement and occupies minimum layout area. The SRAM circuit can self-detect degradation and automatically perform a process to mitigate device degradation at the necessary time periods. The operation of key components in the proposed memory via test chip measurement is confirmed. Additionally, the effectiveness of the degradation-mitigation circuit has been verified.

Finally, PTL-based circuits for computing data are proposed in Chapter. 5. The PTL, which decreases transistor counts and mainly depends on strong p-type transistors, is considered to enhance operation stability and save circuit area. As an example, a full adder using PTL is considered. Compare to the traditional full adder, the proposed circuit can reduce by 50% transistor numbers. Furthermore, for full data processing, a lightweight OISC processor based on PTL is proposed. The proposed processor is simple, thus suitable for the OTFTs implementation. Despite its simplicity, it is programmable and can execute any operation. Including the PTL full adder, the components of the OISC processor are confirmed through test chip measurements, indicating the feasibility of the OTFT OISC processor.

6.2 Future works

In closing this dissertation, several potential future works are summarized.

- **Transistors improvements**: At present, the characteristic of OTFTs, such as carrier mobility, is still relatively low compared to silicon devices. This limits the performance of OTFT circuits. Hence, researches on

improving the mobility of organic semiconductor are required. Meanwhile, the improvements in the OTFTs yield are also essential. In this dissertation, the main device fault is the defects in the gate insulator layer, causing a short between the gate electrode and source/drain electrode. To solve this problem, for instance, several high-k dielectric materials with higher insulation property are expected to use as the gate insulator layer [91, 92].

Moreover, besides OTFTs, other types of flexible thin-film transistors with high mobility such as IGZO and ZnO can also be considered to use. As described in Chapter 1, although these TFTs generally require high supply voltage, some researches have been reported to lower the supply voltage [93]. For most of the TFTs, the devices are unipolar, with only a single type of transistor. Hence, the design topologies proposed in this dissertation are general and can be expected to be implemented in other TFT devices.

- **Large-scale circuits evaluation**: In this dissertation, PUF and SRAM circuits are proposed for data security and storage. Both of them use array structures to construct circuits. However, in the test chip measurements, the scale of the circuit was relatively small. For practical use, large-scale array circuits are necessary. In the large-scale circuit, the effects of device variability and wire capacitance are not negligible. It is essential to figure out these effects on circuits. For example, as the memory becomes large, the wires also become rather long. The long wires have high capacitance, leading to long delay and high power consumption. Generally, large memory is partitioned into multiple small memories. However, each memory presents some area overhead for its periphery circuity, thus it is required to find the best trade-off point between the circuit performance and circuit area.

  Meanwhile, to design large circuits, electronic design automation (EDA) tools, such as automatic placement and routing techniques, are necessary. In this dissertation, all layouts are designed manually. The design of standard cells and routing algorithms are expected to optimize these layouts, such as the SRAM array in Chapter 4 and OISC processor in Chapter 5.

- **OISC processor improvements**: In Chapter 5, we show the feasibility of using a PTL-based OISC processor to compute local data and execute a specific operation. However, the extremely simple architecture is at the expense of execution time and memory. There still are remaining works to improve this processor. One of the possible improvements include

the optimization of architecture. For example, Sakamoto, et al. [94] considered a two instructions set computer. By only adding one additional instruction, it is reported that the operation speed significantly becomes faster. Another potential improvement is the parallel operation of OISC processors. Since the construction is extremely simple, it is reasonable to consider parallel processing using multicore OISC processors. It has been reported that multicore OISC processors can outperform existing processors in terms of throughput and energy efficiency for several specific applications [81].

Even with the development of OTFTs, the low cost fabrication inevitably results in inadequate device yield. Although the OISC processor cannot be realized by current OTFTs, it is still considered as a potential approach to mitigate the problem of transistors yield. Since the fabrication cost is low and the circuit is simple, it is possible to fabricate lots of OISC processors in advance. Although all of the processors may not work correctly, we can bond the performable processors to construct a multicore processor. This approach can be expected to reduce the requirement of device yield and simultaneously speed up the operation speed.

- **Hybrid system construction**: At present, it is still difficult for an organic system to completely use current OTFTs for data processing. Hence, the hybrid system using flexible TFT devices and silicon transistors can be considered as a midway approach. As described in this dissertation, the transmission time and power between two systems are inefficient. However there are some researches mitigating these problems by using TFT devices to do some simple pre-processing before data are transmitted to a silicon system [64,95]. For a hybrid system, it is required to determine which operation is suitable for OTFTs and which one is suitable for silicon. For example, in the OTFT PUF system, the control of the giving input challenge and saving output response can be done by OTFTs, while for the communication to the outside I/O devices, using silicon devices is more realizable. For a hybrid system, a design flow is needed to divide the roles of OTFTs and silicon systems for the best efficiency.

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List of Publications

Journals

1. **Zhaoxing Qin**, Kazunori Kuribara, Yasuhiro Ogasahara, and Takashi Sato, "Hybrid CMOS and pseudo-CMOS organic memory for flexible sensors," IEEE Sensors Journal, 2022 (Early access)

2. Yasuhiro Ogasahara, Kazunori Kuribara, Kunihiro Oshima, **Zhaoxing Qin**, and Takashi Sato. "Yield and leakage current of organic thin-film transistor logic gates toward reliable and low-power operation of large-scale logic circuits for IoT nodes," Japanese Journal of Applied Physics, vol. 61, no. SC, 2022

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Awards

1. IEEE Kansai Section Student Paper Award, Febuary 2021

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