Fundamental Study on SiC Metal-Insulator-Semiconductor Devices for High-Voltage Power Integrated Circuits

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Abstract

Through the rapid progress in SiC process technologies, SiC-based devices have attracted increasing attention as high-voltage and ultra-low loss power devices. Although SiC power devices have been investigated as discrete devices, SiC-based high-voltage power integrated circuits (ICs), which include the lateral power devices and its drive, protection, control, and other circuits, provide additional benefits for power electronics. However, for the realization of SiC smart power ICs, there are many problems that need to be solved.

(1) One of the simplest methods to improve metal-insulator-semiconductor field-effect transistor (MISFET) performance is by scaling down MISFET dimensions. However, short-channel effects, which adversely affect the characteristics of MISFETs, may occur. To prevent those from occurring, investigations on short-channel effects in SiC MISFETs are strongly required.

(2) In terms of n-channel SiC MISFETs, channel mobility has not reached a satisfactory level. In addition, only a limited number of p-channel SiC MIS-based devices have been reported. To improve the performance of both n- and p-channel SiC MIS-based devices, intensive study on gate insulators/SiC interface and insulators themselves is desired.

(3) To realize smart power ICs, the most important component is the lateral power device. Until now, the reported SiC lateral power devices have not shown any significant advancement. Therefore, the performance of SiC lateral power devices needs to be improved.

In this thesis, a systematic study on short-channel effects in SiC MISFETs is presented together with an investigation on deposited insulators for the gate materials of both n- and p-channel MIS devices, to enhance the MIS device performance. In addition, the design, fabrication, and characterization of SiC lateral high-voltage MISFETs is discussed, and the record performance of a lateral MISFET is reported.

In Chapter 2, SiC MISFETs with submicron channel were fabricated and short-channel effects in SiC MISFETs were investigated. The critical channel length, for which the long-channel behavior can be observed, was also estimated from experimental and simulation results. The critical channel length of the fabricated metal-oxide-semiconductor FETs (MOSFETs) was longer than that of simulated MOSFETs due to the high density of effective fixed charge at the MOS interface. Based on an original charge-share model, the influence of effective fixed charges at the MOS interface on the short-channel effects was clarified.

In Chapter 3, the interface properties for MIS structures with thermally-grown and

deposited insulators were characterized. In addition to N_2O-grown oxides, deposited SiO_2 annealed in N_2O and deposited SiN_x/SiO_2 annealed in N_2O were applied to gate insulators for SiC MIS capacitors to suppress formation of interfacial transition layer and influence of near-interface traps (NITs). By optimizing the formation process of the gate insulator, the n-MIS capacitors with deposited insulators adequately processed demonstrated an interface state density of $2 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$, which is one-tenth of the interface state density for n-MOS capacitors with N_2O-grown oxides. P-MIS capacitors with deposited oxides were also investigated. In addition to the interface properties, the dielectric properties such as breakdown field and long-term reliability were studied.

In Chapter 4, SiC MISFETs with thermally-grown and deposited insulators were investigated. SiC MISFETs with various insulators were fabricated and characterized. The n- and p-channel MISFETs fabricated on 4H-SiC (0001) with deposited insulators adequately processed demonstrated a high channel mobility of about $30\,\mathrm{cm^2/Vs}$ and over $10\,\mathrm{cm^2/Vs}$, respectively. The channel mobility was improved to $50\,\mathrm{cm^2/Vs}$ in the n-channel MISFETs on 4H-SiC $(000\bar{1})$. An original method to estimate the interface state density near the minority-carrier band edge was proposed. The crystal face dependencies of channel mobility and interface properties were also discussed.

In Chapter 5, SiC lateral high-voltage MISFETs with a new structure were designed. To decrease the drift resistance, double and triple reduced surface field (RESURF) structures were proposed. The double RESURF MISFETs exhibited superior characteristics to the triple RESURF MISFETs. After optimization of device structure by using device simulation, the simulated MISFETs exhibit a high breakdown voltage over 1.2 kV and a low drift resistance below $15\,\mathrm{m\Omega cm^2}$. The advantages of the proposed structure were also discussed.

In Chapter 6, SiC lateral high-voltage MISFETs were fabricated and characterized. The double RESURF structure is effective not only to decrease the drift resistance but also to increase the breakdown voltage. From the temperature dependence, the additional advantages of the double RESURF MISFETs were found out. By utilizing 4H-SiC $(000\bar{1})$, the MISFETs demonstrated a high breakdown voltage of 1580 V and a low ON-resistance of $40\,\mathrm{m\Omega cm^2}$, which is the best performance among any lateral MISFETs ever reported.

In Chapter 7, a summary of the present work is given, together with the issues yet to be solved and suggestions for future work.

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Chapter 1

Introduction

1.1 Background

Since the end of World War Ⅱ, many countries of the world have benefited from a rapid economic growth. The technological progress, as well as the increase of availability of consumer goods, has indeed improved the quality of life of modern society but it has come to a cost. In the 21st century, we must address the issues posed by the economic growth.

One of key issues that we are coming up against now is the global climate change caused by greenhouse gas (GHG)[1] emissions resulting from energy consumption. Our economic growth stands on top of large emissions of GHG. As it is shown in Fig. 1.1, the total final consumption of energy in the world was 4.7 billion tonnes of oil equivalent (toe) in 1973 and increased up to 8.1 billion toe in 2006 [1]. Figure 1.2 (a) shows that the annual GHG emissions have grown by about 70 % between 1970 and 2004. Figure 1.2 (b) indicates that the carbon dioxide (CO_2), which is emitted due to the burning of fossil fuels, is the most important anthropogenic GHG and is generated mainly by energy supply system, transportation, and industry (Fig. 1.2 (c)) [2].

It is evident from these data that the increase of GHG emissions is closely related to the increase of energy consumption and it is well established that the change of atmospheric GHG concentration alters the energy balance of the climate system, causing climate change. The international energy agency (IEA) reported that the world's primary energy demands are projected to grow by 55 % between 2005 and 2030 [3]. For this reason, now is the time to address the serious problem of energy consumption. The main challenge of the 21st century is to reduce GHG emissions avoiding economic recession, which is vital for both maintaining and improving the standards of life of society.

One way of resolving this dilemma is by a more efficient use of energy. In the sector of energy supply, nearly half of the energy generated at power plants is converted to electric power. The electricity is transmitted to consumers through a great number of power devices, and partly lost at each device. In the sector of industry, many power devices are used

[1] GHGs are carbon dioxide (CO_2), methane (CH_4), nitrous oxide (N_2O), sulphur hexafluoride (SF_6), etc.

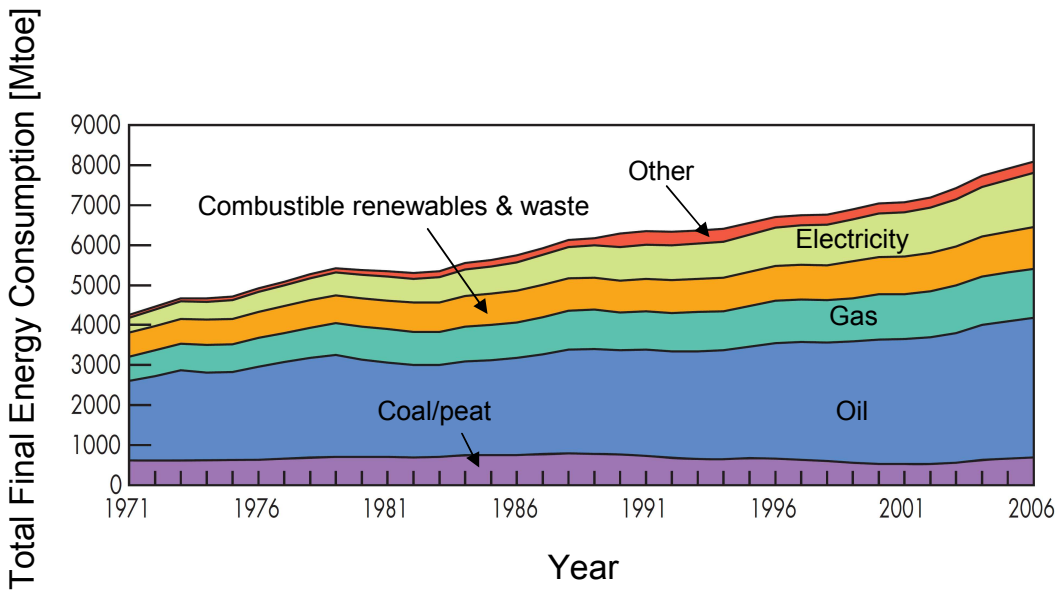


Figure 1.1: Evolution from 1971 to 2006 of total final energy consumption in the world [1].

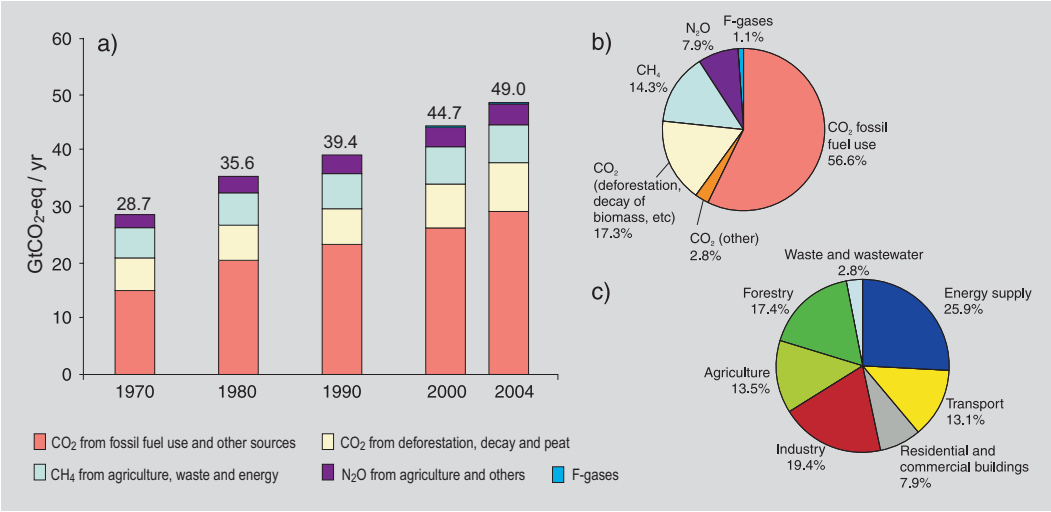


Figure 1.2: Global anthropogenic GHG emissions [2]. (a) Global annual emissions of anthropogenic GHGs from 1970 to 2004. (b) Share of different anthropogenic GHGs in total emissions in 2004 in terms of CO_2-equivalent. (c) Share of different sectors in total anthropogenic GHG emissions in 2004 in terms of CO_2-equivalent.

in production facilities to control inverter-driven motors, etc. In addition, in the sector of transport, hybrid electric vehicles (HEVs) which have power control unit (PCU) will dominate the automobile market, although gasoline-powered vehicles still dominate. The power devices that are used to control the motor current are contained within PCU, and the performance of power devices directly affects the performance of HEVs. Distribution of electricity to households, vehicles, and manufacture facilities rely on the use of power devices, whose efficiency is hindered by power losses, and the improvement of these devices will be of primary importance in the foreseeable future, in order to help reducing GHG emissions.

Nowadays, almost all power devices are made of silicon (Si) due to the availability of high-quality and large-area wafers, the excellent native oxide (SiO_2), and its mature process technology. The performance of the Si power devices has improved by optimizing device structures, introducing new device concepts, etc., and has been approaching the theoretical limit predicted by the material properties. To overcome the "Si limit", alternative semiconductor materials are strongly desired. Silicon carbide (SiC) is one of the most promising candidates, among semiconductor materials, to realize ultra-highly efficient power devices, owing to its superior properties.

1.2 Silicon Carbide Devices

1.2.1 Properties of SiC

SiC is a group Ⅳ–Ⅳ compound semiconductor composed of tetrahedrally bonded silicon (Si) and carbon (C) atoms in a close-packed structure. Due to the strong bonding of Si–C, SiC has superior thermal and chemical stabilities, and has been widely used for polishing powders and heat-resistant coatings over about 100 years. SiC is also a versatile material because of the numerous polytypes, which are one-dimensionally different crystal structures with the same chemical composition. Considering the Si–C pair as a sphere, there are three possible occupation sites denoted by A, B, and C as shown in Fig. 1.3. For example, the B- or C-site bilayer can be placed on the A-site bilayer. Two simple stacking sequences are ABCABC... and ABAB..., so-called "zincblende" and "wurtzite" structures, respectively. More than 200 polytypes have been found in the case of SiC. The most popular and important polytypes for electronic device applications are 3C-, 4H-, and 6H-SiC. In Ramsdell's notation [4], polytypes are represented by the number of bilayers in the unit cell and the crystal structure (C for cubic and H for hexagonal). 3C-SiC is often called β-SiC, and others are called α-SiC. The schematic structures of 3C-, 4H-, and 6H-SiC are shown in Fig. 1.4. The mechanical properties are almost invariant with polytype, whereas the electrical and optical properties do drastically change with the polytype. Polytype control during crystal growth of SiC is a crucial issue, because inclusions of other polytypes deteriorate device performance severely. With the stable physical and chemical characteristics of SiC, it had

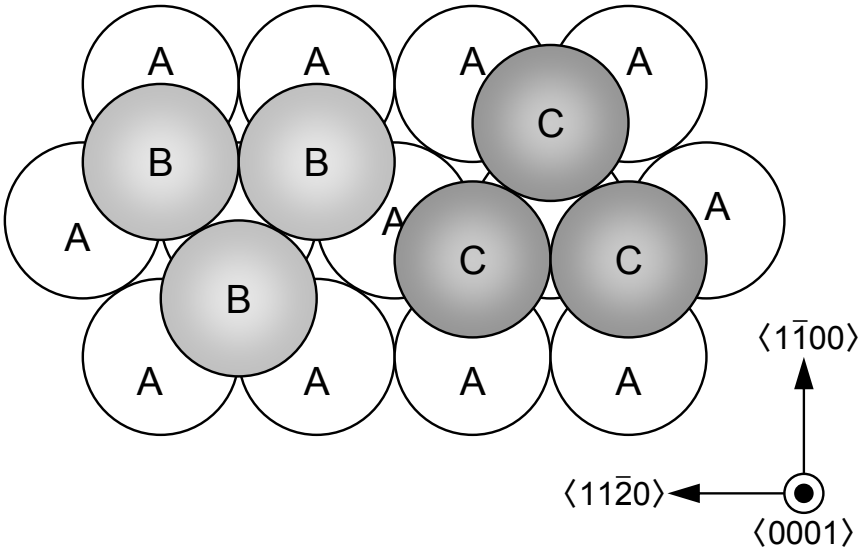


Figure 1.3: Hexagonal close packing of Si–C pairs.

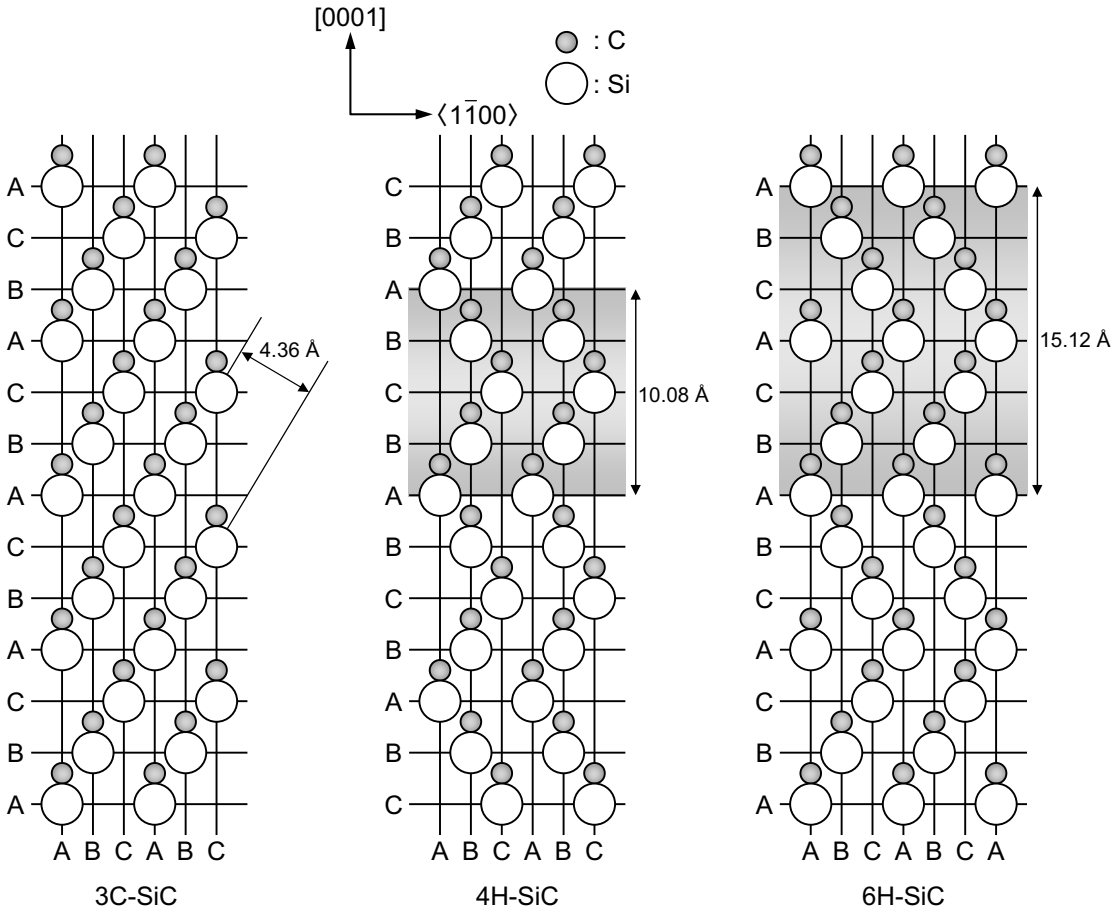


Figure 1.4: Stacking orders along c-axis for 3C-, 4H-, and 6H-SiC. Open and closed circles represent Si and C atoms, respectively.

historically been difficult to obtain high-quality and large-area single crystals without any inclusions of other polytypes.

In the 1980s, two major accomplishments in crystal growth of 6H-SiC were achieved. The first one was the development of a large-area bulk growth technique called "seeded sublimation" or "modified Lely method" [5]. This method has become a standard technique to grow high-quality and large-area 4H- and 6H-SiC bulk crystals through the optimization of furnace design and thermal distribution during growth. The size of 4H- and 6H-SiC wafers commercially available is 50–100 mm in diameter. Low resistivity (about 0.015 Ωcm) and semi-insulating (over 10^5 Ωcm) wafers are also commercially available. Furthermore, an ultra high-quality SiC single crystal has been developed [6].

The second breakthrough was the successful development of epitaxial growth on off-oriented 6H-SiC (0001) substrates by chemical vapor deposition (CVD) [7]. This technique is called "step-controlled epitaxy", and its growth mechanism has been discussed in detail [8, 9]. By using step-controlled epitaxy concepts, device-quality epitaxial layers of 4H- and 6H-SiC can be obtained without any inclusions of other polytypes at growth temperatures of about 1500 °C, which are over 300 °C lower than previous methods. Both n- and p-type dopings can be controlled in a wide range (10^{14}–$10^{19}\,\mathrm{cm}^{-3}$) by introducing N_2 for n-type and trimethylaluminum (TMA: $Al(CH_3)_3$) for p-type.

After these achievements, SiC research work has been markedly accelerated. Almost all research and development for device fabrications on α-SiC are made by using step-controlled epitaxial layers on off-oriented {0001} substrates cut from modified Lely-grown bulk crystals.

The physical properties of SiC are different for each polytype, as listed in Table 1.1, in which Si, gallium arsenide (GaAs), and gallium nitride (GaN) are also shown. The high bonding energy of Si–C atoms (4.53 eV) with short bond length (1.89 Å) [10] leads to a large energy difference between "bonding" and "anti-bonding" states, resulting in a wide bandgap [11]. For example, the bandgap of 4H-SiC at room temperature (RT) is 3.26 eV, suggesting that devices fabricated from this material can operate successfully at high temperatures. The breakdown electric field of 3 MV/cm is one-order-of-magnitude higher than those of Si and GaAs [12]. This parameter is important to reduce ON-resistance (R_{ON}) in power devices, as discussed later. The high saturation drift velocity (2×10^7 cm/s) enables devices to operate at high frequencies [13]. Heat generated in devices by Joule heating can easily be transferred to a heat sink due to the high thermal conductivity of SiC (5 W/cmK) [14]. Among 3C-, 4H-, and 6H-SiC, 4H-SiC is considered to be the most suitable polytype for power devices, because of a wider bandgap and smaller anisotropy of the mobility. Due to the above mentioned superior material properties of 4H-SiC, power devices made of 4H-SiC are expected to show several advantages compared to those fabricated by Si and GaAs, as discussed in the following subsection. GaN also shows excellent physical properties. Since GaN-based blue light-emitting diodes (LEDs) were developed in the early 1990s [15], research work on GaN has received strong efforts to realize short-wavelength laser

Table 1.1: Important physical properties, and technological status of various polytypes of SiC along with other common semiconductor materials (data given for room temperature).

Property	SiC			Si	GaAs	GaN
	3C	4H	6H			
Crystal Structure	ZB	4H	6H	Dia.	ZB	W
Lattice Constant [Å]	4.36	a = 3.09 c = 10.08	a = 3.09 c = 15.12	5.43	5.65	a = 3.19 c = 5.19
Band Structure	I.D.	I.D.	I.D.	I.D.	D.	D.
Bandgap [eV]	2.3	3.26	3.02	1.12	1.42	3.42
Electron Mobility [cm^2/Vs]	1000	1000 ($\perp$ c) 1200 (//c)	450 ($\perp$ c) 100 (//c)	1500	8500	1200
Hole Mobility [cm^2/Vs]	50	120	100	450	400	50
Electron Saturation velocity [10^7 cm/s]	2.7	2.2	1.9	1	1	2.7
Breakdown Field [MV/cm]	2	3	3	0.3	0.4	3
Thermal Conductivity [W/cmK]	4.9	4.9	4.9	1.5	0.46	1.3
Relative Permittivity	10	9.7 ($\perp$ c) 10.2 (//c)	9.7 ($\perp$ c) 10.2 (//c)	11.9	12.8	10.4
Conductivity Control	△	◯	◯	◯	◯	△
Thermal Oxide	◯	◯	◯	◯	×	×
Conductive Wafer	△ (Si)	◯	◯	◯	◯	△ (SiC)
Insulating Wafer	×	◯	◯	△ (SOI)	◯	△ (Sapphire)

ZB: Zincblende Dia.: Diamond W: Wurtzite
I.D.: Indirect D.: Direct
◯: Excellent △: Fair ×: Difficult

diodes and high-power and high-frequency devices. However, some difficulties in crystal growth such as a narrow doping range (especially in p-type material), a high density of defects in grown layers, and immature device technologies such as ion implantation process remain unsolved.

1.2.2 Present Status and Future Prospects of SiC Devices and Circuits

One of the advantages of SiC is a large breakdown electric field (about 3 MV/cm). In general, the breakdown voltage of semiconductor devices (V_{B}) with an abrupt one-dimensional junction is represented as the area of triangle shown in Fig. 1.5 and is described as:

$$V_{\mathrm{B}} = \frac{E_{\mathrm{B}} W_{\mathrm{M}}}{2}, \tag{1.1}$$

where E_{B} is the breakdown electric field and W_{M} the maximum width of depletion region. At the breakdown, the maximum depletion width is given by:

$$W_{\mathrm{M}} = \frac{\varepsilon_{\mathrm{S}} E_{\mathrm{B}}}{e N_{\mathrm{B}}}, \tag{1.2}$$

where ε_{S} is the permittivity of the semiconductor, e the elementary charge, and N_{B} the doping concentration of the semiconductor. In power devices, a reasonably high breakdown voltage is generally required. The drift region to support the breakdown (with the doping concentration of N_{B}) in the device must be thicker than the maximum width of depletion region. From Eq. 1.1 and Eq. 1.2, the breakdown voltage of semiconductor devices is expressed as:

$$V_{\mathrm{B}} = \frac{\varepsilon_{\mathrm{S}} {E_{\mathrm{B}}}^2}{2 e N_{\mathrm{B}}}. \tag{1.3}$$

Equation 1.3 tells high breakdown electric field and low doping concentration are required to achieve the high breakdown voltage. Since the breakdown field is essentially intrinsic to the semiconductor material (not a parameter which can be adjusted by device design), reasonably thick semiconductor layers with reasonably low doping concentrations must be realized. Conversely for a given breakdown voltage, Eq. 1.3 permits the doping concentration to be high in proportion to the square of breakdown field, and Eq. 1.1 allows the maximum width of depletion region to be thin according to the reciprocal of breakdown electric field.

For the forward bias condition (ON-state), the drift region behaves as a resistor in unipolar devices. The drift resistance (R_{Drift}) for unipolar devices can be calculated by [16]:

$$R_{\mathrm{Drift}} = \frac{4 {V_{\mathrm{B}}}^2}{\varepsilon_{\mathrm{S}} \mu {E_{\mathrm{B}}}^3}, \tag{1.4}$$

where μ is the carrier mobility in the semiconductor. Equation 1.4 tells that for a given breakdown voltage, the drift resistance is inversely proportional to the carrier mobility and

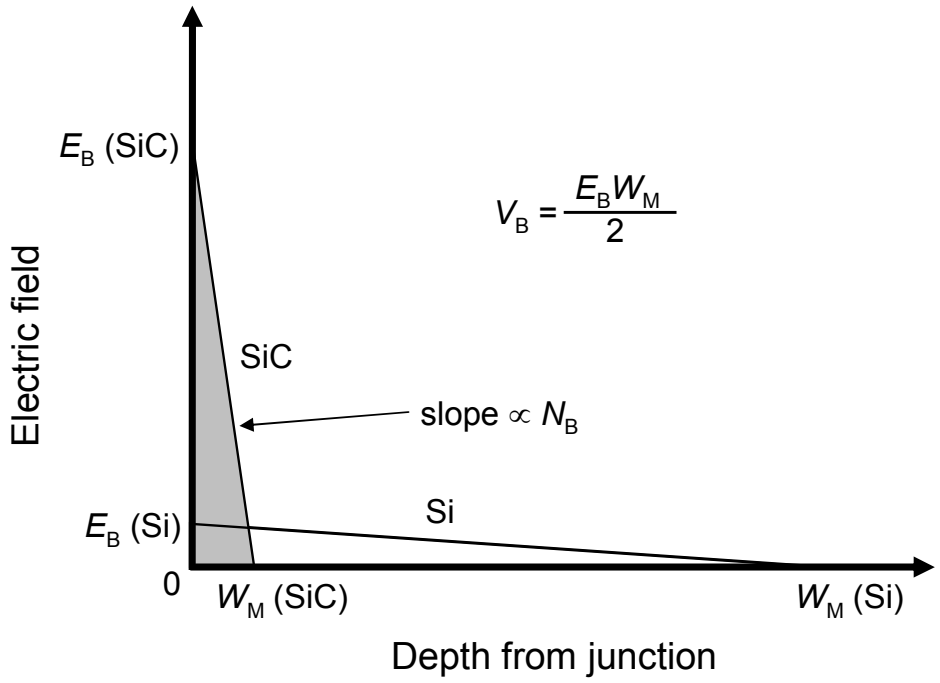


Figure 1.5: Distribution of electric field for Si and SiC abrupt one-dimensional junction at breakdown.

the cube of breakdown field. In the unipolar device with an optimum structure, the drift resistance is the dominant resistance component of the ON-resistance, and other resistance components can be negligible. Thus, a decrease in the drift resistance brings a significant reduction of power losses because a power device handles a great deal of current. The power losses in a device are completely converted to heat, increasing the temperature at the junction. If the junction temperature is raised above a critical value (T_C) determined mainly by the bandgap (E_G) of the semiconductor material ($T_C \propto E_G$), the devices fail to operate and may be damaged.

A higher breakdown electric field of SiC, compared with Si and GaAs, allows the design of SiC power devices with a thinner and more highly doped voltage-blocking layer, resulting in more than 100 times lower drift resistance than Si devices with the same breakdown voltage. The high thermal conductivity takes away the heat produced by power losses, enduring higher power losses from high current (or large device capacity) or high-frequency switching. Furthermore, SiC devices can operate at much higher temperature than Si and GaAs devices, owing to the wide bandgap and high thermal stability of SiC. Thus, SiC is expected to realize much higher efficiency and much wider operating range than ever achieved with Si and GaAs, as shown in Fig. 1.6 [17].

Marked progress has been made in SiC technology for manufacturing power devices and applications, in the last decade. Intensive studies on fundamentals of SiC Schottky barrier diodes (SBDs) [18] as well as on practical issues such as reliability [19] and scaling-up [20] have led to commercial production of 300 V-, 600 V-, and 1.2 kV-class 4H-SiC SBDs [21, 22]. The superior switching behavior in SBDs (without reverse recovery as in *PiN* diodes) and the simplification of the cooling system (due to lower switching loss for SBDs and to higher thermal endurance of SiC devices) favor SiC SBDs for power modules needing power rectifiers.

While the first commercially available SiC power devices were SBDs [21], SiC power "switching" devices have been investigated extensively. As a general trend in power switching devices, metal-oxide-semiconductor (MOS)-gated power devices, which are controlled by voltage applied to gate, has been regarded as an ideal device because of capability of fast switching and simple gate-drive circuits. Although SiC normally-ON junction field-effect transistor (JFET) with Si normally-OFF MOSFET has already released as normally-OFF switch [23], expectation for SiC MOS-based devices has been raised because SiC is the only compound semiconductor to produce SiO_2 by thermal oxidation like in Si. The development of SiC MOS-based devices is advanced in the field of unipolar switching devices such as SiC MOSFETs (MOSFETs) for blocking voltages between 600 V and approximately 5 kV. SiC bipolar devices such as insulated gate bipolar transistors (IGBTs) are also attractive in terms of low ON-resistance owing to the effect of conductivity modulation for devices with a blocking voltage of more than 5 kV. Here we consider MOSFETs and IGBTs, as they are the most important semiconductor power switching devices in power electronics. In this section, we focus attention on vertical-type power devices, and lateral-type power devices

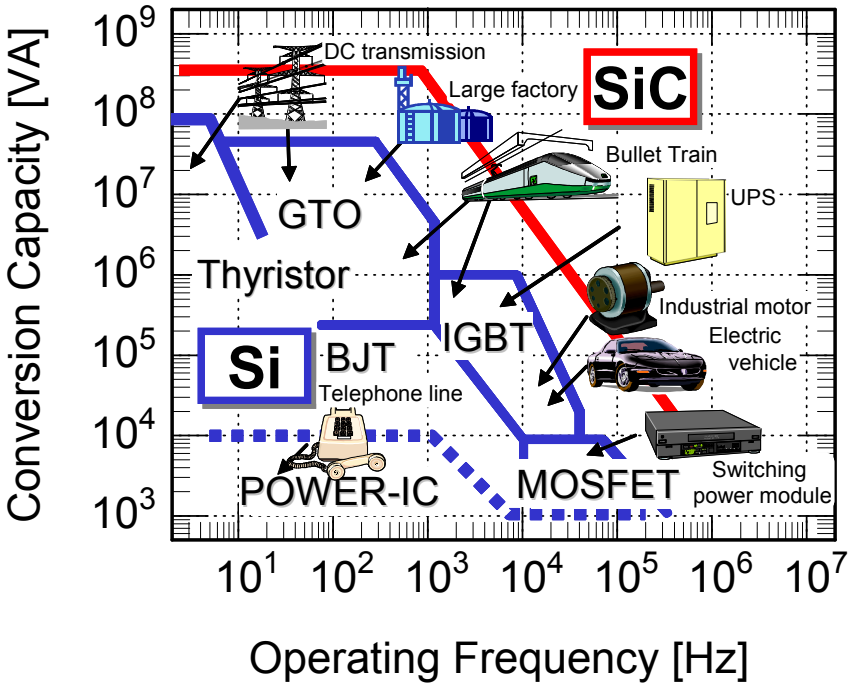


Figure 1.6: Possible range of operation for Si and SiC power devices [17].

are discussed in Section 1.3.3.

SiC power MOSFETs have been investigated extensively as discrete devices. Since the first 6H-SiC power U-shaped MOSFET (UMOSFET), with a blocking voltage of 50 V and a specific ON-resistance of 38 $m\Omega cm^2$, was reported in 1993 [24], the performance of SiC power MOSFETs had been limited by its low inversion channel mobility (several cm^2/Vs for 4H-SiC (0001)) [25, 26] due to its high interface state density. However, several successful developments to enhance the channel mobility (detail will be introduced in Section 1.3.2) have been proposed, and a lot of SiC power MOSFETs, which significantly outperform the theoretical limit of Si unipolar devices, have already been demonstrated. Figure 1.7 shows the relationship between breakdown voltage and ON-resistance for major vertical 4H-SiC MOSFETs reported to date. For example, 660 V-1.8 $m\Omega cm^2$ double-implanted MOSFET (DMOSFET) [27], 1050 V-6.95 $m\Omega cm^2$ DMOSFET [28], and 790 V-1.7 $m\Omega cm^2$ UMOSFET [29] were realized. These ON-resistances of the reported SiC MOSFETs have already become lower than that of Si IGBTs with the same blocking voltage. Although there is room for improvement in channel mobility, the recent trend in SiC MOSFETs is changing from the reduction of the ON-resistance to the increase of the reliability, especially at high temperature, taking practical use into consideration. The reliability of gate oxides on SiC has been investigated, and there are concerns that the dislocations in SiC adversely affect the long-term reliability of gate oxides [30–32]. The typical charge-to-breakdown (Q_{BD}) of the gate oxides thermally grown on 4H-SiC (0001) is 0.01–1 C/cm^2, which is lower than the charge-to-breakdown of thermal oxides on Si (about 50 C/cm^2) [30]. The charge-to-breakdown of the gate oxides on SiC can be improved by "nitridation" and/or utilizing deposited oxides (about 10–100 C/cm^2) [33–35]. SiC vertical power MOSFETs edge closer to practical use and will be commercially released in a few years.

Recently, investigations on SiC IGBTs have started on ultra high-voltage (more than 5 kV) applications. Since the *n*-channel IGBTs are common for Si, SiC IGBTs have been investigated basically on *p*-channel structure to avoid the high resistance of p^+-substrate due to relatively-low carrier concentration of p^+-substrate (about $10^{17}\,cm^{-3}$). After the first 6H-SiC *p*-IGBT with UMOS structure was reported in 1996 [36], the performance of SiC IGBTs has been improved through epitaxial and process technologies. Although the large built-in potential (about 3 eV) in SiC, which is a disadvantage compared with Si, leads to a relatively high forward voltage drop at the ON-state, SiC *p*-IGBT with a blocking voltage of 7.5 kV exhibits a low differential ON-resistance of 26 $m\Omega cm^2$ (a specific ON-resistance of 48 $m\Omega cm^2$) at a collector voltage of about -7 V [37], which is half or even lower than the specific ON-resistance of 10 kV 4H-SiC DMOSFET [38]. One of unsolved issues in SiC *p*-IGBTs is the non-optimized process to form *p*-type MOS channel.

SiC integrated circuits (ICs) are one of the most important applications of SiC MOS-based devices. To apply Si-based logic circuits to gate-drive and/or protection circuits of SiC power devices, these circuits must be isolated from these SiC power devices due to the operational temperature limitation of Si-based systems. On the other hand, SiC-based

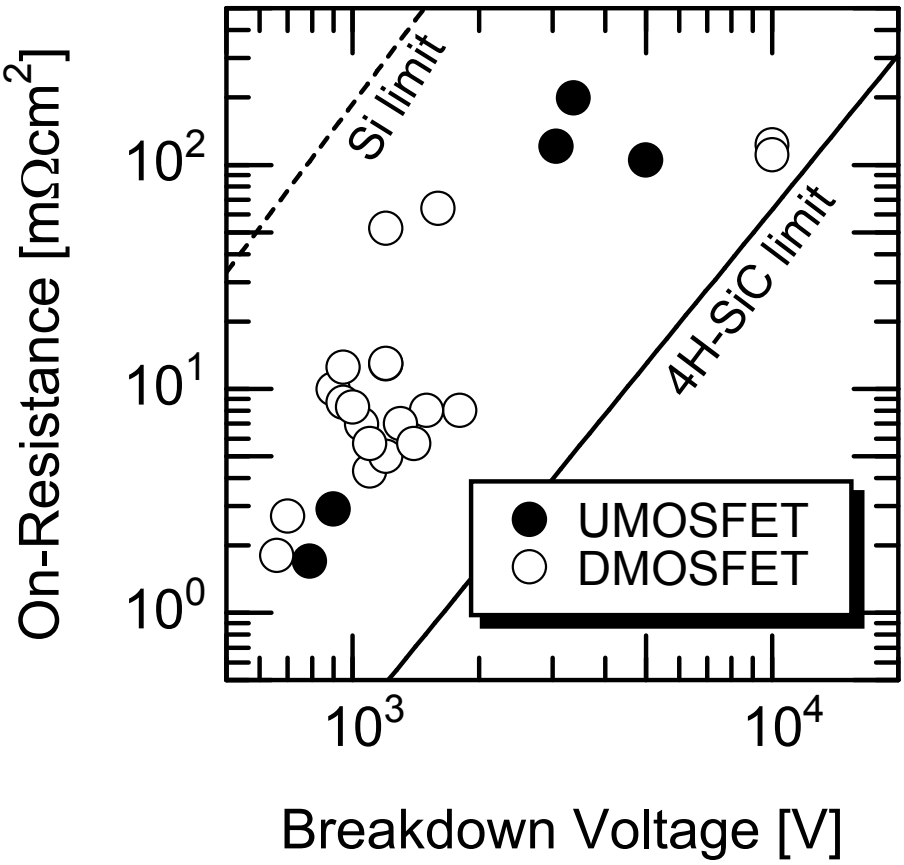


Figure 1.7: Relationship between breakdown voltage and ON-resistance for major vertical 4H-SiC MOSFETs. Open circles mean DMOSFETs and closed circles UMOSFETs. Dashed line denotes theoretical performance of Si unipolar device and solid line that of 4H-SiC unipolar device, which are predicted by material properties.

monolithic circuits overcome the operational temperature limitation. Some groups have already reported an SiC complementary MOS (CMOS) inverter operating at 300 °C [39, 40], which is the key component of SiC-based ICs. The high temperature operation in SiC ICs is the strong advantage compared with Si ICs.

1.2.3 Demands for SiC High-Voltage Power Integrated Circuits

One of major trends in power electronics is the integration of power devices with its drive, protection, control, and other ICs. This kind of application, called power IC, has been intensively developed, and Si power ICs have already been used in many fields such as motor control, electronic power supply, automobiles, displays, etc. Compared to discrete power devices, power ICs have several advantages. For example, the number of components can be reduced, allowing the system to be downsized, and the design can be simplified. The demands for power ICs will continue to grow.

The most important component of power IC is a lateral high-voltage power device. In general, there are various kinds of lateral power devices such as MOSFET, JFET, IGBT, and high electron mobility transistor (HEMT). Si lateral power MOSFETs and IGBTs have been already put to practical use in power ICs. However, the difficulty of device design limits the performance of Si lateral power MOSFETs and IGBTs. For further improvement of the power ICs, the introduction of new device concepts and/or new material is desired.

One of emerging lateral power devices is GaN HEMT. Although GaN HEMTs have already demonstrated remarkable characteristics [41, 42], it is difficult to integrate GaN HEMTs with its control ICs because CMOS circuits are hardly fabricated on GaN. In addition, GaN HEMTs are basically normally-ON, which means that complicated design of gate-drive circuits is needed.

As mentioned above, SiC power devices have been recognized as a promising candidate for low-loss power devices for advanced electronic systems. In addition, n- and p-channel MOSFETs can be fabricated on SiC, which means that CMOS circuits can also be integrated on SiC. Therefore, high-voltage smart power ICs can be realized on SiC by integrating both high-voltage lateral power devices and low-voltage ICs. SiC power ICs have great advantages such as simplified circuits, reduction of module size, and improvement of heat radiation. For these reasons, the demand for SiC power ICs is expected to grow and power electronics will benefit from the realization of SiC power ICs.

SiC high-voltage power ICs consist mainly of two components, low-voltage ICs and high-voltage lateral power devices. The former has several issues that need to be solved. For example, channel mobility in both n- and p-channel SiC MOSFETs is low and fundamental studies on p-channel devices are still missing. In addition, to enhance the performance of CMOS circuits, it is important to reduce the channel length. However, the short-channel effects in SiC MOSFETs have not been examined yet. In terms of lateral power devices, there is still room for improvement. In facts, studies on the optimization of device structure

and/or introduction of new device concepts such as super junction [43] are needed. These issues will be discussed in the next section.

1.3 Key Issues for SiC High-Voltage Power Integrated Circuits

1.3.1 Short-Channel Effects

The downsizing of MOSFETs is the simplest method to enhance the performance. Since the early period of Si MOS devices, researchers have continuously tried to scale down MOSFET dimensions. A smaller size enables higher device density in an IC and higher channel density in a vertical power device. In addition, smaller channel length (L_{Ch}) improves the driving current, which contributes to the enhancement of device performance in ICs and the reduction of ON-resistance in power devices, because drain current (I_{D}) is inversely proportional to channel length ($I_{\mathrm{D}} \propto 1/L_{\mathrm{Ch}}$). For these reasons, the size of MOSFETs decreases year by year [2].

Although the first Si MOSFET reported in 1960 had a channel length of 20 μm [44], Si MOSFET with a short-channel length below 10 nm was demonstrated in 2003 [45]. The minimum feature length in Si commercial ICs has been reduced by more than two orders of magnitude ($L_{\mathrm{Ch}} < 0.1\,\mu$m). In general, the performance of Si MOSFETs for both ICs and power electronics has improved by shrinking MOSFET dimensions. However, MOSFETs need to be designed properly to preserve, as much as possible, the long-channel behavior when the MOSFETs shrink. As the channel length decreases, the depletion width extended from the source and drain regions becomes comparable to the channel length and the potential distribution between the source and drain regions two-dimensional. This two-dimensional potential distribution results in undesirable electric behavior named "short-channel effects". The short-channel effects are recognized as (1) reduction of threshold voltage, (2) drain-induced barrier lowering, (3) punchthrough behavior, (4) deterioration of subthreshold characteristics, etc., and these effects should be minimized.

In the conventional MOSFETs, a rule of thumb for avoiding the short-channel effects is simply to scale down all dimensions and voltage of a long-channel MOSFET so that the internal electric fields are kept the same [46]. However, in practice, it is difficult to downsize the MOSFET dimensions with same scaling factor when the dimensions are extremely small (below 100 nm), due to the increasing influence of non-scalable parameters, such as the built-in potential. Therefore, a generalized guideline for scaling down of MOSFETs with flexible scaling factors suppressing the short-channel effects has been proposed [47].

[2] To take an instance, the international technology roadmap of semiconductors (ITRS) 2007 exhibits the half cell pitch of dynamic random access memory (DRAM) will be decreased to 25 nm in 2015 from 65 nm in 2007.

This generalized guideline can be expressed as:

$$L_{\mathrm{Crit}} = C\{r_{\mathrm{j}} d_{\mathrm{OX}} (W_{\mathrm{S}} + W_{\mathrm{D}})^2\}^n, \tag{1.5}$$

where L_{Crit} is the critical channel length for which long-channel behavior can be observed, C and n the constant, r_{j} the junction depth in μm, d_{OX} the oxide thickness in Å, and W_{S} and W_{D} the depletion width from the source and drain regions in μm, respectively. Figure 1.8 (a) shows these device parameters. In Si MOSFETs, the results of many experimental and simulation studies led to a constant C of $0.41\,\text{Å}^{-1/3}$ and a constant n of 1/3 as shown in Fig. 1.8 (b). This generalized guideline is very useful because the device parameters need not be scaled by the same factor.

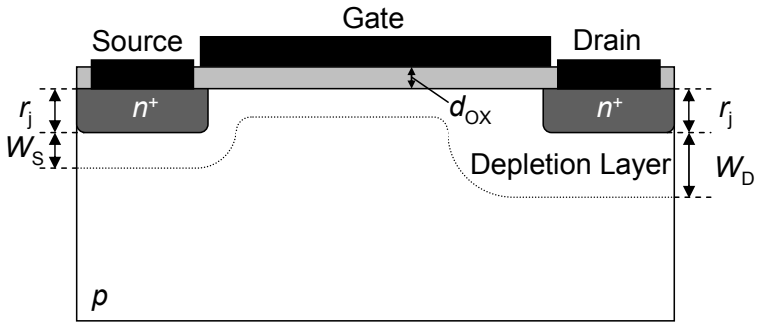
Until now, the understanding of short-channel effects in SiC MOSFETs has been lacking even though the short-channel effects inevitably occur when decreasing the channel length. Compared to Si, SiC has a wide bandgap and different material properties. Thus, there is the possibility that the short-channel effects in SiC MOSFETs may be different from those in Si MOSFETs. In addition, the critical channel length of SiC MOSFETs is not yet understood. Therefore, fundamental studies on the short-channel effects in SiC MOSFETs are strongly required.

1.3.2 Insulator/SiC Interfaces and Channel Mobility in *N*- and *P*-Channel MISFETs

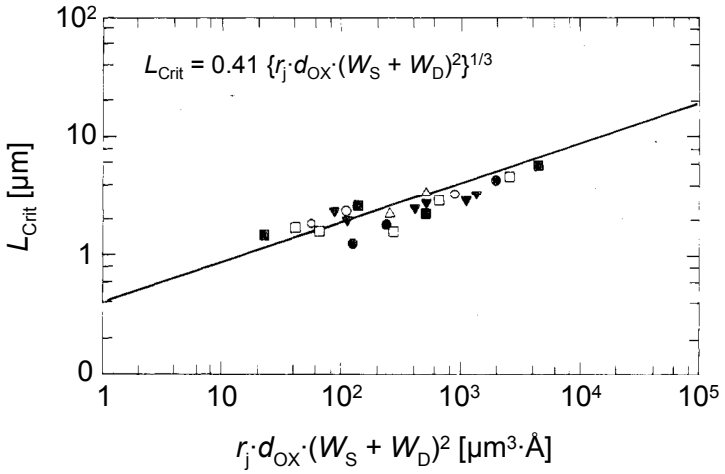
One of the most important properties of SiC is the fact that SiC can be thermally oxidized to grow insulating SiO_2 layers, which are known to have superior dielectric properties for MOS-based devices. The quality of thermally grown oxides on SiC, in terms of breakdown electric field, is comparable to that of SiO_2 layers grown on Si [48]. Thus, the thermally-grown oxides can be applied to gate oxides of MOS-based devices. In addition, other dielectrics are also investigated as alternative gate materials for SiC metal-insulator-semiconductor (MIS)-based devices [49, 50]. These SiC MIS process technologies have focused mainly on n-channel MISFETs (MISFETs) because electrons show higher bulk mobility (about $1000\,\text{cm}^2/\text{Vs}$) than holes (about $120\,\text{cm}^2/\text{Vs}$) [51]. However, the importance of p-channel MISFETs has been increasing as the component of p-IGBTs and CMOS-based applications. Therefore, both n- and p-channel MISFETs (or MOSFETs) on SiC with superior performance are desired.

N-Channel MISFETs

The performance of 4H-SiC n-channel MISFETs directly influences that of both lateral power devices and low-voltage ICs. High channel mobility leads to the decrease of channel resistance in lateral power devices and to the decrease of device area in ICs. SiC n-channel MISFET performance had suffered from its low channel mobility due to its high interface



(a)



(b)

Figure 1.8: (a) Schematic structure of MOSFET with device parameters. (b) Generalized guideline for scaling down of MOSFETs [47]. L_{Crit} means the critical channel length for which long-channel behavior can be observed, r_{j} the junction depth in μm, d_{OX} the oxide thickness in Å, and W_{S} and W_{D} the depletion width of source and drain regions in μm, respectively. In (b), symbols are experimental data obtained in Si MOSFETs with various parameters. The junction depth, the drain voltage, the acceptor concentration of the bulk, and the gate oxide thickness are varied.

state density near the conduction band edge. The density of interface states at dry O_2-oxidized SiO_2/4H-SiC (0001) interface (about $10^{13}\,cm^{-2}eV^{-1}$) [25, 26] is about two orders of magnitude higher than that at the SiO_2/Si interface (10^{10}–$10^{11}\,cm^{-2}eV^{-1}$).

To overcome the problem of low channel mobility, various methods have been investigated. For example, the utilization of other crystal faces such as 4H-SiC $(000\bar{1})$ [52], $(11\bar{2}0)$ [53], and $(03\bar{3}8)$ faces [54] is effective to improve the interface properties (see Fig. 1.9 for the most widely studied crystal planes). 4H-SiC n-channel MOSFETs on these faces exhibit a channel mobility of over $100\,cm^2/Vs$. The oxidation, or re-oxidation, in either NO or N_2O is another attractive process to increase the channel mobility [55–57]. This "nitridation" process is useful to improve the channel mobility in 4H-SiC n-channel MOSFETs on both (0001) face (about $20\,cm^2/Vs$) and other faces (over $30\,cm^2/Vs$) [58] and is widely accepted for fabrication of n-channel SiC MOSFETs. In fact, nitridation leads to a reduction of interface state density, and a possible explanation for this may be that N atoms passivate the interface states. Other techniques to introduce the N atoms into SiO_2/SiC interface have also been proposed [59, 60], and the n-channel MOSFET performance was improved [61].

It has been thought that the fact that SiO_2 can be thermally grown on SiC is one of advantages compared to other compound semiconductors. However, the interfacial transition layer which contains carbon atoms or carbon clusters in SiO_2 is detected between pure SiO_2 grown by thermal oxidation and SiC [58, 62]. Although the origin of the interface states has not been fully understood, it is known that the thickness of interfacial transition layer is correlated with the channel mobility. (The thick interfacial transition layer at the SiO_2/SiC interface may reduce the channel mobility [58].) On the other hand, the transition layer at the interface will hardly be formed when the gate insulators are deposited. Therefore, the deposited insulators/SiC interface may be abrupt and can be expected to show better characteristics than the thermal oxides/SiC interface. A few groups have started to investigate SiC MOS structure with deposited insulators [63–65]. 4H-SiC (0001) n-channel MOSFETs with deposited SiO_2 followed by N_2O annealing [66] and low-temperature deposited Al_2O_3 [67] have already demonstrated a higher channel mobility (over $30\,cm^2/Vs$) than the MOSFETs with thermal oxides. In addition, the deposited insulators exhibited superior reliability to thermal oxides [34, 35]. The deposited insulators are promising for SiC MIS devices.

P-Channel MISFETs

4H-SiC p-channel MISFETs are the key component of low-voltage ICs. In addition, the increase of p-channel mobility contributes to the enhancement of p-IGBT performance. As mentioned above, the investigation on 4H-SiC n-channel MIS devices has shown gradual progress. On the other hand, fundamental studies on 4H-SiC p-channel MIS devices are missing.

A large negative shift of flatband voltage at the dry O_2-oxidized SiO_2/SiC interface is

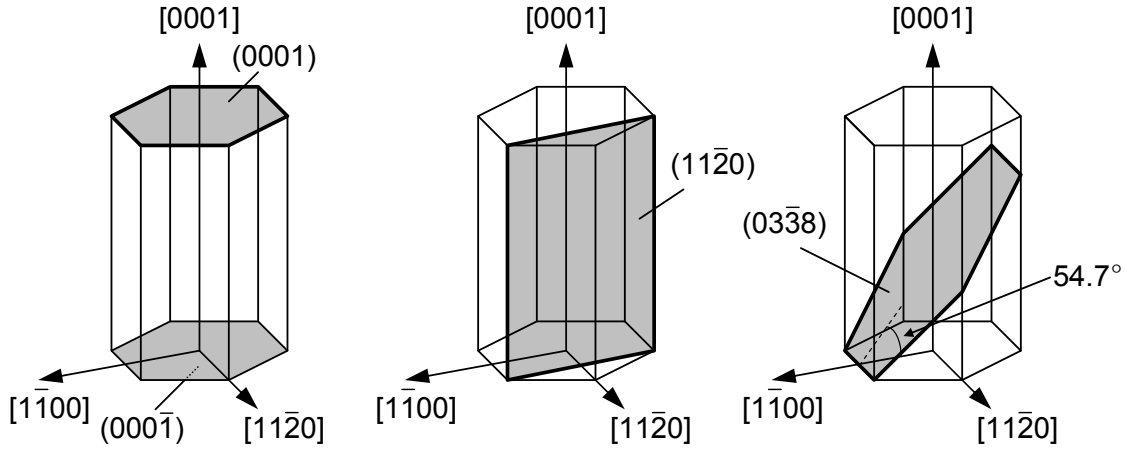


Figure 1.9: 4H-SiC (0001), (000$\bar{1}$), (11$\bar{2}$0), and (03$\bar{3}$8) faces.

typically observed in the capacitance-voltage (C–V) characteristics of p-MOS capacitors [68–71]. Wet oxidation is effective for the reduction of the large negative flatband voltage shift and the interface state density in p-type SiC [72]. A limited number of reports on SiC p-channel MOSFETs have been published [73–75]. The typical channel mobility is about 5–10 cm^2/Vs in 4H-SiC (0001) p-channel MOSFETs with dry O_2-grown oxides and is increased to about 15 cm^2/Vs by wet oxidation. The reported p-channel MOSFETs exhibit a moderate channel mobility in spite of a small bulk hole mobility.

For SiC CMOS circuits, it is very important to realize high channel mobility in n- and p-channel MISFETs using the same process. Taking that into consideration, the validation of nitridation process and deposited insulators for p-channel MIS devices is needed. In addition, the crystal face dependence of the interface state density and the channel mobility in p-type MIS devices have been still missing. Thus, for further development of SiC-based devices and circuits, both basic and practical research is required.

In general, the interface state density near the conduction and valence band edges affects the n- and p-channel MISFETs, respectively. MIS capacitors fabricated on n-type SiC have been used to estimate the interface state density near the conduction band edge, which is related to n-channel mobility of MISFETs fabricated on p-type SiC. In the case of wide bandgap semiconductor, it is difficult to evaluate the interface state density near the minority-carrier band edge because the time constant to generate the minority carriers is too long due to its wide bandgap. The interface state density near the conduction band edge should be estimated by using MIS devices fabricated on p-SiC to minimize the influence of the difference in the conduction type. Therefore, the calculation method to evaluate the interface state density near the minority-carrier band edge should be established.

1.3.3 High-Voltage Lateral Devices

As it was already mentioned, a number of SiC vertical power devices have been reported. On the other hand, only a limited number of promising studies on SiC lateral power devices have been published. To realize high-voltage power ICs, an intensive study on lateral power devices should be addressed.

The first SiC lateral power MOSFET reported in 1998 had a lateral DMOS (LDMOS) structure with a breakdown voltage of 2.6 kV [76]. Since the report of the first LDMOSFET, there have been two major streams in the development of lateral SiC power devices. One is aiming at MOSFETs, and the other one at JFETs. SiC lateral power JFETs have shown better characteristics than SiC lateral power MOSFETs [77–79]. However, JFETs show normally-ON characteristics. In addition, in the case of both normally-OFF and ON JFETs, the gate voltage needs to be lower than built-in potential in SiC (about 3 eV) to keep gate leakage current low, which leads to the fact that more complicated design of gate-drive circuits is required. This is a disadvantage of SiC JFET-based power ICs. On the other

hand, SiC MOSFETs are basically normally-OFF and can be controlled by simple gate-drive circuits. Therefore, SiC lateral power MOSFETs are more favorable for high-voltage power ICs.

The studies on SiC lateral power MOSFETs have focused mainly on a reduced surface field (RESURF) structure [80]. The reported SiC RESURF MOSFETs with high breakdown voltage (about 1 kV) have exhibited a large ON-resistance (over 100 $m\Omega cm^2$) due to large channel resistance [81–86]. However, some successful development of SiC MOS technologies as described in Section 1.3.2 has been reported and the ratio of channel resistance to total specific ON-resistance was decreased. As a result, a dominant component of the specific ON-resistance is the drift resistance [87], and the decrease of the drift resistance becomes more important recently. For further improvement, the new device structure and concepts need to be introduced to decrease the drift resistance.

1.4 Aim of This Study and Outline of Thesis

In this study, the physics of both SiC MIS devices and lateral high-voltage MISFETs is investigated toward the realization of high-voltage power ICs. Systematic study on short-channel effects in SiC MOSFETs was performed and both n- and p-channel MIS devices with deposited insulators were fabricated and characterized in order to improve channel mobility. In addition, lateral high-voltage MISFETs were also explored from scientific and technological aspects.

In Chapter 2, the study of short-channel effects in SiC MISFETs is reported. SiC MOSFETs with submicron channel are fabricated and characterized. The short-channel effects observed in SiC MOSFETs are described and compared to a simulation study. In addition, the critical channel length, for which long-channel behavior can be observed, is also estimated from the experimental and simulation results. The influence of effective fixed charges at MIS interface on the short-channel effects is also discussed.

In Chapter 3, the results of characterization of the interface and dielectric properties of MIS structures with thermally-grown and deposited insulators are presented. N_2O-grown oxides, deposited SiO_2 annealed in N_2O, and deposited SiN_x/SiO_2 annealed in N_2O are applied to gate insulators for SiC MIS capacitors. To achieve low interface state density, deposition and annealing conditions are varied and the influence of these conditions is discussed. The reliability of these insulators are also investigated.

In Chapter 4, the results of the investigation of SiC MISFETs with thermally-grown and deposited insulators are shown. SiC MISFETs with various insulators are fabricated and characterized to increase the channel mobility. The influence of effective fixed charges on the n- and p-channel mobility is discussed. In addition, an original method to estimate the interface state density near the minority-carrier band edge is proposed.

In Chapter 5, SiC lateral high-voltage MISFETs are designed. To decrease the drift

resistance, double and triple RESURF structures are proposed. From both experimental and simulation studies, the MISFET structure is optimized to achieve high breakdown voltage and low ON-resistance. The advantages of the proposed structure are also explained.

In Chapter 6, SiC lateral high-voltage MISFETs are fabricated and characterized. The fabricated MISFETs with an optimum structure exhibited both high breakdown voltage and low ON-resistance. The ON- and OFF-state characteristics are investigated. Temperature dependence is also described. The advantages of the fabricated MISFETs are shown and compared to other reported lateral MISFETs.

In Chapter 7, conclusions of this study and suggestions for future work are presented.

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Chapter 2

Short-Channel Effects in SiC MISFETs

2.1 Introduction

4H-SiC metal-insulator-semiconductor field-effect transistors (MISFETs) have a great potential not only for high-voltage power electronic applications but also for high-temperature integrated circuits (ICs) beyond the Si limit. The most important part of 4H-SiC MISFETs is the channel region, which seriously influences MISFET performance.

To reduce the channel resistance of power MISFETs, there are two effective approaches. The first one consists in increasing the channel mobility (μ_{Ch}), and the other one in decreasing the channel length (L_{Ch}) because the channel resistance is proportional to $L_{\mathrm{Ch}}/\mu_{\mathrm{Ch}}$. In the former case, nitridation process [1–3] and utilization of 4H-SiC $(000\bar{1})$ and $(11\bar{2}0)$ faces [4, 5] are effective to enhance the channel mobility. Deposited insulators are also another method to increase the channel mobility, as it will be discussed in Chapters 3 and 4. In the latter case, a low specific ON-resistance below $10\,\mathrm{m\Omega cm^2}$ has been realized in vertical SiC power MISFETs by reducing the channel length to $0.5\,\mu$m by a self-aligned implantation process [6, 7]. SiC lateral MISFETs with a submicron channel are also very attractive as high-frequency power transistors, which can favorably compete with Si LDMISFET [8]. In terms of low-voltage ICs, the reduction of channel length is effective to gain high-switching speed, and the scaling down of MISFETs increases device density and reduces power dissipation. Thus, the increase of channel mobility is of great importance to realize high-performance SiC MISFETs and the reduction of channel length also contributes greatly to the improvement of SiC MIS-based devices.

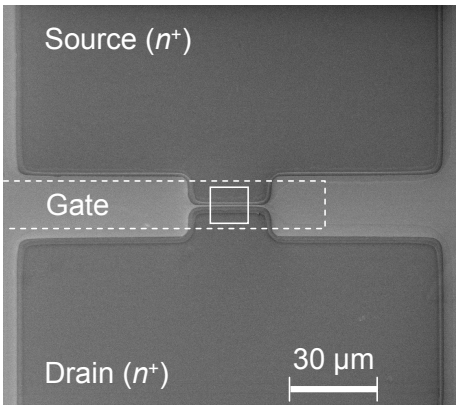
In Si MISFETs, the reduction of channel length may cause short-channel effects [9], which adversely affect the MISFET performance and should be either eliminated or minimized. Although short-channel effects are expected to take place in SiC MISFETs as well, very few investigations on this issue have been reported [10], while a great number of studies on the fundamental characteristics of SiC MISFETs can be found in the literature [11].

In this chapter, 4H-SiC metal-oxide-semiconductor FETs (MOSFETs) with submicron channels have been fabricated and the short-channel effects in SiC MOSFETs have been investigated. The experimentally observed short-channel effects are compared with those simulated by using a two-dimensional device simulator. The experimental and simulated critical channel lengths, below which the short-channel effects occur, are demonstrated for the first time. The influence of effective fixed charges located at the MOS interface on the short-channel effects is also discussed.

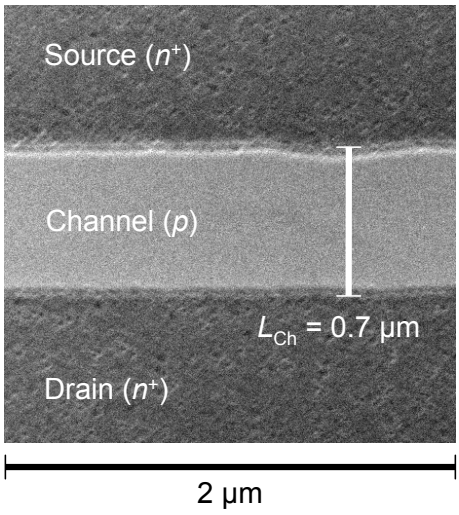
2.2 Device Fabrication

Short-channel planar MOSFETs were fabricated on p-type 8 ° off-axis 4H-SiC (0001), 8 ° off-axis $(000\bar{1})$, and on-axis $(11\bar{2}0)$ epilayers. The thickness of epilayers was 5 μm or 10 μm. The acceptor concentration of p-body (N_{A}) determined from the capacitance-voltage (C–V) measurements was about $1 \times 10^{16}\,\mathrm{cm}^{-3}$ or $1 \times 10^{17}\,\mathrm{cm}^{-3}$. The lightly- and highly-doped MOSFETs were fabricated on the epilayer with an acceptor concentration of about $1 \times 10^{16}\,\mathrm{cm}^{-3}$ and $1 \times 10^{17}\,\mathrm{cm}^{-3}$, respectively. About 1.5 μm-thick SiO_2 deposited by plasma-enhanced chemical vapor deposition (PECVD) was employed as an implantation mask. The SiO_2 mask was patterned by reactive ion etching (RIE) with a CF_4–H_2 chemistry. Multiple P^+ implantations to form the 0.2 μm-deep source/drain regions were carried out at 300 °C with a total implant dose of $5.0 \times 10^{15}\,\mathrm{cm}^{-2}$. After ion implantation, high-temperature annealing was performed at 1600 °C for 10 min with a carbon cap to suppress surface roughening [12]. After the RCA cleaning, thermal oxidation was carried out in dry N_2O (10 % diluted in N_2) ambience at 1300 °C, followed by post-oxidation annealing (POA) in an N_2 ambience at 1300 °C for 30 min [3, 13]. The thickness of gate oxide (d_{OX}) was 55–82 nm. Source/drain and substrate electrodes were Al and Ti/Al, respectively, and both electrodes were annealed at 600 °C for 10 min. Gate metal was Al. The typical channel length (L_{Ch}) and width (W) are 0.2–15 μm and 30–150 μm, respectively.

Figure 2.1 shows typical scanning electron microscopy (SEM) images (plan view) of (a) the overall view of MOSFET and (b) the channel region after post-implantation annealing. In Fig. 2.1, the dark and bright areas correspond to n^+- and p-regions, respectively. The dashed line in Fig. 2.1 (a) means the region where gate electrode is formed after thermal oxidation. Figure 2.1 (b) exhibits the magnified view of channel region in Fig. 2.1 (a), the area enclosed with a white line. A submicron channel (p-region) can be successfully formed. In this chapter, the channel length for each MOSFET was not defined from a mask pattern but directly measured by SEM as shown in Fig. 2.1 (b).



(a)



(b)

Figure 2.1: SEM images of (a) overall view of a fabricated 4H-SiC MOSFET and (b) submicron channel region after post-implantation annealing. The dark area is the n^+-region and the bright area the p-region.

2.3 Basic MOSFET Characteristics

The average effective channel mobility ($\mu_{\rm eff}$) obtained from the fabricated MOSFETs is listed in Table 2.1. The $(11\bar{2}0)$ and $(000\bar{1})$ MOSFETs exhibited higher channel mobility than the (0001) MOSFETs. The MOSFETs on lightly-doped $(11\bar{2}0)$ epilayer showed a high effective channel mobility of $71\,{\rm cm}^2/{\rm Vs}$. Although the increase of acceptor concentration led to the decrease of channel mobility for each face, the $(11\bar{2}0)$ MOSFETs exhibited an effective mobility of $53\,{\rm cm}^2/{\rm Vs}$ even for the p-body doping of $10^{17}\,{\rm cm}^{-3}$. The relatively high channel mobility for $(11\bar{2}0)$ and $(000\bar{1})$ MOSFETs can be attributed to the lower interface state density near the conduction band edge. The detailed analyses on the MOS interface are described in Chapter 3 and elsewhere [13].

2.4 Short-Channel Effects in 4H-SiC MOSFETs

2.4.1 Experimental Observation

Figure 2.2 shows the drain current ($I_{\rm D}$)-drain voltage ($V_{\rm D}$) characteristics of MOSFET with a channel length of $5.0\,\mu$m fabricated on the 4H-SiC (0001) epilayer. Figures 2.3 and 2.4 exhibit the drain characteristics of the 4H-SiC (0001) MOSFETs with a channel length of $1.6\,\mu$m and $0.2\,\mu$m, respectively. These MOSFETs were fabricated on lightly-doped epilayers ($N_{\rm A} = 9 \times 10^{15}\,{\rm cm}^{-3}$). The gate voltage is varied from 0 V to 20 V with 4 V step. The long-channel ($L_{\rm Ch} = 5.0\,\mu$m) MOSFET exhibits saturation characteristics (Fig. 2.2), while non-saturation characteristics due to drain-induced barrier lowering (DIBL) are observed in Fig. 2.3 ($L_{\rm Ch} = 1.6\,\mu$m) [14]. The shortest-channel MOSFET with a channel length of $0.2\,\mu$m exhibits ohmic-like drain current at zero gate bias, indicating a punchthrough behavior due to short-channel effects (Fig. 2.4). The punchthrough behavior was observed only in lightly-doped MOSFETs with submicron channel lengths but not in highly-doped MOSFETs. Similar results were obtained for 4H-SiC $(000\bar{1})$ and $(11\bar{2}0)$ MOSFETs.

Figure 2.5 shows the relationship between channel length and drain current of MOSFETs on lightly-doped epilayers. Drain current at a fixed bias voltage is inversely proportional to channel length for long-channel MOSFETs. As the channel length is reduced, however, the relationship between the drain current and the inverse of channel length deviates from the proportionality. The increase of the drain current was caused by DIBL or punchthrough behavior as shown in Figs. 2.3 and 2.4.

In this study, the threshold voltage ($V_{\rm T}$) was defined from the drain current ($I_{\rm D}$)-gate voltage ($V_{\rm G}$) plot in the linear region and the square root of drain current ($\sqrt{I_{\rm D}}$)-gate voltage plot in the saturation region as shown in Fig. 2.6 (a) and (b), respectively. Figure 2.6 shows the gate characteristics of lightly-doped MOSFETs fabricated on the (0001) face, where the drain current is normalized by channel length ($L_{\rm Ch}$) and width (W). In the linear region (Fig. 2.6 (a)), the threshold voltage is slightly decreased by reducing the channel length. The

Table 2.1: Average effective mobility of fabricated 4H-SiC MOSFETs.

p-body doping	(0001)	$(000\bar{1})$	$(11\bar{2}0)$
$\sim 10^{16}\,\mathrm{cm}^{-3}$	$21\,\mathrm{cm}^2/\mathrm{Vs}$	$28\,\mathrm{cm}^2/\mathrm{Vs}$	$71\,\mathrm{cm}^2/\mathrm{Vs}$
$\sim 10^{17}\,\mathrm{cm}^{-3}$	$11\,\mathrm{cm}^2/\mathrm{Vs}$	$19\,\mathrm{cm}^2/\mathrm{Vs}$	$53\,\mathrm{cm}^2/\mathrm{Vs}$

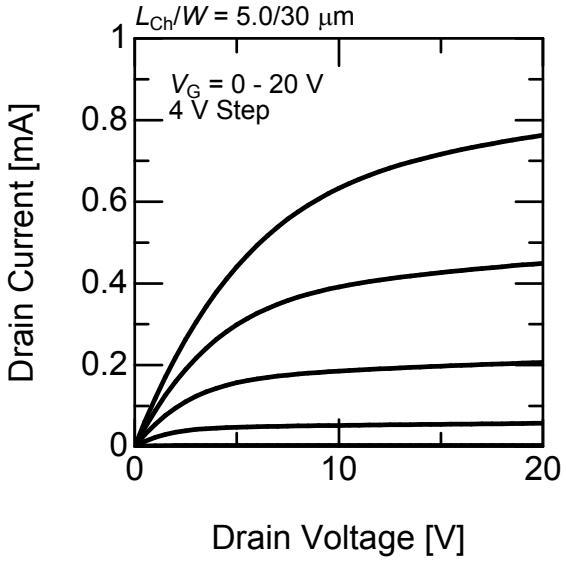


Figure 2.2: Drain characteristics of 4H-SiC (0001) MOSFET with a channel length of $5.0\,\mu$m. The acceptor concentration of p-body is $9 \times 10^{15}\,\mathrm{cm}^{-3}$. Good linear and saturation characteristics are observed.

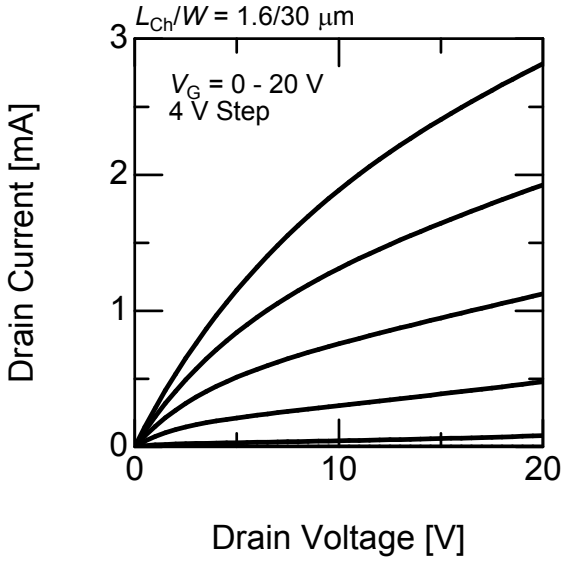


Figure 2.3: Drain characteristics of 4H-SiC (0001) MOSFET with a channel length of $1.6\,\mu$m. The acceptor concentration of p-body is $9 \times 10^{15}\,\mathrm{cm}^{-3}$. Non-saturation characteristics are observed.

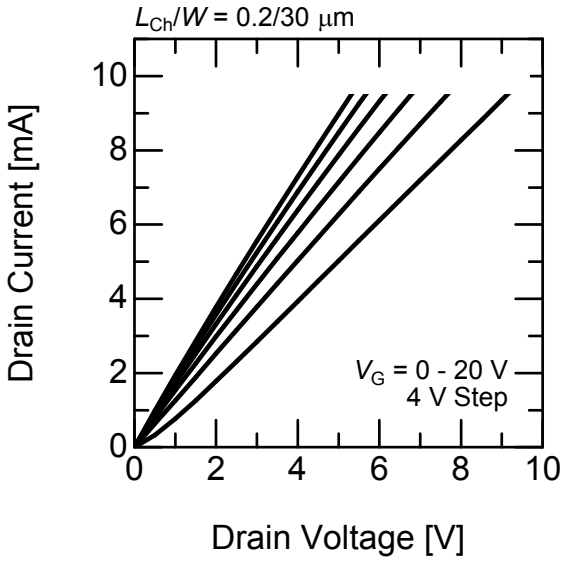


Figure 2.4: Drain characteristics of 4H-SiC (0001) MOSFET with a channel length of $0.2\,\mu$m. The acceptor concentration of p-body is $9 \times 10^{15}\,\mathrm{cm}^{-3}$. Punchthrough behavior is observed.

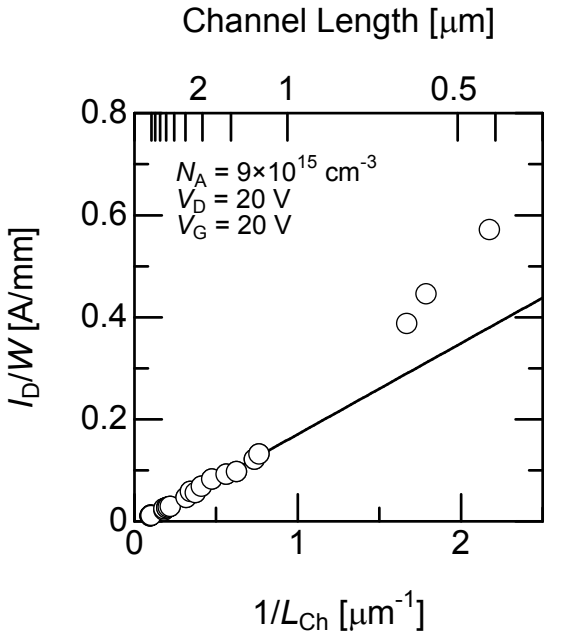
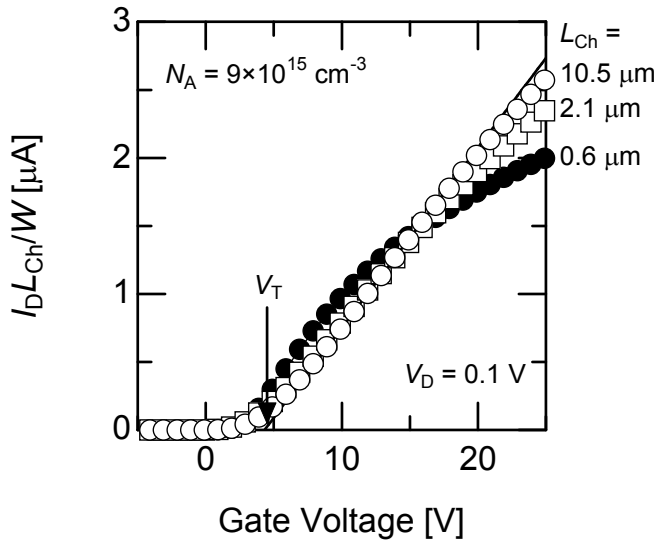
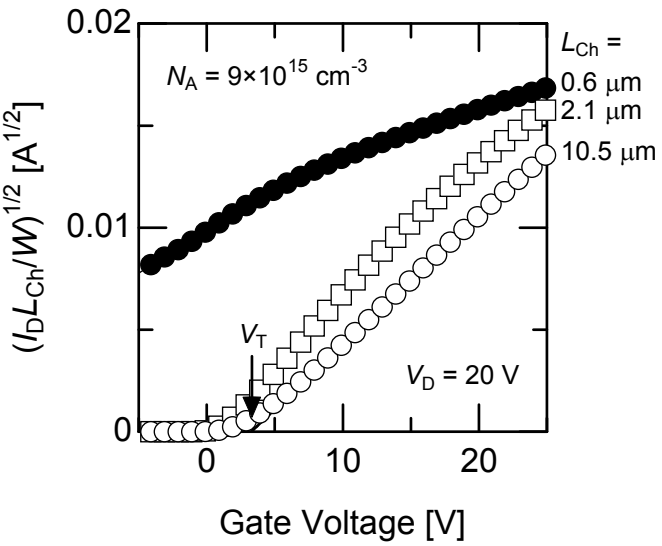


Figure 2.5: Relationship between the drain current (I_{D}) and the inverse of channel length ($1/L_{\mathrm{Ch}}$) in the 4H-SiC (0001) MOSFETs. The drain current is normalized by the channel width. The reduction of the channel length causes the increase of the drain current. The drain current in short-channel MOSFETs is higher than expected values (indicated by solid line).



(a)



(b)

Figure 2.6: Gate voltage dependence of (a) drain current (I_D) and (b) square root of drain current ($\sqrt{I_D}$) in lightly-doped 4H-SiC (0001) MOSFETs. Drain current is normalized by the channel length and width. Threshold voltage in the linear region and saturation region is defined from the plots (a) and (b), respectively.

drain current of 0.6 μm-channel MOSFET is saturated because of series resistance effect. The threshold voltage in the saturation region is shifted toward the negative gate-voltage direction by reducing channel length, and the 0.6 μm-channel MOSFET cannot shut off the drain current due to punchthrough.

The drain voltage dependence of threshold voltage in the (0001) MOSFET with a p-body acceptor concentration of $9 \times 10^{15}\,\mathrm{cm}^{-3}$ is shown in Fig. 2.7. The threshold voltage of the lightly-doped MOSFETs decreased when the drain voltage was increased, and the decrease in threshold voltage is pronounced for MOSFETs with short channel length, which is mainly caused by DIBL [14]. The slope of the relationship between the drain voltage and the threshold voltage is 83 mV/V for the MOSFET with a channel length of 1.4 μm and 29 mV/V for the MOSFET with a channel length of 2.1 μm. The steep slope was observed in the short-channel MOSFETs on lightly-doped epilayers. On the other hand, the highly-doped MOSFETs hardly exhibited such behavior (not shown). The threshold voltage in the highly-doped MOSFETs does not depend on the drain voltage and channel length, which means DIBL was suppressed in the highly-doped MOSFETs.

The channel length dependence of threshold voltage at drain voltages of (a) 0.1 V and (b) 20 V for 4H-SiC (0001) MOSFETs is shown in Fig. 2.8. At a low drain voltage of 0.1 V (Fig. 2.8 (a)), the lightly-doped MOSFETs exhibit gradual decrease in threshold voltage with shortening the channel length, and the threshold voltage decreases below 0 V in the shortest-channel MOSFET. For highly-doped MOSFETs, the decrease of threshold voltage was not observed. At a high drain voltage of 20 V (Fig. 2.8 (b)), the decrease of threshold voltage occurs not only in lightly-doped MOSFETs but to a smaller extent, also in highly-doped MOSFETs. Thus, the decrease of threshold voltage becomes more pronounced in the lightly-doped devices when drain voltage increases, in good agreement with the characteristics of Si MOSFETs [9, 14].

Figure 2.9 shows the subthreshold characteristics (log I_D - V_G characteristics) of (a) lightly-doped and (b) highly-doped (0001) MOSFETs. In Fig. 2.9, the drain current is normalized by the channel length and width. In this measurement, the drain voltage was fixed at 20 V, where short-channel effects are more pronounced. For lightly-doped MOSFETs, the subthreshold characteristics are deteriorated with the reduction of channel length (Fig. 2.9 (a)). However, for highly-doped MOSFETs, the subthreshold characteristics are not deteriorated even for a channel length of 1.2 μm (Fig. 2.9 (b)). In the lightly-doped MOSFETs, when the channel length is reduced from 10.4 μm to 1.3 μm, the subthreshold characteristics slightly shifted toward the negative gate voltage direction, which is consistent with a slight decrease of threshold voltage, as shown in Fig. 2.8, while the change of subthreshold swing is not significant. In the 0.6 μm-channel MOSFET, significant amount of drain current flowed even at the negative gate bias, due to punchthrough behavior.

Figure 2.10 shows the relationship between the transconductance (g_m) and the channel length in 4H-SiC (0001) MOSFETs, where the transconductance was determined at a drain

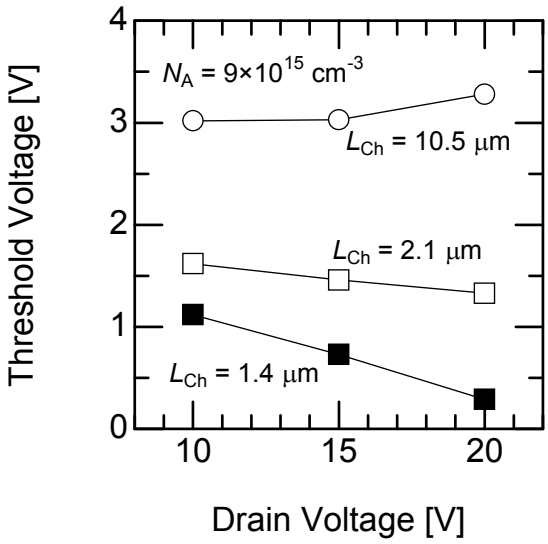
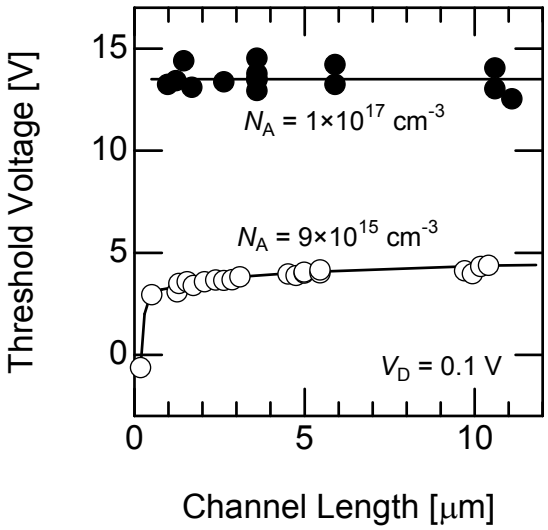
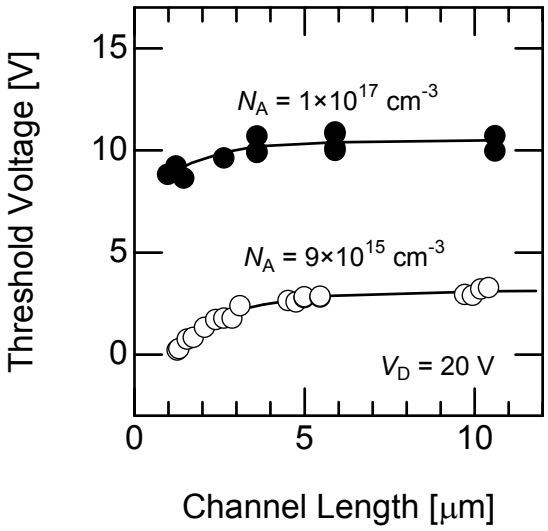


Figure 2.7: Drain voltage dependence of threshold voltage in the lightly-doped MOSFETs fabricated on the 4H-SiC (0001) face. The threshold voltage in the lightly-doped MOSFETs is decreased with increasing drain voltage and/or reducing channel length.

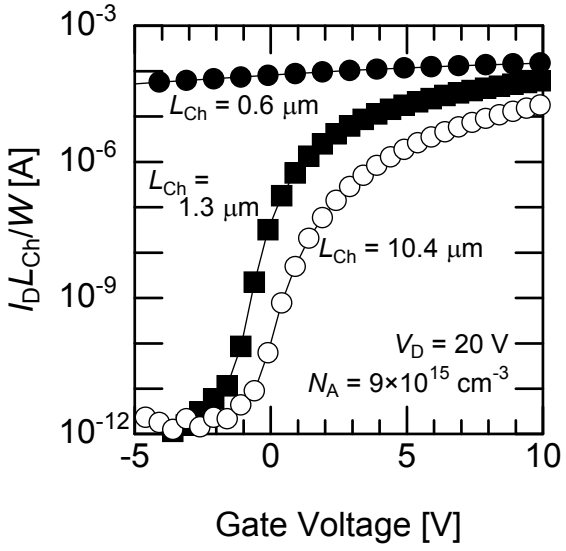


(a)

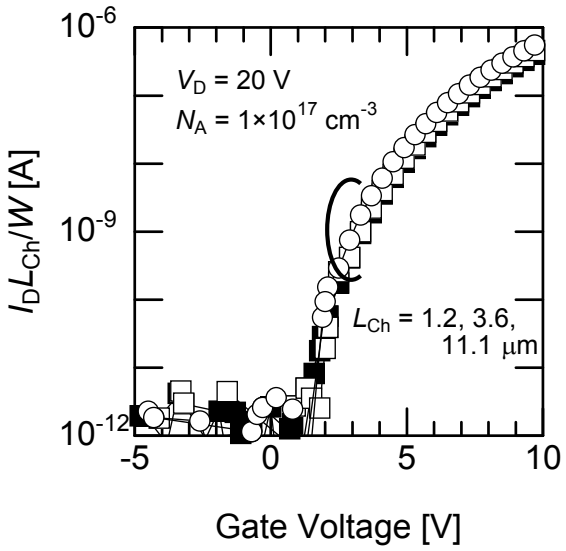


(b)

Figure 2.8: Relationship between the threshold voltage and the channel length in (a) the linear region ($V_D = 0.1\,V$) and (b) the saturation region ($V_D = 20\,V$). Closed and open circles represent characteristics of highly-doped and lightly-doped MOSFETs on 4H-SiC (0001) face, respectively.



(a)



(b)

Figure 2.9: Subthreshold characteristics of 4H-SiC (0001) MOSFETs fabricated on (a) lightly-doped and (b) highly-doped epilayers. The drain current is normalized by the channel length and width. The lightly-doped MOSFET with a submicrometer channel length cannot be turned off.

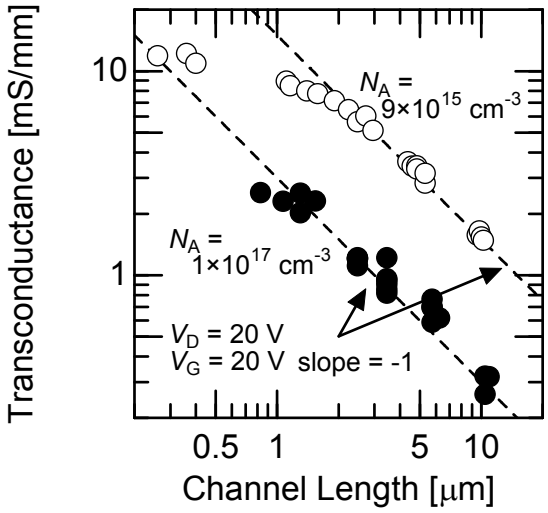


Figure 2.10: Relationship between the transconductance and the channel length in 4H-SiC (0001) MOSFETs. For the lightly-doped MOSFETs, the saturation of transconductance is observed.

voltage of 20 V and a gate voltage of 20 V. The transconductance is defined as:

$$g_{\mathrm{m}} = \frac{\mu_{\mathrm{Ch}} W C_{\mathrm{OX}}}{L_{\mathrm{Ch}} d_{\mathrm{OX}}} (V_{\mathrm{G}} - V_{\mathrm{T}}), \tag{2.1}$$

where μ_{Ch} is the channel mobility and C_{OX} the oxide capacitance per unit area. The transconductance is inversely proportional to the channel length for long-channel MOSFETs within the investigated range of channel length as mentioned in Eq. 2.1. On the other hand, for short-channel ($L_{\mathrm{Ch}} \leq 2\,\mu$m) MOSFETs fabricated on lightly-doped epilayers, however, the transconductance is smaller than that extrapolated from the characteristics of long-channel MOSFETs.

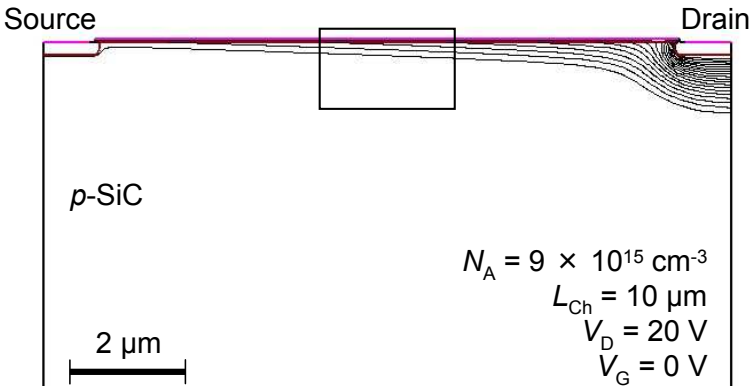
2.4.2 Simulation Study

The phenomena which occurred in short-channel SiC MOSFET were simulated by using a two-dimensional device simulator (Synopsys-Technology Computer-Aided Design (TCAD)[1]). In the device simulation, the acceptor concentration of p-body, the oxide thickness, and the channel length were varied and the junction depth was about 0.2 μm. An ideal MOS interface was assumed in the simulation. Short-channel effects such as the decrease of threshold voltage and the deterioration of subthreshold characteristics were also observed in the simulated MOSFETs.

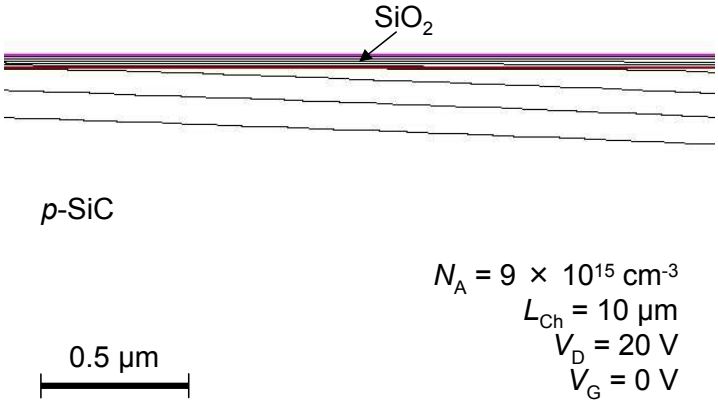
Typical electric potential distributions simulated for SiC MOSFETs are shown in Fig. 2.11. The simulated MOSFETs have an acceptor concentration of $9 \times 10^{15}\,\mathrm{cm}^{-3}$ and a gate oxide thickness of 55 nm. The channel length varied from 0.5 μm to 10 μm. This structure is similar to that of fabricated MOSFETs. Figure 2.11 displays the equipotential lines for (a) a long-channel ($L_{\mathrm{Ch}} = 10\,\mu$m) MOSFET and (c) a short-channel ($L_{\mathrm{Ch}} = 0.5\,\mu$m) MOSFET. Figure 2.11 (b) exhibits the magnification of channel region marked by the rectangle in Fig. 2.11 (a). Although the equipotential lines inside the channel region in the long-channel MOSFET have a one-dimensional distribution as shown in Fig. 2.11 (b), the electric potential distribution becomes two dimensional in the short-channel MOSFETs (Fig. 2.11 (c)). The reduction of channel length makes the influence of depletion layer from the drain region significant, and the potential inside the channel region is decreased, which causes short-channel effects.

Figure 2.12 shows the channel length dependence of threshold voltage obtained by device simulation. In the simulation, the threshold voltage was determined in the same manner as experiments. In Fig. 2.12, the open circles indicate the results for MOSFETs with an acceptor concentration of $2 \times 10^{15}\,\mathrm{cm}^{-3}$ and a gate oxide thickness of 120 nm, the open boxes the MOSFETs with an acceptor concentration of $2 \times 10^{15}\,\mathrm{cm}^{-3}$ and a gate oxide thickness of 60 nm, and the closed boxes the MOSFETs with an acceptor concentration of $2 \times 10^{16}\,\mathrm{cm}^{-3}$ and a gate oxide thickness of 60 nm. In the simulation, a steep decrease of

[1]Two-dimensional device simulator will be introduced in Chapter 5.



(a)



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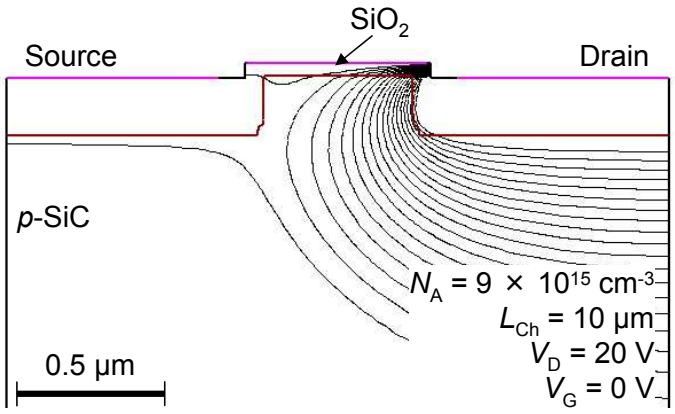


(c)

Figure 2.11: Equipotential lines inside the channel region in simulated 4H-SiC MOSFETs with a channel length of (a) 10 μm and (c) 0.5 μm. The magnified view of the channel region indicated by the rectangle in (a) is shown in (b). The acceptor concentration of p-body is $9 \times 10^{15}\,\mathrm{cm}^{-3}$. The step of each line is 1 V. In the MOSFET with a channel length of 0.5 μm, the electric potential shows two-dimensional distribution.

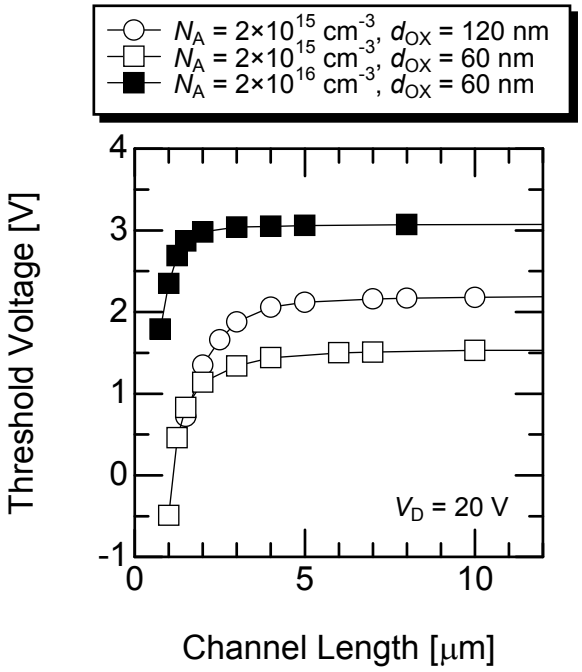


Figure 2.12: Relationship between the threshold voltage and the channel length in simulated MOSFETs. Decrease of threshold voltage is more pronounced when the p-body doping is lower and/or the oxide thickness is thicker.

threshold voltage takes place at a shorter channel length, when the MOSFETs have higher p-body doping and/or thinner oxide thickness, in agreement with experimental results.

In Fig. 2.13, the relationship between threshold voltage and channel length in the simulated MOSFETs is compared with that in the fabricated MOSFETs. The acceptor concentration and gate oxide thickness for simulated MOSFETs are $2 \times 10^{17}\,\mathrm{cm}^{-3}$ and 70 nm (Fig. 2.13 (a)) and $9 \times 10^{15}\,\mathrm{cm}^{-3}$ and 55 nm (Fig. 2.13 (b)), respectively. This structure is similar to that of fabricated MOSFETs in both cases. The open and closed circles denote the simulated and experimental results, respectively. In the long channel region, the experimental threshold voltages (about 10.5 V in (a) and 3.0 V in (b)) are higher than the simulated values (about 6.0 V in (a) and 1.5 V in (b)) because of negative effective fixed charges at the SiO_2/SiC interface. In n-channel 4H-SiC MOSFETs, negative effective fixed charges exist at the MOS interface because electrons, induced by gate voltage, are trapped by a high density of interface states [13, 15]. The influence of the effective fixed charges on the short-channel effects is discussed in Section 2.6. In the short channel region, the threshold voltage of the fabricated MOSFETs decreased gradually at a longer channel length than that of the simulated devices.

Figure 2.14 shows the subthreshold characteristics in the simulated devices with (a) highly-doped and (b) lightly-doped p-body. In Fig. 2.14, the drain current is normalized by the channel length and width. In the simulation of highly-doped MOSFETs, the subthreshold characteristics did not deteriorate when the channel length is reduced to 1 μm (Fig. 2.14 (a)), in agreement with experimental results (Fig. 2.9 (a)). The subthreshold swing (S) of the MOSFET with high p-body doping and channel length of 10 μm is 123 mV/decade. When the channel length is reduced to 1 μm, the subthreshold swing is almost the same (125 mV/decade). For the lightly-doped MOSFETs (Fig. 2.14 (b)), the negative shift of subthreshold characteristics due to the decrease of threshold voltage is observed, and the subthreshold swing is increased from 75 mV/decade to 91 mV/decade when channel length is reduced from 10.0 μm to 1.0 μm. It should be noted, however, that the subthreshold swings (slopes) for simulated MOSFETs are much lower than experimental values, due to a high density of interface states in real MOSFETs.

2.4.3 Estimation of Critical Channel Length

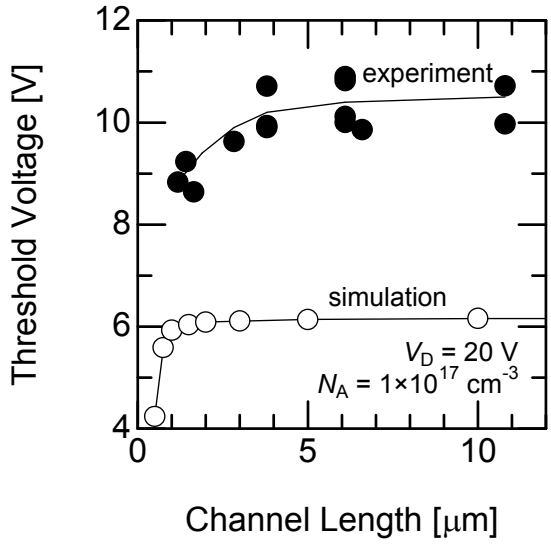
In Si MOSFETs, the boundary between long-channel and short-channel MOSFETs is described as [16]:

$$L_{\mathrm{Crit}} = 0.41\gamma^{1/3}. \tag{2.2}$$

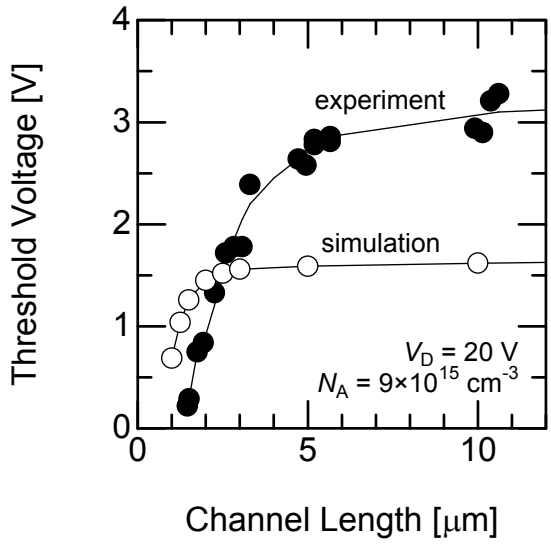
Here, the L_{Crit} means the critical channel length below which short-channel effects occur, and γ is given by:

$$\gamma = r_{\mathrm{j}} d_{\mathrm{OX}} (W_{\mathrm{S}} + W_{\mathrm{D}})^2, \tag{2.3}$$

where r_{j} is the junction depth in μm, d_{OX} the oxide thickness in Å, and W_{S} and W_{D} the source and drain depletion width in μm, respectively. In ref. [16], Si short-channel MOSFETs

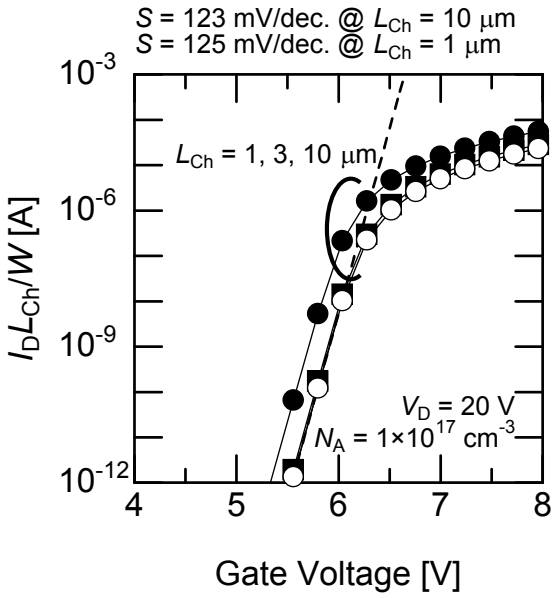


(a)

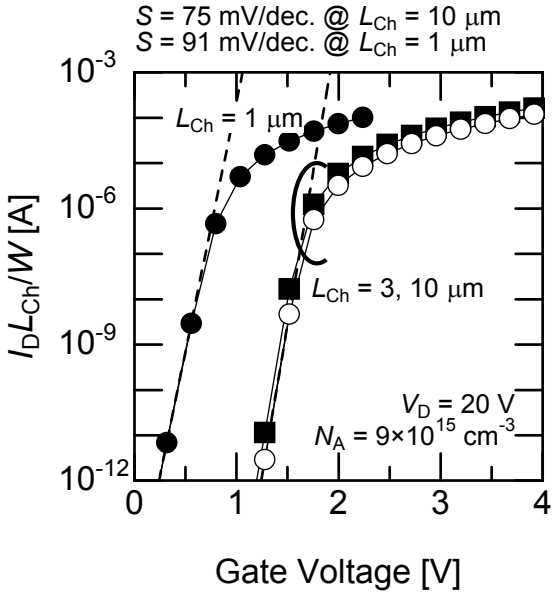


(b)

Figure 2.13: Channel length dependence of threshold voltage for simulated and fabricated SiC MOSFETs with (a) high acceptor concentration and (b) low acceptor concentration of p-body. Open and closed circles denote the threshold voltage for simulated and fabricated MOSFETs, respectively. Decrease of threshold voltage takes place at a shorter channel length in simulated MOSFETs than in fabricated MOSFETs.



(a)



(b)

Figure 2.14: Subthreshold characteristics of 4H-SiC MOSFETs obtained by device simulation. The drain current is normalized by the channel length and width. The simulated devices have (a) an acceptor concentration of $1 \times 10^{17}\,\mathrm{cm}^{-2}$ and an oxide thickness of 70 nm and (b) an acceptor concentration of $9 \times 10^{15}\,\mathrm{cm}^{-2}$ and an oxide thickness of 55 nm. Deterioration of subthreshold characteristics occurs only in lightly-doped MOSFETs.

are defined based upon two criteria. The first criterion is based on the channel length dependence of drain current. The MOSFET which exhibits a 10 % (or more) deviation (increase) in drain current from the linear dependence upon the inverse of channel length is regarded as a short-channel device. The second criterion is related to the dependence of the subthreshold current on drain voltage [17, 18]. Long-channel devices do not exhibit the drain voltage dependence of the drain current in the subthreshold region when the drain voltage is larger than $3kT/q$. The MOSFET, the drain current of which increases with increasing drain voltage in the subthreshold region, is defined as a short-channel device.

Characteristics of SiC MOSFETs with various structures including channel length were simulated, and the critical channel length was estimated. In the simulation, the "short-channel SiC MOSFETs" were defined based upon the same criterion as Si MOSFETs, which is the dependence of subthreshold current on drain voltage. From this analysis, the boundary can be described as:

$$L_{\mathrm{Crit}} = 0.44\gamma^{1/3}. \tag{2.4}$$

The simulation of SiC MOSFETs is shown in Fig. 2.15 and in very good agreement with the empirical relationship for Si MOSFETs (Eq. 2.2). Considering SiC and Si MOSFETs with the same structure, the potential inside channel region should be mainly influenced by the extension of depletion layer from the drain region, and not by the bandgap itself. The extension of depletion region in SiC and Si MOSFETs is almost the same at given bias, because the smaller dielectric constant of SiC (about 10) is almost cancelled by a larger built-in voltage (about 2.9 eV). Therefore, the critical channel lengths of simulated SiC MOSFETs are almost the same as those of Si MOSFETs.

It was difficult to define the short-channel SiC MOSFETs in the same manner as Si MOSFETs, due to fluctuation of drain current observed for the fabricated SiC MOSFETs with similar structures. Therefore, a new criterion related to the decrease of threshold voltage has been employed in this study.

The drain current of a MOSFET can be described as:

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{Ch}} W C_{\mathrm{OX}}}{L_{\mathrm{Ch}}} (V_{\mathrm{G}} - V_{\mathrm{T}}) V_{\mathrm{D}} \tag{2.5}$$

in the linear region and

$$I_{\mathrm{Dsat}} = \frac{\mu_{\mathrm{Ch}} W C_{\mathrm{OX}}}{L_{\mathrm{Ch}}} \frac{(V_{\mathrm{G}} - V_{\mathrm{T}})^2}{2} \tag{2.6}$$

in the saturation region [9]. When the threshold voltage (V_{T}) is reduced to $V_{\mathrm{T}} - \Delta V_{\mathrm{T}}$, the increase of the drain current in the linear and saturation regions (ΔI_{D} and ΔI_{Dsat}, respectively) can be expressed by:

$$\Delta I_{\mathrm{D}} = \frac{\mu_{\mathrm{Ch}} W C_{\mathrm{OX}}}{L_{\mathrm{Ch}}} V_{\mathrm{D}} \Delta V_{\mathrm{T}}, \tag{2.7}$$

and

$$\Delta I_{\mathrm{Dsat}} \simeq \frac{\mu_{\mathrm{Ch}} W C_{\mathrm{OX}}}{L_{\mathrm{Ch}}} (V_{\mathrm{G}} - V_{\mathrm{T}}) \Delta V_{\mathrm{T}}. \tag{2.8}$$

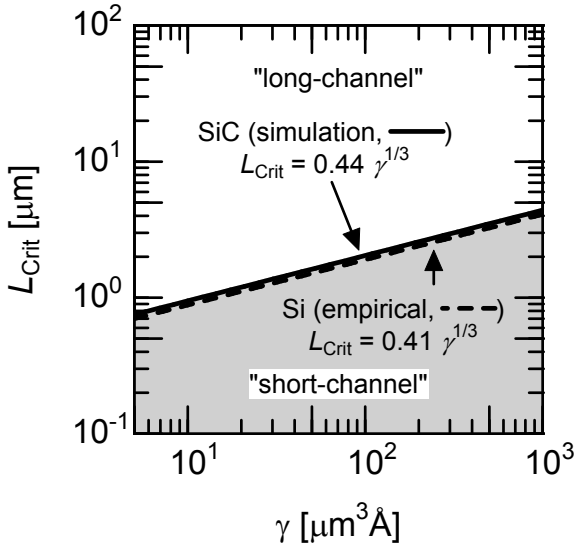


Figure 2.15: Critical channel length versus γ relationship for the simulated SiC MOSFETs. Solid line means the relationship for the simulated SiC MOSFETs ($L_{\mathrm{Crit}} = 0.44\gamma^{1/3}$) and dashed lines the empirical relationship for Si MOSFETs ($L_{\mathrm{Crit}} = 0.41\gamma^{1/3}$). The short-channel SiC MOSFETs are defined based upon the same criterion as Si MOSFETs.

Here, the term $\Delta {V_{\rm T}}^2$ was neglected. Thus, the increase of drain current is proportional to the decrease of threshold voltage. The relative increase normalized by the drain current is given by the following.

$$\frac{\Delta I_{\rm D}}{I_{\rm D}} = \frac{\Delta V_{\rm T}}{V_{\rm G} - V_{\rm T}} \propto \Delta V_{\rm T}, \tag{2.9}$$

in the linear region and

$$\frac{\Delta I_{\rm Dsat}}{I_{\rm Dsat}} = \frac{2\Delta V_{\rm T}}{V_{\rm G} - V_{\rm T}} \propto 2\Delta V_{\rm T}, \tag{2.10}$$

in the saturation region. The $\Delta I_{\rm D}/I_{\rm D}$ and $\Delta I_{\rm Dsat}/I_{\rm Dsat}$ are proportional to $\Delta V_{\rm T}$ and $2\Delta V_{\rm T}$, respectively. Therefore, in this study, short-channel MOSFETs are defined as the devices, the threshold voltage of which is lower than that of sufficiently long-channel MOSFETs by 1.0 V in the linear region and 0.5 V in the saturation region.

Figure 2.16 shows the critical channel length versus γ for various MOSFETs fabricated and simulated in this study. In Fig. 2.16, the open circles with error bars and dotted line mean the critical channel lengths for the fabricated SiC MOSFETs and their least-square fitting, respectively. The solid line represents the simulated critical channel length of SiC MOSFETs determined by the $\Delta V_{\rm T}$ definition described above. The dashed line shows the empirical relationship for Si MOSFETs, which is described as "$L_{\rm Crit} = 0.41\gamma^{1/3}$". In the fabricated MOSFETs, the relationship between $L_{\rm Crit}$ and γ can be described as (shown by the dotted line in Fig. 2.16):

$$L_{\rm Crit} = 1.56\gamma^{1/7}. \tag{2.11}$$

On the other hand, the relationship for simulated SiC MOSFETs is described as (shown by the solid line in Fig. 2.16):

$$L_{\rm Crit} = 0.31\gamma^{1/4}. \tag{2.12}$$

The (calculated) γ and the channel length for a fabricated MOSFET can be plotted on Fig. 2.16. If the point is located in the shaded region, the MOSFET will show the short-channel effects. Although the critical channel lengths of the fabricated SiC MOSFETs show a trend similar to the simulation results, the absolute values of experimental critical channel length are longer than those simulated. From Fig. 2.16, the decrease of γ is effective to suppress the short-channel effects in SiC MOSFETs as in the case of Si MOSFETs. The thinner oxide thickness, shallower junction depth, and higher doping concentration of p-body bring the electrical "long-channel" behavior in the physical "short-channel" MOSFETs.

2.4.4 Discussion

The short-channel effects are most pronounced at high drain voltage in the lightly-doped MOSFETs. The depletion layer from the drain region is more extended at higher drain voltage, resulting in the occurrence of short-channel effects. The extension of depletion region is more significant in lightly-doped devices, which promotes the occurrence of short-channel effects. To investigate the dependence of crystal face orientation, MOSFETs were

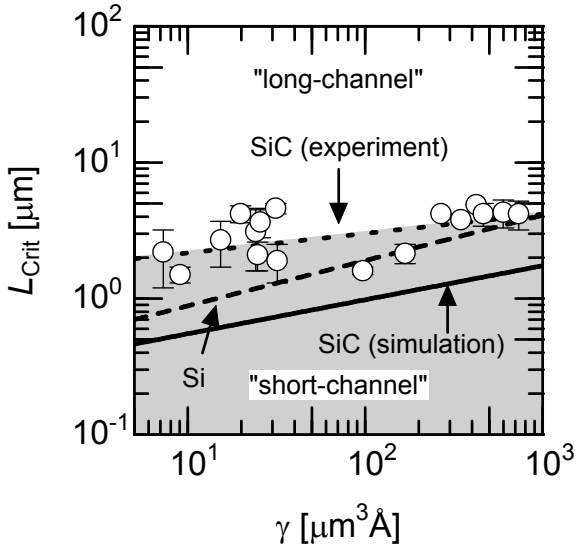


Figure 2.16: Critical channel length versus γ relationship for the fabricated and simulated SiC MOSFETs. Open circles with error bars and dotted line represent experimental results and their least-square fit, respectively. Solid line means the relationship for the simulated SiC MOSFETs and dashed lines the empirical relationship for Si MOSFETs. The short-channel SiC MOSFETs are determined by the ΔV_{T} definition.

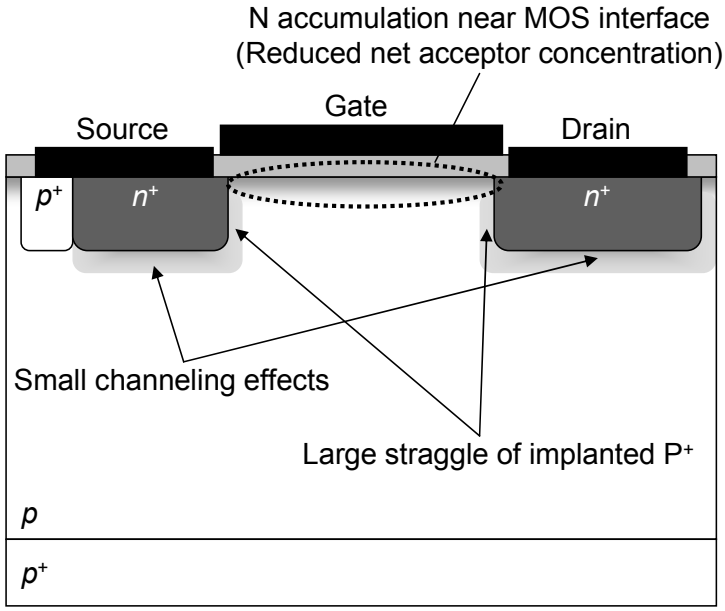
fabricated on (0001), (000$\bar{1}$), and (11$\bar{2}$0) faces. However, MOSFETs on each face showed similar phenomena when the channel length was reduced, and the crystal face dependencies were hardly observed.

To realize high-performance CMOS circuits, both n- and p-channel MOSFETs are required. In this chapter, n-channel MOSFETs were fabricated and characterized. In the case of p-channel MOSFETs, the critical channel length is expected to be almost the same as that for n-channel MOSFETs because the device parameters to estimate critical channel length are not related to the conduction type.

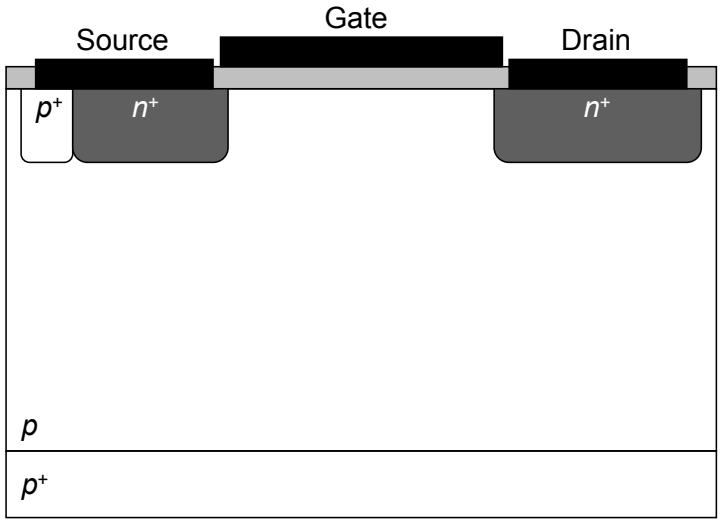
Compared with the simulation results, the experimental threshold voltage was decreased at relatively long channel length. The reasons for the decrease in experimental threshold voltage at relatively long-channel length are described below. The acceptor concentration in SiC near the MOS interface in the fabricated MOSFETs may be lower than the value determined by C–V measurements on as-grown epilayers. After thermal oxidation, the nitrogen atoms are accumulated in SiC near the MOS interface [19]. The increase of nitrogen concentration naturally leads to the decrease of the acceptor concentration near the MOS interface. Another reason may be related to the junction depth in the fabricated MOSFETs. The junction depth (0.2 μm) in the fabricated MOSFETs was simulated by a transport of ions in matter (TRIM) code. However, the real junction depth becomes lager, due to small channeling effects during implantation and slight diffusion near the tail region [20]. Both the decrease of the acceptor concentration and the increase of the junction depth enhance the extension of depletion layer, and lower the potential inside channel region. This suggests that short-channel effects occur more easily in the fabricated MOSFETs, compared with the simulated MOSFETs. Although the channel length was determined from SEM images of SiC surface, the distance between the source and drain region may be shorter in the buried region because of the larger straggle of high-energy P^+ implantation. This may also enhance the short-channel effects in the fabricated devices. These reasons are summarized in Fig. 2.17. Figure 2.17 (a) indicates the structure of the "real" (fabricated) MOSFET and Fig. 2.17 (b) that of the "ideal" (simulated) MOSFET. The N accumulation near the MOS interface, the small channeling effects, and large straggle of implanted P^+ induce the occurrence of the short-channel effects at longer channel length than simulated critical channel length. Therefore, in Fig. 2.16, the critical channel length of the fabricated SiC MOSFETs is longer than that of the simulated SiC MOSFETs. The existence of effective fixed charges at the MOS interface is one of reasons why the short-channel effects occurred at relatively long-channel length as discussed in Section 2.6.

2.5 Short-Channel Effects at High Temperature

As shown in Fig. 2.13, the experimental threshold voltage gradually decreases from a relatively long-channel length region when the channel length is reduced, while the simulated



(a)



(b)

Figure 2.17: Structure of (a) the "real" (fabricated) SiC MOSFET and (b) the "ideal" (simulated) SiC MOSFET. In the real MOSFET, accumulation of nitrogen atoms near the MOS interface, small channeling effects, and large straggle of implanted phosphorus ions with high energy take place. These effects lead to the increase of "γ".

threshold voltage shows a steep decrease near the critical channel length. Thus, the critical channel lengths of fabricated MOSFETs may be overestimated due to the gradual decrease of threshold voltage in the relatively long-channel region, in addition to the reasons mentioned in Section 2.4.4. This gradual decrease of threshold voltage may be caused by effective fixed charges at the MOS interface. To investigate the influence of the effective fixed charges on the short-channel effects, MOSFET characteristics at high temperature were analyzed. Figure 2.18 shows the temperature dependence of threshold voltage for 4H-SiC (0001) MOSFETs fabricated in this study. In Fig. 2.18, the theoretical threshold voltage is also indicated as a solid line. The difference between the experimental and theoretical threshold voltage is caused by the existence of the negative fixed charges at the MOS interface. The threshold voltage decreased at higher temperature, meaning that the decrease of the negative effective fixed charges is due to the enhanced electron emission from interface states. Figure 2.19 exhibits the relationship between the threshold voltage and channel length in the fabricated 4H-SiC (0001) MOSFETs at room temperature (RT) and high temperature (125 °C). The simulated result is also shown by a solid curve. At high temperature, the gradual decrease in the threshold voltage is suppressed, and the relationship between the threshold voltage and the channel length approaches the result obtained by device simulation. As a result, the critical channel lengths at high temperature become shorter than those at RT.

Figure 2.20 shows the relationship between the critical channel length and the γ for the fabricated 4H-SiC MOSFETs at 125 °C. Although only a limited number of devices are plotted, the critical channel length for the fabricated SiC MOSFETs at high temperature (solid line in Fig. 2.20) is slightly shorter than that at RT (dotted line in Fig. 2.20 (Eq. 2.11)). The critical channel length at 125 °C can be expressed as:

$$L_{\mathrm{Crit}} = 1.16\gamma^{1/6}. \tag{2.13}$$

The reduction of the effective fixed charge density at the MOS interface may lead to the shortening of the critical channel length.

2.6 Discussion

From the experimental results, the effective fixed charges may affect the occurrence of the short-channel effects. The effective fixed charges are located at the SiO_2/SiC interface because interface states trap the electrons induced when applying gate voltage. The influence of the effective fixed charges on the short-channel effects are theoretically discussed below. An original model for the relationship between threshold voltage and channel length including the influence of the effective fixed charges is proposed.

In general, the threshold voltage can be simply described as [9]:

$$V_{\mathrm{T}} = V_{\mathrm{FB}} + 2\Psi_{\mathrm{B}} + \frac{Q_{\mathrm{B}}}{C_{\mathrm{OX}}A}, \tag{2.14}$$

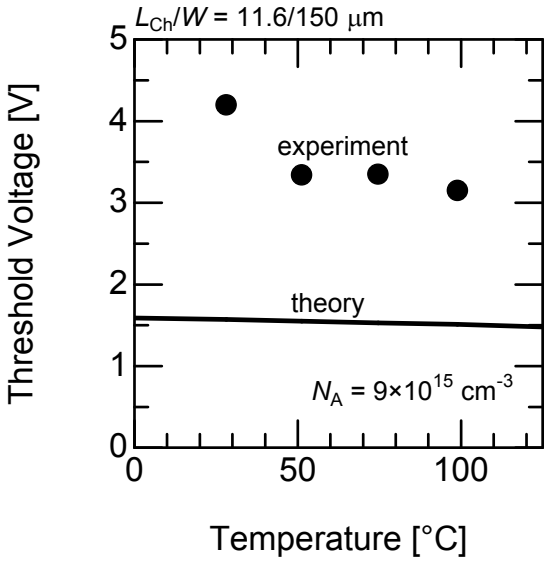


Figure 2.18: Temperature dependence of threshold voltage for a lightly-doped 4H-SiC (0001) MOSFET. The threshold voltage decreased with elevating temperature.

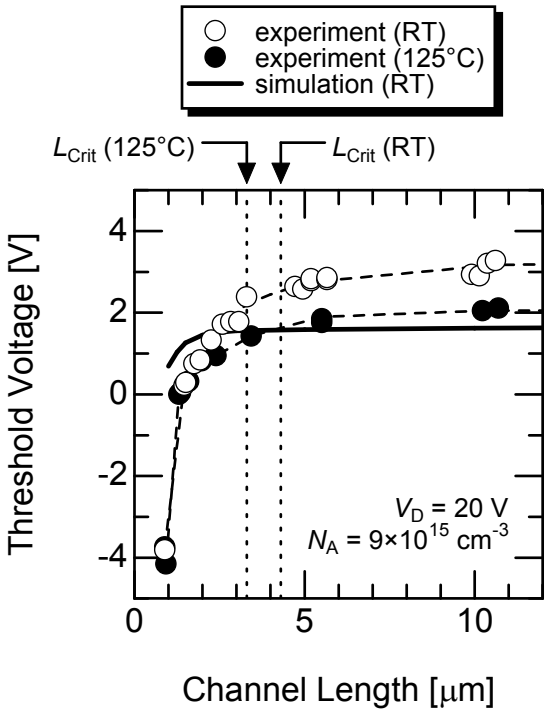


Figure 2.19: Channel length dependence of threshold voltage at RT and 125 °C in 4H-SiC (0001) MOSFETs with lightly-doped p-body. Open and closed circles mean the results experimentally obtained at RT and 125 °C, respectively. The simulated relationship is also plotted by a solid curve. At high temperature, the decrease of threshold voltage occurred more steeply at shorter channel length than at room temperature.

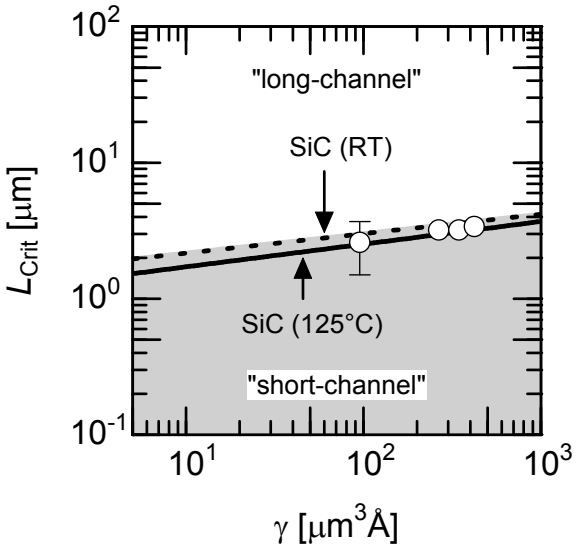


Figure 2.20: Critical channel length versus γ relationship for the fabricated 4H-SiC MOSFETs at 125 °C. Open circles with error bars and solid line represent experimental results and their least-square fit, respectively. Dotted line means the critical channel length at RT for the fabricated SiC MOSFETs.

where V_{FB} is the flatband voltage, Ψ_{B} the difference between the Fermi potential and the intrinsic Fermi potential, Q_{B} the total ionized acceptor in the depletion region, and A the gate area ($W \times L_{\mathrm{Ch}}$). For long-channel MOSFETs, the following equation is basically satisfied,

$$Q_{\mathrm{B}} = eN_{\mathrm{A}}W_{\mathrm{MOS}}A, \tag{2.15}$$

where e is the elementary charge and W_{MOS} the maximum depletion width beneath the gate electrode, which is expressed as:

$$W_{\mathrm{MOS}} = \sqrt{\frac{4\varepsilon_{\mathrm{S}}\Psi_{\mathrm{B}}}{eN_{\mathrm{A}}}}, \tag{2.16}$$

where ε_{S} is the permittivity of the semiconductor. On the other hand, for short-channel MOSFETs, the total ionized acceptors which are controlled by the gate voltage is expressed by:

$$Q'_{\mathrm{B}} = eN_{\mathrm{A}}W_{\mathrm{MOS}}W\frac{L_{\mathrm{Ch}} + {L_{\mathrm{Ch}}}'}{2}. \tag{2.17}$$

Here,

$${L_{\mathrm{Ch}}}' = L_{\mathrm{Ch}} - L_{\mathrm{S}} - L_{\mathrm{D}}, \tag{2.18}$$

where L_{S} and L_{D} is shown in Fig. 2.21 (a). This model is generally known as the "charge-share model" [21]. Figure 2.21 (a) shows the structure of short-channel MOSFET, where the depletion region is also indicated. In the short-channel MOSFETs, the total ionized acceptors are assumed to be equal to the space charge existing in the area of the shaded region in Fig. 2.21 (a). Figure 2.21 (b) is the magnification of the drain region in Fig. 2.21 (a). From Fig. 2.21 (b), L_{D} needs to satisfy the following equation:

$$(r_{\mathrm{j}} + y_{\mathrm{D}}(0\,\mathrm{eV}))^2 = (r_{\mathrm{j}} + L_{\mathrm{D}})^2 + {W_{\mathrm{MOS}}}^2, \tag{2.19}$$

where y_{D} is given as:

$$y_{\mathrm{D}}(\Psi_{\mathrm{S}}) = \sqrt{\frac{2\varepsilon_{\mathrm{S}}}{eN_{\mathrm{A}}}(V_{\mathrm{bi}} + V_{\mathrm{D}} - \Psi_{\mathrm{S}})}, \tag{2.20}$$

where V_{bi} is the built-in potential and Ψ_{S} the surface potential. From Eq. 2.19, L_{D} can be calculated as:

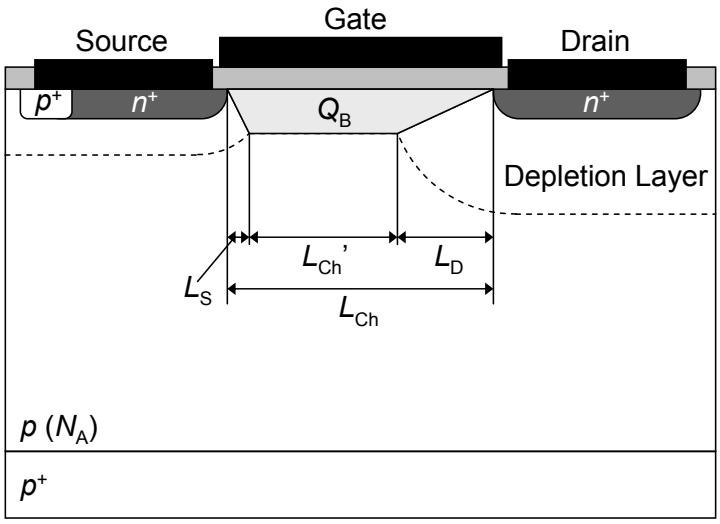
$$L_{\mathrm{D}} = \sqrt{(r_{\mathrm{j}} + y_{\mathrm{D}}(0\,\mathrm{eV}))^2 - {W_{\mathrm{MOS}}}^2} - r_{\mathrm{j}}. \tag{2.21}$$

In a similar way, L_{S} can be obtained as:

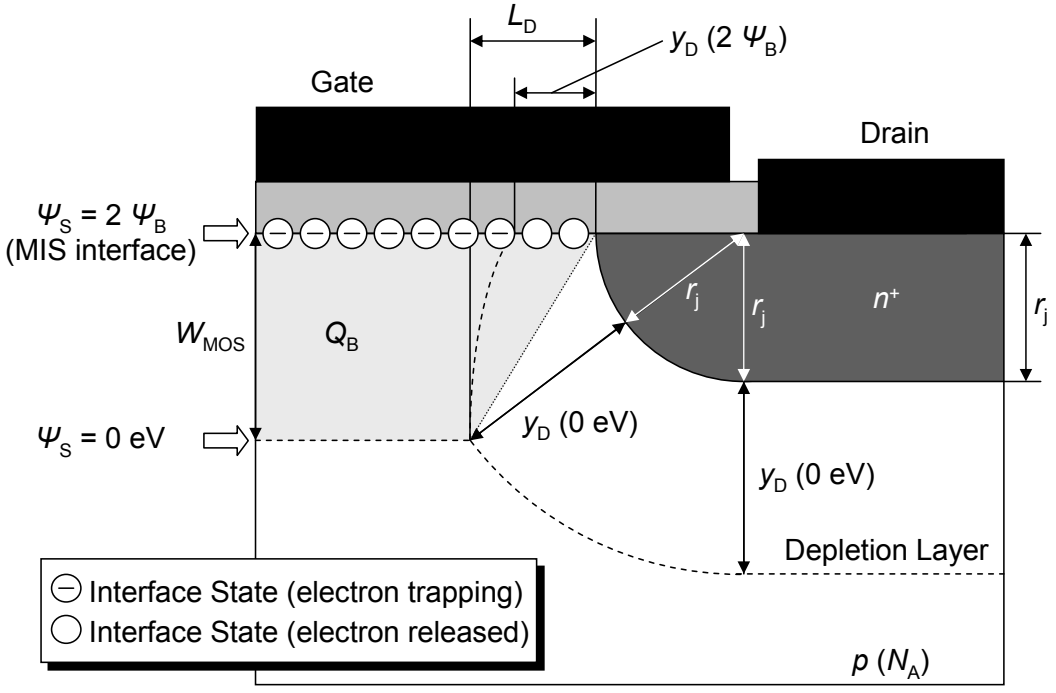
$$L_{\mathrm{S}} = \sqrt{(r_{\mathrm{j}} + y_{\mathrm{S}}(0\,\mathrm{eV}))^2 - {W_{\mathrm{MOS}}}^2} - r_{\mathrm{j}}, \tag{2.22}$$

where y_{S} is described as:

$$y_{\mathrm{S}}(\Psi_{\mathrm{S}}) = \sqrt{\frac{2\varepsilon_{\mathrm{S}}}{eN_{\mathrm{A}}}(V_{\mathrm{bi}} - \Psi_{\mathrm{S}})}. \tag{2.23}$$



(a)



(b)

Figure 2.21: Structures of (a) a short-channel MOSFET and (b) the magnification of the drain region. In (a), L_{Ch}, $L_{\mathrm{Ch}}{}'$, L_{S}, and L_{D} are indicated. Q_{B} is the total ionized acceptors controlled by the gate voltage, which are equal to the space charge existing in the area of shaded region in (a). In (b), W_{MOS}, r_{j}, and $y_{\mathrm{D}}(\Psi_{\mathrm{S}})$ are indicated.

By using Eqs. 2.18, 2.21, and 2.22, the following equation can be obtained,

$$L_{\mathrm{Ch}}{}' = L_{\mathrm{Ch}} - r_{\mathrm{j}} \left\{ \left(\sqrt{\left(1 + \frac{y_{\mathrm{S}}(0\,\mathrm{eV})}{r_{\mathrm{j}}}\right)^2 - \left(\frac{W_{\mathrm{MOS}}}{r_{\mathrm{j}}}\right)^2} - 1 \right) + \left(\sqrt{\left(1 + \frac{y_{\mathrm{D}}(0\,\mathrm{eV})}{r_{\mathrm{j}}}\right)^2 - \left(\frac{W_{\mathrm{MOS}}}{r_{\mathrm{j}}}\right)^2} - 1 \right) \right\}. \quad (2.24)$$

Therefore, the difference in the threshold voltage between long-channel and short-channel devices can be represented as:

$$\begin{aligned} \Delta V_{\mathrm{T}} &= \left(V_{\mathrm{FB}} + 2\Psi_{\mathrm{B}} + \frac{Q'_{\mathrm{B}}}{C_{\mathrm{OX}}A}\right) - \left(V_{\mathrm{FB}} + 2\Psi_{\mathrm{B}} + \frac{Q_{\mathrm{B}}}{C_{\mathrm{OX}}A}\right) \\ &= \frac{eN_{\mathrm{A}}W_{\mathrm{MOS}}W}{C_{\mathrm{OX}}L_{\mathrm{Ch}}W}\left(\frac{L_{\mathrm{Ch}} + L_{\mathrm{Ch}}{}'}{2} - L_{\mathrm{Ch}}\right) \\ &= -\frac{eN_{\mathrm{A}}W_{\mathrm{MOS}}r_{\mathrm{j}}}{2C_{\mathrm{OX}}L_{\mathrm{Ch}}} \left\{ \left(\sqrt{\left(1 + \frac{y_{\mathrm{S}}(0\,\mathrm{eV})}{r_{\mathrm{j}}}\right)^2 - \left(\frac{W_{\mathrm{MOS}}}{r_{\mathrm{j}}}\right)^2} - 1 \right) \right. \\ &\qquad \left. + \left(\sqrt{\left(1 + \frac{y_{\mathrm{D}}(0\,\mathrm{eV})}{r_{\mathrm{j}}}\right)^2 - \left(\frac{W_{\mathrm{MOS}}}{r_{\mathrm{j}}}\right)^2} - 1 \right) \right\}. \end{aligned} \quad (2.25)$$

By using this classical charge-share model, the change in threshold voltage can be theoretically calculated.

Thus far, the effective fixed charges have not been considered. By taking the effective fixed charges, density of which is Q_{eff}, into account, Eq. 2.14 can be modified as follows:

$$V_{\mathrm{T}} = V_{\mathrm{FB}} + 2\Psi_{\mathrm{B}} + \frac{Q_{\mathrm{B}}}{C_{\mathrm{OX}}A} - \frac{eQ_{\mathrm{eff}}A'}{C_{\mathrm{OX}}A}. \quad (2.26)$$

The last term in Eq. 2.26 means threshold voltage shift caused by the existence of the effective fixed charges. For short-channel MOSFETs, the last term in Eq. 2.26 can be modified as:

$$\frac{eQ_{\mathrm{eff}}A'}{C_{\mathrm{OX}}A} = \frac{eQ_{\mathrm{eff}}W(L_{\mathrm{Ch}} - y_{\mathrm{S}}(2\Psi_{\mathrm{B}}) - y_{\mathrm{D}}(2\Psi_{\mathrm{B}}))}{C_{\mathrm{OX}}WL_{\mathrm{Ch}}}. \quad (2.27)$$

Here, the interface states which are located within $y_{\mathrm{D}}(2\Psi_{\mathrm{B}})$ and $y_{\mathrm{S}}(2\Psi_{\mathrm{B}})$ from the drain and source regions, respectively, were assumed to emit the electrons because the depletion layer is extended from these regions to the channel region. Therefore, when the effective fixed charges are considered, the difference in threshold voltage between long-channel and

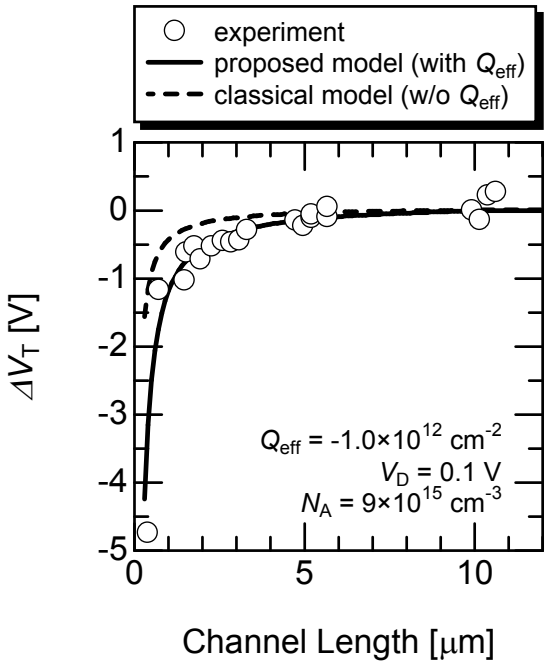
short-channel devices is changed from Eq. 2.25 to:

$$\Delta V_{\mathrm{T}} = -\frac{eN_{\mathrm{A}}W_{\mathrm{MOS}}r_{\mathrm{j}}}{2C_{\mathrm{OX}}L_{\mathrm{Ch}}}\left\{\left(\sqrt{\left(1+\frac{y_{\mathrm{S}}(0\,\mathrm{eV})}{r_{\mathrm{j}}}\right)^2-\left(\frac{W_{\mathrm{MOS}}}{r_{\mathrm{j}}}\right)^2}-1\right)\right.$$
$$\left.+\left(\sqrt{\left(1+\frac{y_{\mathrm{D}}(0\,\mathrm{eV})}{r_{\mathrm{j}}}\right)^2-\left(\frac{W_{\mathrm{MOS}}}{r_{\mathrm{j}}}\right)^2}-1\right)\right\}$$
$$+\frac{eQ_{\mathrm{eff}}(y_{\mathrm{S}}(2\Psi_{\mathrm{B}})+y_{\mathrm{D}}(2\Psi_{\mathrm{B}}))}{C_{\mathrm{OX}}L_{\mathrm{Ch}}}. \quad (2.28)$$

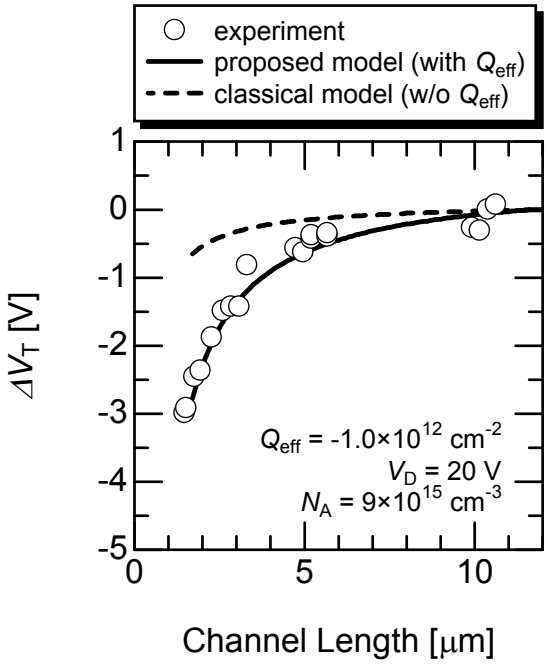
By using the proposed charge-share model (Eq. 2.28), the channel length dependence of the threshold voltage was calculated. For comparison, the classical model (Eq. 2.25) was also used to estimate the relationship between the channel length and the threshold voltage.

Figure 2.22 shows the channel length dependence of the change in threshold voltage (ΔV_{T}) in (a) linear region and (b) saturation region for the lightly-doped 4H-SiC (0001) MOSFETs. In Fig. 2.22, the change in threshold voltage measured from the fabricated MOSFETs is indicated by open circles. The solid line means the theoretical change, which is calculated by taking the effective fixed charges into account (Eq. 2.28). When the effective fixed charges are not taken into account (Eq. 2.25), the relationship between the change in threshold voltage and the channel length can be theoretically calculated as a dashed line in Fig. 2.22. In the calculation, an effective fixed charge density of $-1.0\times10^{12}\,\mathrm{cm}^{-2}$ was assumed [2]. The effective fixed charge density for the calculation ($-1.0\times10^{12}\,\mathrm{cm}^{-2}$) is taken from the value calculated from the difference between the theoretical and experimental threshold voltage of long-channel MOSFETs ($-1.0\times10^{12}\,\mathrm{cm}^{-2}$). In both linear and saturation regions, the theoretical relationship calculated by using the proposed model agrees very well with experimental results, compared with that obtained by using the classical model. In this calculation, the effective fixed charges are assumed to be the same as the charges trapped in interface states. Note that the real fixed charges near the MOS interface affect the absolute value of threshold voltage and not the channel length dependence of threshold voltage. From these results, the decrease in experimental threshold voltage in the relatively long-channel region can be attributed to the effective fixed charges at the SiO_2/SiC interface. As a result, the experimental critical channel length was longer than the simulated critical channel length. To shorten the critical channel length, the reduction of the effective fixed charges at the MOS interface is important.

[2]The effective fixed charges are negatively charged. Thus, the density of effective fixed charge indicates negative value.



(a)



(b)

Figure 2.22: Channel length dependence of the change in threshold voltage for 4H-SiC MOSFETs on lightly-doped epilayer in (a) linear region and (b) saturation region. The experimental results are shown as open circles. The solid curve means the theoretical relationship calculated by using the proposed model (the effective fixed charges are considered (Eq. 2.28)). The dashed curve denotes the relationship obtained by using the classical model (the effective fixed charges are unconsidered (Eq. 2.25)).

2.7 Summary

Short-channel effects in 4H-SiC MOSFETs were investigated. The fabricated 4H-SiC MOSFETs exhibited the punchthrough behavior, DIBL, the deterioration of subthreshold characteristics, the decrease of threshold voltage, and the saturation of transconductance. Similar phenomena were also observed in the simulated MOSFETs. In the MOSFETs on the lightly-doped (about $1 \times 10^{16}\,\mathrm{cm}^{-3}$) epilayer, the short-channel effects occurred at a relatively long-channel length of 3–5 μm, while slight short-channel effects were observed in the MOSFETs on the highly-doped (about $1 \times 10^{17}\,\mathrm{cm}^{-3}$) with a 1 μm-long channel.

The critical channel length, below which the short-channel effects occur, was analyzed. The boundary between short-channel devices and long-channel devices can be described as "$L_{\mathrm{Crit}} = 1.56\gamma^{1/7}$" for the fabricated MOSFETs and "$L_{\mathrm{Crit}} = 0.31\gamma^{1/4}$" for the simulated MOSFETs. The critical channel length for the fabricated MOSFETs was longer than that for the simulated MOSFETs. The difference in critical channel length for Si and 4H-SiC MOSFETs is not very large, because the occurrence of the short-channel effects is mainly affected by the depletion layer extended from the drain and not by the bandgap or breakdown field. The crystal face dependence was hardly observed.

The influence of the effective fixed charges located at the SiC MOS interface on the short-channel effects was also investigated. An original charge-share model, which takes the effective fixed charges into account, has been proposed. When the effective fixed charges are located at the MOS interface, the threshold voltage is decreased by reducing channel length in the relatively long-channel region. From the theoretical calculation, the effective fixed charges affect this decrease in threshold voltage in the relatively long-channel region. The main reason for the long critical channel length for the fabricated MOSFETs, compared with that for the simulated MOSFETs, can be attributed to the presence of effective fixed charges. The reduction of the effective fixed charges contributes greatly to the shortening the critical channel length.

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Chapter 3

Interface and Dielectric Properties of SiC MIS Structures with Thermally-Grown and Deposited Insulators

3.1 Introduction

Despite the superior physical and chemical properties of SiC [1], the performance of SiC metal-insulator-semiconductor (MIS)-based devices has been limited by its poor interface properties. To enhance the performance of SiC MIS-based devices, the gate insulators/SiC interface has been investigated by a number of groups. As a result, the oxidation or re-oxidation in NO or N_2O ("nitridation" processes) [2–4] is one of the effective processes to improve the interface properties of SiC n-channel MIS devices. Although the reason of the improvement of the interface properties by nitridation has not been fully understood, it is put forward the hypothesis that nitrogen atoms may passivate the interface states. The N^+ implantation into surface of SiC before oxidation leads to accumulation of nitrogen atoms at the SiO_2/SiC interface and causes reduction of interface state density [5, 6] and increase of channel mobility [7]. Therefore, the introduction of nitrogen atoms near the gate insulators/SiC interface has an important role in enhancement of SiC MIS-based device performance.

SiC MIS devices are affected by carbon contamination into gate insulators, unlike Si MIS devices, because SiC consists of Si and "C". Several groups have reported the evidence for the existence of a transition layer between thermally-grown pure SiO_2 and SiC [8–10]. The interfacial transition layer may deteriorate the performance of SiC MIS devices [8]. Thus, the formation of interfacial transition layer should be eliminated or minimized. In addition, it was found out that the high density of interface state near the conduction band edge (about $10^{13}\,\mathrm{cm^{-2}eV^{-1}}$) adversely affects the performance of n-channel MIS devices

because a number of carriers is trapped at the interface states and becomes immobile [11]. In n-channel metal-oxide-semiconductor (MOS)-based devices, one of origins for the high interface state density in the shallow energy region is "near-interface traps (NITs)", which are the states not in SiC but in SiO_2 and are located at an energy depth of 2.77 eV from the conduction band edge of SiO_2 (Fig. 3.1) [12]. The energy position of NITs is within the bandgap of 4H-SiC because the conduction band offset between SiC and SiO_2 is 2.74 eV. Therefore, the reduction of NITs is vital for SiC MOS devices.

Considering these factors, regarding the degradation of SiC MIS device performance, the deposition technique is one of the most promising processes for the formation of gate insulators because the interfacial transition layer will not or be hardly formed when gate insulators are deposited. The deposited insulators have other advantages; i) superior reliability (when adequately processed) [13–15], ii) reduction of process time, and iii) nearly isotropic formation of insulators on trench sidewalls. In this chapter, the deposited SiO_2 and SiN_x/SiO_2 are applied to the gate insulators for SiC MIS devices. Compared with thermally-grown SiO_2, the deposited SiO_2 has many advantages such as suppression of interfacial transition layer. In the case of the deposited SiN_x/SiO_2, by inserting the SiN_x layer between the deposited SiO_2 and SiC, the influence of NITs can be weakened as shown in Fig. 3.2 and the nitrogen concentration at the interface can be increased. After deposition, the insulators were annealed in N_2O to introduce additional nitrogen atoms into the gate insulators/SiC interface and to improve dielectric properties of the gate insulators. Current-voltage (I–V) and time dependent dielectric breakdown (TDDB) measurements were also performed to investigate the dielectric properties of gate insulators.

3.2 Experimental

N-type MIS capacitors were fabricated on 8 ° off-axis n-type 4H-SiC (0001) epilayers with a donor concentration of 7–10 $\times$ 10^{15} cm^{-3}. For p-type MIS capacitors, 8 ° off-axis p-type 4H-SiC (0001) epilayers with an acceptor concentration of 3–8 $\times$ 10^{15} cm^{-3} were prepared. Before the gate insulator formation, the samples were subjected to the RCA cleaning method [16], which is a standard technique in the Si MOS process. Even in SiC, it is reported that the RCA cleaning is effective in reducing the interface state density and fixed oxide charges [17, 18]. After RCA cleaning, gate insulators were thermally grown or deposited. Detailed processes are described in each section. The thickness of the gate oxides (d_{OX}) for MOS capacitors and equivalent oxide thickness (EOT) for MIS capacitors calculated by the accumulation capacitance were 40–100 nm. After the gate insulators were formed, the oxides grown on backside were removed by dipping buffered HF (BHF). Then, Al was evaporated on the backside and annealed at 600 °C for 10 min for n-MIS capacitors. For p-MIS capacitors, Ti/Al/Ni annealed at 950 °C for 5 min was used as the substrate contact. The circular gate metal was Al with a diameter of 520 μm for capacitance-voltage (C–V)

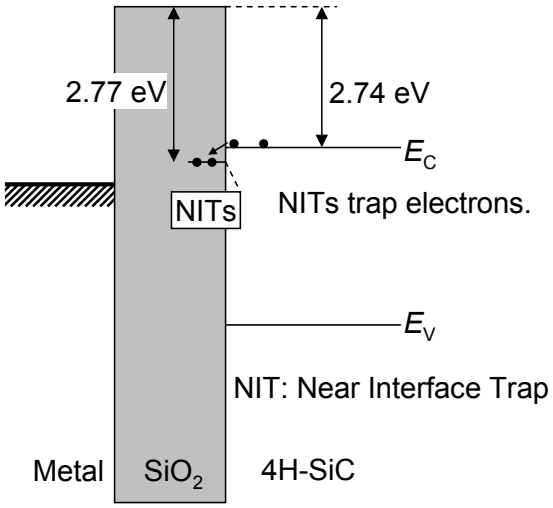


Figure 3.1: Schematic energy band diagram of an SiO_2 single-gate MOS structure.

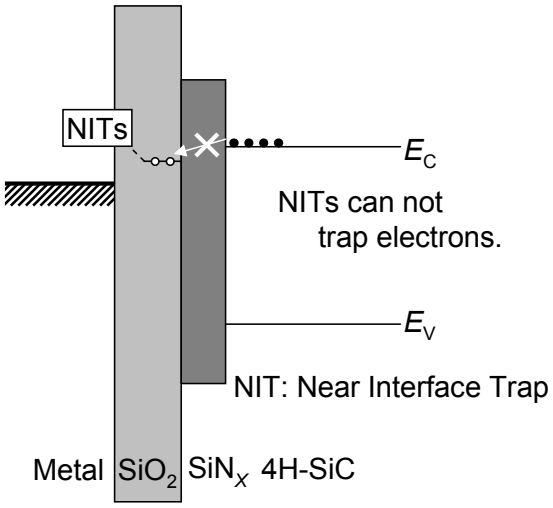


Figure 3.2: Schematic energy band diagram of an SiN_x/SiO_2 stack-gate MIS structure.

measurements and 180 μm for I–V measurements for both n- and p-MIS capacitors. For TDDB measurements, P-doped poly-Si was used as the square-shaped gate electrode with an area of $3.39 \times 10^{-4}\,\mathrm{cm}^2$.

Quasi-static and high-frequency (1 MHz for n-MIS capacitors and 100 kHz for p-MIS capacitors) C–V characteristics (C_{QS} and C_{HF}, respectively) were measured by using a simultaneous C–V system at room temperature (RT) under dark condition to estimate the interface state density. The typical voltage sweep rate for C–V measurements was 0.03 V/s and the voltage sweep was started from the deep-depletion bias condition. The interface state density was calculated basically by a high-low method.

I–V measurements were also performed to measure the breakdown field of the gate insulators. The gate insulator field was corrected by taking account of the flatband-shift voltage. The typical ramp rate for I–V measurements was about 0.03 V/s.

The TDDB measurements were carried out at RT under dark condition to investigate the reliability of the gate insulators. The number of devices for TDDB measurements was 32 for each condition. In the TDDB measurements, the constant field stress was applied. The charge-to-breakdown (Q_{BD}) was determined at a cumulative failure of 63.2 %

The gate insulator/SiC interface was in accumulation during the I–V and TDDB measurements.

3.3 Thermal SiO_2 Grown in N_2O

3.3.1 Formation Process of Gate Oxides

The gate oxide, which was grown in dry N_2O, was used as a reference. The detailed formation process of the gate oxide, including the oxidation system, is mentioned below.

Figure 3.3 shows a schematic illustration of an oxidation system used in this study. The oxidation system consists of high-purity N_2O and N_2 gases, flow meters to control the gas flow, a quartz tube, a resistive-heating furnace, and a chemical trap to remove NO. After RCA cleaning, the samples were immediately loaded into the oxidation furnace. Thermal SiO_2 was grown in N_2O (10 % diluted in N_2) at 1300 °C for 8 h, followed by post-oxidation annealing (POA) in N_2 for 30 min. The thermal oxidation procedure is as follows:

1. The furnace temperature was raised to the oxidation temperature within 1 h.
2. The temperature was kept at 1300 °C during oxidation in dry N_2O (10 % diluted in N_2).
3. The gas was changed from mixture of N_2O and N_2 to pure N_2, and POA in N_2 was done at 1300 °C for 30 min.
4. The furnace temperature was cooled down to 600 °C in N_2 with a cooling rate of −5 °C/min. Then, the temperature fell naturally to RT.

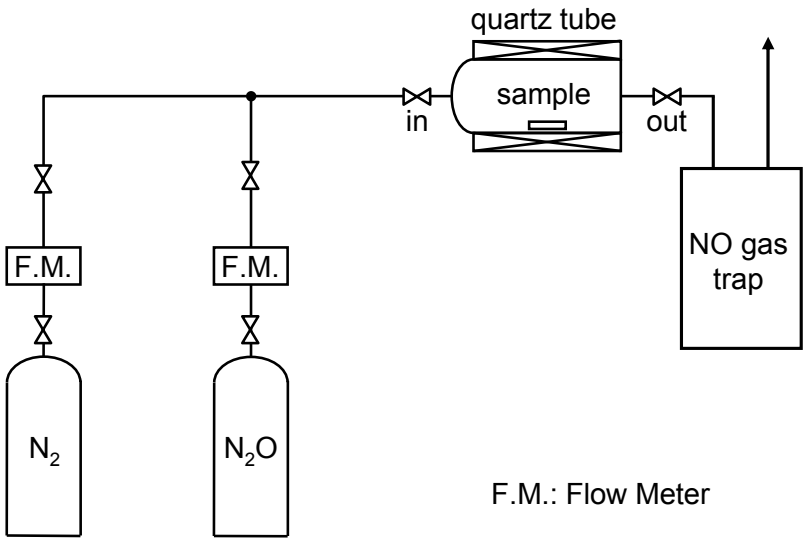


Figure 3.3: Schematic illustration of an oxidation system used in this study.

The samples were unloaded at RT. The thickness of the gate oxide (SiO_2) was about 53 nm.

The "nitridation" process is widely accepted for the fabrication of SiC n-channel MOS field-effect transistors (MOSFETs) because reasonably high channel mobility can be obtained by the oxidation or reoxidation in NO or N_2O [2–4]. N_2O decomposes into O_2, N_2, and NO at 1300 °C, and NO acts as a nitridation gas. During the oxidation, N_2O is diluted in N_2 because a low ratio of N_2O in N_2 leads to improved properties of the gate oxides [2, 19].

3.3.2 Interface Properties

Figure 3.4 shows the quasi-static, high-frequency (1 MHz), and theoretical C–V characteristics of a typical n-MOS capacitor with N_2O-grown oxides. The flatband capacitance (C_{FB}) is also shown in Fig. 3.4 as a horizontal dashed line. In the SiC MIS capacitors, the C–V curves show deep depletion characteristics, unlike in the case of Si MIS capacitors, because of its low intrinsic carrier concentration (about $10^{-9}\,cm^{-3}$) at RT due to the wide bandgap of SiC. The shift of flatband voltage (ΔV_{FB}) was 2.6 V. From the flatband voltage shift, the effective fixed charge density (Q_{eff}) can be calculated by using the following equation [1],

$$Q_{eff} = -\frac{C_i \Delta V_{FB}}{e}, \tag{3.1}$$

where C_i is the insulator capacitance per unit area and e the elementary charge. The calculated density of effective fixed charge was $-1.1 \times 10^{12}\,cm^{-2}$ for the n-MOS capacitors with N_2O-grown oxides. The effective fixed charge density is the sum of the density of real fixed charge (positive and negative) and the density of charges trapped at the interface states (negative in n-MIS capacitors and positive in p-MIS capacitors). In the case of SiC n-MIS capacitors, negative effective fixed charges are observed due to the high density of charges trapped at the interface states. From the measured C–V characteristics, the interface state density (D_{IT}) was calculated by using the high-low method and is shown in Fig. 3.5. Although the interface state density at the 0.6 eV from the conduction band edge is $2 \times 10^{11}\,cm^{-2}eV^{-1}$, that is exponentially increased to $2 \times 10^{12}\,cm^{-2}eV^{-1}$ at 0.2 eV from the conduction band edge. The N_2O-grown oxide/4H-SiC (0001) interface shows superior characteristics to the dry O_2-grown oxide/4H-SiC (0001) interface [20, 21], at which the density of interface states is about $10^{13}\,cm^{-2}eV^{-1}$ [20, 21].

3.3.3 Application to *P*-Type MOS Capacitors

To investigate the influence of N_2O oxidation on the interface states near the valence band edge, C–V characteristics of p-MOS capacitors were also measured. The measured quasi-static and high-frequency (100 kHz) C–V characteristics are shown in Fig. 3.6, in which the

[1] The negative value of effective fixed charge density means that negative charge is located at the interface. When the density indicates positive value, positive charge exists at the interface.

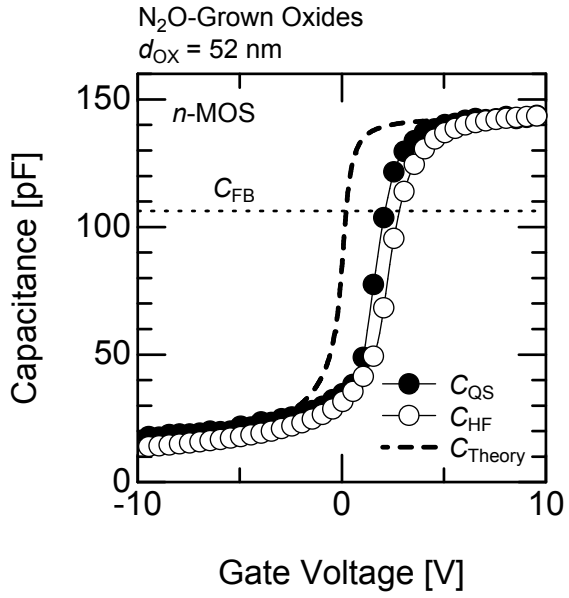


Figure 3.4: C–V characteristics for an n-MOS capacitor with an N_2O-grown oxide. Closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

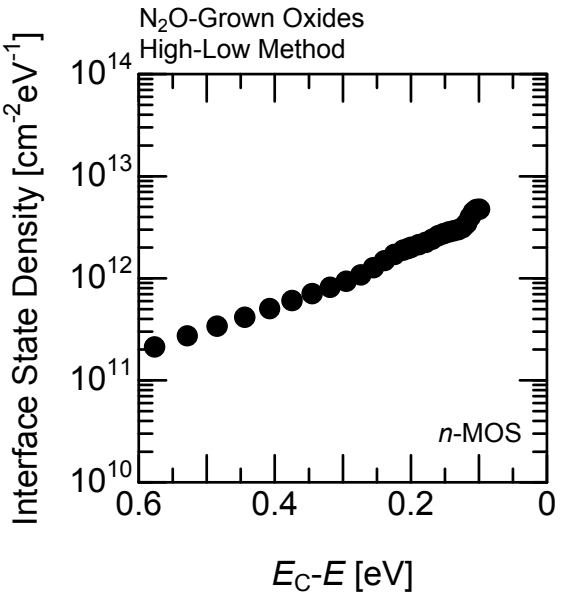


Figure 3.5: Interface state density near the conduction band edge calculated by using the high-low method for an n-MOS capacitor with an N_2O-grown oxide.

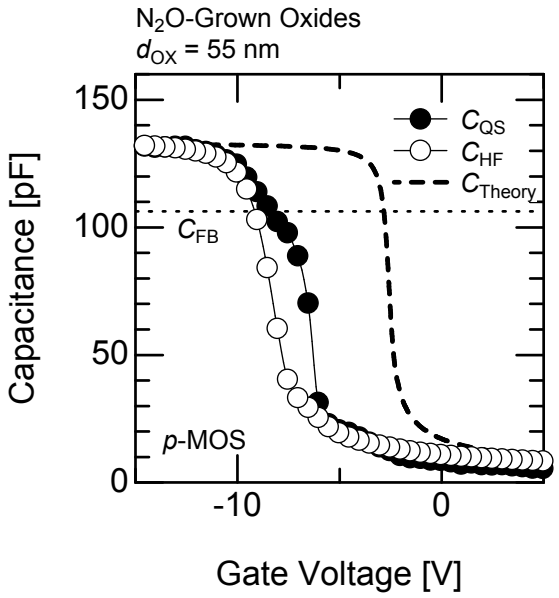


Figure 3.6: C–V characteristics for a p-MOS capacitor with an N_2O-grown oxide. Closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

theoretical C–V characteristic and the flatband capacitance are also indicated. The effective fixed charge density was calculated to be $2.4 \times 10^{12}\,\mathrm{cm}^{-2}$. Figure 3.7 shows the interface state density near the valence band edge for the p-MOS capacitor with an N_2O-grown oxide. The interface states are uniformly distributed with a density of $9 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ in the energy range from $E_V + 0.1\,\mathrm{eV}$ to $E_V + 0.6\,\mathrm{eV}$. The interface state density near the valence band edge was lower than that near the conduction band edge, which implies that the p-channel MOSFETs with N_2O-grown oxides may show reasonably high channel mobility.

3.4 Deposited SiO_2

3.4.1 Formation Process of Gate Oxides

The gate oxide was deposited by using plasma-enhanced chemical vapor deposition (PECVD) and annealed in N_2O. The detailed formation process of the gate oxide is mentioned below.

After RCA cleaning with final HF dip, the samples were loaded into the PECVD system. In the PECVD, the SiO_2 films were deposited at 350 °C by using SiH_4 and N_2O as source gases. Then, the samples were annealed in N_2O (10 % diluted in N_2) at 1300 °C for 0–4 h, followed by N_2 annealing at 1300 °C for 30 min. An N_2O-annealing time of 0 h means that the samples were annealed only in N_2 for 30 min. The thermal annealing procedure is the same as that introduced in Section 3.3.1.

During N_2O annealing, the oxide thickness increased by Δd_{OX}, as shown in Fig. 3.8. Before the N_2O annealing, the thickness of deposited SiO_2 was about 75 nm, which was estimated by using ellipsometry. Table 3.1 lists the final thickness of the deposited oxides after N_2O annealing and the increment of the thickness during the annealing for n-MOS capacitors. The thickness of deposited oxides annealed only in N_2 (an N_2O-annealing time of 0 h) was 75 nm. For p-MOS capacitors, the thickness of deposited SiO_2 by PECVD was 76 nm. After N_2O annealing for 1 h, the thickness was increased to 80 nm ($\Delta d_{OX} = 4$ nm).

3.4.2 Interface Properties

Figure 3.9 shows the C–V characteristics of an n-MOS capacitor with deposited SiO_2 annealed in N_2O for 1 h. Compared with the n-MOS capacitors with N_2O-grown oxides shown in Fig. 3.4, the difference between the quasi-static and high-frequency C–V characteristics becomes smaller. The effective fixed charge density of the n-MOS capacitor with deposited oxides annealed in N_2O for 1 h was $-2.2 \times 10^{11}\,\mathrm{cm}^{-2}$, which is about one-fifth of that for the n-MOS capacitors with N_2O-grown oxides.

Figure 3.10 shows the distribution of the interface state density (D_{IT}) for the n-MOS capacitors with deposited SiO_2 annealed in N_2O for 0 h, 1 h, and 4 h. Compared with the capacitor annealed only in N_2 (N_2O-annealing time: 0 h), the capacitors annealed in N_2O

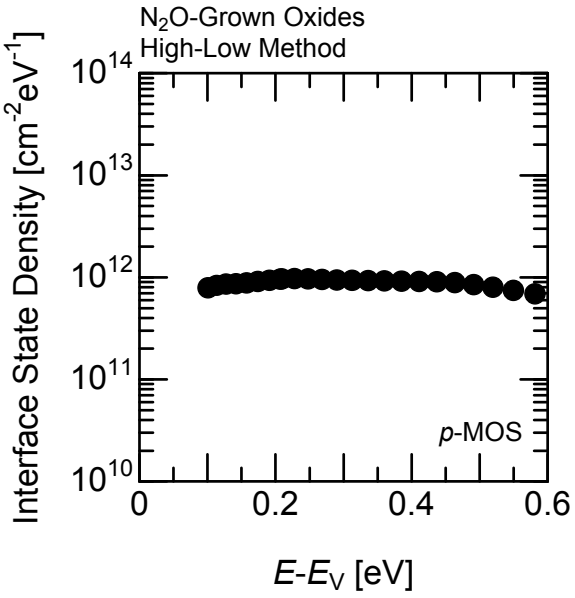


Figure 3.7: Interface state density near the valence band edge calculated by using the high-low method for a p-MOS capacitor with an N_2O-grown oxides.

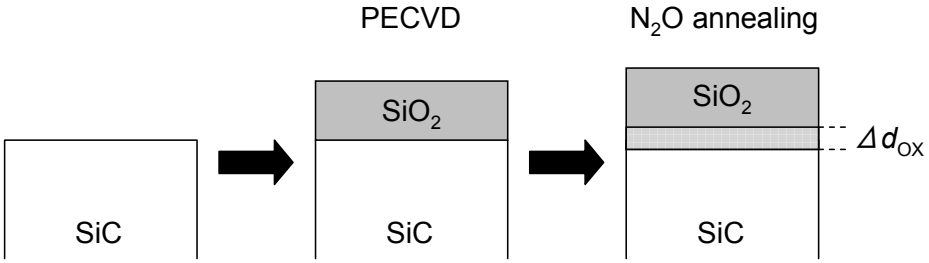


Figure 3.8: Schematic flow of PECVD and N_2O annealing for deposited SiO_2. The increment of the oxide thickness by N_2O annealing is denoted by Δd_{OX}.

Table 3.1: The thickness of the gate oxides after N_2O annealing (d_{OX}) and the increment of the thickness during the annealing (Δd_{OX}) for n-MOS capacitors. The initial thickness of deposited SiO_2 is about 75 nm.

N_2O-annealing time	d_{OX}	Δd_{OX}
1 h	78 nm	3 nm
2 h	80 nm	5 nm
4 h	85 nm	15 nm

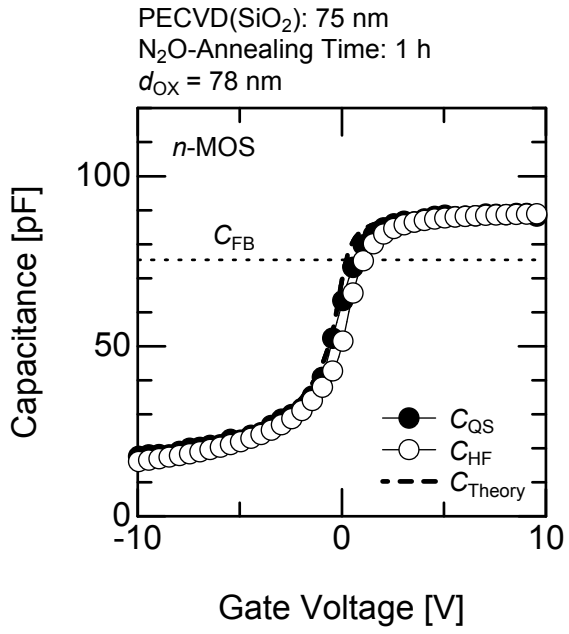


Figure 3.9: C–V characteristics for an n-MOS capacitor with deposited SiO_2 annealed in N_2O for 1 h. Closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

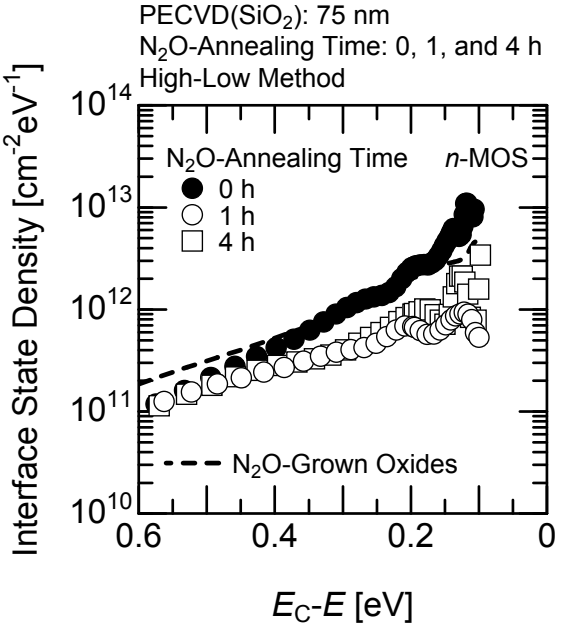


Figure 3.10: Interface state density near the conduction band edge for n-MOS capacitors with deposited SiO_2 annealed in N_2O for 0 h (closed circles), 1 h (open circles), and 4 h (open boxes). The dashed line means the result for N_2O-grown oxides.

(N_2O-annealing time: 1–4 h) exhibit lower interface state density. Although the interface state density of the n-MOS capacitor annealed only in N_2 is comparable to that of n-MOS capacitors with N_2O-grown oxides, the interface state density of the capacitors annealed in N_2O for 1 h is decreased to $7 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$ at an energy level of 0.2 eV from the conduction band edge. Therefore, the N_2O annealing is effective to improve the properties of the deposited SiO_2/4H-SiC (0001) interface.

3.4.3 N_2O-Annealing Time Dependence

The deposition of SiO_2 followed by N_2O annealing reduces the interface state density near the conduction band edge. Figure 3.11 exhibits the relationship between the increment of oxide thickness (Δd_{OX}) and the interface state density (D_{IT}) at $E_C - 0.2\,\mathrm{eV}$ and $E_C - 0.6\,\mathrm{eV}$ for the deposited SiO_2 annealed in N_2O. For comparison, the results of N_2O-grown oxides are also indicated as horizontal dashed and dotted lines. Although the interface state density of the n-MOS capacitor with the deposited oxide annealed only in N_2 at $E_C - 0.2\,\mathrm{eV}$ (N_2O-annealing time: 0 h, indicated by the closed circle in Fig. 3.11) is higher than that of the n-MOS capacitors with N_2O-grown oxides, the n-MOS capacitors with deposited oxides followed by N_2O annealing show lower interface state density. The n-MOS capacitors with deposited SiO_2 show a minimum interface state density of $7 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$ at $E_C - 0.2\,\mathrm{eV}$ when the increment of oxide thickness becomes 3 nm. The additional increment of oxide thickness leads to slight increase of interface state density. On the other hand, the interface state density of n-MOS capacitors with deposited oxides at $E_C - 0.6\,\mathrm{eV}$ does not depend on the increment of oxide thickness. Therefore, the deposition of SiO_2 followed by N_2O annealing is particularly effective to reduce the interface state density near the conduction band edge and the interface state density shows a minimum value when the increment of oxide thickness during N_2O annealing is about 3 nm.

In this study, the SiO_2 was deposited by PECVD with SiH_4 and N_2O as source gases. In this case, the lowest interface state density could be obtained when the increment of oxide thickness becomes 3 nm. The channel mobility was also increased to over $25\,\mathrm{cm^2/Vs}$ in the MOSFETs fabricated under similar condition (the detail will be discussed in Chapter 4). In the case of SiO_2 deposited with TEOS and O_2 as source gases, high channel mobility (25–30 $\mathrm{cm^2/Vs}$) was achieved at an increment of oxide thickness of 3–5 nm [22]. From these results, the MOS interface properties and MOSFET performance hardly depend on the source gases of deposited SiO_2 and may be influenced by the properties of the SiO_2 grown during the N_2O annealing and SiC interface, not by the properties of deposited SiO_2 and SiC interface. Therefore, the precise control of the annealing condition (increment of oxide thickness during N_2O annealing) is important to obtain an improved MOS interface, rather than the choice of the source gases needed to form SiO_2.

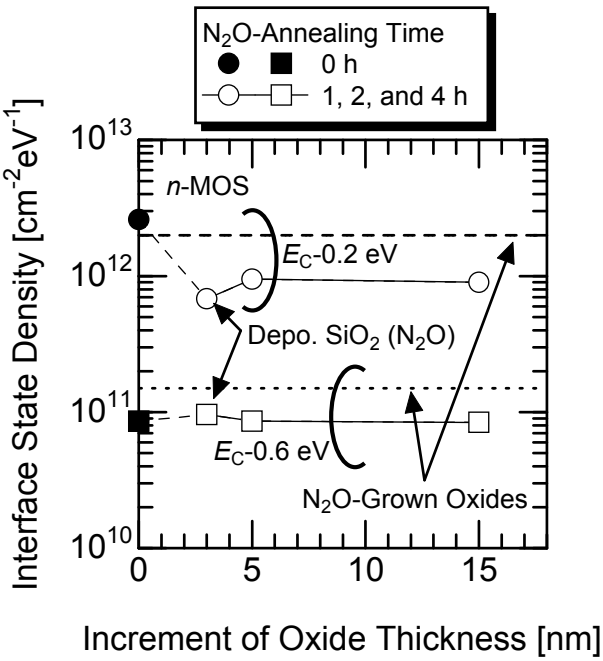


Figure 3.11: The relationship between the interface state density and the increment of oxide thickness during N_2O annealing (Δd_{OX}). Open and closed circles and dashed line represent the interface state density at $E_C - 0.2\,eV$, and open and closed boxes and dotted line that at $E_C - 0.6\,eV$. Open and closed symbols show the results for deposited oxides, and dashed and dotted lines the results for N_2O-grown oxides.

3.4.4 Application to *P*-Type MOS Capacitors

P-MOS capacitors with deposited SiO_2 were also characterized. From the *C*–*V* characteristics, the effective fixed charge density was calculated to be $1.5 \times 10^{12}\,\mathrm{cm}^{-2}$ for the *p*-MOS capacitors with deposited SiO_2 annealed in N_2O for 1 h. Compared with the *p*-MOS capacitors with N_2O-grown oxides, the effective fixed charge density was decreased in the *p*-MOS capacitors with deposited SiO_2. The interface state density distribution near the valence band edge is shown in Fig. 3.12. The interface state density is also reduced to $5 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ at $E_\mathrm{V} + 0.2\,\mathrm{eV}$ in the *p*-MOS capacitors with deposited SiO_2 annealed in N_2O. The deposited SiO_2 followed by N_2O annealing is effective to decrease the interface state density in the shallow energy region not only from the conduction band edge but also from the valence band edge as shown in Figs. 3.10 and 3.12.

3.5 Deposited SiN_x/SiO_2

3.5.1 Formation Process of Gate Insulators

The gate insulators were deposited by using PECVD and annealed in N_2O. The detailed formation process of the gate insulators is mentioned below.

After RCA cleaning with final HF dip, the samples were loaded into the PECVD system. In the PECVD, the SiN_x films were deposited by using SiH_4 and NH_3 as source gases. Then, subsequent SiO_2 deposition was carried out without exposure to air. In the SiO_2 deposition, SiH_4 and N_2O were used as source gases. The typical deposition temperature was about 400 °C. The thickness of SiN_x and SiO_2 was varied in the range from 10 nm to 40 nm and in the range from 40 nm to 60 nm, respectively. After the PECVD processes, the samples were annealed in N_2O (10 % diluted in N_2) at 1300 °C for 0–2 h, followed by N_2 annealing at 1300 °C for 30 min. During N_2O annealing, the SiN_x layer is oxidized and a portion of SiN_x layer is converted to the SiO_xN_y layer, as shown in Fig. 3.13. The thermal annealing procedure is the same as that introduced in Section 3.3.1.

3.5.2 Interface Properties

The density of interface states for stack-gate MIS capacitors with a deposited SiN_x/SiO_2 thickness of 10 nm/55 nm is shown in Fig. 3.14. The N_2O-annealing time was either 0 min or 30 min. Figure 3.14 also shows the interface states density for the MOS capacitors with N_2O-grown oxides. The density of interface states for the stack-gate MIS capacitor annealed in N_2O for 30 min is lower than that for the stack-gate MIS capacitor annealed in N_2 (N_2O-annealing time: 0 min). N_2O annealing is more effective in reducing the interface states than N_2 annealing for the SiN_x/SiO_2 stack-gate structure. Compared with N_2O-grown oxides, the stack-gate structure followed by N_2O annealing for 30 min exhibits low interface state density near the conduction band edge.

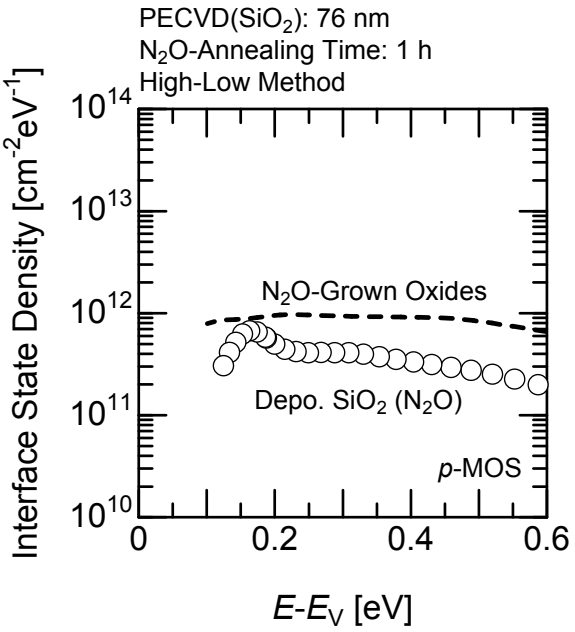


Figure 3.12: Interface state density near the valence band edge for a p-MOS capacitor with deposited SiO_2 annealed in N_2O for 1 h (open circles). The result for N_2O-grown oxides is also shown as the dashed line.

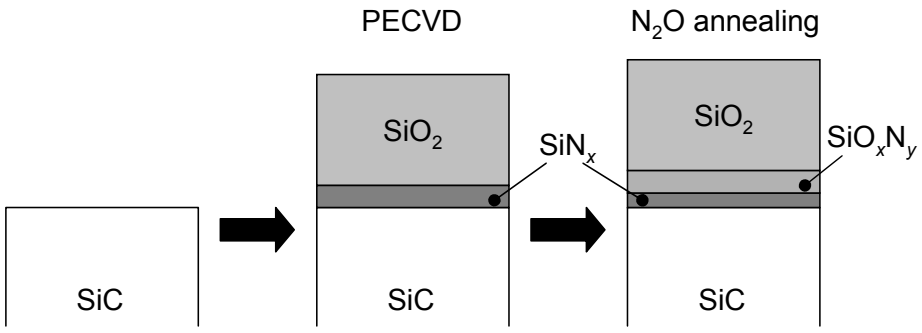


Figure 3.13: Schematic flow of PECVD and N_2O annealing for deposited SiN_x/SiO_2 stack-gate structure. During N_2O annealing, a portion of SiN_x layer is oxidized and converted to SiO_xN_y layer.

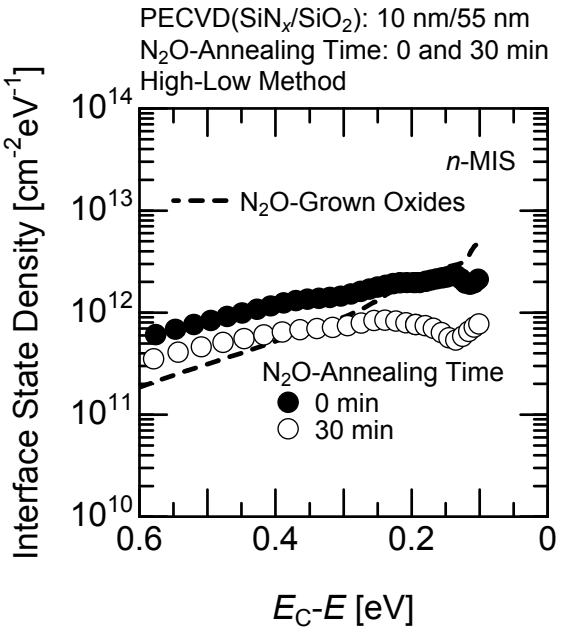


Figure 3.14: Interface state density near the conduction band edge for n-MIS capacitors with deposited SiN_x/SiO_2 annealed in N_2O for 0 min (closed circles) and 30 min (open circles). The thickness of deposited SiN_x/SiO_2 is 10 nm/55 nm. The dashed line means the result for N_2O-grown oxides.

3.5.3 SiN_x Thickness Dependence

To optimize the deposition and annealing condition, the SiN_x thickness dependence of interface state density was investigated. Figure 3.15 shows the interface state density distribution near the conduction band edge for SiN_x/SiO_2 stack-gate n-MIS capacitors annealed in N_2O for 30 min with various SiN_x/SiO_2 thickness values. The thickness of the deposited SiN_x/SiO_2 films is 10 nm/50 nm, 20 nm/45 nm, and 40 nm/40 nm, and EOT is almost the same (57–67 nm). In Fig. 3.15, the interface state density of n-MOS capacitors with thermal oxides grown in N_2O is also shown for comparison. Although the SiN_x/SiO_2 stack-gate MIS capacitors with thick SiN_x layers (15 nm, 20 nm) exhibit higher interface state density than the capacitor with N_2O-grown oxides, the interface state density of n-MIS capacitor with an SiN_x thickness of 10 nm is lower than that of n-MOS capacitors with N_2O-grown oxides in the shallow energy region ($E_C - E < 0.2$ eV).

To confirm the nitridation and oxidation during N_2O annealing, the secondary ion mass spectroscopy (SIMS) measurements were performed. Figure 3.16 shows the results of SIMS measurements for the stack-gate n-MIS capacitor with an SiN_x/SiO_2 thickness of 10 nm/50 nm. The N_2O-annealing time was 30 min. The depth profile of Si, C, N, and O atoms were measured, where the depth resolution was about 3 nm. From Fig. 3.16, the oxygen atoms are clearly detected even between SiO_2 and SiC, indicating that the initial-SiN_x layer was oxidized during N_2O annealing. The oxygen ion count is decreased near SiC, which means the SiN_x layer still remains between the SiO_xN_y and SiC.

In the stack-gate MIS capacitor with an SiN_x/SiO_2 thickness of 10 nm/50 nm, the SiN_x layer was oxidized during N_2O annealing, and a portion of SiN_x layer was converted to an SiO_xN_y layer. Then, the MIS structure is changed to SiC/thin-$SiN_x/SiO_xN_y/SiO_2$ stack-gate structure from $SiC/SiN_x/SiO_2$ stack-gate structure. Influence of traps inside the SiN_x layer may be decreased by thinning the SiN_x layer. Thus, the low interface state density is obtained in the stack-gate MIS capacitor with the thin SiN_x layer annealed in N_2O.

3.5.4 N_2O-Annealing Time Dependence

The C–V characteristics of stack-gate MIS capacitors annealed in N_2O for (a) 30 min and (b) 2 h with a deposited SiN_x/SiO_2 thickness of 10 nm/50 nm are represented in Fig. 3.17. The accumulation capacitance was reduced by increasing N_2O-annealing time, which means that the SiN_x layer is oxidized during N_2O annealing and becomes an SiO_xN_y layer, as shown in Fig. 3.16, and thereby the EOT is increased. The MIS capacitor annealed for 30 min shows a small difference between quasi-static and high-frequency C–V curves. On the other hand, in the MIS capacitor annealed for 2 h, the high-frequency C–V curve is exactly similar to the quasi-static C–V curve (Fig. 3.17 (b)), although large negative flatband voltage shift (about -15 V) is observed. The effective fixed charge density of stack-gate MIS capacitors annealed in N_2O for 30 min and 2 h is about 2×10^{11} cm^{-2} (positive) and 6×10^{12} cm^{-2} (positive), respectively. The stack-gate MIS capacitor followed by N_2O annealing for 2 h

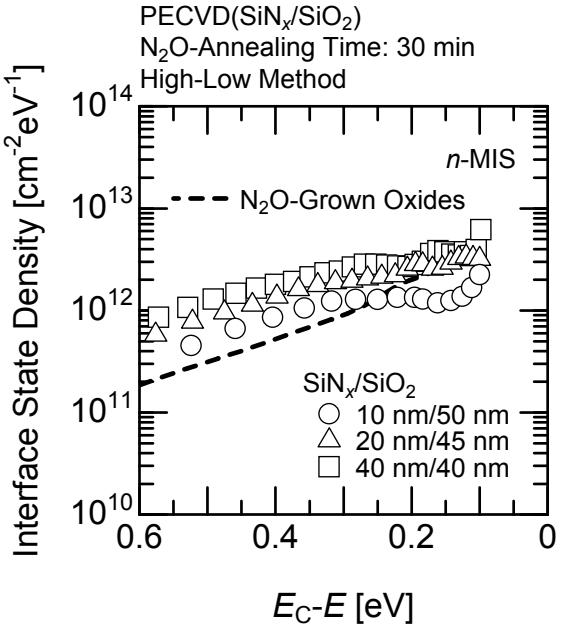


Figure 3.15: Interface state density near the conduction band edge for n-MIS capacitors with deposited SiN_x/SiO_2 annealed in N_2O for 30 min. The thickness of deposited SiN_x/SiO_2 is 10 nm/50 nm (open circles), 20 nm/45 nm (open triangles), and 40 nm/40 nm (open boxes). The dashed line means the result for N_2O-grown oxides.

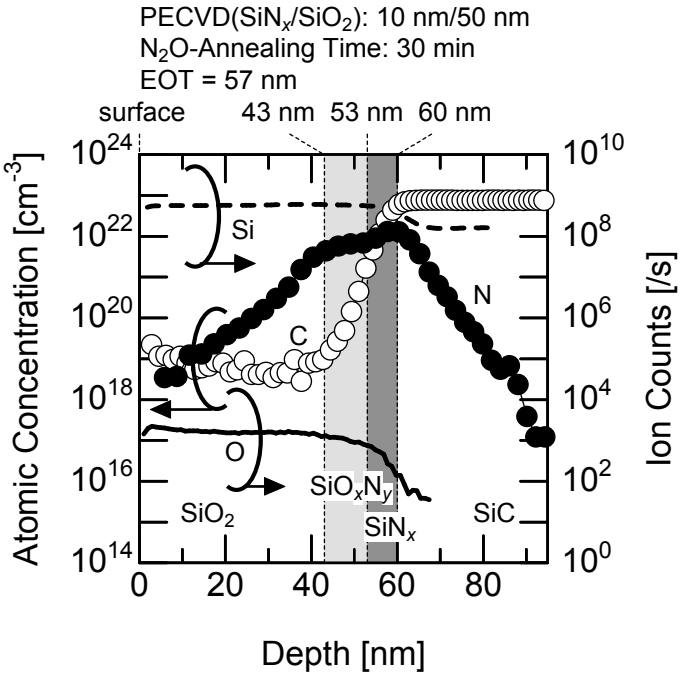
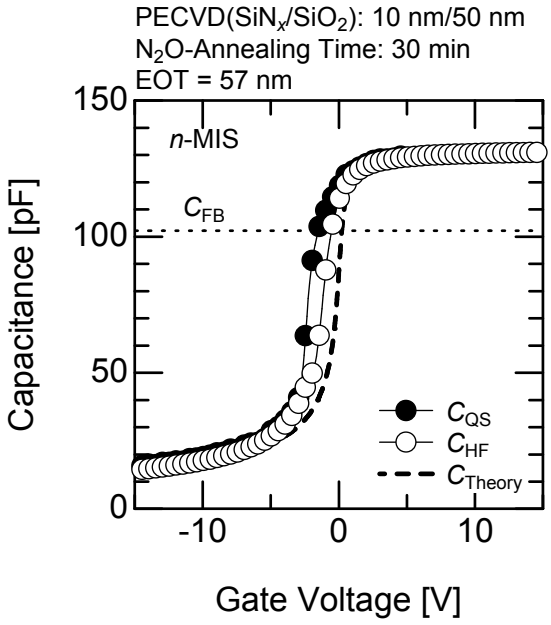
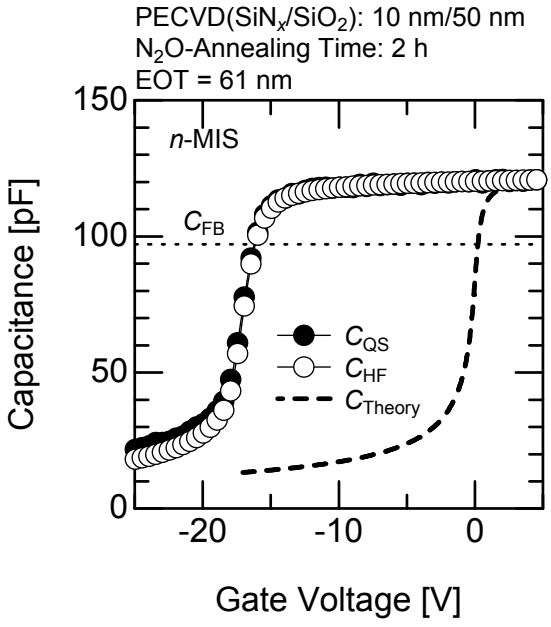


Figure 3.16: Results of SIMS measurement for the stack-gate MIS capacitor with an SiN_x/SiO_2 thickness of 10 nm/50 nm annealed in N_2O for 30 min. The open and closed circles mean the concentration of carbon and nitrogen atoms, respectively. The dashed and solid lines denote silicon and oxygen ion counts, respectively.



(a)



(b)

Figure 3.17: C–V characteristics for n-MIS capacitors with deposited SiN_x/SiO_2 annealed in N_2O for (a) 30 min and (b) 2 h. The thickness of deposited SiN_x/SiO_2 is fixed at 10 nm/50 nm. Closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

exhibits significant increase of effective fixed charges. This increase in effective fixed charges (over $3 \times 10^{12}\,\mathrm{cm}^{-2}$) was also observed in the MIS capacitor fabricated through the same process but another batch.

Figure 3.18 represents the interface state density of SiN_x/SiO_2 stack-gate n-MIS capacitors annealed in N_2O for 30 min, 1 h, and 2 h (open boxes, open triangles, and open circles, respectively), demonstrating that the interface state density could be significantly reduced by extending N_2O-annealing time. The stack-gate MIS capacitors followed by N_2O annealing for 30 min and 1 h show slight decrease of interface state density in the shallow energy region from the conduction band edge. The interface state density of the stack-gate MIS capacitor annealed for 2 h is lower than that of MOS capacitor with thermal oxides grown in N_2O at any energy levels investigated in this study, being as low as $1 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ or below.

Figure 3.19 depicts the depth profile of Si, C, N, and O atoms for the stack-gate n-MIS capacitor with a deposited SiN_x/SiO_2 thickness of 10 nm/50 nm annealed in N_2O for 2 h measured by using SIMS. In this MIS capacitor, the oxygen atoms are detected between SiO_2 and SiC as is the case with an N_2O-annealing time of 30 min (Fig. 3.16). The oxygen ion counts are almost constant in the region between SiO_2 and SiC. Thus, the initial-SiN_x layer was oxidized during N_2O annealing and completely converted to an SiO_xN_y layer. As a result, the MIS structure was changed to $SiC/SiO_xN_y/SiO_2$ stack-gate structure after annealing. The peak concentration of nitrogen atoms at the SiO_xN_y/SiC interface is about $4 \times 10^{21}\,\mathrm{cm}^{-3}$.

From Section 3.5.3, the interface properties are improved by the thinning residual-SiN_x layer after N_2O annealing. In the n-MIS capacitor with deposited SiN_x/SiO_2, of which initial thickness is 10 nm/50 nm, annealed in N_2O for 2 h, the interface state density was dramatically decreased to below $1 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. From the SIMS measurements, $SiC/SiN_x/SiO_2$ structure was changed to $SiC/SiO_xN_y/SiO_2$ structure after the annealing in N_2O for 2 h. In this structure, the influence of traps inside the SiN_x layer and NITs is neglected and hence the amazingly low density of interface states could be achieved. The large shift of flatband voltage indicates that a large number of positive charges are located inside the SiO_xN_y layer or at the SiO_xN_y/SiC interface.

3.5.5 Origin of Positive Charges

In the stack-gate n-MIS capacitor with an initial SiN_x/SiO_2 thickness of 10 nm/50 nm annealed in N_2O for 2 h, the interface state density was remarkably decreased to below $1 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. At the same time, however, a large number of positive charges, which density is over $3 \times 10^{12}\,\mathrm{cm}^{-2}$, was observed. These charges are located inside the SiO_xN_y layer (model A in Fig. 3.20 (a)) or at the SiO_xN_y/SiC interface (model B in Fig. 3.20 (a)). To know where these charges are located, the following experiment was performed.

1. The high-frequency C–V characteristics are measured, and the effective fixed charge

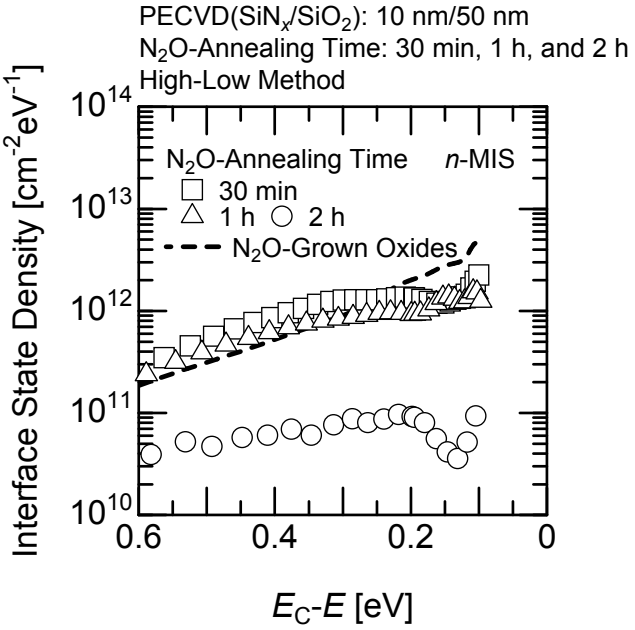


Figure 3.18: Interface state density near the conduction band edge for n-MIS capacitors with deposited SiN_x/SiO_2 annealed in N_2O for 30 min (open boxes), 1 h (open triangles), and 2 h (open circles). The thickness of deposited SiN_x/SiO_2 is fixed at 10 nm/50 nm. The dashed line means the result for N_2O-grown oxides.

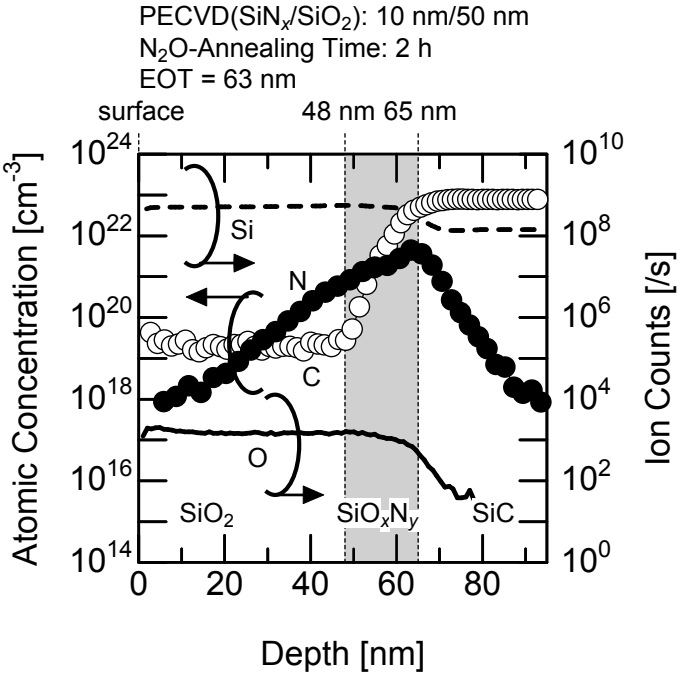
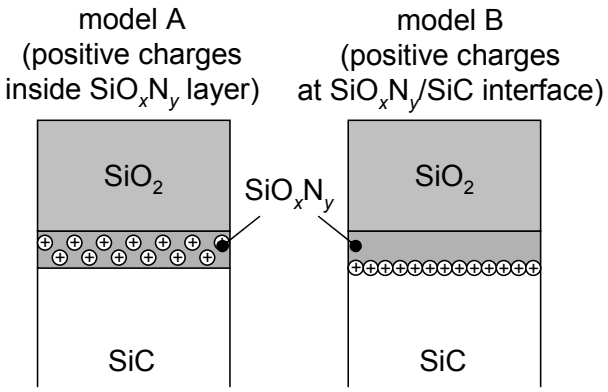
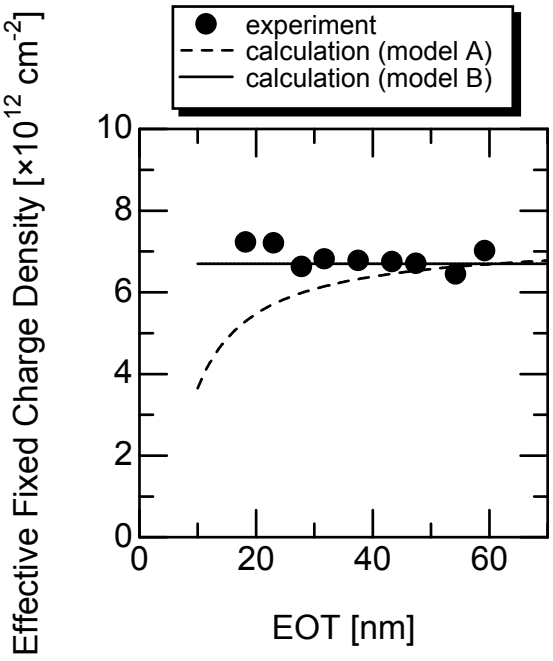


Figure 3.19: Results of SIMS measurement for the stack-gate MIS capacitor with an SiN_x/SiO_2 thickness of 10 nm/50 nm annealed in N_2O for 2 h. The open and closed circles mean the concentration of carbon and nitrogen atoms, respectively. The dashed and solid lines denote silicon and oxygen ion counts, respectively.



(a)



(b)

Figure 3.20: (a) Models for the calculation of effective fixed charge density. In model A and B, the positive charges are assumed to be located inside the SiO_xN_y layer and at the SiO_xN_y/SiC interface, respectively. (b) Relationship between EOT and effective fixed charge density. The closed circles represent the results obtained from the experiment. The dashed and solid lines mean the theoretical relationship calculated by using model A and B, respectively.

density is calculated from the shift of flatband voltage.

2. Gate electrode is removed.

3. The stack-gate structure is dipped into BHF. The top SiO_2 layer is removed from the surface, and EOT is decreased (several nm).

4. Gate electrode is formed.

This procedure was repeated several times. Then, the relationship between EOT and the effective fixed charge density could be deduced. The theoretical correlation between EOT and the effective fixed charge density can also be calculated from the following equation:

$$Q_{\text{eff}} = \int_0^{\text{EOT}} \frac{x}{\text{EOT}} \rho(x) \mathrm{d}x, \tag{3.2}$$

where x is the depth from the surface of gate insulators and $\rho(x)$ the distribution of the fixed charge density inside the SiO_xN_y layer. From Eq. 3.2, when the positive charges are located inside the SiO_xN_y layer, the density of effective fixed charge is reduced with decreasing the EOT, while the density is not changed when the charges exist at the SiO_xN_y/SiC interface. Figure 3.20 (b) shows the results obtained in the stack-gate MIS capacitor annealed for 2 h. From Fig. 3.20 (b), the experimental results indicate the density of effective fixed charge does not depend on EOT. Therefore, the positive charges are unevenly distributed and are located at the SiO_xN_y/SiC interface (model B in Fig. 3.20 (a)).

3.5.6 Formation of Thin-Thermal Oxides Before Deposition

From the analysis described in Section 3.5.5, it was found out that the positive charges, the density of which is over $3 \times 10^{12}\,\text{cm}^{-2}$, are located at the SiO_xN_y/SiC interface. Therefore, the reduction of the positive charges at the MIS interface becomes important while keeping the low interface state density.

From this point of view, the author proposes the formation of thin oxides before deposition of SiN_x/SiO_2 to suppress generation of the positive charges at the MIS interface. By inserting thin oxides between SiC and deposited SiN_x/SiO_2, the MIS interface changes from SiO_xN_y/SiC to SiO_2/SiC. In addition, the influence of NITs is very small and the interfacial transition layer is hardly formed because the thickness of thermal oxides is very thin.

The dry N_2O oxidation at 1300 °C for 5 min was performed to form thin oxides. During oxidation, N_2O gas was diluted by 10 % in N_2. The thickness of thin oxides was 4 nm, which was measured by ellipsometry. After the formation of thin-thermal oxides, the same deposition and annealing processes mentioned in Section 3.5.1 were carried out. The SiN_x/SiO_2 films were deposited by using PECVD, and the thickness of deposited SiN_x/SiO_2 was 10 nm/50 nm. The N_2O annealing was performed at 1300 °C for 2 h. EOT of the stack-gate structure was 63 nm.

Figure 3.21 shows the quasi-static and high-frequency C–V curves of the n-MIS capacitor with thin-thermal oxide between SiN_x/SiO_2 stack-gate structure and SiC. Compared with the capacitor without thin-thermal oxide (Fig. 3.17 (b)), the remarkable reduction of flatband voltage shift is observed in the capacitor with the thin-thermal oxide. The calculated density of the effective fixed charge is below $5 \times 10^{11}\,\mathrm{cm}^{-2}$, which is about one-sixth of that for the MIS capacitor without the thin-thermal oxide (over $3 \times 10^{12}\,\mathrm{cm}^{-2}$). The interface state density was also estimated and is shown in Fig. 3.22. Although the MIS capacitor with thin-thermal oxide between stack-gate structure and SiC shows a slightly higher interface state density of $2 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ at $E_C - 0.2\,\mathrm{eV}$ compared with the MIS capacitor without thin thermal oxide, the interface state density is much lower than that of MOS capacitors with N_2O-grown oxides ($2 \times 10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$). Therefore, the formation of thin-thermal oxides before deposition of SiN_x/SiO_2 stack-gate structure is effective to minimize the generation of positive fixed charges at the MIS interface while keeping moderate interface state density.

3.5.7 Application to *P*-Type MIS Capacitors

To investigate the interface properties near the valence band edge, the p-type MIS capacitors were characterized. The p-MIS capacitors with thin-thermal oxides between stack-gate structure and SiC were fabricated. The formation process of gate insulators was the same as that mentioned in Section 3.5.6. Thin-thermal oxides were formed by N_2O oxidation for 5 min, and then the SiN_x/SiO_2 stack structure was deposited. The thickness of SiN_x/SiO_2 was 10 nm/50 nm and the N_2O-annealing time was 2 h. Figure 3.23 shows the interface state density distribution of the p-MIS capacitors with thin-thermal oxides. Compared with N_2O-grown oxides, the low interface state density near the valence band edge ($6 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$) can be achieved by using the stack-gate structure with thin oxides. From the C–V characteristics, the effective fixed charge density was calculated to be $2.4 \times 10^{12}\,\mathrm{cm}^{-2}$. By applying the thin-thermal oxides to SiN_x/SiO_2 stack-gate structure, the improved interface properties can be obtained not only in the n-MIS capacitors but also in the p-MIS capacitors.

3.6 Further Improvement of Interface Properties

3.6.1 Annealing in NO

Compared with N_2O-grown oxides, the interface properties were improved by utilizing the deposited SiO_2 followed by N_2O annealing. For further improvement of interface properties, the effects of NO annealing were explored. N_2O decomposes into O_2, N_2, and NO, which has a crucial role, during high-temperature N_2O annealing. Although the pure NO gas is tremendously harmful to our health, NO annealing is an attractive process because the generation of O_2 gas, which enhances the undesirable oxidation during N_2O annealing, can

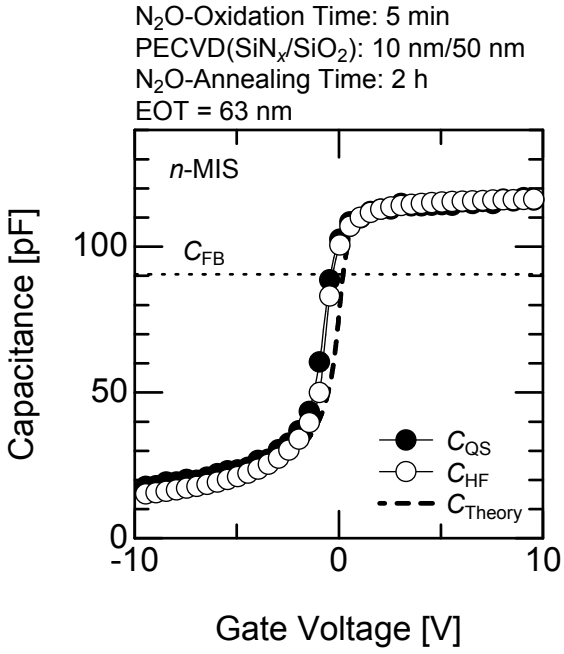


Figure 3.21: C–V characteristics for an n-MIS capacitor with a thin thermal oxide between deposited SiN_x/SiO_2 (10 nm/50 nm) and 4H-SiC (0001). The sample was annealed in N_2O at 1300 °C for 2 h. Closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

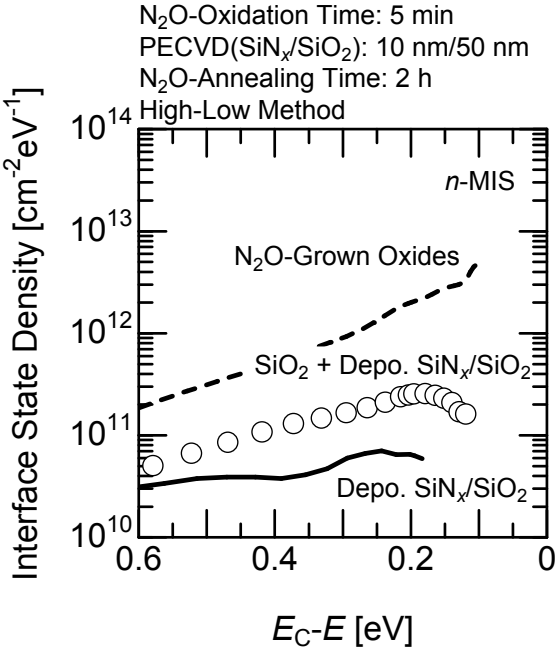


Figure 3.22: Interface state density near the conduction band edge for n-MIS capacitors with thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and 4H-SiC (0001), which were annealed in N_2O for 2 h. The dashed and solid lines mean the result for N_2O-grown oxides and stack-gate structure without thin-thermal oxides, respectively.

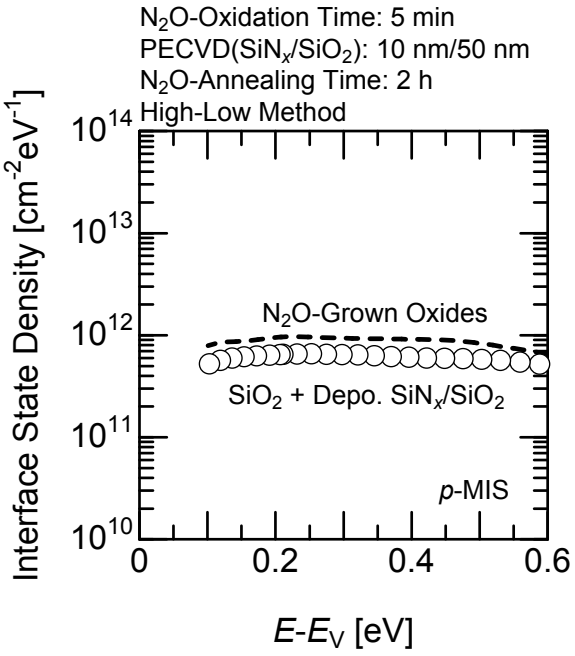


Figure 3.23: Interface state density near the valence band edge for p-MIS capacitors with thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and 4H-SiC (0001), which were annealed in N_2O for 2 h. The thickness of deposited SiN_x/SiO_2 is 10 nm/50 nm. The dashed line means the result for N_2O-grown oxides.

be suppressed.

The gate oxides were deposited by using PECVD with TEOS and O_2 as source gases. The annealing in NO (10 % diluted in N_2) was performed at 1300 °C for 1 h. The thickness of the gate oxides was 51 nm.

The distribution of interface state density for the n-MOS capacitor with deposited SiO_2 annealed in NO for 1 h is shown in Fig. 3.24. For comparison, the interface state density of the n-MOS capacitors with N_2O-grown oxides and deposited SiO_2 annealed in N_2O for 1 h is indicated as dashed and solid lines, respectively. The interface state density at $E_C - 0.2\,eV$ for the MOS capacitor with deposited SiO_2 annealed in NO is $3 \times 10^{11}\,cm^{-2}eV^{-1}$, which is lower than that of the MOS capacitors with N_2O-grown oxides ($2 \times 10^{12}\,cm^{-2}eV^{-1}$) and with deposited oxides annealed in N_2O ($7 \times 10^{11}\,cm^{-2}eV^{-1}$). The effective fixed charge density was also estimated to be $7.4 \times 10^{11}\,cm^{-2}$ from the C–V curves. The deposition of SiO_2 followed by NO annealing improves the interface properties of SiC MOS devices.

3.6.2 Utilization of 4H-SiC (000$\bar{1}$)C Face

MIS interface properties are sensitive to surface orientation: for example, MOS devices fabricated on 4H-SiC (000$\bar{1}$), (03$\bar{3}$8), and (11$\bar{2}$0) faces exhibit superior characteristics to those fabricated on the 4H-SiC (0001) face [23–25]. Although the MIS capacitors were fabricated on the 4H-SiC (0001)Si face so far, the 4H-SiC (000$\bar{1}$)C face is utilized for the fabrication of MIS capacitors.

N-MIS capacitors were fabricated on 8 ° off-axis n-type 4H-SiC (000$\bar{1}$) epilayers with a donor concentration of $1 \times 10^{15}\,cm^{-3}$. After RCA cleaning, the thin-thermal oxides were grown in N_2O (10 % diluted in N_2) at 1300 °C for 3 min. The SiN_x/SiO_2 stack-gate structure was formed and annealed in N_2O (10 % diluted in N_2) at 1300 °C for 2 h. The initial thickness of deposited SiN_x/SiO_2 was 10 nm/50 nm and EOT after N_2O annealing was 60 nm. Other processes were the same as those described in Section 3.2.

Figure 3.25 shows the quasi-static and high-frequency C–V curves of the n-MIS capacitor with a thin-thermal oxide between SiN_x/SiO_2 stack-gate structure and 4H-SiC (000$\bar{1}$). Compared with other MIS capacitors fabricated in this study, the both quasi-static and high-frequency C–V curves are nearly identical to the theoretical C–V curves. The shift of flatband voltage is almost 0 V, which indicates that the effective fixed charge density is below $1 \times 10^{11}\,cm^{-2}$. The interface state density is shown in Fig. 3.26. The n-MIS capacitor fabricated on 4H-SiC (000$\bar{1}$) exhibits a low interface state density below $1 \times 10^{11}\,cm^{-2}eV^{-1}$. The 4H-SiC (000$\bar{1}$)C face is a promising crystal face to reduce both the interface state density and effective fixed charge density.

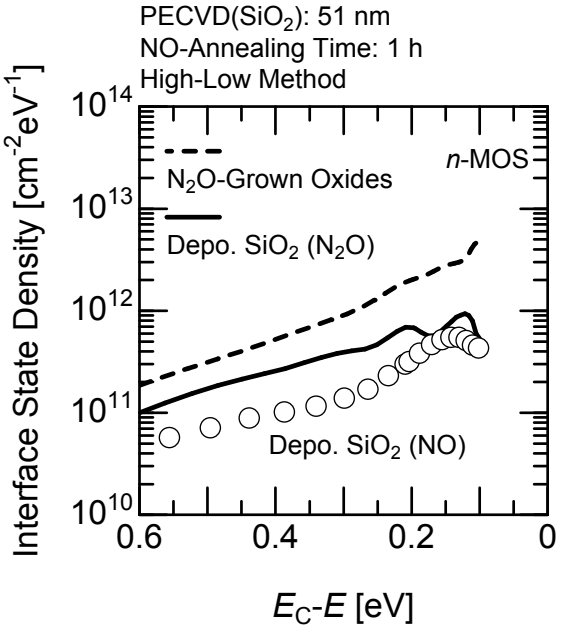


Figure 3.24: Interface state density near the conduction band edge for n-MOS capacitors with deposited SiO_2 annealed in NO for 1 h (open circles). Dashed and solid lines mean the results for N_2O-grown oxides and deposited SiO_2 annealed in N_2O for 1 h, respectively.

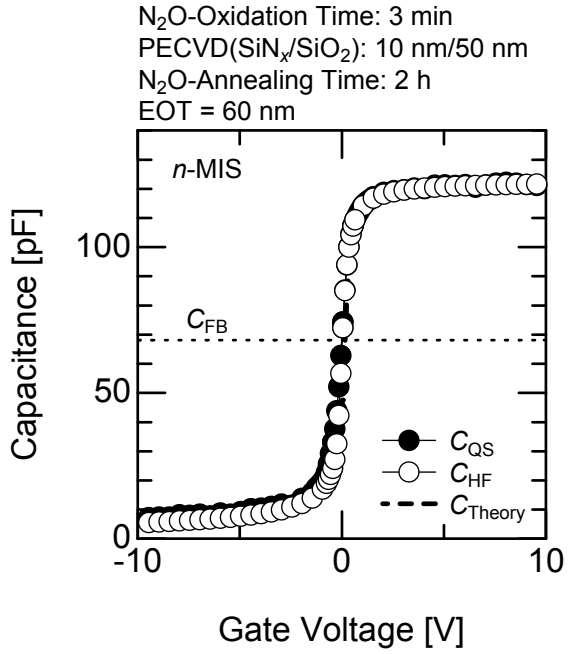


Figure 3.25: C–V characteristics for an n-MIS capacitor with a thin-thermal oxide between deposited SiN_x/SiO_2 (10 nm/50 nm) and 4H-SiC $(000\bar{1})$, which was annealed in N_2O for 2 h. Closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

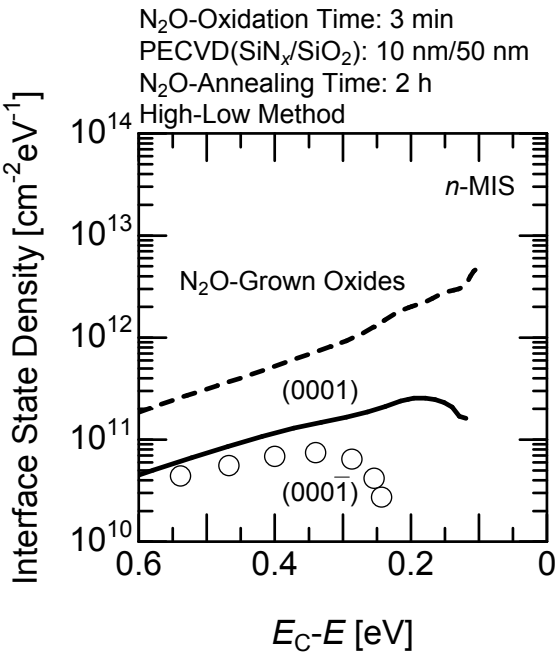


Figure 3.26: Interface state density near the conduction band edge for n-MIS capacitors with thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and 4H-SiC $(000\bar{1})$, which were annealed in N_2O for 2 h. The dashed and solid lines mean the result for N_2O-grown oxides and stack-gate structure with thin-thermal oxides on 4H-SiC (0001), respectively.

3.7 Dielectric Properties

3.7.1 Breakdown Field

To measure the breakdown field (E_{B}) of the gate insulators, I–V measurements were performed. The effective insulator field ($E_{\mathrm{i,eff}}$) was calculated by using the following equation:

$$E_{\mathrm{i,eff}} = \frac{V_{\mathrm{G}} - V_{\mathrm{FB}}}{\mathrm{EOT}}. \tag{3.3}$$

The positive and negative voltages were applied to the gate electrode of n- and p-type MIS capacitors, respectively, to make the MIS interface in accumulation. The gate current was drastically increased, leading to insulator breakdown, after the last point plotted in each graph.

N-Type MIS Capacitors

Figures 3.27 and 3.28 show the typical current density-effective insulator field characteristics for the fabricated n-MOS capacitors and n-MIS capacitors, respectively, on the 4H-SiC (0001)Si face.

The current density-effective insulator field characteristics of thermal SiO_2 grown in N_2O for 4 h, deposited SiO_2 annealed in N_2O for 1 h, and deposited SiO_2 annealed in NO for 1 h (closed circles, open boxes, and closed boxes, respectively) are shown in Fig. 3.27. The breakdown field (E_{B}) of N_2O-grown oxides is 8.9 MV/cm and higher than that of deposited oxides. Although the n-MOS capacitors with deposited SiO_2 followed by N_2O annealing show a breakdown field of 7.0 MV/cm, those with deposited SiO_2 annealed in NO exhibit lower breakdown field (5.9 MV/cm). For this reason, there is still room for improvement in dielectric properties of deposited SiO_2.

In Fig. 3.28, the I–V characteristics of the n-MIS capacitors with deposited SiN_x/SiO_2 stack-gate structures are shown. A high breakdown field of 9.5 MV/cm can be obtained in the n-MIS capacitors with a deposited SiN_x/SiO_2 thickness of 10 nm/50 nm annealed for 2 h (open triangles in Fig. 3.28). This breakdown field is higher than that of N_2O-grown oxides (8.9 MV/cm). In the case of the n-MIS capacitors with thin-thermal oxides between deposited SiN_x/SiO_2 layers (10 nm/50 nm) and SiC, which were annealed in N_2O for 2 h (open circles in Fig. 3.28), the breakdown field is slightly decreased to 8.8 MV/cm. However, the deposited SiN_x/SiO_2 stack-gate structure with thin-thermal oxides is capable of enduring a high current density of about 10^{-3} A/cm^2. The deposited SiN_x/SiO_2 stack-gate structures, if adequately processed, exhibit good dielectric properties.

Figure 3.29 exhibits the relationship between the current density and effective insulator field of the n-MIS capacitors with thin-thermal oxides between SiN_x/SiO_2 (10 nm/50 nm) stack-gate structure and 4H-SiC $(000\bar{1})$, which were annealed in N_2O for 2 h. The deposited SiN_x/SiO_2 with thin-thermal oxides on $(000\bar{1})$ (open circles in Fig. 3.29) shows similar breakdown field (8.7 MV/cm) to the N_2O-grown oxides and the deposited SiN_x/SiO_2 with

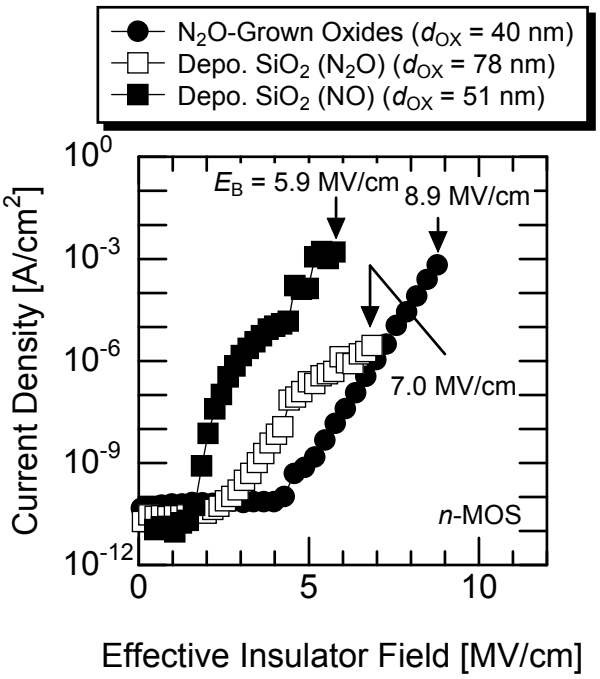


Figure 3.27: Relationship between the current density and effective insulator field of n-MOS capacitors. Close circles denote the characteristics of N_2O-grown oxides. Open and closed boxes depict those of deposited SiO_2 annealed in N_2O for 1 h and NO for 1 h, respectively.

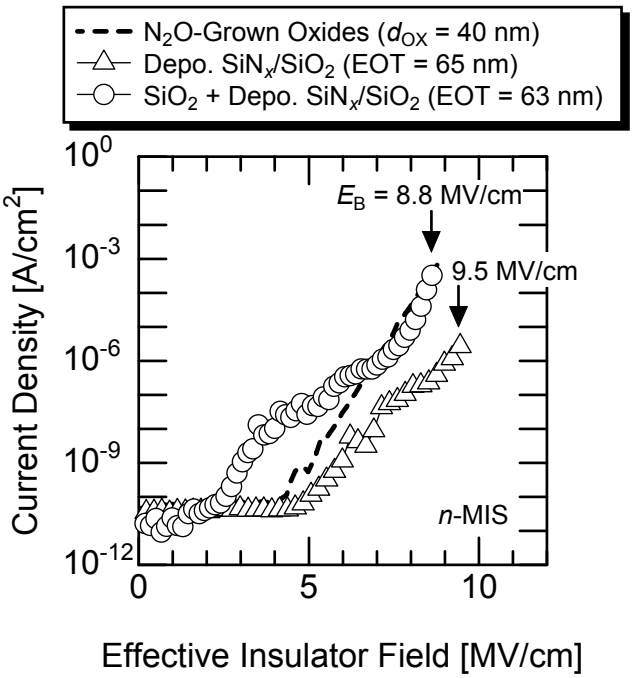


Figure 3.28: Relationship between the current density and effective insulator field of n-MIS capacitors. Open triangles mean the characteristics of the deposited SiN_x/SiO_2 (10 nm/50 nm) followed by N_2O annealing for 2 h. Open circles represent the characteristics of the deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h with thin-thermal oxides. The dashed line denotes those of N_2O-grown oxides.

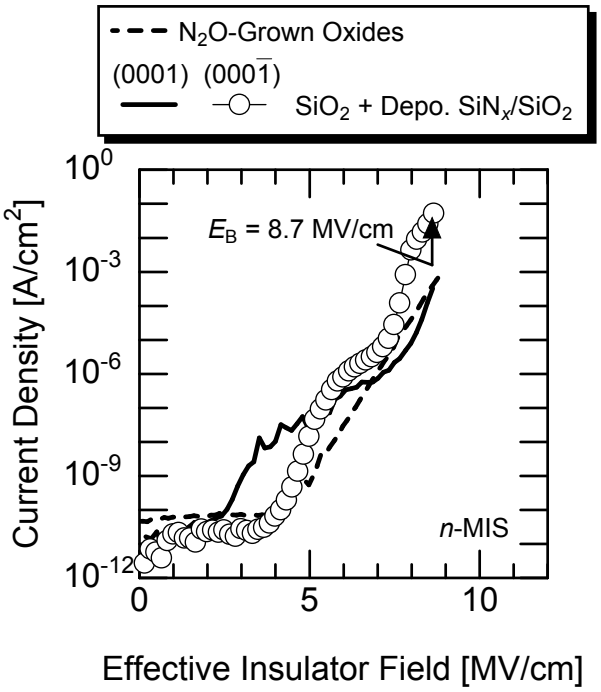


Figure 3.29: Relationship between the current density and effective insulator field of n-MIS capacitors. Open circles denote the characteristics of the deposited SiN_x/SiO_2 with thin-thermal oxides on the 4H-SiC (000$\bar{1}$)C face. The solid line means those of the deposited SiN_x/SiO_2 with thin-thermal oxides on the 4H-SiC (0001)Si face. The dashed line denotes N_2O-grown oxides.

thin-thermal oxides on (0001). The current density at the breakdown of the capacitors on the $(000\bar{1})$ is as high as $10^{-1}\,\mathrm{A/cm^2}$. The gate oxides on 4H-SiC $(000\bar{1})$ often show "leaky" characteristics, compared with those on 4H-SiC (0001), due to the smaller conduction band offset [26, 27]. However, in the case of stack-gate structure with thin-thermal oxides, the gate current density of n-MIS capacitors on the $(000\bar{1})$C face starts to rise when the effective insulator field reaches 4 MV/cm. This value is higher than that for n-MIS capacitors on the (0001)Si face. Although it is hard to estimate the exact value of the conduction band offset for the proposed structure, the deposited SiN_x/SiO_2 with thin-thermal oxides on the $(000\bar{1})$ face may be effective in improving the dielectric properties. By utilizing 4H-SiC $(000\bar{1})$, superior dielectric properties as well as superior interface properties can be realized.

P-Type MIS Capacitors

The I–V measurements were also performed for p-MIS capacitors. Figure 3.30 shows the current density-effective insulator field characteristics of p-MIS capacitors with various insulators. The N_2O-grown oxides (dashed line in Fig. 3.30) and the deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h with thin-thermal oxides (open circles in Fig. 3.30) have a breakdown field of over 7 MV/cm. In the case of the deposited SiO_2 annealed in N_2O (open boxes in Fig. 3.30), the leakage current is low and a breakdown field of 6.9 MV/cm is obtained. The fabricated p-MIS capacitors with N_2O-grown oxides and deposited insulators such as SiO_2 and SiN_x/SiO_2 exhibit moderate dielectric properties.

3.7.2 Reliability

From the standpoint of practical use, the long-term reliability of gate insulators is one of the most important factors. To investigate the reliability of the gate insulators, TDDB measurements were carried out at RT in the dark. The constant field stress was applied. Both n- and p-type MIS capacitors were biased into accumulation by applying positive and negative voltage stress to the gate, respectively. P-doped poly-Si was used as the gate electrode for the TDDB measurements. The area of gate electrode was $3.39 \times 10^{-4}\,\mathrm{cm^2}$.

N-Type MIS Capacitors

In the TDDB measurements, the time dependence of the current density at a fixed gate voltage was measured. The typical relationship between the current density and the measurement time for n-MOS capacitors with N_2O-grown oxides ($d_{\mathrm{OX}} = 61\,\mathrm{nm}$) is shown in Fig. 3.31. The stress voltage (V_{Stress}) was 54 V, and the stress field (E_{Stress}) becomes 8.9 MV/cm. The current density is gradually decreased with time. The electrons are injected to gate insulators from SiC, and the injected electrons are trapped at the defects inside the gate insulators. Since these electrons act as negative charges, the flatband voltage shifts toward the positive direction and the gate insulator field becomes progressively weaker, leading to decreased current. The sudden increase of current density is observed, when the

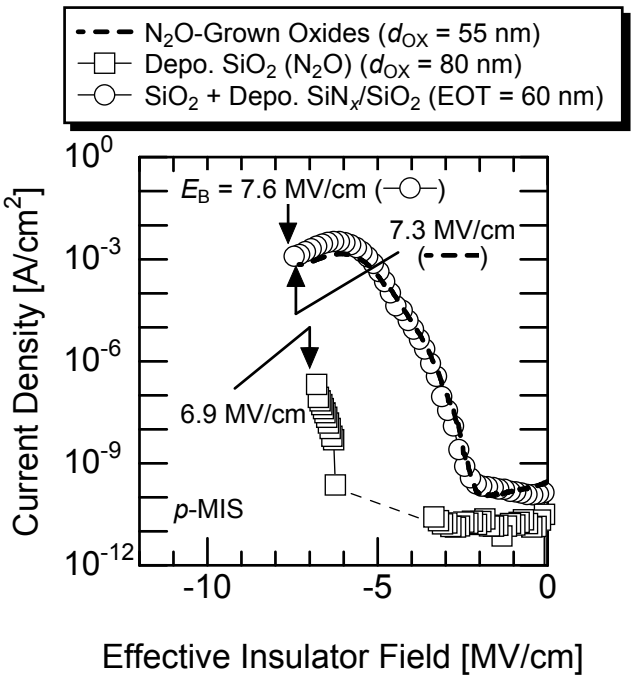


Figure 3.30: Relationship between the current density and effective insulator field of p-MIS capacitors. Open boxes denote the characteristics of the deposited SiO_2 annealed in N_2O for 1 h. Open circles mean those of the deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h with thin-thermal oxides. The dashed line denotes N_2O-grown oxides.

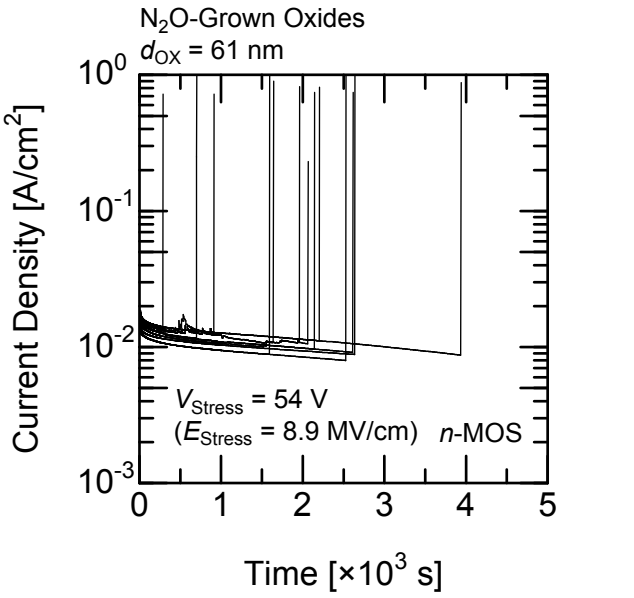


Figure 3.31: Time dependence of gate current density for n-MOS capacitors with N_2O-grown oxides. The stress voltage is 54 V, and the MOS interface is under accumulation condition. The gate electrode is P-doped poly-Si.

gate insulators are broken. The charge-to-breakdown (Q_{BD}) can be obtained by integrating the current, indicating the total amount of the injected charges before breakdown.

Figure 3.32 shows the Weibull plots[2] obtained from the TDDB measurements for various n-MIS capacitors. In Fig. 3.32, F means the cumulative failure rate. The distribution of the charge-to-breakdown can be divided into two region, gradual increase of failure rate in the small charge-to-breakdown region and rapid increase of failure rate in the high charge-to-breakdown region. In the former case, the capacitors show "B-mode" breakdown which indicates the random failure [28]. In the latter case, the capacitors show "C-mode" breakdown which indicates the intrinsic failure [28]. The fabricated capacitors exhibit both B- and C-mode breakdown. The charge-to-breakdown of N_2O-grown oxides on n-SiC at a cumulative failure of 63.2 % is estimated to be 27.5 C/cm^2. Compared with the n-MOS capacitors with N_2O-grown oxides, the n-MIS capacitors with deposited SiO_2 annealed in N_2O for 1 h exhibit a high charge-to-breakdown of 70.0 C/cm^2. On the other hand, the n-MIS capacitors with thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, followed by N_2O annealing for 2 h, show a low charge-to-breakdown of 2.0 C/cm^2. At present, it is hard to compare the charge-to-breakdown of these capacitors because the equivalent oxide thickness and stress field are different from each other. However, the deposited insulators tend to exhibit the high charge-to-breakdown. Although the relatively-low charge-to-breakdown was obtained in the n-MIS capacitors with thin-thermal oxides, the charge-to-breakdown is higher than that of dry O_2-grown oxides (a typical charge-to-breakdown of 0.01–1 C/cm^2 [13]).

P-Type MIS Capacitors

The TDDB measurements were conducted on the p-type MIS capacitors with various gate insulators. Unlike the n-MIS capacitors, the negative bias was applied to the gate electrodes.

Figure 3.33 depicts the Weibull plots for the p-MIS capacitors. As is the case for the n-MIS capacitors, the fabricated p-MIS capacitors exhibit B- and C-mode breakdown. The charge-to-breakdown of N_2O-grown oxides on p-SiC is 4.1 C/cm^2, which is lower than that on n-SiC. By utilizing the deposited SiO_2 annealed in N_2O for 2 h, the charge-to-breakdown is dramatically increased to 54.9 C/cm^2. On the other hand, the p-MIS capacitors with deposited SiN_x/SiO_2, of which thickness is 10 nm/50 nm, followed by N_2O annealing for 2 h on thin-thermal oxides indicate a low charge-to-breakdown of 1.1 C/cm^2 Although the correlation of charge-to-breakdown for p-MIS capacitors is similar to that for n-MIS capacitors, the absolute values of the charge-to-breakdown obtained in p-MIS capacitors is lower than those obtained in n-MIS capacitors. Other groups also reported that gate insulators such as oxide-nitride-oxide (ONO) stack structure and thermally-grown nitrided oxides on p-SiC show lower charge-to-breakdown, compared with n-MIS capacitors fabricated through the

[2]Weibull plots are explained in Appendix A.

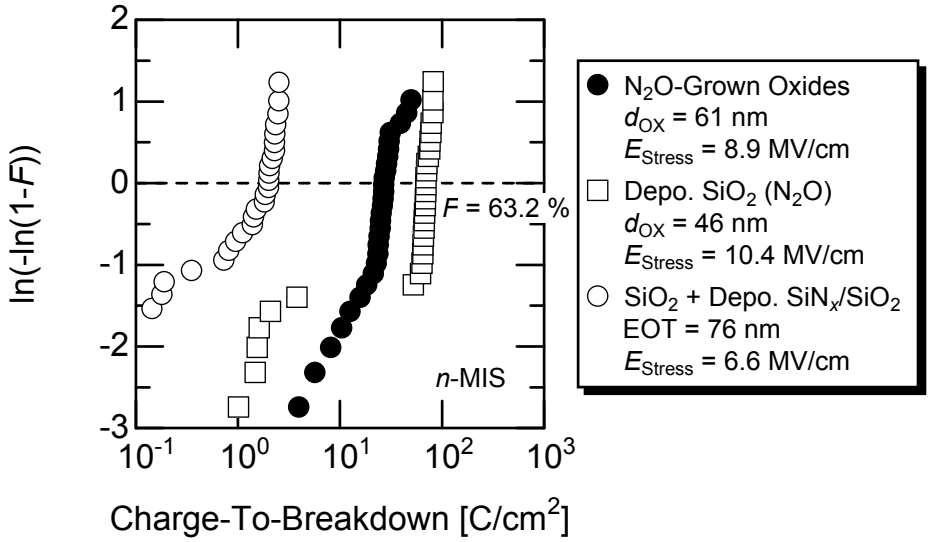


Figure 3.32: Weibull plots for n-MIS capacitors with various insulators. The horizontal axis denotes the charge-to-breakdown and the vertical axis the cumulative failure rate. Closed circles mean N_2O-grown oxides, open boxes deposited SiO_2 annealed in N_2O for 1 h, and open circles deposited SiN_x/SiO_2, of which thickness is 10 nm/50 nm, annealed in N_2O for 2 h with thin-thermal oxides formed before deposition.

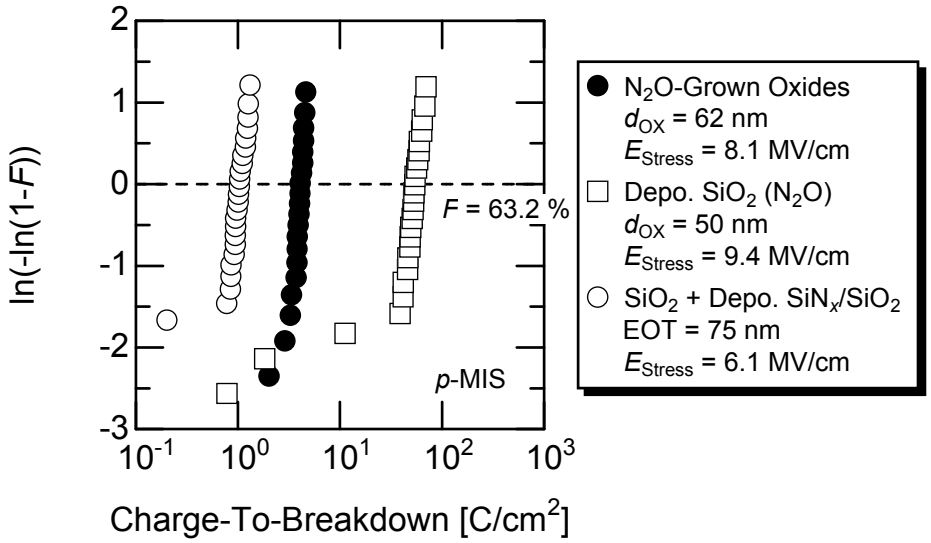


Figure 3.33: Weibull plots for p-MIS capacitors with various insulators. The horizontal axis denotes the charge-to-breakdown and the vertical axis the cumulative failure rate. Closed circles mean N_2O-grown oxides, open boxes deposited SiO_2 annealed in N_2O for 1 h, and open circles deposited SiN_x/SiO_2, of which thickness is 10 nm/50 nm, annealed in N_2O for 2 h with thin-thermal oxides formed before deposition.

same process as p-MIS capacitors [29, 30]. In the case of p-MIS capacitors, the deposited insulators also show superior characteristics to thermal oxides.

The deposited insulators adequately processed are effective to improve not only the interface properties but also the reliability of both n- and p-type SiC MIS devices.

3.8 Discussion

In this chapter, various dielectrics such as thermal oxides and deposited insulators were applied to the gate insulators of 4H-SiC MIS capacitors. The deposited insulators demonstrated advantages over the thermal oxides. The results obtained in n- and p-type MIS capacitors are summarized in Tables 3.2 and 3.3, respectively. In Tables 3.2 and 3.3, the effective fixed charge (Q_{eff}), the interface state density (D_{IT}), the breakdown field (E_{B}), and the charge-to-breakdown (Q_{BD}) are indicated. In Fig. 3.34, the distribution of the interface state density near the both conduction and valence band edges is shown. For comparison, the interface state density obtained from the characteristics of MOS capacitors with thermal oxides grown in dry O_2 ambient at 1300 °C [31] is also represented in Fig. 3.34. The deposited SiO_2 shows superior interface characteristics compared with N_2O-grown oxides although the breakdown field needs to be improved. The deposited SiN_x/SiO_2 adequately processed exhibits remarkable improvement in the interface properties while keeping moderate dielectric properties.

In the case of n-MOS capacitors, by utilizing the deposited SiO_2 annealed in N_2O or NO, the interface state density was decreased to below $1 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$. The deposited SiO_2 annealed in NO is effective in reducing interface state density although there is still room for improvement in the breakdown field. In the case of NO annealing, the generation of O_2 gas, which enhances oxidation during nitridation, can be suppressed, leading to lower interface state density. The n-MOS capacitors with deposited SiO_2 annealed in NO show the positive effective fixed charges in contrast to that annealed in N_2O. The effective fixed charge is the sum of real fixed charges (positive or negative) and negative charges trapped in the slow interface states. It is likely that the negative charges (electrons) trapped at the interface states compensate the positive charges located inside SiO_2 and/or at the SiO_2/SiC interface. The MOS capacitors with deposited SiO_2 annealed in NO exhibit low interface state density, and the negative charges captured at the interface states are negligible. As a result, the positive effective fixed charge was observed in the n-MOS capacitors with deposited SiO_2 annealed in NO, and the real fixed charges inside SiO_2 annealed in NO may be positive. The deposited SiO_2 annealed in N_2O was also applied to the gate insulators of p-type MOS capacitors. In the p-MOS capacitors, the deposited SiO_2 annealed in N_2O shows lower interface state density than N_2O-grown oxides. The deposited SiO_2 is an attractive insulator to decrease the interface state density near the conduction and valence band edges.

The deposited SiO_2 formed with SiH_4 and N_2O shows similar interface properties to the

Table 3.2: Interface and dielectric properties of n-type MIS capacitors with various gate insulators.

N-Type 4H-SiC (0001) Face				
Gate Insulators	Q_{eff} [cm^{-2}]	D_{IT} @ $E_{\mathrm{C}} - 0.2\,\mathrm{eV}$ [$\mathrm{cm}^{-2}\mathrm{eV}^{-1}$]	E_{B} [MV/cm]	Q_{BD} [$\mathrm{C/cm}^2$]
N_2O-Grown Oxides	-1.1×10^{12}	2×10^{12}	8.9	27.5
Depo. SiO_2 (N_2O)[1)]	-2.2×10^{11}	7×10^{11}	7.0	70.0
Depo. SiO_2 (NO)[2)]	7.4×10^{11}	3×10^{11}	5.9	—
Depo. SiN_x/SiO_2 [3)]	$> 3 \times 10^{12}$	$< 1 \times 10^{11}$	9.5	—
SiO_2 + Depo. SiN_x/SiO_2 [4)]	$< 5 \times 10^{11}$	2×10^{11}	8.8	2.0

N-Type 4H-SiC (000$\bar{1}$) Face				
Gate Insulators	Q_{eff} [cm^{-2}]	D_{IT} @ $E_{\mathrm{C}} - 0.2\,\mathrm{eV}$ [$\mathrm{cm}^{-2}\mathrm{eV}^{-1}$]	E_{B} [MV/cm]	Q_{BD} [$\mathrm{C/cm}^2$]
SiO_2 + Depo. SiN_x/SiO_2 [5)]	$< 1 \times 10^{11}$	$< 1 \times 10^{11}$	8.7	—

1) Deposited SiO_2 annealed in N_2O for 1 h ($d_{\mathrm{OX}} = 46$–78 nm).
2) Deposited SiO_2 annealed in NO for 1 h ($d_{\mathrm{OX}} = 51$ nm).
3) Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.
4) Oxidation in N_2O for 5 min + Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.
5) Oxidation in N_2O for 3 min + Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.

Table 3.3: Interface and dielectric properties of *p*-type MIS capacitors with various gate insulators.

P-Type 4H-SiC (0001) Face				
Gate Insulators	Q_{eff} [$\mathrm{cm^{-2}}$]	D_{IT} @ $E_{\mathrm{V}}+0.2\,\mathrm{eV}$ [$\mathrm{cm^{-2}eV^{-1}}$]	E_{B} [MV/cm]	Q_{BD} [$\mathrm{C/cm^2}$]
N_2O-Grown Oxides	2.4×10^{12}	9×10^{11}	7.3	4.1
Depo. SiO_2 (N_2O)[1)]	1.5×10^{12}	5×10^{11}	6.9	54.9
SiO_2 + Depo. SiN_x/SiO_2 [2)]	2.4×10^{12}	6×10^{11}	7.6	1.1

1) Deposited SiO_2 annealed in N_2O for 1 h (d_{OX} = 50–80 nm).
2) Oxidation in N_2O for 5 min + Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.

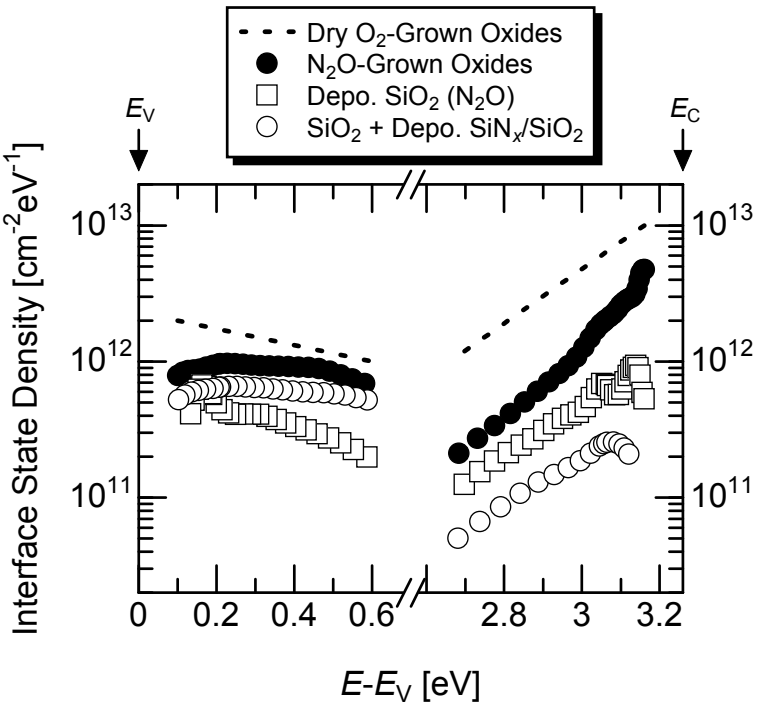


Figure 3.34: Interface state density near the valence and conduction band edges. Closed circles mean the N_2O-grown oxides, open boxes the deposited SiO_2 annealed in N_2O for 1 h, and open circles the deposited SiN_x/SiO_2, of which thickness is 10 nm/50 nm, annealed in N_2O for 2 h with thin-thermal oxides formed before deposition. The dashed line denotes the dry O_2-grown oxides as a reference [31].

deposited SiO_2 formed with TEOS and O_2 [22]. The major difference between these oxides is the concentration of carbon atoms inside SiO_2. In the case of deposited SiO_2, however, the SiO_2/SiC interface properties are influenced by the SiO_2 grown during N_2O annealing, while the SiO_2 grown during annealing displays similar features. As a result, the similar interface characteristics can be obtained in these oxides. The observed difference between these oxides is the breakdown field, which is affected by the quality of deposited SiO_2 itself. The deposited SiO_2 formed with TEOS and O_2 shows a breakdown field of over 10 MV/cm and low leakage current [22]. Regarding the deposited SiO_2 formed with SiH_4 and N_2O, the optimization of deposition and N_2 POA condition are required.

In the case of deposited SiN_x/SiO_2, the interface state density was decreased by thinning SiN_x layer and/or extending N_2O-annealing time. When the SiN_x layer is completely oxidized and converted to an SiO_xN_y layer, the interface state density was dramatically decreased to below $1 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$. The SiO_xN_y layer directly deposited on SiC by PECVD, followed by NO annealing, has been already investigated for the gate insulators of 4H-SiC MOS devices [32]. Compared with the previous report, the interface characteristics were significantly improved in the MIS capacitors fabricated in this study. For this reason, it is important that the SiO_xN_y layer is formed by oxidizing the SiN_x layer.

In this study, the deposited SiO_2 and SiN_x/SiO_2 structures were formed by using PECVD although these insulators can be deposited by using thermal CVD. In general, the SiO_2 deposited by thermal CVD shows higher density (less porosity) than the SiO_2 deposited by PECVD. To improve the dielectric properties of deposited SiO_2, the thermal CVD may be one of the most effective methods.

By utilizing thin-thermal oxides in addition to the deposited SiN_x/SiO_2, superior characteristics could be obtained. In this study, the thickness of thin-thermal oxides was 4 nm and was not optimized. In the case of deposited Al_2O_3, the interface properties are improved when the thickness of thermal oxides between Al_2O_3 and SiC is thinner than 1.3 nm [33]. By optimizing the thickness of thin-thermal oxides, it may be possible for the interface properties to be further improved.

In terms of reliability, high Q_{BD} values can be obtained in the deposited SiO_2 annealed in N_2O on both n- and p-type SiC. On the other hand, the deposited SiN_x/SiO_2 with thin-thermal oxides shows small Q_{BD}. The high Q_{BD} values of deposited SiO_2 agree with the previous reports [13–15]. The lifetime of the gate insulators (τ_{i}) under an effective insulator field of 3 MV/cm is roughly evaluated from the charge-to-breakdown by using the following equation:

$$\tau_{\mathrm{i}} = \frac{Q_{\mathrm{BD}}}{J_{\mathrm{G,leak}}}, \tag{3.4}$$

where $J_{\mathrm{G,leak}}$ is the gate leakage current density. For the n-MIS capacitors, the estimated lifetime of the N_2O-grown oxides, the deposited SiO_2 annealed in N_2O, and the deposited SiN_x/SiO_2 with thin-thermal oxides is 12000 years, 11000 years, and 63 years, respectively. In this calculation, the gate leakage current was assumed to be $7 \times 10^{-11}\,\mathrm{A/cm^2}$,

2×10^{-10} A/cm^2, and 1×10^{-9} A/cm^2 for the N_2O-grown oxides, the deposited SiO_2 annealed in N_2O, and the deposited SiN_x/SiO_2 with thin-thermal oxides, respectively, which are determined as the gate leakage current density at an effective insulator field of 3 MV/cm as shown in Figs. 3.27 and 3.28. For the p-MIS capacitors, the lifetime at 3 MV/cm was estimated to be 1 year for the N_2O-grown oxides, 87000 years for the deposited SiO_2 annealed in N_2O, and 0.6 years for the deposited SiN_x/SiO_2 with thin-thermal oxides. The deposited SiO_2 annealed in N_2O exhibits longer lifetime for both n- and p-MIS capacitors, compared with other insulators. Although the N_2O-grown oxides also show a lifetime of over 10000 years in n-MOS capacitors, the lifetime is shortened in p-MOS capacitors. In the case of the deposited SiN_x/SiO_2 with thin-thermal oxides, the reliability should be improved through optimizing the formation process of gate insulators such as the thickness of thin-thermal oxides, the deposition condition of SiN_x, and the N_2 POA condition. The electric field dependence of charge-to-breakdown needs to be measured to estimate the accurate lifetime of the gate insulators. The reliability of gate insulators at high temperature is the key issue to put the SiC MIS devices into practical use. The TDDB measurements at high temperature should be performed for further understanding of the reliability. The MIS capacitors with thin thermal oxides fabricated on $(000\bar{1})$ exhibit exceptional interface characteristics in addition to moderate breakdown field. Although the TDDB measurements have not been conducted on the $(000\bar{1})$ MIS capacitors with thin-thermal oxides between SiN_x/SiO_2 and SiC, the deposited SiN_x/SiO_2 adequately processed on 4H-SiC $(000\bar{1})$ may be one of the best solutions for the problems of the inferior interface and dielectric properties in 4H-SiC MIS devices.

3.9 Summary

The deposited SiO_2 and SiN_x/SiO_2 were applied to the gate insulators of SiC MIS devices and compared to thermal oxides grown in N_2O.

In the case of N_2O-grown oxides, the interface state density was 2×10^{12} cm^{-2}eV^{-1} at an energy depth of 0.2 eV from the conduction band edge and the effective fixed charge density was -1.1×10^{12} cm^{-2}. From the characteristics of p-MOS capacitors, the interface state density near the valence band edge was 9×10^{11} cm^{-2}eV^{-1}. The charge-to-breakdown are 27.5 C/cm^2 and 4.1 C/cm^2 for n- and p-MOS capacitors, respectively.

In the case of deposited SiO_2, the interface state density was decreased by N_2O annealing, compared with N_2 annealing. An interface state density of 7×10^{11} cm^{-2}eV^{-1} could be achieved when the increment of oxide thickness during N_2O annealing becomes 3 nm. The NO annealing was also effective in reducing the interface state density near the conduction band edge. The interface state density near the valence band edge was also estimated to be 5×10^{11} cm^{-2}eV^{-1} by using p-MOS capacitors with deposited SiO_2 annealed in N_2O. The deposited SiO_2 annealed in N_2O is effective to reduce the interface state density not only near

the conduction band edge but also near the valence band edge. In addition, the deposited SiO_2 annealed in N_2O demonstrated a high charge-to-breakdown of over $50\,C/cm^2$, which is more than 10 times higher than that of dry O_2-grown oxides.

In the case of deposited SiN_x/SiO_2 stack-gate structures, the interface properties were improved by thinning initial-SiN_x layer and/or extending the N_2O-annealing time. From the SIMS measurements, it was found that a portion of SiN_x layer was oxidized during N_2O annealing and converted to an SiO_xN_y layer. The influence of traps inside the SiN_x layer may be reduced and the improvement in interface properties could be realized. The stack-gate structure with an SiN_x/SiO_2 thickness of 10 nm/50 nm annealed in N_2O for 2 h exhibited a low interface state density below $1 \times 10^{11}\,cm^{-2}eV^{-1}$. However, the MIS capacitors annealed for 2 h showed a large negative shift of flatband voltage, which indicates that a large number of positive charges are located at the interface. To reduce the positive charges at the interface, thin-thermal oxides were grown before deposition of SiN_x/SiO_2 stack-gate structure. As a result, the negative shift of flatband voltage disappeared and an interface state density of $2 \times 10^{11}\,cm^{-2}eV^{-1}$ could be obtained, which is one-tenth of that obtained in the MOS capacitors with N_2O-grown oxides. The moderate breakdown filed could be observed in the both n- and p-type MIS capacitors with thin-thermal oxides although the charge-to-breakdown is still low.

For further improvements of interface properties, the stack-gate structure was deposited on the 4H-SiC $(000\bar{1})$C substrates. In the MIS capacitors with thin-thermal oxides between deposited SiN_x/SiO_2 stack-gate structure and 4H-SiC $(000\bar{1})$, the measured C–V curves were nearly identical to the theoretical C–V curve. The interface state density was decreased to below $1 \times 10^{11}\,cm^{-2}eV^{-1}$, which indicates that the 4H-SiC $(000\bar{1})$C face is an attractive crystal face to improve the interface properties. The n-MIS capacitors with thin-thermal oxides on 4H-SiC $(000\bar{1})$ also exhibited reasonable breakdown field.

The deposited SiO_2 and SiN_x/SiO_2 stack-gate structures exhibited superior interface and dielectric properties to the N_2O-grown oxides when these insulators were adequately processed. The characteristics of MISFETs with these insulators are presented in the next chapter.

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Chapter 4

N- and *P*-Channel SiC MISFETs with Thermally-Grown and Deposited Insulators

4.1 Introduction

4H-SiC has superior physical and chemical properties [1] and hence 4H-SiC metal-insulator-semiconductor field-effect transistors (MISFETs) have been regarded as candidates for high-power devices [2] and components of high-temperature integrated circuits (ICs).

In terms of n-channel MIS devices, the n-channel mobility is the most critical factor which limits the performance of SiC power devices. Although several groups have reported 4H-SiC power MISFETs which outperform Si power devices, there is still room for improvement in the channel mobility. In addition, in the case of p-channel MIS devices, a systematic study has been lacking so far, although several groups have reported the p-channel metal-oxide-semiconductor FETs (MOSFETs) on the 4H-SiC (0001) face [3–5]. The SiC p-channel MISFETs are the key component of the p-channel insulated gate bipolar transistors (IGBTs) [6–9] for ultra high-voltage ($> 5\,\mathrm{kV}$) devices as well as complementally MOS (CMOS) circuits [10] for power ICs. Thus, investigations on SiC p-channel MIS devices are strongly required.

Although the increase in the channel mobility has been a major concern in the field of SiC MIS devices, characterization of interface properties should also play an important role. In the case of wide bandgap semiconductors, it is difficult to characterize the interface properties near the minority-carrier band edge by using MIS capacitors due to its extremely long time constant to generate minority carriers. Therefore, a method to estimate the interface state density near the minority-carrier band edge in wide bandgap semiconductors can be put forward.

For the reasons mentioned above, studies on both n- and p-channel SiC MISFETs have been important for the further improvement of SiC power devices and circuits. As discussed

in Chapter 3, the deposited films such as SiO_2 and SiN_x/SiO_2, if adequately processed, are attractive insulators for the n- and p-channel MIS devices due to superior interface and dielectric properties. In this chapter, these insulators were applied to the n- and p-channel 4H-SiC MISFETs. The improved channel mobilities of both n- and p-channel devices are obtained by utilizing deposited insulators such as SiO_2 and SiN_x/SiO_2. The correlation between the channel mobility and the crystal face orientation was also investigated. In addition, the method to evaluate the interface state density near the minority-carrier band edge by using gate-controlled diodes is proposed.

4.2 Device Fabrication

4.2.1 Fabrication Process of Planar MISFETs

For n-channel MISFET fabrication, 8° off-axis p-type 4H-SiC (0001) epilayers with an acceptor concentration of 3–8 × 10^{15} cm^{-3} were employed. N-channel MISFETs were also fabricated on 8° off-axis p-type 4H-SiC $(000\bar{1})$ epilayers with an acceptor concentration of 6–8 × 10^{15} cm^{-3}. The source/drain regions were formed by high-dose P^+ implantation (energy: 10–110 keV, total dose: 5 × 10^{15} cm^{-2}) at 300 °C. After ion implantation, high-temperature annealing was performed at 1600 °C for 15 min in Ar with a carbon cap to suppress surface roughening [11]. The formation process of gate insulators is explained in the next subsection. The source/drain and substrate contacts were formed by thermal evaporation of Al and Ti/Al, respectively, and these contacts were alloyed at 600 °C for 10 min. The gate electrode was Al.

The p-channel MISFETs were fabricated on n-type 4H-SiC 8° off-axis (0001), 8° off-axis $(000\bar{1})$, on-axis $(03\bar{3}8)$, and on-axis $(11\bar{2}0)$ epilayers. The donor concentration of the n-type epilayers estimated from capacitance-voltage measurements was 1 × 10^{16} cm^{-3} for (0001), 1–3 × 10^{15} cm^{-3} for $(000\bar{1})$, 2–5 × 10^{16} cm^{-3} for $(03\bar{3}8)$, and 5–8 × 10^{14} cm^{-3} for $(11\bar{2}0)$. The 0.3 μm-deep source/drain regions were formed by high-dose Al^+ implantation (energy: 10–160 keV, total dose: 5 × 10^{15} cm^{-2}) at 300 °C. After ion implantation, thermal annealing was carried out at 1700 °C for 20 min with a carbon cap [11]. The formation processes of gate insulators are described in the next subsection. The source/drain and substrate electrodes were Ti/Al/Ni and Ni, respectively, and these electrodes were annealed at 950 °C for 5 min. The gate electrode was Al.

The typical channel length (L_{Ch}) and width (W) were 25–100 μm and 200 μm, respectively. The design of long-channel MISFETs was adopted to suppress the short-channel effects discussed in Chapter 2 and to estimate accurate channel mobilities.

4.2.2 Formation Process of Gate Insulators

The thermal SiO_2 grown in N_2O, the deposited SiO_2, and the deposited SiN_x/SiO_2 layers, which were explored in Chapter 3, were applied to the gate insulators of SiC MISFETs.

N-Channel MISFETs

The formation process of thermal SiO_2 grown in N_2O is the same as that introduced in Section 3.3.1 except for the oxidation time. For *n*-channel MOSFETs, the N_2O-oxidation time was 15 h for the (0001) face and 4 h for the $(000\bar{1})$ face. The gate oxide thickness (d_{OX}) was 83 nm for (0001) and 80 nm for $(000\bar{1})$.

SiO_2 was also formed by using plasma-enhanced chemical vapor deposition (PECVD) and annealed in N_2O for 1 h and 2 h for the (0001) and $(000\bar{1})$ faces, respectively, as described in Section 3.4.1. The thickness of deposited SiO_2 after N_2O annealing was 88 nm for (0001) and 102 nm for $(000\bar{1})$. The increment of oxide thickness during N_2O annealing (Δd_{OX}) was 5 nm for (0001) and 17 nm for $(000\bar{1})$. The deposited SiO_2 film (about 70 nm) annealed in NO for 2 h was also utilized as the gate oxides.

The SiN_x/SiO_2 stack-gate structure was formed by using PECVD as mentioned in Section 3.5.1. The initial thickness of deposited SiN_x/SiO_2 was 10 nm/50 nm. The deposited SiN_x/SiO_2 was annealed in N_2O (10 % diluted in N_2) for 2 h. In addition to the SiN_x/SiO_2 stack-gate structure, the thin-$SiO_2/SiN_x/SiO_2$ stack-gate structure was also applied to the *n*-channel SiC MISFETs. The thin-thermal oxides were grown in N_2O (10 % diluted in N_2) for 5 min and 3 min for the (0001) and $(000\bar{1})$ faces, respectively. After the formation of thin-thermal oxides, the SiN_x/SiO_2 films were deposited. The thickness of SiN_x/SiO_2 layer was 10 nm/50 nm and the N_2O-annealing time was 2 h.

P-Channel MISFETs

The formation process of N_2O-grown oxides is the same as that introduced in Section 3.3.1 except for the oxidation time. For *p*-channel MOSFETs, the oxidation time was 7 h for the (0001) face and 3 h for other faces. The thickness of N_2O-grown oxides was about 50 nm. For comparison, thermal oxides grown in dry O_2 at 1150 °C for 3 h were also utilized as the gate oxides of *p*-channel MISFETs ($d_{OX} = 72$ nm).

The deposited SiO_2 was formed by using PECVD. After the deposition, the SiO_2 layer was annealed in N_2O. The thickness of deposited SiO_2 was about 50 nm and the N_2O-annealing time was 30 min.

MISFETs with thin-thermal oxides between SiN_x/SiO_2 and SiC were also fabricated on (0001). The thin-thermal oxides were grown in N_2O (10 % diluted in N_2) for 5 min. The thickness of deposited SiN_x/SiO_2 was 10 nm/50 nm and the N_2O-annealing time was 2 h.

Tables 4.1 and 4.2 summarizes the equivalent oxide thickness (EOT) of the *n*- and *p*-channel MISFETs, respectively.

Table 4.1: EOT for *n*-channel MISFETs.

Gate Insulators	Face	
	(0001)	$(000\bar{1})$
N_2O-Grown Oxides	83 nm	80 nm
Depo. SiO_2 (N_2O)[1)]	88 nm	102 nm
Depo. SiO_2 (NO)[2)]	70 nm	79 nm
Depo. SiN_x/SiO_2 [3)]	60 nm	59 nm
SiO_2 + Depo. SiN_x/SiO_2 [4)]	68 nm	66 nm

1) Deposited SiO_2 ($\sim$ 85 nm) annealed in N_2O for 1–2 h.
2) Deposited SiO_2 ($\sim$ 70 nm) annealed in NO for 2 h.
3) Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.
4) Oxidation in N_2O for 5 min for 4H-SiC (0001) and for 3 min for 4H-SiC $(000\bar{1})$ + Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.

Table 4.2: EOT for *p*-channel MISFETs.

Gate Insulators	Face			
	(0001)	$(000\bar{1})$	$(03\bar{3}8)$	$(11\bar{2}0)$
Dry O_2-Grown Oxides	72 nm	—	—	—
N_2O-Grown Oxides	49 nm	63 nm	44 nm	52 nm
Depo. SiO_2 (N_2O)[1)]	47 nm	51 nm	50 nm	48 nm
SiO_2 + Depo. SiN_x/SiO_2 [2)]	61 nm	—	—	—

1) Deposited SiO_2 ($\sim$ 50 nm) annealed in N_2O for 30 min.
2) Oxidation in N_2O for 5 min + Deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h.

4.3 *N*-Channel MISFETs

4.3.1 MISFET Characteristics

To compare the MISFETs with various structures, the drain current (I_D) in the gate characteristics (drain current (I_D)-gate voltage (V_G) characteristics) was normalized by channel length (L_{Ch}), channel width (W), and insulator capacitance per unit area (C_i).

N_2O-Grown Oxides

Figure 4.1 shows the subthreshold ($\log I_D$-V_G) and gate characteristics of n-channel MOSFETs with N_2O-grown oxides fabricated on the 4H-SiC (0001) and (000$\bar{1}$) faces in the linear region (a drain voltage (V_D) of 0.1 V). Compared with the MOSFETs on the (0001) face (closed circles in Fig. 4.1), the MOSFETs on the (000$\bar{1}$) face exhibit high drain current (open circles in Fig. 4.1), which indicates high channel mobility in the (000$\bar{1}$) MOSFETs. The threshold voltage (V_T) of the (0001) MOSFET, which is obtained from the extrapolation of the gate characteristics, is higher than that of the (000$\bar{1}$) MOSFET, 7.4 V for (0001) and 4.6 V for (000$\bar{1}$). The effective fixed charge density can be calculated by using the following equation:

$$Q_{\text{eff}} = \frac{C_i(V_{T,\text{theory}} - V_T)}{e}, \tag{4.1}$$

where $V_{T,\text{theory}}$ is the theoretical threshold voltage and e the elementary charge. The calculated density of effective fixed charges is $-1.4 \times 10^{12}\,\text{cm}^{-2}$ for the (0001) face and $-7.0 \times 10^{11}\,\text{cm}^{-2}$ for the (000$\bar{1}$) face. The reduced density of effective fixed charges was obtained in the (000$\bar{1}$) MOSFET. In the subthreshold characteristics, the subthreshold swing (S) is also different from each other (413 mV/decade for the (0001) face and 214 mV/decade for the (000$\bar{1}$) face). A steep slope is observed in the (000$\bar{1}$) MOSFET. The subthreshold swing is affected by the interface states in the relatively deep energy region, and the interface state density (D_{IT}) can be estimated from the difference between theoretical and experimental subthreshold swings [12]. The theoretical subthreshold swing (S_{theory}) can be expressed as:

$$S_{\text{theory}} = \frac{kT}{e} \ln 10 \left(1 + \frac{C_D}{C_i}\right), \tag{4.2}$$

where k is the Boltzmann constant, T the absolute temperature, and C_D the capacitance of the depletion layer extended beneath the gate electrode. On the other hand, the experimental subthreshold swing can be described as:

$$S = \frac{kT}{e} \ln 10 \left(1 + \frac{C_D + C_{IT}}{C_i}\right), \tag{4.3}$$

where C_{IT} is the capacitance associated with the interface state, which is equal to eD_{IT}. Therefore, the interface state density is obtained as:

$$D_{IT} = \frac{C_i + C_D}{e} \left(\frac{S}{S_{\text{theory}}} - 1\right). \tag{4.4}$$

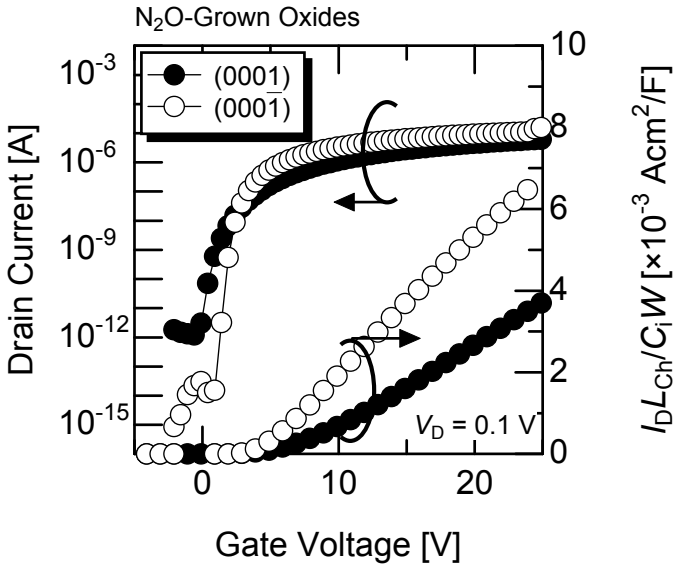


Figure 4.1: Subthreshold and gate characteristics of n-channel MOSFETs with N_2O-grown oxides. Closed circles denote MOSFET on the 4H-SiC (0001) face and open circles MOSFET on the 4H-SiC (000$\bar{1}$) face.

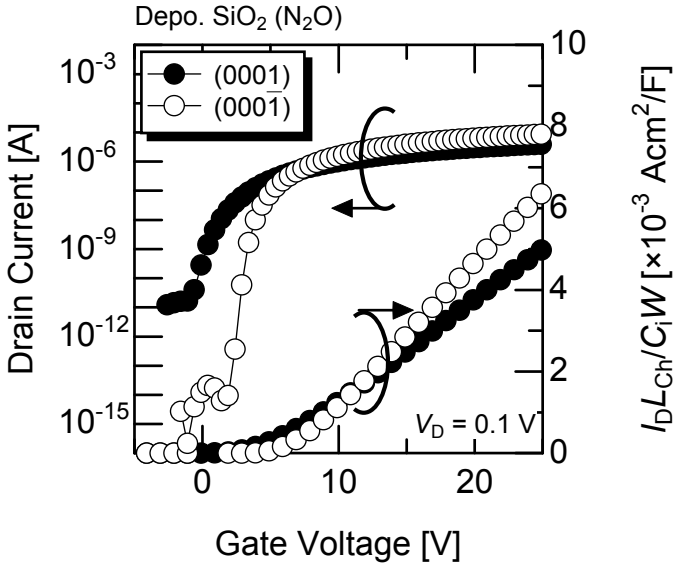
The calculated density of interface states is $1.3 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$ and $4.2 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$ for the (0001) and (000$\bar{1}$) MOSFETs, respectively. Due to its low interface state density, the (000$\bar{1}$) MOSFETs with N_2O-grown oxides show superior characteristics to the (0001) MOSFETs.

Deposited SiO_2

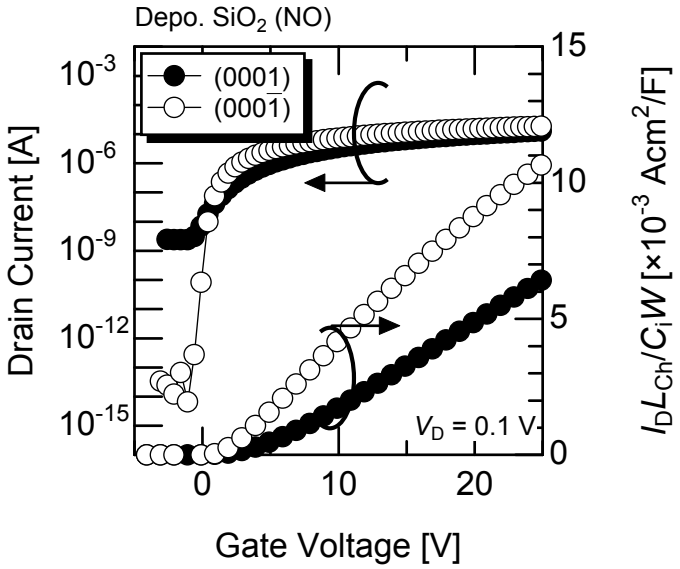
Figure 4.2 shows the subthreshold and gate characteristics of 4H-SiC *n*-channel MOSFETs with deposited oxides annealed in (a) N_2O and (b) NO. In the figure, closed and open circles denote the characteristics of MOSFETs on the (0001) and (000$\bar{1}$) faces, respectively. As is the case for the MOSFETs with N_2O-grown oxides, the (000$\bar{1}$) MOSFETs with deposited SiO_2 exhibit high drain current. The MOSFETs with deposited SiO_2 annealed in N_2O show a threshold voltage of 5.3 V for (0001) face and 7.1 V for (000$\bar{1}$) face. Compared with N_2O-grown oxides, a lower threshold voltage is observed in the (0001) MOSFETs with deposited SiO_2 annealed in N_2O, which indicates the decreased density of effective fixed charges. On the other hand, the threshold voltage of the (000$\bar{1}$) MOSFETs is similar to that of the (000$\bar{1}$) MOSFETs with N_2O-grown oxides. This result may be attributed to the large increment of oxide thickness during N_2O annealing (17 nm), and the interface structure has become similar to that with N_2O-grown oxides. In the case of deposited SiO_2 annealed in NO (Fig. 4.2 (b)), superior characteristics are obtained in both (0001) and (000$\bar{1}$) MOSFETs. The MOSFET on the (0001) face shows a threshold voltage of 4.6 V. Threshold voltage in the MOSFETs fabricated on the (000$\bar{1}$) face is 1.9 V. In the MOSFETs on (000$\bar{1}$), the experimental threshold voltage is almost the same as the theoretical threshold voltage (1.8 V), which means low effective fixed charge density at the deposited SiO_2/(000$\bar{1}$) interface annealed in NO. The effective fixed charge density was calculated to be as low as $-4.2 \times 10^{10}\,\mathrm{cm^{-2}}$ in the (000$\bar{1}$) MOSFETs with deposited SiO_2 annealed in NO. The (000$\bar{1}$) MOSFETs with deposited SiO_2 annealed in NO also exhibit a steep slope in the subthreshold characteristics (a subthreshold swing of 173 mV/decade). In the (0001) MOSFETs, however, the accurate subthreshold swing could not be estimated due to its large OFF current at a negative gate voltage. A low interface state density of $7.1 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$ and $4.5 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$ for the deposited SiO_2 annealed in N_2O and NO on (000$\bar{1}$), respectively, is obtained from the subthreshold swings.

Deposited SiN_x/SiO_2

Subthreshold and gate characteristics of MISFETs with deposited SiN_x/SiO_2 stack-gate structures are shown in Fig. 4.3. Again, in the figure, closed and open circles denote the characteristics of MOSFETs on the (0001) and (000$\bar{1}$) faces, respectively. In Fig. 4.3 (a), the MISFETs have deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h. The MISFETs shown in Fig. 4.3 (b) have thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, annealed in N_2O for 2 h. In the case of SiN_x/SiO_2 without thin-thermal oxides (Fig. 4.3 (a)), the (0001) MISFET shows higher drain current than the (000$\bar{1}$)

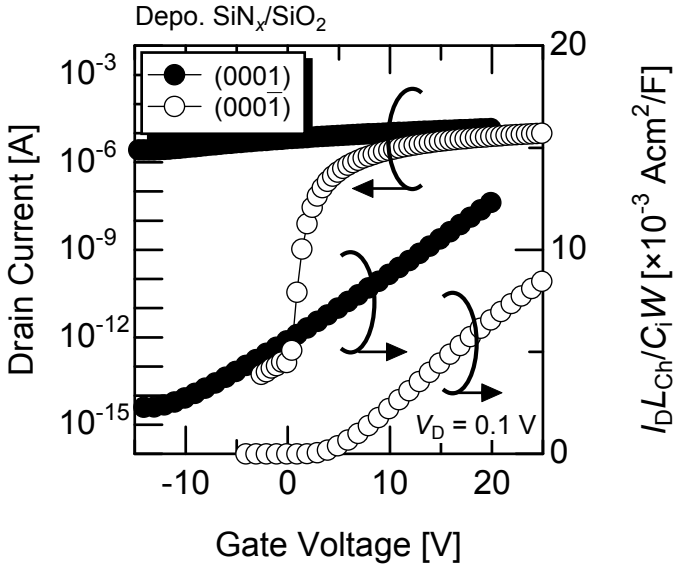


(a)

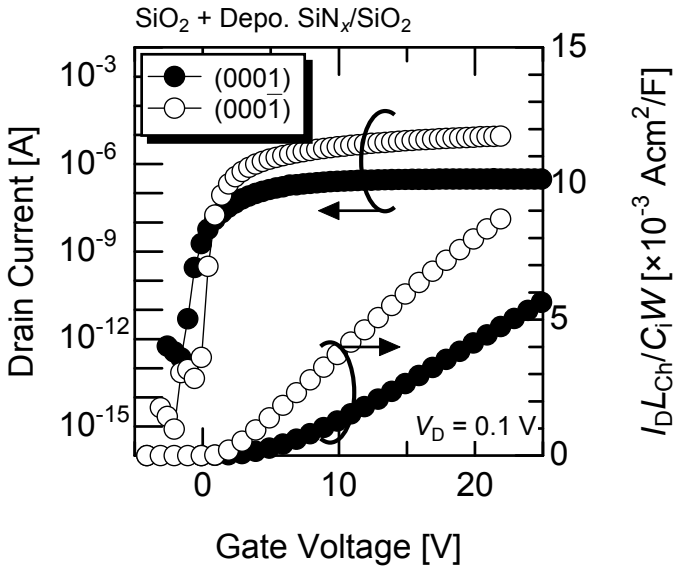


(b)

Figure 4.2: Subthreshold and gate characteristics of n-channel MOSFETs with (a) deposited SiO_2 annealed in N_2O and (b) deposited SiO_2 annealed in NO. Closed circles denote MOSFETs on the 4H-SiC (0001) face and open circles MOSFETs on the 4H-SiC (000$\bar{1}$) face.



(a)



(b)

Figure 4.3: Subthreshold and gate characteristics of n-channel MISFETs with (a) deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h and (b) thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, which were annealed in N_2O for 2 h. Closed circles denote MISFETs on the 4H-SiC (0001) face and open circles MISFETs on the 4H-SiC (000$\bar{1}$) face.

MISFET although the drain current can not be shut off even at negative gate voltage. The (0001) MISFET with deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h shows a considerably shifted threshold voltage of −15 V, which agrees with the large negative shift of the flatband voltage obtained in the MIS capacitor shown in Figure 3.17 (b). On the other hand, the MISFET with deposited SiN_x/SiO_2 on the $(000\bar{1})$ face exhibits a normally-OFF characteristics with a threshold voltage of 5.0 V. In the case of SiN_x/SiO_2 with thin-thermal oxides, the (0001) MISFET shows a positive threshold voltage of 6.2 V and can shut off the drain current in contrast to that without thin-thermal oxides. The insertion of thin-thermal oxides between deposited SiN_x/SiO_2 and SiC is effective to suppress the generation of positive charges at the MIS interface as discussed for the n-MIS capacitors. The $(000\bar{1})$ MISFETs with thin-thermal oxides show a low threshold voltage of 2.0 V and high drain current. The calculated density of effective fixed charges is $-1.4 \times 10^{12}\,\mathrm{cm}^{-2}$ for the (0001) face and $-1.0 \times 10^{11}\,\mathrm{cm}^{-2}$ for the $(000\bar{1})$ face. The $(000\bar{1})$ MISFET shows a small subthreshold swing of 137 mV/decade. The MISFETs with thin-thermal oxides on $(000\bar{1})$ exhibit superior characteristics to those on (0001).

Tables 4.3 and 4.4 summarize the experimental and theoretical threshold voltages (V_T and $V_{T,theory}$, respectively), the effective fixed charge density (Q_{eff}), experimental and theoretical subthreshold swings (S and S_{theory}, respectively), and the interface state density (D_{IT}). From Tables 4.3 and 4.4, the MISFETs fabricated on the $(000\bar{1})$ face tend to exhibit improved device characteristics compared to those fabricated on the (0001) face. The relatively low threshold voltage and small subthreshold swing in the $(000\bar{1})$ MISFETs imply the superior characteristics at these gate insulators/4H-SiC $(000\bar{1})$ interfaces. The utilization of the $(000\bar{1})$ face is attractive to improve the n-channel MISFET performance as previously reported [13].

4.3.2 Channel Mobility

From the gate characteristics, channel mobility was calculated. Figure 4.4 exhibits the effective mobility (μ_{eff}) of the fabricated (a) MOSFETs with N_2O-grown oxides, deposited SiO_2 annealed in N_2O, and deposited SiO_2 annealed in NO and (b) MISFETs with deposited SiN_x/SiO_2 and thin-thermal oxides between SiN_x/SiO_2 and SiC. The horizontal axis of Fig. 4.4 is the gate insulator field, which is defined as V_G/EOT. In the figure, the closed and open symbols denote the mobility of the (0001) and $(000\bar{1})$ MISFETs, respectively. From Fig. 4.4, high channel mobility can be obtained in the $(000\bar{1})$ MISFETs regardless of the gate insulators.

In the case of N_2O-grown oxides, the MOSFETs on the (0001) face show an effective mobility of 21 cm^2/Vs and those on the $(000\bar{1})$ face an effective mobility of 35 cm^2/Vs. By utilizing deposited SiO_2 annealed in N_2O, the effective mobility is increased to 26 cm^2/Vs for the (0001) face. The channel mobility of the $(000\bar{1})$ MOSFETs with deposited SiO_2 annealed

Table 4.3: Threshold voltage and effective fixed charge density of n-channel MISFETs with various gate insulators.

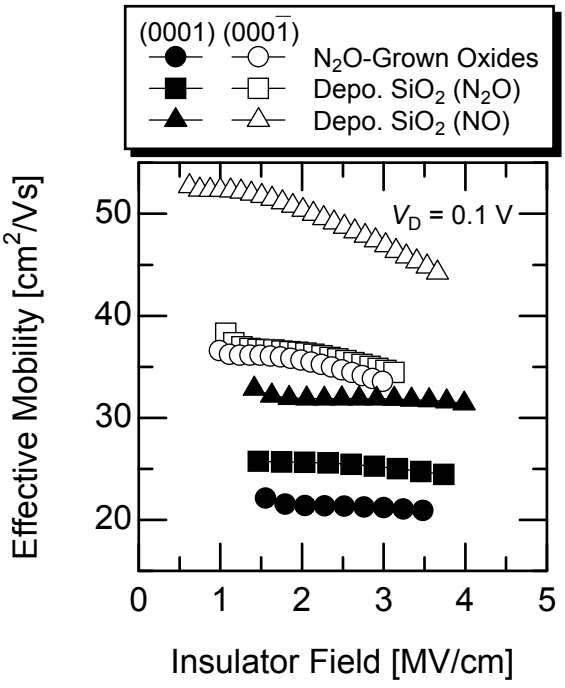
N-Channel 4H-SiC (0001) MISFETs			
Gate Insulators	V_{T} [V]	$V_{\mathrm{T,theory}}$ [V]	Q_{eff} [cm^{-2}]
N_2O-Grown Oxides	7.4	2.1	-1.4×10^{12}
Depo. SiO_2 (N_2O)	5.3	1.9	-8.2×10^{11}
Depo. SiO_2 (NO)	4.6	1.8	-8.9×10^{11}
Depo. SiN_x/SiO_2	-15	1.6	5.7×10^{12}
SiO_2 + Depo. SiN_x/SiO_2	6.2	1.7	-1.4×10^{12}

N-Channel 4H-SiC (000$\bar{1}$) MISFETs			
Gate Insulators	V_{T} [V]	$V_{\mathrm{T,theory}}$ [V]	Q_{eff} [cm^{-2}]
N_2O-Grown Oxides	4.6	2.0	-7.0×10^{11}
Depo. SiO_2 (N_2O)	7.1	2.2	-1.0×10^{12}
Depo. SiO_2 (NO)	1.9	1.8	-4.2×10^{10}
Depo. SiN_x/SiO_2	5.0	1.5	-1.3×10^{12}
SiO_2 + Depo. SiN_x/SiO_2	2.0	1.7	-1.0×10^{11}

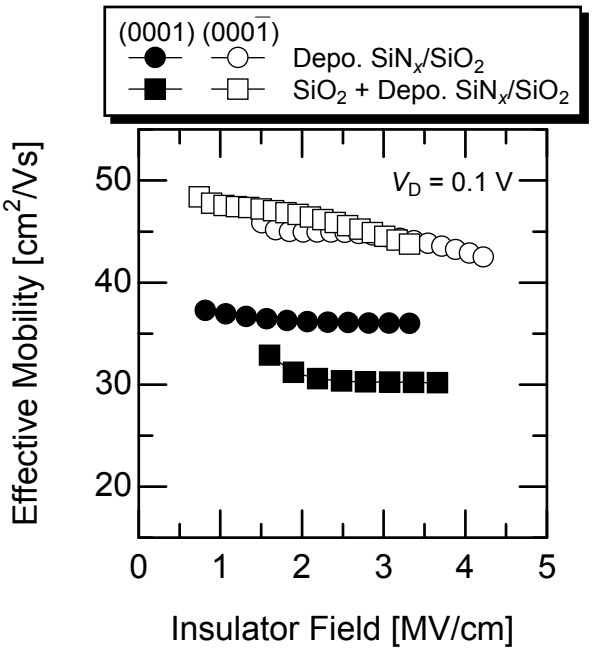
Table 4.4: Subthreshold swing and interface state density of n-channel MISFETs with various gate insulators.

N-Channel 4H-SiC (0001) MISFETs			
Gate Insulators	S [mV/decade]	S_{theory} [mV/decade]	D_{IT} [$\text{cm}^{-2}\text{eV}^{-1}$]
N_2O-Grown Oxides	413	79	1.5×10^{12}
Depo. SiO_2 (N_2O)	—	77	—
Depo. SiO_2 (NO)	—	76	—
Depo. SiN_x/SiO_2	—	74	—
SiO_2 + Depo. SiN_x/SiO_2	299	75	1.2×10^{12}

N-Channel 4H-SiC (000$\bar{1}$) MISFETs			
Gate Insulators	S [mV/decade]	S_{theory} [mV/decade]	D_{IT} [$\text{cm}^{-2}\text{eV}^{-1}$]
N_2O-Grown Oxides	214	78	6.2×10^{11}
Depo. SiO_2 (N_2O)	280	80	7.1×10^{11}
Depo. SiO_2 (NO)	173	76	4.5×10^{11}
Depo. SiN_x/SiO_2	279	73	1.3×10^{12}
SiO_2 + Depo. SiN_x/SiO_2	137	74	3.4×10^{11}



(a)



(b)

Figure 4.4: Effective mobility of the fabricated n-channel (a) MOSFETs and (b) MISFETs. Closed symbols mean the MISFETs on the 4H-SiC (0001) face and open symbols the MISFETs on the 4H-SiC (000$\bar{1}$) face.

in N_2O is almost the same as that of the $(000\bar{1})$ MOSFETs with N_2O-grown oxides. In the fabricated $(000\bar{1})$ MOSFETs, the increment of oxide thickness (17 nm) is large, leading to relatively-low channel mobility. The MOSFETs with deposited SiO_2 annealed in NO exhibit a high effective mobility of 32 cm^2/Vs for the (0001) face and 50 cm^2/Vs for the $(000\bar{1})$ face. Compared to N_2O-grown oxides, the deposited SiO_2 is effective to increase the channel mobility. In particular, the channel mobility is remarkably increased by NO annealing due to the decreased interface state density as shown in Fig. 3.24.

By utilizing the deposited SiN_x/SiO_2, the channel mobility is also increased. In the MISFETs with deposited SiN_x/SiO_2, the channel mobility is increased to 41 cm^2/Vs in the (0001) MISFETs and 45 cm^2/Vs in the $(000\bar{1})$ MISFETs. The high channel mobility can be obtained in the (0001) MISFETs with SiN_x/SiO_2, although large negative threshold voltage and large OFF current were observed. On the other hand, a moderate effective mobility of 30 cm^2/Vs is obtained in the (0001) MISFETs with thin-thermal oxides while keeping a positive threshold voltage of 6.2 V (Fig. 4.3 (b)). In the $(000\bar{1})$ MISFETs with thin-thermal oxides, the effective mobility is improved to 46 cm^2/Vs.

The effective mobility ($\mu_{\rm eff}$) at a $(V_{\rm G} - V_{\rm T})/{\rm EOT}$ of 2 MV/cm is summarized in Table 4.5. In Table 4.5, the peak field-effect mobility ($\mu_{\rm FE}$) is also indicated. Compared to the MOSFETs with N_2O-grown oxides, the MISFETs with deposited insulators demonstrated higher channel mobility. In particular, the $(000\bar{1})$ MOSFETs with deposited SiO_2 annealed in NO demonstrated a high effective mobility of 50 cm^2/Vs. Therefore, the deposition of gate insulators and utilization of the $(000\bar{1})$ face are promising methods to improve the MISFET performance.

4.3.3 Discussion

As discussed in Chapter 3, the properties of deposited SiO_2/4H-SiC (0001) interface were improved by N_2O annealing. When the increment of oxide thickness during the N_2O annealing ($\Delta d_{\rm OX}$) becomes about 3 nm, the interface state density shows a minimum value ($7 \times 10^{11}\,{\rm cm^{-2}eV^{-1}}$) as shown in Fig. 3.11. From this result, it is expected that the performance of the MOSFETs with deposited SiO_2 annealed in N_2O is improved under the same condition ($\Delta d_{\rm OX} = 3$ nm). To confirm this, the MOSFETs with deposited SiO_2, annealed in N_2O for different durations (0–4 h), were fabricated on the 4H-SiC (0001) face. The relationship between the effective mobility and the increment of oxide thickness is shown in Fig. 4.5. The effective mobility indicates a maximum value of 26 cm^2/Vs when the increment of oxide thickness is 5 nm. The increment of oxide thickness to obtain the maximum channel mobility is similar to that to achieve the minimum interface state density. From these results, the high channel mobility in the *n*-channel 4H-SiC MOSFETs with deposited SiO_2 can be obtained when the increment becomes 3–5 nm.

The interface state density was estimated from the capacitance-voltage (*C*–*V*) characteristics of the MIS capacitors fabricated in Chapter 3. The correlation between the channel

Table 4.5: Field-effect mobility and effective mobility of n-channel MISFETs with various gate insulators.

N-Channel 4H-SiC (0001) MISFETs		
Gate Insulators	μ_{FE} [1)] [$\mathrm{cm^2/Vs}$]	μ_{eff} [2)] [$\mathrm{cm^2/Vs}$]
N_2O-Grown Oxides	21	21
Depo. SiO_2 (N_2O)	26	26
Depo. SiO_2 (NO)	32	32
Depo. SiN_x/SiO_2	36	41
SiO_2 + Depo. SiN_x/SiO_2	31	30

N-Channel 4H-SiC ($000\bar{1}$) MISFETs		
Gate Insulators	μ_{FE} [1)] [$\mathrm{cm^2/Vs}$]	μ_{eff} [2)] [$\mathrm{cm^2/Vs}$]
N_2O-Grown Oxides	36	35
Depo. SiO_2 (N_2O)	37	36
Depo. SiO_2 (NO)	53	50
Depo. SiN_x/SiO_2	45	45
SiO_2 + Depo. SiN_x/SiO_2	47	46

1) peak value

2) value at a $(V_{\mathrm{G}} - V_{\mathrm{T}})/\mathrm{EOT}$ of $2\,\mathrm{MV/cm}$

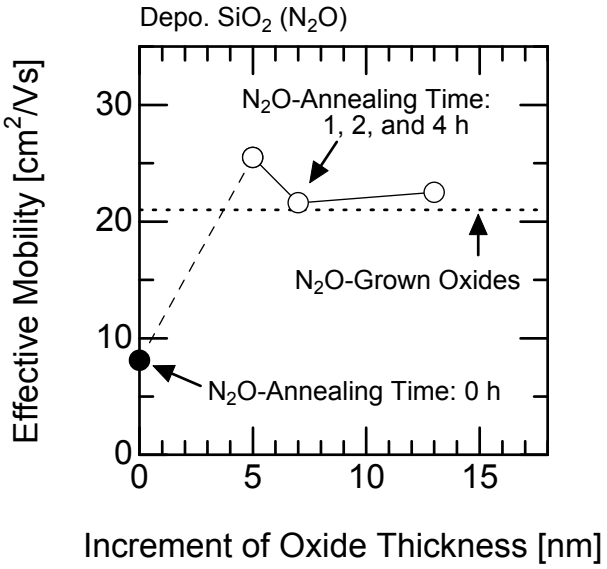


Figure 4.5: Relationship between the effective mobility and the increment of oxide thickness during the N_2O annealing for the n-channel (0001) MOSFETs with deposited SiO_2. The horizontal dotted line indicates the effective mobility of the MOSFETs with N_2O-grown oxides.

mobility of the MISFETs and the interface state density at $E_C - 0.2\,eV$ evaluated by using MIS capacitors is represented in Fig. 4.6. The interface state density in the shallow energy region ($E_C - 0.2\,eV$) strongly affects the effective mobility. The high interface state density leads to low channel mobility, because of increased carrier trapping under strong inversion condition. This result is consistent with the previous report [14]. Thus, the reduction of interface state density in the shallow energy region contributes to the increase of channel mobility.

Another cause for the low channel mobility in the n-channel SiC MISFETs is discussed. Figure 4.7 demonstrates the relationship between the effective mobility and the effective fixed charge density in the n-channel SiC MISFETs with various gate insulators fabricated on the 4H-SiC (0001) and (000$\bar{1}$) faces. The effective fixed charge density was estimated by the difference in the theoretical and experimental threshold voltages. The MISFETs have various gate insulators, such as thermally-grown SiO_2, deposited SiO_2, deposited SiN_x, deposited SiN_x/SiO_2, deposited SiN_x/SiO_2 with thin-thermal oxides, etc. From Fig. 4.7, it is revealed that the low effective fixed charge density is linked to the high channel mobility. The MOSFETs with SiO_2-gate insulators show relatively-linear relationship between the effective channel mobility and the effective fixed charge density (the reduced density of effective fixed charges leads to high effective mobility). Compared to SiO_2-gate insulators, deposited SiN_x/SiO_2 and deposited insulators on thin-thermal oxides show larger variation in the plots.

The main origin of effective fixed charges could be clarified based on the experimental results. Figure 4.8 shows the relationship between the effective fixed charge density and the interface state density estimated from the subthreshold swing. The interface state density evaluated from the difference in the subthreshold swing reflects the density of deep states, which are located in the weak inversion region. The effective fixed charge density is almost proportional to the interface state density for the n-channel MOSFETs with SiO_2-gate insulators (closed circles in Fig. 4.8), which indicates that the effective fixed charges at the SiO_2/SiC interface may be mainly due to the charges trapped at the deep states. On the other hand, correlation between the interface state density and the effective fixed charge density is not clear in the n-channel MISFETs with deposited SiN_x/SiO_2 (open circles in Fig. 4.8). Therefore, in the MISFETs with deposited SiN_x/SiO_2, the origin of effective fixed charges may be the real fixed charges. In the case of the MISFETs with thin-thermal oxides (open boxes in Fig. 4.8), further investigation is required to make a conclusive remark.

From the results mentioned above, in the SiC n-channel MOSFETs with SiO_2-gate insulators (both thermally-grown and deposited SiO_2), the reduction of effective fixed charges, which consist chiefly of the charges trapped at the deep states, contributes greatly to the increase of channel mobility. On the other hand, although the (000$\bar{1}$) MOSFETs with deposited SiO_2 annealed in NO exhibit a low effective fixed charge density of $-4.2 \times 10^{10}\,cm^{-2}$, the channel mobility was improved only to $50\,cm^2/Vs$. An electron mobility in the inversion

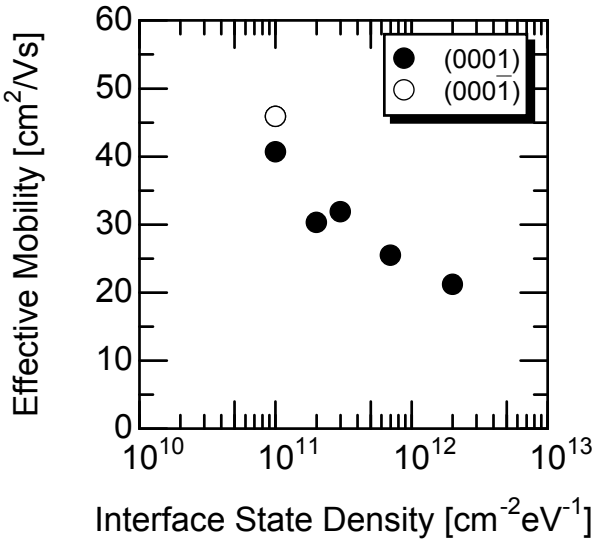


Figure 4.6: Effective mobility versus interface state density. The interface state density, which is evaluated by using MIS capacitors, is the value at $E_C - 0.2\,\mathrm{eV}$. The effective mobility, which is estimated by using MISFETs, is the value at a $(V_G - V_T)$/EOT of 2 MV/cm.

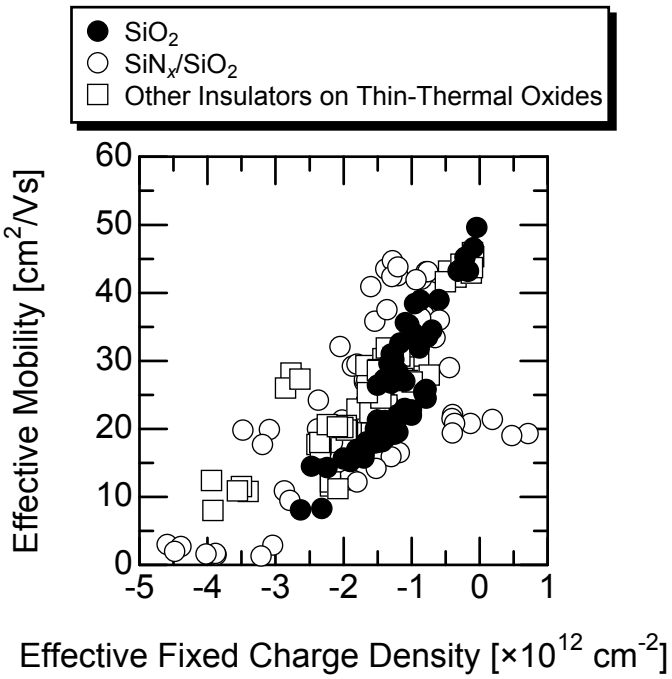


Figure 4.7: Relationship between the effective mobility and the effective fixed charge density for the n-channel 4H-SiC (0001) and (000$\bar{1}$) MISFETs. Closed circles mean the MOSFETs with thermal or deposited oxides, open circles the MISFETs with deposited SiN_x/SiO_2, and open boxes the MISFETs with deposited insulators on thin-thermal oxides.

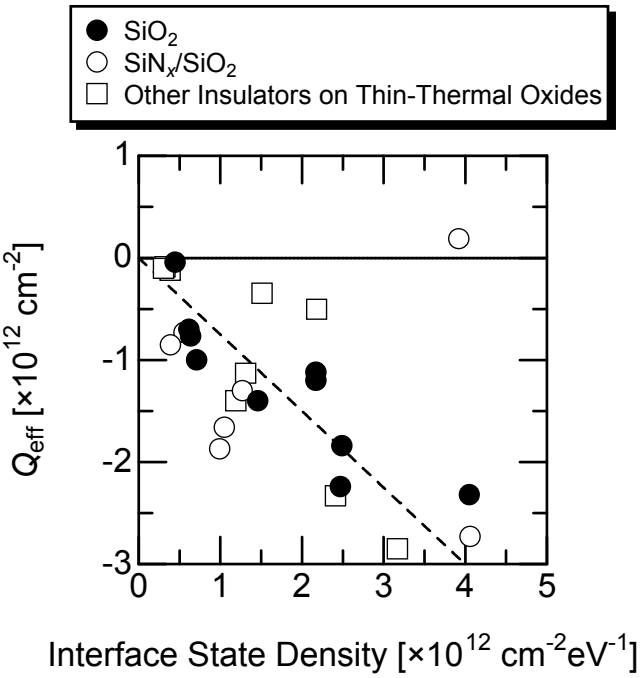


Figure 4.8: Relationship between the effective fixed charge density and the interface state density evaluated from the subthreshold slope. Closed circles mean the MOSFETs with thermal or deposited oxides, open circles the MISFETs with deposited SiN_x/SiO_2, and open boxes the MISFETs with deposited insulators on thin-thermal oxides.

layer of MISFETs ($\mu_{\rm inv}$) can be expressed as [15]:

$$\frac{1}{\mu_{\rm inv}} = \frac{1}{\mu_{\rm Coulomb}} + \frac{1}{\mu_{\rm other}}, \tag{4.5}$$

where $\mu_{\rm Coulomb}$ is the carrier mobility limited by Coulomb scattering, and $\mu_{\rm other}$ the carrier mobility which includes the effects of other scattering factors such as acoustic-phonon scattering, surface roughness scattering, etc. The effect of Coulomb scattering is generally known to dominate the surface electron mobility at low temperature and in weakly inverted surfaces. In SiC MISFETs, the Coulomb scattering is mainly caused by the charges trapped at interface states, of which density (about $10^{12}\,{\rm cm}^{-2}$) is comparable to the electron density in the inversion layer (below $10^{13}\,{\rm cm}^{-2}$). The Coulomb mobility can be described as:

$$\mu_{\rm Coulomb} = \frac{\theta}{|N_{\rm IT}| + |N_{n,\rm real}| + |N_{p,\rm real}|}, \tag{4.6}$$

where θ is the constant, $N_{\rm IT}$ the density of charges trapped at the interface states, and $N_{n,\rm real}$ and $N_{p,\rm real}$ the density of real negative and positive fixed charges, respectively, at the interface and/or inside gate insulators. The effective fixed charge density is represented as:

$$Q_{\rm eff} = N_{\rm IT} + N_{n,\rm real} + N_{p,\rm real}. \tag{4.7}$$

By using Eqs. 4.6 and 4.7, Eq. 4.5 can be modified as:

$$\begin{aligned}\frac{1}{\mu_{\rm inv}} &= \frac{|N_{\rm IT}| + |N_{n,\rm real}| + |N_{p,\rm real}|}{\theta} + \frac{1}{\mu_{\rm other}} \\ &= \frac{-N_{\rm IT} - N_{n,\rm real} + N_{p,\rm real}}{\theta} + \frac{1}{\mu_{\rm other}} \\ &= -\frac{Q_{\rm eff}}{\theta} + \frac{2N_{p,\rm real}}{\theta} + \frac{1}{\mu_{\rm other}}.\end{aligned} \tag{4.8}$$

In the case of SiO_2-gate insulators, the effective fixed charges ($Q_{\rm eff}$) are mainly attributed to the charges trapped at the interface states ($N_{\rm IT}$), and the second term in Eq. 4.8 can be neglected because the density of real fixed charges ($N_{n,\rm real}$ and $N_{p,\rm real}$) is expected to be low. Therefore, the inverse of the inversion channel mobility will be proportional to the effective fixed charge density in the MOSFETs with SiO_2-gate insulators.

Figure 4.9 plots the $1/\mu_{\rm eff}$-$-Q_{\rm eff}$ relationship for the n-channel SiC MISFETs fabricated in this study. As shown in Fig. 4.9, in the MOSFETs with SiO_2-gate insulators (closed circles), the inverse of the effective mobility is almost proportional to the effective fixed charge density when the density is larger than $1 \times 10^{12}\,{\rm cm}^{-2}$, whereas the effective mobility does not depend on the effective fixed charge density when the density is smaller than $1 \times 10^{12}\,{\rm cm}^{-2}$. Therefore, the effective mobility of the n-channel MOSFETs with SiO_2-gate insulators is limited by Coulomb scattering when the effective fixed charge density is high and by other factors when the density is small. In the MISFETs with deposited insulators on thin-thermal oxides (open boxes), although small variations in the plots are

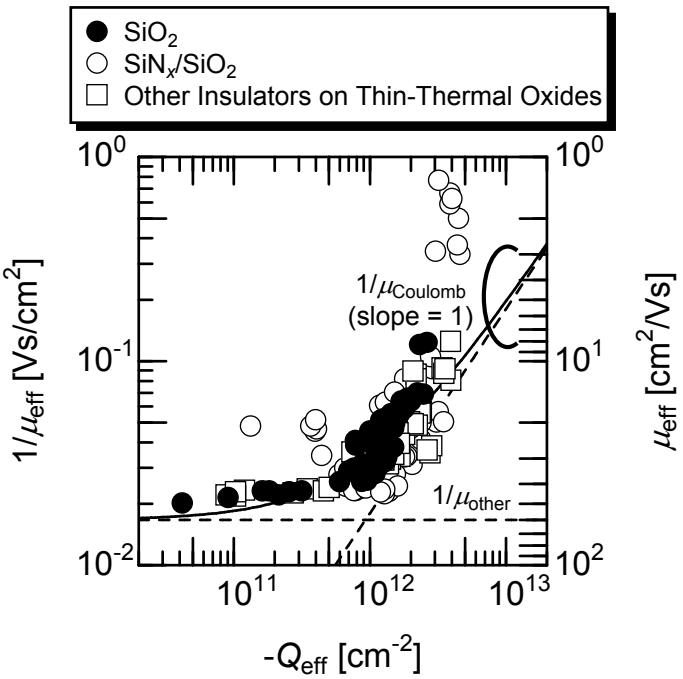


Figure 4.9: Relationship between the effective fixed charge density and the inverse of effective mobility for the n-channel SiC MISFETs on (0001) and (000$\bar{1}$). Closed circles mean the MOSFETs with thermal or deposited oxides, open circles the MISFETs with deposited SiN_x/SiO_2, and open boxes the MISFETs with deposited insulators on thin-thermal oxides.

observed in the region of high effective fixed charge density, the effective mobility is similar to that of MOSFETs with SiO_2-gate insulators. The same scattering factor may limit the effective mobility of the MISFETs with thin-thermal oxides. In the MISFETs with deposited SiN_x/SiO_2, the effective mobility is not dependent of the effective fixed charge density because the real fixed charges may be located inside deposited SiN_x/SiO_2 and/or the MIS interface. In this case, the second term in Eq. 4.8 can not be neglected. Therefore, the channel mobility depends not only on the charges trapped at the interface states but also on the real positive fixed charges, causing the variation in the channel mobility.

From Fig. 4.9, the mobility limited by other scattering factor is calculated to be about $60\,\mathrm{cm^2/Vs}$. Even in the MISFETs with SiO_2-gate insulators, the impact of the real fixed charges on the channel mobility become significant when the charges trapped at the interface states is decreased. For further enhancement of n-channel mobility, other scattering factors, which may be caused by the real fixed charges, need to be minimized.

4.4 *P*-Channel MISFETs

4.4.1 MISFET Characteristics

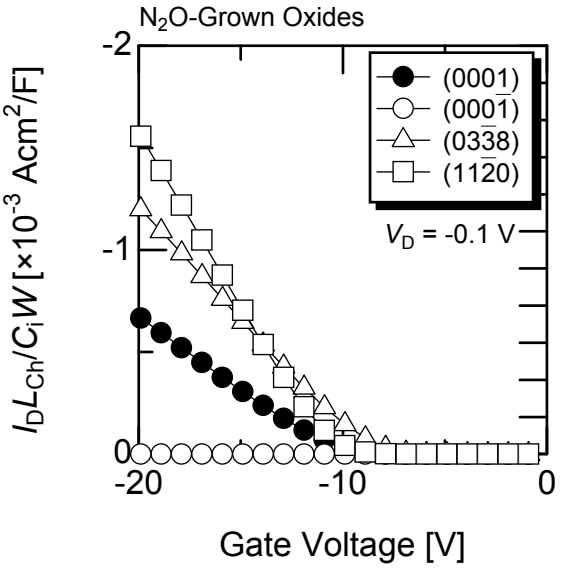
To compare the p-channel MISFETs with various structures, the drain current (I_D) in the gate characteristics was normalized by channel length (L_Ch), channel width (W), and insulator capacitance per unit area (C_i) as is the case for the n-channel MISFETs.

Dry O_2-Grown Oxides

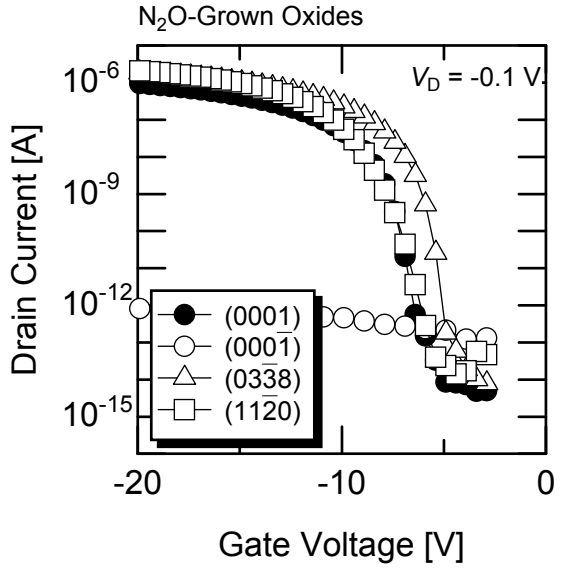
The p-channel (0001) MISFETs with dry O_2-grown oxides showed a threshold voltage (V_T) below $-30\,\mathrm{V}$ and an effective mobility (μ_eff) below $1\,\mathrm{cm^2/Vs}$. The large negative shift of threshold voltage is caused by high density of positive charges at the dry O_2-grown oxides/SiC interface [16]. The dry O_2 oxidation is not a suitable process to form gate insulators of p-channel SiC MOSFETs.

N_2O-Grown Oxides

Figure 4.10 shows the (a) gate (I_D-V_G) and (b) subthreshold ($\log I_\mathrm{D}$-V_G) characteristics of the p-channel MOSFETs with N_2O-grown oxides fabricated on various 4H-SiC faces in the linear region (at a drain voltage (V_D) of $-0.1\,\mathrm{V}$). Although the $(000\bar{1})$ MOSFET is not operational, the MOSFETs on the $(03\bar{3}8)$ and $(11\bar{2}0)$ faces exhibit higher drain current than that on the (0001) face. The p-channel MOSFETs with N_2O-grown oxides exhibit superior characteristics to those with dry O_2-grown oxides. The theoretical/measured threshold voltage is $-4.0\,\mathrm{V}/-10.8\,\mathrm{V}$ for the (0001) MOSFETs, $-5.3\,\mathrm{V}/-9.2\,\mathrm{V}$ for the $(03\bar{3}8)$ MOSFETs, and $-2.8\,\mathrm{V}/-10.8\,\mathrm{V}$ for the $(11\bar{2}0)$ MOSFETs. The measured threshold voltage was shifted toward the negative direction, compared to the theoretical value for each face, which means positive charges, the density of which is over $1 \times 10^{12}\,\mathrm{cm^{-2}}$, exist at the SiO_2/SiC



(a)



(b)

Figure 4.10: (a) Gate and (b) subthreshold characteristics of p-channel MOSFETs with N_2O-grown oxides on various faces. Closed circles denote MOSFET on the 4H-SiC (0001) face, open circles MOSFET on the 4H-SiC (000$\bar{1}$) face, open triangles MOSFET on the 4H-SiC (03$\bar{3}$8) face, and open boxes MOSFET on the 4H-SiC (11$\bar{2}$0) face.

interface. From Fig. 4.10 (b), the subthreshold swings of the MOSFETs with N_2O-grown oxides on the 4H-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) faces are estimated to be 301 mV/decade, 280 mV/decade, and 265 mV/decade, respectively. The (03$\bar{3}$8) and (11$\bar{2}$0) MOSFETs exhibit steep slope in the subthreshold region. From these results, the non-basal faces such as the 4H-SiC (03$\bar{3}$8) and (11$\bar{2}$0) faces are more attractive for improving the performance of *n*-channel SiC MOSFETs [17, 18] as well as *p*-channel SiC MOSFETs.

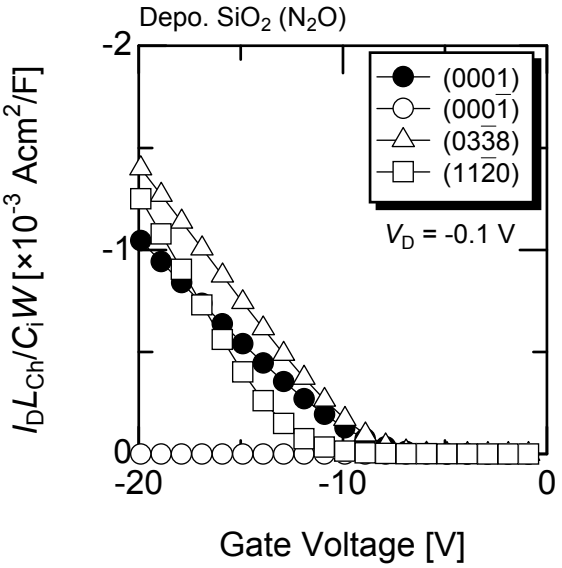
Deposited SiO_2

Figure 4.11 shows the (a) gate and (b) subthreshold characteristics of the fabricated *p*-channel MOSFETs with deposited SiO_2 annealed in N_2O on various faces in the linear region. The (000$\bar{1}$) MOSFET with deposited SiO_2 is not operational as is the case for the N_2O-grown oxides. On the other hand, the *p*-channel MOSFETs with deposited SiO_2 fabricated on other faces show good linear and saturation characteristics. The threshold voltage is −9.8 V for the (0001) MOSFETs, −9.3 V for the (03$\bar{3}$8) MOSFETs, and −12.7 V for the (11$\bar{2}$0) MOSFETs. The threshold voltage approaches the theoretical value (−4.0 V) in the (0001) MOSFETs with deposited SiO_2 compared to those with N_2O-grown oxides. From the subthreshold characteristics (Fig. 4.11 (b)), the subthreshold swing was calculated to be 278 mV/decade for the (0001) face and 274 mV/decade for the (03$\bar{3}$8) face. In the (11$\bar{2}$0) MOSFETs with deposited SiO_2, the subthreshold swing was not calculated because the subthreshold current showed abnormal behavior. By utilizing the deposited SiO_2, the subthreshold characteristics is improved in the (0001) and (03$\bar{3}$8) MOSFETs.

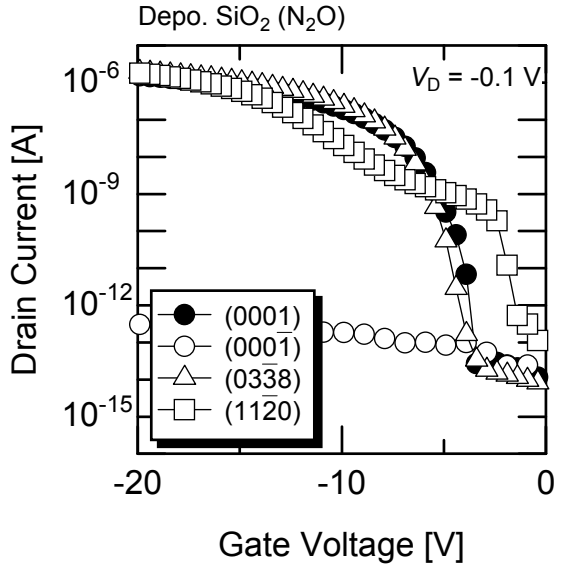
Deposited SiN_x/SiO_2

Figure 4.12 shows the characteristics of the (0001) MISFETs with thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, annealed in N_2O for 2 h. The (0001) MISFETs with thin-thermal oxides exhibit a threshold voltage of −16.9 V and the effective fixed charge density is calculated to be $4.7 \times 10^{12}\,cm^{-2}$. The large negative shift of threshold voltage was measured in the MISFETs with thin-thermal oxides. The subthreshold swing is 469 mV/decade, which is larger than the subthreshold swing of *p*-channel MISFETs with N_2O-grown oxides. The large subthreshold swing indicates the high density of interface states ($2.4 \times 10^{12}\,cm^{-2}eV^{-1}$), and hence the large negative shift of threshold voltage is observed. The reduction of effective fixed charge density is important to improve the *p*-channel MISFETs with deposited SiN_x/SiO_2 on thin-thermal oxides.

The threshold voltage experimentally and theoretically obtained (V_T and $V_{T,theory}$, respectively), and the effective fixed charge density (Q_{eff}) are summarized in Table 4.6. Table 4.7 summarizes the subthreshold swing experimentally and theoretically estimated (S and S_{theory}, respectively) and the interface state density (D_{IT}). From the Table 4.6, compared to the SiC *n*-channel MISFETs (Table 4.3), the absolute value of the effective fixed charge density tends to be large in the SiC *p*-channel MISFETs regardless of the



(a)



(b)

Figure 4.11: (a) Gate and (b) subthreshold characteristics of p-channel MOSFETs with deposited SiO_2 annealed in N_2O on various faces. Closed circles denote MOSFET on the 4H-SiC (0001) face, open circles MOSFET on the 4H-SiC $(000\bar{1})$ face, open triangles MOSFET on the 4H-SiC $(03\bar{3}8)$ face, and open boxes MOSFET on the 4H-SiC $(11\bar{2}0)$ face.

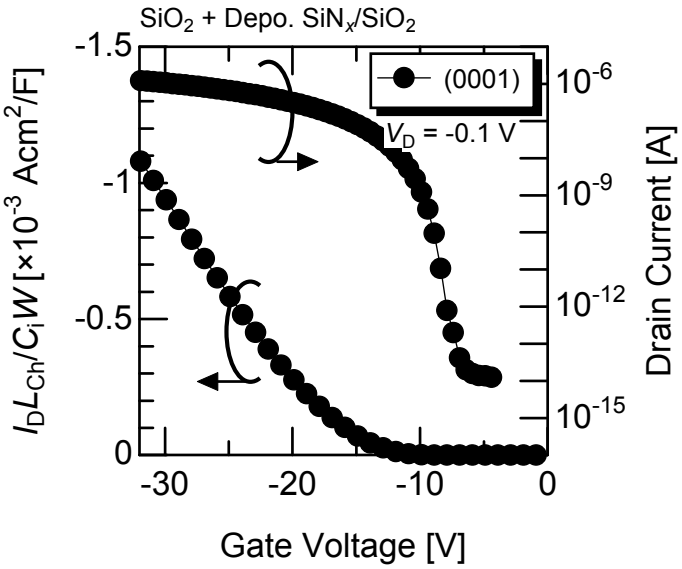


Figure 4.12: Gate and subthreshold characteristics of the (0001) p-channel MISFETs with thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, annealed in N_2O for 2 h.

Table 4.6: Threshold voltage and effective fixed charge density of p-channel MISFETs with various gate insulators.

P-Channel 4H-SiC (0001) MISFETs			
Gate Insulators	V_{T} [V]	$V_{\mathrm{T,theory}}$ [V]	Q_{eff} [cm^{-2}]
Dry O_2-Grown Oxides	< -20	-4.7	$> 5 \times 10^{12}$
N_2O-Grown Oxides	-10.8	-4.0	3.0×10^{12}
Depo. SiO_2 (N_2O)	-9.8	-4.0	2.7×10^{12}
SiO_2 + Depo. SiN_x/SiO_2	-16.9	-3.5	4.7×10^{12}

P-Channel 4H-SiC (000$\bar{1}$) MISFETs			
Gate Insulators	V_{T} [V]	$V_{\mathrm{T,theory}}$ [V]	Q_{eff} [cm^{-2}]
N_2O-Grown Oxides	—	-3.4	—
Depo. SiO_2 (N_2O)	—	-3.1	—

P-Channel 4H-SiC (03$\bar{3}$8) MISFETs			
Gate Insulators	V_{T} [V]	$V_{\mathrm{T,theory}}$ [V]	Q_{eff} [cm^{-2}]
N_2O-Grown Oxides	-9.2	-5.3	1.9×10^{12}
Depo. SiO_2 (N_2O)	-9.3	-4.5	2.1×10^{12}

P-Channel 4H-SiC (11$\bar{2}$0) MISFETs			
Gate Insulators	V_{T} [V]	$V_{\mathrm{T,theory}}$ [V]	Q_{eff} [cm^{-2}]
N_2O-Grown Oxides	-10.8	-2.8	3.3×10^{12}
Depo. SiO_2 (N_2O)	-12.7	-2.9	4.4×10^{12}

Table 4.7: Subthreshold swing and interface state density of p-channel MISFETs with various gate insulators.

P-Channel 4H-SiC (0001) MISFETs			
Gate Insulators	S [mV/decade]	S_{theory} [mV/decade]	D_{IT} [$\text{cm}^{-2}\text{eV}^{-1}$]
Dry O_2-Grown Oxides	—	81	—
N_2O-Grown Oxides	301	74	1.7×10^{12}
Depo. SiO_2 (N_2O)	278	73	1.6×10^{12}
SiO_2 + Depo. SiN_x/SiO_2	469	69	2.4×10^{12}

P-Channel 4H-SiC (000$\bar{1}$) MISFETs			
Gate Insulators	S [mV/decade]	S_{theory} [mV/decade]	D_{IT} [$\text{cm}^{-2}\text{eV}^{-1}$]
N_2O-Grown Oxides	—	68	—
Depo. SiO_2 (N_2O)	—	65	—

P-Channel 4H-SiC (03$\bar{3}$8) MISFETs			
Gate Insulators	S [mV/decade]	S_{theory} [mV/decade]	D_{IT} [$\text{cm}^{-2}\text{eV}^{-1}$]
N_2O-Grown Oxides	280	85	1.6×10^{12}
Depo. SiO_2 (N_2O)	274	78	1.4×10^{12}

P-Channel 4H-SiC (11$\bar{2}$0) MISFETs			
Gate Insulators	S [mV/decade]	S_{theory} [mV/decade]	D_{IT} [$\text{cm}^{-2}\text{eV}^{-1}$]
N_2O-Grown Oxides	265	62	1.6×10^{12}
Depo. SiO_2 (N_2O)	—	63	—

gate insulators. The subthreshold swing of the fabricated p-channel MISFETs is almost the same (about 300 mV/decade) except for the MISFET with thin-thermal oxides (over 400 mV/decade).

4.4.2 Channel Mobility

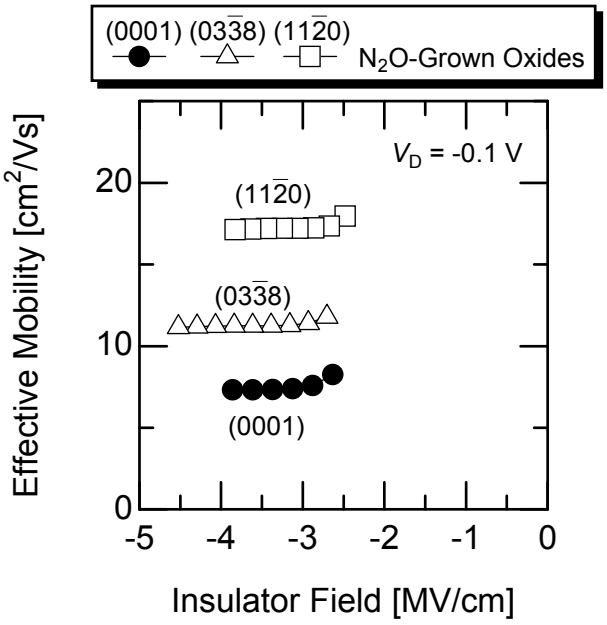
Figure 4.13 shows the effective mobility of the fabricated p-channel MISFETs. Figure 4.13 (a) indicates the mobility of the MOSFETs with N_2O-grown oxides and Fig. 4.13 (b) that of the MISFETs with deposited SiO_2 annealed in N_2O and thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, which were annealed in N_2O for 2 h. In Fig. 4.13, the characteristics of the MOSFETs fabricated on the $(03\bar{3}8)$ and $(11\bar{2}0)$ faces are also exhibited.

From Fig. 4.13, the effective mobility is as high as 17 cm^2/Vs in the $(11\bar{2}0)$ MOSFETs regardless of gate insulators. In Fig. 4.13 (a), the (0001) and $(03\bar{3}8)$ MOSFETs with N_2O-grown oxides show an effective mobility of 7 cm^2/Vs and 11 cm^2/Vs, respectively. In the (0001) and $(03\bar{3}8)$ MOSFETs, however, by utilizing the deposited SiO_2, the channel mobility is increased to 10 cm^2/Vs and 13 cm^2/Vs, respectively. In the case of deposited SiN_x/SiO_2 with thin-thermal oxides (closed rhombuses in Fig. 4.13 (b)), the effective mobility is about 7 cm^2/Vs, which is similar to the mobility of MOSFETs with N_2O-grown oxides.

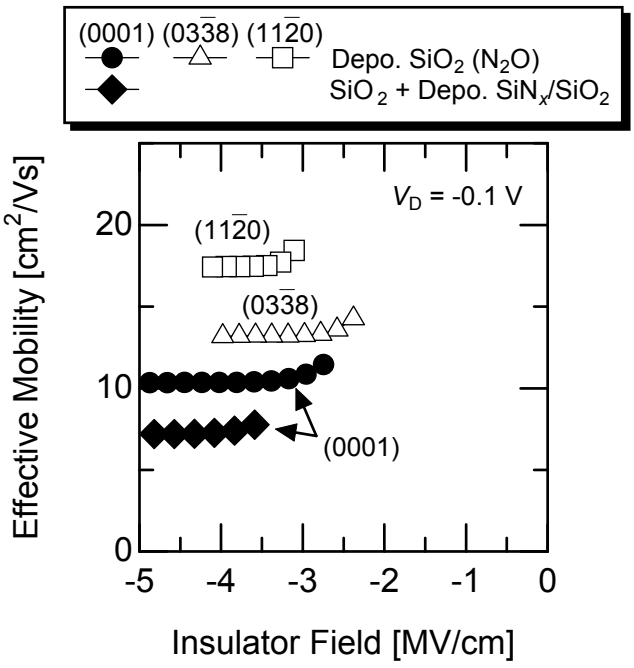
The peak field-effect mobility (μ_{FE}) and the effective mobility (μ_{eff}) at a $(V_G - V_T)/EOT$ of 2 MV/cm are summarized in Table 4.8. The utilization of non-basal faces is effective in improving the p-channel mobility as in the case of n-channel SiC MISFETs [17, 18]. In addition, the deposited SiO_2 can enhance the effective mobility of not only the n-channel MOSFETs but also the p-channel MOSFETs. A channel mobility of over 10 cm^2/Vs is relatively-high value compared to low bulk mobility of holes (about 120 cm^2/Vs). Although the p-channel MISFETs with thin-thermal oxides between deposited SiN_x/SiO_2 and SiC show similar channel mobility to those with N_2O-grown oxides, the positive charges at the interface need to be reduced.

4.4.3 Discussion

Figure 4.14 plots the relationship between the effective mobility and the effective fixed charge density, which is estimated by the difference in the theoretical and experimental threshold voltages, in the p-channel SiC MISFETs with various gate insulators fabricated on the 4H-SiC (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ faces. In contrast to the n-channel SiC MISFETs (Fig. 4.7), the effective mobility does not depend on the effective fixed charge density in the p-channel SiC MISFETs. Figure 4.15 shows the relationship between the effective fixed charge density and the interface state density evaluated from the difference in the subthreshold swing. In Fig. 4.15, no correlation between the interface state density and the effective fixed charge density is observed, although the number of data points is limited.



(a)



(b)

Figure 4.13: Effective mobility of the fabricated p-channel MISFETs with (a) N_2O-grown oxides and (b) deposited insulators. In (b), the channel mobility of the MISFETs with deposited SiO_2 annealed in N_2O and thin-thermal oxides between deposited SiN_x/SiO_2 (10 nm/50 nm) and SiC, which were annealed in N_2O for 2 h, is shown. Closed circles and rhombuses mean the MISFETs on the 4H-SiC (0001) face, open triangles the MOSFETs on the 4H-SiC (03$\bar{3}$8) face, and open boxes the MOSFETs on the 4H-SiC (11$\bar{2}$0) face.

Table 4.8: Field-effect mobility and effective mobility of *p*-channel MISFETs with various gate insulators.

P-Channel 4H-SiC (0001) MISFETs		
Gate Insulators	μ_{FE} [1)] [cm^2/Vs]	μ_{eff} [2)] [cm^2/Vs]
Dry O_2-Grown Oxides	< 1	< 1
N_2O-Grown Oxides	7	7
Depo. SiO_2 (N_2O)	10	10
SiO_2 + Depo. SiN_x/SiO_2	7	7

P-Channel 4H-SiC (03$\bar{3}$8) MISFETs		
Gate Insulators	μ_{FE} [1)] [cm^2/Vs]	μ_{eff} [2)] [cm^2/Vs]
N_2O-Grown Oxides	11	11
Depo. SiO_2 (N_2O)	13	13

P-Channel 4H-SiC (11$\bar{2}$0) MISFETs		
Gate Insulators	μ_{FE} [1)] [cm^2/Vs]	μ_{eff} [2)] [cm^2/Vs]
N_2O-Grown Oxides	17	17
Depo. SiO_2 (N_2O)	17	17

1) peak value
2) value at a $(V_G - V_T)/EOT$ of 2 MV/cm

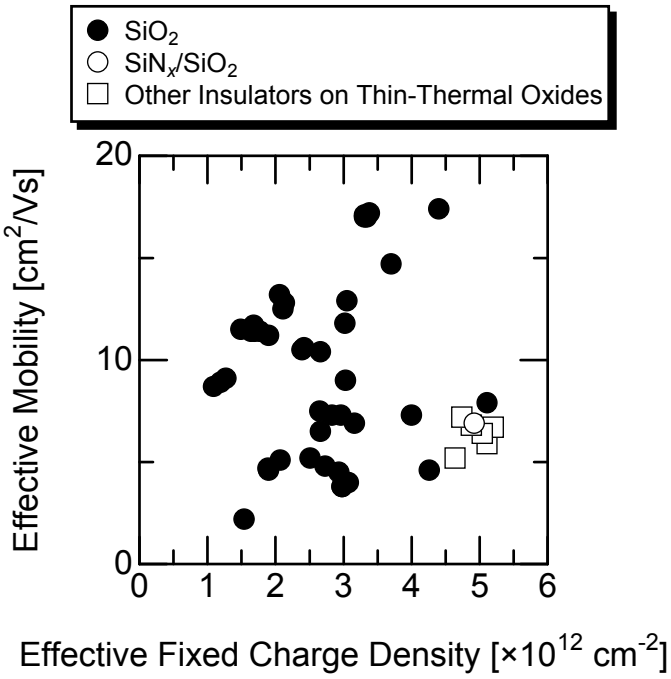


Figure 4.14: Relationship between the effective mobility and the effective fixed charge density for the p-channel 4H-SiC (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ MISFETs. Closed circles denote the MOSFETs with thermally-grown or deposited SiO_2, open circles the MISFETs with deposited SiN_x/SiO_2, and open boxes the MISFETs with deposited insulators on thin-thermal oxides.

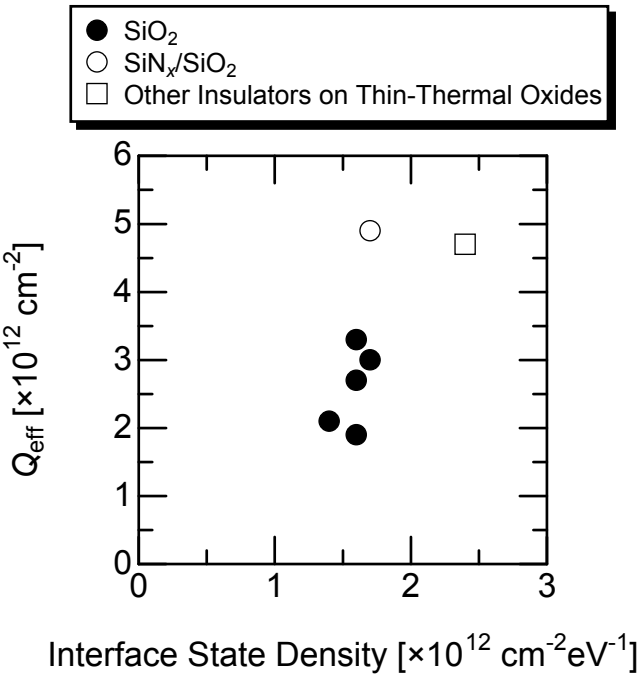


Figure 4.15: Relationship between the effective fixed charge density and the interface state density evaluated from the subthreshold slope for the p-channel SiC MISFETs. Closed circles denote the MOSFETs with thermally-grown or deposited SiO_2, open circles the MISFETs with deposited SiN_x/SiO_2, and open boxes the MISFETs with deposited insulators on thin-thermal oxides.

In the p-channel SiC MISFETs, the effective fixed charges may consist not of the charges trapped at the interface states but rather of the real fixed charges.

In the n-channel SiC MISFETs, the inversion channel mobility can be expressed as Eq. 4.8. In the case of p-channel SiC MISFETs, Eq. 4.5 can be modified as:

$$\begin{aligned}\frac{1}{\mu_{\rm inv}} &= \frac{|N_{\rm IT}| + |N_{n,\rm real}| + |N_{p,\rm real}|}{\theta} + \frac{1}{\mu_{\rm other}} \\ &= \frac{N_{\rm IT} - N_{n,\rm real} + N_{p,\rm real}}{\theta} + \frac{1}{\mu_{\rm other}} \\ &= \frac{Q_{\rm eff}}{\theta} - \frac{2N_{n,\rm real}}{\theta} + \frac{1}{\mu_{\rm other}}. \end{aligned} \tag{4.9}$$

Here, the charges trapped at the interface states ($N_{\rm IT}$) are positive. In contrast to the n-channel SiC MISFETs, the effective fixed charges are nearly independent of the charges trapped at the deep states and the second term in Eq. 4.9 can not be neglected in the p-channel SiC MISFETs. Figure 4.16 represents the $1/\mu_{\rm eff}$-$Q_{\rm eff}$ relationship for the p-channel SiC MISFETs on the (0001) face. To make a fair comparison of channel mobility, the data only for the (0001) face are used because the different surface roughness and doping concentration of the 4H-SiC $(03\bar{3}8)$ and $(11\bar{2}0)$ epilayers increase the influence of other scattering factors. However, no clear correlation is observed in Fig. 4.16. To speculate the scattering mechanism in the p-channel MISFETs, further investigations are needed.

4.5 Interface Properties Evaluated by Using Gate-Controlled Diodes

4.5.1 Analysis Method

The interface properties have been characterized by using MIS capacitors in Chapter 3. In the case of MIS capacitors fabricated on wide bandgap semiconductors such as SiC and GaN, however, it is difficult to characterize the interface state density near the minority-carrier band edge. On the other hand, the interface state density near the minority-carrier band edge can be evaluated by using a gate-controlled diode structure. By using the gate-controlled diode structure [19], the influence of the difference in the conduction type of epilayers can be minimized.

In the gate-controlled diodes (Fig. 4.17), the source/drain regions act as an external source of electrons for n-channel MISFETs and holes for p-channel MISFETs. Thus, the measured C–V curves do not demonstrate "accumulation-depletion-deep depletion" characteristics but "accumulation-depletion-inversion" characteristics in contrast to the normal SiC MIS capacitors. The interface states near the minority-carrier band edge at the gate insulators/SiC interface were analyzed from the measured C–V curves. In this subsection, the detailed characterization of the interface properties of the p-channel MOSFETs with

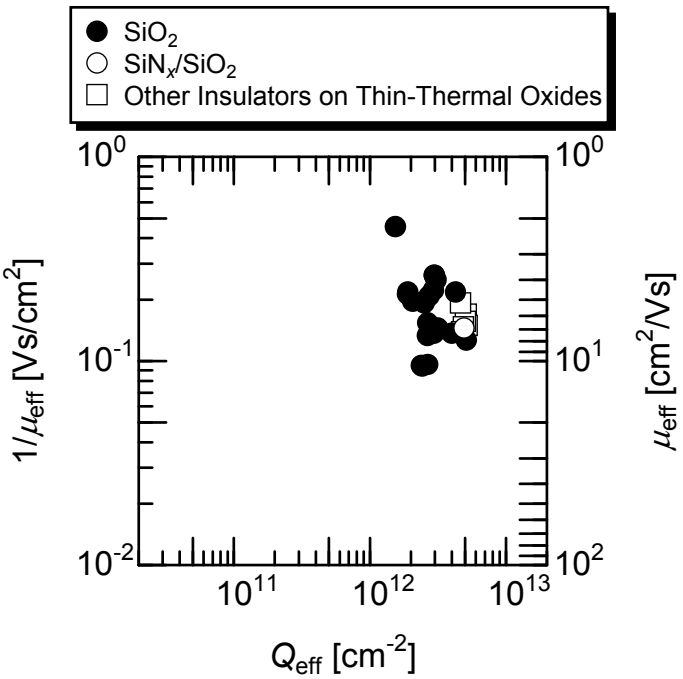


Figure 4.16: Relationship between the effective fixed charge density and the inverse of effective mobility for the p-channel MISFETs on the 4H-SiC (0001) face. Closed circles mean the MOSFETs with thermal or deposited oxides, open circles the MISFETs with deposited SiN_x/SiO_2, and open boxes the MISFETs with deposited insulators on thin-thermal oxides.

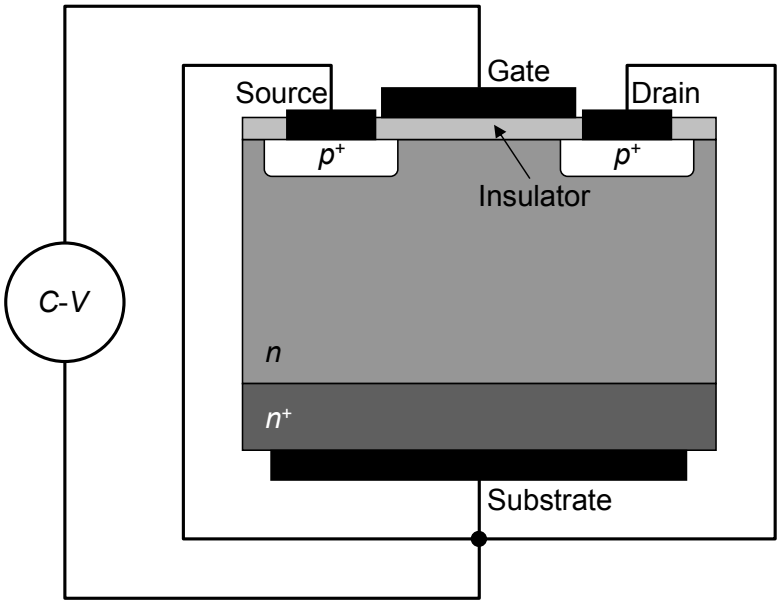


Figure 4.17: Measurement circuit for a gate-controlled diode (the case of p-channel MISFET).

N_2O-grown oxides is explained as an example of the proposed method. In the following subsections, the interface properties of other n- and p-channel MISFETs are explored by using gate-controlled diodes.

Figure 4.18 shows the quasi-static C–V curve ($C_{\rm QS}$) obtained from the p-channel $(03\bar{3}8)$ MOSFET with an N_2O-grown oxide by using the gate-controlled diode structure. The theoretical low-frequency C–V curve is also indicated in Fig. 4.18. The area of gate electrode is about $4.9 \times 10^{-4}\,{\rm cm}^2$. The measured C–V characteristics indicate that the MOS interface under the gate electrode shows strong inversion at sufficiently negative gate voltage. From the measured C–V curves, the interface state density near the valence band edge was evaluated. At first, the surface potential ($\Psi_{\rm S}$)-gate voltage ($V_{\rm G}$) characteristics were calculated by using the following equation [20]:

$$\Psi_{\rm S}(V_{\rm G2}) = \int_{V_{\rm G1}}^{V_{\rm G2}} \left(1 - \frac{C_{\rm QS}(V_{\rm G})}{C_{\rm i}}\right) {\rm d}V_{\rm G} + \Psi_{\rm S}(V_{\rm G1}). \tag{4.10}$$

In Eq. 4.10, to determine the absolute value of surface potential, the basis of surface potential must be defined. In this study, the author assumed that the surface potential calculated from the measured C–V characteristics coincides with that theoretically obtained at a gate voltage of $-15\,{\rm V}$ (sufficiently large bias in the strong inversion). Then, the $\Psi_{\rm S}$-$V_{\rm G}$ characteristics experimentally obtained are compared with the theoretical $\Psi_{\rm S}$-$V_{\rm G}$ relationship.

Figures 4.19–4.21 show the $\Psi_{\rm S}$-$V_{\rm G}$ curves experimentally and theoretically obtained for the (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ gate-controlled diodes, respectively. Due to the different donor concentration of the epilayers, the absolute value of $2\Psi_{\rm B}$ (solid lines in Figs. 4.19–4.21) is different for each device on the (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ faces. Compared with the theoretical curves, the shift of experimental $\Psi_{\rm S}$-$V_{\rm G}$ curves toward the negative gate voltage direction is caused by the presence of effective fixed charges (positive) located at the SiO_2/SiC interface, and the stretch-out of $\Psi_{\rm S}$-$V_{\rm G}$ curves by the presence of interface states. In the ideal case (theoretical $\Psi_{\rm S}$-$V_{\rm G}$ curve), the change of gate voltage directly causes that of the surface potential. On the other hand, in the case of the experimental $\Psi_{\rm S}$-$V_{\rm G}$ curves, the additional increment of gate voltage is needed in order to fill the interface states with holes. Thus, the interface state density ($D_{\rm IT}$) can be evaluated from the difference between the slope of $\Psi_{\rm S}$-$V_{\rm G}$ characteristics theoretically and experimentally obtained as described in the following equation:

$$D_{\rm IT} = \frac{C_{\rm i}}{e}\left(\left.\frac{{\rm d}V_{\rm G}}{{\rm d}\Psi_{\rm S}}\right|_{\rm theory} - \left.\frac{{\rm d}V_{\rm G}}{{\rm d}\Psi_{\rm S}}\right|_{\rm experiment}\right). \tag{4.11}$$

From this equation, the interface state density near the valence band edge in the p-channel SiC MOSFETs with N_2O-grown oxides can be calculated.

4.5.2 *N*-Channel MISFETs

The interface state density of n-channel 4H-SiC (0001) MOSFETs with N_2O-grown oxides is compared with that of n-type 4H-SiC (0001) MOS capacitors with N_2O-grown oxides.

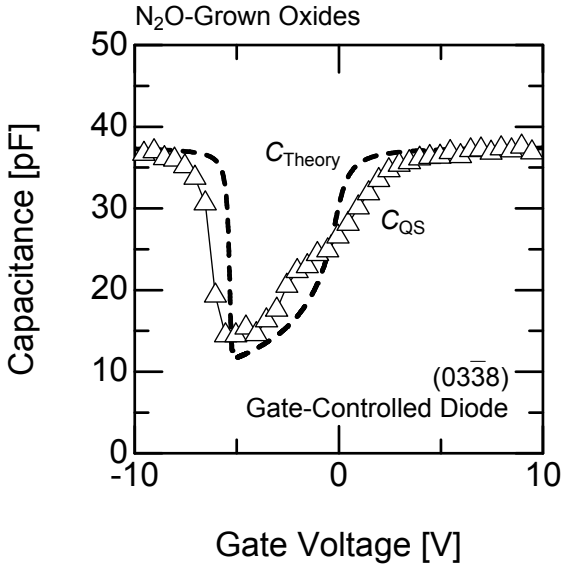


Figure 4.18: Quasi-static C–V curve obtained from a p-channel MOSFET with an N_2O-grown oxide fabricated on the 4H-SiC (03$\bar{3}$8) face by using a gate-controlled diode structure. A theoretical C–V curve is also shown by a dashed line.

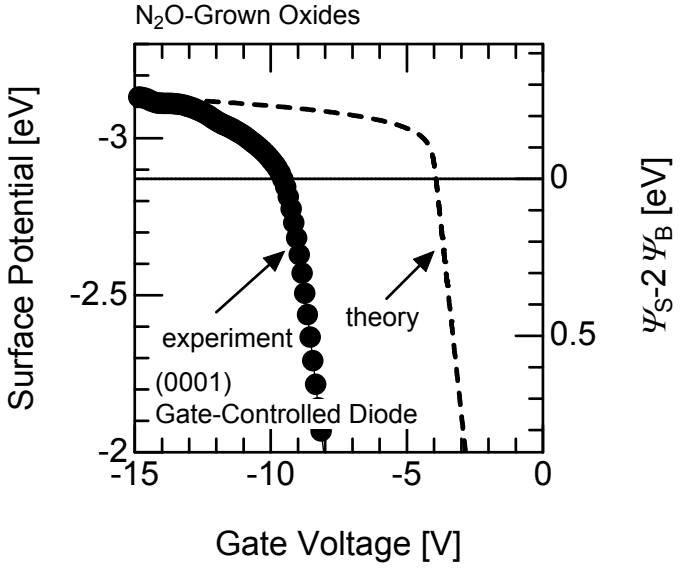


Figure 4.19: Ψ_S-V_G characteristics of the (0001) MOSFET with an N_2O-grown oxide. Closed circles mean the Ψ_S-V_G characteristics experimentally obtained. The dashed line means the theoretical Ψ_S-V_G curve. The right vertical axis denotes the $\Psi_S - 2\Psi_B$, and the horizontal solid line represents the $\Psi_S = 2\Psi_B$.

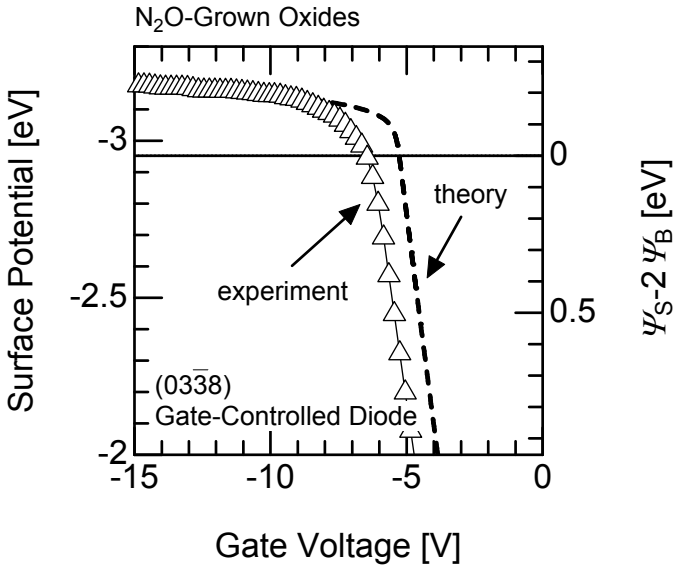


Figure 4.20: Ψ_S-V_G characteristics of the (03$\bar{3}$8) MOSFET with an N_2O-grown oxide. Open triangles mean the Ψ_S-V_G characteristics experimentally obtained. The dashed line means the theoretical Ψ_S-V_G curve. The right vertical axis denotes the $\Psi_S - 2\Psi_B$, and the horizontal solid line represents the $\Psi_S = 2\Psi_B$.

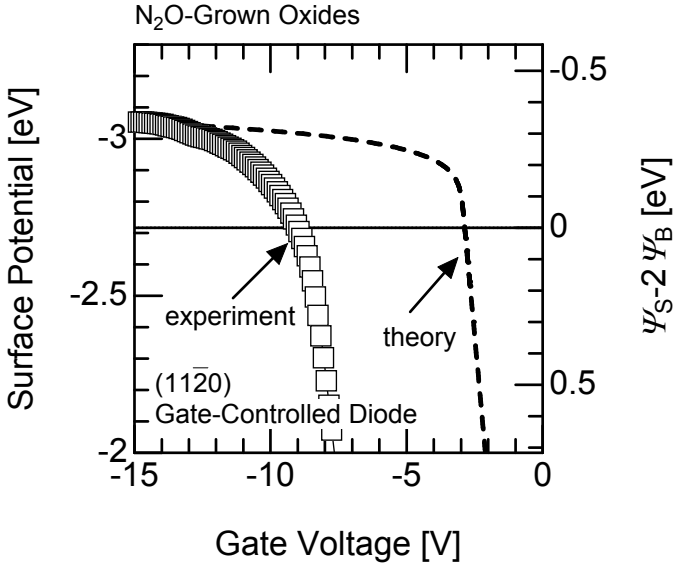


Figure 4.21: Ψ_S-V_G characteristics of the (11$\bar{2}$0) MOSFET with an N_2O-grown oxide. Open circles mean the Ψ_S-V_G characteristics experimentally obtained. The dashed line means the theoretical Ψ_S-V_G curve. The right vertical axis denotes the $\Psi_S - 2\Psi_B$, and the horizontal solid line represents the $\Psi_S = 2\Psi_B$.

Figure 4.22 shows the distribution of interface state density obtained for the n-channel (0001) MOSFET (gate-controlled diode) and n-MOS capacitor with N_2O-grown oxides. Although the gate-controlled diode shows the low interface state density in the deep energy region, the interface state density in the shallow energy region estimated by using the gate-controlled diodes ($1 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$) is similar to that evaluated by the MOS capacitors ($2 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$).

The distribution of the interface state density for the n-channel 4H-SiC ($000\bar{1}$) MISFETs with N_2O-grown oxides, deposited SiO_2 annealed in NO, thin-thermal oxides between deposited SiN_x/SiO_2 and SiC was estimated by using the gate-controlled diodes. Figure 4.23 represents the interface state density of these MISFETs. For comparison, the interface state density of the (0001) MOSFETs with N_2O-grown oxides is also shown as a dashed line in Fig. 4.23. Although the ($000\bar{1}$) MISFETs with various gate insulators exhibit lower interface state density than the (0001) MOSFETs with N_2O-grown oxides, there is little difference in the interface state density of the ($000\bar{1}$) MISFETs, regardless of the gate insulators. The thickness of gate insulators for the n-channel ($000\bar{1}$) MISFETs is about 60–80 nm, which is thicker than that of the p-channel MISFETs (Tables 4.1 and 4.2). As a result, the accumulation and inversion capacitance for these MISFETs is decreased to below 20 pF. On the other hand, the noise level in the C–V measurement system is about 1–2 pF, which can affect the accurate measurements of the accumulation and inversion capacitances. Therefore, it is difficult to measure the change in the "inversion-depletion" capacitance, which is critically important for the calculation of the interface state density. By fabricating the MISFETs with larger gate area or thinner oxide thickness (to increase the inversion capacitance), this problem can be avoided and the accurate distribution of the interface state density for the ($000\bar{1}$) MISFETs can be obtained.

4.5.3 *P*-Channel MISFETs

Figure 4.24 shows the distributions of the interface state density near the valence band edge for the (0001), ($03\bar{3}8$), and ($11\bar{2}0$) MOSFETs with N_2O-grown oxides. From Fig. 4.24, the interface state density is exponentially increased toward the valence band edge and reaches to $2 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$ at $E_V + 0.2\,\mathrm{eV}$ for the (0001) interface. On the other hand, the ($03\bar{3}8$) face shows a lower interface state density of $1 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$ at 0.2 eV above the valence band edge. Contrary to expectation, the ($11\bar{2}0$) face exhibits higher interface state density than the ($03\bar{3}8$) face, and the interface state density is $2 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}}$ at $E_V + 0.2\,\mathrm{eV}$. Compared with the SiO_2/4H-SiC (0001) interface, the interface state density at the SiO_2/4H-SiC ($11\bar{2}0$) interface is high in the deep energy region and relatively low in the shallow energy region from the valence band edge.

Interface state density of the p-channel MOSFETs with deposited SiO_2 annealed in N_2O was also calculated. Figure 4.25 shows the distribution of the interface state density for the p-channel MOSFETs with deposited SiO_2 fabricated on the 4H-SiC (0001), ($03\bar{3}8$), and

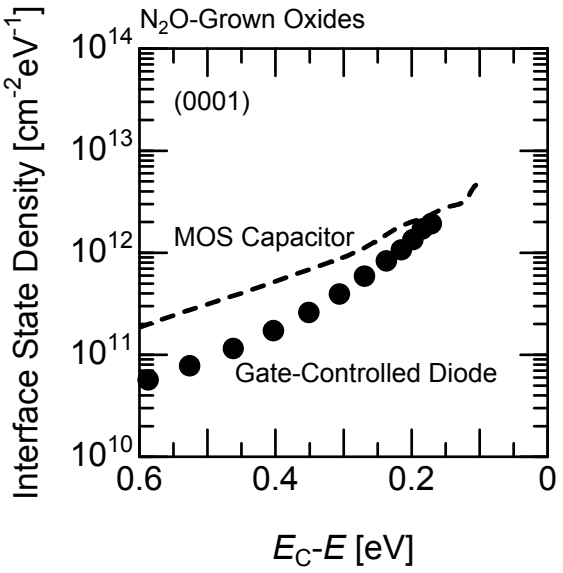


Figure 4.22: Interface state density of N_2O-grown oxides/4H-SiC (0001) interface. The dashed line represents the interface state density evaluated by using the MOS capacitor, and closed circles that evaluated by using the gate-controlled diode.

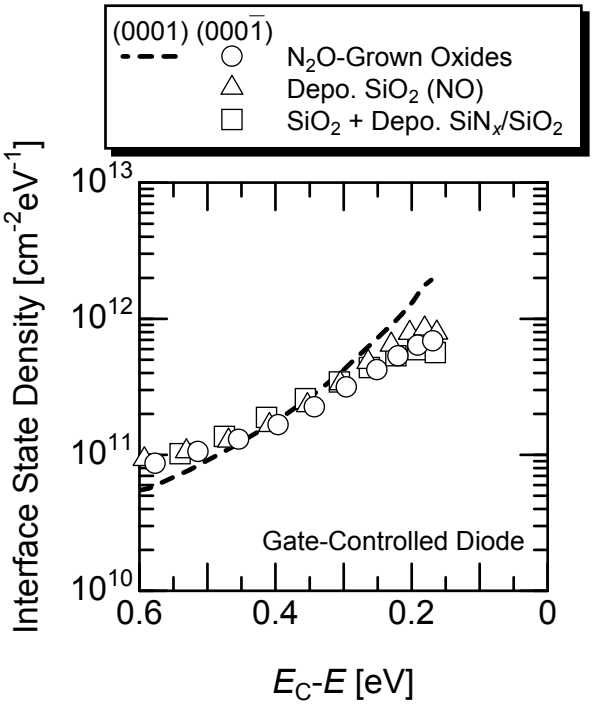


Figure 4.23: Interface state density of various gate insulators/4H-SiC $(000\bar{1})$ interface evaluated by using the gate-controlled diodes. Open circles mean the MISFETs with N_2O-grown oxides, open triangles those with deposited SiO_2 annealed in NO, and open boxes those with thin-thermal oxides between deposited SiN_x/SiO_2 and SiC. The dashed line represents the interface state density of the (0001) MOSFETs with N_2O-grown oxides.

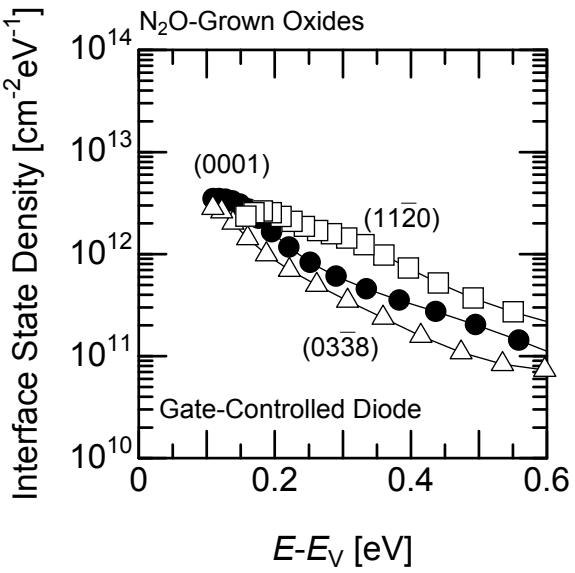


Figure 4.24: Interface state density of N_2O-grown oxides/4H-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) interfaces (closed circles, open triangles, and open boxes, respectively). The interface state density was estimated from C–V curves measured by using the gate-controlled diode structure.

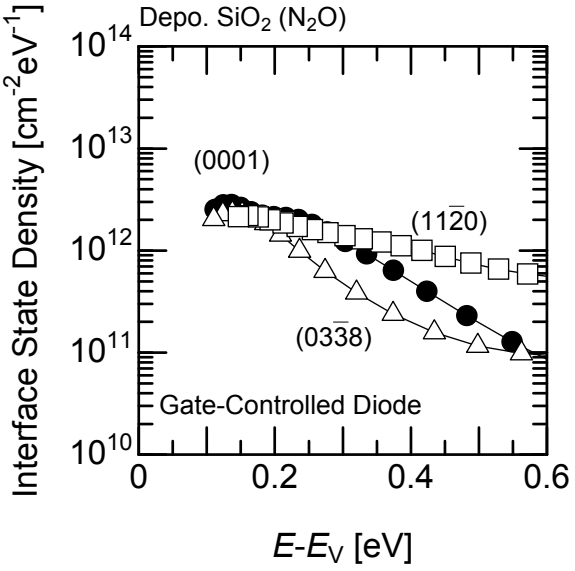


Figure 4.25: Interface state density of deposited SiO_2 annealed in N_2O/4H-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) interfaces (closed circles, open triangles, and open boxes, respectively). The interface state density was estimated by C–V curves measured by using the gate-controlled diode structure.

$(11\bar{2}0)$ faces. In the case of deposited SiO_2 annealed in N_2O, the lowest interface state density is observed in the $(03\bar{3}8)$ MOSFETs ($1 \times 10^{12}\,cm^{-2}eV^{-1}$ at $E_V + 0.2\,eV$) as in the case of those with N_2O-grown oxides. On the other hand, the (0001) and $(11\bar{2}0)$ MOSFETs with deposited SiO_2 annealed in N_2O show an interface state density of $2 \times 10^{12}\,cm^{-2}eV^{-1}$ at 0.2 eV above the valence band edge. The absolute value of the interface state density for the *p*-channel MOSFETs with deposited SiO_2 annealed in N_2O is similar to that for the *p*-channel MOSFETs with N_2O-grown oxides regardless of crystal face orientation.

In this study, although *p*-channel MOSFETs were fabricated on the 4H-SiC $(000\bar{1})$C face, they were not operational. Figure 4.26 shows the quasi-static *C*–*V* curve of a $(000\bar{1})$ MOSFET with an N_2O-grown oxide measured by using gate-controlled diode structure. In contrast to the *p*-channel MOSFETs with N_2O-grown oxides fabricated on other faces (Fig. 4.18), MOSFETs fabricated on $(000\bar{1})$ exhibit "accumulation-depletion-deep depletion" characteristics. Similar characteristics were observed even in $(000\bar{1})$ MOSFETs with deposited SiO_2 annealed in N_2O. The source-substrate and drain-substrate junctions in the $(000\bar{1})$ MOSFETs act as a *pn*-junction without problems. Therefore, these SiO_2/*n*-type 4H-SiC $(000\bar{1})$ interfaces can not be inverted or more negative gate voltage is needed to invert the interfaces.

4.6 Discussion

In this chapter, various dielectrics such as N_2O-grown oxides, deposited SiO_2, and deposited SiN_x/SiO_2, which were explored in Chapter 3, were applied to the gate insulators of 4H-SiC *n*- and *p*-channel MISFETs. Figure 4.27 exhibits the typical (a) gate characteristics and (b) effective mobility of the *n*- and *p*-channel MISFETs with various gate insulators fabricated on the 4H-SiC (0001) face. In Fig. 4.27 (a), the drain current (I_D) is normalized by the channel length (L_{Ch}), the channel width (W), and the insulator capacitance (C_i). In the case of *n*-channel MISFETs, the drain current is increased by utilizing the deposited SiO_2 annealed in N_2O and the deposited SiN_x/SiO_2 with thin-thermal oxides, and hence the MISFETs with these insulators show high channel mobility. In the case of *p*-channel MISFETs, the deposited SiO_2 is also effective in increasing the drain current. *P*-channel MISFETs with deposited SiN_x/SiO_2 on thin-thermal oxides show similar channel mobility as those with N_2O-grown oxides, although the threshold voltage is shifted toward the negative gate direction. The deposited insulators have advantages over the N_2O-grown oxides.

The utilization of 4H-SiC $(000\bar{1})$ is attractive to improve the channel mobility in *n*-channel MISFETs, in addition to the utilization of deposited insulators. On the other hand, the *p*-channel 4H-SiC $(000\bar{1})$ MISFETs were not operational because the MIS interface can not become inversion condition. In the case of CMOS circuits, both *n*- and *p*-channel MISFETs must be fabricated on the same crystal face under the same formation process of gate insulators. Therefore, the problem that *p*-channel $(000\bar{1})$ MISFETs can not operate

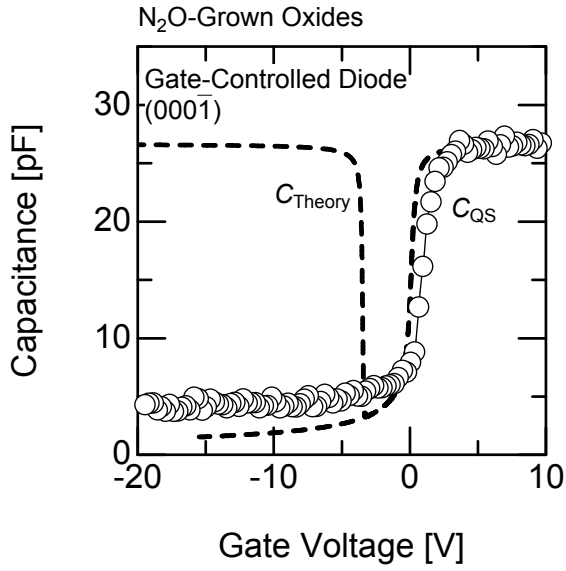
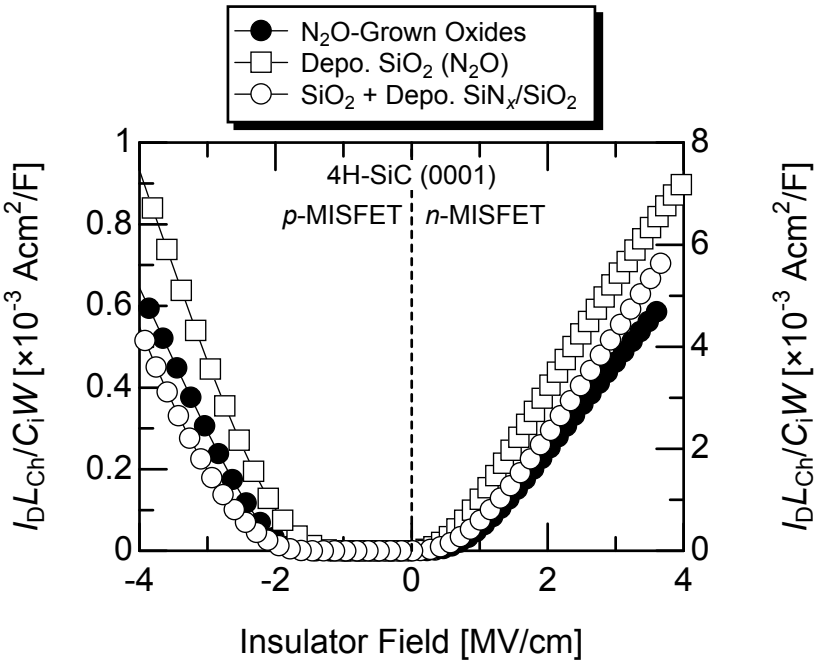
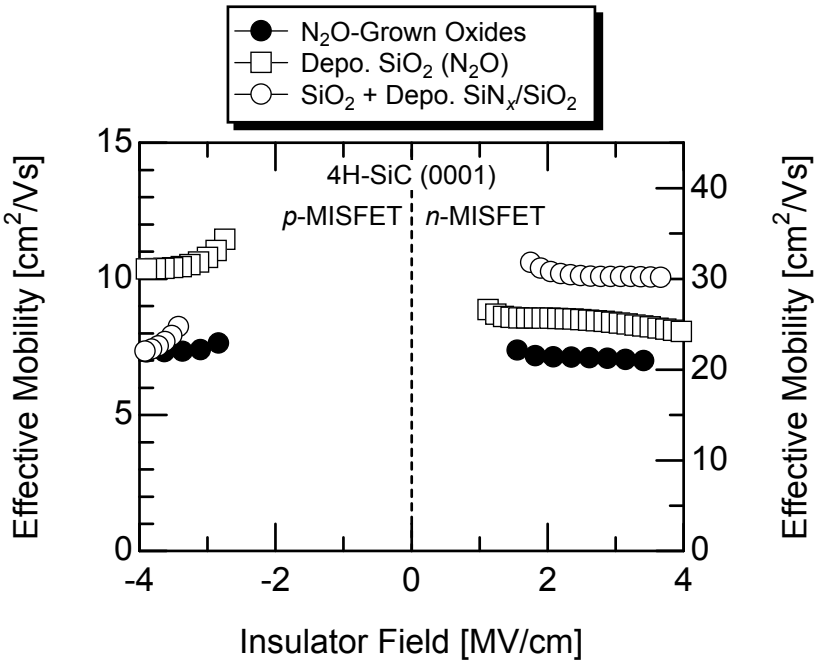


Figure 4.26: Quasi-static C–V curve obtained in the p-channel MOSFET with an N_2O-grown oxide fabricated on the 4H-SiC (000$\bar{1}$) face by using a gate-controlled diode structure. A theoretical C–V curve is also shown by a dashed line.



(a)



(b)

Figure 4.27: Typical (a) gate characteristics and (b) effective mobility of the fabricated n- and p-channel 4H-SiC (0001) MISFETs with various gate insulators. Closed circles mean the characteristics of the MOSFETs with N_2O-grown oxides, open boxes those of the MOSFETs with deposited SiO_2 annealed in N_2O, and open circles those of the MISFETs with thin-thermal oxides between deposited SiN_x/SiO_2 and SiC, annealed in N_2O. The drain current is normalized by the channel length, the channel width, and the insulator capacitance per unit area. The horizontal axis is the gate insulator field (V_G/EOT).

needs to be solved, to receive the full benefit of a high channel mobility in n-channel $(000\bar{1})$ MISFETs.

In the case of n-channel MISFETs with SiO_2-gate insulators, the channel mobility is limited by the Coulomb scattering mainly caused by the charges trapped at the interface states. In addition, the interface states reduce the number of mobile electrons due to electron trapping. When the interface state density is reduced and hence the effective fixed charge density is decreased, other scattering mechanism becomes dominant. On the other hand, the channel mobility of the n-channel MISFETs with deposited SiN_x/SiO_2 and the p-channel MISFETs with various gate insulators may be limited by the real fixed charges and/or other scattering factors. It is useful to measure the temperature dependence of channel mobility for classification of the scattering mechanism. By measuring the MISFET performance over a wide temperature range, the dominant scattering mechanism should be elucidated, which contributes greatly to the further improvement in channel mobility.

In the case of p-channel MISFETs, the N_2O-grown oxides and deposited SiO_2 annealed in N_2O/4H-SiC $(03\bar{3}8)$ interfaces exhibit the lowest interface state density, leading to a high channel mobility in $(03\bar{3}8)$ MOSFETs with these oxides. Although the N_2O-grown oxides and deposited SiO_2/4H-SiC $(11\bar{2}0)$ interfaces show high interface state density in the deep energy region, the p-channel MOSFETs on the 4H-SiC $(11\bar{2}0)$ face exhibit high channel mobility as described in Section 4.4.2. The main reason for the high channel mobility in $(11\bar{2}0)$ MOSFETs may be the low donor concentration ($N_D = 5$–$8 \times 10^{14}\,cm^{-3}$) of the employed epilayers. The channel mobility of MISFETs generally depends on the doping concentration of epilayers [21, 22]. The decrease in donor concentration results in an increase in channel mobility, because the influence of surface roughness scattering and Coulomb scattering from the charges located near the interface is weakened due to its low vertical electric field in the inversion layer. In addition, the SiO_2/4H-SiC $(11\bar{2}0)$ interface shows the relatively low interface state density near the valence band edge. In the case of 4H-SiC n-channel MISFETs, the interface state density near the conduction band edge adversely affects the channel mobility due to severe electron trapping (Fig. 4.6). In a similar way, the channel mobility of p-channel MOSFETs fabricated on the (0001) face may be severely influenced by the shallow interface states, which cause hole trapping. For these reasons, the p-channel MOSFETs fabricated on the $(11\bar{2}0)$ face may exhibit the high channel mobility.

In this study, the p-channel MOSFETs with N_2O-grown oxides were fabricated on the 4H-SiC (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ faces. Few groups have reported that the interface state density, evaluated by using MOS capacitors, near the valence band edge on the (0001) face is decreased in the nitrided-gate oxides/SiC interface, compared with dry O_2 oxidation [23, 24]. Thus, the nitridation of SiO_2/SiC interface is one of the promising processes to improve the performance of both n-channel and p-channel MOS devices on most crystal faces of SiC.

From the characteristics of the p-channel MISFETs, the 4H-SiC $(03\bar{3}8)$ and $(11\bar{2}0)$ faces are attractive crystal faces to achieve high p-channel mobility. On the other hand, n-channel

SiC MISFETs on these faces have not been fabricated in this study. The n-channel $(03\bar{3}8)$ and $(11\bar{2}0)$ MOSFETs with wet O_2-grown oxides exhibit higher channel mobility than the (0001) MOSFETs [17, 18]. By utilizing N_2O-grown oxides and deposited insulators, the channel mobility of n-channel MISFETs on the 4H-SiC $(03\bar{3}8)$ and $(11\bar{2}0)$ faces may be improved. Although the immature epitaxial technology for these non-basal faces remains as an issue to be solved, the 4H-SiC $(03\bar{3}8)$ and $(11\bar{2}0)$ faces have the potential for the becoming substrates of high-performance ICs.

4.7 Summary

The deposited SiO_2 and SiN_x/SiO_2 were applied to the gate insulators of 4H-SiC n- and p-channel MISFETs.

The channel mobility of the n-channel MOSFETs with N_2O-grown oxides was about $21\,cm^2/Vs$ on the 4H-SiC (0001) face and improved to $35\,cm^2/Vs$ on the $(000\bar{1})$ face. In the case of the p-channel MOSFETs, a channel mobility of $7\,cm^2/Vs$ was obtained on the (0001) face and the mobility could be increased to over $10\,cm^2/Vs$ by utilizing the $(03\bar{3}8)$ and $(11\bar{2}0)$ faces.

The deposited insulators improve the MISFET performance. The n- and p-channel mobility of the MOSFETs with deposited SiO_2 annealed in N_2O on (0001) was $26\,cm^2/Vs$ and $10\,cm^2/Vs$, respectively. The NO annealing after SiO_2 deposition is effective in improving the n-channel mobility, and the MOSFETs with deposited SiO_2 annealed in NO exhibited a channel mobility on $32\,cm^2/Vs$ on (0001). In addition, a high channel mobility of $50\,cm^2/Vs$ could be realized by utilizing the deposited SiO_2 on the 4H-SiC $(000\bar{1})$ face. The deposited SiN_x/SiO_2 is also attractive to increase the channel mobility. The n-channel MISFETs with deposited SiN_x/SiO_2 on thin-thermal oxides showed a channel mobility of $30\,cm^2/Vs$ on (0001) and $46\,cm^2/Vs$ on $(000\bar{1})$. The p-channel mobility of the (0001) MISFETs with deposited SiN_x/SiO_2 on thin-thermal oxides was $7\,cm^2/Vs$, which is similar to that of the (0001) MOSFETs with N_2O-grown oxides. Therefore, the utilization of deposited insulators can contribute greatly to the increase of both n- and p-channel mobility of SiC MISFETs.

In the n-channel MOSFETs with SiO_2-gate insulators, the channel mobility is limited by Coulomb scattering mainly caused by the charges trapped at the deep states. On the other hand, in the n-channel MISFETs with deposited SiN_x/SiO_2 and the p-channel MISFETs with various gate insulators, other scattering mechanism may affect the channel mobility. For further improvement in channel mobility, it is important to clarify the other scattering mechanism.

The interface state density was estimated by using the gate-controlled diodes. By using the proposed method, the interface properties near the minority-carrier band edge can be characterized. The N_2O-grown oxides/4H-SiC (0001) interface state density near the conduction band edge evaluated by the n-channel MOSFETs was similar to that evaluated

by the n-MOS capacitors. In the p-channel MOSFETs, the interface state density was as low as $1 \times 10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ on the 4H-SiC $(03\bar{3}8)$ face.

Both n- and p-channel MISFETs with deposited insulators such as SiO_2 and SiN_x/SiO_2 adequately processed exhibited superior characteristics as in the case of MIS capacitors. In addition, the 4H-SiC $(000\bar{1})$, $(03\bar{3}8)$, and $(11\bar{2}0)$ faces are also attractive to enhance the MISFET performance.

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Chapter 5

Designing of SiC High-Voltage Lateral MISFETs

5.1 Introduction

SiC lateral power metal-insulator-semiconductor field-effect transistors (MISFETs) are the key component of the high-voltage power integrated circuits (ICs) for the advanced electronic systems [1], although most of the investigations on SiC power MISFETs have focused mainly on vertical-type structure. In the last decade, the performance of SiC lateral high-voltage MISFETs has shown gradual progress through the development of process technology. The fabricated high-voltage lateral metal-oxide-semiconductor FETs (MOSFETs) with nitrided-gate oxides [2, 3] and with buried-channel structure [4] and the MOSFETs fabricated on 4H-SiC $(000\bar{1})$ and $(11\bar{2}0)$ faces [5, 6] show reasonably high channel mobility and hence low channel resistance. On the other hand, the design of lateral high-voltage MISFETs, which strongly influences the blocking and conducting characteristics, has not been taken into account. In fact, the MOSFETs described above [2–6] have similar structure, called a reduced surface field (RESURF) structure [7].

The RESURF MISFETs have a lightly-doped n-type RESURF region near the drain region. By depleting the RESURF region, the RESURF MISFETs withstands high drain voltage. However, the RESURF MISFETs also show high drift resistance because the lightly-doped RESURF region acts as a resistor at the ON-state. The ON-resistance consists mainly of the channel resistance and the drift resistance. As mentioned above, the channel resistance has been decreased through the extensive development of SiC MIS technology. SiC lateral RESURF MOSFET, reported in 2005, showed a breakdown voltage of 1330 V and an ON-resistance of 67 $\mathrm{m\Omega cm^2}$ [3]. In this MOSFET, the ratio of drift resistance to the total ON-resistance was increased up to 50 %. Therefore, the reduction of drift resistance has become important even in SiC high-voltage lateral MISFETs for further improvement of the device performance.

The design of SiC lateral MISFETs is a critical issue that need to be tackled to reduce the

drift resistance, and for this reason, the new device concepts, which have not been adopted for the SiC MISFETs, should be introduced. In this chapter, double and triple RESURF structures [8, 9] are employed for further reduction of the drift resistance. The structure of SiC high-voltage lateral MISFETs is designed through fabrication and simulation of MISFETs.

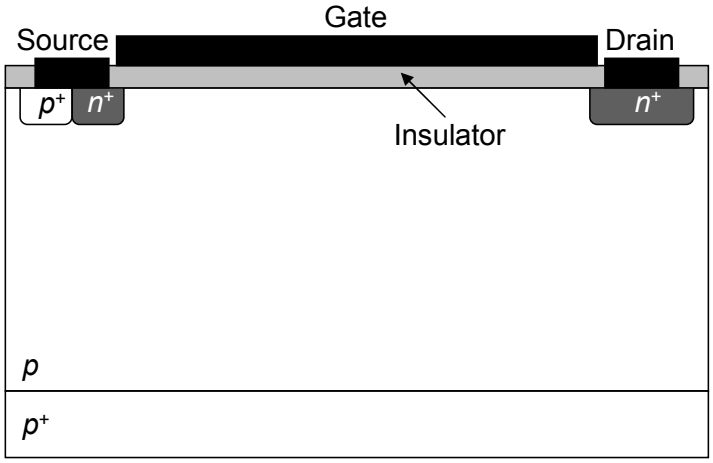
5.2 Device Structure and Concepts

5.2.1 Reduced Surface Field (RESURF) Structure

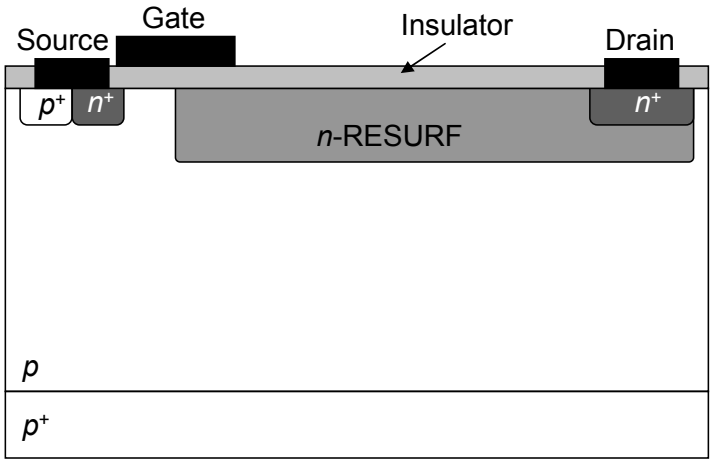
A RESURF structure is a promising type of lateral power MISFET [7]. Figure 5.1 shows schematic structures of (a) a normal planar MISFET and (b) a conventional RESURF MISFET. Compared with the planar MISFET (Fig. 5.1 (a)), a lightly-doped n-type RESURF region is formed near the drain region in the RESURF MISFET (Fig. 5.1 (b)). RESURF MISFETs exhibit high breakdown voltage by depleting the RESURF region.

RESURF Principle

Figure 5.2 shows the schematic structures of (a) a lateral double-diffused MISFET (LDMISFET), which is one of structures to obtain high breakdown voltage in the lateral MISFETs, and (b) the conventional RESURF MISFET. At the OFF-state, high blocking capability can be obtained by depleting the n-drift region in the LDMISFET and the n-RESURF region in the RESURF MISFET. In the LDMISFETs, the depletion region is extended from the vertical p-well/n-drift junction. At a low drain bias voltage (V_{D}) of V_{D1}, the electric field distribution at the surface of semiconductor (gate insulator/semiconductor interface) shows triangular distribution as shown in the middle graph of Fig. 5.2 (a). When the drain voltage is increased to V_{D2}, the shape of the electric field distribution at the semiconductor surface is kept triangular, although the absolute value of the electric field is increased (the upper graph of Fig. 5.2 (a)). The LDMISFETs break down when the maximum electric field at the p-well/n-drift junction ($E_{\mathrm{MAX,LD}}$) reaches the breakdown field of the semiconductor. The breakdown voltage of the LDMISFETs is determined from the doping concentration of the n-drift layer and the distance between the p-well and the drain region. On the other hand, in the RESURF MISFETs, the depletion region inside the RESURF region is laterally and vertically extended from the vertical and bottom p-epilayer/n-RESURF junctions, respectively. At a low drain bias voltage (V_{D}) of V_{D1}, the triangular-shaped distribution of the electric field is achieved at the surface of semiconductor as shown in the middle graph of Fig. 5.2 (b), as is the case with the LDMISFETs. However, after the RESURF region is fully depleted by the depletion layer vertically extended from the bottom p-epilayer/n-RESURF junction, the distribution of the electric field at the semiconductor surface becomes almost uniform except for the region near channel/RESURF junction when further drain voltage is applied. At a drain voltage of V_{D2}, which is higher than the voltage of a fully depleted



(a)



(b)

Figure 5.1: Schematic structures of (a) a normal planar MISFET and (b) a conventional RESURF MISFET. In the RESURF MISFET, a lightly-doped n-type RESURF region is formed near the drain region.

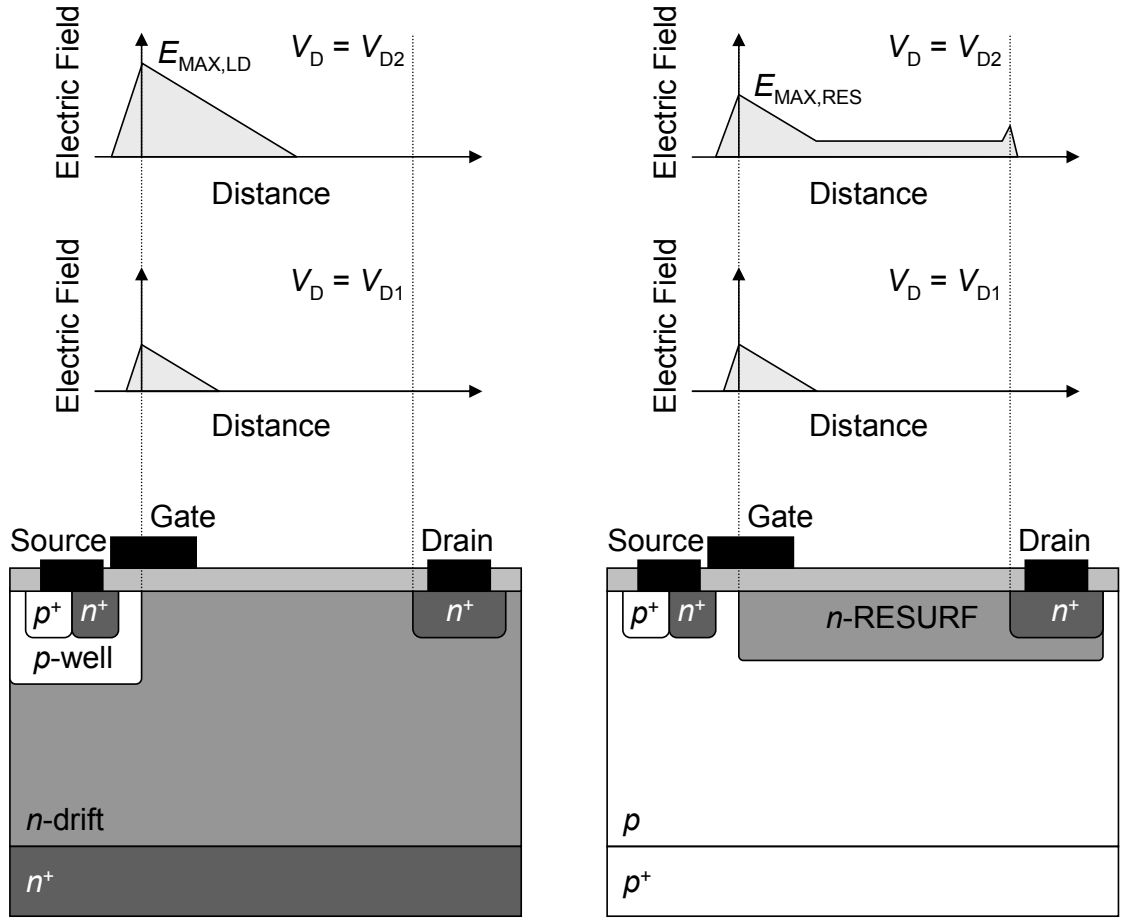


Figure 5.2: Schematic structures of (a) a conventional LDMISFET and (b) a conventional RESURF MISFET. The middle and upper graphs show the electric field distribution at the surface of semiconductor (MIS interface) at a low drain bias voltage of V_{D1} and a high drain voltage of V_{D2}, respectively.

RESURF region, the electric field distribution shown in the upper graph of Fig. 5.2 (b) is obtained. The maximum electric field at the junction ($E_{\mathrm{MAX,RES}}$) is lower than $E_{\mathrm{MAX,LD}}$ because a high drain voltage of V_{D2} can be supported by the fully-depleted RESURF region with almost uniform distribution of the electric field. Therefore, the RESURF MISFETs show higher breakdown voltage than LDMISFETs. In the RESURF MISFETs, the breakdown voltage is relatively insensitive to the doping concentration in the RESURF region and mainly determined from the lateral length of RESURF region because of its uniform electric field distribution. Note that the most important point is the full depletion of the RESURF region from the bottom p-epilayer/n-RESURF junction before the vertical pn junction breaks down. If the RESURF region can not be fully depleted, the breakdown voltage of RESURF MISFETs is decreased dramatically because the distribution of the electric field at the surface becomes triangular as in the case of LDMISFETs.

Two-Zone RESURF Structure

From the theoretical calculation[1], the maximum RESURF dose for 4H-SiC RESURF MISFETs can be increased to $1.1 \times 10^{13}\,\mathrm{cm}^{-2}$, which is about 10 times higher than that for Si RESURF MISFETs ($1.4 \times 10^{12}\,\mathrm{cm}^{-2}$). This is true only if the gate insulators do not break down before the avalanche breakdown occurs in SiC. The electric field under the gate edge is multiplied in the insulators by the ratio of the permittivity of SiC and the insulator ($\varepsilon_{\mathrm{SiC}}/\varepsilon_{\mathrm{i}}$, $\varepsilon_{\mathrm{SiC}}$: the permittivity of SiC, ε_{i}: the permittivity of the insulator). For example, at the SiO_2/SiC interface, the electric field of SiO_2 is about 2.5 times higher than that of SiC near the interface. It is likely that the insulator breakdown, which fatally damages the device, takes place in SiC RESURF MISFETs because the breakdown electric field of SiC (about 3 MV/cm) is much higher than that of Si. Therefore, the insulator breakdown must be suppressed in SiC RESURF MISFETs.

From this point of view, a two-zone RESURF structure is a very attractive approach to suppress the insulator breakdown [10]. The schematic structure of a two-zone RESURF MISFET is shown in Fig. 5.3. In the two-zone RESURF MISFETs, the RESURF region is divided into two regions, a lightly-doped RESURF1 region close to the gate edge and a highly-doped RESURF2 region close to the drain edge. If the insulator breakdown is eliminated, the breakdown of the RESURF MISFETs takes place mainly at the drain edge as shown in Fig. 5.3. To achieve a high breakdown voltage, it is important to reduce the electric field at both gate and drain edges.

The RESURF1 dose determines the maximum electric field at the gate edge since the field remains almost constant once the RESURF1 region is completely depleted. The electric field at the drain edge starts increasing only when RESURF2 zone is depleted, and hence the avalanche breakdown voltage is controlled by the RESURF2 dose. Therefore, the electric field at the gate and drain edges can be optimized independently to achieve high breakdown

[1]Details of the calculation are described in Appendix B.

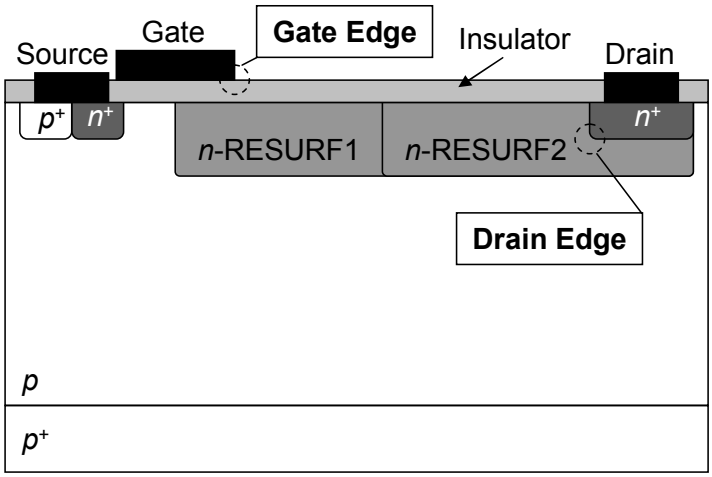


Figure 5.3: Schematic structure of a two-zone RESURF MISFET. The RESURF region is divided into two region, a lightly-doped RESURF1 region near the gate edge and a highly-doped RESURF2 region near the drain edge.

voltage. A higher breakdown voltage can be obtained in the two-zone RESURF MISFETs compared with the one-zone RESURF MISFETs.

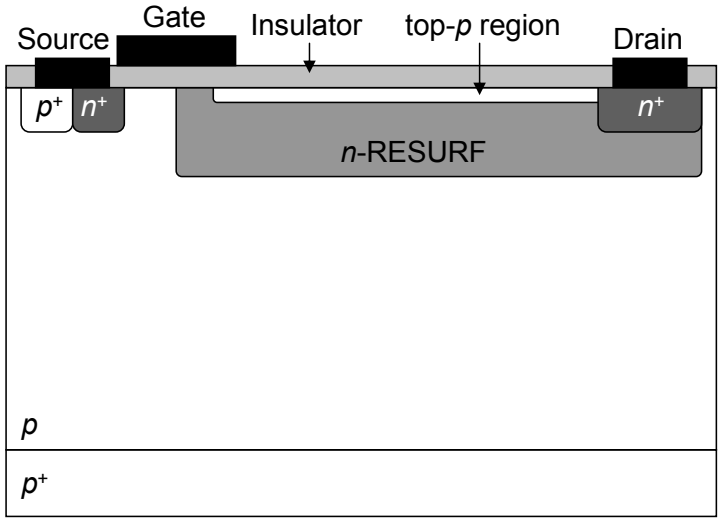
5.2.2 Double and Triple RESURF Structures

As previously mentioned, the reduction of drift resistance becomes important in SiC RESURF MISFETs. In terms of reduction of drift resistance, new device concepts such as a double RESURF structure [8] and a triple RESURF structure [9] should be added to the SiC RESURF MISFETs. Figure 5.4 shows the schematic structures of (a) double and (b) triple RESURF MISFETs. In both MISFETs, thin p-layer, which is named as top-p region in the double RESURF structure and buried-p region in the triple RESURF structure, is embedded in the RESURF region. Since the RESURF region is depleted not only from the bottom p-epilayer/n-RESURF interface but from n-RESURF/thin p-layer interface, a higher RESURF dose can be employed than single (normal) RESURF structure, leading to a lower drift resistance. The concepts of the double and triple RESURF structure are similar to "superjunction" concept [11].

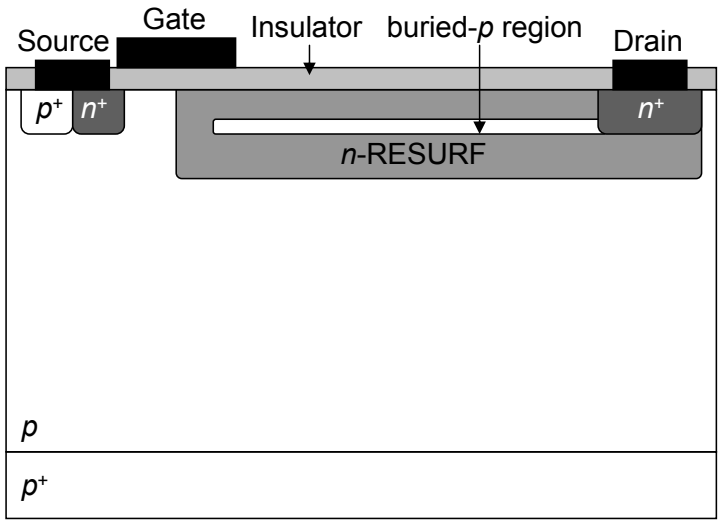
5.3 Experimental Comparison of Double and Triple RESURF MISFETs

5.3.1 Device Fabrication

To confirm which the effective structure to reduce the drift resistance in SiC high-voltage lateral MISFETs is, double and triple RESURF MISFETs were fabricated and compared. The double and triple RESURF MOSFETs with N_2O-grown oxides were fabricated on 10 μm-thick p-type 4H-SiC (0001) epilayers with an acceptor concentration (N_A) of $6 \times 10^{15}\,cm^{-3}$. The schematic structures of the fabricated double and triple RESURF MISFETs are shown in Fig. 5.5. The top-p and buried-p regions inside double and triple RESURF region, respectively, were formed by a self-aligned process as described in Section 6.2.2. Multiple N^+ implantations were carried out at room temperature (RT) to form a 0.6 μm-deep RESURF region. The total implant dose of N^+ (RESURF dose: D_{RES}) varied in the range from $2.6 \times 10^{12}\,cm^{-2}$ to $11.0 \times 10^{12}\,cm^{-2}$. The top-$p$ and buried-p regions were formed by multiple Al^+ implantations at RT. The total implant dose of Al^+ (top-p dose: D_{TP} for double RESURF MOSFETs and buried-p dose: D_{BP} for triple RESURF MOSFETs) varied in the range from $1.1 \times 10^{12}\,cm^{-2}$ to $8.5 \times 10^{12}\,cm^{-2}$. The typical doping profile in RESURF region was calculated by transport of ions in matter (TRIM) simulation. Figure 5.6 exhibits the concentration of implanted N^+ and Al^+ in RESURF region of (a) the double RESURF MOSFETs and (b) the triple RESURF MOSFETs. The source/drain regions and the p^+-contact region were formed by high-dose ($5 \times 10^{15}\,cm^{-2}$) P^+ implantation and high-dose ($4 \times 10^{15}\,cm^{-2}$) Al^+ implantation, respectively, at 300 °C. After ion implantation,

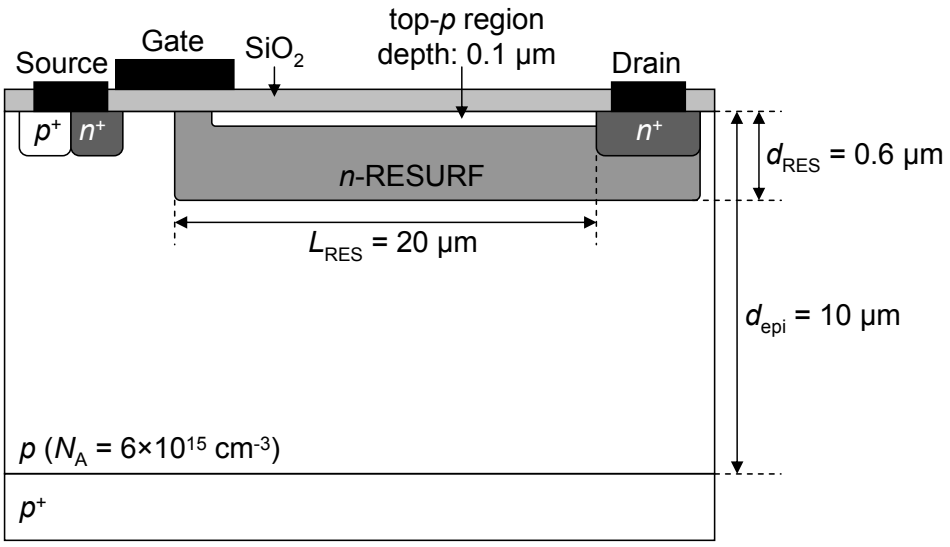


(a)

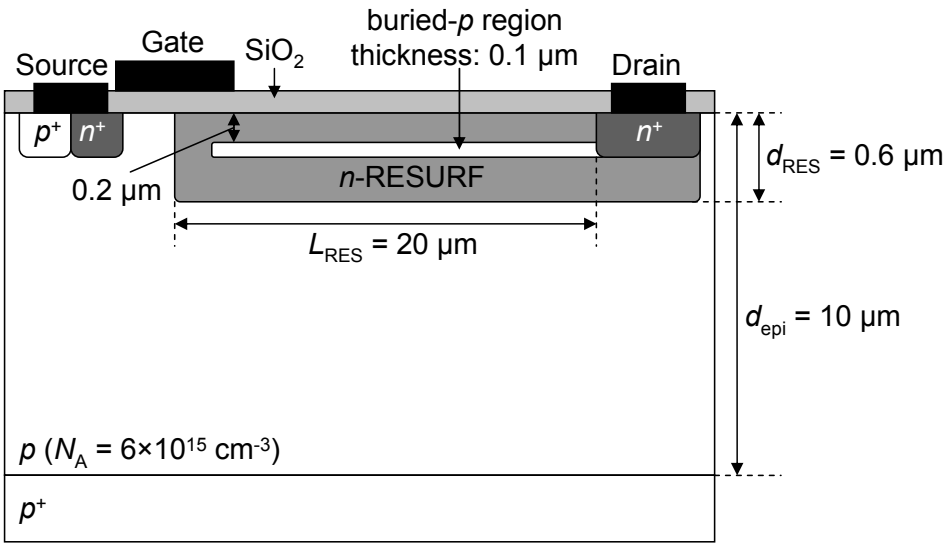


(b)

Figure 5.4: Schematic structures of (a) a double RESURF MISFET and (b) a triple RESURF MISFET.

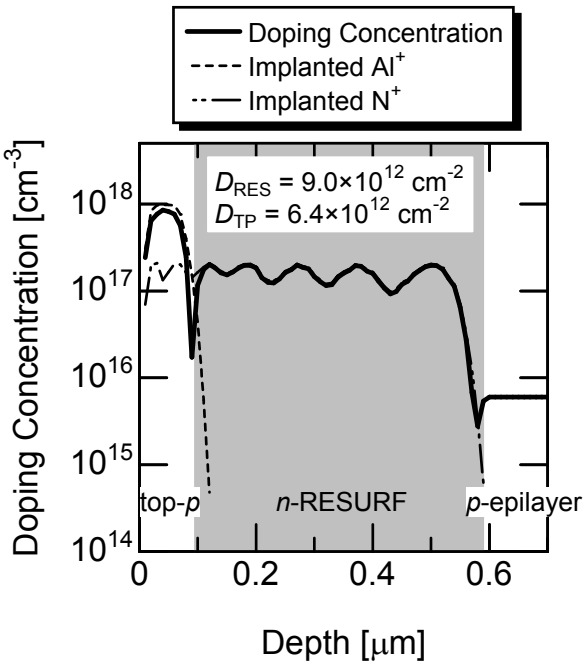


(a)

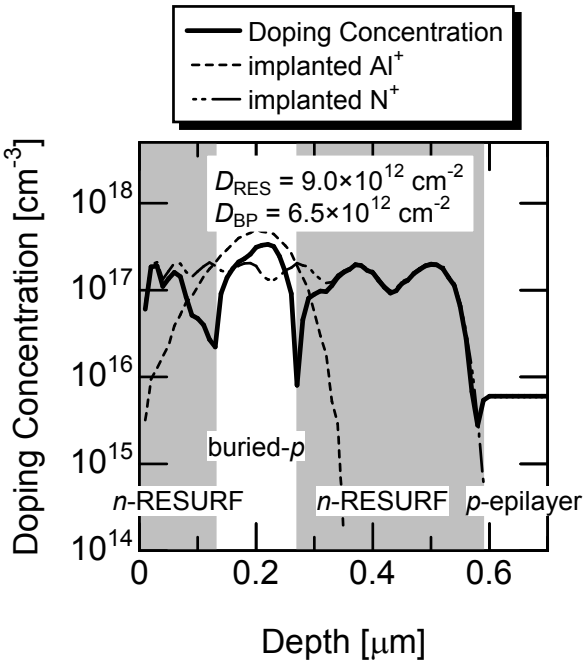


(b)

Figure 5.5: Schematic structures of the fabricated (a) double and (b) triple RESURF MOSFETs.



(a)



(b)

Figure 5.6: Depth profile of doping concentration, implanted Al^+ concentration, and implanted N^+ concentration in the RESURF region of (a) double RESURF MOSFET and (b) triple RESURF MOSFET. The RESURF dose of both MOSFETs is $9.0 \times 10^{12}\,\mathrm{cm}^{-2}$, the top-$p$ dose of the double RESURF MOSFET $6.4 \times 10^{12}\,\mathrm{cm}^{-2}$, and the buried-$p$ dose of the triple RESURF MOSFET $6.5 \times 10^{12}\,\mathrm{cm}^{-2}$.

high-temperature annealing was performed at 1700 °C for 20 min with a carbon cap [12]. After RCA cleaning, thermal oxidation was carried out in dry N_2O (10 % diluted in N_2) ambience at 1300 °C, followed by post-oxidation annealing in N_2 ambience at 1300 °C for 30 min [13, 14]. The thickness of gate oxide (d_{OX}) was about 55 nm. The source/drain and p^+-contact electrodes were Ni annealed at 950 °C for 3 min. The gate electrode was formed by Al. The typical channel length (L_{Ch}) and width (W) were 1–10 μm and 200 μm, respectively.

5.3.2 Device Characteristics

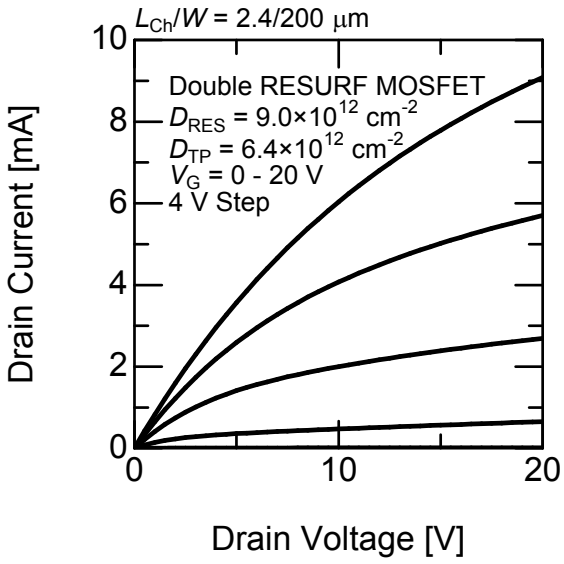
The fabricated RESURF MOSFETs exhibit good drain characteristics. Figure 5.7 shows the drain characteristics of the fabricated (a) double and (b) triple RESURF MOSFETs. The MOSFETs shown in Fig. 5.7 have a RESURF dose (D_{RES}) of $9.0 \times 10^{12}\,cm^{-2}$. The double and triple RESURF MOSFETs have a top-p dose (D_{TP}) of $6.4 \times 10^{12}\,cm^{-2}$ and a buried-p dose (D_{BP}) of $6.5 \times 10^{12}\,cm^{-2}$, respectively. Although these MOSFETs have similar RESURF doses, the drain current of the double RESURF MOSFET is higher than that of the triple RESURF MOSFET. The maximum breakdown voltage of these particular devices was 600 V.

Figure 5.8 shows the ON-resistance of the two different RESURF MOSFETs with a same RESURF dose ($D_{RES} = 9.0 \times 10^{12}\,cm^{-2}$) as a function of the channel length (L_{Ch}). As expected, the ON-resistance at a fixed effective oxide field ($(V_G - V_T)/d_{OX}$) of 2 MV/cm can be reduced by decreasing the channel length, owing to the decrease of MOS channel resistance. In general, the ON-resistance of a MOSFET can be expressed by the following equation:

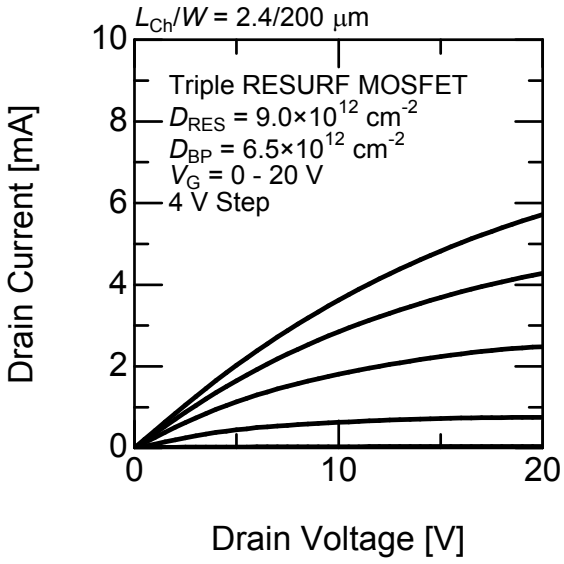
$$R_{ON} = \frac{L_{Ch} d_{OX}}{\mu_{Ch} W \varepsilon_{OX} (V_G - V_T)} + R_{RES} + R_C \tag{5.1}$$

where μ_{Ch} is the channel mobility, ε_{OX} the permittivity of the gate oxide, R_{RES} the RESURF resistance, and R_C the contact resistance. From Eq. 5.1, the intercept at the ordinate means the sum of the RESURF resistance and the contact resistance. The sum of the RESURF resistance and the contact resistance was estimated to be 0.54 kΩ (about 31 mΩcm^2) for the double RESURF MOSFETs and 1.50 kΩ (about 87 mΩcm^2) for the triple RESURF MOSFETs. Due to its high RESURF resistance, the drain current of the triple RESURF MOSFETs is lower than that of double RESURF MOSFETs as shown in Fig. 5.7. From the slope of the relationship between the ON-resistance and the channel length, the channel mobility can also be estimated by using Eq. 5.1. The estimated channel mobility was 25–30 cm^2/Vs for both MOSFETs.

Figure 5.9 shows the relationship between the *net* RESURF dose ($D_{RES} - D_{TP}$ for the double RESURF MOSFETs and $D_{RES} - D_{BP}$ for the triple RESURF MOSFETs) and the ON-resistance. In both RESURF MOSFETs, the increase in the *net* RESURF dose leads to the decrease in the ON-resistance because the RESURF resistance is reduced by increasing



(a)



(b)

Figure 5.7: Drain characteristics of the fabricated (a) double and (b) triple RESURF MOSFETs.

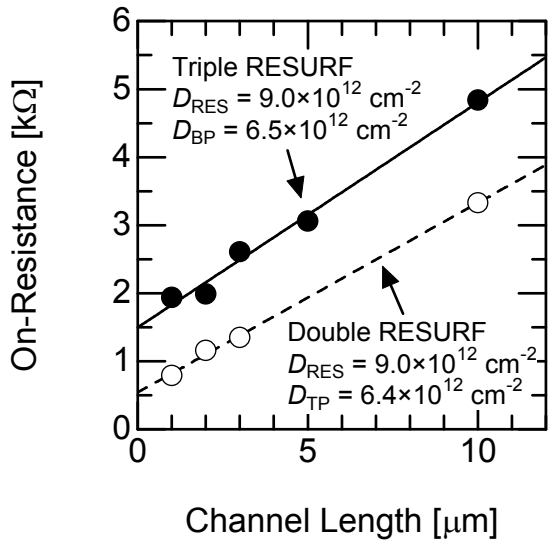


Figure 5.8: Channel length dependence of ON-resistance for 4H-SiC double and triple RESURF MOSFETs. Open and closed circles mean the ON-resistance of the fabricated double and triple RESURF MOSFETs, respectively.

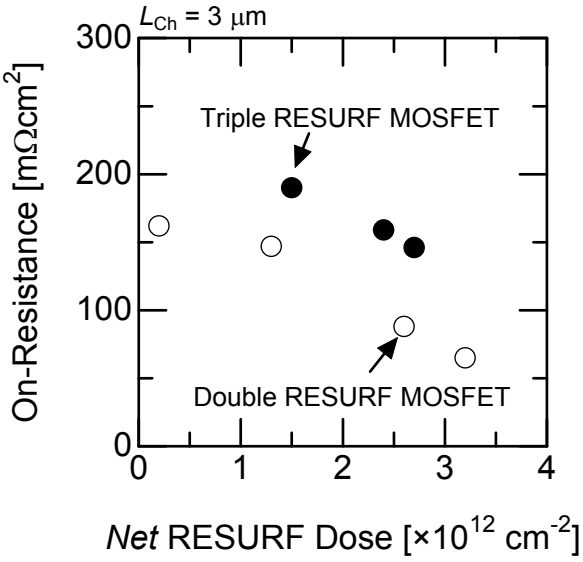


Figure 5.9: *Net* RESURF dose ($D_{\mathrm{RES}} - D_{\mathrm{TP}}$ for the double RESURF MOSFETs and $D_{\mathrm{RES}} - D_{\mathrm{BP}}$ for the triple RESURF MOSFETs) dependence of ON-resistance of the fabricated double and triple RESURF MOSFETs. Open and closed circles mean the ON-resistance of the fabricated double and triple RESURF MOSFETs, respectively.

the *net* RESURF dose. The double RESURF MOSFETs show lower drift resistance than the triple RESURF MOSFETs.

5.3.3 Superiority of Double RESURF Structure

From Figs. 5.7–5.9, it can be understood that double RESURF MOSFETs exhibit superior characteristics to triple RESURF MOSFETs. Triple RESURF MOSFETs show higher ON-resistance than double RESURF MOSFETs due to higher drift resistance. Figure 5.10 shows the structure of (a) double and (b) triple RESURF MOSFETs. In the double RESURF MOSFETs, the current path in the double RESURF region is wide (about 0.4–0.5 μm) and the drift resistance decreases. On the other hand, triple RESURF MOSFETs have very narrow current path in the triple RESURF region as shown in Fig. 5.10 (b). In particular, the thickness of current path located on the upper side of the buried-p region becomes very narrow because depletion layer is extended from the MOS interface due to high density of the negative charge located at the N_2O-grown SiO_2/n-SiC interface as discussed in Chapters 3 and 4. Thus, the high drift resistance was measured in the triple RESURF MOSFETs. In addition, the triple RESURF structure has a junction FET (JFET) region inside the RESURF region. The location of JFET region is indicated in Fig. 5.10 (b) as dashed circle. This is another reason for the high drift resistance in the triple RESURF MOSFETs.

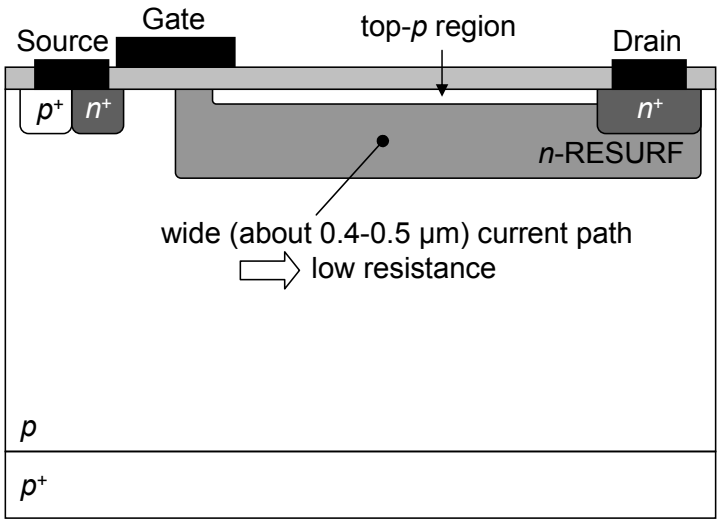
In the case of double RESURF structure, the top-p region is located at the top of the RESURF region and the depletion layer into the RESURF region from the MOS interface is not extended. For these reasons, double RESURF MOSFETs exhibit lower drift resistance than triple RESURF MOSFETs and are an attractive structure for the fabrication of lateral high-voltage MISFETs.

5.4 Device Simulation for Dose Optimization of Double RESURF MISFETs

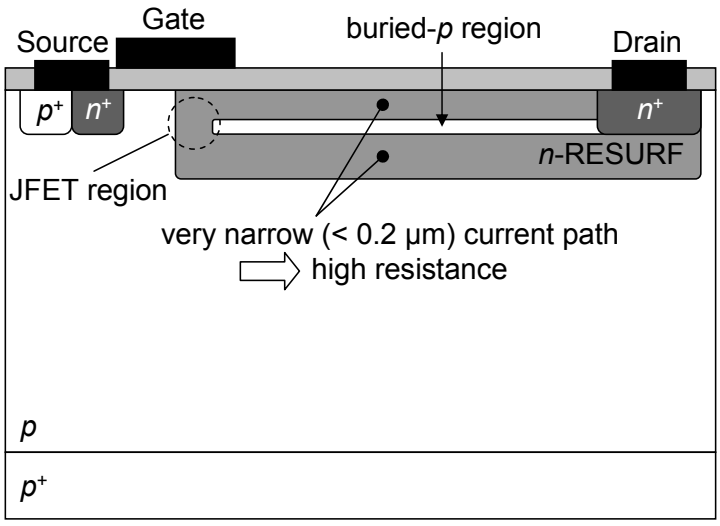
5.4.1 Two-Dimensional Device Simulator

The double RESURF structure is effective to decrease the drift resistance. To obtain high breakdown voltage, a careful design is strongly required. Therefore, the device structure was optimized by using two-dimensional device simulator (Synopsys-Technology Computer-Aided Design (TCAD)).

In the device simulation, the author defined the device with a two-dimensional structure and built a mesh by using the MDRAW software. In the defined device, size, materials, and doping concentration of each region can be set. After the structure was assumed, the MDRAW creates adequate mesh for device simulation. Then, the DESSIS software was used to simulate the electrical characteristics of the modeled device. In the DESSIS simulation,



(a)



(b)

Figure 5.10: Current path inside (a) double and (b) triple RESURF MOSFETs. Compared with the double RESURF MOSFETs, the triple RESURF MOSFETs have two narrow current path and JFET region.

the potential, the electric field, the carrier concentration, etc. at each node were calculated by using the finite element method. The results obtained after DESSIS simulation were then analyzed by using the INSPECT software (tool to create the graph such as I_{D}-V_{G} curves) and PICASSO software (tool to display the distribution of simulated parameters such as the potential, the electric field, etc.). In this calculation, a device simulated in two-dimension was assumed to have a thickness in the third dimension of 10 μm.

In this simulation, the author assumed an isotropic crystal, although 4H-SiC shows anisotropic physical properties. The gate insulator was SiO_2, and fixed charges at the SiO_2/SiC interface was neglected (if not specified). The important parameters used in this simulation are described as follows:

- Bandgap: 3.193 eV
- Relative Permittivity: 9.88
- Impact Ionization Coefficient [15]:

  for electron

$$\alpha_{\mathrm{n}} = 1.47 \times 10^6 \exp\left(-\frac{1.21 \times 10^7}{E}\right) \quad \mathrm{cm}^{-1} \tag{5.2}$$

  for hole

$$\alpha_{\mathrm{p}} = 5.52 \times 10^6 \exp\left(-\frac{1.27 \times 10^7}{E}\right) \quad \mathrm{cm}^{-1} \tag{5.3}$$

  E: electric field [V/cm]

- Electron Mobility [16]:

$$\mu_{\mathrm{n}} = \frac{947}{1 + \left(\dfrac{N}{1.94 \times 10^{17}}\right)^{0.61}} \quad \mathrm{cm}^2/\mathrm{Vs} \tag{5.4}$$

  N: impurity concentration [cm^{-3}]

5.4.2 Breakdown Voltage

By using two-dimensional device simulator, the optimum dose to achieve high breakdown voltage was estimated. The structure of the simulated double RESURF MOSFETs is shown in Fig. 5.11. To obtain a high breakdown voltage, the author employed the two-zone RESURF structure in addition to the double RESURF structure. The two-zone double RESURF MOSFET with a drift length of 20 μm (RESURF1 and RESURF2 lengths are 10 μm each) was employed for the simulation. The acceptor concentration of 10 μm-thick p-epilayer was fixed as $7.5 \times 10^{15}\,\mathrm{cm}^{-3}$, and a channel length of 3 μm and a gate oxide

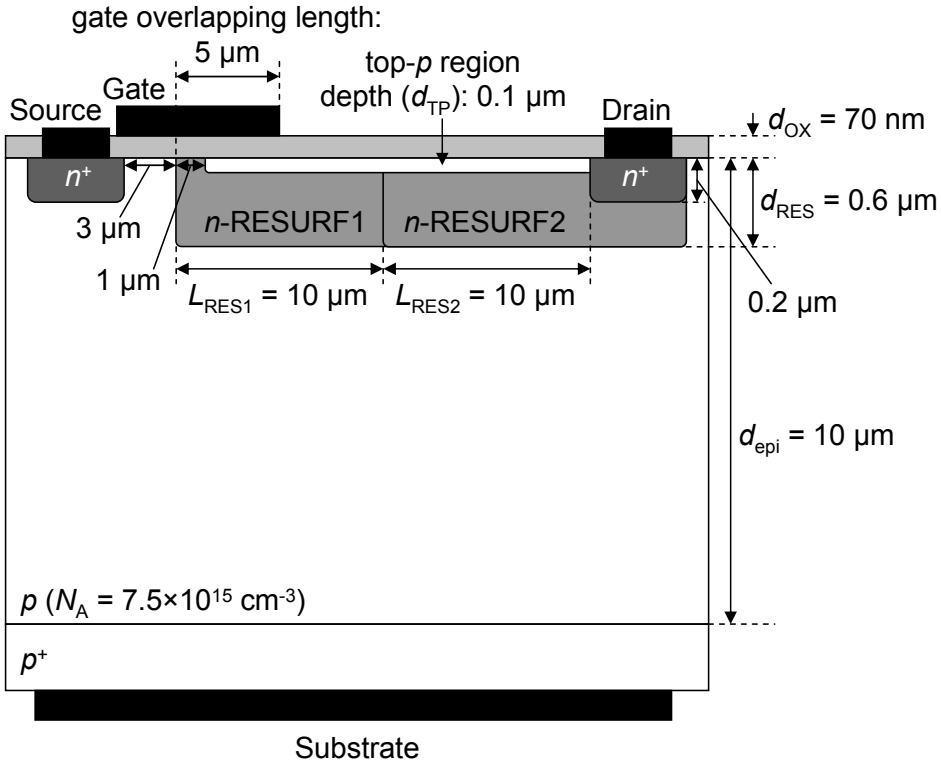
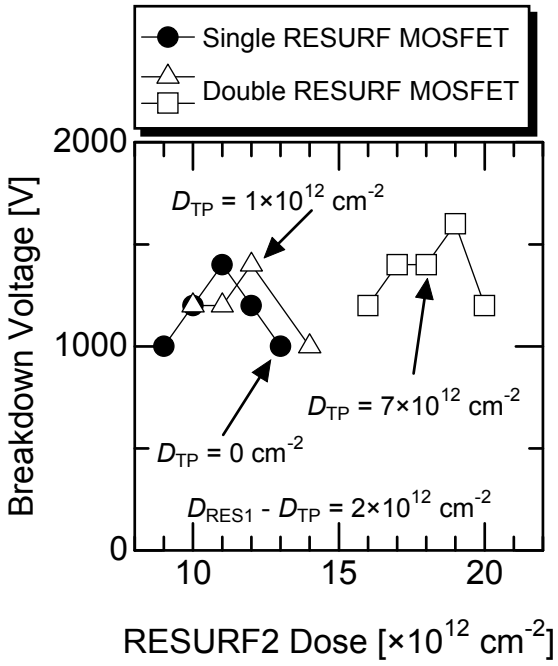


Figure 5.11: Schematic structure of a simulated two-zone double RESURF MOSFET to estimate breakdown voltage.

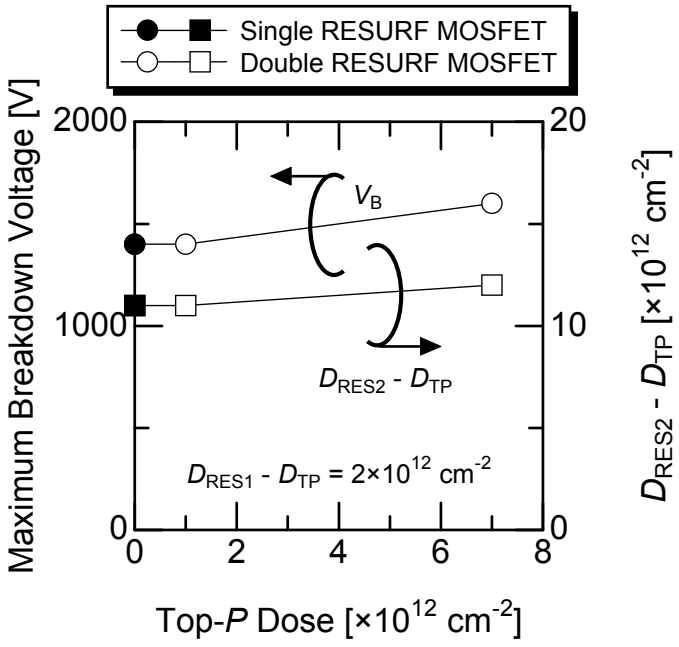
thickness of 70 nm were used. This MOSFET has a similar structure to the MOSFETs fabricated in the next chapter. In the simulation, the RESURF1, RESURF2, and top-p doses varied and any other parameters were not changed. The MOSFETs with top-p dose of $0\,\mathrm{cm}^{-2}$ mean the two-zone single RESURF MOSFETs in which the top-p region does not exist (single RESURF structure). In the breakdown analysis, the source, gate, and substrate contacts were grounded, and the drain voltage was increased. The breakdown voltage of the device was defined as the voltage at which the maximum electric field in SiC exceeds 3 MV/cm or that in SiO_2 becomes higher than 10 MV/cm.

Figure 5.12 (a) shows the RESURF2 dose (D_{RES2}) dependence of the breakdown voltage (V_{B}) at a fixed *net* RESURF1 dose ($D_{\mathrm{RES1}}-D_{\mathrm{TP}}$) of $2\times10^{12}\,\mathrm{cm}^{-2}$. The closed circles denote the breakdown voltage of SiC two-zone single RESURF MOSFETs (without top-p region), the open triangles that of SiC two-zone double RESURF MOSFETs with a top-p dose of $1\times10^{12}\,\mathrm{cm}^{-2}$, and the open boxes that of SiC two-zone double RESURF MOSFETs with a top-p dose of $7\times10^{12}\,\mathrm{cm}^{-2}$. From Fig. 5.12 (a), the simulated RESURF MOSFETs show a peak breakdown voltage at a certain RESURF2 dose. Figure 5.12 (b) represents the relationship between the maximum breakdown voltage and top-p dose for simulated MOSFETs with a fixed *net* RESURF1 dose of $2\times10^{12}\,\mathrm{cm}^{-2}$. In Fig. 5.12 (b), the *net* RESURF2 dose to obtain the maximum breakdown voltage is also indicated. From Fig. 5.12 (b), the maximum breakdown voltage (over 1.2 kV) is predicted at a *net* RESURF2 dose ($D_{\mathrm{RES2}}-D_{\mathrm{TP}}$) of about $11\times10^{12}\,\mathrm{cm}^{-2}$ regardless of the top-p dose. It is noted that the double RESURF MOSFETs show slightly high breakdown voltage compared with the single RESURF MOSFETs, the detail of which is described later. The breakdown voltage also depends on the *net* RESURF1 dose (not shown). The simulated breakdown voltage was mainly determined not by the individual doses but by the *net* RESURF1 dose ($D_{\mathrm{RES1}}-D_{\mathrm{TP}}$) and *net* RESURF2 dose ($D_{\mathrm{RES2}}-D_{\mathrm{TP}}$). From the results of device simulation, the optimum *net* RESURF1 and *net* RESURF2 doses for 4H-SiC two-zone double RESURF MOSFET with a drift length of 20 μm could be estimated to be $2\times10^{12}\,\mathrm{cm}^{-2}$ and $10\text{–}12\times10^{12}\,\mathrm{cm}^{-2}$, respectively. These results indicate that the drift resistance can be reduced by increasing the RESURF1, RESURF2, and top-p doses while keeping high breakdown voltage, as far as both the *net* RESURF1 dose and *net* RESURF2 dose are kept at the optimum values.

Figure 5.13 exhibits the equipotential lines for (a) the single RESURF MOSFET and (b) the double RESURF MOSFET at a drain voltage of 1000 V with zero-gate bias. The magnified plots of RESURF2 region in both MOSFETs are included in Fig. 5.13. In Fig. 5.13, the single RESURF MOSFET has a RESURF1 dose of $2\times10^{12}\,\mathrm{cm}^{-2}$ and a RESURF2 dose of $11\times10^{12}\,\mathrm{cm}^{-2}$. In the case of double RESURF MOSFET, a RESURF1 dose of $9\times10^{12}\,\mathrm{cm}^{-2}$, a RESURF2 dose of $18\times10^{12}\,\mathrm{cm}^{-2}$, and a top-$p$ dose of $7\times10^{12}\,\mathrm{cm}^{-2}$ are employed. Although the RESURF1 and RESURF2 doses of double RESURF MOSFET are much higher than those of the single RESURF MOSFET, difference in electric potential distribution is very small between the single and double RESURF MOSFETs. This result originates from that the *net* RESURF1 and *net* RESURF2 doses are the same, $2\times10^{12}\,\mathrm{cm}^{-2}$

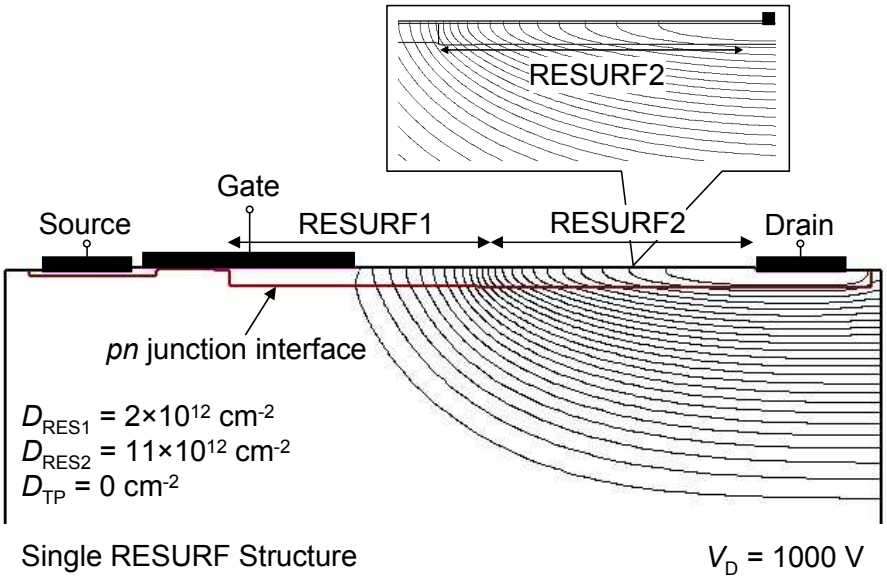


(a)

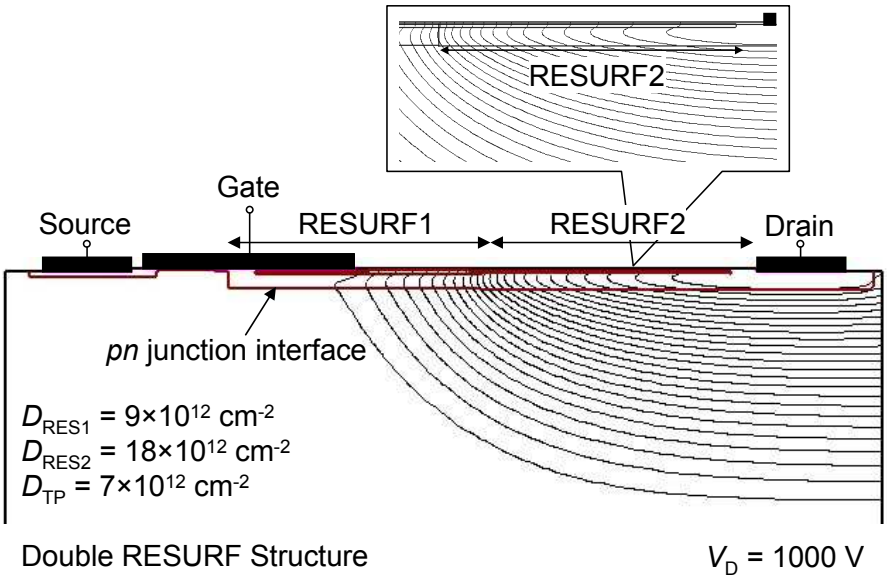


(b)

Figure 5.12: (a) RESURF2 dose (D_{RES2}) and (b) top-p dose dependence of maximum breakdown voltage simulated for two-zone double RESURF MOSFETs. In (b), the *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) to obtain the maximum breakdown voltage is also indicated as open and closed boxes (right vertical axis). In both cases, the *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) is fixed at $2 \times 10^{12}\,\mathrm{cm}^{-2}$. Closed symbols denote the characteristics of single RESURF MOSFET, and open symbols those of double RESURF MOSFETs.



(a)



(b)

Figure 5.13: Equipotential lines for 4H-SiC (a) single RESURF MOSFET and (b) double RESURF MOSFET. A drain voltage of 1000 V is applied. The step for the equipotential lines is 40 V. The magnified plots of RESURF2 region in both MOSFETs are also shown. Although the individual doses are different, the *net* RESURF1 and *net* RESURF2 doses are the same, which are $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $11 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively.

($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and $11 \times 10^{12}\,\mathrm{cm}^{-2}$ ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$), respectively, for these MOSFETs. Since the "*net* space charge" is the same for these devices due to charge compensation, the equipotential lines for the double RESURF MOSFETs are similar to those for the single RESURF MOSFET.

Figure 5.14 shows the electric field distribution in the RESURF region near the SiO_2/SiC interface for single and double RESURF MOSFETs. These MOSFETs have a *net* RESURF1 dose of $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and a *net* RESURF2 dose of $11 \times 10^{12}\,\mathrm{cm}^{-2}$, and have the same doses as the MOSFETs shown in Fig. 5.13. In most of the region, the electric field distribution for the double RESURF MOSFET is comparable with that for the single RESURF MOSFET in spite of higher RESURF doses. The top-p region suppresses the increase of electric field at the SiO_2/SiC interface. The electric field near the channel region (about $1\,\mu$m from the channel region) of the double RESURF MOSFET is higher than that of the single RESURF MOSFET. The high electric field near the channel region in the double RESURF MOSFET can be ascribed to the relatively high electric potential region, compared with single RESURF MOSFET, extended from the drain region due to its high RESURF doses.

As previously mentioned, it is interesting to note that the double RESURF structure is also effective to achieve high breakdown voltage in addition to the reduction of drift resistance. Figure 5.15 (a) illustrates the structure of the double RESURF MOSFETs, in which the gate edge is indicated by dashed circle. The relationship between the electric field at the gate edge and the RESURF1 dose is shown in Fig. 5.15 (b). In Fig. 5.15 (b), the *net* RESURF1 and *net* RESURF2 doses are fixed at $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $11 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. Closed circle denotes the single RESURF MOSFETs ($D_{\mathrm{TP}} = 0\,\mathrm{cm}^{-2}$), and open circles denote the double RESURF MOSFETs ($D_{\mathrm{TP}} > 0\,\mathrm{cm}^{-2}$). A drain voltage of 1000 V is applied with zero-gate bias. As shown in Fig. 5.15 (b), the gate oxide field at the gate edge is remarkably decreased in the double RESURF MOSFETs. Figure 5.16 shows the electric potential distribution under the gate edge from the SiO_2/SiC interface to (a) $1\,\mu$m-deep and (b) $0.05\,\mu$m-deep locations. From Fig. 5.16 (a), the higher electric potential is observed in the RESURF region with higher RESURF doses because high electric potential region can be easily extended from the drain region due to its high RESURF doses. On the other hand, from Fig. 5.16 (b), the electric potential near the SiO_2/SiC interface is reduced by increasing the RESURF dose. The top-p region in the double RESURF structure protects the gate oxide from high electric field in the OFF-state because the electric potential at the MOS interface is reduced by the existence of top-p/n-RESURF junction. Therefore, the double RESURF structure is effective to suppress the oxide breakdown and to achieve high breakdown voltage.

5.4.3 Drift Resistance

After the simulation to evaluate the breakdown voltage of RESURF MOSFETs, another simulation program was employed to estimate the drift resistance of double RESURF MOS-

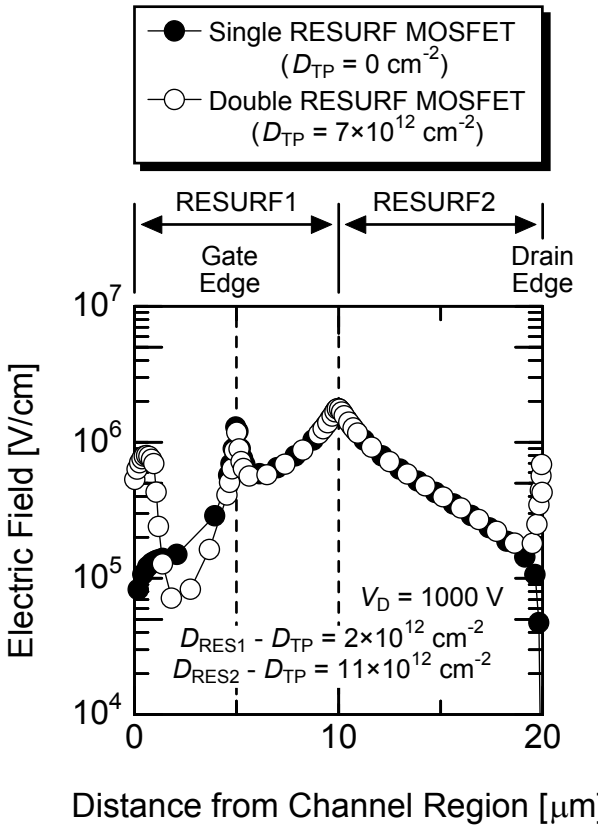
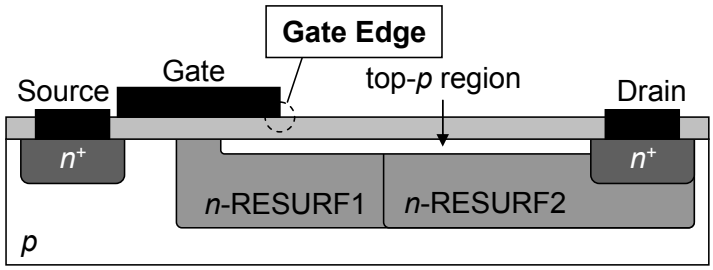
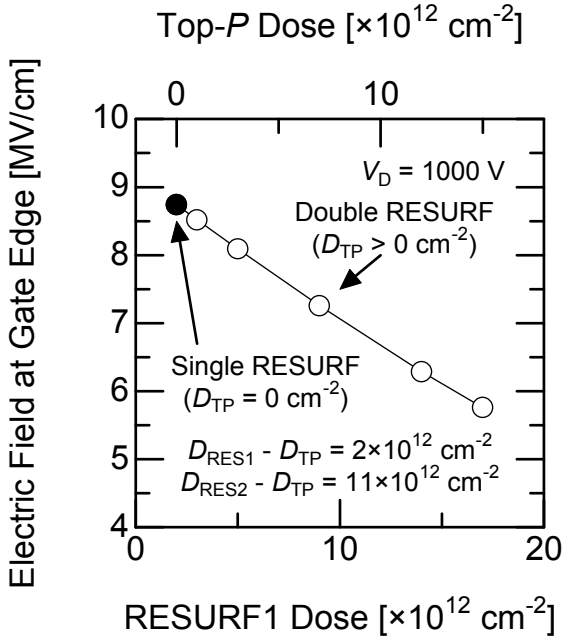


Figure 5.14: Electric field distribution in the RESURF region near the SiO_2/SiC interface from the edge of channel to the drain for single and double RESURF MOSFETs. A drain voltage of 1000 V is applied. The *net* RESURF1 and *net* RESURF2 doses are fixed at $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $11 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. Closed circles represent the single RESURF MOSFET with a top-p dose (D_{TP}) of $0\,\mathrm{cm}^{-2}$ and open circles the double RESURF MOSFET with a top-p dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$.

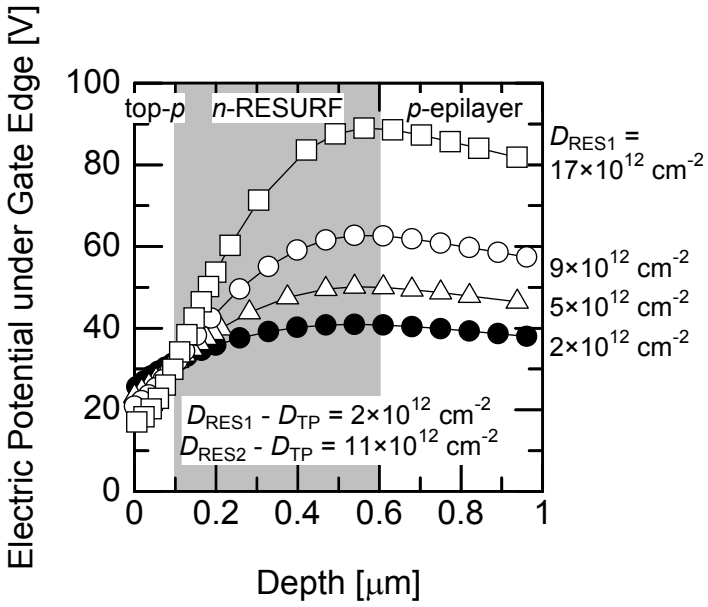


(a)

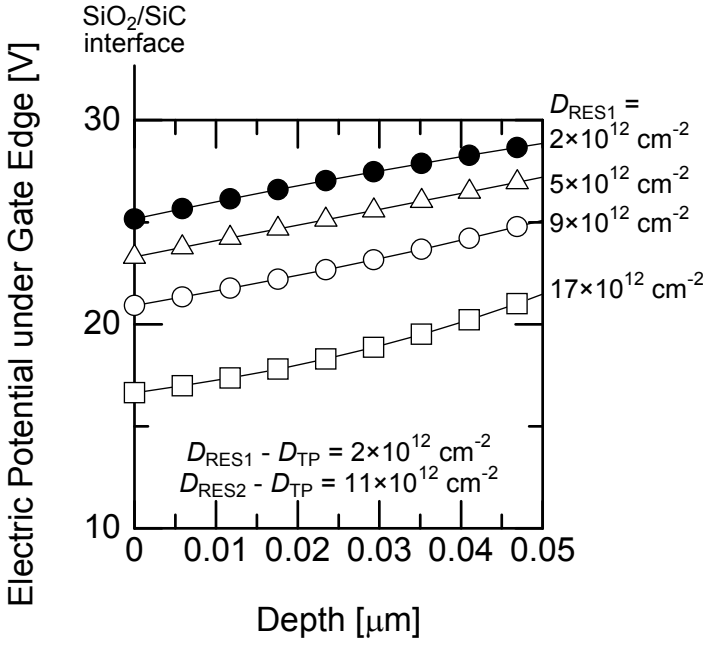


(b)

Figure 5.15: (a) Structure of double RESURF MOSFETs. Dashed circle indicates the gate edge. (b) RESURF1 dose dependence of electric field at the gate edge. The upper axis shows the top-p dose. Closed circle denotes the single RESURF MOSFET, and open circles denote the double RESURF MOSFETs. The *net* RESURF1 dose and the *net* RESURF2 dose are fixed at $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $11 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. A drain voltage of 1000 V is applied with zero-gate bias.



(a)



(b)

Figure 5.16: Electric potential distribution under the gate edge from the gate oxide/SiC interface to (a) 1 μm-deep and (b) 0.05 μm-deep locations. Closed circles mean the single RESURF MOSFETs, and open symbols the double RESURF MOSFETs.

FETs. Figure 5.17 shows the structure of the simulated device. This test elementary group (TEG) device has a similar structure to the RESURF MOSFET, except for channel region. In the TEG device, the RESURF1 region is shorted to the source region. Therefore, the channel resistance component can be neglected, and the ON-resistance of the TEG device is almost equal to the drift resistance of the RESURF MOSFET. The TEG device has a drift length of 20 μm (RESURF1 and RESURF2 lengths are 10 μm each). In the next chapter, the drift resistance of the fabricated MOSFETs will be estimated by using the characteristics of the fabricated TEG devices which have the similar structure to simulated TEG devices. As is the case with the simulation for estimation of breakdown voltage, the RESURF1, RESURF2, and top-p doses were varied and any other parameters were not changed. In this simulation, a drain voltage of 0.1 V was applied, and the gate voltage was changed from 0 V to 30 V. The source and substrate contacts were grounded. The drift resistance was calculated from the simulated drain current obtained at a gate oxide field of 3 MV/cm, at which the gate bias voltage becomes 21 V.

Figure 5.18 shows (a) the RESURF1 dose (D_{RES1}) and (b) the *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) dependence of the drift resistance for the TEG devices with a *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) of $11 \times 10^{11}\,\mathrm{cm}^{-2}$. From Fig. 5.18 (a), the drift resistance was decreased by increasing RESURF1 dose regardless of top-p dose. The increase of RESURF1 dose leads to the increase of the carrier concentration in the RESURF1 region and to the decrease of the drift resistance. From Fig. 5.18 (b), the TEG devices with a top-p dose of $1 \times 10^{12}\,\mathrm{cm}^{-2}$ (double RESURF structure) show higher drift resistance than that with a top-p dose of $0\,\mathrm{cm}^{-2}$ (single RESURF structure). The top-p region in the double RESURF structure narrows current pathway because the current can not flow the top-p region at the ON-state. In the case of low top-p dose, the influence of narrowing the current pathway balances out the effects of high RESURF dose in the double RESURF region because the increment of carrier concentration in the double RESURF region is very low. Thus, the drift resistance of double RESURF structure with a low top-p dose becomes higher than that of single RESURF structure. In the case of high top-p dose, however, the drift resistance of the double RESURF structure can be significantly decreased to below that of the single RESURF structure. The TEG devices with double RESURF structure, which has a top-p dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$, exhibit a low drift resistance below $15\,\mathrm{m\Omega cm}^2$, compared with a drift resistance of the TEG device with the single RESURF structure (about 20–80 $\mathrm{m\Omega cm}^2$). Compared with the single RESURF structure, the *net* RESURF1 dose dependence of the drift resistance is small in the double RESURF structure (Fig. 5.18 (b)). When the *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) was changed from $1 \times 10^{12}\,\mathrm{cm}^{-2}$ to $3 \times 10^{12}\,\mathrm{cm}^{-2}$, the absolute value of the RESURF1 dose was almost the same in the double RESURF structure with a top-p dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$ (RESURF1 dose was changed from $8 \times 10^{12}\,\mathrm{cm}^{-2}$ to $10 \times 10^{12}\,\mathrm{cm}^{-2}$, which is 25 % difference). Therefore, the double RESURF structure with high RESURF doses showed a small RESURF1 dose dependence of the drift resistance.

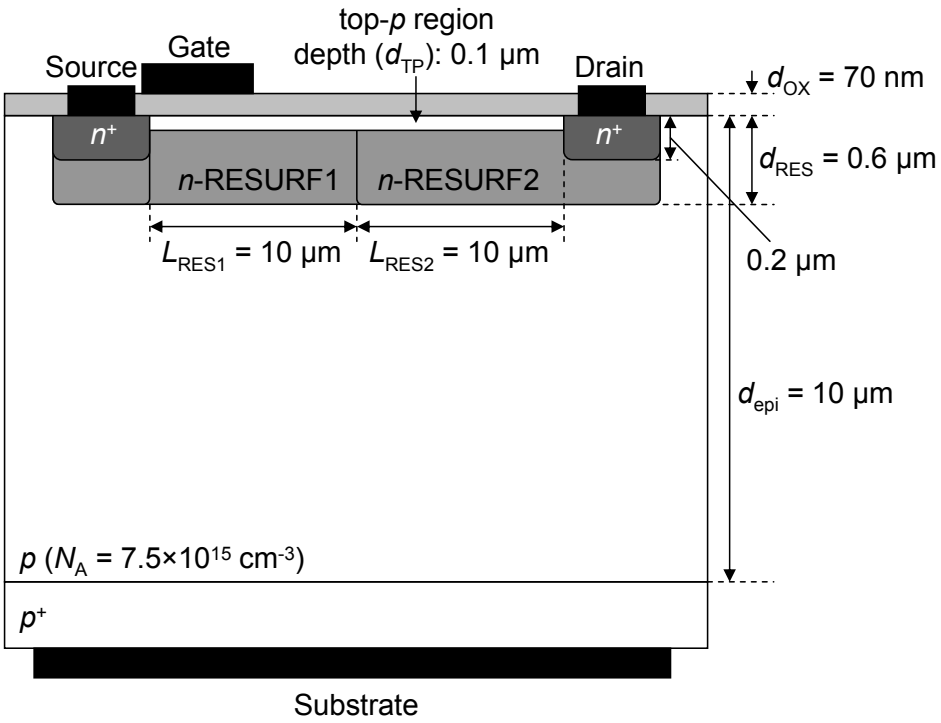
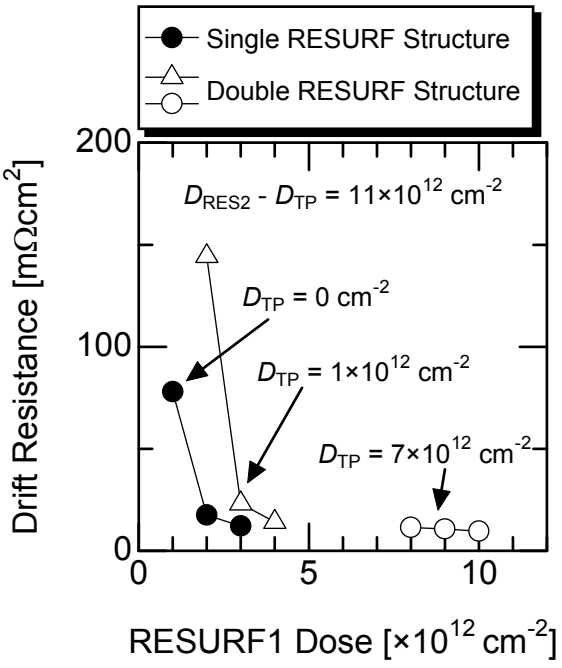
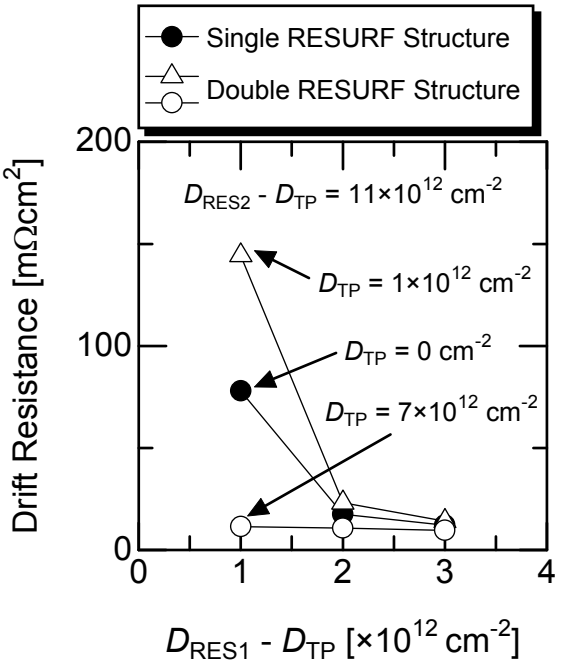


Figure 5.17: Schematic structure of a simulated TEG device to estimate the drift resistance. In the TEG device, the RESURF1 region is shorted to the source region. Therefore, the channel resistance component can be negligible, and the ON-resistance of the TEG device is almost equal to the drift resistance of the RESURF MOSFET with the same RESURF doses.



(a)



(b)

Figure 5.18: (a) RESURF1 dose (D_{RES1}) and (b) *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) dependences of the drift resistance simulated for TEG devices. Closed circles denote the breakdown voltage of TEG devices with single RESURF structure, and open symbols that of TEG devices with double RESURF structure. In both cases, the *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) is fixed at $11 \times 10^{12}\,\mathrm{cm}^{-2}$.

5.5 Discussion

Compared with the single and triple RESURF MISFETs, double RESURF MISFETs are effective to reduce the drift resistance as described in Section 5.4.3. In addition, the double RESURF is an attractive structure for suppressing the insulator breakdown and to achieve high breakdown voltage. The gate insulators in the single and triple RESURF MISFETs are not effectively protected from the high electric potential. Therefore, the double RESURF MISFET will be the best structure to achieve both high breakdown voltage and low drift resistance.

In the simulation, a two-zone double RESURF MISFET was employed. The one-zone double RESURF structure was also simulated to compare with the two-zone double RESURF structure. Although the detailed analyses were described elsewhere [17], the optimum *net* RESURF dose ($D_{\mathrm{RES}} - D_{\mathrm{TP}}$) was estimated to be $4 \times 10^{12}\,\mathrm{cm}^{-2}$. The one-zone single RESURF MISFETs with an optimum *net* RESURF dose show a simulated breakdown voltage of 600 V. By using two-zone RESURF structure, the simulated breakdown voltage was increased to more than 2 times higher value, over 1.2 kV.

Figure 5.19 demonstrates the RESURF1 dose dependence of the drift resistance and breakdown voltage simulated for the two-zone double RESURF MISFETs. The simulated MISFETs shown in Fig. 5.19 have an optimum RESURF1 dose of $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and an optimum RESURF2 dose of $11 \times 10^{12}\,\mathrm{cm}^{-2}$. The top-$p$ dose to keep the optimum *net* doses is also shown in the upper axis of Fig. 5.19. Figure 5.19 clearly exhibits the advantage of the double RESURF structure over the single RESURF structure. The drift resistance can be decreased to lower than $10\,\mathrm{m\Omega cm}^2$ by increasing the RESURF1, RESURF2, and top-p doses (D_{RES1}, D_{RES2}, and D_{TP}, respectively) while keeping the same *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$), although too low RESURF doses increase the drift resistance. In terms of breakdown voltage, double RESURF MISFETs with the optimum *net* RESURF doses show a high breakdown voltage of 1.4 kV. However, the breakdown voltage is decreased when the RESURF doses are too high. For example, when the RESURF1, RESURF2, top-p doses are $22 \times 10^{12}\,\mathrm{cm}^{-2}$, $31 \times 10^{12}\,\mathrm{cm}^{-2}$, and $20 \times 10^{12}\,\mathrm{cm}^{-2}$ (*net* RESURF1 and *net* RESURF2 doses are "optimum", $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $11 \times 10^{12}\,\mathrm{cm}^{-2}$), respectively, the breakdown voltage is reduced to about 500 V because electric field crowding takes place at the top-p/drain and/or top-p/RESURF junctions. It is also likely that the insulator breakdown occurs when the RESURF doses are too high because the electric field was increased near the channel region as shown in Fig. 5.14. Therefore, the RESURF1 dose should be kept within the range from $9 \times 10^{12}\,\mathrm{cm}^{-2}$ to $17 \times 10^{12}\,\mathrm{cm}^{-2}$ (corresponding top-p dose: 7–15 $\times 10^{12}\,\mathrm{cm}^{-2}$) to obtain a high breakdown voltage over 1.2 kV and a low drift resistance below $15\,\mathrm{m\Omega cm}^2$.

In Section 5.4.2, the optimum *net* RESURF1 and *net* RESURF2 doses were estimated to be $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and 10–12 $\times 10^{12}\,\mathrm{cm}^{-2}$, respectively. When the RESURF doses get out of the optimum value, the breakdown voltage of double RESURF MISFETs is decreased.

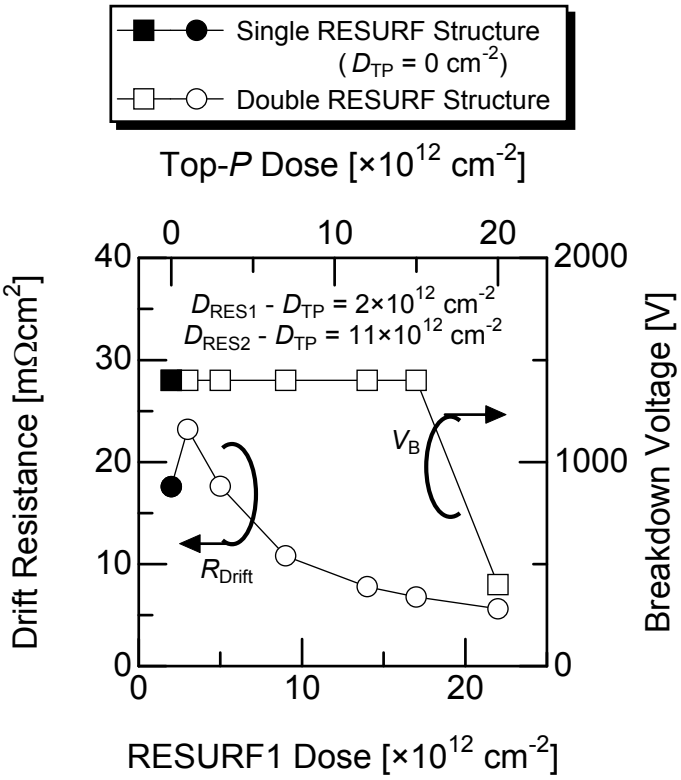


Figure 5.19: RESURF1 dose dependence of drift resistance and breakdown voltage for the simulated SiC RESURF MOSFETs. Open and closed circles represent the drift resistance, and open and closed boxes represent the breakdown voltage. Closed symbols denote the characteristics of single RESURF MOSFETs, and open symbols those of double RESURF MOSFETs. The *net* RESURF1 and *net* RESURF2 doses are fixed at $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $11 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. The top-$p$ dose to keep the optimum *net* doses is indicated at the top of the plot.

When double RESURF MISFETs have lower RESURF doses than the optimum doses, the breakdown occurs at the drain edge because the electric potential is hardly extended from the drain region and electric field crowding takes place at the drain edge. On the other hand, the high RESURF doses lead to insulator breakdown because the high electric potential is easily extended from the drain region to the region under the gate edge. To ensure the reliability of the device operation, the insulator breakdown must be avoided. Therefore, the actual RESURF MISFETs should have lower RESURF doses than the optimum value from the standpoint of the suppression of the insulator breakdown.

In a previous work [3], the blocking characteristics of RESURF MOSFETs are influenced by the effective fixed charges at the SiO_2/SiC interface. In the case of single RESURF MISFETs, there are negative charges at the SiO_2/n-RESURF interface because of electron trapping to interface states. These negative charges terminate the electric force lines from the ionized donor in the RESURF region, causing depletion from the SiO_2/SiC interface. Thus, the effective density of ionized donors in the RESURF region is reduced, indicating a decrease of the effective RESURF dose. Therefore, high RESURF doses, compared with the optimum RESURF doses, are required in the single RESURF MISFETs to ensure optimum device performance. On the other hand, in the case of double RESURF MISFETs, the interface is formed by SiO_2/top-p region. There are positive charges at the MIS interface, as discussed in Chapters 3 and 4. The positive charges reduce the effective density of ionized acceptors in the top-p region. The decrease in effective density of ionized acceptors in the top-p region leads to the increase in effective RESURF doses because a portion of ionized donors can not cancel out the ionized acceptors in the top-p region. To keep the *net* RESURF doses optimum, the RESURF doses should be lower than the optimum RESURF doses.

5.6 Summary

The structure of high-voltage lateral MISFETs was designed, and the breakdown voltage and the drift resistance were analyzed. The author employed two different structures to reduce drift resistance, double RESURF structure and triple RESURF structure.

From the characteristics of the fabricated double and triple RESURF MOSFETs, the double RESURF structure was favorable for the reduction of the drift resistance. The narrow JFET region inside triple RESURF region caused high drift resistance.

From the device simulation, the breakdown voltage of the two-zone double RESURF MOSFETs depends not on individual doses themselves (D_{RES1}, D_{RES2}, and D_{TP}) but on the *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and the *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$). The optimum *net* RESURF1 dose and *net* RESURF2 dose were $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $10\text{–}12 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. The advantages of double RESURF structure over the single RESURF structure were revealed after the simulation. The drift resistance can be

decreased to below $15\,\mathrm{m\Omega cm^2}$ by increasing RESURF doses while the *net* RESURF1 and *net* RESURF2 doses were kept at the optimum value, although too low RESURF doses increase the drift resistance. The top-p region protects the gate oxide at the OFF state. The breakdown voltage was kept over 1.2 kV in the double RESURF MISFETs with the optimum *net* RESURF doses when the RESURF doses were not too high. Too high RESURF doses cause the breakdown at the gate insulator and/or inside double RESURF region. Therefore, the double RESURF MISFETs with the optimum RESURF doses exhibit high breakdown voltage and low drift resistance, as far as the top-p dose were varied in the range from $7 \times 10^{12}\,\mathrm{cm^{-2}}$ to $15 \times 10^{12}\,\mathrm{cm^{-2}}$.

In the next chapter, the fabrication and characterization of two-zone double RESURF MISFETs will be explained. To suppress the insulator breakdown, the RESURF doses in the fabricated MISFETs should be slightly lower than the optimum RESURF doses obtained from the device simulation.

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Chapter 6

Fabrication and Characterization of SiC Double RESURF MISFETs

6.1 Introduction

In Chapter 5, preliminary fabrication and simulations demonstrated that the double reduced surface field (RESURF) metal-insulator-semiconductor field-effect transistors (MISFETs) are a promising structure not only for decreasing ON-resistance but also for increasing breakdown voltage in lateral power devices. In this chapter, double RESURF MISFETs are fabricated and characterized. In the fabrication, a self-aligned process to form top-p region is proposed. In the fabricated double RESURF MISFETs, the ON-resistance is significantly decreased due to its low drift resistance. The fabricated MISFETs with two-zone double RESURF structure exhibit superior characteristics to lateral high-voltage MISFETs previously reported. From the experimental results, additional advantages of the double RESURF structure are found. The fabricated 4H-SiC double RESURF MISFETs demonstrate a record performance among any lateral MISFETs ever reported.

6.2 Device Fabrication

6.2.1 Fabrication Process of Double RESURF MISFETs

RESURF metal-oxide-semiconductor FETs (MOSFETs) were fabricated on 15 μm-thick p-type 4H-SiC (0001) epilayers with an acceptor concentration (N_{A}) of $8 \times 10^{15}\,\mathrm{cm}^{-3}$. The structure of the fabricated MOSFETs are shown in Fig. 6.1. The top-p region of double RESURF MOSFETs was formed by using a self-aligned process explained in Section 6.2.2. Multiple N^+ implantations were carried out at room temperature (RT) to form 0.6 μm-deep RESURF1 and RESURF2 regions. The total implant doses of N^+ to form the RESURF1 and RESURF2 regions (RESURF1 dose (D_{RES1}) and RESURF2 dose (D_{RES2}), respectively) varied in the range from $1 \times 10^{12}\,\mathrm{cm}^{-2}$ to $21 \times 10^{12}\,\mathrm{cm}^{-2}$ and in the range from $9 \times 10^{12}\,\mathrm{cm}^{-2}$

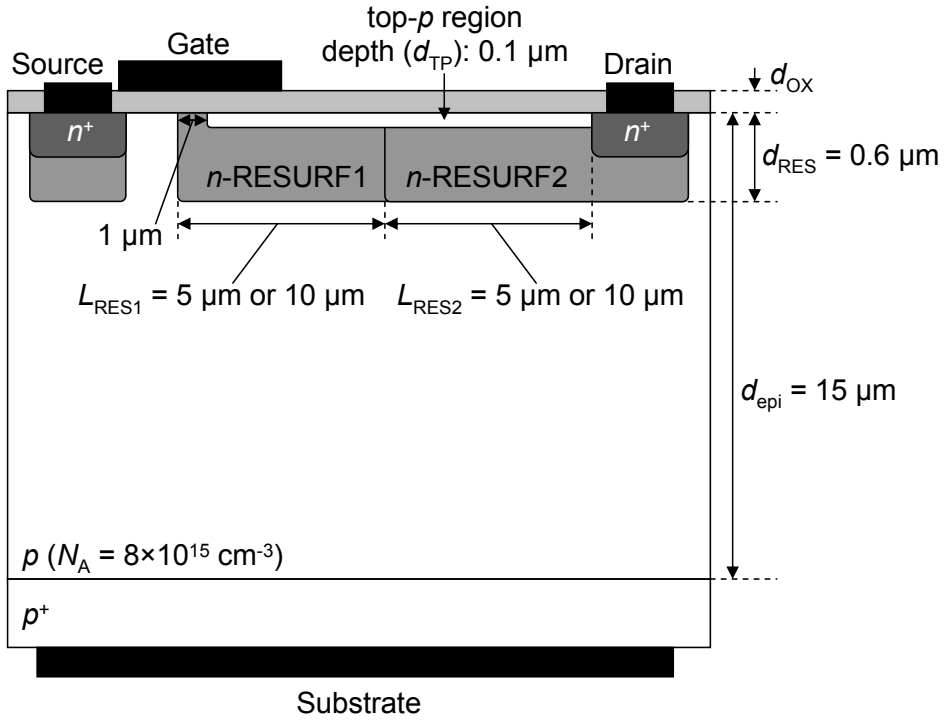


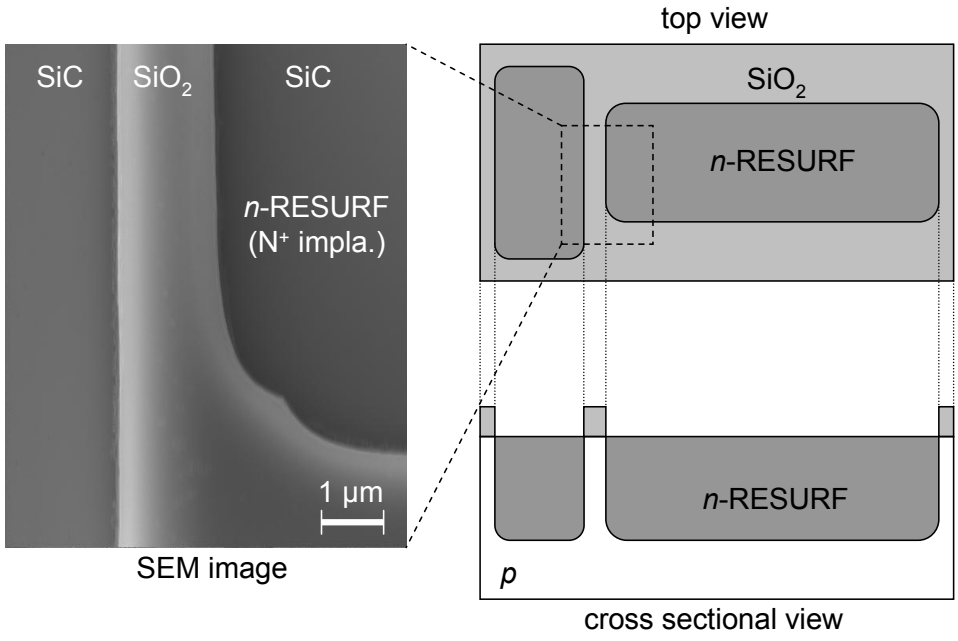
Figure 6.1: Schematic structure of a SiC two-zone double RESURF MISFET.

to $29 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. The $0.1\,\mu$m-deep top-p region was formed by multiple Al^+ implantations at RT. The total implant dose of Al^+ (top-p dose (D_{TP})) varied in the range from $3 \times 10^{12}\,\mathrm{cm}^{-2}$ to $20 \times 10^{12}\,\mathrm{cm}^{-2}$. The *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and the *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) were fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. As discussed in Section 5.5, the *net* RESURF1 and *net* RESURF2 doses were kept at slightly lower values than the optimum *net* RESURF1 and *net* RESURF2 doses ($2 \times 10^{12}\,\mathrm{cm}^{-2}$ and 10–$12 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively). High-dose ($5 \times 10^{15}\,\mathrm{cm}^{-2}$) P^+ implantation at 300 °C was employed to form the source/drain regions. After these ion implantations, high-temperature annealing was performed at 1700 °C for 20 min with a carbon cap to suppress surface roughening [1]. Nearly all of the implanted N and Al atoms are activated (activation ratio > 95 %) through the present annealing procedure [2, 3]. After RCA cleaning, thermal oxidation was carried out in dry N_2O (10 % diluted in N_2) ambience at 1300 °C, followed by post-oxidation annealing (POA) in an N_2 ambience at 1300 °C for 30 min [4, 5]. The gate oxide thickness (d_{OX}) was about 80 nm. Al and Ti/Al were used as the contact metal for the source/drain regions and substrate, respectively, and these metals were annealed at 600 °C for 10 min. The gate electrode was formed by Al. The typical channel length (L_{Ch}) and width (W) of RESURF MOSFETs were 1–5 μm and 200 μm, respectively. The drift length (L_{Drift}) of the fabricated RESURF MOSFETs was 10 μm (RESURF1 length (L_{RES1}) and RESURF2 length (L_{RES2}) were 5 μm each) or 20 μm (RESURF1 and RESURF2 lengths were 10 μm each).

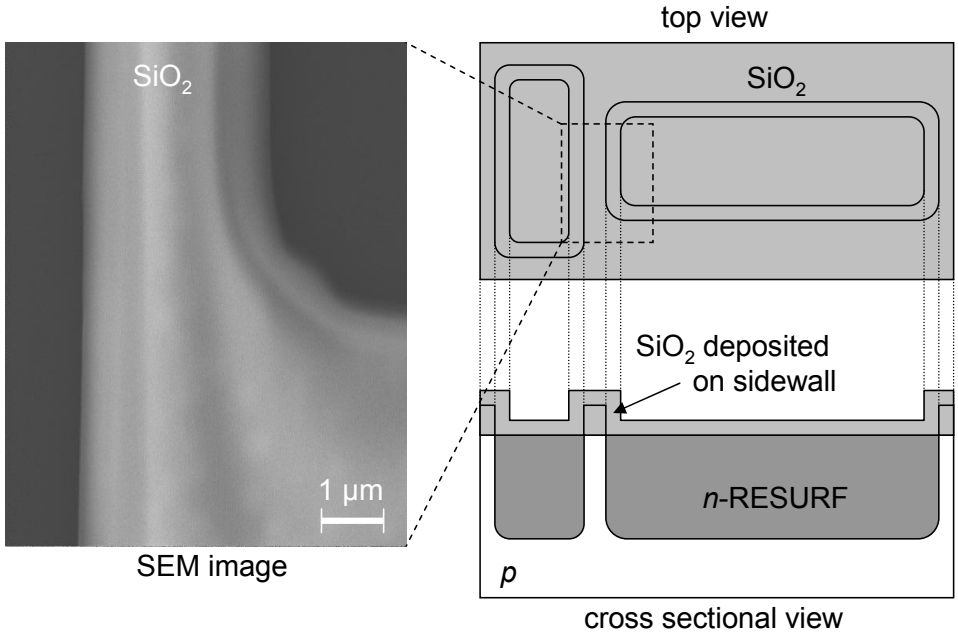
6.2.2 Self-Aligned Process

In the double RESURF MISFETs, the top-p region needs to be formed inside the RESURF region. When the distance between the top-p region and the channel region is too long (e.g. $> 3\,\mu$m), the device may exhibit low breakdown voltage because the top-p region cannot protect the gate insulators as discussed in Chapter 5. On the other hand, when the distance is too short (e.g. $< 0.2\,\mu$m), the resistance of junction FET (JFET) located in the region between the channel region and the top-p region may become high. Therefore, it is important to keep the distance about 1 μm to suppress these adverse impacts.

In this study, a self-aligned process is proposed to reproducibly maintain the adequate distance between the top-p region and the channel region. Figures 6.2 and 6.3 show the schematic flow of the self-aligned process. The self-aligned process begins with the deposition of 1.5 μm-thick SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). The deposited SiO_2 was patterned by reactive ion etching (RIE) with a CF_4-H_2 chemistry and used as an implantation mask. Multiple N^+ implantations were carried out at RT to form the RESURF1 region (Fig. 6.2 (a)). Then, 1.5 μm-thick SiO_2 was deposited by PECVD without removal of the initial SiO_2 mask (Fig. 6.2 (b)). The SiO_2 was deposited both on the surface of SiC and the initial SiO_2 mask and on the sidewall of the SiO_2 mask. After the second deposition of SiO_2, the whole area of SiO_2 film was etched by RIE to expose the SiC

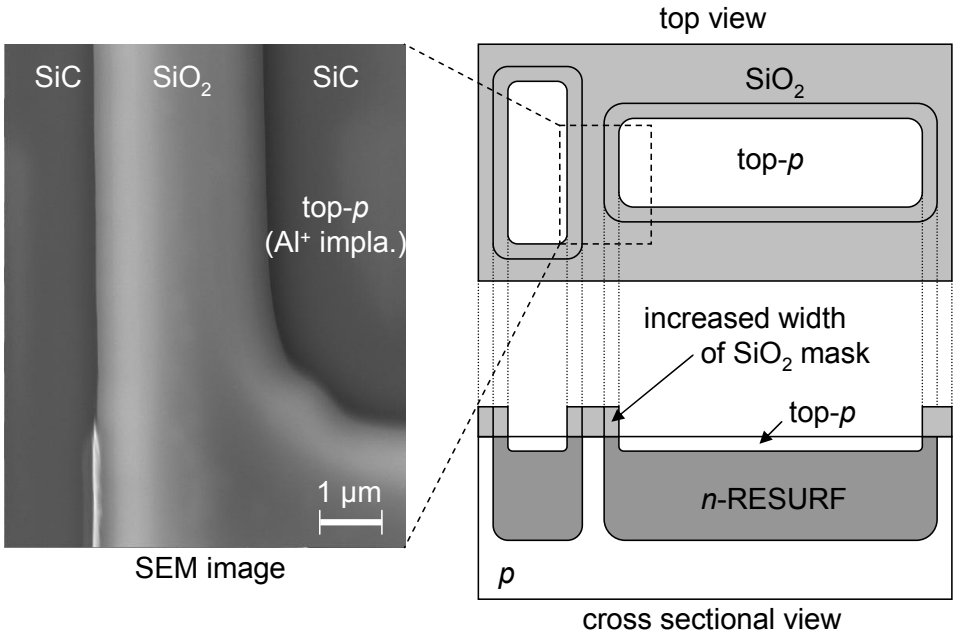


(a)

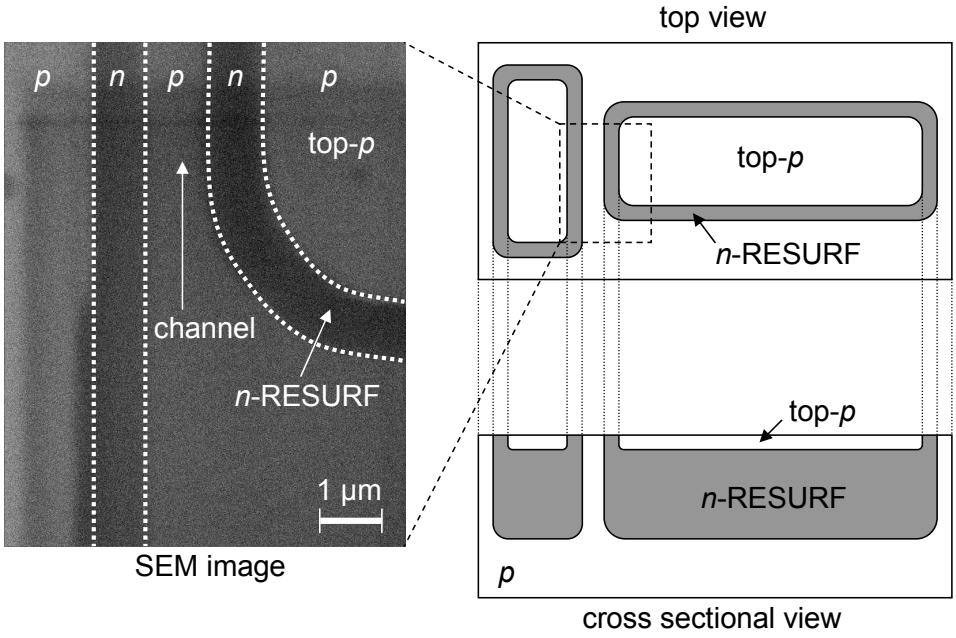


(b)

Figure 6.2: Schematic flow of a self-aligned process (1). RESURF region is formed by multiple N^+ implantations (a). Then, SiO_2 deposition is carried out without removal of initial SiO_2 mask (b). The SiO_2 film is deposited on the sidewall of the initial SiO_2 mask as well.



(a)



(b)

Figure 6.3: Schematic flow of a self-aligned process (2). The SiO_2 film (Fig. 6.2 (b)) is etched by RIE and multiple Al^+ implantations are performed through the SiO_2 mask with increased width to form the top-p region (a). After removing the SiO_2 mask, thermal annealing is carried out to activate the implant dopants (b).

surface. The SiO_2 mask with increased width (about 1 μm on each side) can be employed as a mask for subsequent top-p implantation without any additional lithographic process. The top-p region was formed by multiple Al^+ implantations at RT (Fig. 6.3 (a)). After all implantation processes to form the RESURF2 region and the source/drain regions, thermal annealing was performed to activate implanted species. The left image of Fig. 6.3 (b) exhibits a scanning electron microscopy (SEM) image after activation annealing. In this SEM image, the dark and bright areas correspond to n- and p-regions, respectively. By using the self-aligned process, the top-p region can be successfully formed inside the RESURF region and maintain an adequate distance from the channel region. The self-aligned process eliminates the risk that the channel region is connected to the top-p region.

6.2.3 TEG Devices and RESURF Diodes

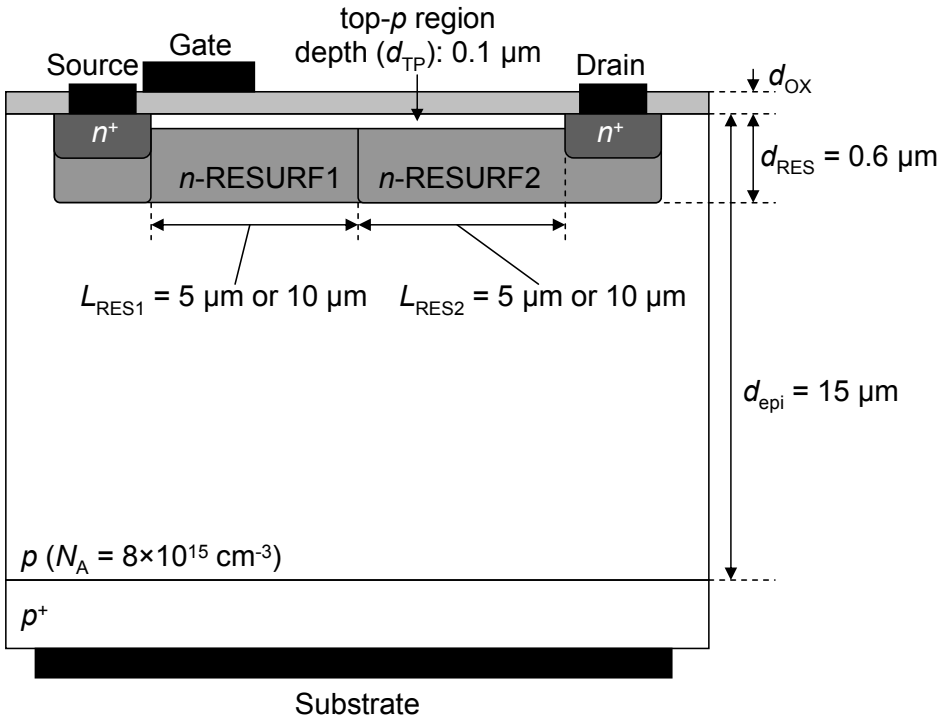
The ON-resistance of RESURF MISFETs consists basically of the drift resistance, the channel resistance, and the contact resistance. To evaluate the drift resistance component separately from the total ON-resistance, a test elementary group (TEG) device was fabricated. Figure 6.4 (a) shows the structure of the TEG device fabricated in this study. The TEG devices have a similar structure to RESURF MISFETs, except for the channel region. The channel length of TEG device was 0 μm, which means that the source region is connected with the RESURF1 region. Thus, the channel resistance can be neglected in the TEG devices, and the dominant resistance component is the drift resistance and the contact resistance. To estimate the contact resistance, transfer length method (TLM) structure was also formed on the same wafer of the RESURF MISFETs. Therefore, the drift resistance of RESURF MISFETs could be estimated from that of TEG devices with the same RESURF1, RESURF2, and top-p doses as those of fabricated RESURF MISFETs.

Figure 6.4 (b) shows the structure of a RESURF diode fabricated in this study. The structure of RESURF diodes is similar to that of fabricated RESURF MISFETs but without the source region and gate electrode. The RESURF diodes have a circular geometry. Thus, breakdown voltage of RESURF diodes corresponds to that of RESURF MISFETs when the breakdown takes place in SiC (not in the gate insulators). The ideal breakdown voltage of RESURF MISFETs can be estimated by using RESURF diodes.

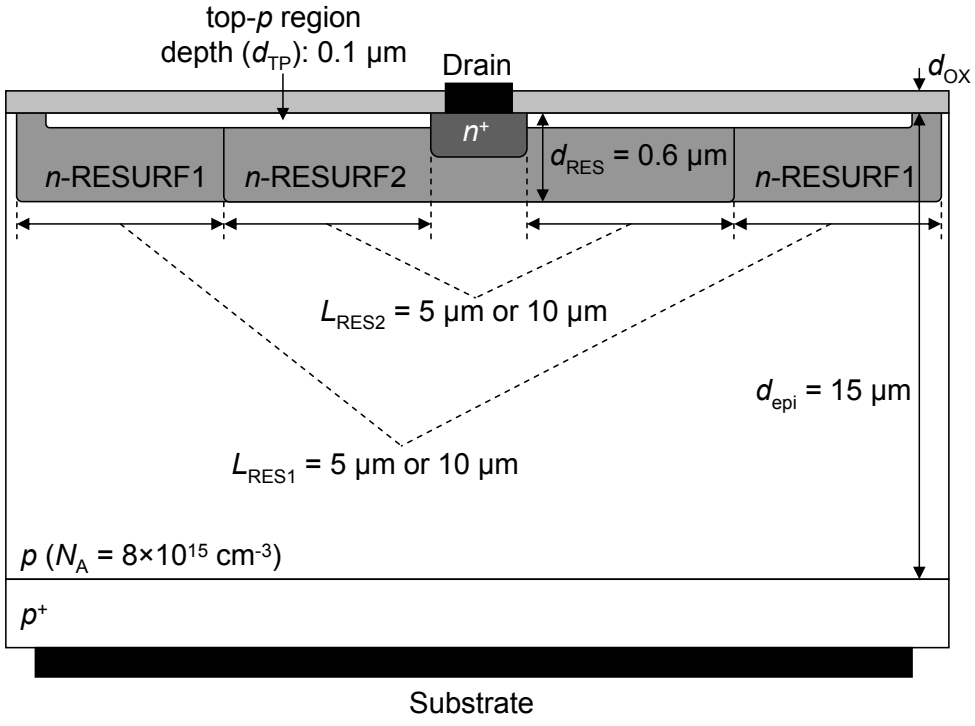
6.3 Basic Performance

6.3.1 On-State Characteristics

The gate characteristics of a test MOSFET without processing the RESURF region on the same wafer are shown in Fig. 6.5. The channel length and width of test MOSFETs with N_2O-grown oxides are 50 μm and 200 μm, respectively. Figure 6.5 also shows the relationship between the channel mobility and gate voltage (V_G). The effective mobility is



(a)



(b)

Figure 6.4: Schematic structures of (a) a TEG device and (b) a RESURF diode. TEG devices and RESURF diodes are used to estimate the drift resistance and the ideal breakdown voltage of RESURF MISFETs, respectively.

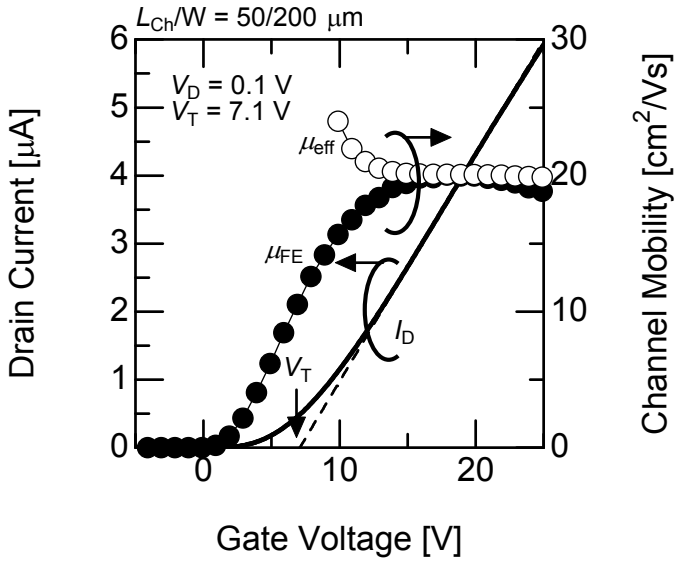


Figure 6.5: Gate characteristics of a test MOSFET without the RESURF region, processed on the same wafer, in the linear region. The channel length and width are 50 μm and 200 μm, respectively. The relationship between the channel mobility and gate voltage is also shown. The solid line denotes the drain current ($I_{\rm D}$), closed circles the field effect mobility ($\mu_{\rm FE}$), and open circles the effective mobility ($\mu_{\rm eff}$).

approximately $20\,\mathrm{cm^2/Vs}$, and the threshold voltage was estimated to be 7.1 V from the gate characteristics. The test MOSFETs with N_2O-grown oxides fabricated on 4H-SiC (0001) show a typical channel mobility of 20–22 $\mathrm{cm^2/Vs}$, as described in Chapter 4.

The ON-resistance was calculated by using the following equation:

$$R_{\mathrm{ON}} = \frac{V_{\mathrm{D}}}{I_{\mathrm{D}}} \times A_{\mathrm{Act}}, \tag{6.1}$$

where V_{D} is the drain voltage, I_{D} the drain current, and A_{Act} the are of the active region. Here, the area of the active region was defined as:

$$A_{\mathrm{Act}} = (L_{\mathrm{Ch}} + L_{\mathrm{Drift}} + L_{\mathrm{SD}})W, \tag{6.2}$$

where L_{SD} is the length of source/drain pads. A source/drain pad length of 6 μm was used to calculate the ON-resistance in this study. From the characteristics of TLM structure, the contact resistance of the source/drain regions was about 1–2 $\mathrm{m\Omega cm^2}$ for each MOSFET on the 4H-SiC (0001) face.

Figure 6.6 shows the gate characteristics of 4H-SiC (0001) two-zone single and double RESURF MOSFETs with a drift length of 20 μm. These MOSFETs have the same *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) of $1 \times 10^{12}\,\mathrm{cm^{-2}}$ and $9 \times 10^{12}\,\mathrm{cm^{-2}}$, respectively. The top-$p$ doses of the single and double RESURF MOSFETs are $0\,\mathrm{cm^{-2}}$ and $12 \times 10^{12}\,\mathrm{cm^{-2}}$, respectively. In Fig. 6.6, the gate voltage dependence of the ON-resistance (R_{ON}) is also exhibited. The typical threshold voltage is 4–6 V, which is lower than that of the test MOSFETs. Slight decrease in the threshold voltage is due to short-channel effects discussed in Chapter 2. The drain current is dramatically increased in the double RESURF MOSFET, compared with the single RESURF MOSFET, leading to the decrease in ON-resistance. Although the ON-resistance of the single RESURF MOSFET at a gate oxide field ($V_{\mathrm{G}}/d_{\mathrm{OX}}$) of 3 MV/cm was $192\,\mathrm{m\Omega cm^2}$, the ON-resistance was decreased to $56\,\mathrm{m\Omega cm^2}$ in the double RESURF MOSFET. The ON-resistance can be reduced by utilizing the double RESURF structure.

The relationship between the drift resistance and the RESURF1 dose in the fabricated double RESURF MOSFETs with a drift length of 10 μm and 20 μm is shown in Fig. 6.7. The drift resistance was estimated by using the TEG devices with the same doses as RESURF MOSFETs. In Fig. 6.7, the *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) were fixed at $1 \times 10^{12}\,\mathrm{cm^{-2}}$ and $9 \times 10^{12}\,\mathrm{cm^{-2}}$, respectively, and the RESURF1, RESURF2, and top-p doses were changed. For example, when the RESURF1 dose (D_{RES1}) was increased, the top-p dose (D_{TP}) was also increased to keep the fixed *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$). The MOSFET with a RESURF1 dose of $1 \times 10^{12}\,\mathrm{cm^{-2}}$ has a single RESURF structure (without top-p region, denoted by closed symbols). By increasing the RESURF1 dose, the drift resistance was reduced from $40\,\mathrm{m\Omega cm^2}$ to $6\,\mathrm{m\Omega cm^2}$ in the double RESURF MOSFETs with a drift length of 10 μm. In the fabricated MOSFETs with a long drift length of 20 μm, the drift resistance was as low as $13\,\mathrm{m\Omega cm^2}$ by employing

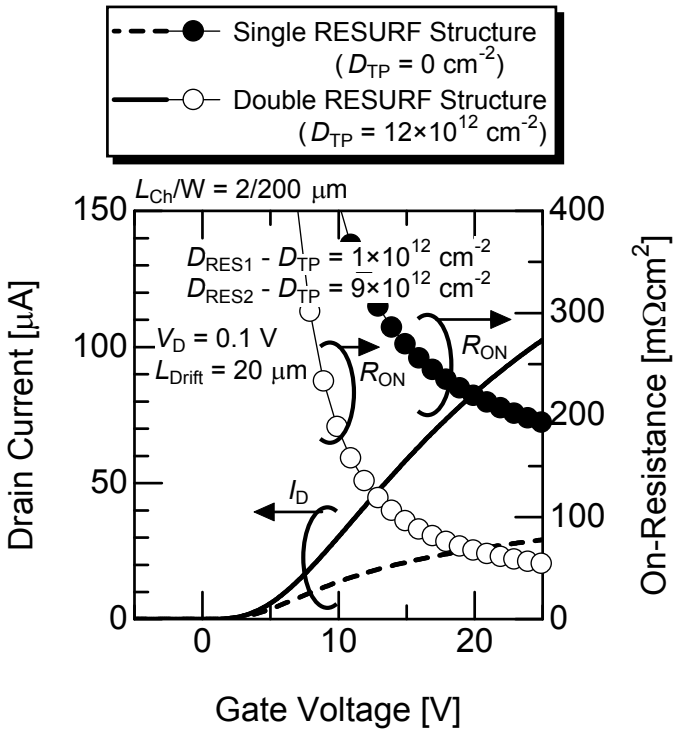


Figure 6.6: Gate characteristics of SiC two-zone single and double RESURF MOSFETs with a long drift length of 20 μm. Both MOSFETs have the same *net* RESURF1 dose of $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and the same *net* RESURF2 dose of $9 \times 10^{12}\,\mathrm{cm}^{-2}$. ON-resistance ($R_{\mathrm{ON}}$) is also shown as a function of gate voltage. The dashed line and closed circles mean the single RESURF MOSFET (without top-p region), and the solid line and open circles the double RESURF MOSFET with a top-p dose of $12 \times 10^{12}\,\mathrm{cm}^{-2}$. The dashed and solid lines denote the drain current, and closed and open circles the ON-resistance.

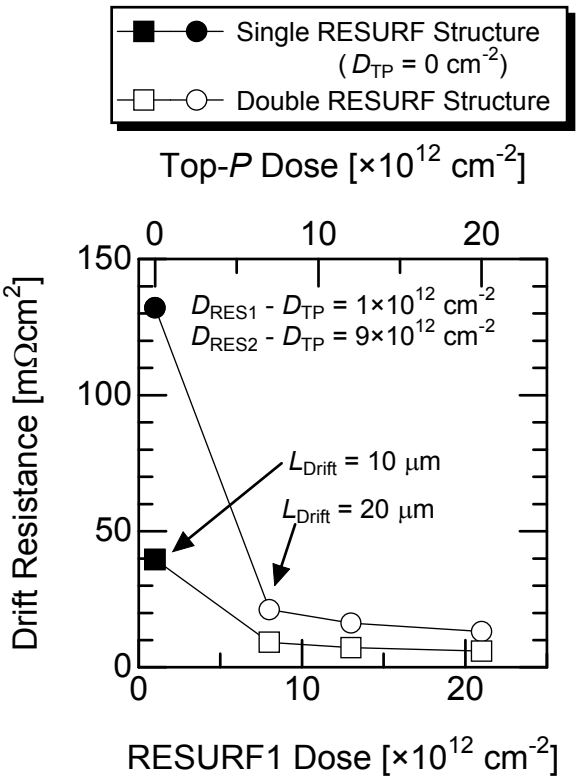


Figure 6.7: Relationship between the RESURF1 dose and the drift resistance for the RESURF MOSFETs fabricated on 4H-SiC (0001). The *net* RESURF1 and *net* RESURF2 doses are fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. Open and closed circles denote the drift resistance of RESURF MOSFETs with a drift length of $20\,\mu$m, and open and closed boxes that of RESURF MOSFETs with a drift length of $10\,\mu$m. Closed symbols mean the characteristics of single RESURF structure, and open symbols those of double RESURF structure.

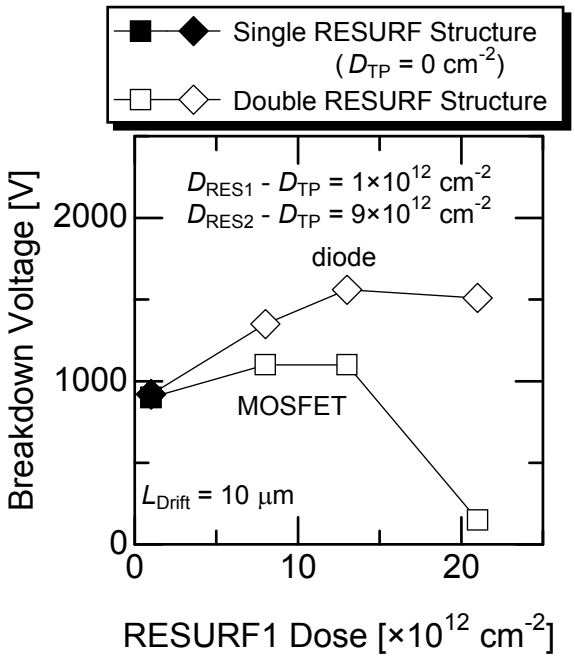
the double RESURF structure, although the drift resistance in the single RESURF MOSFET was 132 mΩcm^2. The longer drift length naturally results in higher drift resistance. By increasing the RESURF doses, the drift resistance can be decreased by over 80 %. The double RESURF structure is effective in reducing the drift resistance, as expected by device simulation.

6.3.2 Off-State Characteristics

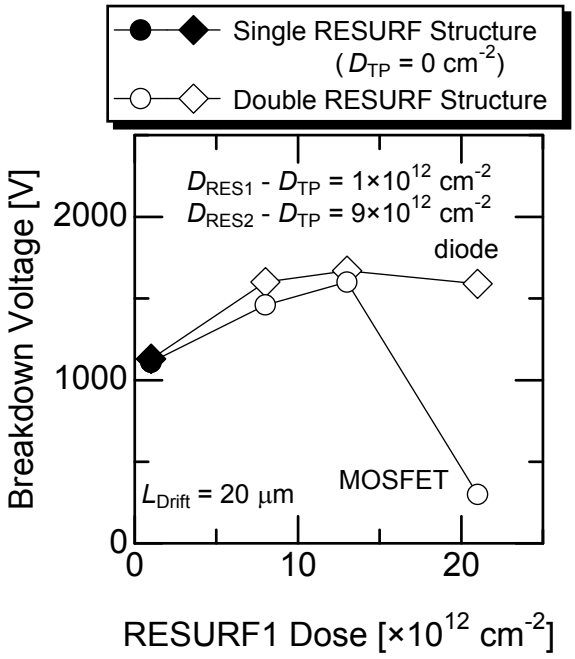
Figure 6.8 shows the relationship between the breakdown voltage (V_B) and the RESURF1 dose in the fabricated 4H-SiC (0001) two-zone double RESURF MOSFETs with a drift length of (a) 10 μm and (b) 20 μm. The *net* RESURF1 and *net* RESURF2 doses were fixed at 1×10^{12} cm^{-2} and 9×10^{12} cm^{-2}, respectively. In Fig. 6.8, the breakdown voltage of RESURF diodes is also shown. Note that the breakdown voltage of the fabricated MOSFETs is greater than 1 kV, although Si lateral MISFETs hardly exhibit breakdown voltage over 1 kV. In Fig. 6.8 (a), the breakdown voltage of RESURF MOSFETs with a short drift length of 10 μm is about 1050 V and lower than that of RESURF diodes (over 1300 V). On the other hand, in the case of long drift length (Fig. 6.8 (b)), RESURF MOSFETs exhibit similar breakdown voltage (about 1500 V) to RESURF diodes when the RESURF1 dose is kept below 20×10^{12} cm^{-2}. The breakdown voltage of the RESURF diodes should be the same as the breakdown voltage of the RESURF MOSFETs with the same RESURF doses, when the breakdown occurs in SiC (not in the gate oxides). Therefore, most MOSFETs with the short drift length break down in the gate oxides (not in SiC).

Note that the breakdown voltage is increased by using the double RESURF structure compared with the single RESURF structure. In the case of the short drift length, the double RESURF diodes show higher breakdown voltage and the breakdown voltage of double RESURF MOSFETs is increased slightly. In the double RESURF diodes, the breakdown occurred in SiC, especially at the drain edge, as mentioned above. The difference in the donor concentration between the n^+-drain region and the n-RESURF region is small in the double RESURF structure. Thus, the electric field crowding at the drain edge was relaxed by utilizing the double RESURF structure. In the double RESURF MOSFETs with the short drift length, the breakdown voltage is also increased, compared with the single RESURF MOSFET. Although the breakdown in the double RESURF MOSFETs with short drift length occurred in the gate oxides, the electric field at the drain edge as well as the gate edge is reduced by employing the double RESURF structure as expected from the device simulation.

In the case of the long drift length, the breakdown voltage was increased in both diodes and MOSFETs. The breakdown took place in SiC, and the breakdown voltage increased due to the decreased electric field at the drain edge. The breakdown voltage of the MOSFETs with a RESURF1 dose of 21×10^{12} cm^{-2} dropped below 500 V. These MOSFETs break down destructively. Therefore, the breakdown may occur at the gate oxides near the channel



(a)



(b)

Figure 6.8: RESURF1 dose dependence of breakdown voltage for the fabricated 4H-SiC (0001) RESURF MOSFETs and diodes with a drift length of (a) 10 μm and (b) 20 μm. The *net* RESURF1 and *net* RESURF2 doses are fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. Open and closed boxes (in (a)) and circles (in (b)) represent the breakdown voltage of RESURF MOSFETs. Open and closed rhombuses denote the breakdown voltage of RESURF diodes. Closed symbols mean the characteristics of single RESURF structure, and open symbols those of double RESURF structure.

region, as discussed in Section 5.5.

6.3.3 Temperature Dependence

The correlation between the effective mobility and the temperature is shown in Fig. 6.9. The channel mobility was estimated from the characteristics of the test MOSFETs processed on the same wafer of RESURF MOSFETs. The effective mobility is almost constant or slightly decreased by increasing temperature. The threshold voltage did not vary (or was slightly decreased) at elevated temperature. Therefore, the channel resistance of RESURF MOSFETs is almost unchanged or shows a slight increase.

Figure 6.10 shows the temperature dependence of the drift resistance for the fabricated 4H-SiC (0001) two-zone single and double RESURF MOSFETs with a long drift length of $20\,\mu$m. The MOSFETs shown in Fig. 6.10 have a *net* RESURF1 dose of $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and a *net* RESURF2 dose of $9 \times 10^{12}\,\mathrm{cm}^{-2}$. The single RESURF MOSFET (closed circles in Fig. 6.10 (a)) exhibits large increase of drift resistance, compared with the double RESURF MOSFETs (open symbols in Fig. 6.10 (a)). The drift resistance of the fabricated single RESURF MOSFET is increased by about 200 %, from $132\,\mathrm{m\Omega cm}^2$ at RT to $258\,\mathrm{m\Omega cm}^2$ at 150 °C. Due to its high drift resistance, the ON-resistance of the single RESURF MOSFET was $333\,\mathrm{m\Omega cm}^2$ at 150 °C, which is much higher than that at RT ($192\,\mathrm{m\Omega cm}^2$). On the other hand, as shown in Fig. 6.10 (a), the double RESURF MOSFETs with higher RESURF doses show a considerably smaller temperature dependence of the drift resistance. Figure 6.10 (b) shows the temperature dependence of the drift resistance for the fabricated double RESURF MOSFETs. The double RESURF MOSFET with a RESURF1 dose of $13 \times 10^{12}\,\mathrm{cm}^{-2}$ shows a low drift resistance of $24\,\mathrm{m\Omega cm}^2$ at 150 °C which is only 1.5 times higher than that at RT ($16\,\mathrm{m\Omega cm}^2$). The ON-resistance of the double RESURF MOSFETs with a RESURF1 dose of $13 \times 10^{12}\,\mathrm{cm}^{-2}$ at 150 °C was still low, $72\,\mathrm{m\Omega cm}^2$, while that at RT was $57\,\mathrm{m\Omega cm}^2$. This small temperature dependence of ON-resistance is another strong advantage of the double RESURF MOSFETs.

Temperature dependence of breakdown voltage for the fabricated double RESURF MOSFET with a long drift length of $20\,\mu$m is represented in Fig. 6.11. The MOSFET has a RESURF1 dose of $8 \times 10^{12}\,\mathrm{cm}^{-2}$, a RESURF2 dose of $16 \times 10^{12}\,\mathrm{cm}^{-2}$, and a top-$p$ dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$. The gate bias voltage was 0 V. The breakdown voltage is increased to 1450 V at 150 °C from 1400 V at RT. The breakdown voltage of single RESURF MOSFETs with the long drift length has also risen by increasing temperature. The positive temperature dependence of breakdown voltage indicates that the breakdown mechanism of the double RESURF MOSFET is due to avalanche multiplication, which agrees with the results from the analyses of RESURF diodes.

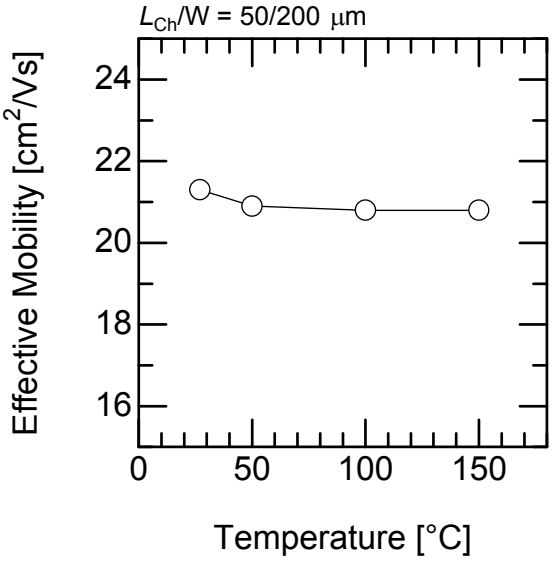
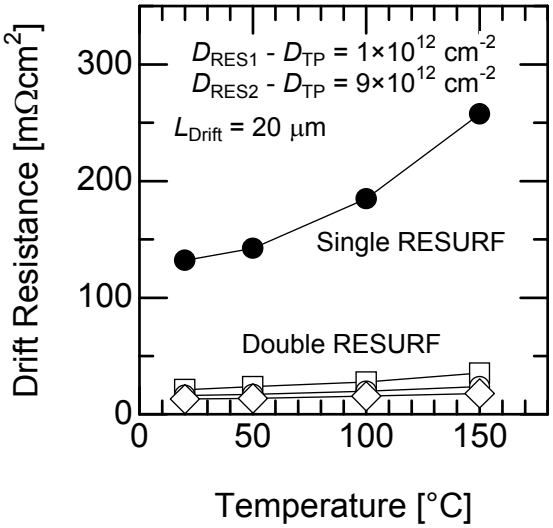
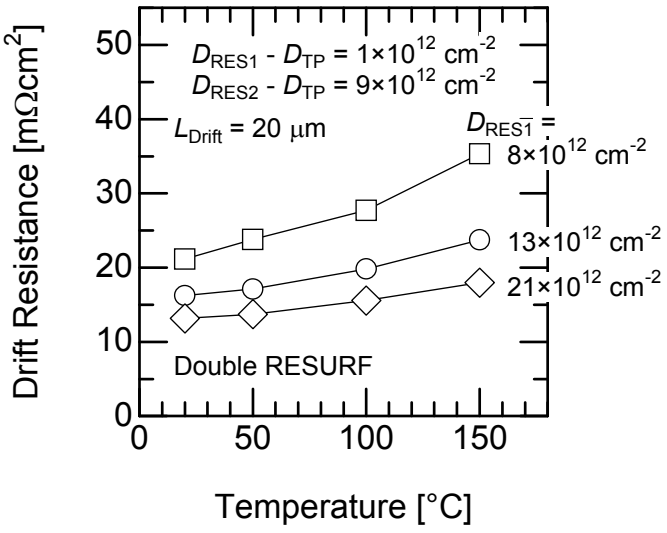


Figure 6.9: Temperature dependence of effective mobility for a 4H-SiC (0001) MOSFET. The effective mobility is estimated from the gate characteristics of the test MOSFETs without the RESURF region.



(a)



(b)

Figure 6.10: Temperature dependence of drift resistance for the fabricated 4H-SiC (0001) RESURF MOSFETs with a long drift length of 20 μm. The *net* RESURF1 and *net* RESURF2 doses are fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. In (a), closed circles mean the single RESURF structure, and open symbols the double RESURF structure. In (b), open boxes denote the double RESURF structure with a RESURF1 dose of $8 \times 10^{12}\,\mathrm{cm}^{-2}$, open circles that with a RESURF1 dose of $13 \times 10^{12}\,\mathrm{cm}^{-2}$, and open rhombuses that with a RESURF1 dose of $21 \times 10^{12}\,\mathrm{cm}^{-2}$.

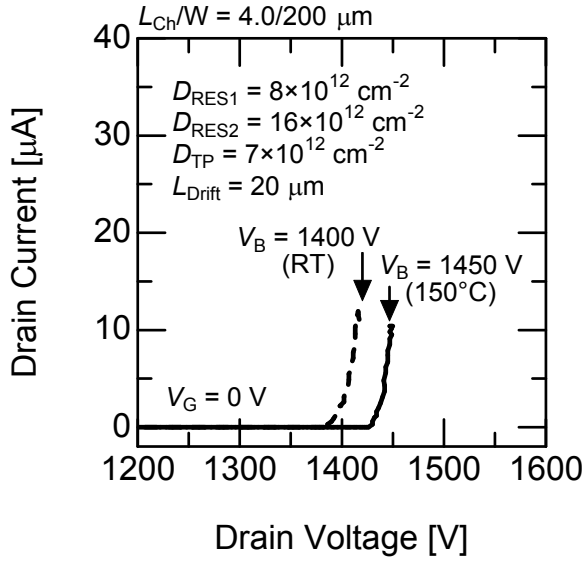


Figure 6.11: Blocking characteristics of the double RESURF MOSFETs with a RESURF1 dose of $8 \times 10^{12}\,\mathrm{cm}^{-2}$, a RESURF2 dose of $16 \times 10^{12}\,\mathrm{cm}^{-2}$, and a top-$p$ dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$ at RT and 150 °C. The double RESURF MOSFET has a drift length of 20 μm. The gate voltage is 0 V. The dashed and solid lines represent the characteristics at RT and 150 °C, respectively.

6.3.4 Switching Characteristics

In general, the total power loss (P_{total}) of the switching devices is expressed as:

$$P_{\text{total}} = P_{\text{ON}} + f_{\text{S}} E_{\text{S}}, \tag{6.3}$$

where P_{ON} is the power dissipation during the ON-state, f_{S} the switching frequency, and E_{S} the power dissipation per switching. Here, the OFF-state loss was neglected. When the switching frequency is increased, the switching loss ($f_{\text{S}} E_{\text{S}}$) becomes a dominant component of the total power loss. Therefore, the switching characteristics are important in the power switching devices.

Figure 6.12 shows a simple circuit with a resistive load to measure the turn-ON and turn-OFF times (t_{ON} and t_{OFF}, respectively) of the fabricated MOSFETs. The gate resistance (R_{G}) and load resistance (R_{L}) was varied, and the change in the turn-ON and turn-OFF times was measured. The OFF/ON gate voltage was 0 V/15 V and the DC supply voltage was set at 16 V. The gate voltage and the drain voltage were recorded by using a digital oscilloscope. The drain current was calculated from the recorded drain voltage and the load resistance. It should be noted that the structure of the fabricated MOSFETs were not optimized for high-speed switching. For example, the MOSFETs have large parasitic capacitances because the gate pads were formed directly on the gate oxides, not on field oxides. The MOSFET used for the measurements exhibits a threshold voltage of 4.7 V and an ON-resistance of 100 mΩcm^2 at a gate voltage of 15 V. Due to the low gate drive voltage (a gate oxide field of 1.8 MV/cm), the ON-resistance increases.

Typical turn-ON and -OFF transient waveforms are shown in Fig. 6.13. A gate resistance of 10 Ω and a load resistance of 15 kΩ were used for the measurement. When the gate voltage is changed, the drain current is increased (decreased) and the drain voltage is decreased (increased). The turn-ON and -OFF times depend on the gate resistance and the load resistance. Figure 6.14 shows the load resistance dependence of the turn-ON/OFF times, where the gate resistance was fixed at 10 Ω. In Fig. 6.14, the turn-OFF time is increased by increasing the load resistance. The drain current is reduced by increasing the load resistance, and hence the time to discharge the gate-drain capacitance is extended. The gate resistance dependence of the turn-OFF time is represented in Fig. 6.15, where load resistance was fixed at the 1 kΩ. The turn-OFF time is dependent on the gate resistance. In the case of the low gate resistance (below 1 kΩ), the turn-OFF time is almost constant (about 500 ns). On the other hand, in the case of the high gate resistance (over 1 kΩ), the turn-OFF time is increased by increasing the gate resistance. The internal gate resistance (r_{G}) generally exists in MOSFETs. Although the turn-OFF time is determined by the internal gate resistance at the low external gate resistance (R_{G}), the turn-OFF time is governed by the external gate resistance when the external resistance is higher than the internal resistance. The turn-OFF time depends on $(R_{\text{G}} + r_{\text{G}})C_{\text{iss}}$, where C_{iss} is the input capacitance which is equal to the sum of the gate-source capacitance and the gate-drain capacitance. From Fig. 6.15, the

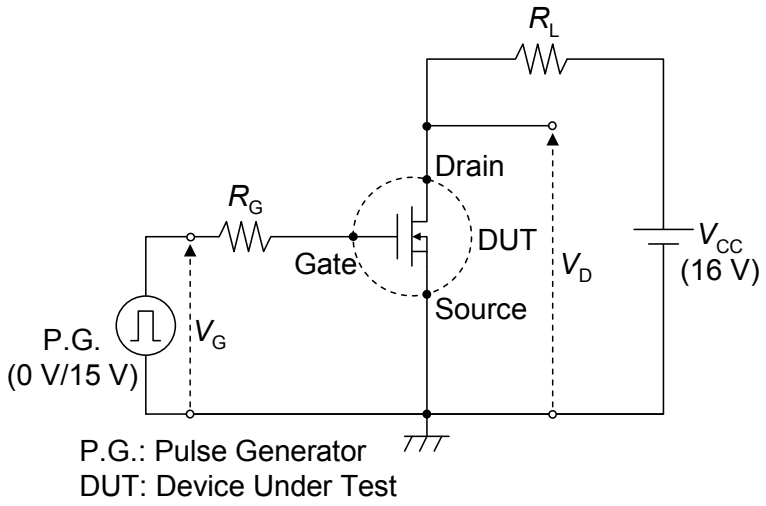


Figure 6.12: Circuit used for analyses of switching time during turn-ON and turn-OFF of the fabricated double RESURF MOSFET.

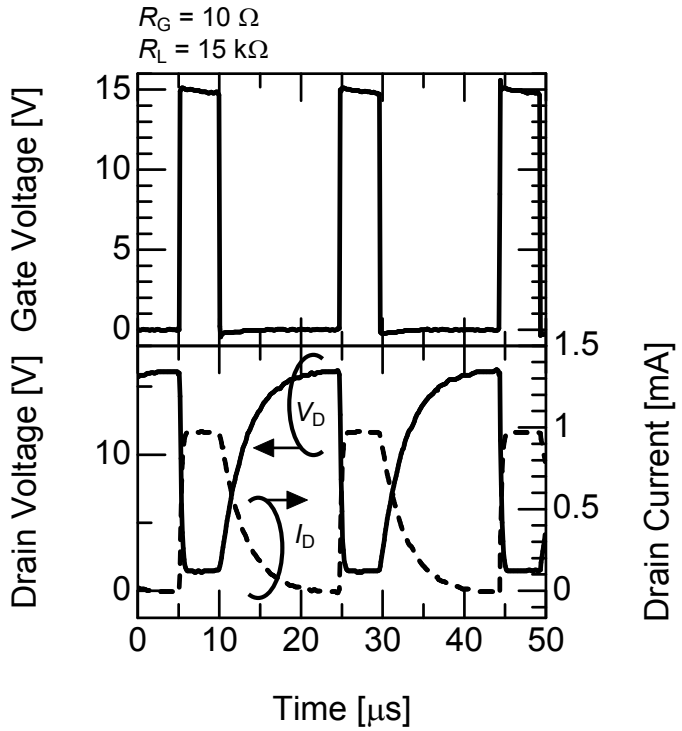


Figure 6.13: Typical switching characteristics of the fabricated double RESURF MOSFET. The gate and load resistance is 10 Ω and 15 kΩ, respectively. The upper graph shows the gate voltage. The lower graph represents the drain voltage (solid line) and the drain current (dashed line).

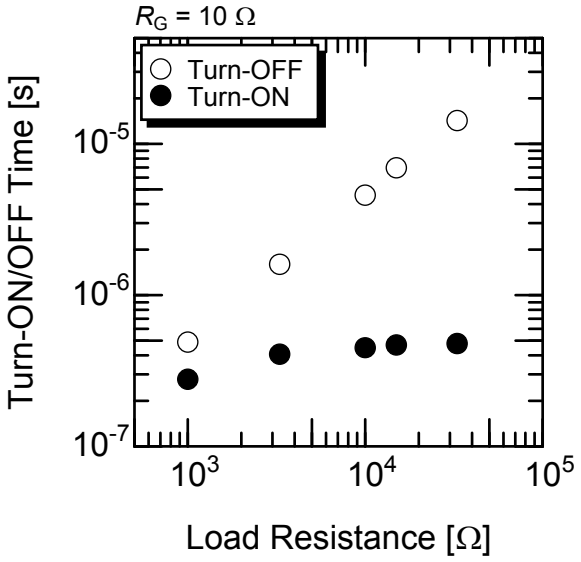


Figure 6.14: Load resistance dependence of the turn-ON/OFF time for the fabricated double RESURF MOSFET. The gate resistance is fixed at 10 Ω. Open circles mean the turn-OFF time, and closed circles the turn-ON time.

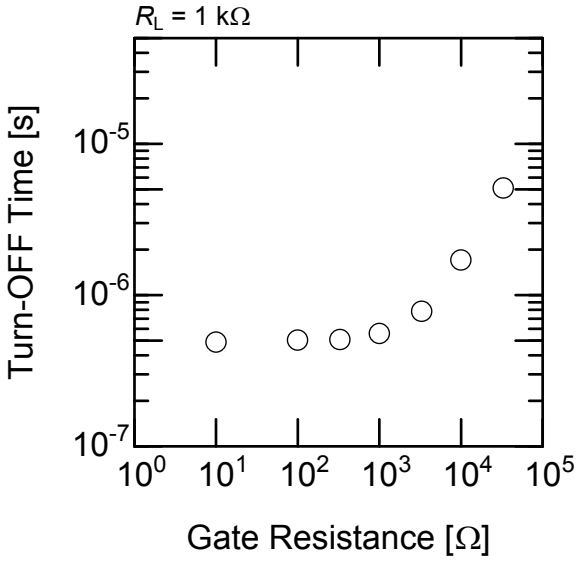


Figure 6.15: Gate resistance dependence of the turn-OFF time for the fabricated double RESURF MOSFET. The load resistance is fixed at 1 kΩ. The drain current during the ON-state is about 8 mA.

internal gate resistance is estimated to be about 2 kΩ. To shorten the turn-OFF time, the optimization of device structure (decrease of gate capacitance, etc.), as well as the decrease of the internal gate resistance, is an important step to be taken into account.

6.3.5 Discussion

The drift resistance and the breakdown voltage of the fabricated MOSFETs are compared with those of the simulated MOSFETs. The relationship between the drift resistance and the RESURF1 dose for the fabricated and simulated MOSFETs with a drift length of 20 μm is shown in Fig. 6.16. The *net* RESURF1 dose and the *net* RESURF2 dose were fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. The RESURF1 dose dependence of the drift resistance for the fabricated MOSFETs denotes the similar tendency of that for the simulated MOSFETs, although small difference is observed in the absolute values. The ionization ratio of nitrogen donors in the RESURF region is almost unity in the simulation, while that in the real devices is lower than unity, about 90 %. In addition, the fabricated RESURF MOSFETs show self-heating during the ON-state because the current need to flow the RESURF region which cross section area is $1 \times 10^{-6}\,\mathrm{cm}^2$ (current density: about $100\,\mathrm{A/cm}^2$). The increase of temperature drops the electron mobility due to phonon scattering. Therefore, the fabricated MOSFETs show the higher drift resistance than the simulated MOSFETs.

The RESURF1 dose dependence of the breakdown voltage for the fabricated and simulated MOSFETs with a drift length of 20 μm is shown in Fig. 6.17. The *net* RESURF1 dose and the *net* RESURF2 dose were fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. The fabricated double RESURF MOSFETs exhibit a higher breakdown voltage than the simulated MOSFETs. As discussed in Section 5.5, the effective concentration of the ionized donors in the RESURF region may be increased because a portion of ionized acceptors inside the top-p region is terminated by the positive charges at the MOS interface, not by the ionized donors inside the RESURF region. Therefore, the effective doses of the fabricated MOSFETs approach the optimum values. As a result, the fabricated MOSFETs exhibited a higher breakdown voltage compared with the simulated MOSFETs with the same RESURF doses.

Furthermore, the double RESURF MOSFETs exhibited the small temperature dependence of the drift resistance, and hence the increase in ON-resistance at high temperature was small for the double RESURF MOSFETs. In terms of practical use, the positive temperature dependence of ON-resistance is essential requirement for power devices to suppress thermal runaway. On the other hand, the large ON-resistance of power devices results in the large power dissipation. Therefore, the small increase of drift resistance with elevating temperature is a strong advantage of double RESURF structure. Owing to the high doping concentration in the double RESURF MOSFETs, the temperature dependence of electron mobility in the double RESURF region is smaller than that in the single RESURF

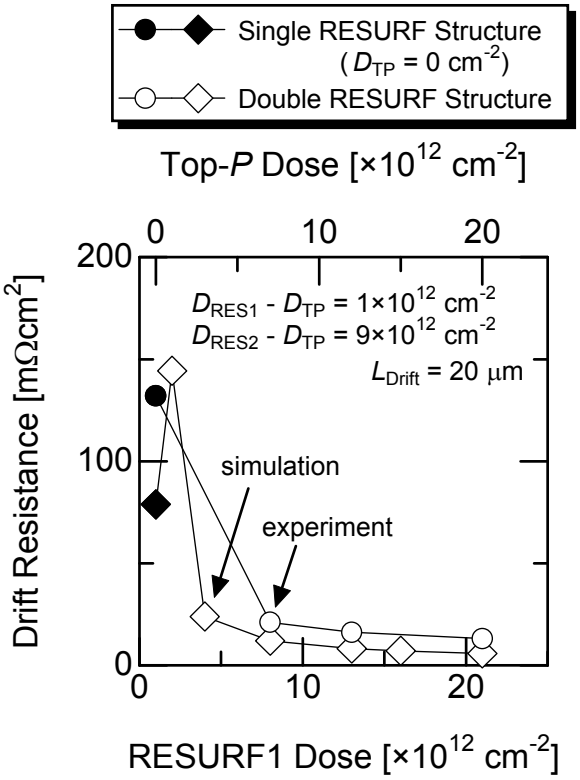


Figure 6.16: Relationship between the drift resistance and the RESURF1 dose for the fabricated and simulated MOSFETs with a drift length of 20 μm. The *net* RESURF1 and *net* RESURF2 doses are fixed at 1×10^{12} cm^{-2} and 9×10^{12} cm^{-2}, respectively. Closed symbols mean the single RESURF structure, and open symbols the double RESURF structure. Open and closed circles denote the drift resistance of fabricated MOSFETs and open and closed rhombuses that of simulated MOSFETs.

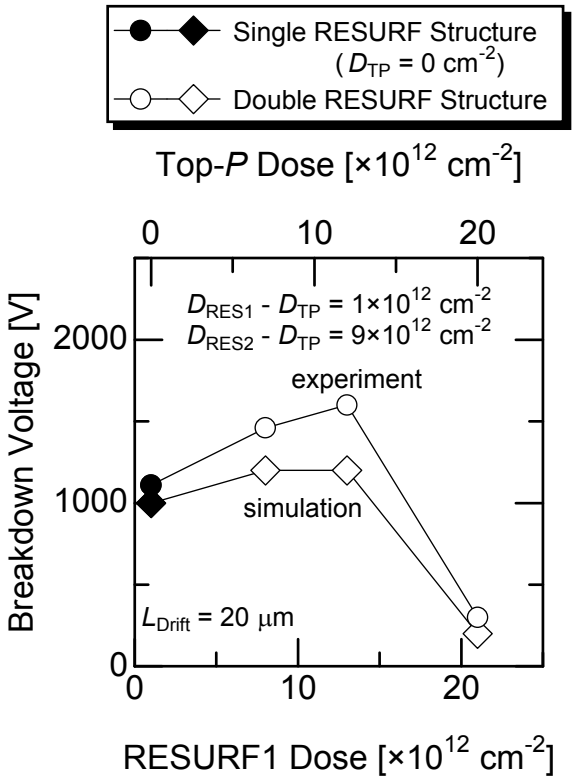


Figure 6.17: Relationship between the breakdown voltage and the RESURF1 dose for the fabricated and simulated MOSFETs with a drift length of 20 μm. The *net* RESURF1 and *net* RESURF2 doses are fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. Closed symbols mean the single RESURF structure, and open symbols the double RESURF structure. Open and closed circles denote the breakdown voltage of fabricated MOSFETs and open and closed rhombuses that of simulated MOSFETs.

region [6]. In addition, the free electron concentration (n_{free}) increases with temperature, due to incomplete ionization of nitrogen donors in SiC at RT. The increment of carrier concentration with increasing temperature is large in the case of high doping concentration, which compensates the decrease in mobility. For example, the single RESURF MOSFET with a RESURF1 dose of $1 \times 10^{12}\,\mathrm{cm}^{-2}$ is compared with the double RESURF MOSFET with a RESURF1 dose of $13 \times 10^{12}\,\mathrm{cm}^{-2}$. The ionization ratio ($n_{\mathrm{free}}/N_{\mathrm{RES1}}$, N_{RES1}: the donor concentration of RESURF1 region) is calculated to be about 98.5 % at RT and about 99.6 % at 150 °C in the single RESURF MOSFET [1]. The increment of free electron concentration at elevated temperature was about 1 % in the single RESURF structure. On the other hand, the ionization ratio of double RESURF structure is increased from about 87.5 % at RT to about 95.0 % at 150 °C. Therefore, the increase in drift resistance at elevated temperature for double RESURF MOSFETs is significantly smaller than that for single RESURF MOSFETs.

As discussed above, by utilizing the double RESURF structure, the drift resistance was decreased and the breakdown voltage was increased by increasing the RESURF doses while keeping the same *net* RESURF1 and *net* RESURF2 doses. Figure 6.18 shows the output characteristics of the fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 10 μm. The MOSFET shown in Fig. 6.18 has a RESURF1 dose of $8 \times 10^{12}\,\mathrm{cm}^{-2}$, a RESURF2 dose of $16 \times 10^{12}\,\mathrm{cm}^{-2}$, and a top-$p$ dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$. A breakdown voltage of 1040 V was obtained. Although the oxide breakdown is the dominant breakdown mechanism in most MOSFETs with the short drift length, the MOSFET shown in Fig. 6.18 breaks in SiC. In the ON-state, the MOSFET exhibits an ON-resistance (R_{ON}) of 36 $\mathrm{m\Omega cm}^2$ at a gate oxide field ($V_{\mathrm{G}}/d_{\mathrm{OX}}$) of 3 MV/cm. From the characteristics of TEG devices, the drift resistance (R_{Drift}) and channel resistance were estimated to be 9 $\mathrm{m\Omega cm}^2$ and 26 $\mathrm{m\Omega cm}^2$, respectively. The contact resistance was obtained as about 1 $\mathrm{m\Omega cm}^2$ from a TLM test structure. The channel resistance component accounts for 72 % of ON-resistance.

Figure 6.19 exhibits the drain and blocking characteristics of the fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 20 μm. The MOSFET shown in Fig. 6.19 has a RESURF1 dose of $13 \times 10^{12}\,\mathrm{cm}^{-2}$, a RESURF2 dose of $21 \times 10^{12}\,\mathrm{cm}^{-2}$, and a top-$p$ dose of $12 \times 10^{12}\,\mathrm{cm}^{-2}$. The fabricated MOSFET exhibits an ON-resistance of 55 $\mathrm{m\Omega cm}^2$ at a gate oxide field of 3 MV/cm and a breakdown voltage of 1540 V at zero gate bias. The threshold voltage determined from the gate characteristics is 4.6 V. From the characteristics of TEG devices, the drift resistance, the channel resistance, and the contact resistance were estimated to be 17 $\mathrm{m\Omega cm}^2$, 36 $\mathrm{m\Omega cm}^2$, and 2 $\mathrm{m\Omega cm}^2$, respectively. The drift resistance could be reduced, however, the channel resistance component accounts for 65 % of the total ON-resistance. The dramatic decrease in the drift resistance makes the reduction of channel resistance again important in the double RESURF MOSFETs with both short and long drift lengths.

[1] In the calculation, an ionization energy of 50 meV was used for N donors.

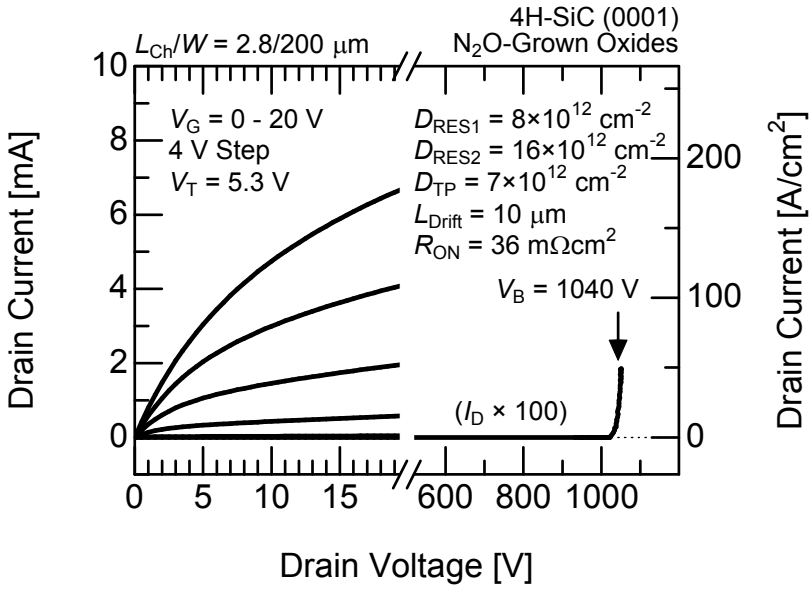


Figure 6.18: Output characteristics of a fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 10 μm. The device with the short drift length exhibits a breakdown voltage of 1040 V and an ON-resistance of 36 mΩcm^2 at an oxide field of 3 MV/cm.

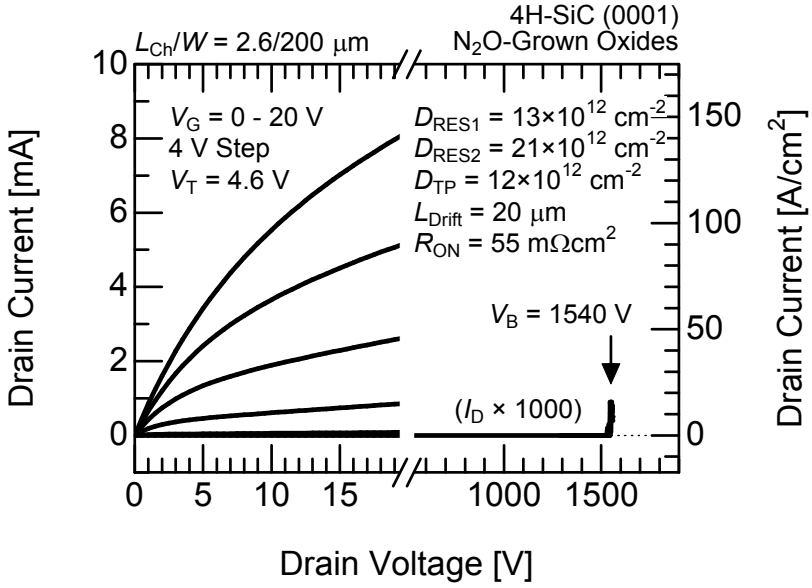


Figure 6.19: Output characteristics of a fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 20 μm. The device with the long drift length exhibits a breakdown voltage of 1540 V and an ON-resistance of 55 mΩcm^2 at an oxide field of 3 MV/cm.

6.4 Improved Performance by Utilizing $(000\bar{1})$

By employing the double RESURF structure, the drift resistance could be dramatically reduced. As a result, the importance of reducing the channel resistance has been again highlighted. In Chapter 4, the MISFETs on the 4H-SiC $(000\bar{1})$ face exhibit higher channel mobility than those on the 4H-SiC (0001) face. The 4H-SiC $(000\bar{1})$ epilayers were used to fabricate double RESURF MISFETs for reducing the channel resistance.

Double RESURF MOSFETs were fabricated on 10 μm-thick p-type 4H-SiC $(000\bar{1})$ epilayers with an acceptor concentration of $6 \times 10^{15}\,\mathrm{cm}^{-3}$. The structure of 4H-SiC $(000\bar{1})$ MOSFETs is similar to that of 4H-SiC (0001) MOSFETs as shown in Fig. 6.1. The RESURF1 dose (D_{RES1}), RESURF2 dose (D_{RES2}), and top-p dose (D_{TP}) were also similar to those of MOSFETs fabricated on 4H-SiC (0001). The *net* RESURF1 dose ($D_{\mathrm{RES1}} - D_{\mathrm{TP}}$) and the *net* RESURF2 dose ($D_{\mathrm{RES2}} - D_{\mathrm{TP}}$) were fixed at $1 \times 10^{12}\,\mathrm{cm}^{-2}$ and $9 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. Thermal oxidation was carried out in dry N_2O (10 % diluted in N_2) at 1300 °C to form the gate oxides. After oxidation, POA was also performed in N_2 at 1300 °C for 30 min. The thickness of gate oxides was about 80 nm. Other processes were the same as explained in Section 6.2.1.

Figure 6.20 shows the gate characteristics of a test MOSFET fabricated on a 4H-SiC $(000\bar{1})$ epilayer. The channel mobility is also shown in Fig. 6.20. The channel length and width of the test MOSFET was 50 μm and 200 μm, respectively. The effective mobility is approximately $33\,\mathrm{cm}^2/\mathrm{Vs}$. Compared with the characteristics of test MOSFETs on the (0001) face, the threshold voltage was decreased to 4.9 V. A typical channel mobility of 30–35 $\mathrm{cm}^2/\mathrm{Vs}$ was obtained in the test MOSFETs with N_2O-grown oxides fabricated on 4H-SiC $(000\bar{1})$. The high channel mobility in the MOSFETs on the $(000\bar{1})$ face, which leads to lower channel resistance, agrees with the results obtained in Chapter 4.

Figure 6.21 shows (a) the output characteristics and (b) the gate characteristics of the 4H-SiC $(000\bar{1})$ two-zone double RESURF MOSFET with N_2O-grown oxides. The drift length of the MOSFET shown in Fig. 6.21 is 10 μm. The RESURF1, RESURF2, and top-p doses are $8 \times 10^{12}\,\mathrm{cm}^{-2}$, $16 \times 10^{12}\,\mathrm{cm}^{-2}$, and $7 \times 10^{12}\,\mathrm{cm}^{-2}$, respectively. The MOSFET breaks at the gate oxide when a drain voltage of 1100 V is applied. The ON-resistance (R_{ON}) of MOSFET is $30\,\mathrm{m\Omega cm}^2$ at a gate oxide field of 3 MV/cm. The MOSFET shows a low threshold voltage of 3.3 V and a subthreshold swing of 172 mV/decade. The channel resistance component accounts for 50 % of ON-resistance (a channel resistance of $15\,\mathrm{m\Omega cm}^2$). The ratio of channel resistance component can be decreased in the $(000\bar{1})$ MOSFETs due to its high channel mobility, compared to the (0001) MOSFETs.

Figure 6.22 shows (a) the drain and blocking characteristics and (b) the gate characteristics of the 4H-SiC $(000\bar{1})$ two-zone double RESURF MOSFET with a long drift length of 20 μm. The MOSFET has a RESURF1 dose of $8 \times 10^{12}\,\mathrm{cm}^{-2}$, a RESURF2 dose of $16 \times 10^{12}\,\mathrm{cm}^{-2}$, and a top-$p$ dose of $7 \times 10^{12}\,\mathrm{cm}^{-2}$. Compared with the MOSFET on the (0001) face shown in Fig. 6.19, the MOSFET on the $(000\bar{1})$ face exhibits a lower threshold

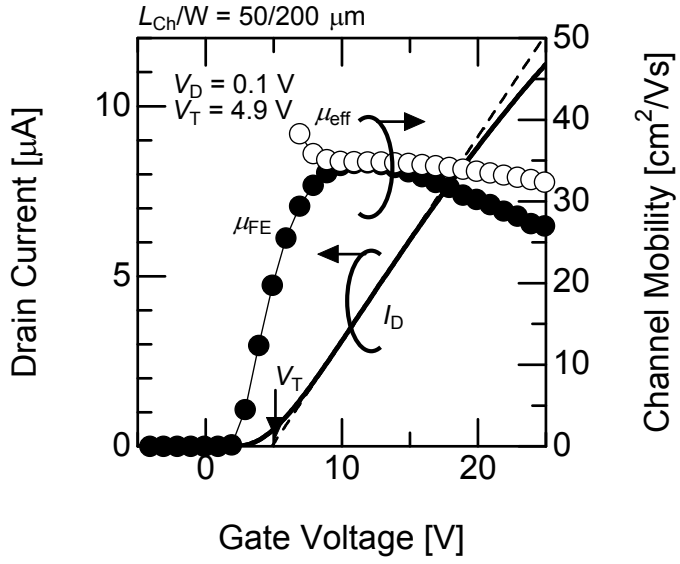
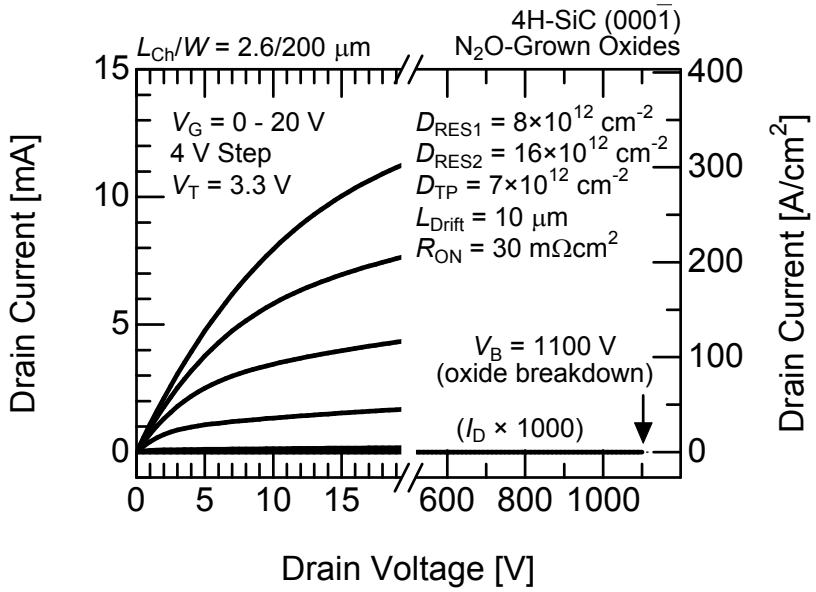
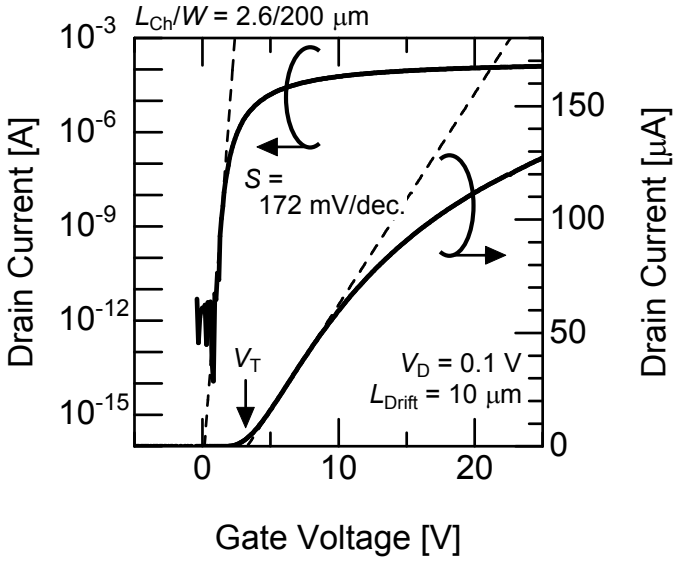


Figure 6.20: Gate characteristics of a 4H-SiC (000$\bar{1}$) test MOSFET without the RESURF region in the linear region. The gate oxide was thermally grown in dry N_2O (10 % diluted in N_2). The relationship between channel mobility and gate voltage is also shown. The solid line denotes the drain current (I_D), closed circles the field effect mobility (μ_{FE}), and open circles the effective mobility (μ_{eff}).

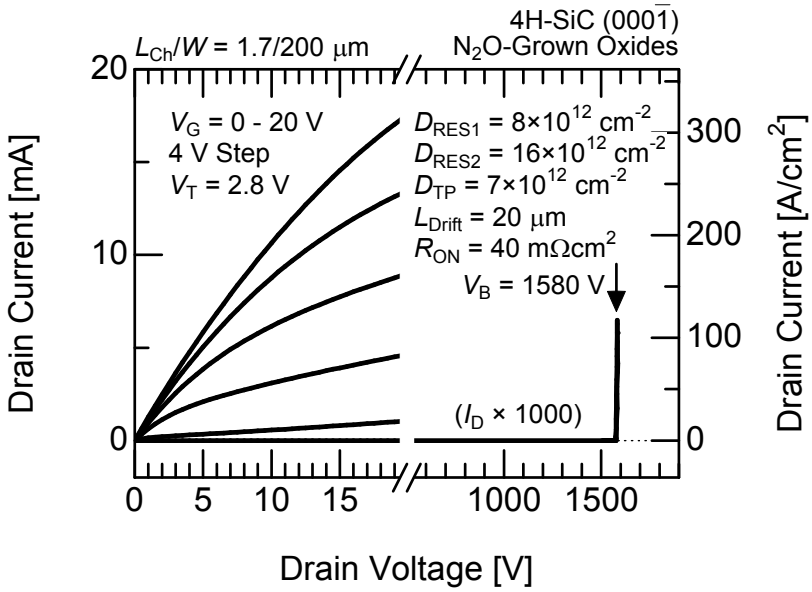


(a)

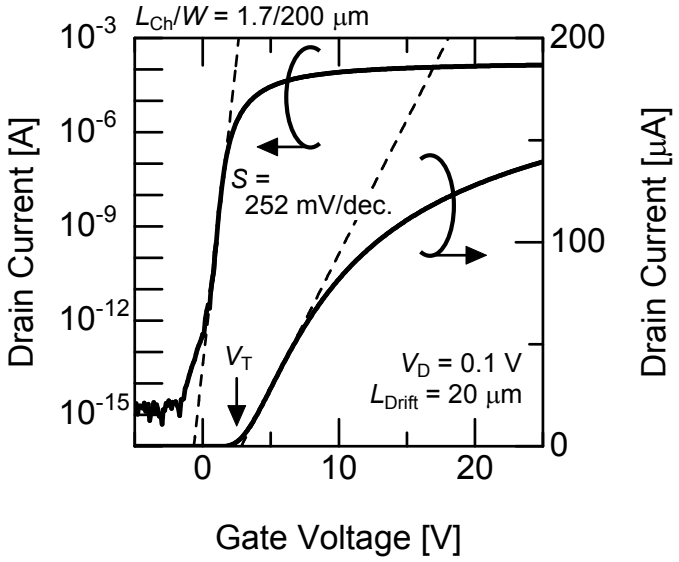


(b)

Figure 6.21: (a) Output and (b) gate characteristics of a fabricated 4H-SiC (000$\bar{1}$) two-zone double RESURF MOSFET with a short drift length of 10 μm. The device with the short drift length exhibits a breakdown voltage of 1100 V and an ON-resistance of 30 mΩcm^2 at an oxide field of 3 MV/cm.



(a)



(b)

Figure 6.22: (a) Output and (b) gate characteristics of a fabricated 4H-SiC (000$\bar{1}$) two-zone double RESURF MOSFET with a long drift length of 20 μm. The device with the long drift length exhibits a high breakdown voltage of 1580 V and a low ON-resistance of 40 mΩcm^2 at an oxide field of 3 MV/cm.

voltage of 2.8 V, a lower ON-resistance of 40 mΩcm^2 at a gate oxide field of 3 MV/cm, and a higher breakdown voltage of 1580 V at zero gate bias. The channel resistance is reduced to 12 mΩcm^2 in the (000$\bar{1}$) MOSFET from 36 mΩcm^2 in the (0001) MOSFET. The reduction of channel length is also effective to minimize the channel resistance. The subthreshold swing of the double RESURF MOSFET on 4H-SiC (000$\bar{1}$) is 252 mV/decade. The small subthreshold swing indicates the superior characteristics of N_2O-grown oxides/4H-SiC (000$\bar{1}$) interface. The 4H-SiC (000$\bar{1}$) face is effective in enhancing the MOSFET performance.

6.5 Comparison with Reported High-Voltage Lateral Devices

The two-zone double RESURF MOSFET fabricated on the 4H-SiC (0001) face exhibited a breakdown voltage of 1540 V and an ON-resistance of 55 mΩcm^2. By utilizing the 4H-SiC (000$\bar{1}$)C face, the ON-resistance was decreased to 40 mΩcm^2, while keeping a similar breakdown voltage of 1580 V. Figure 6.23 plots the relationship between breakdown voltage and ON-resistance for major lateral SiC MISFETs reported in literature [7–13] and this study. For comparison, the relationship for Si "CoolMOS^{TM}" [14], which is the commercially-available vertical superjunction MOSFETs [15], as well as Si lateral MOSFETs and Si lateral insulated gate bipolar transistors (IGBTs) [16–18] are also represented in Fig. 6.23. The figure-of-merit ($V_B{}^2/R_{ON}$) is 12 MW/cm^2 for the CoolMOS^{TM} and is lower than about 10 MW/cm^2 for the reported lateral Si devices. In the case of SiC lateral MISFETs, the figure-of-merit had not been able to exceed 30 MW/cm^2. The figure-of-merit obtained in this study is 43 MW/cm^2 for the MOSFET on (0001) and 62 MW/cm^2 for that on (000$\bar{1}$), which is the highest value among any lateral MISFETs ever reported. The two-zone double RESURF MOSFETs fabricated on the 4H-SiC (000$\bar{1}$)C face demonstrated a record performance, which is more than 10 times better than the "Si limit".

6.6 Discussion

In this chapter, the two-zone double RESURF MISFETs were fabricated and characterized. Through the simulation and fabrication, many advantages of the double RESURF structure over the single RESURF structure were revealed. The followings are the major advantages of the double RESURF structure.

- Low drift resistance:
  The most important feature of the double RESURF structure is that the reduced drift resistance can be obtained. Although the absolute value of the donor concentration in the double RESURF region is much higher than that in the single RESURF region, the *net* concentration is in the same range due to the charge compensation. The high donor concentration naturally decreases the drift resistance.

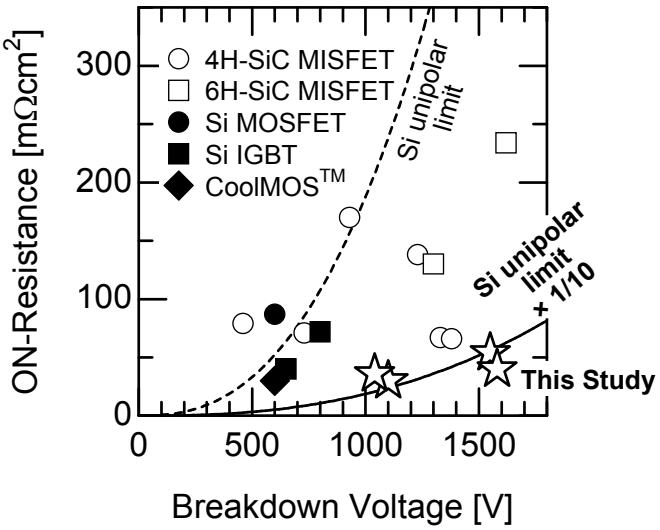


Figure 6.23: Relationship between breakdown voltage and ON-resistance for major lateral high-voltage devices in the literature (${V_\mathrm{B}}^2/R_\mathrm{ON} < 30\,\mathrm{MW/cm^2}$) and this study (${V_\mathrm{B}}^2/R_\mathrm{ON} =$ 30–62 $\mathrm{MW/cm^2}$). The MOSFET fabricated in this study demonstrates a highest figure-of-merit of 62 $\mathrm{MW/cm^2}$ among any lateral MISFETs ever reported, which is more than 10 times better than "Si limit".

- High breakdown voltage:
  The top-p region protects the gate insulators from the high electric field. In addition, the electric field crowding at the drain edge is relaxed because the difference in donor concentration between the drain region and the RESURF2 region becomes smaller in the double RESURF structure. The decreased electric field strength at both gate and drain edges leads to high breakdown voltage.

- Small increase in drift resistance at elevated temperature:
  The donor concentration in the double RESURF structure is higher than that in the single RESURF structure. Due to its smaller decrease of electron mobility and larger increment of ionization ratio in the highly-doped RESURF region at elevated temperature, the temperature dependence of the drift resistance in the double RESURF structure is smaller than that in the single RESURF structure.

The difference between the single and double RESURF structures is the existence of top-p region. In general, to realize the different structure, the number of lithographic process varies. On the other hand, in this study, the top-p region can be formed without additional lithographic process by using the self-aligned process explained in Section 6.2.2. In addition, the risk that the top-p region is connected with the channel region can be entirely eliminated.

By utilizing the double RESURF structure, the fabricated MOSFETs demonstrated a highest figure-of-merit of $62\,\mathrm{MW/cm^2}$ among any lateral MISFETs ever reported. Although the fabricated MISFETs exhibit high breakdown voltage and low ON-resistance, there is room for improvement in the following aspects.

From the analysis of the RESURF diodes, the RESURF MISFETs with a short drift length of $10\,\mu\mathrm{m}$ are potentially capable of enduring a drain voltage of 1500 V at the OFF-state (Fig. 6.8 (a)). The drift resistance in the MOSFETs with the short drift length is about $10\,\mathrm{m\Omega cm^2}$ (Fig. 6.7). Therefore, the double RESURF MOSFETs with the short drift length will exhibit a breakdown voltage of 1500 V and a drift resistance of $10\,\mathrm{m\Omega cm^2}$, although further optimization of device structure is required.

To decrease the channel resistance, the deposited SiO_2 and SiN_x/SiO_2 are attractive insulators, as discussed in Chapters 3 and 4. The MOSFET with deposited SiO_2 annealed in NO on 4H-SiC $(000\bar{1})$ exhibited a channel mobility of $50\,\mathrm{cm^2/Vs}$. In this case, the channel resistance can decrease by 60 % and 30 %, compared to (0001) and $(000\bar{1})$ MOSFETs with N_2O-grown oxides, respectively. The deposited SiO_2 annealed in NO, however, exhibits a low breakdown field of $5.9\,\mathrm{MV/cm}$. Although the top-p region protects the gate insulators, field-plate structure may be needed to suppress the insulator breakdown.

Considering these factors, the double RESURF MISFETs with similar structure used in this study (thickness of epilayer, drift length, etc.) possess the potential to demonstrate a breakdown voltage of 1500 V and an ON-resistance of $15\,\mathrm{m\Omega cm^2}$ (a drift resistance of $10\,\mathrm{m\Omega cm^2}$, a channel resistance of $4\,\mathrm{m\Omega cm^2}$, and a contact resistance of $1\,\mathrm{m\Omega cm^2}$). To

realize high-voltage smart power integrated circuits (ICs), further improvement in the performance of lateral power devices is desired.

6.7 Summary

The double RESURF MISFETs with N_2O-grown oxides were fabricated and characterized. To form the top-p region, the self-aligned process was proposed and employed. By utilizing the double RESURF structure, the drift resistance was reduced by over 80 %. In the case of MOSFETs with the short drift length (10 μm), the breakdown occurred at the gate oxides. On the other hand, the MOSFETs with a long drift length of 20 μm broke down in SiC (not in the gate oxides). The double RESURF MOSFETs exhibited higher breakdown voltage (about 1500 V) than the single RESURF MOSFETs (1100 V) when the breakdown takes place in SiC. Therefore, the double RESURF structure is effective not only for decreasing the drift resistance but also for increasing the breakdown voltage. In addition, double RESURF MOSFETs exhibited a small temperature dependence of drift resistance (small increase in drift resistance at elevated temperature). This is another advantage over the single RESURF structure.

The fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 20 μm exhibited a breakdown voltage (V_B) of 1540 V and an ON-resistance (R_{ON}) of 55 mΩcm^2. In the case of MOSFET fabricated on the 4H-SiC (000$\bar{1}$) face, the breakdown voltage was 1580 V and the ON-resistance was 40 mΩcm^2. The figure-of-merit (${V_B}^2/R_{ON}$) of the fabricated MOSFETs was 30–62 MW/cm^2. A figure-of-merit of 62 MW/cm^2 is the highest value among any lateral MISFETs ever reported and more than 10 times higher than the "Si limit".

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Chapter 7

Conclusions

7.1 Conclusions

For the realization of high-performance smart power integrated circuits (ICs) in SiC, the fundamental study on SiC metal-insulator-semiconductor (MIS) devices has been conducted in the present study. Short-channel effects, which occur when scaling down the MIS field-effect transistor (MISFET) dimensions, have been investigated and both n- and p-channel MIS devices with N_2O-grown oxides as well as deposited insulators have been fabricated and characterized to improve the channel mobility. In addition, lateral high-voltage MISFETs, which are the key component of power ICs, have been explored from scientific and technological aspects.

The main conclusion obtained in the present study can be summarized as follows.

In Chapter 2, the short-channel effects in SiC MISFETs were investigated. The critical channel length (L_{Crit}), below which the short-channel effects occur, were analyzed. The boundary between short-channel devices and long-channel devices can be described as "$L_{\mathrm{Crit}} = 1.56\{r_{\mathrm{j}} d_{\mathrm{OX}} (W_{\mathrm{S}} + W_{\mathrm{D}})^2\}^{1/7}$" for the fabricated SiC metal-oxide-semiconductor FETs (MOSFETs) and "$L_{\mathrm{Crit}} = 0.31\{r_{\mathrm{j}} d_{\mathrm{OX}} (W_{\mathrm{S}} + W_{\mathrm{D}})^2\}^{1/4}$" for the simulated SiC MOSFETs, where r_{j} is the junction depth in μm, d_{OX} the oxide thickness in Å, W_{S} and W_{D} the width of depletion layer extended from the source and drain regions in μm, respectively. The critical channel length for the fabricated MOSFETs was longer than that for the simulated MOSFETs.

To investigate the influence of the effective fixed charges on the short-channel effects, an original charge-share model, which takes the effective fixed charges into account, was proposed. According to the original charge-share model, the threshold voltage is decreased by reducing channel length at relatively long-channel region when the effective fixed charges are located at the MOS interface. The major reason for the long critical channel length for the fabricated MOSFETs, compared to that for the simulated MOSFETs, can be attributed to the presence of effective fixed charges. The reduction of the effective fixed charges contributes greatly to the shortening the critical channel length.

In Chapter 3, the deposited SiO_2 and SiN_x/SiO_2 were applied to the gate insulators of n- and p-type SiC MIS capacitors. The deposited SiO_2 and SiN_x/SiO_2 were annealed in N_2O after the deposition, to improve the interface and dielectric properties. A low interface state density of $7 \times 10^{11}\,cm^{-2}eV^{-1}$ at an energy depth of 0.2 eV from the conduction band edge could be obtained in the n-MOS capacitors with deposited SiO_2 annealed in N_2O. The interface state density near the valence band edge is also reduced to $5 \times 10^{11}\,cm^{-2}eV^{-1}$ at the deposited SiO_2/SiC interface from $9 \times 10^{11}\,cm^{-2}eV^{-1}$ at the N_2O-grown oxides/SiC interface. The NO annealing after the SiO_2 deposition was also effective to decrease the interface state density near the conduction band edge.

In the case of the deposited SiN_x/SiO_2, the interface properties were improved by oxidizing the SiN_x layer during the N_2O annealing. An interface state density of $2 \times 10^{11}\,cm^{-2}eV^{-1}$ could be achieved, which is one-tenth of that obtained at the N_2O-grown oxides/SiC interface, in the n-MIS capacitors with deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h on thin-thermal oxides. The interface state density near the valence band edge for the p-MIS capacitors with thin-thermal oxides was $6 \times 10^{11}\,cm^{-2}eV^{-1}$. For further improvements of interface properties, the stack-gate structure was deposited on the 4H-SiC $(000\bar{1})$C face. The interface state density of the $(000\bar{1})$ MIS capacitors with deposited SiN_x/SiO_2 (10 nm/50 nm) annealed in N_2O for 2 h on thin-thermal oxides is decreased to below $1 \times 10^{11}\,cm^{-2}eV^{-1}$, which indicates that the utilization of the 4H-SiC $(000\bar{1})$C face is attractive for improving the interface properties.

The dielectric properties were also investigated. In the n-MIS capacitors, although the breakdown field of deposited SiO_2 (5.9–7.0 MV/cm) was lower than that of N_2O-grown oxides (8.9 MV/cm), the deposited SiN_x/SiO_2 adequately processed exhibits a similar breakdown field (8.7–9.5 MV/cm) to the N_2O-grown oxides. In the case of p-MIS capacitors, similar tendency was observed. The deposited SiO_2 exhibits higher charge-to-breakdown (over $50\,C/cm^2$) than the N_2O-grown oxides (4–28 C/cm^2). The deposited insulators such as SiO_2 and SiN_x/SiO_2 are promising for improving both the interface and dielectric properties.

In Chapter 4, the deposited insulators such as SiO_2 and SiN_x/SiO_2 were applied to the n- and p-channel SiC MISFETs. Although the n-channel mobility in the (0001) MOSFETs with deposited SiO_2 annealed in N_2O was $26\,cm^2/Vs$, it became as high as $32\,cm^2/Vs$ on (0001) and $50\,cm^2/Vs$ on $(000\bar{1})$ by utilizing the deposited SiO_2 annealed in NO. The fabricated n-channel (0001) MISFETs with thin-thermal oxides between deposited SiN_x/SiO_2 and SiC also showed a high channel mobility of $30\,cm^2/Vs$. From the experimental results, in the n-channel SiC MOSFETs with SiO_2-gate insulators, it was found out that the channel mobility tends to be increased by decreasing the effective fixed charge density. Although the channel mobility is limited by the Coulomb scattering mainly caused by the charges trapped at the deep states when the effective fixed charge density is larger than $1 \times 10^{12}\,cm^{-2}$, other scattering mechanism becomes dominant when the effective fixed charge density is smaller than $1 \times 10^{12}\,cm^{-2}$. The reduction of the effective fixed charge density has an important role not only for the suppression of the short-channel effects but also the further increase

of channel mobility.

The *p*-channel SiC MISFETs were also investigated. The fabricated *p*-channel MOSFETs with N_2O-grown oxides exhibited a channel mobility of $7\,cm^2/Vs$ for the (0001) face, $11\,cm^2/Vs$ for the $(03\bar{3}8)$ face, and $17\,cm^2/Vs$ for the $(11\bar{2}0)$ face. The deposited SiO_2 annealed in N_2O was also effective to increase the channel mobility as is the case for *n*-channel MOSFETs. In contrast to the *n*-channel MISFETs, however, the channel mobility is not much dependent on the effective fixed charge density.

The interface state density was estimated by using an original method. By using gate-controlled diodes, the interface properties near the minority-carrier band edge can be characterized. The N_2O-grown oxides/4H-SiC (0001) interface state density near the conduction band edge evaluated by the *n*-channel MOSFETs was similar to that evaluated by the *n*-MOS capacitors. In the *p*-channel MOSFETs, the interface state density was as small as $1 \times 10^{12}\,cm^{-2}eV^{-1}$ on the 4H-SiC $(03\bar{3}8)$ face, while the (0001) and $(11\bar{2}0)$ faces shows a interface state density of $2 \times 10^{12}\,cm^{-2}eV^{-1}$. Although GaN MOSFETs have received much attention in recent years [1–3], the proposed method can be applied for the characterization of GaN MOS interfaces.

In Chapter 5, the structure of high-voltage lateral MISFETs was designed. According to the characteristics of the fabricated double and triple reduced surface field (RESURF) MOSFETs, the double RESURF structure is favorable for the reduction of the drift resistance. The device simulation revealed that the breakdown voltage of the two-zone double RESURF MISFETs depends not on individual doses themselves (D_{RES1}, D_{RES2}, and D_{TP}) but on the *net* RESURF1 dose ($D_{RES1} - D_{TP}$) and the *net* RESURF2 dose ($D_{RES2} - D_{TP}$). The optimum *net* RESURF1 dose and *net* RESURF2 dose were $2 \times 10^{12}\,cm^{-2}$ and $10\text{–}12 \times 10^{12}\,cm^{-2}$, respectively. In the simulation, the drift resistance can be decreased to below $15\,m\Omega cm^2$ by increasing the RESURF doses while the *net* RESURF1 and *net* RESURF2 doses were kept at the optimum values. The top-*p* region protects the gate insulators at the OFF-state. The breakdown voltage was kept over 1.2 kV in the double RESURF MISFETs with the optimum *net* RESURF doses. Therefore, the double RESURF MISFETs with the optimum RESURF doses exhibit high breakdown voltage and low drift resistance, as far as the top-*p* dose were varied in the range from $7 \times 10^{12}\,cm^{-2}$ to $15 \times 10^{12}\,cm^{-2}$.

In Chapter 6, the double RESURF MISFETs were fabricated and characterized. The double RESURF structure is effective not only to decrease the drift resistance but also to increase the breakdown voltage as expected from the device simulation. In the fabricated double RESURF MOSFETs with N_2O-grown oxides, the drift resistance was decreased by over 80 % and the breakdown voltage was increased by 400 V, compared with the single RESURF MOSFETs. In addition, the double RESURF MOSFETs exhibit a small temperature dependence of drift resistance (small increase in drift resistance at elevated temperature).

The fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 20 μm exhibited a breakdown voltage of 1540 V and an ON-resistance of $55\,m\Omega cm^2$. In the

case of MOSFET fabricated on the 4H-SiC $(000\bar{1})$ face, the breakdown voltage was 1580 V and the ON-resistance was 40 mΩcm^2. The figure-of-merit (${V_B}^2/R_{ON}$) of the fabricated MOSFETs with normally-OFF characteristics was 30–62 MW/cm^2. A figure-of-merit of 62 MW/cm^2 is the highest value among any lateral MISFETs ever reported and more than 10 times higher than the "Si limit".

7.2 Future Work

Through this study, several issues in SiC MIS device physics have been clarified and superior characteristics could be realized in SiC lateral devices. However, there are still several issues to be solved, and there have emerged several goals to be accomplished in the future.

- **Critical channel length for SiC MISFETs with deep-submicron channel:** The critical channel length for simulated SiC MOSFETs is similar to that for Si MISFETs because the width of the depletion layer from the drain region is almost the same. In the MISFETs with deep-submicron channel ($L_{Ch} < 0.1\,\mu$m), the applied voltage will be decreased. In this case, the width of depletion layer in SiC is wider than that in Si due to its large built-in potential. Therefore, the critical channel length for SiC MISFETs may be longer than that for Si MISFETs. To realize SiC ICs, it is important to reveal the critical channel length for the SiC MISFETs with deep-submicron channel.

- **Structural and chemical analyses of deposited insulators/SiC interface:** Although the remarkable reduction in the interface states could be achieved in this study, the origin of interface state density has not been clarified. The capacitance-voltage (C–V) measurements and secondary ion mass spectroscopy (SIMS) measurements were performed to analyze the electrical and structural properties of SiC MIS structures. For further understanding of the interface states, other technique such as X-ray photoelectron spectroscopy (XPS) and electron probe micro-analysis (EPMA) should be employed to investigate the chemical and microstructural properties of deposited insulators/SiC interface. The detailed analyses on deposited insulators/SiC interface contribute greatly to the understanding of the interface states and hence the channel mobility can further increased.

- **Correlation between scattering mechanism and channel mobility:** In the n-channel MOSFETs with SiO_2-gate insulators, the channel mobility was affected by the charges trapped at the deep states when its density is high. On the other hand, when the density of these charges is low, the channel mobility was limited to 50 cm^2/Vs due to other scattering mechanism. To increase the channel mobility, the scattering centers in the inversion layer of SiC MISFETs should be clarified and eliminated. The

understanding of chemical and microstructural properties mentioned above may give a great help for this analysis.

- **Fabrication and characterization of SiC CMOS circuits:** In this study, both n- and p-channel MISFETs were fabricated. To realize power ICs, the complementary MOS (CMOS) circuits need to be fabricated. In the CMOS circuits, the n- and p-channel MISFETs should operate at low voltage (below 5 V). In the p-channel MISFETs, in particular, the threshold voltage is still high and should be decreased. To receive the full benefit of the high n-channel mobility on the 4H-SiC $(000\bar{1})$ face, the p-channel MISFETs on $(000\bar{1})$ which can function should be realized through process optimization. In addition, to demonstrate the advantages of SiC-based ICs over Si-based ICs, SiC CMOS circuits should be characterized at high temperature (about 300 °C).

- **Characterization of MISFETs on implanted-well regions:** From a practical application standpoint, the MISFETs will be fabricated on implanted-well regions. In general, the doping concentration of the implanted-well regions is higher than $10^{17}\,\mathrm{cm}^{-3}$ to suppress the short-channel effects. The interface properties and the channel mobility of the MISFETs on these implanted-well regions may deteriorate. To put into practical use, it is important to characterize the SiC MISFETs on implanted-well regions and to achieve high channel mobility on these highly-doped well regions.

- **Realization of 600 V-class lateral MISFETs on 6H-SiC:** In this study, 4H-SiC was used for the fabrication of lateral MISFETs with a breakdown voltage over 1 kV. For 600 V-class lateral MISFETs, in which the channel resistance is expected to be higher than the drift resistance because of the short drift length, 6H-SiC possesses the potential properties such as reasonably high-channel mobility in MISFETs (about $100\,\mathrm{cm}^2/\mathrm{Vs}$) [4, 5]. Although low-bulk mobility in 6H-SiC increases the drift resistance significantly in the high-voltage (over 1 kV) MISFETs, 6H-SiC double RESURF MISFETs may demonstrate superior performance to 4H-SiC double RESURF MISFETs in the 600 V or lower voltage range. 600 V-class power ICs with low power loss are strongly desired in the field of home electronics.

- **Further reduction of ON-resistance in lateral high-voltage 4H-SiC MISFETs:** To reduce the drift resistance of lateral MISFETs, a superjunction structure [6] is one of attractive structures. In addition, the three-dimensional gate structure [7] is effective to decrease the channel resistance. The deposited insulators also contribute to the reduction of channel resistance. Although more careful design is required, the lateral high-voltage MISFETs with ultra-low ON-resistance will become reality by combining these structures and processes.

- **Successful demonstration of SiC-based high-voltage smart power ICs:** After the problems mentioned above are solved, SiC-based smart power ICs capable of handling high power with ultra-low loss can be realized.

A market for power devices began to accept SiC Schottky barrier diodes (SBDs), and SiC SBDs have started to be used in home electronics and industry. Although SiC power MISFETs have not come on the market yet, the author believes that SiC power MISFETs, SiC smart power ICs, and all of SiC-based power devices and systems will be widely used in the world to save energy and to preserve the environment while sustaining the economic growth in the foreseeable future.

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Appendix A

Weibull Plots

A.1 Weibull Distribution

When a series of devices are tested, the devices will fail in time (t). In the Weibull distribution function [1], the failure rate ($\lambda(t)$) varies as a power of the device age.

$$\lambda = \frac{\beta}{\tau}\left(\frac{t}{\tau}\right)^{\beta}, \tag{A.1}$$

where β is a constant, which is named as "shape parameter", and τ is also a constant, which is named as "scale parameter".

The cumulative failure rate ($F(t)$) is the probability that the device will fail at or before time (t).

$$F(t) = 1 - \exp\left\{-\left(\frac{t}{\tau}\right)^{\beta}\right\}. \tag{A.2}$$

A.2 Weibull Plots for TDDB Measurements

In time dependent dielectric breakdown (TDDB) measurements, the time is replaced by a charge-to-breakdown (Q_{BD}). Equation A.2 is changed to:

$$F(Q_{\mathrm{BD}}) = 1 - \exp\left\{-\left(\frac{Q_{\mathrm{BD}}}{Q_{\mathrm{BD0}}}\right)^{\beta}\right\}. \tag{A.3}$$

Here, the scale parameter is also changed to Q_{BD0} from τ. From Eq. A.3, the following equation is obtained:

$$\ln(-\ln(1 - F(Q_{\mathrm{BD}}))) = \beta \ln Q_{\mathrm{BD}} - \beta \ln Q_{\mathrm{BD0}}. \tag{A.4}$$

The typical charge-to-breakdown of gate insulators is defined as the value when the left-hand side becomes zero. In addition, by plotting "$\ln(-\ln(1-F))$ vs. $\ln Q_{\mathrm{BD}}$" relationship, the scale parameter (β) is also obtained. (1) When the β is smaller than unity, the failure

rate decreases over time (initial failure). (2) When the β is equal to unity, the failure rate is constant over time (random failure). (3) When the β is larger than unity, the failure rate increases over time (intrinsic failure). The large β means the small variation in the distribution of charge-to-breakdown.

In Chapter 3, the charge-to-breakdown at a cumulative failure rate of 63.2 %, at which "$\ln(-\ln(1-F)) = 0$" ($F = 0.632$) is satisfied, was used as the typical charge-to-breakdown.

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Appendix B

Theoretical Comparison of Si and SiC RESURF MISFETs

B.1 Simple Model for Theoretical Calculation

Theoretical relationship between breakdown voltage and ON-resistance is calculated by using a simple model of reduced surface field (RESURF) metal-insulator-semiconductor field-effect transistor (MISFET). The simple model for the calculation is shown in Fig. B.1. The MISFET shown in Fig. B.1 indicates the half cell of RESURF MISFET. The main component of ON-resistance is expressed as the sum of the channel resistance and the drift resistance. In this calculation, the contact resistance is not considered [1]. The MISFET has a cell pitch of L_{Cell}, a channel length of L_{Ch}, a RESURF length of L_{RES}, and a source/drain pad length of L_{SD}. The device width, which is the length perpendicular to the paper, is W. From the calculation, the prospective performance of SiC RESURF MISFETs is compared with that of Si RESURF MISFETs.

To calculate the breakdown voltage and the ON-resistance, several assumptions were used.

- The drift region is fully depleted from the bottom p-epilayer/n-RESURF junction (Junction A in Fig. B.1) when the drain voltage of V_{D1} is applied. After that, further drain voltage is supported by the fully-depleted RESURF region with almost uniform distribution of the electric field except for the region near the vertical p-epilayer/n-RESURF junction (Junction B in Fig. B.1).

- The electric field crowding (spike field) occurs at the Junction B. Thus, the distribution of the electric field at the surface of the semiconductor (gate insulator/semiconductor interface) can be depicted as shown in Fig. B.2. The electric field crowding at the drain edge is unconsidered.

[1] In the lateral MISFETs, the substrate resistance can be negligible.

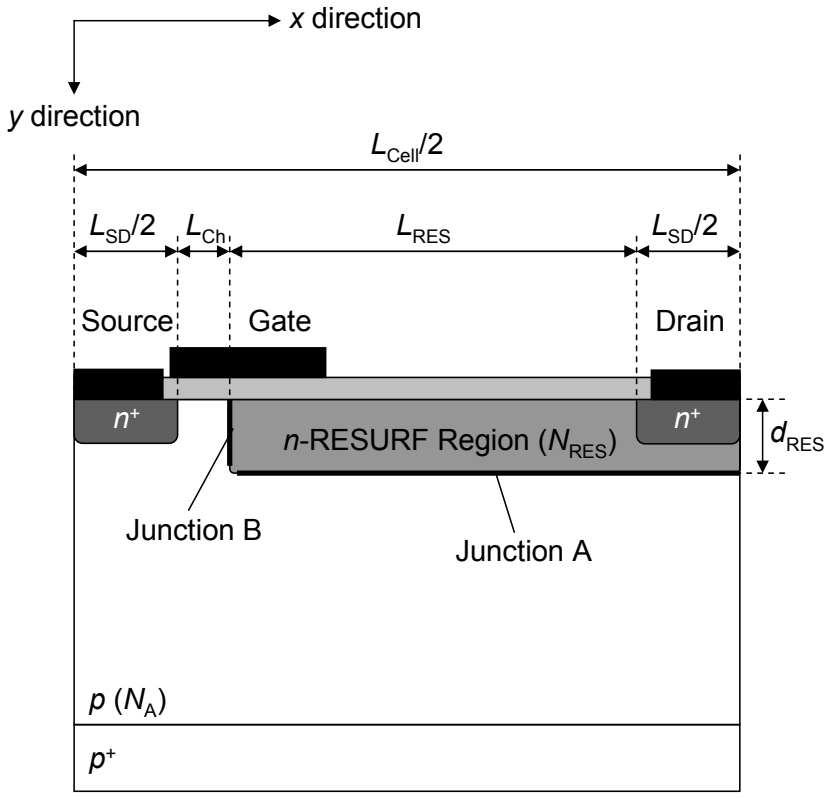


Figure B.1: Schematic structure of RESURF MISFET for the theoretical calculation of breakdown voltage and ON-resistance.

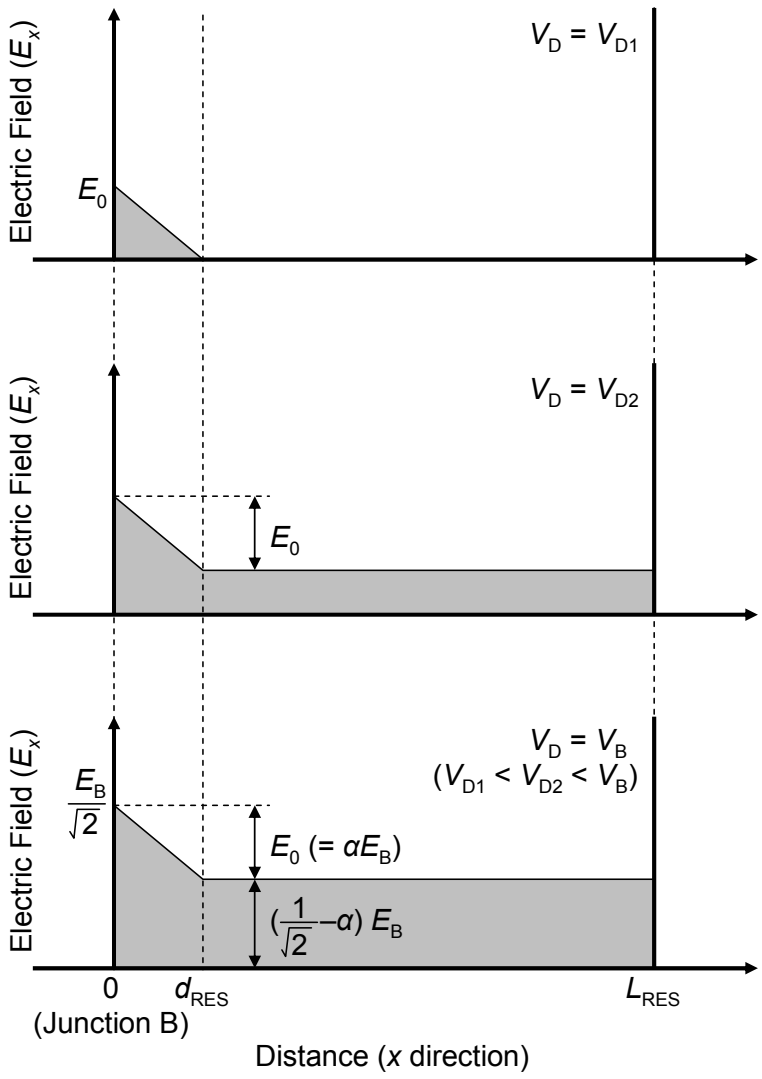


Figure B.2: Electric field distribution at the surface of the semiconductor (MIS interface).

- In the RESURF region, lateral and vertical electric field (E_x and E_y, respectively) is the same ($E_x = E_y$). The electric field in the RESURF region is described by

$$E = \sqrt{{E_x}^2 + {E_y}^2} = \sqrt{2}E_x. \tag{B.1}$$

  The MISFET breaks down only at the Junction B when its spike field reaches $E_{\mathrm{B}}/\sqrt{2}$. In other words, the breakdown takes place when the lateral electric field becomes $E_{\mathrm{B}}/\sqrt{2}$.

- The thickness of p-epilayer is sufficiently thick, and the breakdown at Junction A does not occur. The gate-insulator breakdown is also unconsidered.

- The ionization ratio of donors in the RESURF region is unity. The electron concentration in the RESURF region is equal to the donor concentration of RESURF region (N_{RES}) at the ON-state.

- For the calculation of drift resistance, the width of depletion region extended from the Junction A by built-in potential is neglected.

B.2 Theoretical Calculation of Breakdown Voltage and On-Resistance

Breakdown Voltage

The drain voltage (V_{D1}) to deplete the RESURF region completely is expressed by

$$V_{\mathrm{D1}} = \frac{e(N_{\mathrm{RES}} + N_{\mathrm{A}}){N_{\mathrm{RES}}{d_{\mathrm{RES}}}^2}}{2\varepsilon_{\mathrm{S}}N_{\mathrm{A}}}, \tag{B.2}$$

where e is the elementary charge, ε_{S} the permittivity of the semiconductor, and N_{A} the acceptor concentration of the p-epilayer. At the same time, the electric field at the Junction A and B becomes

$$\begin{aligned} E_0 &= \sqrt{\frac{2eN_{\mathrm{RES}}N_{\mathrm{A}}}{\varepsilon_{\mathrm{S}}(N_{\mathrm{RES}} + N_{\mathrm{A}})}V_{\mathrm{D1}}} \\ &= \frac{eN_{\mathrm{RES}}d_{\mathrm{RES}}}{\varepsilon_{\mathrm{S}}}. \end{aligned} \tag{B.3}$$

The upper graph of Fig. B.2 shows the distribution of the electric field at the MIS interface. The peak electric field is E_0 and the depletion width from the Junction B becomes d_{RES}. After that, the further drain voltage is supported by the fully-depleted RESURF region. Thus, the electric field distribution at a drain bias voltage of V_{D2} ($V_{\mathrm{D1}} < V_{\mathrm{D2}} < V_{\mathrm{B}}$, V_{B}: breakdown voltage) becomes like the middle graph of Fig. B.2. At the breakdown, the spike

field at the Junction B reaches $E_{\rm B}/\sqrt{2}$. At that time, the electric field distribution can be described as the bottom graph of Fig. B.2 and hence the breakdown voltage is given by

$$V_{\rm B} = \frac{E_0 d_{\rm RES}}{2} + \left(\frac{E_{\rm B}}{\sqrt{2}} - E_0\right) L_{\rm RES} = \alpha \frac{E_{\rm B} d_{\rm RES}}{2} + \left(\frac{1}{\sqrt{2}} - \alpha\right) E_{\rm B} L_{\rm RES}. \tag{B.4}$$

Here,

$$\alpha = \frac{E_0}{E_{\rm B}} = \frac{e N_{\rm RES} d_{\rm RES}}{\varepsilon_{\rm S} E_{\rm B}} \leq \frac{1}{\sqrt{2}}. \tag{B.5}$$

By using α, the $N_{\rm RES}$ can be expressed by

$$N_{\rm RES} = \frac{\alpha \varepsilon_{\rm S} E_{\rm B}}{e d_{\rm RES}}. \tag{B.6}$$

Channel Resistance

In this MISFET, the channel resistance ($R_{\rm Ch}$) is described by

$$R_{\rm Ch} = \frac{V_{\rm D}}{I_{\rm D}} \times L_{\rm Cell} W = \frac{L_{\rm Ch} L_{\rm Cell} d_{\rm i}}{2\varepsilon_{\rm i} \mu_{\rm Ch} (V_{\rm G} - V_{\rm T})}, \tag{B.7}$$

where $V_{\rm D}$ is the drain voltage, $I_{\rm D}$ the drain current, $d_{\rm i}$ the gate-insulator thickness, $\varepsilon_{\rm i}$ the permittivity of the gate insulator, $\mu_{\rm Ch}$ the channel mobility, $V_{\rm G}$ the gate voltage, and $V_{\rm T}$ the threshold voltage.

Drift Resistance

The drift resistance is expressed by

$$\begin{aligned} R_{\rm Drift} &= \frac{1}{e\mu_{\rm RES} N_{\rm RES}} \frac{L_{\rm RES}}{2W d_{\rm RES}} \times W L_{\rm Cell} \\ &= \frac{1}{e\mu_{\rm RES} \dfrac{\alpha \varepsilon_{\rm S} E_{\rm B}}{e d_{\rm RES}}} \frac{L_{\rm RES} L_{\rm Cell}}{2 d_{\rm RES}} \\ &= \frac{L_{\rm RES} L_{\rm Cell}}{2\alpha \mu_{\rm RES} \varepsilon_{\rm S} E_{\rm B}}, \end{aligned} \tag{B.8}$$

where $\mu_{\rm RES}$ is the electron mobility in the RESURF region. Here, Eq. B.6 was used.

B.3 Maximum RESURF Dose

A maximum RESURF dose to reduce the RESURF resistance while keeping high breakdown voltage can be theoretically calculated from Eq. B.6. The RESURF dose ($D_{\rm RES}$), which is the same as $N_{\rm RES} \times d_{\rm RES}$, can be described as:

$$D_{\rm RES} = N_{\rm RES} d_{\rm RES} = \frac{\alpha \varepsilon_{\rm S} E_{\rm B}}{e} \leq \frac{\varepsilon_{\rm S} E_{\rm B}}{\sqrt{2} e}. \tag{B.9}$$

Here, $\alpha \leq 1/\sqrt{2}$ is used. From Eq. B.9, the maximum RESURF dose could be calculated to be $1.4 \times 10^{12}\,\mathrm{cm}^{-2}$ in Si RESURF MISFETs and $1.1 \times 10^{13}\,\mathrm{cm}^{-2}$ in 4H-SiC RESURF MISFETs [2]. The maximum RESURF dose for SiC RESURF MISFETs can be increased to about 10 times higher value compared with that for Si RESURF MISFETs because of the high breakdown field of SiC.

B.4 Relationship between Breakdown Voltage and On-Resistance

As described above, the breakdown voltage, the channel resistance, and the drift resistance can be calculated. The specific ON-resistance (R_{ON}) and the breakdown voltage (V_{B}) were summarized as follows.

$$R_{\mathrm{ON}} = R_{\mathrm{Ch}} + R_{\mathrm{Drift}} = \frac{L_{\mathrm{Ch}} L_{\mathrm{Cell}} d_{\mathrm{i}}}{2\varepsilon_{\mathrm{i}} \mu_{\mathrm{Ch}} (V_{\mathrm{G}} - V_{\mathrm{T}})} + \frac{L_{\mathrm{RES}} L_{\mathrm{Cell}}}{2\alpha \mu_{\mathrm{RES}} \varepsilon_{\mathrm{S}} E_{\mathrm{B}}}, \tag{B.10}$$

$$V_{\mathrm{B}} = \alpha \frac{E_{\mathrm{B}} d_{\mathrm{RES}}}{2} + \left(\frac{1}{\sqrt{2}} - \alpha \right) E_{\mathrm{B}} L_{\mathrm{RES}}, \tag{B.11}$$

and

$$\alpha = \frac{e N_{\mathrm{RES}} d_{\mathrm{RES}}}{\varepsilon_{\mathrm{S}} E_{\mathrm{B}}}. \tag{B.12}$$

By using these equations, the relationship between the breakdown voltage and the ON-resistance was calculated. In the calculation of the breakdown voltage and the ON-resistance, the following equations [1, 2] were used to obtain the E_{B} and μ_{RES}:

$$E_{\mathrm{B}} = \frac{2.49 \times 10^6}{1 - \frac{1}{4} \log_{10} \left(\frac{N_{\mathrm{RES}}}{10^{16}\,\mathrm{cm}^{-3}} \right)} \quad \mathrm{V/cm} \tag{B.13}$$

and

$$\mu_{\mathrm{RES}} = \frac{947}{1 + \left(\frac{N_{\mathrm{RES}}}{1.94 \times 10^{17}\,\mathrm{cm}^{-3}} \right)^{0.61}} \quad \mathrm{cm^2/Vs}, \tag{B.14}$$

for SiC RESURF MISFETs. For Si RESURF MISFETs, the following equations were used [3, 4]:

$$E_{\mathrm{B}} = \frac{4 \times 10^5}{1 - \frac{1}{3} \log_{10} \left(\frac{N_{\mathrm{RES}}}{10^{16}\,\mathrm{cm}^{-3}} \right)} \quad \mathrm{V/cm} \tag{B.15}$$

and

$$\mu_{\mathrm{RES}} = 92 + \frac{1268}{1 + \left(\frac{N_{\mathrm{RES}}}{1.3 \times 10^{17}\,\mathrm{cm}^{-3}} \right)^{0.91}} \quad \mathrm{cm^2/Vs}. \tag{B.16}$$

[2] In the calculation, the material properties (the breakdown field and the permittivity of semiconductors) listed in Table 1.1 were used.

The relationship between the calculated breakdown voltage and ON-resistance for Si and SiC RESURF MISFETs is shown in Fig. B.3. The parameters used in the calculation are summarized in Table B.1. These parameters were chosen based on the parameters for the MISFETs fabricated in Chapter 6. In Fig. B.3, the theoretical limits for Si and 4H-SiC unipolar devices are also shown as dashed and solid lines, respectively. In the case of short drift length (10 μm), the maximum breakdown voltage is 210 V for Si RESURF MISFETs and 1690 V for 4H-SiC RESURF MISFETs. In the case of long drift length (20 μm), 4H-SiC RESURF MISFETs show high breakdown voltage over 3000 V. Although SiC MISFETs show higher breakdown voltage than Si MISFETs, the ON-resistance of SiC MISFETs is limited by its high channel resistance, when a low channel mobility of 20 $\mathrm{cm^2/Vs}$ is assumed.

The donor concentration of 4H-SiC RESURF MISFETs can be increased to an about 10 times higher value compared with Si RESURF MISFETs due to its high breakdown field as described in Section B.3. Therefore, the drift resistance of SiC RESURF MISFETs is lower than that of Si RESURF MISFETs. For example, in the case of long drift length, the drift resistance of SiC RESURF MISFET with the highest figure-of-merit was 17.7 $\mathrm{m\Omega cm^2}$ (V_B = 3263 V), which is less than half of the value in Si RESURF MISFET with the highest figure-of-merit (R_Drift = 46.7 $\mathrm{m\Omega cm^2}$, V_B = 327 V). On the other hand, the channel resistance of SiC RESURF MISFETs is much higher than that of Si RESURF MISFETs due to its low channel mobility. The channel resistance of SiC RESURF MISFETs is 16.3 $\mathrm{m\Omega cm^2}$, while that of Si RESURF MISFETs is 0.7 $\mathrm{m\Omega cm^2}$.

Figure B.4 represents the relationship between the ON-resistance and the channel mobility in the 4H-SiC RESURF MISFETs with a drift length of (a) 10 μm and (b) 20 μm. The donor concentration of the RESURF region was fixed at $1 \times 10^{17}\,\mathrm{cm^{-3}}$. A channel length of either 1 μm or 2 μm is used. Other parameters used in the calculation are the same as those listed in Table B.1. The breakdown voltage for the MISFETs with short and long drift length is calculated to be 1260 V and 2490 V, respectively. From Fig. B.4, the increase of channel mobility and the decrease of channel length contribute greatly to the reduction of the ON-resistance. In the case of short drift length (Fig. B.4 (a)), the channel resistance is a dominant component of the ON-resistance when the channel mobility is lower than 40 $\mathrm{cm^2/Vs}$ and 70 $\mathrm{cm^2/Vs}$ in the MISFETs with a channel length of 1 μm and 2 μm, respectively. On the other hand, in the case of long drift length (Fig. B.4 (b)), a channel mobility of 20 $\mathrm{cm^2/Vs}$ and 30 $\mathrm{cm^2/Vs}$ is required to reduce the channel resistance to the same level as the drift resistance in the MISFETs with a channel length of 1 μm and 2 μm, respectively. The increase of channel mobility (over 30–40 $\mathrm{cm^2/Vs}$) is essential to realize low ON-resistance in the 4H-SiC RESURF MISFETs and to benefit from the material properties of SiC.

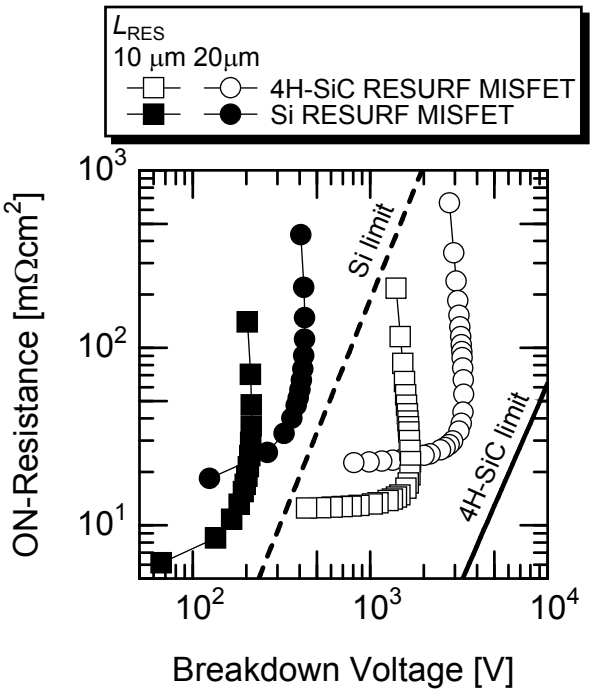
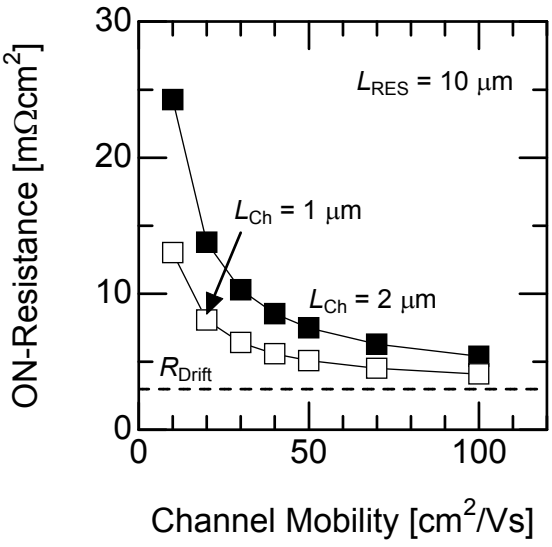


Figure B.3: Relationship between the breakdown voltage and the ON-resistance for the calculated Si and 4H-SiC RESURF MISFETs. Closed boxes and circles denote the Si RESURF MISFETs with a drift length of 10 μm and 20 μm, respectively. Open boxes and circles represent the SiC RESURF MISFETs with a drift length of 10 μm and 20 μm, respectively. Dashed and solid lines show the theoretical limits for the unipolar Si and SiC devices, respectively.

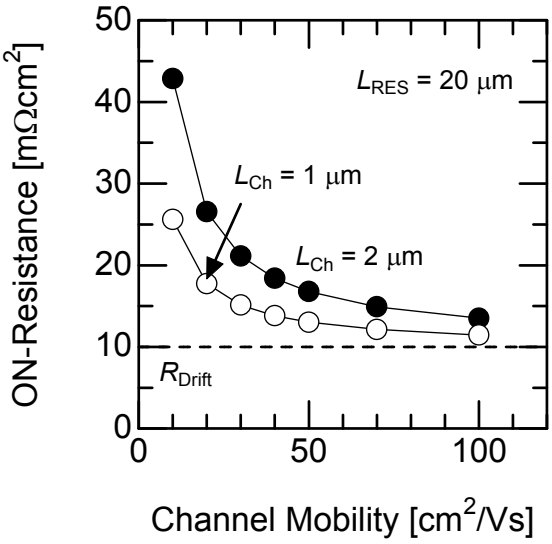
Table B.1: Parameters used in the calculation.

Parameter	Si	4H-SiC
L_{Ch}	2 μm	
L_{RES}	10 μm or 20 μm	
L_{SD}	6 μm	
d_{RES}	0.6 μm	
$\frac{V_{\mathrm{G}} - V_{\mathrm{T}}}{d_{\mathrm{i}}}$	2 MV/cm	
μ_{Ch}	400 cm^2/Vs	20 cm^2/Vs
ε_{S}	11.7ε_0	9.7ε_0
ε_{i}	3.9 ε_0 (SiO_2)	

ε_0: the permittivity of the vacuum



(a)



(b)

Figure B.4: Relationship between the ON-resistance and the channel mobility for the 4H-SiC RESURF MISFETs with a drift length of (a) 10 μm and (b) 20 μm. Open and closed symbols mean the ON-resistance of the MISFETs with a channel length of 1 μm and 2 μm, respectively.

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List of Publications

A. Full Length Papers and Letters

1. T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami,
"Interface Properties of Metal-Oxide-Semiconductor Structures on 4H-SiC {0001} and (11$\bar{2}$0) Formed by N_2O Oxidation,"
Jpn. J. Appl. Phys. **44**, 1213–1218 (2005).

2. M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto,
"Experimental and Theoretical Investigations on Short-Channel Effects in 4H-SiC MOSFETs,"
IEEE Trans. Electron Devices **52**, 1954–1962 (2005).

3. M. Noborio, J. Suda, and T. Kimoto,
"4H-SiC Lateral Double RESURF MOSFETs with Low ON Resistance,"
IEEE Trans. Electron Devices **54**, 1216–1223 (2007).

4. M. Noborio, J. Suda, and T. Kimoto,
"4H-SiC MIS Capacitors and MISFETs with Deposited SiN_x/SiO_2 Stack-Gate Structures,"
IEEE Trans. Electron Devices **55**, 2054–2060 (2008).

5. M. Noborio, J. Suda, and T. Kimoto,
"Improved Performance of 4H-SiC Double Reduced Surface Field Metal-Oxide-Semiconductor Field-Effect Transistors by Increasing RESURF Doses,"
Appl. Phys. Express **1**, art. no. 101403 (2008).

6. K. Yamaji, M. Noborio, J. Suda, and T. Kimoto,
"Improvement of Channel Mobility in Inversion-Type *N*-Channel GaN Metal-Oxide-Semiconductor Field-Effect Transistor by High-Temperature Annealing,"
Jpn. J. Appl. Phys. **47**, 7784–7787 (2008).

7. M. Noborio, J. Suda, and T. Kimoto,
"N_2O-Grown Oxides/4H-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) Interface Properties Characterized by Using *P*-Type Gate-Controlled Diodes,"
Appl. Phys. Lett. **93**, art. no. 193510 (2008).

8. M. Noborio, T. Kimoto, S. Reshanov, S. Beljakowa, T. Frank, B. Zippelius, M. Krieger, and G. Pensl,
"4H-SiC Metal-Oxide-Semiconductor Field-Effect Transistors with Overoxidation Layer of N^+- and Al^+-Implanted Surface,"
to be submitted to Jpn. J. Appl. Phys.

9. M. Noborio, J. Suda, and T. Kimoto,
"Influence of Effective Fixed Charges on Short-Channel Effects in SiC MOSFETs"
in preparation.

10. M. Noborio, J. Suda, and T. Kimoto,
"4H-SiC *P*-Channel MISFETs with Deposited Insulators"
in preparation.

11. M. Noborio, J. Suda, and T. Kimoto,
"1580 V-40 mΩcm^2 Double RESURF MOSFETs on 4H-SiC (000$\bar{1}$)"
in preparation.

B. Proceedings of International Conferences

1. T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami,
"MOS Interface Properties and MOSFET Performance on 4H-SiC {0001} and Non-Basal Faces by N_2O Oxidation,"
Mater. Res. Soc. Symp. Proc. **815**, 199–204 (2004).
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2. T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami,
"MOS Interface Properties and MOSFET Performance on 4H-SiC {0001} and (11$\bar{2}$0) Processed by N_2O Oxidation,"
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5. T. Kimoto, H. Kawano, M. Noborio, J. Suda, and H. Matsunami,
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10. M. Noborio, J. Suda, and T. Kimoto,
"Enhanced Channel Mobility in 4H-SiC MISFETs by Utilizing Deposited SiN/SiO_2 Stack Gate Structures,"
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11. K. Yamaji, M. Noborio, J. Suda, and T. Kimoto,
"Improvement of Channel Mobility in Inversion-Type N-Channel GaN MOSFETs by High-Temperature Annealing,"
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12. M. Noborio, J. Suda, and T. Kimoto,
"4H-SiC Double RESURF MOSFETs with a Record Performance by Increasing RESURF Dose,"
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13. M. Noborio, J. Suda, and T. Kimoto,
"High Channel Mobility in P-Channel MOSFETs Fabricated on 4H-SiC (0001) and Non-Basal Faces,"
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14. M. Noborio, J. Suda, and T. Kimoto,
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"First Demonstration of SiC MISFETs with 4H-AlN Gate Dielectric Heteroepitaxially-Grown on 4H-SiC $(11\bar{2}0)$,"
(*European Conf. on Silicon Carbide and Related Materials 2008*, Barcelona, Spain, 2008.)

16. Y. Nanen, H. Yoshioka, M. Noborio, J. Suda, and T. Kimoto,
"Improved On-Current of 4H-SiC MOSFET with a Three-Dimensional Gate Structure,"
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18. S. Reshanov, S. Beljakowa, T. Frank, B. Zippelius, G. Pensl, M. Noborio, and T. Kimoto,
"High Channel Mobility of 4H-SiC MOSFETs Fabricated by Overoxidation of the N-/Al-Coimplanted Surface Layer,"
submitted to Mater. Sci. Forum
(*European Conf. on Silicon Carbide and Related Materials 2008*, Barcelona, Spain, 2008.)

C. Review Paper

1. M. Noborio, J. Suda, T. Kimoto, S. Reshanov, and M. Krieger,
"4H-SiC MISFETs with N-Contained Insulators"
to be submitted to physica status solidi (b)