

# Simulation and Experimental Study on the Junction Termination Structure for High-Voltage 4H-SiC PiN Diodes

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**Abstract**—Designing and fabrication of 10-kV 4H-SiC PiN diodes with an improved junction termination structure have been investigated. An improved bevel mesa structure and a single-zone junction termination extension (JTE) have been employed to achieve a high breakdown voltage ( $\geq 10$  kV). The improved bevel mesa structure, nearly a vertical sidewall at the edge of the p-n junction and a gradual slope at the mesa bottom, has been fabricated by reactive ion etching. The effectiveness of the improved bevel mesa structure has been experimentally demonstrated. The JTE region has been optimized by device simulation, and the JTE dose dependence of the breakdown voltage has been compared with experimental results. A 4H-SiC PiN diode with a JTE dose of  $1.1 \times 10^{13}$  cm<sup>-2</sup> has exhibited a high blocking voltage of 10.2 kV. The locations of electric field crowding and breakdown are also discussed.

**Index Terms**—Bevel mesa, junction termination extension (JTE), PiN, silicon carbide (SiC), simulation.

## I. INTRODUCTION

SILICON carbide (SiC) is an attractive semiconductor for high-voltage, high-temperature, and high-frequency devices due to its excellent electrical and physical properties [1], [2]. In recent years, high-voltage 4H-SiC Schottky barrier diodes are in the market [3], and SiC junction field-effect transistors (JFETs) [4] and metal-oxide-semiconductor FETs (MOSFETs) [5], [6] have been intensively developed as power switches, mainly for 600- to 1700-V applications. To realize advanced electric power networks, very high-voltage (more than several-kilovolts) SiC bipolar devices are superior to unipolar devices in terms of lower on-resistance, owing to the effect of conductivity modulation.

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In the literatures, several SiC diodes and switches with a very high breakdown voltage greater than 10 kV have been demonstrated [7]–[12]. However, fundamental studies on the junction termination structure for such very high voltage devices are still limited. Several edge termination structures have been investigated, involving guard rings [13], [14], multijunction termination extensions (multi-JTEs) [15]–[17], multi-JTEs combined with guard rings [18], and mesa combined with JTEs [7], [19]. Among these termination structures, the mesa structure combined with JTEs has been accepted as one of the most effective structures for very high voltage devices [20]. Effects in reducing electric field crowding should strongly depend on the mesa shape and the JTE dose, details that have not been reported.

In this paper, the mesa shape has been improved for the alleviation of electric field crowding at the mesa edge. The improved bevel mesa structure, formed by reactive ion etching (RIE), has a nearly vertical sidewall at the edge of the p-n junction and a gradual slope at the mesa bottom. A single-zone JTE has been employed, and the optimization of the JTE is also investigated by means of device simulation. Employing the improved bevel mesa structure combined with an optimized JTE, a 10-kV 4H-SiC PiN diode is realized. The fabrication process and the effectiveness of the improved bevel mesa structure are presented. In addition, a comparison between the simulated and experimental blocking voltages of PiN diodes is also discussed.

## II. CONCEPT AND FABRICATION PROCESS OF THE IMPROVED BEVEL MESA STRUCTURE

Fig. 1 shows various termination structures employed for high-voltage SiC PiN diodes (the JTE region is not indicated). In the planar structure shown in Fig. 1(a), the electric field crowding takes place at the edge of the p-n junction (dotted circle A). In the vertical mesa structure shown in Fig. 1(b), the electric field crowding may occur at the right-angled corner of the mesa bottom, shown as the dotted circle B. By employing the bevel mesa structure shown in Fig. 1(c), the electric field crowding at the right-angled corner (dotted circle C) can be alleviated. However, the negative bevel mesa structure near the p-n junction (dotted circle D) enhances the electric field crowding. The improved bevel mesa structure fabricated in this paper is shown in Fig. 1(d): a rounded corner at the mesa bottom and a nearly vertical sidewall at the edge of the p-n junction are

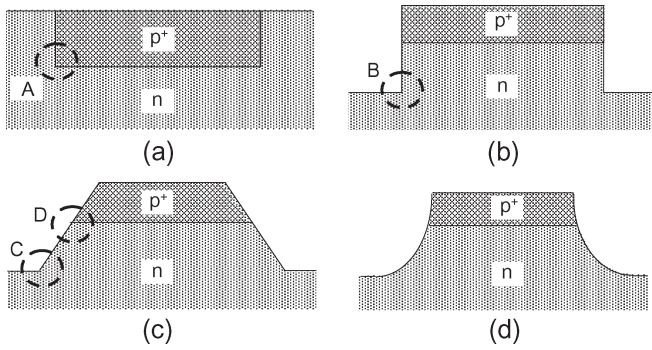


Fig. 1. Various PiN structures. (a) Planar structure. (b) Vertical mesa structure. (c) Bevel mesa structure. (d) Improved bevel mesa structure.

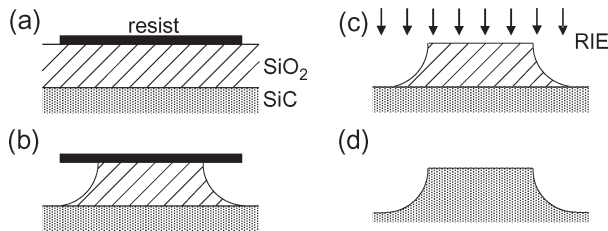


Fig. 2. Fabrication process of the improved bevel mesa structure. (a) SiO<sub>2</sub> deposition and resist patterning. (b) SiO<sub>2</sub> wet etching. (c) RIE after resist removal. (d) SiC-improved bevel mesa structure.

formed. With this structure, the electric field crowding caused by a right-angled corner and a negative bevel mesa structure can be minimized.

In this paper, the improved bevel mesa structure was formed by RIE with a SiO<sub>2</sub> bevel mask. Fig. 2 shows the fabrication process of the improved bevel mesa structure. The process consists of the following steps.

- SiO<sub>2</sub> was deposited on a SiC epilayer by plasma-enhanced chemical vapor deposition (PECVD), and a photoresist was patterned on SiO<sub>2</sub>.
- SiO<sub>2</sub> was etched by BHF, and a SiO<sub>2</sub> bevel mask was formed.
- The photoresist was removed, and the SiC epilayer was etched by RIE with a CF<sub>4</sub>-O<sub>2</sub> chemistry.
- SiO<sub>2</sub> was removed by BHF, leaving the improved bevel mesa structure.

The cross-sectional SEM image of a SiO<sub>2</sub> bevel mask formed by BHF etching is shown in Fig. 3(a). The rounded sidewall of SiO<sub>2</sub> was formed by isotropic wet etching. Fig. 3(b) and (c) shows the cross-sectional SEM images of SiC mesa structures after RIE. The shape of the SiC mesa structures strongly depends on the conditions of RIE. In the case of the nonoptimized RIE conditions, i.e., high RF power and high etching selectivity (CF<sub>4</sub>: 5 sccm; O<sub>2</sub>: 10 sccm; pressure: 50 Pa; RF power: 150 W; etching selectivity SiC/SiO<sub>2</sub>: 1.8; etching rate of SiC: 310 nm/min), the rounded corner of the improved bevel mesa structure is not formed due to the high etching selectivity, as shown in Fig. 3(b). By optimizing the RIE conditions, i.e., low RF power and low etching selectivity (CF<sub>4</sub>: 5 sccm; O<sub>2</sub>: 10 sccm; pressure: 50 Pa; RF power: 75 W; etching selectivity SiC/SiO<sub>2</sub>: 1.0; etching rate of SiC: 75 nm/min), the shape of the SiO<sub>2</sub> bevel mask is reproduced in the etched SiC,

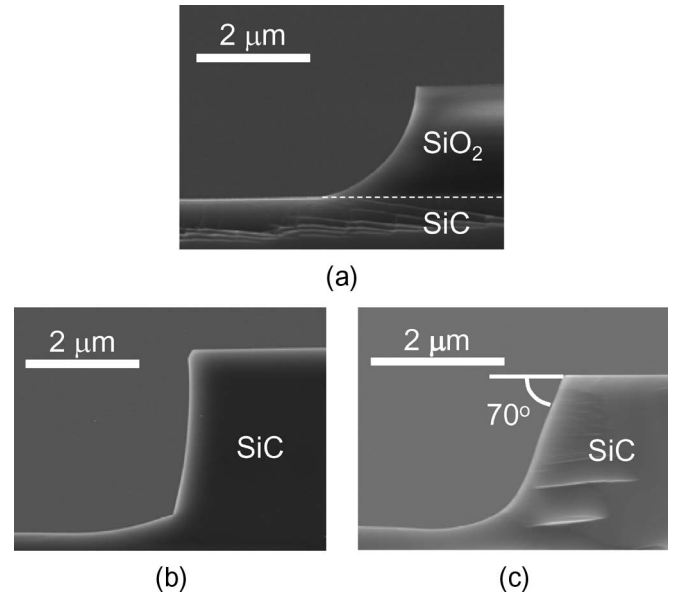


Fig. 3. Cross-sectional SEM images of SiC mesa structures after RIE. (a) SiO<sub>2</sub> bevel mask formed by BHF etching. (b) Nearly vertical mesa formed by the nonoptimized RIE condition. (c) Improved bevel mesa formed with the optimized RIE condition.

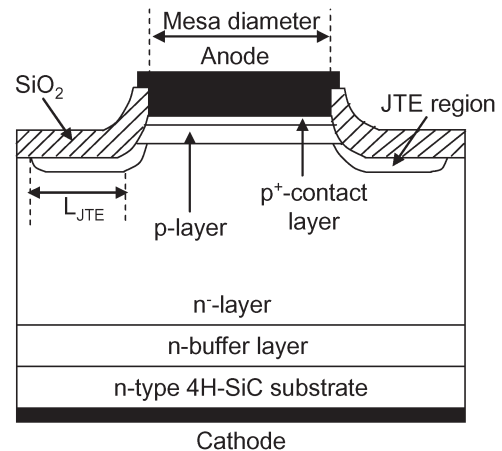


Fig. 4. Structure of the 4H-SiC PiN diode.

as shown in Fig. 3(c). The bevel angle of the present mesa structure was about 70°.

### III. DEVICE SIMULATION FOR THE OPTIMUM JTE REGION

Fig. 4 shows the schematic illustration of a 4H-SiC PiN diode simulated and fabricated in this paper. The JTE region was introduced in addition to the improved bevel mesa structure. To achieve high breakdown voltages, the JTE dose and the JTE length have been optimized by 2-D device simulation (ISE-DESSIS). The JTE dose should be optimized so that the JTE region is completely depleted at the desired reverse voltage to spread the equipotential lines toward the lateral direction. In the device simulation, the thickness and the donor concentration of the n<sup>-</sup> layer were fixed at 95 μm and 4 × 10<sup>14</sup> cm<sup>-3</sup>, respectively. The height of the improved bevel mesa is 2 μm. The depth and the acceptor concentration of the p-layer were 0.8 μm and 1 × 10<sup>20</sup> cm<sup>-3</sup>, respectively. The JTE dose was

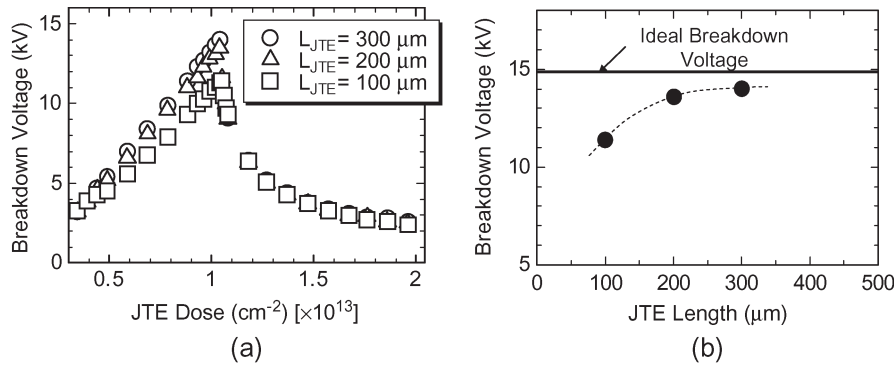


Fig. 5. (a) JTE dose dependence of the simulated breakdown voltage for 4H-SiC PiN diodes with an improved bevel mesa structure. (b) JTE length dependence of the simulated breakdown voltage.

changed from  $0.3 \times 10^{13}$  to  $2.0 \times 10^{13} \text{ cm}^{-2}$  to investigate the dependence of the breakdown voltage on the JTE dose. The JTE length was changed from 100 to 300  $\mu\text{m}$  to investigate the JTE length dependence. The SiC/SiO<sub>2</sub> interface charge was not considered in the simulation. A more accurate breakdown voltage should be obtained from the ionization integral in the simulation. However, the breakdown of a simulated device was defined when the maximum electric field in SiC reaches 3.0 MV/cm to simplify the simulation.

Fig. 5(a) shows the simulated breakdown voltage as a function of the JTE dose. The open circles, open triangles, and open squares denote the simulated breakdown voltage for the JTE length of 300, 200, and 100  $\mu\text{m}$ , respectively. The simulated breakdown voltage exhibited a maximum value at the optimum JTE dose of  $1.0 \times 10^{13} \text{ cm}^{-2}$  irrespective of the JTE length. Fig. 5(b) depicts the JTE length dependence of the breakdown voltage with the optimum JTE dose of  $1.0 \times 10^{13} \text{ cm}^{-2}$ . The highest simulated voltages are 11.4, 13.5, and 14.0 kV for JTE lengths of 100, 200, and 300  $\mu\text{m}$ , respectively. The simulated breakdown voltage begins to saturate at a JTE length of 200  $\mu\text{m}$ , indicating that a 200- $\mu\text{m}$ -long JTE region may be sufficient to realize 10-kV SiC devices.

Fig. 6 shows the simulated equipotential lines at a reverse voltage of 10 kV with a low JTE dose of  $0.4 \times 10^{13} \text{ cm}^{-2}$  [Fig. 6(a)], a high JTE dose of  $1.6 \times 10^{13} \text{ cm}^{-2}$  [Fig. 6(b)], and the optimum JTE dose of  $1.0 \times 10^{13} \text{ cm}^{-2}$  [Fig. 6(c)]. In this simulation, the JTE length was 200  $\mu\text{m}$ . In the case of a low JTE dose, the JTE region completely depletes at a low reverse voltage, and the equipotential lines severely curve at the mesa edge, as shown in Fig. 6(a). On the other hand, when the JTE dose is higher than the optimum value, electric field crowding takes place at the outer edge of the JTE region, as shown in Fig. 6(b), because the JTE region does not deplete even at high reverse voltages. By optimizing the JTE dose, the equipotential lines can be widely distributed in the depleted JTE region, as shown in Fig. 6(c).

#### IV. DIODE FABRICATION

Thick (90–125  $\mu\text{m}$ ) n<sup>-</sup> epilayers intentionally doped to  $(2\text{--}7) \times 10^{14} \text{ cm}^{-3}$  have been grown on n-type 8° off-axis 4H-SiC(0001) substrates. Epitaxial growth was performed by horizontal hot-wall chemical vapor deposition (CVD) with a

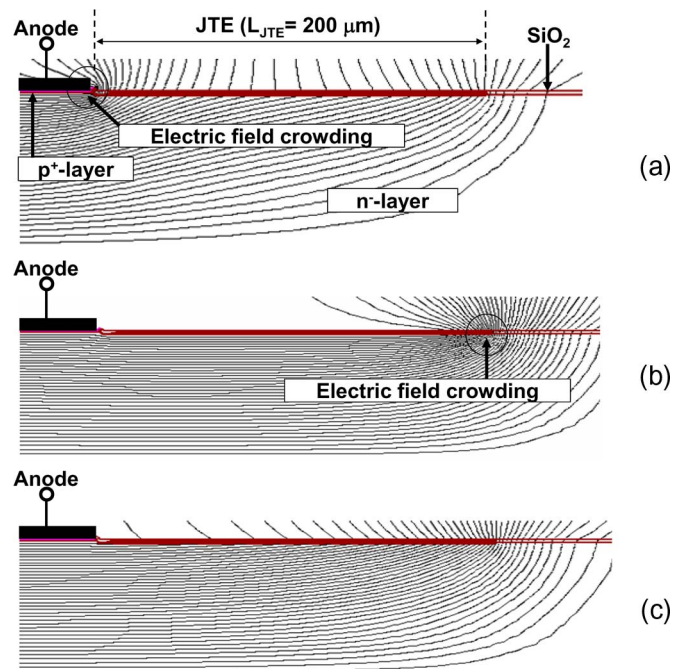


Fig. 6. Simulated equipotential lines (pitch: 250 V) in 4H-SiC PiN diodes for (a) low JTE dose of  $0.4 \times 10^{13} \text{ cm}^{-2}$ , (b) high JTE dose of  $1.6 \times 10^{13} \text{ cm}^{-2}$ , and (c) optimum JTE dose of  $1.0 \times 10^{13} \text{ cm}^{-2}$ .

high growth rate of 45  $\mu\text{m}/\text{h}$  [21]. The p-anode (depth: 0.8  $\mu\text{m}$ ) and the contact layer (depth: 0.2  $\mu\text{m}$ ) were formed by Al ion implantation with a concentration of  $2 \times 10^{18}$  and  $2 \times 10^{20} \text{ cm}^{-3}$ , respectively. The single-zone JTE region (depth: 0.8  $\mu\text{m}$ ) was also formed by Al ion implantation at room temperature. The JTE dose was changed from  $0.4 \times 10^{13}$  to  $1.6 \times 10^{13} \text{ cm}^{-2}$  to investigate the dependence of the breakdown voltage on the JTE dose. After Al ion implantation, all the implanted species in the anode and in the JTE region were activated by annealing at 1700 °C for 30 min with a carbon cap to suppress surface roughening [22], [23]. The typical JTE length  $L_{\text{JTE}}$  and the mesa diameter were (100–300) and (300–800)  $\mu\text{m}$ , respectively. For surface passivation, thermal oxidation was carried out in dry N<sub>2</sub>O ambient at 1330 °C for 4 h [24], and, subsequently, a 2.0- $\mu\text{m}$ -thick SiO<sub>2</sub> layer was deposited by PECVD. Ti/Al and Ni annealed at 1000 °C for 3 min were used as ohmic contacts on the anode and the cathode, respectively.

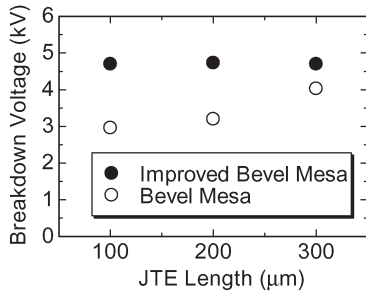


Fig. 7. Breakdown voltage as a function of the JTE length for 4H-SiC PiN diodes with (o) bevel mesa and (●) improved bevel mesa.

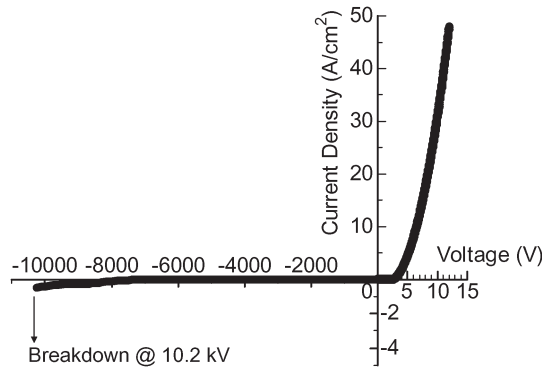


Fig. 8. Current density versus voltage characteristics of a 4H-SiC PiN diode ( $N_d$ :  $4 \times 10^{14} \text{ cm}^{-3}$ ; epi layer thickness:  $92 \text{ } \mu\text{m}$ ; JTE dose:  $1.1 \times 10^{13} \text{ cm}^{-2}$ ; JTE length:  $200 \text{ } \mu\text{m}$ ).

## V. EXPERIMENTAL RESULTS AND DISCUSSION

To experimentally investigate the effectiveness of the improved bevel mesa structure, the breakdown voltages of the two mesa structures shown in Fig. 1(c) and (d) were compared. A thick  $n^-$  epilayer (donor concentration:  $2 \times 10^{14} \text{ cm}^{-3}$ ; thickness:  $100 \text{ } \mu\text{m}$ ) was used. The diodes were processed at the same time except for the mesa formation. The bevel mesa structure has a bevel angle of  $35^\circ$ . Both diodes have a mesa height of  $1.5 \text{ } \mu\text{m}$ . The JTE dose of these diodes was  $0.7 \times 10^{13} \text{ cm}^{-2}$ , so that the electric field crowding should occur at the mesa edge.

Fig. 7 shows the dependence of the breakdown voltage on the JTE length of the bevel mesa and the improved bevel mesa. The breakdown voltage of the improved bevel mesa is clearly higher than that of the bevel mesa at any JTE length. This result means that the electric field crowding at the mesa edge in the normal bevel mesa was enhanced by the shallow bevel angle.

Fig. 8 shows the current density versus voltage characteristics of a 10-kV 4H-SiC PiN diode at room temperature. The donor concentration and the thickness of the  $n^-$  layer are  $4 \times 10^{14} \text{ cm}^{-3}$  and  $92 \text{ } \mu\text{m}$ , respectively. The diode has a mesa diameter of  $350 \text{ } \mu\text{m}$  and a mesa height of  $2.0 \text{ } \mu\text{m}$ . The JTE dose is  $1.1 \times 10^{13} \text{ cm}^{-2}$  (700 keV:  $3.19 \times 10^{12} \text{ cm}^{-2}$ ; 450 keV:  $2.78 \times 10^{12} \text{ cm}^{-2}$ ; 280 keV:  $2.1 \times 10^{12} \text{ cm}^{-2}$ ; 170 keV:  $1.28 \times 10^{12} \text{ cm}^{-2}$ ; 100 keV:  $7.91 \times 10^{11} \text{ cm}^{-2}$ ; 55 keV:  $4.69 \times 10^{11} \text{ cm}^{-2}$ ; 26 keV:  $2.57 \times 10^{11} \text{ cm}^{-2}$ ; 10 keV:  $1.34 \times 10^{11} \text{ cm}^{-2}$ ), and the JTE length is  $200 \text{ } \mu\text{m}$ . The differential on-resistance obtained from forward characteristics was  $95 \text{ m}\Omega \cdot \text{cm}^2$ . Under the forward-bias condition, blue electroluminescence was mainly observed in the p-type anode layer.

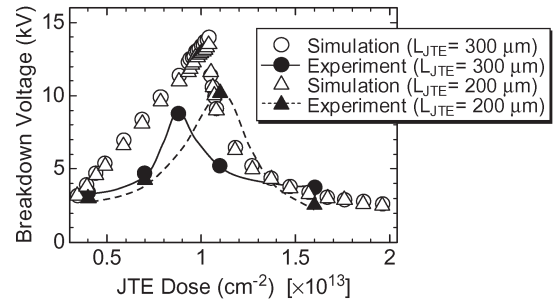


Fig. 9. JTE dose dependence of the experimental breakdown voltage of fabricated 4H-SiC PiN diodes with a JTE length of (▲)  $200 \text{ } \mu\text{m}$  and (●)  $300 \text{ } \mu\text{m}$ . The corresponding simulated results are also plotted for comparison.

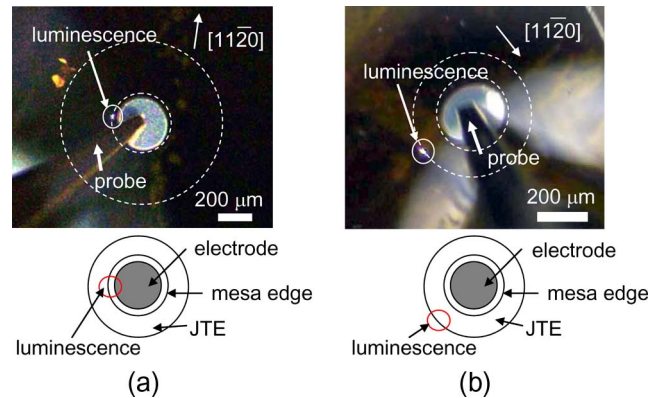


Fig. 10. Luminescence from 4H-SiC PiN diodes at breakdown. JTE dose: (a)  $7 \times 10^{12} \text{ cm}^{-2}$  ( $V_B = 4.0 \text{ kV}$ ) and (b)  $1.6 \times 10^{13} \text{ cm}^{-2}$  ( $V_B = 3.0 \text{ kV}$ ).

The diode has exhibited a high blocking voltage of 10.2 kV, which corresponds to about 72% of a parallel-plane breakdown voltage for the epilayer. The reverse characteristics were measured by the dc voltage supply; thus, the breakdown was mostly destructive.

Fig. 9 represents the dependence of the experimental breakdown voltage on the JTE dose, measured at room temperature. Closed triangles and closed circles denote the experimental results for JTE lengths of 200 and 300  $\mu\text{m}$ , respectively. The thickness and the donor concentration of an  $n^-$  layer are (85–100)  $\mu\text{m}$  and  $(3\text{--}5) \times 10^{14} \text{ cm}^{-3}$ , respectively. With these epilayers, almost the same parallel-plane breakdown voltage of 14.0 kV is expected. A mesa diameter and a mesa height of a diode are 350 and 2.0  $\mu\text{m}$ , respectively. The simulated results are also plotted in the same figure. The experimental results showed a good agreement with the simulated results in the trend. The difference in the absolute values of the breakdown voltage between simulated and experimental results may be caused by RIE damage or differences between the simulated model and the real device. For example, the mesa structure of the simulated model does not perfectly reproduce the shape of the experimental diodes, and the experimental donor concentration of  $n^-$  layer is not exactly the same as the value of  $4 \times 10^{14} \text{ cm}^{-3}$  in the simulation.

Fig. 10 reveals the photographs of PiN diodes just before breakdown for a low JTE dose of  $7 \times 10^{12} \text{ cm}^{-2}$  [ $V_B = 4.0 \text{ kV}$ ; Fig. 10(a)] and a high JTE dose of  $1.6 \times 10^{13} \text{ cm}^{-2}$  [ $V_B = 3.0 \text{ kV}$ ; Fig. 10(b)]. Luminescence, as a result of impact

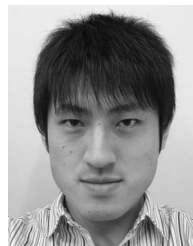
multiplication, was observed at the mesa edge for the low JTE dose [Fig. 10(a)] and at the outer edge of the JTE region for the high JTE dose [Fig. 10(b)]. This observation is in a good agreement with the simulation, as shown in Fig. 6.

## VI. CONCLUSION

We have simulated and fabricated high-voltage 4H-SiC PiN diodes with an improved junction termination structure. The fabrication process of an improved bevel mesa structure, a nearly vertical sidewall at the p-n junction and a rounded corner at the mesa bottom, was presented. For the mesa preparation, a SiO<sub>2</sub> bevel mask was used in the RIE process. The key RIE conditions for the formation of the improved bevel mesa structure were low RF power (75 W) and low SiC/SiO<sub>2</sub> etching selectivity of 1.0. The dose and the length of a single-zone JTE were optimized by means of device simulation. The minimum JTE length and the optimum JTE dose obtained from the simulation of 10-kV PiN diodes were 200 μm and  $1.0 \times 10^{13}$  cm<sup>-2</sup>, respectively. 4H-SiC PiN diodes with a JTE dose of  $(0.4\text{--}1.6) \times 10^{13}$  cm<sup>-2</sup> have been fabricated on thick and lightly doped epilayers grown at a high growth rate of 45 μm/h. A 4H-SiC PiN diode (n<sup>-</sup> layer:  $4 \times 10^{14}$  cm<sup>-3</sup>, 92 μm) with an improved bevel mesa structure (JTE dose:  $1.1 \times 10^{13}$  cm<sup>-2</sup>; JTE length: 200 μm) exhibited a high blocking voltage of 10.2 kV. The dependence of the breakdown voltage on the JTE dose observed in the fabricated diodes showed a good agreement with the simulated results in the trend. The location of breakdown was discussed in terms of simulated equipotential lines and luminescence observed in experiments.

## REFERENCES

- [1] H. Matsunami and T. Kimoto, "Step-controlled epitaxial growth of SiC: High quality homoepitaxy," *Mater. Sci. Eng.*, vol. R20, no. 3, pp. 125–166, 1997.
- [2] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 645–655, Mar. 1993.
- [3] thinQ!. [Online]. Available: <http://www.infineon.com/>
- [4] P. Friedrichs, H. Mitlehner, R. Kaltschmidt, U. Weinert, W. Bartsch, C. Hecht, K. O. Dohnke, B. Weis, and D. Stephani, "Static and dynamic characteristics of 4H-SiC JFETs designed for different blocking categories," *Mater. Sci. Forum*, vol. 338–342, pp. 1243–1246, 2000.
- [5] M. Matin, A. Saha, and J. A. Cooper, Jr., "A self-aligned process for high-voltage, short-channel vertical DMOSFETs in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1721–1725, Oct. 2004.
- [6] S. Harada, M. Kato, M. Okamoto, T. Yatsuo, K. Fukuda, and K. Arai, "Low on-resistance in inversion channel IEMOSFET formed on 4H-SiC C-face substrate," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2006, pp. 125–128.
- [7] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. W. Palmour, and T. Hayashi, "12–19 kV 4H-SiC PiN diodes with low power loss," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2001, pp. 27–30.
- [8] R. Singh, K. G. Irvine, J. T. Richmond, and J. W. Palmour, "High-temperature performance of 10 kilovolts, 200 amperes (pulsed) 4H-SiC PiN rectifiers," *Mater. Sci. Forum*, vol. 389–393, p. 1265, 2002.
- [9] J. H. Zhao, P. Alexandrov, and X. Li, "Demonstration of the first 10-kV 4H-SiC Schottky barrier diodes," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 402–404, Jun. 2003.
- [10] J. H. Zhao, P. Alexandrov, J. Zhang, and X. Li, "Fabrication and characterization of 11-kV normally off 4H-SiC trench-and-implanted vertical junction FET," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 474–476, Jul. 2004.
- [11] Q. Zhang, H.-R. Chang, M. Gomez, C. Bui, E. Hanna, J. A. Higgins, T. Isaacs-Smith, and J. R. Williams, "10 kV trench gate IGBTs on 4H-SiC," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 303–306.
- [12] S. H. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, and A. Hefner, "10 kV, 5A 4H-SiC power DMOSFET," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2006, pp. 265–268.
- [13] H. Onose, S. Oikawa, T. Yatsuo, and Yutaka, "Over 2000 V FLR termination technologies for SiC high voltage devices," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 245–248.
- [14] D. C. Sheridan, G. Niu, J. N. Merrett, J. D. Cressler, C. Ellis, and C. C. Tin, "Design and fabrication of planar guard ring termination for high-voltage SiC diodes," *Solid State Electron.*, vol. 44, no. 8, pp. 1367–1372, Aug. 2000.
- [15] D. Peters, P. Friedrichs, H. Mitlehner, R. Schoerner, U. Weinert, B. Weis, and D. Stephani, "Characterization of fast 4.5 kV SiC P-N diodes," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 241–244.
- [16] H. Lendenmann, F. Dahlquist, J. P. Bergman, H. Bleichner, and C. Hallin, "High-power SiC diodes: Characteristics, reliability and relation to material defects," *Mater. Sci. Forum*, vol. 389–393, pp. 1259–1264, 2002.
- [17] J. B. Fedison, N. Ramungul, T. P. Chow, M. Ghezzi, and J. W. Kretschmer, "Electrical characteristics of 4.5 kV implanted anode 4H-SiC P-I-N junction rectifiers," *IEEE Electron Devices Lett.*, vol. 22, no. 3, pp. 130–132, Mar. 2001.
- [18] R. Pérez, D. Tournier, A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán, "Planar edge termination design and technology considerations for 1.7-kV 4H-SiC PiN diodes," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2309–2316, Oct. 2005.
- [19] R. Singh, J. A. Cooper, Jr., M. R. Melloch, T. P. Chow, and J. W. Palmour, "SiC power Schottky and PiN diodes," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 665–672, Apr. 2002.
- [20] Y. Sugawara, K. Asano, R. Singh, and J. W. Palmour, "6.2 kV 4H-SiC pin diode with low forward voltage drop," *Mater. Sci. Forum*, vol. 338–342, pp. 1371–1374, 2000.
- [21] T. Hori, K. Danno, and T. Kimoto, "Fast homoepitaxial growth of 4H-SiC with low basal-plane dislocation density and low trap concentration by hot-wall chemical vapor deposition," *J. Cryst. Growth*, vol. 306, no. 2, pp. 297–302, Aug. 2007.
- [22] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, "Electronic behaviors of high-dose phosphorus-ion implanted 4H-SiC (0001)," *J. Appl. Phys.*, vol. 96, no. 1, pp. 224–228, Jul. 2004.
- [23] Y. Negoro, T. Kimoto, and H. Matsunami, "Carrier compensation near tail region in aluminum- or boron-implanted 4H-SiC (0001)," *J. Appl. Phys.*, vol. 98, no. 4, pp. 043 709-1–043 709-7, Aug. 2005.
- [24] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami, "Interface properties of metal-oxide-semiconductor structures on 4H-SiC{0001} and (11–20) formed by N<sub>2</sub>O oxidation," *Jpn. J. Appl. Phys.*, vol. 44, no. 3, pp. 1213–1218, 2005.



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