On Design Verification
between Different Levels of Abstraction
Using Regular Temporal Logic
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1 Introduction

The progress of VLSI technology makes it a pressing need to establish methods for verifying the correctness of logic design. In order to verify whether a designed system satisfies a specification for it, formal verification methods have been developed.

In logic design, hierarchical design methodology is adopted to manage complex logic systems. Our main concern is to develop a formal verification method applicable to hierarchical design.

We consider formal verification of sequential machines in this paper. As a language for describing specification, we adopt infinitary regular temporal logic ($\infty$RTL)[1] which is an extension of $\epsilon$-free RTL proposed by Hiraishi et al. [2]. While traditional temporal logic or computation tree logic (CTL) cannot characterize finite state machines[3,4], $\infty$RTL is powerful enough to express regular sets and $\omega$ regular sets.

In hierarchical design, specifications and implementations are often given at different levels of abstractions. For example, a specification at register transfer level (a higher level) and an implementation at gate level (a lower level) can be given. In order to verify whether the lower-level implementation satisfies the higher-level specification, we must determine some formal relation and bridge the gap between the two levels.

In this paper, we propose a formal framework based on $\infty$RTL to explicitly describe relations between two different levels. We regard the
relation as a part of an implementation and show a verification method for a lower-level implementation (i.e., a lower-level sequential machine and a relation) and a higher-level specification described in $\infty$RTL.

This paper is organized as follows: Chapter 2 introduces $\infty$RTL. Chapter 3 discusses a formal framework for describing relations between different levels and shows a design verification method considering two different levels. Chapter 4 summarizes this paper.

2 Regular Temporal Logic

The empty word $\epsilon$, $\Sigma^*$ and $\Sigma^+$ are defined as in the usual way. An omega word over an alphabet $\Sigma$ is an infinite-length sequence of symbols from $\Sigma$. $\Sigma^\omega$ is the set of all omega words over $\Sigma$. $\Sigma^\infty \overset{\text{def}}{=} \Sigma^* \cup \Sigma^\omega$.

The class of infinitary regular sets is the union of regular sets[5] and $\omega$ regular sets[6].

For $\sigma \in \Sigma^\infty - \{\epsilon\}$, $|\sigma|$ denotes the length of $\sigma$, i.e., the number of symbols in $\sigma$ (If $\sigma$ is in $\Sigma^\omega$, then we denote $|\sigma| = \omega$). $\sigma(i)$ denotes the $i$th symbol of $\sigma$. In the case that $|\sigma| \geq i$, $\sigma^i$ denotes the suffix sub-sequence of $\sigma$ starting from $\sigma(i)$.

2.1 Definition of Regular Temporal Logic

Definition 1 Syntax

An $\infty$RTL formula is simply called an RTL formula. RTL formulas are defined inductively as follows. Let $AP$ be a set of atomic propositions. If $p \in AP$, and $\eta$ and $\xi$ are RTL formulas, then so are $(p)$, ($\neg\eta$), ($\eta \vee \xi$), ($\bigcirc \eta$), ($\eta : \xi$) and $[\exists \eta]$.

Definition 2 Model and semantics

$M = (\Sigma, I)$ is a linear model, where $\Sigma$ is a set of states and $I : \Sigma \rightarrow 2^{AP}$ is an interpretation function.
Let $\sigma \in \Sigma^\infty - \{\epsilon\}$. $M, \sigma \models \eta$ denotes that an RTL formula $\eta$ holds along the sequence $\sigma$ with respect to a linear model $M$. If there is no confusion, $M$ is omitted like $\sigma \models \eta$. Let $p$ be an atomic proposition, $\eta$ and $\xi$ be RTL formulas. The relation $\models$ is defined inductively as follows:

1. $\sigma \models p$ iff $p \in I(\sigma(1))$.
2. $\sigma \models (\neg \eta)$ iff $\sigma \not\models \eta$.
3. $\sigma \models (\eta \vee \xi)$ iff $\sigma \models \eta$ or $\sigma \models \xi$.
4. $\sigma \models (\O \eta)$ iff $|\sigma| \geq 2$ and $\sigma^2 \models \eta$.
5. $\sigma \models (\eta; \xi)$ iff there exist $\sigma_1 \in \Sigma^+$ and $\sigma_2 \in \Sigma^\infty - \{\epsilon\}$ such that $\sigma = \sigma_1 \sigma_2, \sigma_1 \models \eta$ and $\sigma_2 \models \xi$ or $|\sigma| = \omega$ and $\sigma \models \eta$.
6. $\sigma \models (\exists \eta)$ iff there exist $\sigma_i \in \Sigma^+(i = 1, \ldots, m - 1)$ and $\sigma_m \in \Sigma^\infty - \{\epsilon\}$ such that $\sigma = \sigma_1 \sigma_2 \ldots \sigma_m$ and $\sigma_i \models \eta$ for all $i$ or there exist an infinite number of finite sequences $\sigma_i \in \Sigma^+$ such that $\sigma = \sigma_1 \sigma_2 \ldots$ and $\sigma_i \models \eta(i = 1, 2, \ldots)$.

In the following, ‘$\wedge$’, $V_T$ and $V_F$ represent ‘conjunction’, ‘tautology’ and ‘invalid’ respectively. Unary operators have higher precedence than binary operators. If there is no ambiguity, ‘(’ and ‘)’ are omitted.

Finite RTL is defined as a subclass of $\infty$ RTL, whose semantics domain is restricted to $\Sigma^+$. Finite RTL is exactly the same as $\epsilon$-free RTL[2].

2.2 Regular Temporal Logic and Regular Sets

First, we introduce several notations. $\text{Len 1}$ holds along a set of sequences whose length is 1. ‘$\diamond$’(‘sometime’) and ‘$\square$’(‘always’) correspond to the temporal operators used traditionally in other temporal logic. $Inf$ and $Fin$ represent infinite sequences and finite sequences respectively.
\[ Len_1 \text{ def } \neg \Diamond V_T. \]

\[ \Diamond \eta \text{ def } \eta \lor (V_T : \eta). \quad \Box \eta \text{ def } \neg \Diamond \neg \eta = \eta \land \neg (V_T : \neg \eta). \]

\[ Inf \text{ def } (V_T : V_F). \quad Fin \text{ def } \neg Inf = \neg (V_T : V_F). \]

In order to discuss the relation between $\infty$RTL and regular sets, we define $L(\Sigma, I)(\eta) \text{ def } \{ \sigma | \sigma \in \Sigma^\infty - \{ \epsilon \}, \sigma \models \eta \}$, $L_f(\Sigma, I)(\eta) \text{ def } \{ \sigma | \sigma \in \Sigma^+, \sigma \models \eta \}$ and $L_\omega(\Sigma, I)(\eta) \text{ def } \{ \sigma | \sigma \in \Sigma^\omega, \sigma \models \eta \}$.

If there is no confusion, $L(\eta)$ etc. are used, omitting $\langle \Sigma, I \rangle$.

**Theorem 1** For an arbitrary RTL formula $\eta$ and an arbitrary model $(\Sigma, I)$, $L(\Sigma, I)(\eta)$ is an $\epsilon$-free infinitary regular set. Conversely, for an arbitrary $\epsilon$-free infinitary regular set $R$ over $\Sigma$, we can construct an RTL formula $\eta$ such that $L(\Sigma, I)(\eta) = R$, by introducing, for each state $s \in \Sigma$, an atomic proposition $p_s$ such that $I(s) = \{ p_s \}$.

This theorem is proved in [1].

**Corollary 1** $L_f(\eta)$ and $L_\omega(\eta)$ are an $\epsilon$-free regular set and an omega regular set respectively.

From the definition of $L(\eta)$, $L_f(\eta)$ and $L_\omega(\eta)$, we can see that an RTL formula $\eta$ can be used to specify some property of sequences, and $L(\eta)$ is a set of the sequences that have the property.

### 3 Formal Verification between Two Different Levels

#### 3.1 Formal Framework for Describing Relations between Two Different Levels

In this section, we provide a formal framework to explicitly describe relations between the two different levels. We assume two different levels, that is, a higher level for a specification and a lower level for an implementation.
As an implementation to be verified, we consider a Mealy type deterministic sequential machine $M$ with $n$ binary input signals $x_1, x_2, \ldots, x_n$ and $m$ binary output signals $z_1, z_2, \ldots, z_m$. Let $M = (X, Z, S, \delta, \lambda, s_0)$ be a Mealy type deterministic sequential machine with an initial state, where $X$, $Z$, and $S$ are finite, nonempty sets of binary input signals, binary output signals, and states, respectively. $s_0 \in S$ is the initial state. 

$\delta : 2^X \times S \rightarrow S$ is the state transition function (We assume that at least one next state is defined for each state in $S$). $\lambda : 2^X \times S \rightarrow 2^Z$ (We assume that the $\lambda$ is defined so long as $\delta$ is defined).

A possible input-output sequence of the sequential machine $M$ is an infinite or finite sequence $\rho$ over $2^{X \cup Z}$ such that $x_i \in \rho(k)$ iff $x_1 = 1$ at the $k$th input and $z_j \in \rho(k)$ iff $z_j = 1$ at the $k$th output, where $i = 1, 2, \ldots, n$, $j = 1, 2, \ldots, m$ and $k = 1, 2, \ldots, |\rho|$.

A possible input-output sequence can be regarded as a sequence of states of $\infty$RTL by introducing atomic propositions $p_{x_i}$ and $p_{z_j}$ associated with input signal $x_i$ and output signal $z_j$ respectively, such that $p_{x_i}$ is true iff $x_i = 1$ and $p_{z_j}$ is true iff $z_j = 1$. From Theorem 1 and Corollary 1, we can specify the behavior of the sequential machine in finite RTL or $\infty$RTL.

In [2], specifications are described for finite possible input-output sequences by using finite RTL. While finite RTL can express any behavior of sequential machines, fairness constraints [4], which are important in describing input constraints, cannot be described. In this paper, we

(1) adopt $\infty$RTL to describe specifications and

(2) focus our attention to only infinite possible input-output sequences.

When we describe a specification at the higher level, we assume that there are possible input-output sequences at the level, even if there does not exist a realized machine, and we specify the property of the sequences.
by an RTL formula. In describing relations between two different levels formally, we should pay attention to higher-level and lower-level sequences of states of ∞RTL. We formalize the relations as mappings from lower-level sequences to higher-level ones.

The framework for describing the relation of two state sequences of ∞RTL is formalized by the following the transformation rule and abstraction mapping. Here subscripts $H$ and $L$ are used to distinguish two objects which belong to the higher level and the lower level respectively.

**Definition 3 Transformation Rule**

For two given sets of atomic propositions $AP_H$ and $AP_L$, $\langle \eta_L, SI \rangle$ is called a transformation rule, where

- $\eta_L$ is a finite RTL formula,
- $SI = \bigcup_{p_H \in AP_H} \{p_H \leftarrow f_L | f_L \text{ is a lower-level (finite) RTL formula.}\}$

$\eta_L$ is called a time marker and $p_H \leftarrow f_L$ a state interpreter.

**Definition 4 Abstraction Mapping**

For a lower-level sequence $\langle I_L, \sigma_L \rangle$ and a transformation rule $A = \langle \eta_L, SI \rangle$, it is called transformation of $\sigma_L$ by $A$ to obtain a higher-level sequence $\langle I_H, \sigma_H \rangle$ such that, if $s_{L1} s_{L2} \cdots s_{Li} \models \eta_L$, then $\sigma_H(i)$ is a higher-level state such that $I_H(\sigma_H(i)) \ni p_H$ if $s_{L1} s_{L2} \cdots s_{Li} \models \xi_L$, for all $p_H \leftarrow \xi_L \in SI$, otherwise $\sigma_H(i) = \epsilon$.

Let us consider the example of Figure 1; a specification is assumed to be written at the higher level, and an implementation is given at the lower level. The higher-level adder calculates the addition (mod 16) of two integers $P, Q$ given as inputs and then, after a higher-level unit delay, it outputs the result. The lower-level adder serially adds two integers as 4-bit binary numbers. And then, after a lower-level unit delay, starts to output the result.
In Figure 1, a higher-level state corresponds to the lower-level sequences which end with four consecutive bits of inputs, and the output 0010 at the lower level corresponds to 4 at the higher level.

A transformation rule $A = (\eta, SI)$ of the example of Figure 1 is shown as follows, where $P, Q, R$ are represented in binary representation using atomic propositions, i.e., $(p_3, p_2, p_1, p_0), (q_3, q_2, q_1, q_0), (r_3, r_2, r_1, r_0)$ respectively. $p_3$, $q_3$ and $r_3$ are the most significant bits. Here the higher-level integers are regarded as binary numbers, for simplicity.

\[
\begin{align*}
\eta & \overset{\text{def}}{=} \Box \text{Len}4 \\
SI & \overset{\text{def}}{=} \{ p_0 \leftarrow \text{last}(4, a), p_1 \leftarrow \text{last}(4, \bigcirc a), \cdots \\
& \phantom{=} : \ \\
& \phantom{=} r_0 \leftarrow \text{last}(7, c), r_1 \leftarrow \text{last}(7, \bigcirc c), \\
& \phantom{=} r_2 \leftarrow \text{last}(7, \bigcirc \bigcirc c), r_3 \leftarrow \text{last}(7, \bigcirc \bigcirc \bigcirc c) \}
\end{align*}
\]

where $\text{last}(i, \eta) \overset{\text{def}}{=} (\eta \land \text{Len} i) \lor (V_T : (\eta : \text{Len} i))$. $\text{Len} i$ holds only along the sequences that consist of exactly $i$ states.

The example of the transformation from a lower-level sequence to a higher-level sequence of the adders of Figure 1 is shown in Figure 2.
Figure 2: Transformation from a Lower-level Sequence to a Higher-level Sequence

Although the detail is omitted in this paper, we can prove that the abstraction mapping can be simulated by a generalized sequential machine (gsm)[5]. Because regular sets and infinitary regular sets are closed under gsm mapping[5], any higher-level sequence obtained through the abstraction mapping can be characterized by $\infty$RTL.

3.2 A Formal Verification Method Considering Two Different Levels

In this section, we show the outline of a formal verification method for an implementation and a specification given at two different levels.

We regard that a transformation rule is a part of an implementation.

Here a structure model is introduced to handle possible input-output sequences easily.

**Definition 5** Structure model

$K = (\Sigma, I, R, \Sigma_0)$ is called a structure model, where $(\Sigma, I)$ is a linear model of $\infty$RTL. $R \subseteq \Sigma \times \Sigma$ is a total binary relation on $\Sigma$ and denotes the possible transitions between states. $\Sigma_0 \subseteq \Sigma$ is a set of initial states.

An RTL formula $\eta$ is said to be universally $K$-true, if $\eta$ holds along all finite and all infinite paths $\pi$ from $s_0$ for all $s_0 \in \Sigma_0$ in the structure model $K$. Otherwise universally $K$-false.
For a Mealy machine $M_l = (X, Z, S, \delta, \lambda, s_0)$, its corresponding structure $K_l = (\Sigma, I, R, \Sigma_0)$ is constructed as follows:

- $\Sigma = \{s_{i,j,k}'|s_i \in S, j \in 2^X, k \in 2^Z, \lambda(j, i) = k\}$
- $I(s_{i,j,k}') = \{p_x|x \in j\} \cup \{p_z|z \in k\}$
- $R = \{(s_{i,j,k}, s_{i',j',k'})|s_{i,j,k}, s_{i',j',k'} \in \Sigma, \delta(j, s_i) = s_{i'}\}$
- $\Sigma_0 = \{s_{0,j,k}' \in \Sigma\}$

Figure 3: Generation of a Structure Model from a Sequential Machine [2]

When we focus to only infinite paths on the structure model $K$, the term universally $K$-omega true (or false) is employed.

A structure model $K$ corresponding to a designed sequential machine $M$ is obtained so that the possible input-output sequences of $M$ have one-to-one correspondence with paths on $K$. The ways of generating a structure model from a given Mealy machine are shown in Figure 3.

Then formal verification is to make sure that a given specification formula holds along all the higher-level state sequences obtained by the transformation rule from all the lower-level state sequences.

To do this, firstly, we generate a higher-level structure model $K_H$ from the lower-level structure model $K_L$ corresponding to the machine. The transformation is performed by applying the abstraction mapping to all the paths of $K_L$. Its algorithm is omitted in this paper. Our remaining work is to check whether a specification formula is universally $K_H$-omega true. The outline of its algorithm is shown in [7].

4 Considerations

In this paper, we show a formal framework based on $\infty$RTL for describing relations between two different levels of abstraction and a verification method for them.

The size of the higher-level structure model obtained from a lower-
level one can be larger than that of the lower-level one. In order to avoid the increase of the size, some restriction will be necessary to the framework of abstraction mapping. However, describing the correspondence between a higher-level sequence and a lower-level one explicitly, seems a suitable approach for formal verification of hierarchical design.

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References


