P-Channel MOSFETs on 4H-SiC {0001} and Nonbasal Faces Fabricated by Oxide Deposition and N₂O Annealing

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Abstract—In this paper, we have investigated 4H-SiC p-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) with deposited SiO_2 followed by N_2O annealing. In addition to deposited oxides, dry-O_2-grown oxides and N_2O-grown oxides were also adopted as the gate oxides of SiC p-channel MOSFETs. The MOSFETs have been fabricated on the 4H-SiC (0001), $(000\bar{1})$, $(03\bar{3}8)$, and $(11\bar{2}0)$ faces. The (0001) MOSFETs with deposited oxides exhibited a relatively high channel mobility of $10 \mathrm{~cm^2/V \cdot s}$, although a mobility of $7 \mathrm{~cm^2/V \cdot s}$ was obtained in the (0001) MOSFETs with N_2O-grown oxides. The channel mobility was also increased by utilizing the deposited SiO_2 in the MOSFETs fabricated on nonbasal faces, although the MOSFETs on $(000\bar{1})$ were not operational. Compared with the thermally grown oxides, the deposited oxides annealed in N_2O are effective in improving the performance of 4H-SiC p-channel MOSFETs.

Index Terms—Channel mobility, deposited oxide, interface state density, metal–oxide–semiconductor field-effect transistor (MOSFET), p-channel, silicon carbide (SiC), $(000\bar{1})$, $(03\bar{3}8)$, $(11\bar{2}0)$.

I. INTRODUCTION

SILICON carbide (SiC) has superior properties such as high breakdown field, high thermal conductivity, and high saturation electron drift velocity [1], and hence, power electronics will benefit from the realization of SiC-based power devices. SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) have been regarded as a promising candidate for low-loss and fast power devices in advanced electronic systems [2], and high-voltage SiC n-channel MOSFETs that outperform Si power devices have been already reported [3]–[10].

SiC p-channel MOSFETs are the key components of p-channel insulated-gate bipolar transistors (p-IGBTs) [11]–[13] for ultrahigh-voltage (> 5-kV) devices. In addition, the development of SiC p-channel MOSFETs contributes to the realization of SiC-based complementary-MOS (CMOS) circuits [14], [15] for future power integrated circuits (ICs). Although

it is important to investigate SiC p-channel MOS devices, the fundamental study has been lacking. On the other hand, the understanding on SiC n-channel MOS devices has shown gradual progress, which leads to the improvement of MOS-FET performance mentioned earlier [3]–[10]. For example, the usage of 4H-SiC $(000\bar{1})$ [16], $(03\bar{3}8)$ [17], and $(11\bar{2}0)$ [18] and the nitridation process such as oxidation or reoxidation in NO or N_2O [19]–[21] are effective in increasing the channel mobility of SiC n-channel MOSFETs. In addition, utilization of deposited insulators [22]–[25] is an attractive method to improve the performance of n-channel SiC MOS and metal–insulator–semiconductor devices.

Although the influence of oxidation condition on the performance of 4H-SiC (0001) p-channel MOSFETs with thermal oxides has been investigated [26]–[28], the effectiveness of the deposited insulators has not been reported. The deposited oxides have several advantages over the thermal oxides, such as the following: 1) thin interfacial transition layer; 2) nearly isotropic formation of gate oxides on trenches; 3) reduction of process time; and 4) superior reliability (when adequately processed) [29], [30]. In this paper, the authors fabricated p-channel MOSFETs with deposited SiO_2 followed by N_2O annealing on the 4H-SiC (0001), $(000\bar{1})$, $(03\bar{3}8)$, and $(11\bar{2}0)$ faces. The mobility on $(11\bar{2}0)$ is particularly important for the development of SiC trench p-IGBTs. The MOS capacitors with deposited oxides were also fabricated on the 4H-SiC (0001) face. The performance of SiC p-channel MOSFETs is improved by utilizing the deposited oxides and/or nonbasal faces.

II. DEVICE FABRICATION

P-channel MOSFETs were fabricated on n-type 4H-SiC $8°$ off-axis (0001), $8°$ off-axis $(000\bar{1})$, on-axis $(03\bar{3}8)$, and on-axis $(11\bar{2}0)$ epilayers. The donor concentrations of n-epilayers were $1 \times 10^{16} \mathrm{~cm^{-3}}$ for (0001), $1–3 \times 10^{15} \mathrm{~cm^{-3}}$ for $(000\bar{1})$, $2–5 \times 10^{16} \mathrm{~cm^{-3}}$ for $(03\bar{3}8)$, and $5–8 \times 10^{14} \mathrm{~cm^{-3}}$ for $(11\bar{2}0)$. The source/drain regions were formed by high-dose (5×10^{15}-$\mathrm{cm^{-2}}$) Al^+ implantation at $300 °C$. High-temperature annealing was performed at $1700 °C$ for 20 min in Ar with a carbon cap to suppress surface roughening [31]. After RCA cleaning with a final HF dip, a SiO_2 layer was deposited by plasma-enhanced CVD (PECVD) at $400 °C$, with TEOS and O_2 as source gases. The thickness of the deposited SiO_2 was about 45 nm. After the PECVD process, thermal annealing was performed in dry-N_2O (10% diluted in N_2) ambient at $1300 °C$ for 30 min. The oxide thicknesses (d_{OX}'s) were increased to

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47 nm for the (0001) face, 51 nm for the $(000\bar{1})$ face, 50 nm for the $(03\bar{3}8)$ face, and 48 nm for the $(11\bar{2}0)$ face after the N_2O annealing. Ti/Al/Ni and Ni, annealed at 950 °C for 5 min, were used as the source/drain and substrate contacts, respectively. The gate metal was Al. The typical channel length (L_{Ch}) and width (W) were 100 and 200 μm, respectively. To accurately estimate channel mobility and suppress short-channel effects [32], the authors adopted the design of long-channel lateral MOSFETs.

For fabrication of MOS capacitors, p-type 4H-SiC (0001) epilayers with an acceptor concentration of 8×10^{15} cm^{-3} were prepared. The formation process of gate oxides was similar to that mentioned previously. The thickness of the deposited SiO_2 was 76 nm, and the N_2O-annealing time was 1 h. The N_2O-annealing time was extended because the initial thickness of the deposited oxides for MOS capacitors (76 nm) was thicker than that for MOSFETs (about 45 nm). The oxide thickness after the N_2O annealing was 80 nm. Ti/Al/Ni was evaporated on the backside and annealed at 950 °C for 5 min. The circular gate metal was Al with a diameter of 520 μm.

For comparison, the p-type MOS capacitors and p-channel MOSFETs with thermal oxides grown in pure O_2 at 1150 °C and N_2O (10% diluted in N_2) at 1300 °C were fabricated. The 4H-SiC (0001) MOSFETs with dry-O_2-grown oxides have a gate oxide thickness of 72 nm. The thicknesses of the gate oxides for MOSFETs with N_2O-grown oxides were 49 nm for (0001), 63 nm for $(000\bar{1})$, 44 nm for $(03\bar{3}8)$, and 52 nm for $(11\bar{2}0)$, and that for the (0001) MOS capacitors with N_2O-grown oxides was 55 nm. The interface properties of SiC p-channel MOSFETs with N_2O-grown oxides have already been reported [33].

III. EXPERIMENTAL RESULTS AND DISCUSSION

The typical drain characteristics of the MOSFETs with dry O_2-grown oxides are shown in Fig. 1. The 4H-SiC (0001) MOSFETs with dry-O_2-grown oxides show poor ON-state characteristics. As shown in Fig. 1, the drain current (I_D) is extremely low (−0.2 nA), even at a gate voltage (V_G) of −40 V (a corresponding gate oxide field (V_G/d_{OX}) of 5.5 MV/cm). The (0001) MOSFETs with dry-O_2-grown oxides show a threshold voltage below −30 V and a channel mobility below 1 cm^2/V · s. The large negative shift of the threshold voltage is caused by high density of positive charges at the dry-O_2-grown-oxide/SiC interface [34]. The dry-O_2 oxidation is not a suitable process for p-channel SiC MOSFETs.

Fig. 2 shows the drain characteristics of the fabricated MOSFETs with N_2O-grown oxides and deposited oxides on (a) (0001), (b) $(03\bar{3}8)$, and (c) $(11\bar{2}0)$. The dashed lines mean the characteristics of the MOSFETs with N_2O-grown oxides, and the solid lines denote those of the MOSFETs with deposited SiO_2 annealed in N_2O for 30 min. In contrast to the MOSFETs with dry-O_2-grown oxides, the MOSFETs with N_2O-grown oxides and the deposited oxides exhibit good linear and saturation characteristics, regardless of the crystal face orientation, except for the $(000\bar{1})$ face. The $(000\bar{1})$ MOSFETs showed oxide breakdown before turn-on, when the gate voltage was increased (not shown). The MOSFETs on the $(03\bar{3}8)$ and
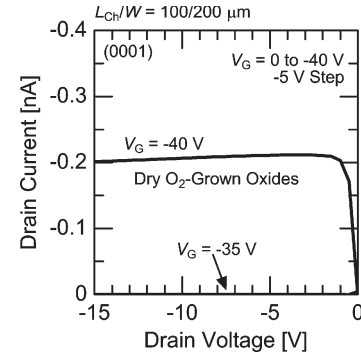

Fig. 1. Drain characteristics for the 4H-SiC (0001) MOSFET with a dry-O_2-grown oxide. The gate voltage is varied from 0 V to −40 V with −5 V step.

$(11\bar{2}0)$ faces exhibit higher drain current than that on the (0001) face. The enhanced drain current is observed in the (0001) and $(03\bar{3}8)$ MOSFETs with deposited SiO_2, which indicates that the MOSFETs with deposited SiO_2 possess higher channel mobility than those with N_2O-grown oxides.

Fig. 3 shows the gate (I_D–V_G) characteristics of the p-channel MOSFETs with N_2O-grown oxides fabricated on the various 4H-SiC faces in the linear region (at a drain voltage (V_D) of −0.1 V). To compare the p-channel MOSFETs with various structures, the drain current (I_D) in the gate characteristics was normalized by the channel length (L_{Ch}), the channel width (W), and the oxide capacitance per unit area (C_{OX}). Although the MOSFETs on the $(000\bar{1})$ face are not operational, the MOSFETs on the $(03\bar{3}8)$ and $(11\bar{2}0)$ faces exhibit higher drain current than that on the (0001) face. The theoretical/measured threshold voltages are −4.0 V/ −10.8 V for the (0001) MOSFETs, −5.3 V/−9.2 V for the $(03\bar{3}8)$ MOSFETs, and −2.8 V/−10.8 V for the $(11\bar{2}0)$ MOSFETs. The measured threshold voltage was shifted toward the negative direction, compared to the theoretical value for each face, which means that positive charges, the density of which is over 1×10^{12} cm^{-2}, exist at the SiO_2/SiC interface. From the subthreshold characteristics, the subthreshold swings of the p-channel MOSFETs with N_2O-grown oxides on the 4H-SiC (0001), $(03\bar{3}8)$, and $(11\bar{2}0)$ faces are estimated to be 301, 280, and 265 mV/decade, respectively. The $(03\bar{3}8)$ and $(11\bar{2}0)$ MOSFETs exhibit steeper slopes in the subthreshold region. From these results, the nonbasal faces, such as the 4H-SiC $(03\bar{3}8)$ and $(11\bar{2}0)$ faces, are attractive for improving the performance of p- and n-channel SiC MOSFETs [17], [18].

Fig. 4 shows the gate characteristics of the fabricated p-channel MOSFETs with deposited SiO_2 annealed in N_2O on the various faces in the linear region. The drain current in the gate characteristics was normalized by the channel length, the channel width, and the oxide capacitance per unit area. The threshold voltages are −9.8 V for the (0001) MOSFETs, −9.3 V for the $(03\bar{3}8)$ MOSFETs, and −12.7 V for the $(11\bar{2}0)$ MOSFETs. As is the case for the N_2O-grown oxides, the MOSFETs with deposited oxides could not turn on. From the subthreshold characteristics, the subthreshold swing was calculated to be 278 mV/decade for the (0001) face. By utilizing the deposited SiO_2, the subthreshold characteristics are slightly improved in the (0001) MOSFETs.
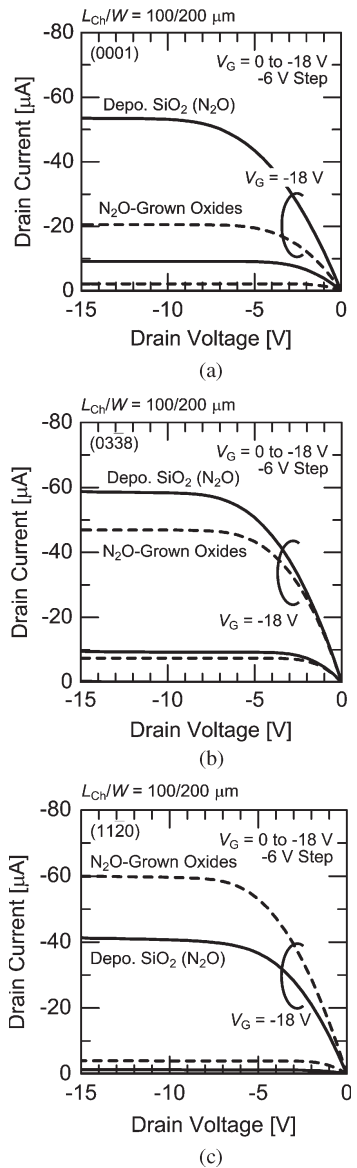
Fig. 2. Drain characteristics for 4H-SiC MOSFETs fabricated on (a) the (0001) face, (b) the (03$\bar{3}$8) face, and (c) the (11$\bar{2}$0) face. The dashed lines mean the characteristics of the MOSFETs with N_2O-grown oxides, and the solid lines denote those of the MOSFETs with deposited SiO_2 annealed in N_2O for 30 min.
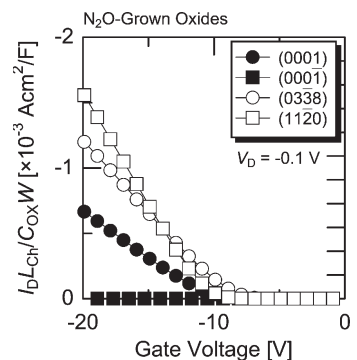

Fig. 3. Gate characteristics of the 4H-SiC p-channel MOSFETs with N_2O-grown oxides on various faces. The closed circles denote the MOSFETs on the 4H-SiC (0001) face, the closed boxes mean the MOSFETs on the 4H-SiC (000$\bar{1}$) face, the open circles represent the MOSFETs on the 4H-SiC (03$\bar{3}$8) face, and the open boxes depict the MOSFETs on the 4H-SiC (11$\bar{2}$0) face.
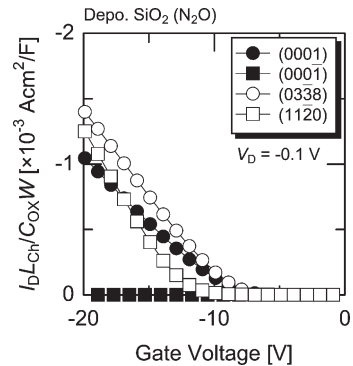

Fig. 4. Gate characteristics of the 4H-SiC p-channel MOSFETs with deposited oxides annealed in N_2O for 30 min on various faces. The closed circles denote the MOSFETs on the 4H-SiC (0001) face, the closed boxes mean the MOSFETs on the 4H-SiC (000$\bar{1}$) face, the open circles represent the MOSFETs on the 4H-SiC (03$\bar{3}$8) face, and the open boxes depict the MOSFETs on the 4H-SiC (11$\bar{2}$0) face.

Fig. 5 shows the effective mobility versus the gate oxide field of the fabricated p-channel MOSFETs on the 4H-SiC (0001), (03$\bar{3}$8), and (11$\bar{2}$0) faces. The effective mobility of the MOSFETs on 4H-SiC (000$\bar{1}$) could not be calculated due to the low drain current. Fig. 5(a) shows the mobility of the MOSFETs with N_2O-grown oxides, and Fig. 5(b) shows that of the MOSFETs with deposited SiO_2 annealed in N_2O. The horizontal axes in Fig. 5(a) and (b) denote the gate oxide field that is defines as V_G/d_{OX}. From Fig. 5(a) and (b), the effective mobility is as high as 17 cm^2/V · s in the (11$\bar{2}$0) MOSFETs, regardless of the gate oxides. The (0001) and (03$\bar{3}$8) MOSFETs with N_2O-grown oxides show effective mobility values of 7 and 11 cm^2/V · s, respectively. By utilizing the deposited SiO_2, the channel mobility values are increased to 10 and 13 cm^2/V · s in the (0001) and (03$\bar{3}$8) MOSFETs, respectively. The deposited SiO_2 can enhance the effective mobility of not only the n-channel MOSFETs [23] but also the p-channel MOSFETs. A channel mobility over 10 cm^2/V · s is a relatively high value, taking account of the low bulk mobility of holes (about 100–120 cm^2/V · s). Although p-channel 4H-SiC (0001) MOSFETs with wet-O_2-grown oxide exhibit a channel mobility of 15 cm^2/V · s [27], the N_2O-grown oxides and the deposited SiO_2 followed by N_2O annealing are also suited to improve the channel mobility of p-channel 4H-SiC MOSFETs.

To estimate the interface state density near the valence-band edge (E_V), capacitance–voltage (C–V) measurements were performed by using MOS capacitors on the (0001) face at room temperature under the dark condition. The interface state density was evaluated by using the high–low method.

The measured and theoretical C–V characteristics of the fabricated 4H-SiC (0001) MOS capacitors with N_2O-grown oxides and deposited oxides are shown in Fig. 6(a) and (b), respectively. The voltage sweep was started from the deep-depletion bias condition. The closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. From the flatband shift in C–V characteristics, the effective fixed charge density was calculated to be 2.4 × 10^{12} cm^{-2} for the MOS capacitors with N_2O-grown oxides and 1.5 × 10^{12} cm^{-2} for those with deposited SiO_2 annealed in N_2O. Fig. 7 shows the distribution of interface state density near
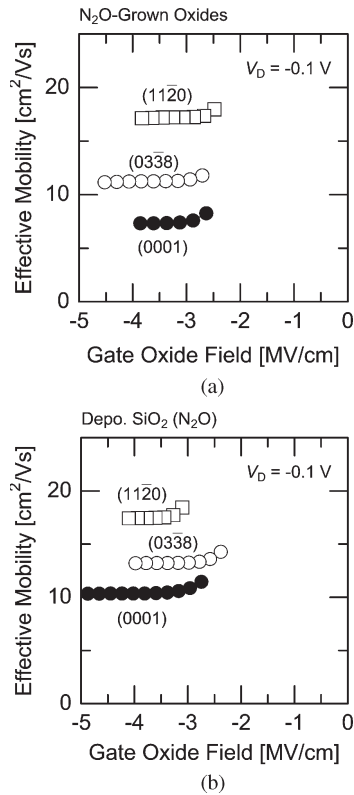
Fig. 5. Effective mobility of the fabricated 4H-SiC p-channel MOSFETs with (a) N$_2$O-grown oxides and (b) deposited SiO$_2$ annealed in N$_2$O for 30 min. The closed circles mean the MOSFETs on the 4H-SiC (0001) face, the open circles represent the MOSFETs on the 4H-SiC (03$\bar{3}$8) face, and the open boxes denote the MOSFETs on the 4H-SiC (11$\bar{2}$0) face.

Fig. 6. C–V characteristics for the fabricated p-type 4H-SiC (0001) MOS capacitors with (a) N$_2$O-grown oxides and (b) deposited oxides. The closed and open circles denote the quasi-static and high-frequency C–V characteristics, respectively. The dashed line represents the theoretical C–V characteristics. The horizontal dotted line means the flatband capacitance.

the valence-band edge for the p-type MOS structures with N$_2$O-grown oxides and deposited oxides on (0001). The interface states for the MOS structures with N$_2$O-grown oxides are uniformly distributed with a density of 9×10^{11} cm$^{-2} \cdot$ eV^{-1} in the energy range from $E_V + 0.1$ eV to $E_V + 0.5$ eV. The interface state density is reduced to 5×10^{11} cm$^{-2} \cdot$ eV^{-1} at $E_V + 0.2$ eV in the p-MOS structures with deposited SiO$_2$ annealed in N$_2$O. The deposited SiO$_2$ followed by N$_2$O annealing is effective to decrease the interface state density not only near the conduction-band edge [23] but also near the valence-band edge, as shown in Fig. 7. The low density of interface states in the deposited SiO$_2$/SiC structure may lead to a higher channel mobility.

As mentioned previously, the performance of p-channel SiC MOSFETs is improved by utilizing the deposited oxides and/or nonbasal faces, such as (03$\bar{3}$8) and (11$\bar{2}$0). On the other hand, the p-channel MOSFETs on the (000$\bar{1}$) face were not operational. Fig. 8 shows the quasi-static C–V curve of the p-channel MOSFETs with N$_2$O-grown oxides fabricated on (a) (0001) and (b) (000$\bar{1}$) measured by using a gate-controlled diode structure [35]. In gate-controlled diodes, the source/drain regions act as an external source of inversion carriers. Thus, the C–V curves measured by using the gate-controlled diode structure will demonstrate "accumulation–deep depletion" characteristics, although the MOS capacitors fabricated on wide-bandgap semiconductors generally show "accumulation–depletion–deep-depletion" characteristics. As shown in Fig. 8(a), the C–V curve
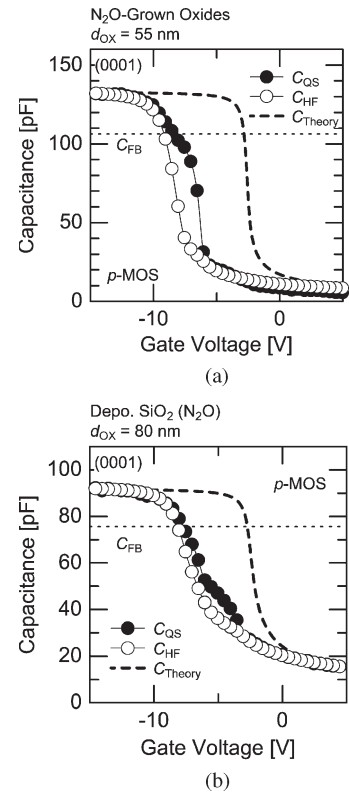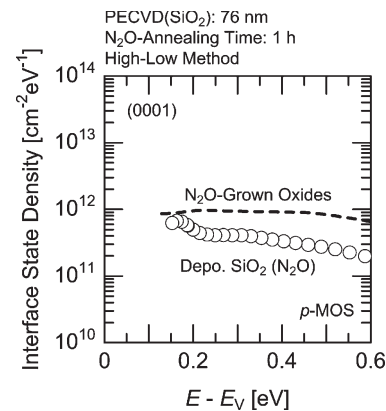

Fig. 7. Interface state density near the valence-band edge for (open circles) the 4H-SiC (0001) MOS structures with deposited SiO$_2$ annealed in N$_2$O for 1 h. The result for N$_2$O-grown oxides is also shown as the dashed line.

shows accumulation–depletion–inversion characteristics in the (0001) MOSFET. The p-channel MOSFETs with N$_2$O-grown oxides on the 4H-SiC (03$\bar{3}$8) and (11$\bar{2}$0) faces also exhibited accumulation–depletion–inversion characteristics in the C–V curves [33]. In contrast, MOSFETs fabricated on (000$\bar{1}$) exhibit "accumulation–depletion–deep depletion" characteristics [Fig. 8(b)]. Similar characteristics were also observed in the (000$\bar{1}$) MOSFETs with deposited SiO$_2$ annealed in N$_2$O. The source–substrate and drain–substrate junctions in the (000$\bar{1}$) MOSFETs act as a good p-n junction. Therefore, the SiO$_2$/n-type 4H-SiC (000$\bar{1}$) interfaces cannot be

N₂O-Grown Oxides

Gate-Controlled Diode
(0001)

C_{QS}

C_{Theory}

N₂O-Grown Oxides

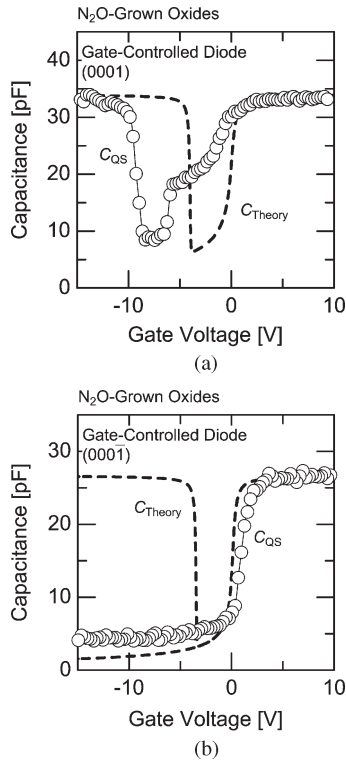Gate-Controlled Diode
(000$\bar{1}$)

C_{Theory}

C_{QS}

Fig. 8. Quasi-static C–V curve obtained in the p-channel MOSFET with an N₂O-grown oxide fabricated on the 4H-SiC (a) (0001) and (b) (000$\bar{1}$) faces by using a gate-controlled diode structure. A theoretical C–V curve is also shown by a dashed line.

inverted, or more negative gate voltage is needed to invert the interfaces, probably due to very high interface states.

IV. CONCLUSION

P-channel MOSFETs with N₂O-grown oxides and deposited SiO₂ followed by N₂O annealing were fabricated on the 4H-SiC (0001), (000$\bar{1}$), (03$\bar{3}$8), and (11$\bar{2}$0) faces. The MOSFETs on the 4H-SiC (000$\bar{1}$) face were not operational. The (0001) MOSFETs with N₂O-grown oxides showed a channel mobility of $7 \text{ cm}^2/\text{V} \cdot \text{s}$, and the mobility was increased to $10 \text{ cm}^2/\text{V} \cdot \text{s}$ by utilizing the deposited oxides. The channel mobility of the (03$\bar{3}$8) MOSFETs with deposited oxides was also improved to $13 \text{ cm}^2/\text{V} \cdot \text{s}$ from $11 \text{ cm}^2/\text{V} \cdot \text{s}$ in the (03$\bar{3}$8) MOSFETs with N₂O-grown oxides. The MOSFETs on the (11$\bar{2}$0) face exhibited a high channel mobility of $17 \text{ cm}^2/\text{V} \cdot \text{s}$, regardless of the gate oxides. From the C–V characteristics, the lower interface state density $(5 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1})$ was obtained at the deposited-oxide/4H-SiC (0001) interface, compared with the N₂O-grown-oxide/4H-SiC (0001) interface $(9 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1})$. The deposited SiO₂ followed by N₂O annealing is one of the attractive processes to enhance both the n- and p-channel 4H-SiC MOSFET performances.

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