# Thermal stability of deep levels between room temperature and 1500 °C in as-grown 3*C*-SiC

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We report on the thermal stability of deep levels detected in as-grown bulk 3*C*-SiC. The investigation was performed by Fourier-transform deep level transient spectroscopy and an isochronal annealing series was carried out in the 100–1500 °C temperature range. We found three traps located between 0.14–0.50 eV below the conduction band edge minimum ($E_C$). The shallower trap anneals out at temperatures below 1200 °C while the others display a high thermal stability up to at least 1500 °C. The nature of the former trap is discussed in detail on the basis of its annealing behavior and previous theoretical data found in the literature. © *2009 American Institute of Physics*. [doi:10.1063/1.3243086]

## I. INTRODUCTION

It is now well established that SiC is the candidate as a replacement of Si for future electronic applications. In fact, SiC has both physical and chemical properties that make it more suitable than Si for the manufacture of high power, high frequency, and high-temperature operating devices.[1] One of the most interesting features of SiC is polytypism. Over 200 different SiC polytypes are known, the most important of which, from a technological point of view, are the 3*C*-SiC, 4*H*-SiC, and 6*H*-SiC. Of these, despite the lack of adequate substrates that make the growth feasible only by using Si substrates, 3*C*-SiC has attracted the attention of the industry due also to the recent progress of epitaxial growth techniques that has made the reduction of stacking faults possible.[2]

3*C*-SiC presents several advantages compared to 4*H*-SiC and 6*H*-SiC. For instance, its junction breakdown electric field is $2\times10^6$ V/cm and because of the higher channel mobility in the inversion layer than that of 4*H*-SiC devices, 3*C*-SiC is very promising for the fabrication of high power electronics, high current, and high voltage switching applications. In fact, due to the smaller band gap (2.36 eV compared to 3.26 eV of 4*H*), the near-interface traps that are known to limit the mobility of carriers in 4*H*-SiC based metal oxide semiconductor field effect transistors (MOSFET) do not affect the mobility of carriers in 3*C*-SiC based MOSFETs because in 3*C*-SiC these states lie in the conduction band.[3]

However, as many scientists devote their efforts to the improvement of the quality of 3*C*-SiC epitaxial layers, not much is known on the presence of deep levels in this polytype. Electrically active levels are known to behave as traps or recombination/generation centers affecting the mobility of carriers thus preventing the correct functionality of electronic devices and for this reason the knowledge of the thermal behavior and microscopic nature of such levels is also of primary importance.

Throughout the years, few investigations by capacitance transient methods on deep levels of as-grown 3*C*-SiC have been performed,[4–9] the most recent of which dates back to 2003 and since the 3*C*-SiC epitaxial growth is a continuously evolving field of study, new reports on the characterization of electrically active levels are strongly needed. Furthermore, the analysis of the thermal behavior and nature of deep levels can provide additional ground for epitaxial growth scientists so to better understand growth mechanisms and tune the parameters involved in the 3*C*-SiC growth process.

For this reason, we report on the isochronal annealing behavior, between room temperature and 1500 °C, of electrically active levels in as-grown 3*C*-SiC.

## II. EXPERIMENTAL DETAILS

Bulk N-doped ($N_D\sim1\times10^{16}$ cm$^{-3}$) 3*C*-SiC samples, provided by HOYA, were electrically characterized by means of Fourier-transform deep level transient spectroscopy (FT-DLTS),[10] in the 130–500 K temperature range, by using a reverse bias of −1 V, a period width of 0.2 s and a filling pulse of 1 ms. The samples were annealed for 15 min from 100 to 1500 °C. From 100 to 400 °C thermal annealings were performed under vacuum using the DLTS cryostat, from 500 to 1000 °C using a rapid thermal annealing furnace in Ar flow. For heat treatments above 1000 °C a *C*-cap[11] was first deposited on the sample surface and a hot-wall chemical vapor deposition chamber (in Ar-ambient) was employed. After annealing treatments above 1100 °C, the samples underwent a dry oxidation process at 1100 °C for 15 min in order to minimize the effects of surface decomposition that can occur when performing annealing at such high

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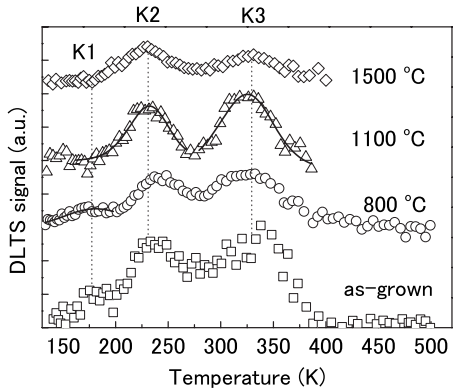


FIG. 1. DLTS spectra of 3*C*-SiC for as-grown, 800, 1100, and 1500 °C annealed samples.

temperatures[12] and to ensure a high quality surface for subsequent Schottky diode formation.[13] No effects of such process on the defects evolution could be revealed, as it can later be seen by the similar concentrations of the detected levels. After every heat treatment, samples were dipped into HF for 15 min and 1 mm in diameter Schottky diodes were formed by depositing Au on the surface. Before every heat treatment, the Au contacts were removed by using aqua regia. Although the authors tried higher temperature annealing (1600–1700 °C), a high density of stripe grooves, most likely slip lines, were generated on the surface, making the DLTS measurements difficult due to the increased leakage current.

## III. RESULTS AND DISCUSSION

In Fig. 1 the DLTS spectra of the measurements performed on the as-grown and samples annealed at 800, 1100, and 1500 °C are shown. It can be seen that three levels are found in the 175–350 K temperature range. The three levels are located at ~175, ~230, and ~350 K and were labeled K1, K2, and K3, respectively. No DLTS signal could be detected at temperatures higher than 500 K. This is in accordance with the study of Yamada *et al.*,[7] which has been one of the few reporting on DLTS measurements on 3*C*-SiC for temperatures higher than 400 K. Also Saddow *et al.*[6] investigated deep levels on a wide range of temperatures but, unlike other works present in the literature, they have reported no electron traps in 3*C*-SiC.

A subsequent heat treatment at higher temperatures (800 °C) did not yield any meaningful change of the K1, K2, and K3 levels but annealing at 1100 °C resulted in the annihilation of the K1 level. The final thermal annealing at 1500 °C did not produce any alteration in the DLTS spectrum as the K2 and K3 are still persistent.

Because of the relatively low trap concentrations in the material, the signal-to-noise ratio was rather poor in the DLTS spectrum and the energy position and capture cross section were affected by high errors. For this reason we decided to employ a fitting procedure of the F-DLTS in order to obtain more reliable values of the energy position in the bandgap and capture cross section. We used the following equation for a single FT-DLTS peak:

TABLE I. Labeling, energy position below $E_C$ and capture cross section ($\sigma$) for the three detected levels.

| Label | Energy (eV)[a] | $\sigma$(cm$^2$) | Comments |
|---|---|---|---|
| K1 | $0.14 \pm 0.03$ | $\sim 2 \times 10^{-17}$ | Anneals out below 1200 °C |
| K2 | $0.29 \pm 0.08$ | $\sim 2 \times 10^{-16}$ | Stable up to 1500 °C |
| K3 | $0.50 \pm 0.09$ | $\sim 3 \times 10^{-16}$ | Stable up to 1500 °C |

[a]below $E_C$.

$$S = \frac{N_T C_{st}}{T_W N_D}(e^{-T_W/\tau} - 1)\frac{2\pi/T_W}{1/\tau^2 + (2\pi/T_W)^2}, \quad (1)$$

where $N_T$, $C_{ST}$, and $T_W$ are the trap concentration, the steady capacitance under reverse bias condition and the period width, respectively, while $\tau$ is defined as

$$\tau = \frac{1}{\sigma v_{th} N_C} e^{E_C - E_T/kT} \quad (2)$$

with $\sigma$, $v_{th}$, $N_C$, $E_T$, $k$ are the capture cross section, thermal velocity, effective density of states, activation energy and Boltzmann constant, respectively. Except for $v_{th}$, $N_C$, $T_W$, $N_D$, the parameters were considered as free parameters and the fitted K1, K2, and K3 F-DLTS peaks are shown in Fig. 1 by solid line while the resulting values of $E_T$ and $\sigma$ are reported in Table I. The activation energy was determined to be 0.14, 0.29, and 0.50 eV for the K1, K2, and K3 trap, respectively.

It is not an easy task to trace the presence of the K1, K2, and K3 centers in the literature, as 3*C*-SiC growth techniques employed in the previous studies were either different or improved through the years. The K1 has not been reported by any previous author. Despite the fact that Zekentes *et al.*[5] and Yamada *et al.*[7] indeed noted the presence of a DLTS peak in roughly the same temperature position as that of the K1 level, the defect energy positions reported by these two authors are 0.1–0.15 eV deeper than that of the K1. Moreover, Yamada *et al.*[7] showed that the detected defect displays Poole–Frenkel effect implying that it should be a donor while, in the present case, the emission rates of all the detected levels do not show any electric field dependence.

Both Zhou *et al.*[4] and Zekentes *et al.*[5] reported levels close to the K2 center, the SCE1 and the $T_1$ centers, respectively. However, the SCE1 was detected in polished and subsequently oxidized samples, which is not the case of the K2 center since no oxidation was performed at least for the as-grown material. On the contrary, the identification of the K2 center with the $T_1$ may be more plausible because Zekentes *et al.*[5] found this level in nonoxidized samples but did not put forward any hypothesis on the possible microscopic structure of this level. Indeed, the capture cross section value of the $T_1$ level was of the order of $10^{-20}$ cm$^2$ while that of the K2 center is $10^{-16}$ cm$^2$, but this difference can be ascribed to the estimation method used by the authors who neglected the nonexponential capture kinetics in the Debye tail.[14]

Regarding the K3 level, located at 0.50 below $E_C$, two levels have been reported with a similar energy position in the band gap as that of the K3 level, an unlabeled defect found by Nagesh *et al.*[15] and the $T_2$.[5] The former cannot be

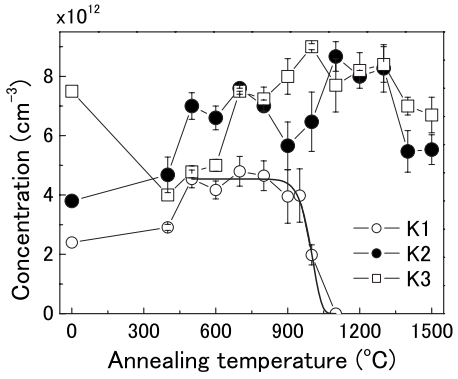


FIG. 2. Isochronal annealing behavior of the K1, K2, and K3 traps. The time step was of 15 min. For the K1 level an extra measurement was performed after annealing at 950 °C to increase the accuracy. The solid line represents a first order annealing process with an activation energy of 4.05 eV and a pre-exponential factor of $10^{13}$ $s^{-1}$.

identified with the K3 level because it was detected after neutron irradiation while the latter seems a more reasonable choice. As for the case of the $T_1$ level, Zekentes *et al.*[5] gave no indications on the possible microscopic structure of this level but excluded the possible involvement of silicon antisites ($Si_C$).

In order to give a more clear indication on the nature of the detected levels, the isochronal annealing behavior of the three detected levels is reported in Fig. 2. The concentrations of the K1, K2, and K3 levels are below $10^{13}$ $cm^{-3}$, indicating the high quality of the material. It can be seen that the concentrations of the K2 and K3 levels are almost constant throughout the isochronal annealing series and they both reveal a high thermal stability up to 1500 °C. On the contrary the K1 level anneals out at 1100 °C and this allows us to model this annealing behavior with a first order annealing kinetic curve described by

$$[N] = [N_0] \times e^{-ct}, \tag{3}$$

where $[N]$, $[N_0]$, $c$, and $t$ are the concentration of the defect, the concentration of the defect at $t=0$, the rate constant, and the annealing time, respectively. The rate constant is defined as $c=c_0 e^{-E_a/kT}$, with $c_0$, $k$, $E_a$, and $T$, the frequency factor, the Boltzmann constant, the activation energy, and the absolute temperature. By setting $c_0$ to $10^{13}$ $s^{-1}$,[17] it is possible to extract an $E_a$ for the process to occur of $4.05 \pm 0.01$ eV (solid line in Fig. 2). This value, in addition to the wealth of theoretical studies on point defects in SiC, which can be found in the literature,[16–18] can give useful indications on the nature of the K1 center. However, the severe lack of experimental studies on 3*C*-SiC leaves plenty of room for different interpretations.

We exclude the possible involvement of both Si and C interstitials due to their low migration barrier (1.4 and 0.9 eV, respectively), which makes them more mobile than vacancies, thus lowering the annealing temperature.[16,17] Also antisites, both $C_{Si}$ and $Si_C$ can be excluded from the picture since antisites are produced by neutron irradiation in 3*C*-SiC.[15,19] These considerations, together with the fact that they both can be found at cubic sites,[18] leave vacancies as possible candidates for the involvement in the microscopic structure of the K1 center. However, the $V_C$ has a higher thermal stability than $V_{Si}$ (Ref. 17) and it is known to persist annealing up to 1600 °C.[20] Moreover, the involvement of the $V_C - C_{Si}$ complex, which is known to be electrically active, can also be ruled out since it is known to arise after annealing at 700–750 °C.[16] Therefore, the possibility that a $V_{Si}$ may explain the nature of the K1 center can be put forward.

It can be argued that density functional calculations, in the local density approximation, performed by Zywietz *et al.*[21] have shown that $V_{Si}$ ionization levels in 3*C*-SiC are located in the lower half of the band gap. However, the authors did not exclude the existence of a $V_{Si}$ in the upper part of the bandgap of 3*C*-SiC, closer to $E_C$, and also Bockstedte *et al.*,[16] by using the same methodology but a denser Brillouin zone sampling, reached the same conclusion adding that $V_{Si}$ related complexes may also be found in the 0.1–0.6 eV range, below $E_C$.

Another argument against the possibility of the involvement of $V_{Si}$ is that $V_{Si}$ and related complexes anneal out at temperatures higher than that of the K1 but, as it was later found out in electron irradiated *n*-type 6*H*-SiC epilayers, the annealing temperature of $V_{Si}$ can be affected by the nitrogen content which, in the case of a concentration of $5 \times 10^{15}$ $cm^{-3}$ (in our case is $\sim 10^{16}$ $cm^{-3}$), occurs between 1000 and 1200 °C.[16] In addition, three acceptor levels found in *n*-type 6*H*-SiC, which annealed at 1050 °C, were also associated to $V_{Si} - N$ complexes.[22] Furthermore, density functional theory calculations performed by Rauls *et al.*[17] have predicted a sublattice migration for the $V_{Si}$ of 3.9 and 4.1 eV for 3*C*-SiC and 4*H*-SiC, respectively, which is quite similar to our value of the $E_a$.

## IV. CONCLUSIONS

In conclusion, we reported on the thermal behavior of three deep levels in as-grown 3*C*-SiC, located at 0.14, 0.29, and 0.50 eV below $E_C$. Our investigation revealed that while the two deeper levels are thermally stable up to at least 1500 °C, the shallower level anneals out after 15 min at 1100 °C. For this level, by assuming a first order annealing process, we extracted an activation energy of 4.05 eV and the possible participation of a $V_{Si}$ in its microscopic structure is put forward, on the basis of previous theoretical investigations found in the literature.

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