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The influence of parasitic components on power MOSFET switching operation in power conversion circuits

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Abstract: This paper discusses the quantification of parasitic components inherent in printed circuit board (PCB) wiring, which can be of considerable value in power conversion circuits. The influence of parasitic inductance and mutual coupling are evaluated in terms of electromagnetic compatibility (EMC) for the switching operation of power MOSFETs in a dc-dc buck converter. The parasitic components are identified based on the partial element equivalent circuit (PEEC) method and modeled with circuit simulation. The estimated effect of the parasitic component on the switching operation of a power MOSFET is validated by comparing it with experimental results.

Keywords: switching, parasitic inductance, mutual coupling, EMC

Classification: Electron devices, circuits, and systems

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1 Introduction

A power conversion circuit with high frequency switching, like a PWM inverter or a dc-dc switching converter, suffers from electromagnetic compatibility (EMC) problems. There are large di/dt and dv/dt in a power conversion circuit, resulting from fast switching of power devices with high voltage and large current. The occurrence of EMI noise and its generating mechanism has been studied and clarified especially for small signal systems, such as LSI and digital circuits, and a macro model of numerical simulation to perform EMC design has been proposed [1]. However, few studies have focused on EMC designs for large signals with high frequency power conversion circuits [2], because conventional high power conversion circuits have operated at low switching frequencies. Thus di/dt and dv/dt have been low. However, state of the art power switching devices enable high frequency switching. In particular, SiC power devices promise fast switching of high voltage and large currents [3], and can realize high power density in a small circuit. This leads to high frequency EMI noise problems.

Switching devices in a power conversion circuit handle high power (loss) and high voltage. Thus, there are constraints on the placement of the electro mechanical components for heat radiation and insulation clearance. These differ from small signal and low voltage circuits. The printed circuit board (PCB) wiring is lengthened to meet these requirements, but lengthened wiring leads to non-ideal circuit wiring with finite resistance and inductance values. Estimating the parasitic components in the wiring and couplings, and their influence on circuit behavior must be assessed.

This paper estimates and models the parasitic components and their couplings in PCB wiring to provide EMC design of power conversion circuits. A dc-dc buck converter is illustrated to experimentally and numerically evaluate their influence on power conversion circuit operation.

2 Modeling parasitic inductance in power conversion circuit wiring

Figure 1 (a) depicts the circuit diagram of a dc-dc buck converter. A junction temperature Tj $< 150°C$ is necessary to avoid failure of Si power switching devices, which requires radiating heat originating from conduction and switching losses in the power device with a heat sink attached to the power switching device. Heat sinks for power devices are generally bulky and take up a great deal of space and ensure air flow. This constrains the placement of power switching devices and can lengthen the PCB wiring for the main circuit current or gate driving signals. PCB wiring pattern designs from the power source, load, and gate driver to the power switching device can have large self and mutual parasitic inductances, as shown in the analysis of twisty conductor alignment in Fig. 1 (b). The affect of parasitic components is evaluated by comparing the transient response of the circuit between the placement of power MOSFET at sites X and Y in Fig. 1 (b). Site X has fewer parasitic components and less influence of mutual coupling; site Y has larger parasitics

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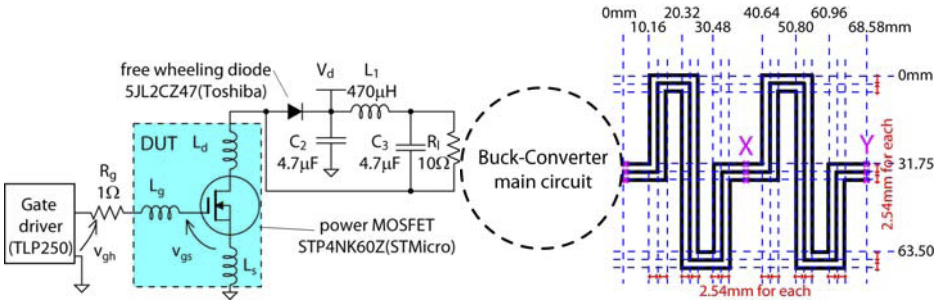
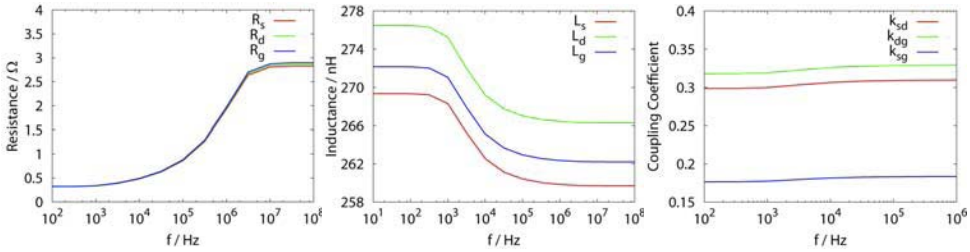


(a) Circuit diagram of a buck converter. (b) Wiring to the MOSFET.

Fig. 1. Tested power conversion circuit (dc-dc buck converter).



(a) Resistance. (b) Inductance. (c) Coupling coefficient.

Fig. 2. The frequency characteristics of identified parasitic component in wiring of PCB.

and the circuit response is more amenable to it. The parasitic component of the PCB for sites X and Y are estimated from the geometric structure of the wiring in Fig. 1 (b), based on partial element equivalent circuit (PEEC) method [4], using the software Fast Henry [5], where the copper conductor on an FR4 dialetric board is assumed to be 0.5 mm wide and 0.035 mm thick. The calculated parasitic components of resistance, inductance, and coupling coefficients for site Y are shown in Fig. 2 as frequency characteristics. A 500 kHz MOSFET switching frequency is used and modeled in the simulation as representative of the parasitic component to simplify the analysis.

The numerical simulation of power conversion at 500 kHz is performed by SPICE3f5, implementing the modeled parasitic wiring component shown in Fig. 1 (b). The simulated results are evaluated by comparing the simulation with experimental results.

3 Experimental and numerical simulation results

Figure 3 illustrates the experimental and numerical simulation results of the on and off response time for the gate-source (Vgs) and drain-source (Vds) MOSFET voltages when it is placed at X and Y in Fig. 1 (b). The buildup of gate voltage Vgs is affected by the Miller effect and shows a plateau around Vgs = 5 V (0 ∼ 100 ns) as shown in the experimental results of Figs. 3 (a) and (b). There are overshoots in Vgs at turn on, which become significant as the parasitic component increases with longer wiring. The effect of mutual

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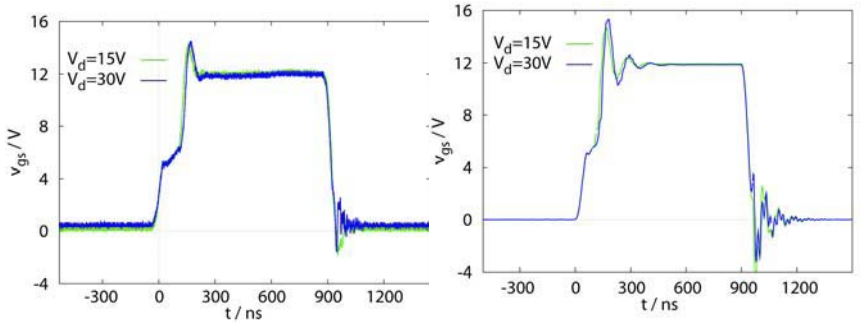
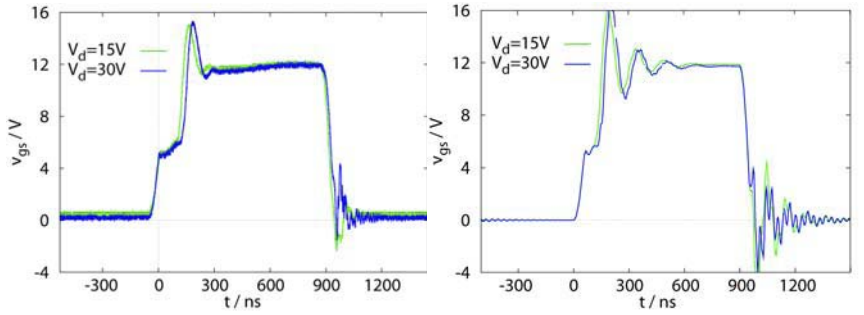
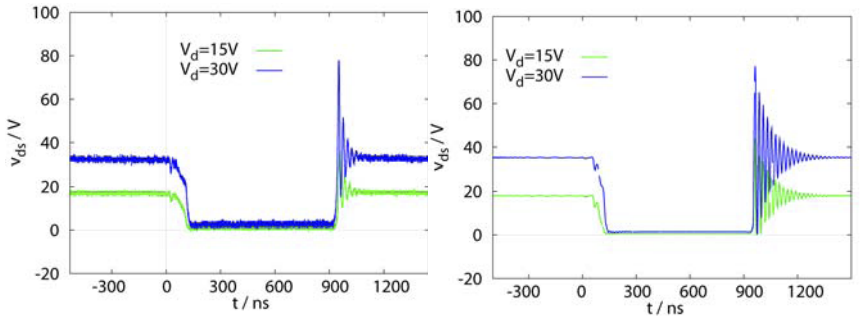


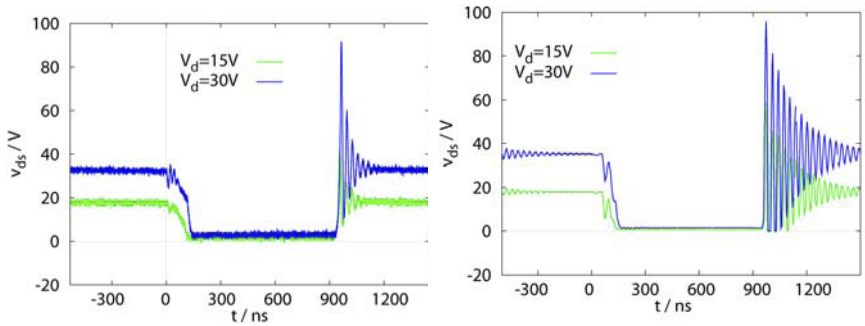
(a) Vgs response at site X.



(b) Vgs response at site Y.



(c) Vds response at site X.



(d) Vds response at site Y.

Fig. 3. Influences of parasitic component in the circuit for switching operation of power conversion circuit. (Left-experiment. Right-simulation.)

coupling is can be seen in the form of crosstalk between the drain and gate wiring. Lengthening the wiring makes the coupling effect significant, as seen by comparing Figs. 3 (a) and (b). The impact of drain current intensity is seen by comparing Vds = 15 and 30 V, where the drain current is doubled. The drain current begins to flow when Vgs reaches the plateau voltage, and

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the difference in drain current appears in the Vgs behavior. This difference is also identified in the simulation.

Ringing in Vds at the moment of turn on is small, as shown in Figs. 3 (c) and (d), whereas the ringing at the instant of turn off is large, and the peak voltage increases as the wiring is lengthened. The peak voltages obtained from numerical simulations almost coincide with the experimental results. The ringing oscillation frequencies were 9.23 and 7.39 MHz, respectively, for X and Y in the experiment, and in the simulation they were 8.79 and 6.94 MHz, respectively. They were approximately consistent, with a 7% error between the experiment and simulation values. This validates the estimated self and mutual parasitic inductance.

The oscillation damps and converges at about 200 ns for site X and 300 ns for site Y in the experiment, but are 400 ns for site X and 700 ns for site Y in the simulation. The numerical simulation does not accurately reproduce the dissipative phenomena in oscillation. The circuit model used for simulation considers only the parasitic component for 500 kHz, and its frequency characteristics are excluded. The wiring resistance increases with frequency due to the skin effect. The resistive component of the conductor on the PCB obtained from PEEC is shown in Fig. 2 (a). The wiring resistance becomes high when the frequency exceeds 100 kHz. The resistance doubles at 10 MHz to the switching frequency 500 kHz. This shows that the high frequency oscillation of ringing dampens quickly due to high resistance. This supposition is validated by the independence of dampening of the supplied voltage Vd. Therefore, a frequency dependent wiring resistance model should be used to simulate oscillation dampening.

4 Conclusion

This paper numerically evaluated the effects of parasitic inductance and mutual coupling intrinsic in the wiring of PCB on the operation of a power conversion circuit, and validated the results by experiment. The self and mutual parasitic inductance in longer PCB wiring induces a ringing phenomena and crosstalk at the instant of switching operation. It becomes exacerbated as the circuit wiring is lengthened and the parasitic component has a major influence. The switching transient response in the experiment with a dc-dc converter validated the parasitic component identified by the PEEC method. The frequency dependency of the resistive component stemming from skin effect affects the dampening of oscillations; therefore, the frequency independent constant resistance of the wiring used in the simulation caused differences in the convergence of the ringing. The application and validation of a frequency dependent resistance model in numerical simulations of power conversion circuits is planned as future work.

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