TITLE:

Experimental Study of Uniaxial-Stress Effects on DC Characteristics of nMOSFETs

AUTHOR(S):

Koganemaru, Masaaki; Ikeda, Toru; Miyazaki, Noriyuki; Tomokage, Hajime

---

CITATION:

Koganemaru, Masaaki ...[et al]. Experimental Study of Uniaxial-Stress Effects on DC Characteristics of nMOSFETs. IEEE Transactions on Components and Packaging Technologies 2010, 33(2): 278-286

ISSUE DATE:

2010-06

URL:

<http://hdl.handle.net/2433/131834>

RIGHT:

© 2010 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other users, including reprinting/ republishing this material for advertising or promotional purposes, creating new collective works for resale or redistribution to servers or lists, or reuse of any copyrighted components of this work in other works.

Experimental Study of Uniaxial-Stress Effects on DC Characteristics of nMOSFETs

Masaaki Koganemaru, Toru Ikeda, Noriyuki Miyazaki, and Hajime Tomokage

Abstract—Stress-induced shifts of the direct current characteristics on n-type metal oxide semiconductor field effect transistors (nMOSFETs) were investigated experimentally. The stress sensitivities of nMOSFET characteristics were measured by the 4-point bending method, and the gate-length dependence of transconductance shifts caused by uniaxial stress was evaluated. As a result, it is shown that the gate-length dependence of transconductance shifts is attributed to parasitic resistance of the nMOSFETs. Also, this paper verified the electron-mobility model proposed in the previous study that includes stress effects in comparison with the experimental results. As a result, several improvements for the electron-mobility model are proposed in this paper. We describe the change of the conduction-band energy induced by the shear deformation of silicon. The shear deformation with a uniaxial stress along the [110] direction of silicon should be considered in the change of the conduction-band energy.

Index Terms—Deformation potential, electron mobility, n-type metal oxide semiconductor field effect transistors (nMOSFETs), parasitic resistance, residual stress.

I. INTRODUCTION

SEMICONDUCTOR electronic devices are sometimes subjected to high-residual stress owing to various packaging processes, and such stress-induced effects result in a serious problem. The residual stress affects the electronic characteristics, such as the transconductance, of the transistor device. This is one of the most serious issues in the production of electronic devices and packages. It is believed that the stress effects on the electronic characteristics of the transistor device cannot be disregarded in a high-density package such as a device-embedded substrate. Hence, more studies on the stress-induced effects of a semiconductor device are needed, and an evaluation method must be established.

The stress-induced effects in bulk silicon are known as piezoresistance effects [1], [2]. In addition, several studies

have been carried out on stress-induced effects in metal oxide semiconductor field effect transistors (MOSFETs) [3]–[12]. Several phenomenological methods based on an empirical formula or a piezoresistance effect model have already been examined to evaluate the stress-induced effects in MOSFETs [5], [8]. However, since in practice there is a wide variety of devices, it is difficult to evaluate their stress effects using only an empirical method. Although it is, therefore, required to establish a versatile evaluation method such as a numerical simulation, there is not a sufficient comprehensive understanding of the physical phenomena of the stress effects. It is necessary to investigate the factors influencing the stress-induced effects in MOSFETs and to improve the analytical model that can be used in the numerical simulation.

Therefore, the objectives of this paper are to investigate the factors influencing the stress sensitivity of n-type MOSFETs (nMOSFETs) and to discuss the uniaxial-stress effects on nMOSFETs through the discussion about the electron-mobility variations induced by stress. That is, an electron-mobility model including the stress effects is studied in comparison with the present experimental results. Such an investigation can help to establish a numerical simulation model of stress-induced effects in semiconductor devices. In this paper, we measure the stress sensitivities of the transconductance in nMOSFETs using a 4-point bending fixture, and investigate its device-shape dependence and load-direction dependence. Then, we examine the influence of the parasitic resistance in the nMOSFET on the stress sensitivity. Furthermore, we discuss an electron-mobility model that takes the stress effects into consideration and compare it with the present experimental results. Several improvements of the electron-mobility model are shown.

II. EXPERIMENTS

A. Specimens

nMOSFET specimens were supplied by the manufacturer of semiconductor devices. Fig. 1 illustrates the schematic configurations of nMOSFETs on a 4-point bending specimen. The 4-point bending specimens are 30 mm in length, 5 mm in width and 0.63 mm in thickness. nMOSFETs are formed on the silicon (001) surface. The direction from the source to the drain (i.e., the current direction) is the [110] direction; the direction from the source to the drain is the [110] direction (“longitudinal” in Fig. 1) or the $\bar{1}10$ direction (“transverse” in Fig. 1). Since silicon is a cubic crystal, the [110] direction is equivalent

Manuscript received August 14, 2008; revised November 19, 2009. Date of current version June 9, 2010. This work was partly supported by the Knowledge Cluster Initiative Second Stage Grant implemented by the Ministry of Education, Culture, Sports, Science, and Technology (MEXT) of Japan. Recommended for publication by Associate Editor R. Prasher upon evaluation of reviewers' comments.

M. Koganemaru is with Mechanics and Electronics Research Institute, Fukuoka Industrial Technology Center, Yahatanishi-ku, Kitakyushu 807-0831, Japan (e-mail: koganema@fitc.pref.fukuoka.jp).

T. Ikeda and N. Miyazaki are with the Department of Mechanical Engineering and Science, Graduate School of Engineering, Kyoto University, Sakyo-ku, Kyoto 606-8501, Japan (e-mail: ikeda@solid.me.kyoto-u.ac.jp; miyazaki@mech.kyoto-u.ac.jp).

H. Tomokage is with the Department of Electronics Engineering and Computer Science, Fukuoka University, Jonan-ku, Fukuoka 814-0180, Japan (e-mail: tomokage@fukuoka-u.ac.jp).

Digital Object Identifier 10.1109/TCAPT.2010.2045378

Fig. 4. Experimental results of drain-current shifts induced by stress. (a) $W/L = 24/0.8$, longitudinal. (b) $W/L = 24/0.8$, transverse. (c) $W/L = 24/24$, longitudinal. (d) $W/L = 24/24$, transverse.

due only to the influence of parasitic series resistance in the source and drain [5]. We investigated the source of the gate-length dependence of the stress sensitivity using the present experimental results. For this purpose, we investigated the factors influencing the stress sensitivity using four types of nMOSFET that have different gate lengths with the same gate width $W = 24 \mu\text{m}$: $W/L = 24/24$, $24/12$, $24/6$, and $24/0.8$.

Fig. 7 shows the variations of the drain-current measured under the unstressed condition with the gate length L . The drain-current I_{DS} in the linear region is given by

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS} \quad (1)$$

where μ , V_{GS} , V_T , V_{DS} , and C_{ox} are the electron mobility, gate voltage, threshold voltage, drain voltage, and oxide capacity, respectively. Among the parameters in (1), only the gate length L is different among the nMOSFETs used in this paper. Considering (1), we can normalize the measured drain-current

curves in Fig. 7 by using the gate length L and the gate width W ; the measured drain-current curves were multiplied by L and divided by W . Fig. 8 shows the normalized drain-current curves. The least-squares line obtained by the measured drain-current values of $W/L = 24/24$ is shown in Fig. 8 as well. It is found from the figure that the measured drain-current curves for $W/L = 24/24$ and $W/L = 24/12$ agree well with the least-squares line of $W/L = 24/24$. On the other hand, the measured drain-current curves for $W/L = 24/0.8$ deviate from the least-squares line of $W/L = 24/24$. As described, one possible reason for such deviation is the parasitic resistance in the source and drain of the nMOSFET. It is well known that the performance of MOSFETs suffers from the parasitic resistance in the source and drain. In this paper, the parasitic resistances of the nMOSFETs are estimated according to the following procedure.

Fig. 9 illustrates an nMOSFET model including the parasitic resistance. R_S and R_D denote the parasitic resistance of the

(a)

(b)

Fig. 5. Experimental results of g_m change induced by stress. (a) $W/L = 24/0.8$. (b) $W/L = 24/24$. Fig. 6. Variations of stress sensitivity of g_m change with gate length.

Fig. 7. Variations of the drain-current measured under an unstressed condition with the gate length (longitudinal).

Fig. 8. Normalized drain-current curves under an unstressed condition (longitudinal).

Fig. 9. nMOSFET model including parasitic resistance.

source and that of the drain, respectively. The measured drain-current $I_{D'S'}$ including the parasitic resistance is given by [5]

$$I_{D'S'} = \mu C_{ox} \frac{W}{L} \left[V_{GS'} - V_T - \frac{V_{D'S'}}{2} \right] (V_{D'S'} - I_{D'S'} R_P) \quad (2)$$

where R_P represents $R_S + R_D$. Equation (2) can be transformed in order to make a comparison with (1) as follows:

$$I_{D'S'} = \mu C_{ox} \frac{W}{L} \left[V_{GS'} - V_T - \frac{V_{D'S'}}{2} \right] V_{D'S'} \left(1 - \frac{I_{D'S'}}{V_{D'S'}} R_P \right). \quad (2a)$$

Fig. 10. Normalized drain-current curves corrected using the parasitic resistance of 75Ω under unstressed condition (longitudinal).

A comparison between (1) and (2a) indicates that the relationship between the corrected drain-current I_{D0} without the parasitic resistance and the measured drain-current $I_{D'S'}$ is given by

$$I_{D'S'} = I_{D0} \left(1 - \frac{I_{D'S'}}{V_{D'S'}} R_P \right). \quad (3)$$

Then, (3) can be transformed as follows:

$$I_{D0} = \frac{I_{D'S'}}{1 - \frac{I_{D'S'}}{V_{D'S'}} R_P}. \quad (3a)$$

The corrected drain-current I_{D0} can be calculated from the measured drain-current $I_{D'S'}$ using (3a). In the next section, the value of the parasitic resistance will be estimated from the experimental results by using (3a).

B. Evaluation Method for Parasitic Resistance

The results shown in Figs. 7 and 8 suggest that the gross resistance for $W/L = 24/24$ is much larger than its parasitic resistance, and the drain-current for $W/L = 24/24$ varies linearly with the gate voltage. Therefore, in this paper, we can neglect the parasitic resistance for $W/L = 24/24$. In addition, $W/L = 24/24$ and $W/L = 24/0.8$ have the same configurations except the gate length L , and the distributions of impurities at the region of the source and drain are similar as well. Hence, we estimated the parasitic resistance R_P for $W/L = 24/0.8$ by fitting the drain-current curve for $W/L = 24/0.8$ corrected using (3a), which is a function of R_P , to the least-squares line for $W/L = 24/24$ shown in Fig. 8. As a result, it is determined that the parasitic resistance of $W/L = 24/0.8$ is 75Ω . This value will be used for the examination in the following section.

C. Results and Discussion

Fig. 10 shows the normalized drain-current curves corrected using the parasitic resistance of 75Ω under the unstressed condition. The same value was used as the value of the parasitic resistance for all nMOSFETs, because they have the

Fig. 11. Variations of the stress sensitivity of g_m change with the gate length obtained from the drain-current curves corrected by the parasitic resistance of 75Ω .

same distributions of impurities in the region of their source and drain. The normalized drain-current curves corrected by the parasitic resistance agree well with each other. The fabrication processes of semiconductor devices themselves induce an “intrinsic” residual stress, which affects the intrinsic electrical performance of the device. It is found from the figure that there are few differences in the intrinsic residual stress among the four kinds of nMOSFET used in this paper.

Fig. 11 shows the gate-length dependence of the stress sensitivity of g_m change obtained from the drain-current curves corrected using the parasitic resistance of 75Ω . As shown in Fig. 11, the corrected stress sensitivities of g_m change are regarded as a constant value regardless of the different gate lengths for each load direction (longitudinal or transverse). It is found from Fig. 11 that the major factor influencing the gate-length dependence of the stress sensitivity of g_m change is the parasitic resistance for the present nMOSFETs. In other words, the intrinsic electrical response against the “external” stress caused by the 4-point bending is similar for all nMOSFETs used in this paper. There are few differences in the external stress distribution in the channel region among the four kinds of nMOSFET as well. The present results obtained from an independent validation of the studies by Bradley *et al.* [5] approve the conclusions reached in literature [5]. That is, there is no significant gate-length dependence to the sensitivity of the intrinsic MOSFET channel to stress.

The above results indicate that the difference of the stress distribution in the channel region can be neglected for the present nMOSFETs. Therefore, in the following section, we can evaluate the stress-induced effects of the nMOSFETs by using the “nominal” stress generated by the 4-point bending. However, this does not mean that there is no influence of the stress distribution in the channel region of an nMOSFET. If we consider an nMOSFET with a very short channel, its electronic characteristics are considered to be affected by the stress distribution in the channel region [8].

Fig. 12. Schematic diagram of many-valley model in k -space for conduction band in silicon.

IV. EVALUATION OF UNIAXIAL-STRESS EFFECTS ON ELECTRON MOBILITY

A. Many-Valley Model

In the unstrained state, the conduction-band energy minima of bulk silicon degenerate into six equivalent “valleys” [13]. The “many-valley” energy surfaces of the silicon conduction band in k (wave number)-space are shown in Fig. 12. Each minimum is characterized by the longitudinal effective mass m_L^* along each principal axis (i -axis, $i = 1, 2, 3$) and the transverse effective mass m_T^* perpendicular to the principal axis. Here, m_L^* is larger than m_T^* . Hence, the mobility, which is longitudinal μ_L or perpendicular μ_T to the principal axis, is also anisotropic, i.e., $\mu_L < \mu_T$. However, in the unstrained state, since the six valleys of bulk silicon are equivalent, the “total” electron mobility μ along each direction is given by

$$\mu = \frac{\mu_L + 2\mu_T}{3} \quad (4)$$

and it is isotropic for all directions.

On the other hand, the conduction-band energy in the inversion layer of Si metal oxide semiconductor (MOS) is different from that of bulk silicon. Even in the unstrained state, the conduction-band energy valleys in the inversion layer of Si MOS split into the subband energies; six equivalent valleys split into twofold or fourfold valleys [14]. In this paper, the stress-induced effects of the electronic characteristics of the nMOSFETs were evaluated by defining the electronic-characteristics variation of unstressed nMOSFETs (not bulk silicon) as being equal to zero. The external stress causes the shifts of the conduction-band energy in the inversion layer, which lead to the variation of the electron mobility in the inversion layer (i.e., the variation of the electronic characteristics of nMOSFET).

B. Shifts of Conduction-Band Energy

In this paper, the shift of the conduction-band energy minima (valleys) due to strain, ΔE_c , is defined by the deformation-potential model [13]. ΔE_c is expressed by

$$\Delta E_c = \frac{\partial E}{\partial \varepsilon_{11}} e_1 + \frac{\partial E}{\partial \varepsilon_{22}} e_2 + \frac{\partial E}{\partial \varepsilon_{33}} e_3 + \frac{\partial E}{\partial \varepsilon_{12}} e_4 + \frac{\partial E}{\partial \varepsilon_{23}} e_5 + \frac{\partial E}{\partial \varepsilon_{31}} e_6 + \dots \quad (5)$$

TABLE I
REPRESENTATION OF DEFORMATION POTENTIALS IN A CUBIC SEMICONDUCTOR [15]

Type of Valley $\rightarrow$	100	110
$\partial E / \partial \varepsilon_{11}$	$\mathcal{E}_d + \mathcal{E}_u$	$\mathcal{E}_d + \mathcal{E}_u - \mathcal{E}_s/2$
$\partial E / \partial \varepsilon_{22}$	$\mathcal{E}_d$	$\mathcal{E}_d + \mathcal{E}_u - \mathcal{E}_s/2$
$\partial E / \partial \varepsilon_{33}$	$\mathcal{E}_d$	$\mathcal{E}_d - \mathcal{E}_u + \mathcal{E}_s$
$\partial E / \partial \varepsilon_{12}$	0	$\mathcal{E}_s/2$
$\partial E / \partial \varepsilon_{23}$	0	0
$\partial E / \partial \varepsilon_{31}$	0	0

$$e_1 = \varepsilon_{11}, e_2 = \varepsilon_{22}, e_3 = \varepsilon_{33}, e_4 = \varepsilon_{12} + \varepsilon_{21},$$

$$e_5 = \varepsilon_{23} + \varepsilon_{32}, e_6 = \varepsilon_{31} + \varepsilon_{13} \quad (6)$$

where ε_{ij} is the strain tensor and $\partial E / \partial \varepsilon_{ij}$ is the “deformation-potential constant.” Considering that the valleys lie on a symmetry axis, it is possible to describe all the deformation-potential constants in terms of two or three independent constants, as shown in Table I [15]. Hence, the shifts of the conduction-band energy (minimum) along the i -axis valley ΔE_i can be expressed through the deformation potential constants $\mathcal{E}_d$ and $\mathcal{E}_u$ [15]

$$\Delta E_i = \mathcal{E}_d(\varepsilon_{11} + \varepsilon_{22} + \varepsilon_{33}) + \mathcal{E}_u \varepsilon_{ii}. \quad (7)$$

The values of the deformation potentials have been obtained by cyclotron resonance experiments and numerical simulations. We used the following values: $\mathcal{E}_d = 1.1 \text{ eV}$ and $\mathcal{E}_u = 10.5 \text{ eV}$ [16]. The strain tensor ε_{ij} is converted from the stress tensor using the compliance coefficients of silicon [17]. The shifts of conduction-band energy can be calculated using (7), and the stress-induced variations of the electron mobility can then be estimated using the following electron-mobility model.

C. Electron-Mobility Model

Egley and Chidambarrao proposed an electron-mobility model that takes the stress effects into consideration [18]. In their model, the effects of stress or strain are seen in the change of electron mobility which reflects the relative change of the electron population of each valley. The change in the average relaxation time due to stress [14] is neglected. In this paper, we used Egley’s model with some simplification [19]. Boltzmann distribution was used as the distribution function of electrons for each valley. The distribution function $f(E)$ is given by

$$f(E) = \exp\left(-\frac{E - E_F}{k_B T}\right) \quad (8)$$

where k_B is the Boltzmann’s constant, T is the lattice temperature, and E_F is the Fermi energy. When we consider the shift of the conduction-band energy due to the stress effects, (8) is replaced by

$$f(E) = \exp\left(-\frac{E - E_F + \Delta E_{\text{stress}}}{k_B T}\right) \quad (9)$$

where ΔE_{stress} is the shift of conduction-band energy induced by stress. Therefore, the population rate of the electron on the i -axis valley is given by

$$v_i = \frac{\exp\left(-\frac{E-E_F+\Delta E_i}{k_B T}\right)}{\sum_{i=1}^3 \exp\left(-\frac{E-E_F+\Delta E_i}{k_B T}\right)} = \frac{\exp\left(-\frac{\Delta E_i}{k_B T}\right)}{\sum_{i=1}^3 \exp\left(-\frac{\Delta E_i}{k_B T}\right)}. \quad (10)$$

The gradient of the quasi-Fermi level is assumed to be parallel to the current flow. The coefficient of electron-mobility change f_{stress} along the current flow is, therefore, given by

$$f_{\text{stress}} = \frac{\sum_{i=1}^3 c_i \cdot \exp\left(-\frac{\Delta E_i}{k_B T}\right)}{\sum_{i=1}^3 \exp\left(-\frac{\Delta E_i}{k_B T}\right)} \quad (11)$$

where c_i represents the effect of the i -axis valley on the electron mobility along the current flow direction. If the nMOSFET is formed on the silicon (001) surface and the angle between the 1-axis and the current flow direction is θ , c_i is given by

$$c_1 = R_L \cos^2 \theta + R_T \sin^2 \theta \quad (12)$$

$$c_2 = R_T \cos^2 \theta + R_L \sin^2 \theta \quad (13)$$

$$c_3 = R_T \quad (14)$$

where R_L and R_T are expressed by

$$R_L = \frac{\mu_L}{\mu} = \frac{\mu_L}{(\mu_L + 2\mu_T)/3} = \frac{3}{1 + 2(m_L^*/m_T^*)} \quad (15)$$

$$R_T = \frac{\mu_T}{\mu} = \frac{\mu_T}{(\mu_L + 2\mu_T)/3} = \frac{3(m_L^*/m_T^*)}{1 + 2(m_L^*/m_T^*)}. \quad (16)$$

In the above equations, μ is the nominal isotropic mobility without stress given by (4). From the above relationship, the stress-induced electron mobility μ_{stress} is given by

$$\mu_{\text{stress}} = f_{\text{stress}} \cdot \mu. \quad (17)$$

In the following section, the above electron-mobility model will be verified by comparing the electron-mobility variations calculated by (11) with that obtained in the experimental results.

D. Results and Discussion

The rate of electron-mobility change estimated by the above electron-mobility model was compared with that obtained in the experimental results shown in Section II. The rate of electron-mobility change $\Delta\mu/\mu$ can be defined as

$$\frac{\Delta\mu}{\mu} = \frac{\mu_{\text{stress}} - \mu}{\mu} = f_{\text{stress}} - 1 \quad (18)$$

where f_{stress} is given by (11). In contrast, the drain-current I_{DS} is given by (1). If we assume that the shape deformation of the nMOSFET due to stress is minute in (1), the relationship between the rate of drain-current change and the rate of electron-mobility change is given by [5]

$$\frac{\Delta I_{DS}}{I_{DS}} \approx \frac{\Delta\mu}{\mu}. \quad (19)$$

Fig. 13. Comparison between the estimated results of electron-mobility change and the experimental results ($W/L = 24/24$).

Therefore, the experimental results for the rate of electron-mobility change can be obtained from the experimental results shown in Fig. 4 using (19).

Fig. 13 shows a comparison between the estimated results of electron-mobility change and the experimental results. It is found from the figure that the electron-mobility model is not able to provide the load-direction dependence obtained in the experimental results. In (7), when a uniaxial stress is applied along the 1-axis, the relationship among the shifts of conduction-band energy is $\Delta E_1 \neq \Delta E_2 = \Delta E_3$ because of $\varepsilon_{11} \neq \varepsilon_{22} = \varepsilon_{33}$. The shift of the conduction-band energy is schematically shown in Fig. 14(a). The solid lines show the effect of stress. Then, we consider that a uniaxial stress is applied along the [110] direction. The relationship among the shifts of conduction-band energy is calculated using (7) as $\Delta E_1 = \Delta E_2 \neq \Delta E_3$. The shifts of the conduction-band energy are schematically shown in Fig. 14(b). If the relationship among the shifts of conduction-band energy is $\Delta E_1 = \Delta E_2 \neq \Delta E_3$, both f_{stress} along the [110] direction and that along the $[\bar{1}10]$ direction become the same value. Therefore, the estimated results are different from the experimental results depending on the load direction as shown in Fig. 5.

It is clear from the above discussion that some improvements of the electron-mobility model proposed by Egley and Chidambarrao [18] are necessary to evaluate the uniaxial-stress effects on nMOSFET. We suggest the shifts of the conduction-band energy induced by shear deformation in addition to (7). That is to say, we consider that the deformation potential $\partial E/\partial \varepsilon_{12}$ is not zero, and the shift of the conduction-band energy induced by shear deformation is schematically shown in Fig. 14(c). Considering the representation of deformation potentials given in Table I, it might be inferred that the shift of the conduction-band energy ΔE_3 of a 3-axis valley can be defined as

$$\Delta E_{3(110)} = \bar{\varepsilon}_d(\varepsilon_{11} + \varepsilon_{22} + \varepsilon_{33}) + \bar{\varepsilon}_u \varepsilon_{33} + \frac{1}{2} \bar{\varepsilon}_s \varepsilon_{12} \quad (20)$$

Fig. 14. Schematic diagrams of stress effects in valleys for n-silicon. (a) [100] Uniaxial stress in (7). (b) [110] Stress in (7). (c) Shear deformation caused by [110] uniaxial stress.

$$\Delta E_{3(\bar{1}10)} = \mathcal{E}_d(\varepsilon_{11} + \varepsilon_{22} + \varepsilon_{33}) + \mathcal{E}_u\varepsilon_{33} - \frac{1}{2}\mathcal{E}_s\varepsilon_{12} \quad (21)$$

where $\mathcal{E}_s/2$ indicates $\partial E/\partial \varepsilon_{12}$. It is considered that the shifts of the conduction-band energy ΔE_1 of a 1-axis valley and ΔE_2 of a 2-axis valley can be defined including the deformation potential constant $\mathcal{E}_s$ as well. For these improvements, we need both further experiments and further understanding with regard to the physical phenomena of uniaxial-stress effects.

The validity of the electron-mobility model for evaluating the uniaxial-stress effects is still open to discussion. It is considered that a numerical simulation is versatile and is useful for evaluating the reliability issues induced by mechanical stress. Hence, the carrier-mobility model for the simulation method should be further examined and improved.

V. CONCLUSION

We have experimentally investigated the uniaxial-stress effects on nMOSFETs. It was demonstrated that the stress-induced shifts of dc characteristics depend on the device shape and load direction in nMOSFETs. We evaluated the influence of parasitic series resistance in the source and drain region of nMOSFETs on the transconductance change induced by stress. The result showed that the stress sensitivity of the transconductance change is constant regardless of the gate length of the nMOSFETs. Also, we discussed an electron-mobility model, taking the stress effects into consideration, and proposed the improvement of the electron-mobility model so as to account for the shear deformation in the shift of conduction-band energy induced by stress. This paper contributes to the establishment of a method of evaluating the stress-induced effects on semiconductor devices.

ACKNOWLEDGMENT

The authors would like to thank S. Yoshida at New Japan Radio Company, Ltd., Fujimino, Japan, as well as Y. Iseri at Mitsumi Electric Company, Ltd., Iizuka, Japan, for their helpful support throughout the experiments.

REFERENCES

- [1] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, 1954.
- [2] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *IEEE Trans. Electron Devices*, vol. 29, no. 1, pp. 64–70, Jan. 1982.
- [3] A. Hamada, T. Furusawa, N. Saito, and E. Takeda, "A new aspect of mechanical stress effects in scaled MOS devices," *IEEE Trans. Electron Devices*, vol. 38, no. 4, pp. 895–900, Apr. 1991.
- [4] C. L. Huang, H. R. Soleimani, G. J. Grula, J. W. Sleight, A. Villani, H. Ali, and D. A. Antoniadis, "LOCOS-induced stress effects on thin-film SOI devices," *IEEE Trans. Electron Devices*, vol. 44, no. 4, pp. 646–650, Apr. 1997.
- [5] A. T. Bradley, R. C. Jaeger, J. C. Suhling, and K. J. O'Connor, "Piezoresistive characteristics of short-channel MOSFETs on (100) silicon," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2009–2015, Sep. 2001.
- [6] W. Zhao, J. He, R. E. Belford, L. E. Wernersson, and A. Seabaugh, "Partially depleted SOI MOSFETs under uniaxial tensile strain," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 317–323, Mar. 2004.
- [7] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, R. Gwoziecki, S. Orain, E. Robilliart, C. Raynaud, and H. Dansas, "Electrical analysis of mechanical stress induced by STI in short MOSFETs using externally applied stress," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1254–1261, Aug. 2004.
- [8] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, and R. Gwoziecki, "Electrical analysis of external mechanical stress effects in short channel MOSFETs on (001) silicon," *Solid-State Electron.*, vol. 48, no. 4, pp. 561–566, 2004.
- [9] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial versus substrate induced biaxial stressed Si and Ge channel MOSFETs," in *Proc. Int. Electron Devices Meeting*, 2004, pp. 221–224.
- [10] H. Irie, K. Kita, K. Kyuno, and A. Toriumi, "In-plane mobility anisotropy and universality under uni-axial strains in n and p-MOS inversion layers on (100), (110), and (111) Si," in *Proc. Int. Electron Devices Meeting*, 2004, pp. 225–228.
- [11] K. Uchida, R. Zednik, C. H. Lu, H. Jagannathan, J. McVittie, P. C. McIntyre, and Y. Nishi, "Experimental study of biaxial and uniaxial strain effects on carrier mobility in bulk and ultrathin-body SOI MOSFETs," in *Proc. Int. Electron Devices Meeting*, 2004, pp. 229–232.
- [12] K. Uchida, T. Krishnamohan, K. C. Saraswat, and Y. Nishi, "Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime," in *Proc. Int. Electron Devices Meeting*, 2005, pp. 135–138.
- [13] K. Seeger, *Semiconductor Physics*, 4th ed. New York: Springer-Verlag, 1989, chs. 2 and 7.
- [14] S. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, "Comparative study of phonon-limited mobility of 2-D electrons in strained and unstrained Si metal-oxide-semiconductor field effect transistors," *J. Appl. Phys.*, vol. 80, no. 3, pp. 1567–1577, 1996.
- [15] C. Herring and E. Vogt, "Transport and deformation-potential theory for many-valley semiconductors with anisotropic scattering," *Phys. Rev.*, vol. 101, no. 3, pp. 944–961, 1956.
- [16] M. V. Fischetti and S. E. Laux, "Band structure, deformation potential, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2252, 1996.
- [17] J. J. Wortman and R. A. Evans, "Young's modulus, shear Modulus, and Poisson's ratio in silicon and germanium," *J. Appl. Phys.*, vol. 36, no. 1, pp. 153–156, 1965.
- [18] J. L. Egley and D. Chidambarrao, "Strain effects on device characteristics: Implementation in drift-diffusion simulators," *Solid-State Electron.*, vol. 36, no. 12, pp. 1653–1664, 1993.
- [19] *HyDeLEOS User's Manual*, Selete, Inc., Tsukuba, Japan, 2000.

Masaaki Koganemaru was born in Fukuoka, Japan, in 1968. He received the B.E. degree in nuclear engineering and the M.E. degree in science and engineering from Kyushu University, Fukuoka, Japan, in 1992 and 1994, respectively, and the Ph.D. degree in mechanical engineering from Kyoto University, Kyoto, Japan, in 2008.

Since 1994, he has been a Researcher with Mechanics and Electronics Research Institute, Fukuoka Industrial Technology Center, Kitakyushu, Japan. His current research interests include device simulation

of strained-silicon metal oxide semiconductor field effect transistors.

Toru Ikeda received the B.S., M.S., and Ph.D. degrees in chemical engineering from Kyushu University, Fukuoka, Japan, in 1986, 1988, and 1992, respectively. After his doctoral study, he was with Kyushu University as a Research Associate for four years and an Associate Professor for eight years. Since 1994, he has been an Associate Professor with the Department of Mechanical Engineering and Science, Graduate School of Engineering, Kyoto University, Kyoto, Japan. He has published over 75 journal papers and over 60 conference papers

in the area of electronic packaging, fracture mechanics and computational mechanics. His current research interests include the interfacial fracture mechanics, reliability of electronic packages, and computational mechanics.

Dr. Ikeda received the Encouragement Award for Young Researchers from the Division of Composite, Society of Material Science, Japan, in 1997, the Japan Institute of Electronic Packaging (JIEP) Award for outstanding paper in 2002, the Japan Society of Mechanical Engineers (JSME) Funai Award in 2004, the Best Paper Award in Microjoining and Assembly Technology in Electronics 2006: Mate 2006 Conference of the Japan Welding Society, the JSME Medal for Outstanding Paper in 2008, and the Best Paper Award in Micro Electronics Symposium 2008 Conference of the JIEP.

Noriyuki Miyazaki received the B.E. and M.E. degrees in nuclear engineering, and the Ph.D. degree in engineering from the University of Tokyo, Tokyo, Japan, in 1972, 1974, and 1977, respectively.

After working as a Research Scientist with the Japan Atomic Energy Research Institute, Tokai-mura, Japan, for six years, he joined Kyushu University, Fukuoka, Japan, in 1983. He spent 21 years with Kyushu University as an Associate Professor and a Professor with the Department of Chemical Engineering. He has been a Professor with the

Department of Mechanical Engineering and Science, Graduate School of Engineering, Kyoto University, Kyoto, Japan, since 2004. He has published over 234 journal papers and over 122 conference papers. His current research interests include the fields of computational solid mechanics and fracture mechanics, especially, their applications to the mechanical strength studies of single crystals for electronic/optical devices, and the reliability studies of electronic packaging.

Dr. Miyazaki received several awards from the Japan Society of Mechanical Engineers, the Japan Institute of Electronic Packaging and the International Conference on Computational Engineering Science. He is an Editorial Board Member of several international journals, including: *International Journal of Pressure Vessels and Piping*, *International Journal of Computational Methods*, and *Computer Modeling in Engineering and Sciences*. He is currently the President of the Japan Association for Computational Mechanics, a General Council Member of the Asian Pacific Association for Computational Mechanics, and the International Association for Computational Mechanics. He has served as the Co-Chair of the International Conference Concerning Electronic Packaging, the 2005 InterPACK Conference, and the 7th International Conference on Electronics Materials and Packaging (EMAP2005).

Hajime Tomokage was born in Yamaguchi, Japan, in 1953. He received the B.Eng., M.Eng., and Dr. Eng. degrees in electrical engineering from Kyushu University, Fukuoka, Japan, in 1977, 1979, and 1982, respectively.

He was a Lecturer with Fukuoka University from 1982 to 1987, until becoming an Associate Professor in 1987. He has been a Professor with the Department of Electronics Engineering and Computer Science, Fukuoka University, since 1992. His current research interests include nanotechnology with carbon

materials and high-frequency system-in-a-package design and evaluation.

Dr. Tomokage has been the President of the Japan Institute of Electronics Packaging, since 2009 and the Director of Kyushu Chapter, Japan Society of Applied Physics, since 2000. He has been the Chairman of the International Workshop on Microelectronics Assembling and Packaging, since 2001.