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Characterization of the gate-voltage dependency of input capacitance in a SiC MOSFET

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Abstract: The charge/discharge phenomenon of capacitance between terminals in a power MOSFET affects on its switching behavior of the device. The input capacitance is composed of the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD}, which vary with gate voltage V_{GS}. This paper characterizes the relationship between the input capacitance of a SiC MOSFET and the gate voltage with considering the internal device structure. The results give us a clue to understand the switching dynamics of the power MOSFET.

Keywords: C-V characteristics, voltage dependency, SiC, MOSFET

Classification: Electron devices, circuits, and systems

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1 Introduction

Power MOSFETs are practically used in high frequency switching power converter circuits due to fast turn-off capability [1, 2]. Recently, power converters have been requested to operate at high voltage, high-temperature, and fast switching to realize their high performances. However, the limitation to the above requirements is low for the silicon (Si) power devices. To overcome the difficulty, silicon carbide (SiC) power devices have been researched and developed because of its several superior physical characteristics than Si [2, 3].

The equivalent capacitance between terminals of a power device affects on its switching behavior, because it must be charged and discharged at the turn-off and turn-on operations. The capacitance in a power device changes nonlinearly with the applied voltage between terminals, because it comprises the depletion capacitance in the device [4]. Then, it is important to characterize the C-V characteristics of the SiC MOSFET to estimate its switching performance. Figures 1 (a) and (b) show the equivalent capacitance between terminals and the cross section of the SiC DiMOSFET cell, respectively [2, 3]. The equivalent capacitances are composed of the capacitances C_{GS}, C_{GD}, and C_{DS}. Here, the C_{GS} and C_{GD}, which combine the gate oxide and depletion capacitance, constitute the input capacitance $C_{ISS}(= C_{GS} + C_{GD})$ [4, 5]. The C_{GS} mainly depends on the applied gate-source voltage V_{GS}, and the C_{GD} varies with both the applied gate-source voltage V_{GS} and drain-source voltage V_{DS}.

This paper focuses on the gate-source capacitance C_{GS}, gate-drain capacitance C_{GD}, and input capacitance C_{ISS} of power MOSFETs. Then it compares the difference in V_{GS} dependency between the SiC MOSFET and the Si MOSFET to estimate the difference in their switching behavior. The constitution of internal parasitic components in the devices are also addressed.

2 Interelectrode input capacitance of SiC MOSFET and setup for characterization

This section describes the origin of the interelectrode capacitive components in a SiC MOSFET and discusses their gate-voltage dependency.

2.1 Input capacitance C_{ISS} of SiC MOSFET

Figure 1 (b) illustrates the simplified cross section of one cell structure in a SiC DiMOSFET studied in this paper [2, 3]. SiC DiMOSFET is fabricated to have the structure similar to that of a Si DMOSFET [1]. The main differences between these two devices are the fabrication process and dimensions of p well and n^+ source regions. They are formed by ion implantation for SiC

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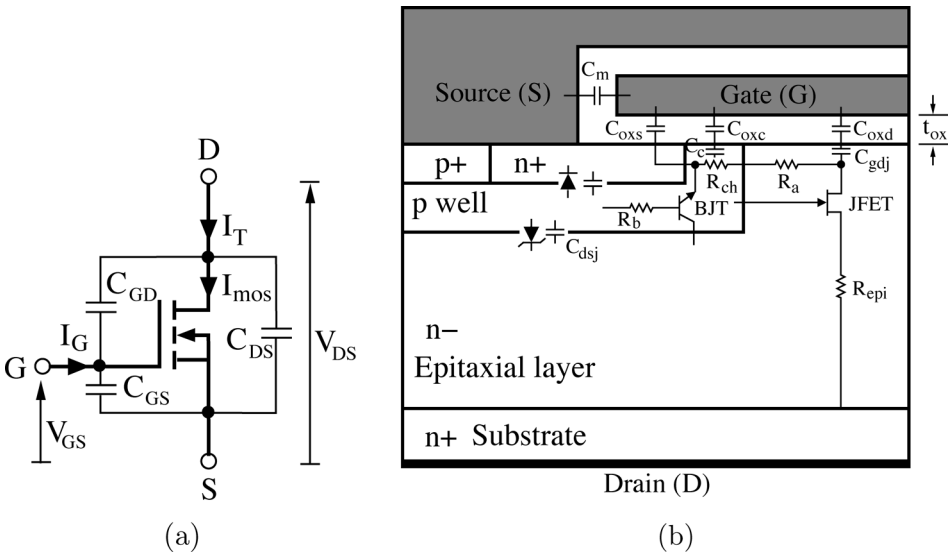

Fig. 1. Example of a gate-controlled transistor to illustrate parasitic components. (a) Equivalent capacitance between terminals of SiC DiMOSFET. (b) Cross section of a SiC DiMOSFET cell.

DiMOSFET and shallower than a Si DMOSFET formed by diffusion. The various internal parasitic components of the device are superimposed on its cross section in Fig. 1 (b). The physical capacitances residing in the SiC DiMOSFET are composed of the gate oxides and the depletion layer formed in the semiconductor. They are integrated into the equivalent capacitances between terminals of MOSFET C_{GS}, C_{GD}, and C_{DS}. The C_{DS} corresponds to the junction capacitance stemmed by depletion at the junction between the p well and the n$^-$-epitaxial layer C_{dsj}. It largely depends on V_{DS}. The two other C_{GS} and C_{GD} have MOS structures provided with inversion charge injectors. The C_{GS} is comprised of the gate oxide capacitance between the gate-source electrode C_m, the capacitance between the gate electrode and source n$^+$ region C_{oxs}, the capacitance between the gate electrode and the top surface of the p well region C_{oxc}, and the capacitance between the depletion region of the p well region under the gate C_c. The C_c varies depending on V_{GS}. Though the polysilicon is utilized as gate electrode, it also depletes the applied gate voltage. It is heavily doped, so that its effect on the synthesized capacitance can be neglected [6]. As for C_{GD}, it is the series connection of the gate-drain oxide capacitance C_{oxd} and the drain depletion layer beneath the gate oxide capacitance C_{gdj}. It varies with gate-drain voltage $V_{GD}(= V_{GS} - V_{DS})$. Thus, C_{GS} and C_{GD} can be expressed by the capacitive components as

$$\begin{cases} C_{GS} = C_m + C_{oxs} + \frac{1}{1/C_{oxc}+1/C_c}, \\ C_{GD} = \frac{1}{1/C_{oxd}+1/C_{gdj}}. \end{cases} \quad (1)$$

In this paper, we focus on the characterization of C_{ISS}, which is sum of the C_{GS} and C_{GD}, and the dependency on V_{GS}. C_m, C_{oxs}, C_{oxc}, and C_{oxd}, related to the gate oxide, do not change with the applied voltage. C_c and C_{gdj}, originated from the depletion layer in the top of p well and n$^-$-epitaxial

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layer semiconductor respectively, are associated with the depletion region formed in the semiconductor beneath the gate oxide. They can be derived from the depleted space charge Q_s, which varies as a function of the surface potential of semiconductor ψ_s. The surface potential ψ_s is governed by gate voltage [4, 5]. Then, the depleted charge sensitivity to the voltage expresses a differential capacitance $dQ_s/d\psi_s$.

2.2 Characterization setup

The interelectrode input capacitance $C_{ISS}(= C_{GS} + C_{GD})$ of the SiC DiMOSFET has already been discussed in the section 2.1. Voltage dependence of the capacitance is evaluated by the clarification of the device structure and fabrication. The C-V characteristics are precisely measured by a LCR meter with applying the dc bias voltage V_{GS} and V_{DS} to the device, through C-V measurement fixture in Ref. [7]. In this paper, we measure C_{GS}, C_{GD}, and C_{ISS} individually.

3 Results and discussion of C-V characteristics

Figures 2 (a) and (b) show the measured C-V characteristics, which illustrate the relationships between the measured C_{GS}, C_{GD}, C_{ISS}, and the V_{GS}, for a 600-V, 2-A Si DMOSFET and a 900-V, 1-A SiC DiMOSFET, respectively. The measurements are performed with setting $V_{DS} = 0\,V$ to minimize the depletion region at the top of the n^--epitaxial layer (C_{gdj}) and to neglect its influence in the equivalent capacitance. When V_{GS} is swept from $-25\,V$ to $+25\,V$, the relationship between the capacitance characteristics and the device structure can be characterized.

When the applied voltage V_{GS} is lower than $-5\,V$ (Si DMOSFET) and $-7\,V$ (SiC DiMOSFET), the capacitance holds a constant value. This is because the carrier accumulation occurs at the device channel in the top of the p well region. The C_c results in very large capacitance or disappears with conducting condition. Then, the C_{GS} achieves their highest values. On the other hand, the inversion occurs at the top of the n^--epitaxial layer under the gate oxide as the negative V_{GS} attracts holes to the interface and constitutes depletion layer underneath, then the C_{gdj} is very small. Thus, the C_{GD} achieves their lowest values.

When the applied voltage V_{GS} becomes higher than $-5\,V$ (Si DMOSFET) and $-7\,V$ (SiC DiMOSFET), the C_{GS} begins to decrease and reaches to a minimum around $V_{GS} = 3\,V$ (Si DMOSFET) and $= 1\,V$ (SiC DiMOSFET), because the holes in the p well are repelled from the surface. Thus, the depletion layer appears at the surface of the channel. The inversion at the channel begins to occur with increasing V_{GS} when V_{GS} exceeds $3\,V$ (Si DMOSFET) and $1\,V$ (SiC DiMOSFET). The C_{GS} increases up to the threshold gate voltage V_T where the C_c disappears by channel conduction. At the same region of V_{GS}, the electrons are attracted to the top of the JFET region or the n^--epitaxial layer under the gate oxide. Thus, it induces the accumulation layer there, and increase of C_{gdj}. Then, the C_{GD} becomes large within the

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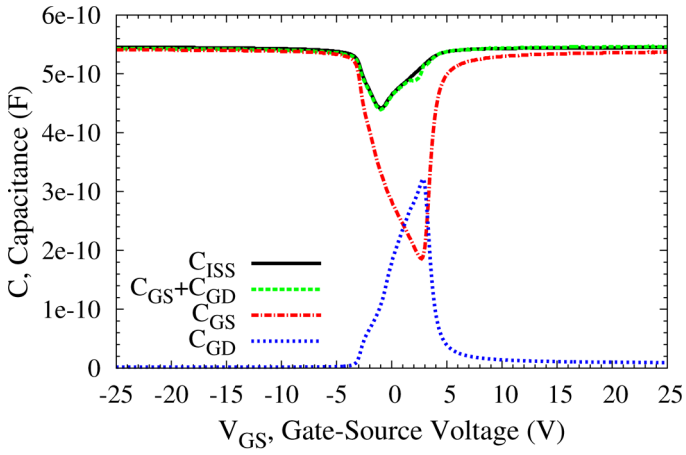
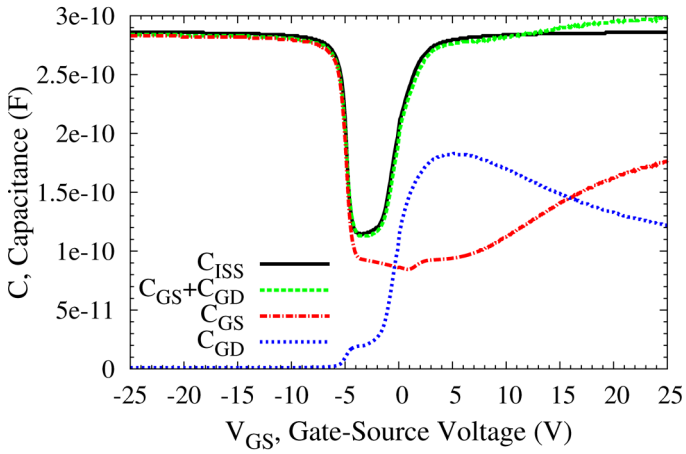


(a) Si DMOSFET



(b) SiC DiMOSFET

Fig. 2. Measured C-V characteristics.

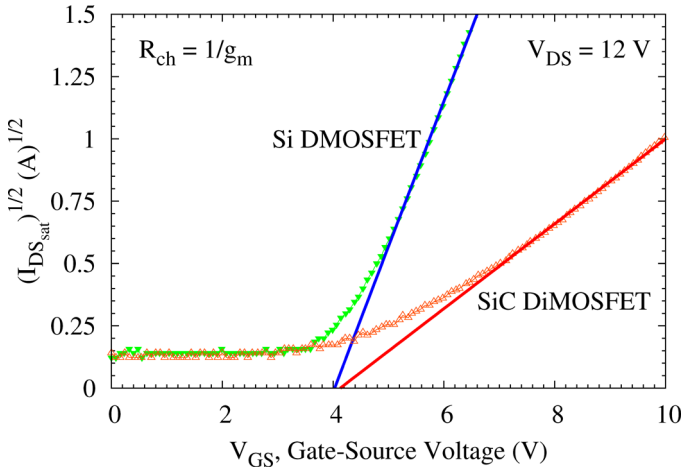


Fig. 3. Measured $\sqrt{I_{\mathrm{DS_{sat}}}}$-$V_{\mathrm{GS}}$ characteristics.

$-3\,\mathrm{V} < V_{\mathrm{GS}} < 3\,\mathrm{V}$ region for the Si DMOSFET and $-5\,\mathrm{V} < V_{\mathrm{GS}} < 5\,\mathrm{V}$ for the SiC DiMOSFET. The V_{T} of the Si DMOSFET is 4.0 V and of the SiC DiMOSFET is 4.1 V, as shown in Fig. 3. The V_{T} from measured C-V characteristics corresponds to the V_{T} from the measured $\sqrt{I_{\mathrm{DS_{sat}}}}$-$V_{\mathrm{GS}}$ char-

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acteristics. In Fig. 3, when $V_{GS} < V_T$, the measured $\sqrt{I_{DS_{sat}}}$ is kept around $0.1\,A^{1/2}$. This does not mean leakage current, but is the residual error due to quantization of A/D converter in curve tracer.

The channel conducts when the applied voltage V_{GS} becomes higher than the V_T. Then, the strong inversion of electrons occurs at the top of the p well region. The C_{GS} of the Si DMOSFET becomes abruptly large and saturates with increasing V_{GS}, but the C_{GS} of the SiC DiMOSFET becomes gradually large and hardly saturates with increasing V_{GS}. This nonsaturable characteristics stem from the short channel effects [8]. The channel length of the SiC DiMOSFET is approximately equal to $0.75\,\mu$m. Thus, the channel resistance R_{ch} [see Fig. 1 (a)] of the Si DMOSFET is much lower than that of the SiC DiMOSFET. At the same region of V_{GS}, the electrons are attracted to the surface of the JFET region and forms the accumulation layer when V_{DS} is lower than V_{GS}. The C_{GD} of the Si DMOSFET becomes abruptly small and saturates with increasing V_{GS}, but the C_{GD} of the SiC DiMOSFET becomes gradually small and hardly saturates with increasing V_{GS}. The variation of the C_{GD} associates with the total of the parasitic resistance R_{JFET} and epitaxial resistance R_{epi}, which depend on the impurity concentration in n^--epitaxial layer [1, 9]. These resistances of the Si DMOSFET are higher than that of the SiC DiMOSFET, because the doped impurity concentration of Si DMOSFET is lower than that of SiC DiMOSFET [2, 9]. The C_{GD} characteristics in Fig. 2 validates this facts.

As the results in Figs. 2 (a) and (b), the C_{ISS} are obtained as the sum of C_{GS} and C_{GD}. In Fig. 2 (b), the measured C_{ISS} is smaller than the sum of C_{GS} and C_{GD}. This can be attributted to the overlap area, between p well and n^--epitaxial layer, which appears through the strong inversion and the accumulation of electrons at the top of them individually. The difference of the C-V characteristics between the Si DMOSFET and the SiC DiMOSFET is explained by the short channel effects in SiC DiMOSFET and the doping density difference in the n^--epitaxial layer.

4 Conclusions

This paper has experimentally shown the relationship between input capacitance C_{ISS} and gate-voltage of the SiC DiMOSFET with comparison to the Si DMOSFET, precisely. Input capacitance C_{ISS} results from the sum of the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD}. The measured capacitances can be explained along the device structure and the physical phenomenon in the device, which is distinguished as the accumulation, the depletion, and the inversion condition. The dynamics in the switching operation of the devices can be investigated based on these results.

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