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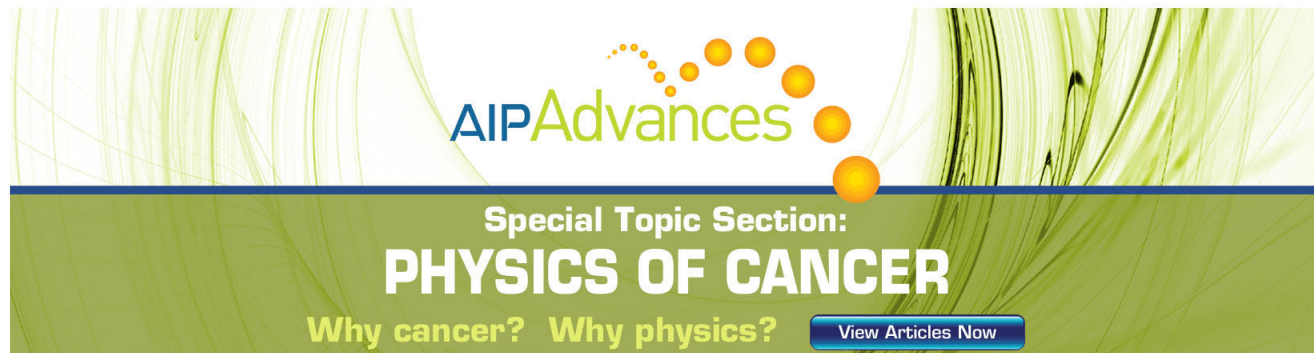
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Molecular doping effect in bottom-gate, bottom-contact pentacene thin-film transistors

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A bottom-gate, bottom-contact (BGBC) organic thin-film transistor (OTFT) with carrier-doped regions over source-drain electrodes was investigated. Device simulation with our originally developed device simulator demonstrates that heavily doped layers (p^+ layers) on top of the source-drain contact region can compensate the deficiency of charge carriers at the source-channel interface during transistor operation, leading to the increase of the drain current and the apparent field-effect mobility. The phenomena expected with the device simulation were experimentally confirmed in typical BGBC pentacene thin-film transistors. The 5-nm-thick p^+ layers, located 10 nm (or 20 nm) over the source-drain electrodes, were prepared by coevaporation of pentacene and 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane as an acceptor dopant. Since the molecular doping in this study can increase the drain current without positive shift of threshold voltage, p^+ layers were formed precisely on top of the source-drain regions. This study shows that common inferior characteristics of bottom-contact OTFT devices mainly derive from the supply shortage of charge carriers to the channel region. The importance of reliable molecular doping techniques or heavily doped semiconductor materials for improving OTFT device performance is clearly suggested. © *2011 American Institute of Physics*. [doi:10.1063/1.3627240]

I. INTRODUCTION

Organic thin-film transistors (OTFTs) have been intensely studied for their attractive features toward future printable electronics.[1–3] Recently, the improvement of device performance in top-contact *p*-channel organic thin-film transistors was demonstrated by contact-area-limited doping, where an electron-acceptor-doped layer was formed at the interface between a semiconductor layer and a contact electrode.[4–7] Since these molecular doping methods have been employed for controlling the electrical conductivity of organic semiconductors,[8–12] it has been commonly considered that *p*-type doping of the organic layer causes the decrease of the contact resistance and the hole injection barrier. However, it was also reported that acceptor/electrode charge transfer (without any organic/organic charge transfer) can also mimic *p*-type doping of the organic layer.[13] The origin of a series of doping effects in OTFTs is still controversial. In addition, Ishikawa *et al*. suggested with the device simulation that the origin of characteristics differences between top and bottom-contact OTFTs lies in the deficiency of charge carriers at the source-channel interface, neither in poor contact characteristics nor in poor semiconductor quality of bottom contact OTFTs.[14,15] These past studies reveal the great importance of controlling the bulk (majority) carrier concentration for realizing high-performance organic semiconductor devices.

In this work, we examined *p*-type doping for bottom-gate, bottom-contact (BGBC) OTFTs in terms of both theoretical and experimental viewpoints. A BGBC structure is suitable for forthcoming flexible-device application because of its easy fabrication on any plastic substrate with higher device densities. In order to avoid the acceptor/electrode charge transfer, high hole concentration regions (p^+) have been located a few tens of nanometers over contact electrodes, as shown in Fig. 1(a). Our device simulation results by using a Toyo University Organic Thin Film Transistor Advanced Simulator (TOTAS)[14,15] showed that even this transistor with doped layers causes the enhancement of the drain current without any change of the threshold voltage. This expectation was also experimentally confirmed by fabrication and characterization of pentacene thin-film transistors site-selectively doped with an acceptor dopant of 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F$_4$TCNQ).[16] Chemical structures of pentacene and F$_4$TCNQ molecules are shown in Fig. 1(b). In this study, the authors propose a general method for improving the performance of bottom-contact OTFTs, thereby demonstrating that the bulk carrier concentration in organic semiconductors plays a significant role in determining the performance of OTFTs.

II. DEVICE SIMULATION AND EXPERIMENTS

A. Device simulation

Current-voltage characteristics and cross-sectional distribution of potential and hole concentration in OTFTs were calculated with TOTAS, where finite difference method is employed and Poisson's equation and current continuity equation are solved by full Newton method. TOTAS is capable of simulating devices with simple contact resistance while nonlinear contact resistance such as Schottky barriers cannot be considered. The details of TOTAS are explained in Refs. 14 and 15. For TOTAS simulation in this study, extrinsic effects

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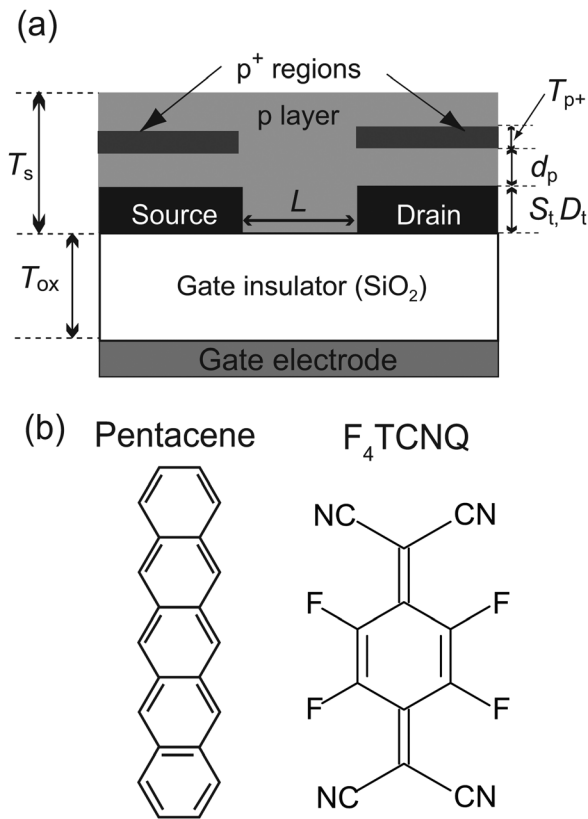
(a)

(b) Pentacene   F$_4$TCNQ

FIG. 1. (a) Schematic cross section of a bottom-gate, bottom-contact (BGBC) OTFT with p^+ regions over the source-drain electrodes. (b) Chemical structures of pentacene and F$_4$TCNQ molecules.

in device performance, such as contact resistance, charge carrier traps and interface states are not included because we aim at examining intrinsic properties of the OTFTs.

The device structure of bottom-gate, bottom-contact OTFTs examined in this work is shown in Fig. 1(a). In this model, high hole concentration regions (p^+) are prepared on top of source(S)-drain(D) electrodes. The distance between p^+ region and contact area was chosen as a parameter. Structural and physical parameters employed in this study are listed in Table I. The value of the bulk hole concentration (p) of the semiconductor layer was set to be 10^{15} cm^{-3}, which followed previous simulation studies.[14,15] The dielectric constants of gate insulator (SiO$_2$) and semiconductor (pentacene) were regarded as 3.9 and 3.0, respectively.[17,18]

B. Sample and experimental

To verify the results of device simulation experimentally, we fabricated and characterized BGBC pentacene thin-film transistors with p^+ layers as follows. Pentacene was purchased from Aldrich and twice-sublimed before device fabrication. Sublimed F$_4$TCNQ was purchased from Tokyo Kasei Kogyo Co. and used without any further purification. Heavily doped n-type silicon wafers ($<$0.02 Ω cm, size: 1.5 cm $\times$ 1.5 cm) which has a thermally grown SiO$_2$ with a nominal thickness of 300 nm, were employed as substrate. After cleaning these wafers by sonication and vapor degreasing with ethanol, a 25-nm-thick gold was deposited onto the Si wafers through a shadow mask to form S-D electrodes

TABLE I. List of physical and structural parameters employed for device simulation in this study.

L (channel length)	50 μm
G (gate electrode length)	150 μm
W (channel width)	1 mm
S,D (source and drain electrode length)	50 μm
S$_t$,D$_t$ (thickness of source and drain electrode)	25 nm
T_{ox} [thickness of gate insulator (SiO$_2$)]	300 nm
ε_{ox} [dielectric constant of gate insulator (SiO$_2$)]	3.9
μ [hole mobility of semiconductor (p) layer]	2.0×10^{-2} cm^2/Vs
T_S (thickness of p layer)	50 nm
ε_{ox} [dielectric constant of semiconductor (pentacene)]	3.0
p (impurity concentration of p layer)	10^{15} cm^{-3}
T_{p+} (thickness of p^+ region)	5 nm
p (impurity concentration of p^+ region)	10^{18} cm^{-3}
d_p (distance between p^+ region and contact electrode)	0, 10, 20 nm
Source voltage, V_S	0
Drain voltage, V_D	0 to -50 V
Gate voltage, V_G	0 to -25 V

under a vacuum of 1.0×10^{-4} Pa. The channel length (L) and width (W) were 50 μm and 1 mm, respectively.

For devices with p^+ regions, pentacene layers were deposited onto S-D contact electrodes by using the same shadow mask for electrode fabrication, followed by the deposition of a 5-nm-thick p^+ layer. This doped layer was fabricated by coevaporation of pentacene and F$_4$TCNQ under a vacuum of 4.0×10^{-5} Pa. The evaporation rates for pentacene and F$_4$TCNQ were 0.45 and 0.15 nm/min, respectively. Successively, after removal of the shadow mask in air, pentacene (50 nm) was thermally evaporated onto the substrates under a vacuum of 4.0×10^{-5} Pa. For the device without p^+ regions, active layer of pentacene (50 nm) was directly deposited onto SiO$_2$ surface with S-D electrodes. The substrate temperature was kept at room temperature through a series of fabrication process.

The surface morphology of pentacene thin films was studied by a JEOL JSPM 5200 atomic force microscope (AFM). Electrical measurements of OTFTs were conducted in a vacuum (7.0×10^{-3} Pa) with a Keithley 4200-SCS semiconductor parameter analyzer. The apparent field-effect mobility for hole (μ_h) and threshold voltage (V_T) were obtained from transfer characteristics [drain current (I_D) versus gate voltage (V_G)] in the saturation regime according to the following conventional equation:

$$I_D = WC_i\mu_h(V_G - V_T)^2/(2L), \tag{1}$$

where C_i is the gate capacitance per unit area. Here, the dielectric constant for SiO$_2$ was regarded to be 3.9 as in the device simulation.

III. RESULTS AND DISCUSSION

A. Simulation of current-voltage characteristics

Figure 2 shows calculated output characteristics of BGBC OTFTs with and without p^+ regions at gate voltages between 0 and -25 V, where the major parameters are, the impurity concentration of p layer 10^{15} cm^{-3}, the impurity
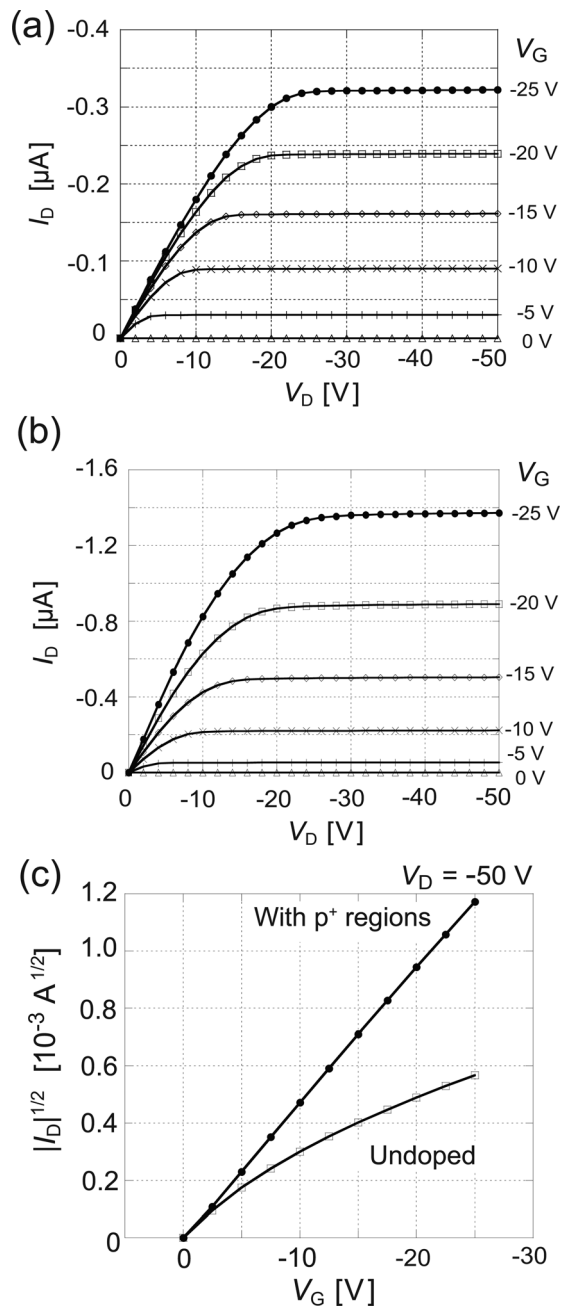
FIG. 2. Electrical characteristics of BGBC OTFTs calculated with the device simulation. (a) Output characteristics of undoped device. (b) Output characteristics of a device with p^+ regions 10 nm over the source-drain electrodes. (c) Transfer characteristics of both devices. In the figures of (a) and (b), the values of gate voltage (V_G) for each curve were indicated in these profiles. In the figure of (c), the drain voltage (V_D) was set to be -50 V. (Hole concentrations: $p = 10^{15}$ cm^{-3}, $p^+ = 10^{18}$ cm^{-3}).
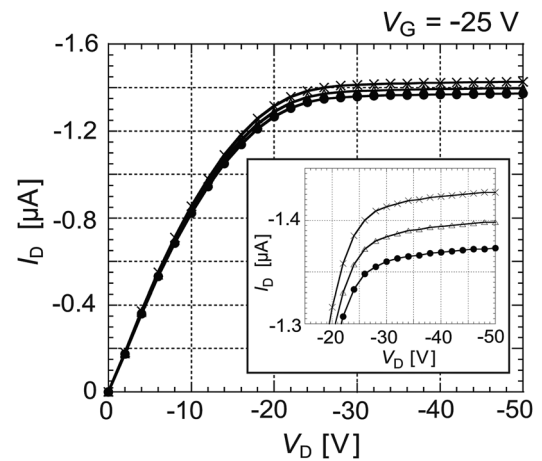

FIG. 3. Calculated output characteristics in doped OTFTs with various positions of p^+ regions. The gate voltage (V_G) was set to be -25 V. The distance between the bottom side of p^+ region and the top side of contact electrode (d_p) was 0 (cross), 10 nm (solid circle), and 20 nm (open triangle), respectively. The inset shows magnified details of the saturation regime. (Hole concentrations: $p = 10^{15}$ cm^{-3}, $p^+ = 10^{18}$ cm^{-3}.)

while a linear relation between $|I_D|^{1/2}$ and V_G is observed for the doped device. The apparent hole field-effect mobility (μ_h) with and without p^+ regions, calculated with Eq. (1), are 1.94×10^{-2} cm^2/Vs and 0.30×10^{-2} cm^2/Vs, respectively. For the device with p^+ regions, the μ_h value is almost similar to that given for the simulation in this work (2.0×10^{-2} cm^2/Vs). On the contrary, the μ_h value becomes much smaller for undoped BGBC device (0.30×10^{-2} cm^2/Vs).

A relationship between the position of p^+ region and corresponding transistor characteristics was also investigated with the device simulation. Here d_p was defined as the distance between the bottom side of p^+ regions and the top side of the contact electrode, as shown in Fig. 1(a). The other physical parameters for device simulation were the same as in the case of Fig. 2. In the calculated results presented in Fig. 3, p^+ regions directly contacting the source-drain electrode causes the maximum drain current (-1.43×10^{-6} A). In the case of $d_p = 10$ nm and 20 nm, the saturation current reach -1.37×10^{-6} A and -1.40×10^{-6} A, respectively. It seems that the drain current settles to the maximum value of -1.43×10^{-6} A with further increase of d_p. The μ_h and V_T values calculated from Eq. (1) and simulation results with different d_p are summarized in Table II.

concentration of p^+ regions 10^{18} cm^{-3} and the distance between p^+ regions and contact areas 10 nm. As shown in Figs. 2(a) and 2(b), the drain current (I_D) of the devices with and without p^+ regions at the drain voltage (V_D) of -50 V are -1.37×10^{-6} A and -0.32×10^{-6} A, respectively, at the gate voltage of -25 V. This p^+ region makes the I_D value about four times larger than that of undoped BGBC device. Transfer characteristics at $V_D = -50$ V obtained from this simulation are represented in Fig. 2(c). $|I_D|^{1/2}$–V_G plot shows a nonlinear behavior with normal BGBC device,

TABLE II. List of the apparent field-effect mobility and the threshold voltage of pentacene BGBC TFTs. Theoretical values were calculated with device simulation. Experimental values were obtained from experimental results shown in Figs. 6 and 7.

Position of p^+ layer d_p (nm)	Theoretical hole mobility [cm^2/(Vs)]	Experimental hole mobility [cm^2/(Vs)]	Theoretical threshold voltage (V)	Experimental threshold voltage (V)
Undoped	0.30×10^{-2}	0.54×10^{-2}	6.4	4.8
10	1.94×10^{-2}	1.7×10^{-2}	0	-1.3
20	1.94×10^{-2}	2.3×10^{-2}	0	-1.5

B. Simulation of potential and hole concentration

Figure 4 displays calculated cross-sectional profiles of potential and hole concentration at 1 nm above the semiconductor and gate insulator interface (transistor channel region). In Fig. 4(a), a large potential drop at the drain-channel interface, which is commonly observed for all potential profiles, is due to the formation of depletion layer (pinch-off phenomenon). At the source-channel interface, a large potential drop appears only for undoped BGBC device and can be suppressed by introducing p^+ regions on top of the contact electrodes. In the hole concentration profile shown in Fig. 4(b), the hole concentration shows the maximum value at the source-channel interface (6.0×10^{18} cm^{-3} for undoped device and 1.9×10^{19} cm^{-3} for doped devices) and decreased linearly with the distance from the source electrode. Accordingly, it is clearly indicated that the suppression of potential drop near the source electrode derives from the promotion of hole accumulation, which was theoretically suggested by previous studies with TOTAS.[14,15]

Since extrinsic effects such as contact resistance, charge carrier traps and interface states are not accounted for in TOTAS, above-mentioned device simulation suggests that the carrier supply near the source-channel interface improves the performance of BGBC OTFTs. Wang *et al.* obtained an analytical formula of contact resistance (R_c) in the bottom-contact configuration and showed that R_c is inversely proportional to the bulk carrier concentration of a semiconductor film, suggesting that the carrier doping above contact electrodes can reduce R_c.[19] The validity of our device simulation is also supported by this previous work, although the concept of contact resistance has not been introduced in the device simulation.

C. Experimental results of BGBC pentacene TFTs with p^+ regions

In the former part of this study, the device simulation proposes that the doped layers directly on top of contact electrodes should give rise to the best performance of BGBC OTFTs. However, in that case, there are some possibilities for acceptor molecules to be adsorbed onto metal electrodes. It is quite difficult to distinguish donor/acceptor charge transfer and acceptor/metal charge transfer for discussing p-type doping effect in this study. In order to circumvent this difficulty, we prepared BGBC pentacene transistors with p^+ regions at $d_p = 10$ and 20 nm. The film structures for all the specimens employed in this study were almost identical, and we saw many small granular grains, as shown in Fig. 5. So
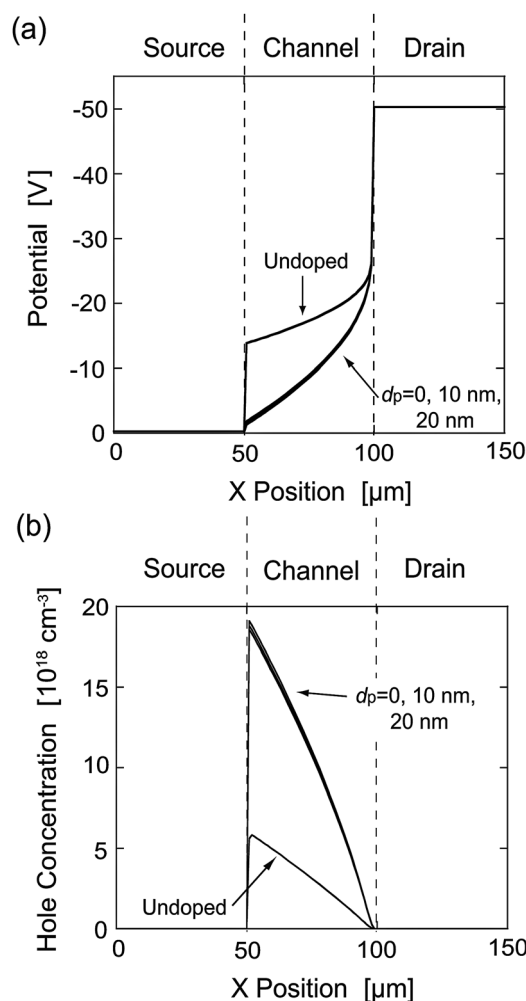

FIG. 4. Calculated cross-sectional profiles of (a) potential and (b) hole concentration at 1 nm above the semiconductor and gate insulator interface (transistor channel region) of BGBC OTFTs with p^+ regions. The values of V_D and V_G were set to be -50 and -25 V, respectively. (Hole concentrations: $p = 10^{15}$ cm^{-3}, $p^+ = 10^{18}$ cm^{-3}.)

we assumed that there was almost no difference in hole mobility inside the semiconductor films.

Figure 6 shows output characteristics of the pentacene BGBC TFTs with and without p^+ regions. All the devices fabricated in this work display clear p-channel operation. The drain current at $V_D = -50$ V and $V_G = -25$ V was improved from -0.47×10^{-6} A up to -1.09×10^{-6} A ($d_p = 10$ nm) and -1.16×10^{-6} A ($d_p = 20$ nm) by inserting p^+ layers into transistors. Next, transfer characteristics of the pentacene BGBC TFTs are indicated in Fig. 7. Because typical injection-type hysteresis curves appeared due to hole trapping on
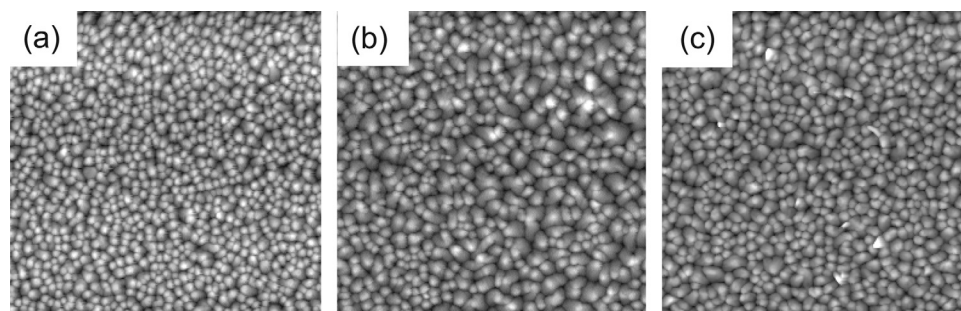

FIG. 5. AFM images of the surfaces over the channel region of pentacene BGBC TFTs: (a) an undoped device, (b) a device with p^+ regions at $d_p = 10$ nm, and (c) a device with p^+ regions at $d_p = 20$ nm (scanning area: 3.5 μm $\times$ 3.5 μm).
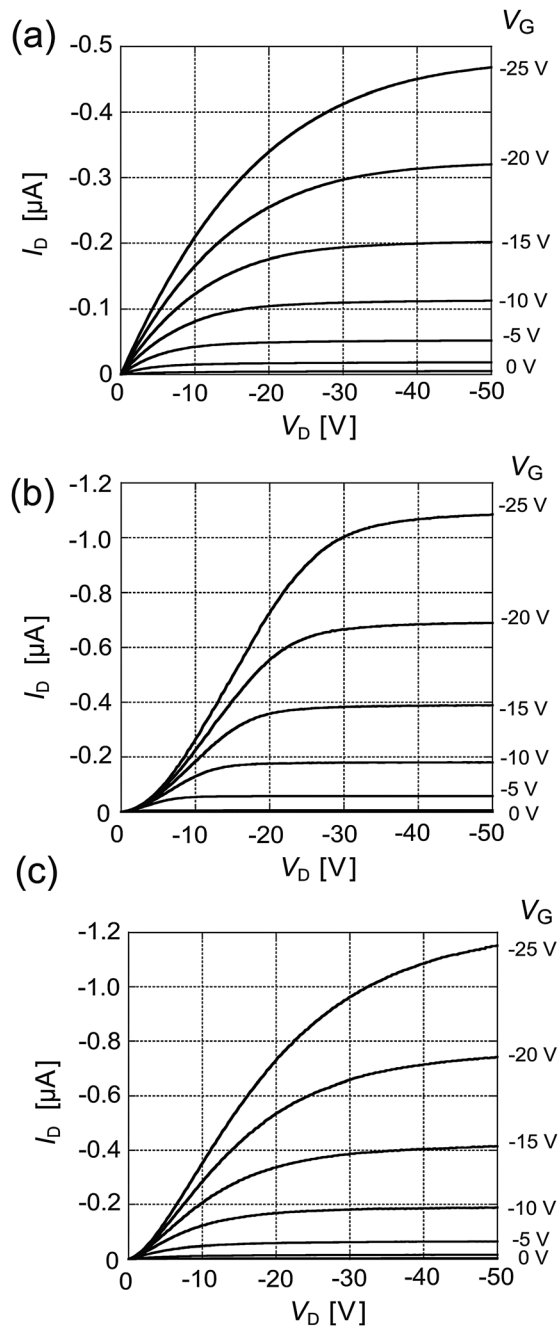
FIG. 6. Experimental output characteristics of pentacene BGBC TFTs: (a) the undoped device, (b) the device with p^+ regions at $d_p = 10$ nm, and (c) the device with p^+ regions at $d_p = 20$ nm. The values of gate voltage (V_G) for each curve were indicated in these profiles.
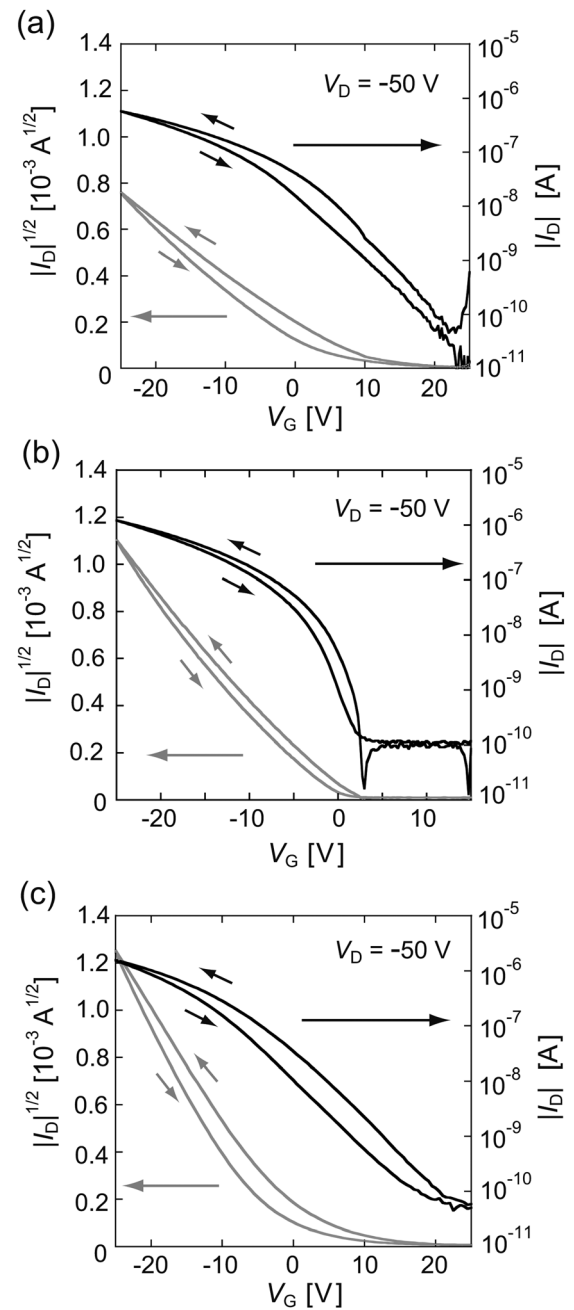

FIG. 7. Experimental transfer characteristics of pentacene BGBC TFTs without and with p^+ regions over the source-drain electrodes: (a) the undoped device, (b) the device with p^+ regions at $d_p = 10$ nm, and (c) the device with p^+ regions at $d_p = 20$ nm.

(or inside) SiO_2 insulators, the apparent field-effect mobility and the threshold voltage were obtained from the gate-sweep curves with the increase of $-V_G$. The experimental values of μ_h and V_T based on Eq. (1) are summarized in Table II.

The low field-effect mobility for pentacene TFTs, which ranges from 10^{-3} to 10^{-2} cm^2/Vs in Table II, is probably due to the film structure with small granular grains as shown in Fig. 5. The condition of pentacene film deposition was not completely optimized in this study. It is well known that the surface passivation of oxide gate insulators and higher substrate temperatures during film deposition can promote the larger grain growth of pentacene, resulting in the increase of carrier mobility.[20]

There appears to be some differences between theoretical and experimental values of mobility and threshold voltages in Table II, suggesting extrinsic effects of carrier traps and interfacial states in realistic OTFTs.[20] For instance, field-effect mobility is greatly influenced by gate-biasing and the existence of shallow carrier traps in the channel region. Threshold voltage also mainly depends on interfacial states on gate insulators.

Despite the aforementioned discussion, these experimental data are qualitatively consistent with the results of the device simulation. Accordingly, the molecular doping effects observed in this study reflect intrinsic properties of

OTFTs. Additionally, F_4TCNQ molecules worked for increasing the hole concentration due to donor-acceptor charge transfer, not for lowering the energy barrier for hole injection at contact electrodes. If we assume the hole concentration of undoped (p) layer as $\sim 10^{15}$ cm^{-3}, the hole concentration in p^+ regions can be roughly estimated to be 10^{17} -10^{18} cm^{-3} in comparison with drain currents in the saturation regime for both the device simulation and the experimental results, which coincides well with a value of the hole concentration (2×10^{17} cm^{-3}) obtained from our preliminary Hall effect measurement.

So far molecular p-type doping on top of the existing channel in OTFTs has already been reported, where p-type doping causes the positive shift of threshold voltage owing to the increase of hole concentration in the channel region.[21] However, no threshold-voltage shift in positive direction was observed for our transistors with p^+ regions. This means that precise doping on top of contact electrodes does not cause the threshold-voltage shift, which can be also inferred from the device simulation results. For further progress in device fabrication with reliable molecular doping techniques, quantitatively precise control of dopant concentration should be established. Actually, some discrepancies in the trend for theoretical and experimental values of μ_h and V_T with different d_p are observed in Table II, which is possibly caused by slight deviation of dopant concentration in p^+ layer for each device.

In the experimental output characteristics of BGBC OTFTs (Fig. 6), parasitic contact series resistance appears, which is very common in realistic OTFTs. Extraction of intrinsic carrier mobilities was attempted according to the procedures described elsewhere,[22,23] however reasonable data on intrinsic mobility could not be attained probably due to the existence of Schottky energy barriers indicated by the nonlinearity of I_D-V_D curve[24] as shown in Fig. 6. Trials for removal of these parasitic contact resistance effects by sophisticating device fabrication processes are going on for achieving more exact expectation of OTFT characteristics with TOTAS.

Thus, this study presents a versatile method for enhancing the drain current with keeping the threshold voltage in high-performance bottom-contact OTFTs. Device design based on precise control of carrier concentration in organic semiconductors should be a quite important subject for developing practical application of OTFTs.

IV. CONCLUSION

The bottom-gate, bottom-contact (BGBC) configuration with carrier-doped regions over contact electrodes was examined for the purpose of presenting a new strategy for realizing high-performance OTFTs. Device simulation results demonstrate that the heavily doped layers (p^+) on top of the source-drain contact region can compensate the deficiency of charge carriers at the source-channel interface during transistor operation, leading to the increase of the drain current and the apparent field-effect mobility. The phenomena expected with the device simulation were experimentally confirmed in typical BGBC pentacene thin-film transistors by using F_4TCNQ as an acceptor dopant. Since no positive shift of threshold voltage was observed, p^+ layers were

formed precisely on top of the source-drain regions. Considering that even p^+ layers with a thickness of a few tens of nanometers over the source-drain electrodes can enhance the transistor characteristics, we concluded that acceptor molecules in our doped devices worked for increasing the hole concentration, not for lowering the energy barrier for hole injection at contact electrodes. The results shown here suggest that common inferior characteristics of bottom-contact OTFT devices mainly derive from the supply shortage of charge carriers to the channel region, not from the charge injection barrier at metal-semiconductor contacts. The necessity of establishment of reliable carrier doping or heavily doped semiconductor materials for improving OTFT device performance is clearly denoted.

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