

Area-Effective Inductive Peaking with Interwoven Inductor for High-Speed Laser-Diode Driver for Optical Communication System

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SUMMARY This paper presents an area-effective bandwidth enhancement technique using interwoven inductors. Inductive peaking is a common practice for bandwidth enhancement, however the area overhead of inductors is a serious issue. We implement six or four inductors into an interwoven inductor. Furthermore parasitics of the inductors can be reduced. The proposed inductor is applied to a laser-diode driver in a 0.18 μm CMOS. Compared to conventional shunt-peaking, the proposed circuit achieves 1.6 times faster operation and 60% reduction in power consumption under the condition for the same amount of data transmission and the LD driving current. The interwoven inductor can reduce the circuit area by 26%. Parasitic capacitance in interwoven inductor is discussed. Simulation results reveal that line-to-line capacitance is a significant factor on bandwidth degradation.

key words: interwoven inductor, LD driver, optical communication

1. Introduction

Increasing demand for over-10 Gb/s optical communication systems strongly activates intensive study for high-speed and low-power laser-diode (LD) driver circuits for high-performance yet economical optical transmitters [1], [2]. An off-chip laser-diode usually requires higher supply voltage over 1.8 V. Therefore an LD driver is also required to operate at this relatively high supply voltage. In order to guarantee higher breakdown voltage, transistors with thicker oxide thickness are necessary, which prevents to rely on process scaling for speed improvement. We thereby need to design an efficient circuit in a moderate process such as 0.18 μm CMOS for higher transmission speed. Besides the need for speed improvement, there is also a strong demand for lower power dissipation. At present, an LD driver is a major source of power-dissipating components which consumes more than half of the whole optical communication system. A power-efficient LD driver is a great help for the

success of Green ICT.

An effective method for improving speed performance is inductive peaking. There are many peaking techniques proposed so far [1]–[4]. For example, Ref. [3] propose cascaded amplifiers with asymmetric transformer peaking and achieves a 70 GHz bandwidth in 0.13 μm CMOS. It however requires several dozen of on-chip spiral inductors that consume large silicon area accordingly. It is desirable to design a circuit in an area as small as possible.

In this paper, we propose a power and area efficient LD driver circuit with interwoven mutually coupled inductors. We interweave six mutually coupled inductors into an area corresponds to a single inductor which greatly save silicon area while keeping strong peaking performance. Interwoven inductor can reduce the occupied area and utilize the mutual inductances, on the other hand, parasitic capacitance becomes large since number of inductors are integrated in a small area. A preliminary work was already presented [5], however Ref. [5] did not discuss the parasitics. Still the impact of parasitic capacitances and how to design interwoven inductor are not clear. This paper discusses the parasitic capacitances in interwoven inductor. Simulation results show that line-to-line capacitances have significant impact on the bandwidth. Together with other circuit techniques for speed improvement and power reduction such as a cascaded pre-driver circuit and an output driver with active-back termination [1], the proposed circuit in a 0.18 μm CMOS performs 16 Gb/s operation with 80 mA modulation current in 211 mW power dissipation at 1.8 V power supply. Compared to the LD driver reported previously [1], the power dissipation index, which is defined by power dissipation normalized by transmission speed and modulation current, of the proposed LD driver is 60% improved in more than 26% smaller area.

The reminder of this paper is organized as follows. In Sect. 2, the structure of the interwoven inductor is explained, and in Sect. 3, the proposed LD driver with interwoven inductors is explained in details. The circuit performance is compared with a conventional shut-peaking circuit without interwoven inductors, and the effectiveness of the proposed approach with respect to operating speed and chip area is demonstrated by simulation. The proposed circuit, together with the shunt-peaking circuit, has been fabricated in a 0.18 μm process. The measured result and comparison with other circuits in literature are explained in Sect. 4. Finally, Sect. 5 concludes the discussion.

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2. Interwoven Inductor for Area Effective Inductive Peaking

This section introduces interwoven inductor for inductive peaking. Figure 1 shows a structure of interwoven inductor. The wire of interwoven inductor branches at a certain point, thus interwoven inductor can realize mutually coupled inductors in small area. In the case of Fig. 1, the structure has six ports and six inductors as shown in Fig. 2.

Interwoven inductor shown in Fig. 1 contains six intrinsic inductors with six components of mutual coupling. Advantages of the interwoven inductor are summarized as follows.

- The area is much smaller than the design that uses individual spiral inductors.

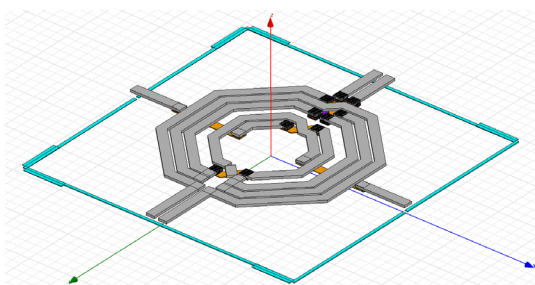


Fig. 1 An example structure of the interwoven inductor.

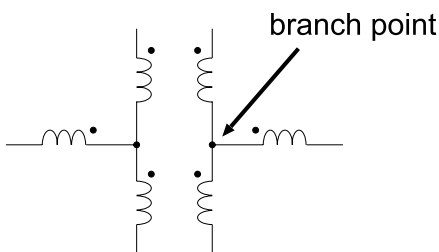


Fig. 2 An example schematic of the interwoven inductor.

- All the inductors are mutually coupled. The amount of coupling coefficient can be adjusted by relative position, the number of turns and the amount of interleaving of each inductor.
- Layout parasitics associated with interconnection to inductors are minimized.
- It is well suited to differential circuit that a set of inductors can be interwoven into a single differential inductor.

However, interwoven inductor has disadvantages, as follows.

- The design is difficult because of its structure is complex.
- However parasitics is smaller than individual spiral inductors, parasitic capacitance of line-to-line may increase and degrade the bandwidth of circuits. Because each wireline of interwoven inductor is very close.

In this paper, we analyze the parasitic capacitance of interwoven inductor and show design course of the interwoven inductor. We discuss specific influence by the parasitic capacitance of interwoven inductor in Sect. 3.

3. LD Driver with the Proposed Interwoven Inductors

In this section, we show the proposed LD driver with interwoven inductors and design of interwoven inductor.

3.1 Proposed LD Driver

Figure 3 shows the schematic of the proposed circuit. The LD driver should drive a large modulation current of 80 mA. In order to supply large modulation current of 80 mA at the output while reducing the power dissipated inside the circuit, we have adopted a three-stage configuration with tapering ratio of two and active back-termination at the output stage [1]. A cascode configuration is adopted for all the stages to reduce the capacitive loading of Miller effect. Inductive peaking with interwoven inductors is applied for

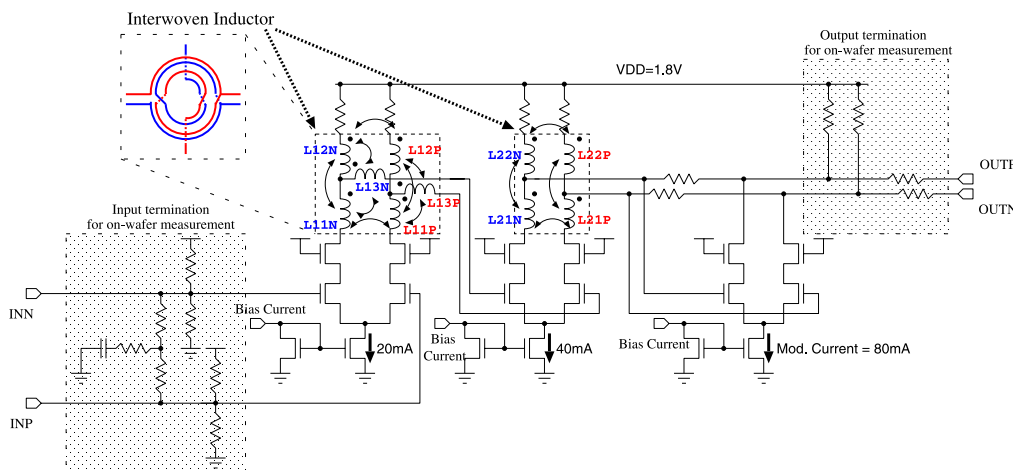


Fig. 3 Schematic of the proposed laser-diode driver.

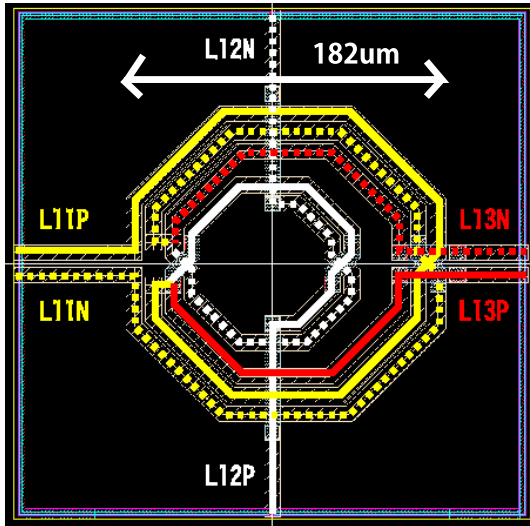


Fig. 4 Interwoven inductor in the 1st stage amplifier.

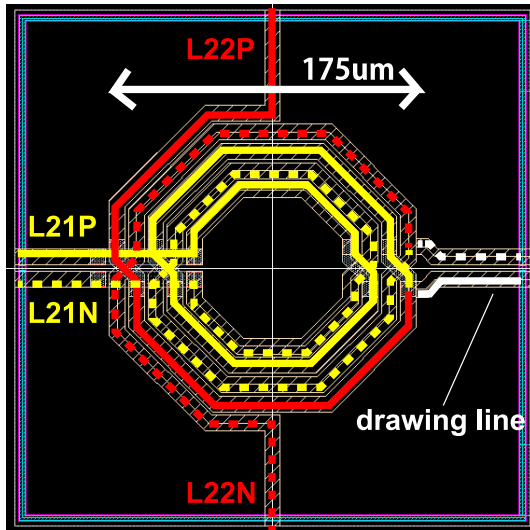


Fig. 5 Interwoven inductor in the 2nd stage amplifier.

bandwidth enhancement in an area-efficient manner. The peaking structure at the first stage is based on a shunt-and-double-series peaking [6], and the second stage employs an asymmetric T-coil peaking [3], [7], [8]. We have extended the shunt-and-double-series peaking to include mutual coupling among the three inductors. Those mutual inductance introduce additional freedom in the tuning of frequency characteristics as well as an area-effective implementation of three inductors as a single interwoven inductor. Differential configuration further enables us to realize a set of differential inductors onto the same space. Thus, we can interweave six inductors at the first stage onto an area equivalent to a single inductor. Figure 4 shows the first stage interwoven inductor. Also, four inductors at the second stage can be interwoven into one, as shown in Fig. 5. We therefore realize the circuit with two interwoven inductors, whereas we need 10 inductors if we do not introduce mutual coupling.

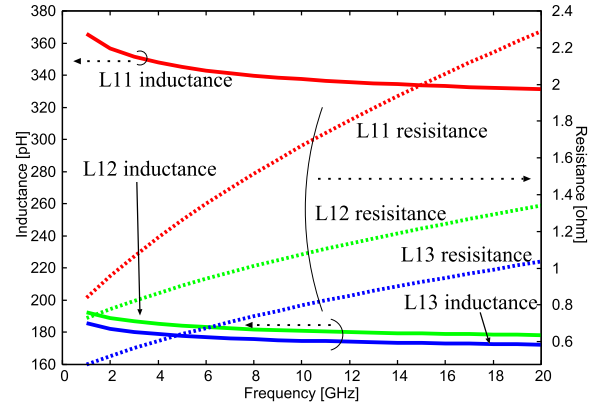


Fig. 6 Frequency characteristic of inductance and resistance in the 1st stage interwoven inductor.

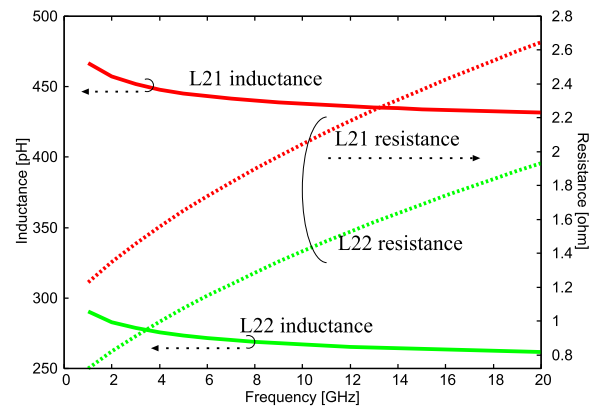


Fig. 7 Frequency characteristic of inductance and resistance in the 2nd stage interwoven inductor.

The line width of these interwoven inductors in Figs. 4 and 5 is $9\ \mu\text{m}$ to satisfy the current density rule. The diameter of Figs. 4 and 5 is $182\ \mu\text{m}$ and $175\ \mu\text{m}$ respectively. In Fig. 4, the inductors L12P and L12N are shifted from the center of the other inductors to minimize the unnecessary interconnect from branch point. Figures 6 and 7 show the frequency characteristic of inductance and resistance of interwoven inductors.

Direct benefit of reducing the number of inductors is chip-size reduction. An inductor occupies much larger area than transistors and hence total chip area is almost proportional to the number of inductors. Besides the area efficiency, inductor reduction also helps to decrease the amount of parasitics associated with a routing wire that connects a transistor and an inductor, which also helps to maintain higher cutoff frequency than otherwise.

3.2 Design of Interwoven Inductors

3.2.1 Ground Capacitance and Line-to-Line Capacitance within Interwoven Structure

Interwoven inductor can include several inductance and contribute area-efficiency. However, capacitance within inter-

Table 1 The ground capacitance and the line-to-line capacitance of the first stage interwoven inductor.

	L11P	L11N	L12P	L12N	L13P	L13N
L11P	14.5 fF					
L11N	58.5 fF	14.9 fF				
L12P	6.15 fF	8.28 fF	8.23 fF			
L12N	8.13 fF	6.06 fF	28.7 fF	8.32 fF		
L13P	22.8 fF	9.29 fF	5.86 fF	6.85 fF	6.4 fF3	
L13N	5.56 fF	26.5 fF	6.95 fF	5.93 fF	5.21 fF	6.34 fF

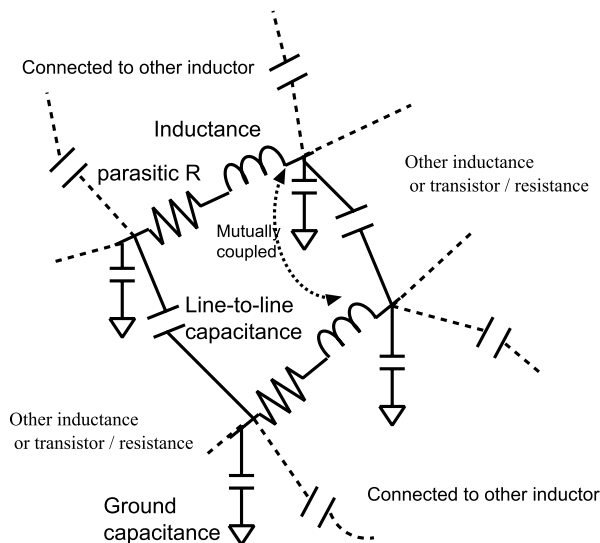


Fig. 8 Parasitic model of interwoven inductor.

woven inductor may degrade the circuit performance, because interwoven inductor have long wireline and each wireline is very close. Table 1 shows the capacitance matrix of the first stage interwoven inductor. There are slight differences in the differential pairs, i.e. L11P-L11N, L12P-L12N and L13P-L13N. The interwoven inductor are designed symmetrically however the structure is not completely symmetry because of the undercross of the line. From Table 1, the line-to-line capacitance between L11P and L11N is the largest in the first inductor. Moreover the line-to-line capacitance influence the operation speed because of Miller effect. Figure 9 shows the impact of the capacitances. Figure 9 compares a circuit without any capacitance in interwoven inductor, a circuit with only ground capacitances (the diagonal elements in Table 1), a circuit with only line-to-line capacitances (the off-diagonal elements in Table 1) and a circuit with all capacitances. In Fig. 9, interwoven inductors are modeled as π -type RLC network as shown in Fig. 8 analyzed by a 3D electro-magnetic analyzer. From Fig. 9, the impact of the ground capacitances is negligible compared to that of the line-to-line capacitances. The line-to-line capacitance between L11P and L11N is the dominant factor. The capacitance value is the largest (58.5 fF) and its impact is doubled by Miller effect. Therefore reducing the line-to-line capacitances is important for design of interwoven inductor.

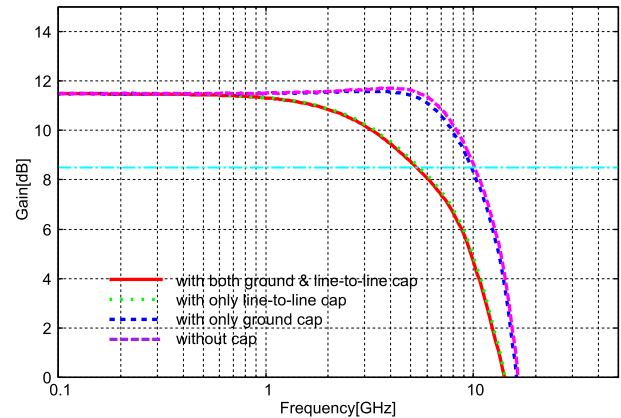


Fig. 9 Comparison with bandwidth degradation by line-to-line vs. ground cap.

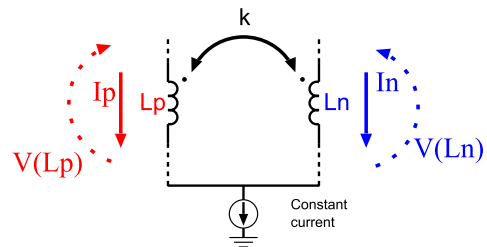


Fig. 10 Interwoven inductor in differential pair.

3.2.2 Mutual Inductance and Line-to-Line Capacitance

We here discuss relationship between mutual inductance and line-to-line capacitance. The mutual inductance between differential pair affects the effective inductance. Figure 10 shows the effect of mutual coupling between differential inductance pair. In Fig. 10, we can express the voltage of inductance as follows,

$$V(L_p) = L_p \frac{dI_p}{dt} - M \frac{dI_n}{dt}, \quad (1)$$

$$V(L_n) = L_n \frac{dI_n}{dt} - M \frac{dI_p}{dt}. \quad (2)$$

Here, $M = k \sqrt{L_p L_n}$. In differential system, differential current can be expressed as follows, $dI_p/dt = -dI_n/dt$. Equations (1) and (2) can be transformed as follows,

$$V(L_p) = (L_p + M) \frac{dI_p}{dt}, \quad (3)$$

$$V(L_n) = (L_n + M) \frac{dI_n}{dt}. \quad (4)$$

If coupling coefficient k is positive, the mutual inductance M becomes positive. In this case, we can regard $L_p + M$ and $L_n + M$ as effective inductances and we can realize larger inductance than intrinsic inductances L_p and L_n . In other word, we can obtain stronger peaking effect by smaller intrinsic inductance. Thus the mutual inductance helps to save the silicon area.

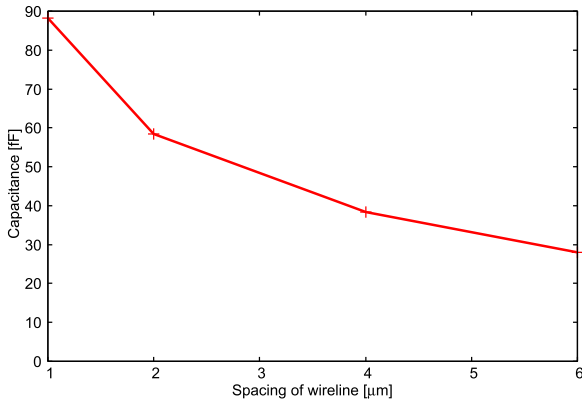


Fig. 11 Line-to-line capacitance of L11P and L11N.

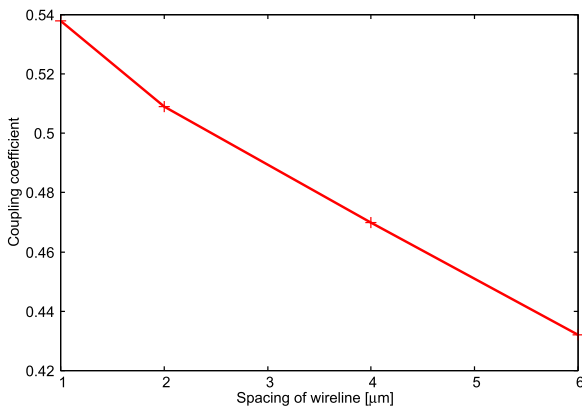


Fig. 12 Mutual coefficient and spacing between L11P and L11N.

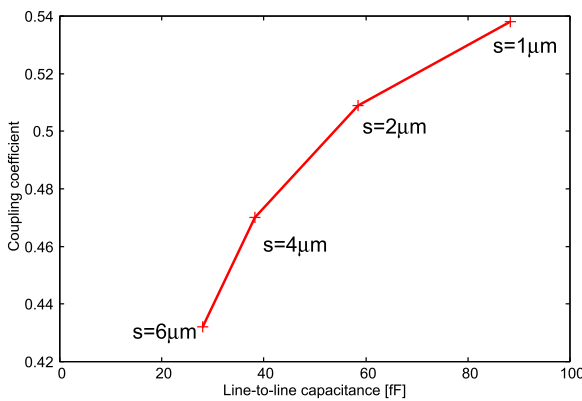


Fig. 13 Mutual coefficient and line-to-line capacitance of L11P and L11N.

However mutual inductance strongly depends on the spacing between wires as well as the line-to-line capacitance. As the spacing becomes larger, both capacitance and inductance become smaller. We analyzed the interwoven inductor by a 3D electro-magnetic analyzer. In this analysis, the radius and the number of turns are fixed. Thus the sum of wireline width and spacing is constant. From this assumption, the self-inductances of interwoven inductor are almost constant. Figure 11 shows line-to-line capacitance

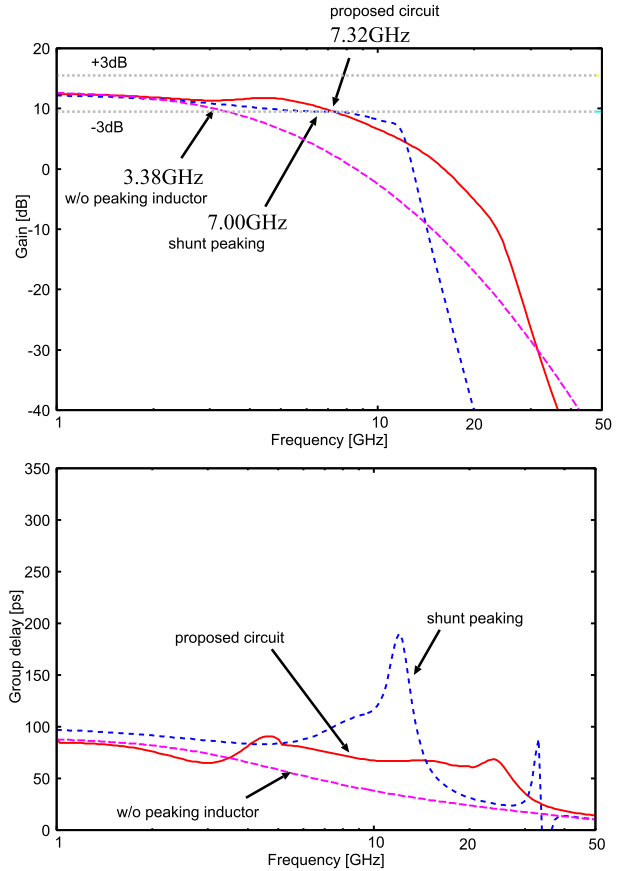


Fig. 14 Simulated gain curve and group delay.

and ground capacitance of L11P and L11N. Here, we deal L11P and L11N as the same value because of their symmetry. Roughly speaking, line-to-line capacitance is inversely proportional to wireline spacing. Figure 12 shows coupling coefficient and wireline spacing between L11P and L11N. On the other hand, the coupling coefficient changes linearly. From Figs. 11 and 12, we shows the trade-off between line-to-line capacitance and mutual coefficient in Fig. 13. As shown in Fig. 11, the line-to-line capacitance changes rapidly when the spacing is small. However as the spacing becomes larger, the change of the capacitance becomes smaller. On the other hand, the coupling coefficient changes linearly against the spacing. Figure 13 shows the relationship between the line-to-line capacitance and the coupling coefficient. The curve is convex upward. This means when the spacing is small, we can reduce capacitance effectively with small sacrifice of coupling coefficient by increasing the spacing. Considering this trade-off, 2 μm spacing is employed.

3.3 Comparison with Conventional Shunt-peaking Driver

In order to evaluate the performance of the proposed circuit, we have designed the proposed circuit, a circuit without inductive peaking, and a circuit with shunt-peaking with the same supply current in a 0.18 μm CMOS process. In all cir-

circuits, the size of transistors and resistance value are the same and only the peaking part is changed. The proposed and these two circuits are all laid out and frequency characteristics are simulated based on extracted circuits from their lay-

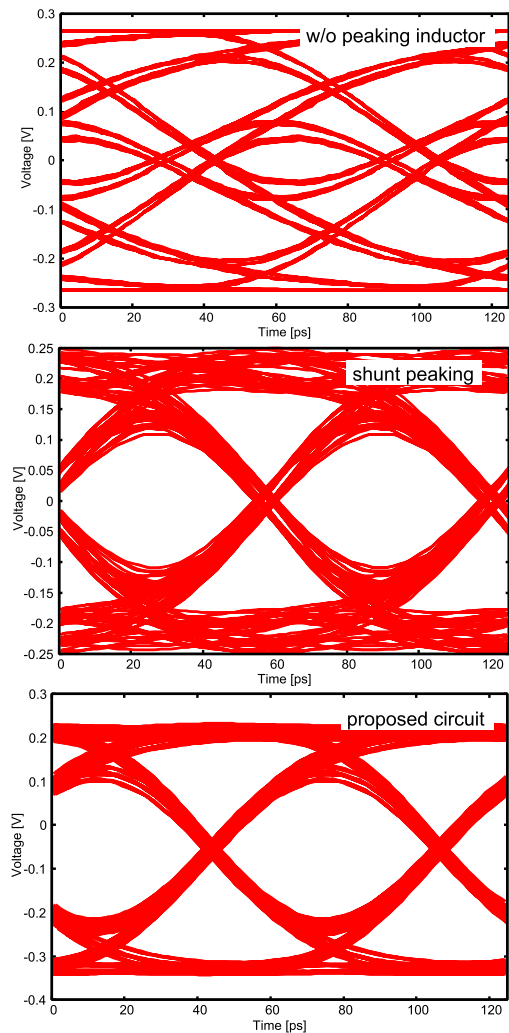


Fig. 15 Simulated eye-diagram of the proposed circuit and the circuit with shunt peaking at 16 Gb/s.

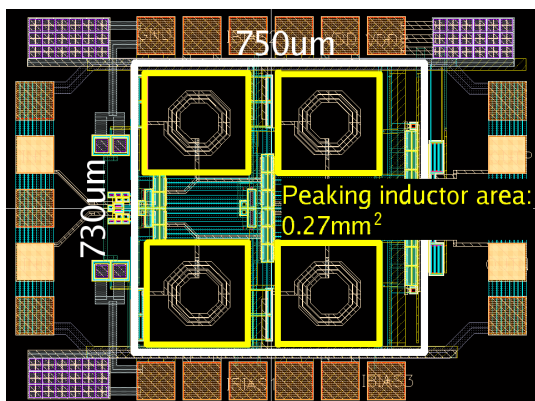


Fig. 16 Layout of a conventional shunt-peaking LD driver.

outs. A 2.5D field solver [9] is used to derive S-parameters of the interwoven inductors as well as shunt inductors from their layout. Those numerically derived S-parameters are used in the simulation.

Figure 14 shows the simulated gain and group delay characteristics of the three circuits. The -3 dB bandwidth of the proposed circuit is 7.3 GHz which is 2.2 times higher than that of the non-peaking driver. The shunt peaking circuit has designed to have a similar -3 dB bandwidth of 7.0 GHz. The group delay characteristics of the shunt peaking circuit, however, has a steep peak around 11 GHz which may introduce jitters, whereas those of the proposed circuit are rather smooth.

The effect of better frequency and group-delay characteristics can be clearly seen in the simulation of eye-diagram. Figure 15 shows simulated eye-diagrams of the three circuits at 16 Gb/s. There is no eye-openings in the non-peaking circuit. The proposed circuit gives the best eye-opening. The shunt-peaking circuit exhibits a larger jitter than the proposed circuit as expected from Fig. 14. Moreover, the shunt-peaking circuit occupies large circuit area of 0.55 mm² due to four individual inductors as shown in Fig. 16.

4. Measurement Results

We have fabricated the proposed circuit and a non-peaking circuit in a 0.18 μm CMOS process. Figure 17 shows a chip micrograph of the proposed circuit. We evaluated eye-diagrams by on-wafer measurement. The input signal is 2³¹ - 1 PRBS whose bitrate is 16 Gb/s and voltage swing is 0.55 V-0.75 V peak-to-peak. Figure 18 and Fig. 19 shows the measured eye-diagram of the circuit without inductive peaking and the proposed circuit, respectively. The eye-opening of the proposed circuit is 280 mV and the jitter is 14.2 ps. In order to evaluate power efficiency of LD drivers with different modulation current and different data rate, we define the power dissipation index which indicates effective power dissipation normalized by data rate and modulation

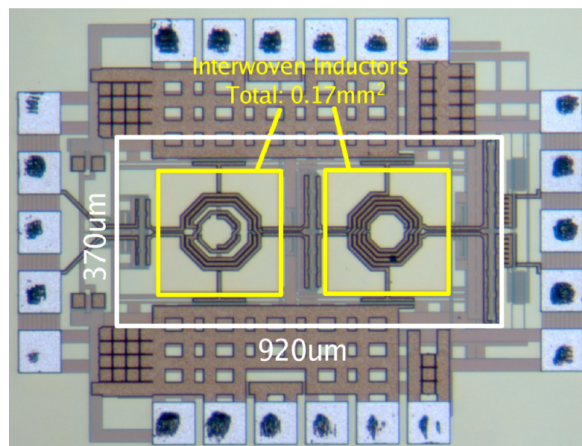


Fig. 17 Chip micrograph of the proposed LD driver.

current as follows,

$$\frac{\text{LD power dissipation}}{\text{Data Rate} \times \text{Modulation Current}} \quad (5)$$

The performance summary and the comparison with

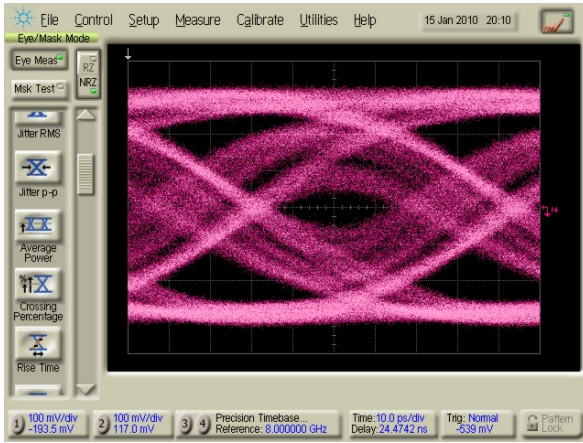


Fig. 18 Measured eye-diagram of LDD without peaking inductors at 16 Gb/s (Horz: 10 ps/div, Vert: 100 mV/div).

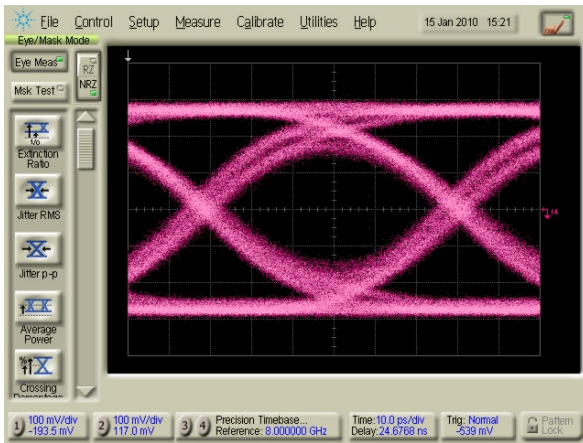


Fig. 19 Measured eye-diagram of the proposed circuit at 16 Gb/s (Horz: 10 ps/div, Vert: 100 mV/div).

other designs are shown in Table 2. Compared to 10 Gb/s LD driver in Ref. [1], the proposed design reduces the area by 26% and larger modulation current and lower power dissipation. Reference [1] also employed active back termination. However the circuit in Ref. [1] uses additional circuit and the additional circuit consumes several tens mA. On the other hand, the active back termination in the proposed circuit is implemented by resistors. Thus the proposed circuit can reduce the power consumption compared to Ref. [1]. Reference [2] achieves higher modulation current, however the area becomes 4.8 times larger and the power dissipation increases by 70%. From the discussion above, the proposed interwoven inductor realize both bandwidth enhancement and smaller area. We verified the interwoven inductor can be combined with other circuit techniques and the proposed circuit achieves cost-effective implementation of LD driver.

5. Conclusion

In this paper, a LD driver design with interwoven peaking inductors is proposed. The proposed interwoven inductor realized small area and the proposed LD driver realize 38% smaller area compared with a conventional shunt-peaking layout. The interwoven inductor is suitable for peaking of operation speed enhancement in a differential amplifier. The performance is verified in a 0.18-μm CMOS and the proposed design achieves 16 Gb/s operation. Compared to the conventional LD drivers in 0.18-μm CMOS, the proposed design achieves 1.6 times higher operating speed and 26% smaller area. To evaluate power efficiency of LD drivers, we defined a power dissipation index and verified the proposed LD driver is over 60% efficient than conventional LD drivers in power dissipation index. Therefore the proposed inductor effective to realize a cost- and area-effective design of a high-speed differential circuit. Parasitic capacitance in interwoven inductor is discussed. Simulation results reveal that line-to-line capacitance is a dominant factor on bandwidth degradation.

Table 2 Design summary and comparison with other designs.

	This work†	shunt peaking‡	w/o peaking inductor‡	[1]	[2]
Technology	0.18 μm CMOS				
Supply Voltage	1.8 V				
Area	0.34 mm ²	0.55 mm ²	0.15 mm ²	0.46 mm ²	1.62 mm ²
Data Rate	16 Gb/s	16 Gb/s	7.4 Gb/s	10 Gb/s	10 Gb/s
Jitter (pp)	14.2 ps	—	—	13 ps	N/A
Rise/Fall	60.4 ps / 64.0 ps	— / —	— / —	38 ps / 38 ps	N/A
Power	211 mW	—	—	240 mW	360 mW
Mod. Current	80 mA	80 mA	80 mA	60 mA	>100 mA
Power Dissipation Index	0.16	0.16	0.36	0.40	0.36
Technique	T-coil peaking Cascode Active-back term. Interwoven inductors	shunt peaking Cascode Active-back term.	Cascode Active-back term.	shunt peaking Active-back term.	T-coil peaking Active-feedback term. Negative Capacitance

† A proposed circuit was evaluated by electrical measurement.

‡ evaluated by transistor level simulation.

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