Effects of Neutron-Induced Well Potential Perturbation for Multiple Cell Upset of Flip-Flops in 65 nm

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***Abstract*—We measure and investigate the relationship between well potential perturbation and MCUs (Multiple Cell Upsets) by neutron irradiation. Area-efficient cell-based perturbation detectors are placed adjacent to FFs (Flip-Flops). They can measure duration time of perturbation with 5 μm spatial resolution at two voltage levels. The measurement results by neutron irradiation on a 65-nm bulk CMOS show that 95% of MCUs occur simultaneously with well-potential perturbation, while there is very weak relationship between SEUs (Single Event Upsets) and the perturbation.**

***Index Terms*—Multiple Cell Upset, soft-error, neutron irradiation, sensor, parasitic bipolar effect.**

I. Introduction

As a result of process scaling, MCU is becoming one of the most significant issues for LSI (Large Scale Integration) reliability since it can flip several stored values on SRAMs (Static Random Access Memories) and cannot be recovered by ECC (Error Correction Code) [1]. In a 65-nm process, MCUs are observed in FFs and increase soft-error rates of radiation-hardened FFs such as multiple modular redundancy [2], [3]. SEMTs (Single Event Multiple Transients) are also reported by neutron and heavy-ion experiments [4], [5]. In a future advanced process, it is impossible to improve soft-error resilience of flip-flops without considering such multiple errors.

The parasitic bipolar effect is considered as a source of multiple errors. It is caused by well-potential perturbation due to a particle hit [6], [7]. Since well-potential perturbation is strongly affected by well-contact density [8], MCU rates also depend on the distance from well-contacts [9], the angle of particle [10], [11] and back bias [6]. Ref. [12] also shows parasitic bipolar effect increases widths of SET (Single Event Transient) pulses. Parasitic bipolar and well-potential perturbation are significant phenomena that cause single and multiple errors. For estimating soft error rate from circuit-level simulations and improving soft-error resilience, it is necessary to measure well-potential perturbation caused by a particle hit and evaluate relationship between well-potential perturbation and soft errors. However, no one shows measurement results of well-potential perturbation caused by a particle hit. Only simulation results are reported in [7], [8], [11].

In this paper, we show actual measurement results of well-potential perturbation by neutron irradiation using well-potential perturbation detectors based on [13]. We also show the relationship between well-potential perturbations and MCU occurrences on FFs. Test structures are fabricated in a 65-nm bulk CMOS process and they can measure duration time of perturbation with 5 μm spatial resolution at two voltage levels. Accelerated tests were carried out by the spallation neutron beam at RCNP (Research Center for Nuclear Physics, Osaka University).

This paper is organized as follows. Section II explains the test circuit structure in detail. Section III shows our neutron-beam experimental setups in RCNP, followed by Section IV which discusses experimental results. Section V concludes this paper.

II. Test Circuit Structure

Fig. 1 shows unit circuits of the well-potential perturbation detector [13]. They consist of AND / OR chains and two time-to-digital converters (TDCs) based on the ring oscillator [14]. An input port of each logic gate is connected to the P-well or N-well through an inverter. If a particle hit on a chip and well-potential is elevated over the threshold voltage, the inverter is flipped until well-potential goes back to less than the threshold voltage. Therefore, well-potential perturbation is converted to a rectangular pulse by the inverter and it propagates through the logic chain. Finally, the TDC detects well-potential perturbation and measures its duration. The measurable voltage level of the proposed circuit is determined by the threshold voltage of the inverter, which can be easily changed by skewing transistor sizes of inverters.

Fig. 2 shows a block diagram of the fabricated test circuit. The purposes of this test circuit are as follows.

- To measure the relationship between well-potential perturbation and MCUs on FFs.
- To reveal that SEU on FFs can be detected by measuring well-potential perturbation. If SEU is strongly correlated, it can be detected by proposed circuit and built-in current sensors [15].
- To obtain the characteristics of well-potential perturbation caused by a neutron strike such as dependence of the well-contact distance.

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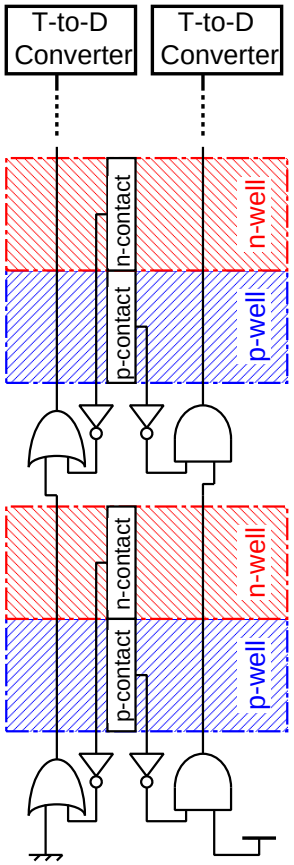

Fig. 1. Well-Potential perturbation detector composed of AND chain, OR chain and two T-to-D converters.

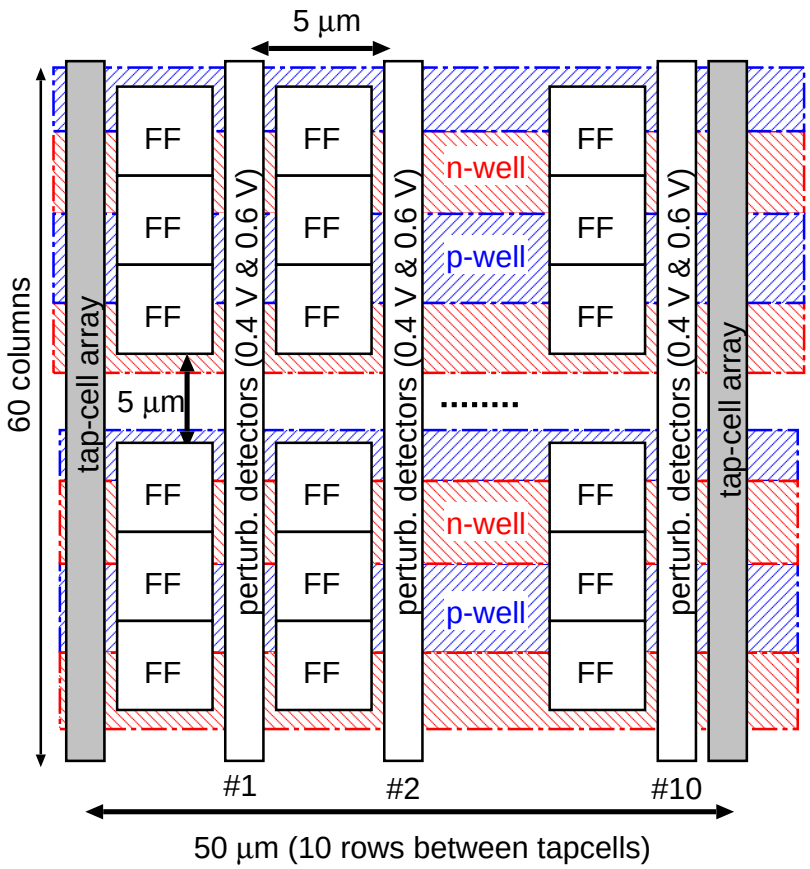

Fig. 2. Block diagram of measurement circuit with detector and shift register.

As shown in Fig. 2, FF arrays and two types of detectors are implemented every 5 μm. FFs arrays are composed of a 60×100-bit shift register. Fig. 3 shows the schematic diagram of the implemented FF. Tap-cell arrays are inserted into every 50 μm. The tap-cell is constructed by N-well and P-well contacts and it stabilizes well-potential. There are 10 columns of FF arrays and detectors between two tap-cell columns. The threshold voltages of detectors are 0.4 V and 0.6 V. The latter threshold voltage, 0.6 V is equal to the threshold voltage value above which the current flows to PN diode between well and drain regions. We assume that if an MCU is caused by the parasitic bipolar effect, the proposed circuit detects 0.6 V perturbation of well-potential whenever an MCU occurs on FFs. The 0.4 V perturbation detector is fabricated to detect SEUs and also to duplicate perturbation detector and remove wrong detections by an SEU on 0.6 V perturbation detector.

In this test circuit, duration time of well-potential perturbations is measured with 5 μm spatial resolution at two voltage levels, 0.4 V and 0.6 V. In order to remove the parasitic bipolar effect on the chains caused by well-potential perturbation, they are placed on wells isolated from the measured ones.

III. Experimental Setup

Fig. 4 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. It is implemented by tapless standard cells [16] on a twin-well (dual-well) structure. In order to measure neutron-induced well-potential perturbation and MCU rates on FFs, a 6,000 (60 × 100) bit shift register is

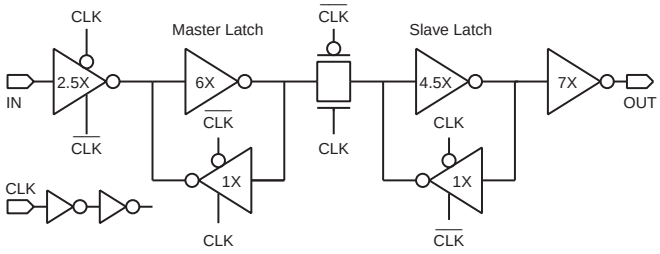

Fig. 3. Schematic diagram of implemented FF.

implemented and its total area is 0.5 × 0.6 mm^2 on a 2 × 4 mm^2 die.

Accelerated tests were carried out at RCNP (Research Center for Nuclear Physics, Osaka University). Fig. 5 shows the neutron beam spectrum compared with the terrestrial neutron spectrum at the ground level of Tokyo. The average acceleration factor is 3.8×10^8. In order to increase error counts, we measured 28 chips at the same time using stacked DUT (Device Under Test) boards. An engineering LSI tester is used to control DUTs and collect shifted error data. During irradiation, stored values of the shift register are initialized to "ALL0" and clock signal is fixed to "1" to keep master latches on FFs in the hold state. Stored values are retrieved every 5 minutes.

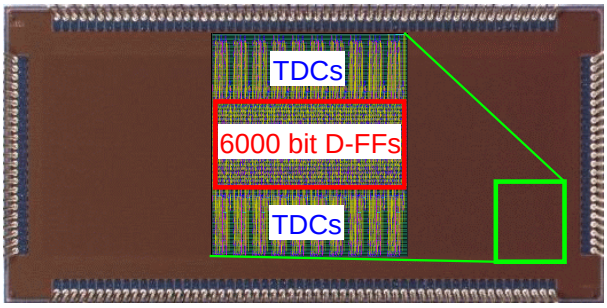

Fig. 4. Chip micrograph and floorplan.

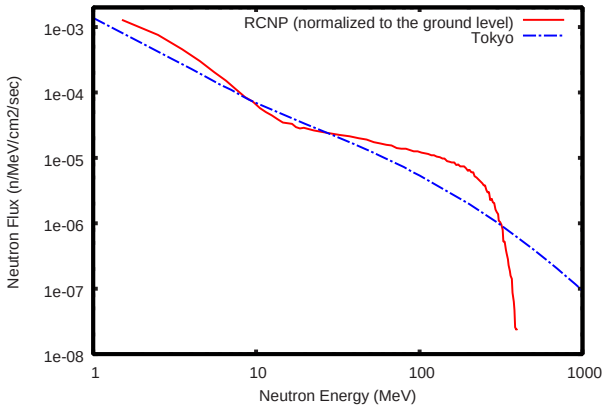

Fig. 5. Neutron spectrum at RCNP.

IV. Experimental Results and Discussions

In this section, we show measurement results of well-potential perturbation and soft errors on FFs. To show measurement results shortly, we use these abbreviations as shown in Table I.

A. Relationship between Well-Potential Perturbations and Soft-Error on FFs

Table II shows the total number of SEUs, MCUs and WPPs. $\mathrm{MCU_{vertical}}$ shows the number of flips on 2 bit FFs between vertically-contacted cells, whose master latches are separated by 0.7 μm. $\mathrm{MCU_{horizontal}}$ shows the number of flips on 2 bit FFs between horizontally-contacted cells,whose master latches are separated by 5 μm. The rates of WPPs are about 1 – 4x bigger than the SEU rate on FFs. It is because well-potential perturbation may happen without SEUs when a particle hits on the circuit blocks which do not cause an SEU such as clock buffers or slave latches in the transparent state.

Fig. 6 shows the relationship between well-potential perturbation and soft-errors on FFs. The relationship between

TABLE I
LIST OF ABBREVIATION.

Abbreviation	Meaning
WPP	well-potential perturbation
WPP[P, 0.4 V]	P-well-potential perturbation over 0.4 V
WPP[P, 0.6 V]	P-well-potential perturbation over 0.6 V
WPP[N, 0.4 V]	N-well-potential perturbation over 0.4 V
WPP[N, 0.6 V]	N-well-potential perturbation over 0.6 V

TABLE II
THE TOTAL NUMBER OF WPPS, SEUS AND MCUS ON FFS.

	Count
SEU	455
$\mathrm{MCU_{vertical}}$	33
$\mathrm{MCU_{horizontal}}$	4
WPP[P, 0.4 V]	1514
WPP[P, 0.6 V]	709
WPP[N, 0.4 V]	1633
WPP[N, 0.6 V]	565

TABLE III
AVERAGE DURATION TIME OF WPPS WHEN SOFT-ERROR ON FF OCCURS WITH WPP.

	Average duration time of WPP			
	[P, 0.4 V]	[P, 0.6 V]	[N, 0.4 V]	[N, 0.6 V]
No error	530 ps	350 ps	670 ps	460 ps
SEU	930 ps	750 ps	920 ps	880 ps
$\mathrm{MCU_{vertical}}$	1070 ps	800 ps	1030 ps	920 ps
$\mathrm{MCU_{horizontal}}$	1450 ps	1200 ps	1400 ps	1220 ps

WPPs and MCUs are very strong and 95% (35 / 37) of MCUs occur with WPP[P, 0.6 V]. However, no MCU occurs with WPP[P, 0.4 V] but without WPP[P, 0.6 V] as shown in Fig. 6. Therefore, MCUs occur on FFs when the voltage level of P-well-potential perturbation is under 0.4 V or over 0.6 V. We conclude that all MCUs are not caused by the identical mechanism. All MCUs except for two are caused by the parasitic bipolar effect and two MCUs are caused by different mechanisms such as charge sharing or successive hits by one ion [3]. In the fabricated technology, the parasitic bipolar effect is a critical issue for soft-error resilience on redundant flip-flops.

As shown in Fig. 6 and our previous work [13], WPP is weakly overlapped with SEUs on FFs. The WPP detector or bulk built-in current sensor cannot detect all SEU on FFs. However, it can be used as an error detector for redundant FFs because WPP is almost overlapped with MCUs on FFs. The proposed detector and a roll-back function increase soft-error resilience of a radiation-hard system using redundant FFs by 20 times since 95% (35 / 37) of MCUs can be detected by the proposed detector.

Table III shows the average duration time of WPPs when a soft error on FF occurs with WPP. When MCU occurs on FFs, well-potential is perturbed for about 1000 ps at 0.4 V. Especially in the case of horizontal MCU occurrence, it is perturbed for 1,400 ps at 0.4 V and for 1,200 ps at 0.6 V.

B. Characterization of Well-Potential Perturbations

Here, we show measurement results of WPPs. Fig. 7 shows an example of measurement results observing an MCU detected by wide-spread WPPs. The test circuit can detect WPP properly since WPP[P, 0.4 V] (WPP[N, 0.4 V]) always detect longer WPP than WPP[P, 0.4 V] (WPP[N, 0.6 V]) and longest durations of WPPs are detected at the same location, #4. Well-potential is perturbed for 400 – 600 ps at 0.6 V.

Fig. 8 and 9 show the number of well-potential perturbations by keeping clock signal to "1" during irradiation. X-axis shows the number of the WPP detectors which detect WPP

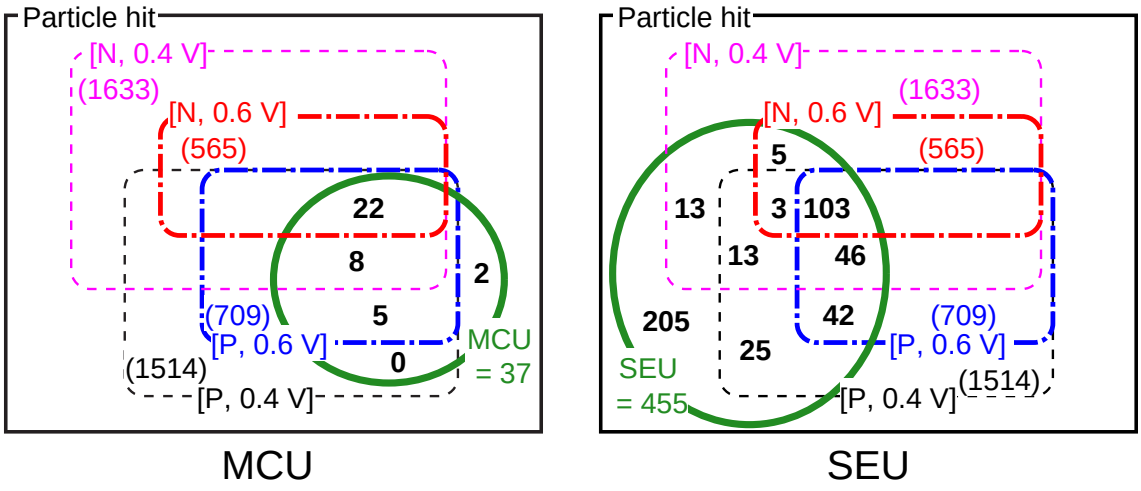

Fig. 6. Venn diagrams showing the relationship between WPPs and MCUs and SEUs. Values in parentheses show the total number of WPP.

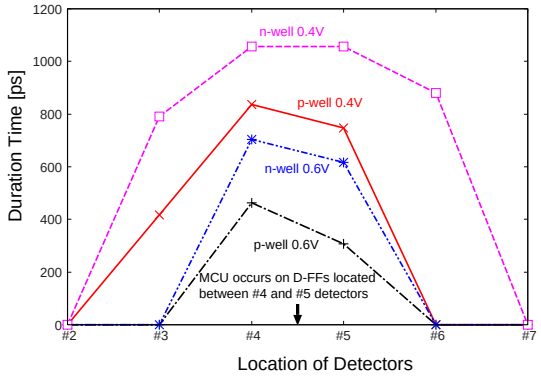

Fig. 7. Example of measurement results for well-potential perturbation with MCU occurrence on FFs placed between #4 and #5 detectors.

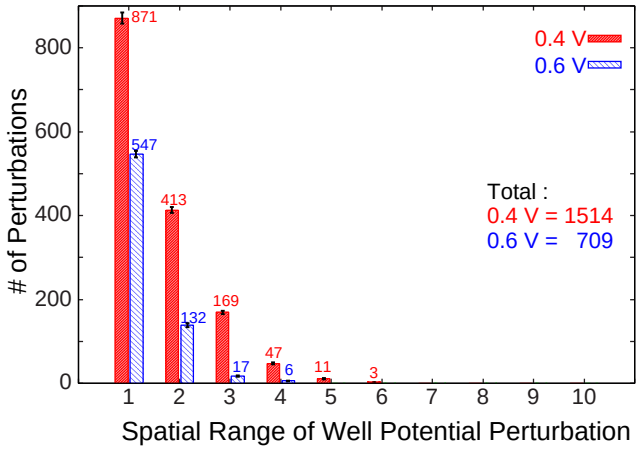

Fig. 8. Spatial range of P-well-potential perturbations.

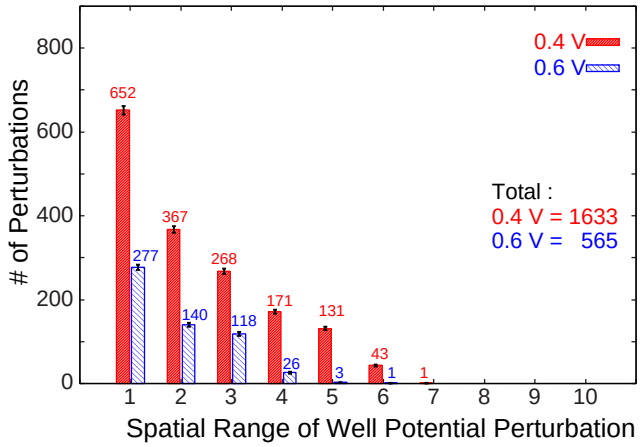

Fig. 9. Spatial range of N-well-potential perturbations.

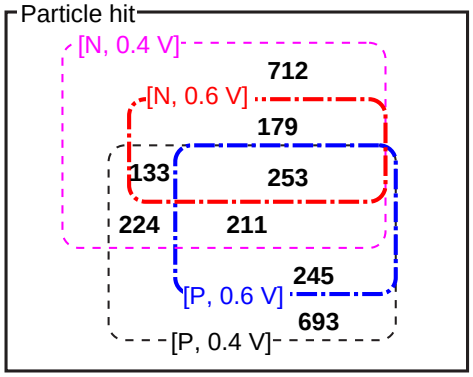

Fig. 10. Venn diagram showing the relationship among WPPs.

simultaneously. It is equal to spatial range of WPP since the WPP detectors are implemented every 5 μm as shown Fig. 2. Comparing WPPs in P-well and in N-well, the number of WPP[N, 0.4 V] is larger than that of WPP[P, 0.4 V]. This is because the transistor width and drain area of pMOS are larger than that of nMOS. However, the number of WPPs[N, 0.6 V] is smaller than those of WPPs[P, 0.6 V]. We assume that electrons generated by a neutron strike in N-well are diffused more quickly and N-well-potential is not easily reduced since the electron mobility is bigger than the hole mobility. The spatial range of N-well-potential perturbations is wider than that of P-well-potential perturbations. The difference of the spatial ranges is also caused by the difference of N-well and P-well structures. Our test chip is implemented with the twin-well structure. The depth of N-well is much thinner than P-well (P-substrate).

Fig. 10 shows relationship between P-well-potential and N-

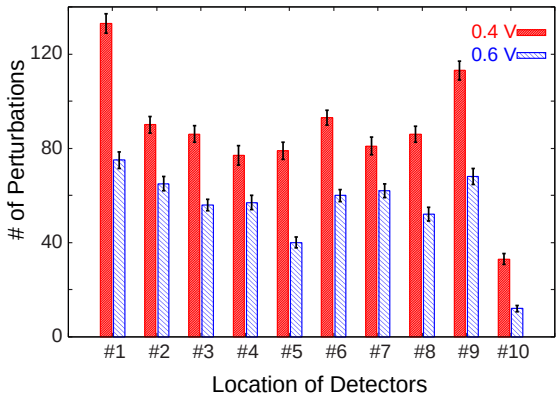

Fig. 11. The number of P-well-potential perturbation detected by one detector according to the distance from tap-cells.

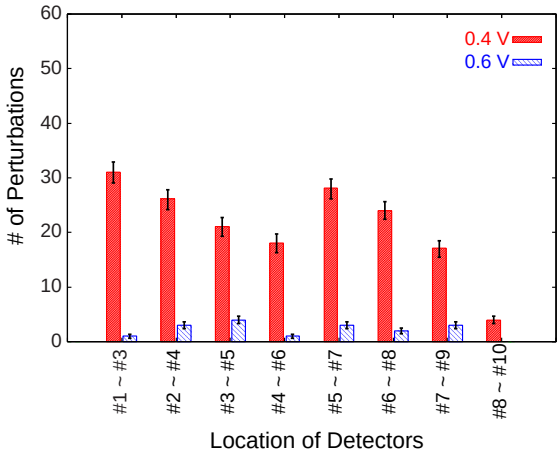

Fig. 12. The number of P-well-potential perturbation detected by three adjacent detectors according to the distance from tap-cells.

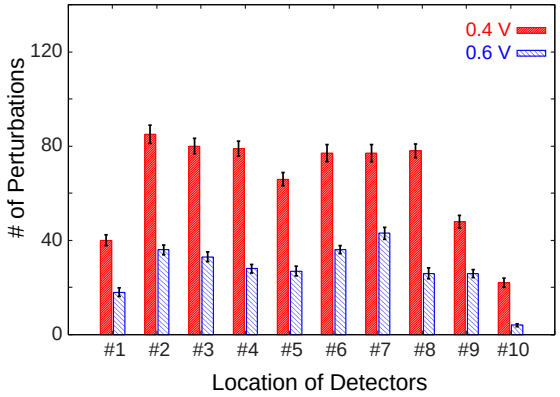

Fig. 13. The number of N-well-potential perturbation detected by one detector according to the distance from tap-cells.

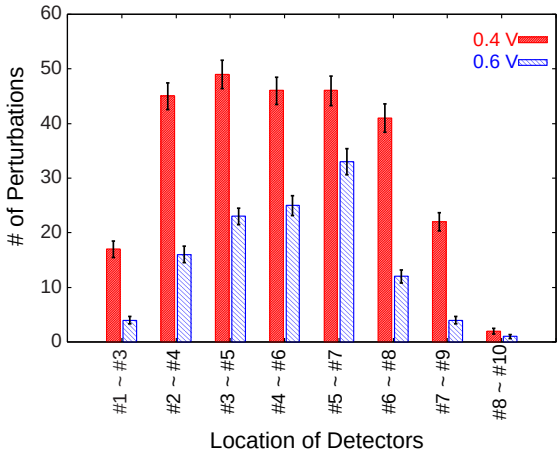

Fig. 14. The number of N-well-potential perturbation detected by three adjacent detectors according to the distance from tap-cells.

well-potential perturbations. About a half of WPPs[N, 0.4 V] occurs simultaneously with WPP[P, 0.4 V]. We assume that it is caused by the diffusion current flowing into a PN junction between P-well and N-well.

Fig. 11–14 show the number of well-potential perturbations detected by one or three adjacent detectors respectively according to the distance from tap-cells. As shown in Fig. 13 and 14, the number of N-well-potential perturbations depends on the distance from tap-cells. The number of WPP[N, 0.4 V] detected by #1, #9 and #10 detectors is smaller than that detected by #2 – #8 detectors which are separated from tap-cell by over 10 μm. In contrast, the number of P-well-potential perturbations does not depend on the distance from tap-cells. The #1 detector detects the maximum number of WPP[P, 0.4 V].

The number of P-well-potential perturbation is small detected by the #10 detector which is nearest to tap-cells. Therefore, even if tap-cells are inserted every 5 μm, MCU rate on FFs is not reduced drastically. In order to reduce WPPs and MCU rate on FFs, we should not fabricate a chip composed of tapless standard cells. It must be composed of conventional standard cells which have well-contacts under their power and ground rails.

V. Conclusion

We show measurement results of well potential perturbation caused by a particle hit from spallation neutron irradiation. The implemented detectors can measure duration time of well-potential perturbation with 5 μm spatial resolution at two voltage levels, 0.4 V and 0.6 V. Experimental results by neutron irradiation on a 65-nm bulk CMOS show that rate of well-potential perturbation is 1 to 4 times bigger than the SEU rate on FFs and perturbation durations of over 1,000 ps are also measured. 95% of MCUs are detected simultaneously with well potential perturbation. There is a very strong overlap between well-potential perturbation and MCUs on FFs. To reduce MCU rates on FFs or SEU rates on redundant FFs, a chip must be composed of conventional standard cells which have well-contacts under their power and ground rails.

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