

## PAPER

# Device-Parameter Estimation through IDDQ Signatures

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**SUMMARY** We propose a novel technique for the estimation of device-parameters suitable for postfabrication performance compensation and adaptive delay testing, which are effective means to improve the yield and reliability of LSIs. The proposed technique is based on Bayes' theorem, in which the device-parameters of a chip, such as the threshold voltage of transistors, are estimated by current signatures obtained in a regular IDDQ testing framework. Neither additional circuit implementation nor additional measurement is required for the purpose of parameter estimation. Numerical experiments demonstrate that the proposed technique can achieve 10-mV accuracy in threshold voltage estimations.

**Key words:** *IDDQ testing, statistical leakage current analysis, Bayes' theorem*

## 1. Introduction

The recent advances in process technology are major driving forces for achieving high-performance, high-density LSIs. The performance of LSIs is often limited by process parameter variability, in particular, by delay variability. Statistical static timing analysis (SSTA) has been proposed to effectively handle statistical delay variations and is expected to become a mainstream timing sign-off method in advanced technologies [1]. The effective use of SSTA will contribute to alleviate timing margin and thus reduce the number of design iterations required to achieve the timing constraint.

The use of SSTA, however, may increase parametric faults because many paths will have delays that are very close to the constraint. This issue has been pointed out by the International Technology Roadmap for Semiconductors (ITRS) [2]. To cope with this difficulty, adaptive techniques are very effective. For example, an adaptive substrate-bias control for each manufactured chip has been proposed to compensate for delay change resulting from threshold voltage variations [3]. In LSI testing, the idea of adaptive testing, in which a set of test paths is altered to apply the most suitable one for a chip, has been proposed [4]–[6]. Both of these techniques rely on the device-parameter estimations, such as threshold voltages of transistors, of an individual chip. The effectiveness and accuracy of the estimation have crucial impact on adaptive techniques, thus determining their effectiveness.

On-chip process parameter variations are classified into

global variations and local variations [7]. The above adaptive techniques try to compensate for or make use of knowledge of the global component of the parameters based on measurements. Global variations are deviations from a target value, which is common to all transistors within a chip. The global variation component can also be considered as an offset of a parameter calculated as an average over a chip [8], [9]. Local variations, in contrast, manifest themselves at the device-level fluctuation and vary independently from device to device.

Various circuits have been studied [10]–[14] for estimating the device-parameters. In [10], [15], a circuit called a device matrix array is used for estimating parameter variations of a large number of transistors. In the device array, transistors are placed regularly to minimize pattern-dependent variations. Current versus voltage characteristics are measured first, and then global and local parameters are numerically extracted with postprocessing. The array circuits, in general, occupy a large silicon area, and special instruments that can accurately measure device currents are required, which makes it difficult to integrate these circuits on a chip cost-effectively. It is unrealistic to place the array-like circuits on a product chip.

For the purpose of fast and simple on-chip parameter estimation, a method using ring oscillators has been proposed [11]. The frequency change of the ring oscillator roughly indicates the device-parameters of the chip. Compared with the transistor array, its measurement is easy and its area is small. However, the method cannot distinguish the parameters; such as threshold voltage shift between pMOS and nMOS transistors. Information available from the ring oscillator is so limited that it is still insufficient to use in postfabrication compensation techniques or adaptive testing schemes that require quantitative device-parameters. In [12]–[14], methods to extract global and local parameters from ring oscillator frequencies have been proposed. Although these techniques can extract device-parameters accurately, implementation of additional circuits irrelevant to the original functionality of the circuit is still required. In addition, these techniques require measurement time for the circuits implemented on the chip.

In this paper, we propose a novel technique for device-parameter estimation. Our estimation technique requires no additional circuit and no extra measurement time. In other words, our technique can be used within a regular IDDQ testing framework. In the proposed technique, expected statistical leakage currents of a standard logic cell under vari-

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ous device-parameters are constructed in advance as a statistical leakage library. Then, likelihood functions for leakage currents of a target circuit at various process regions in the device-parameter space are calculated using the library. Finally, device-parameters are estimated as probabilities through Bayes' theorem by comparing a current signature obtained by a regular IDDQ testing flow with the likelihood functions.

The remainder of this paper is organized as follows. In Sect. 2, the proposed estimation method to extract device-parameter variation is described. In Sect. 3, experimental results on the ISCAS'89 benchmark circuit are presented. An estimation accuracy within 10 mV has been achieved in this experiment. Finally, we conclude this paper in Sect. 4.

## 2. Device-Parameter Estimation Using IDDQ Signatures

In this section, we propose a device-parameter estimation using the IDDQ signature of an individual chip by using Bayes' theorem.

Figure 1 shows the overall flow of the proposed technique. The salient feature of this technique is that information required to execute our process estimation is all obtained from a regular IDDQ testing flow. Hence, no additional circuit nor modification of the testing flow is required to put our estimation technique into practice. In regular IDDQ testing, an ATPG tool generates a test pattern set targeting an IDDQ fault model for a given circuit. At the same time, the ATPG tool also generates respective internal states of all logic gates for each test pattern. After a chip is manufactured, the test patterns are applied and IDDQ currents are measured. Statistical postprocessing, such as nearest neighbor residual (NNR), is conducted to judge whether or not a chip under test is defective [16], [17].

In the proposed parameter estimation, an IDDQ current signature of a nondefective chip is utilized. Our goal is to estimate device-parameters of a chip. We perform this task

through the following three steps:

- A. gate-level leakage library preparation,
- B. chip-level leakage library calculation, and
- C. Bayesian parameter estimation.

In the proposed flow, a gate-level statistical leakage library (SLL) is first prepared for a given standard logic cell set. The gate-level SLL is constructed for all gates in the given standard logic cell library under given device-parameter variations. Then, a chip-level SLL is prepared for a target circuit by using the gate-level SLL and input-pin states of all logic gates determined by IDDQ testing patterns. The chip-level library contains the total leakage current distributions of the circuit for the combinations of all process regions in the process space and all IDDQ test patterns. The chip-level SLL can be efficiently calculated by consulting the gate-level SLL. Finally, global parameters are estimated using Bayes' theorem by using chip-level SLL and measured IDDQ signature.

The preparation of the gate-level SLL is necessary only once for a given set of standard logic cells. The second step, leakage current calculation, is necessary once for a circuit. The last step, Bayesian parameter estimation, is necessary for every chip to know its specific device-parameters.

IDDQ current is defined as the quiescent current when all node voltages in a circuit have settled to the final values [18]. For a chip that has passed the IDDQ test, its IDDQ current is equivalent to the leakage current. Here, the leakage current consists of subthreshold leakage, gate tunneling leakage, and the reverse-bias p-n junction leakage currents. In this paper, we assume the subthreshold leakage is the dominant component that determines IDDQ current [9]. In [19], the subthreshold leakage current  $I$  is expressed as

$$I = I_0 \exp\left(\frac{V_{gs} - V_{th}}{nV_T}\right) \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right). \quad (1)$$

Here,  $I_0 = \mu_0 C_{ox}(W_{eff}/L_{eff})V_T^2 \exp(1.8)$  and  $V_T = kT/q$ , while  $k$  is the Boltzmann constant,  $\mu_0$  is the charge-carrier effective mobility,  $C_{ox}$  is the gate oxide capacitance per unit area,  $T$  is the absolute temperature,  $q$  is the electric charge of an electron,  $n$  is an exponent coefficient,  $V_{gs}$  and  $V_{ds}$  are gate-source and drain-source voltages, respectively,  $V_{th}$  is the threshold voltage of the device, and  $W_{eff}$  and  $L_{eff}$  are effective channel width and length, respectively. We see that the subthreshold leakage current  $I$  is exponentially dependent on  $V_{th}$ .

### 2.1 Gate-Level Leakage Library Preparation

In our proposed technique, a device-parameter space is divided into regions spanned by the range of possible variations of parameters. Each region in the device-parameter space is considered as the minimum resolution in our estimation. An example of a segmented two-dimensional device-parameter space is illustrated in Fig. 2. The horizontal and vertical axes express device-parameters, i.e., global parameters,  $\Delta V_{thn}$  and  $\Delta V_{thp}$ , respectively. Here,  $\Delta V_{thn}$  and

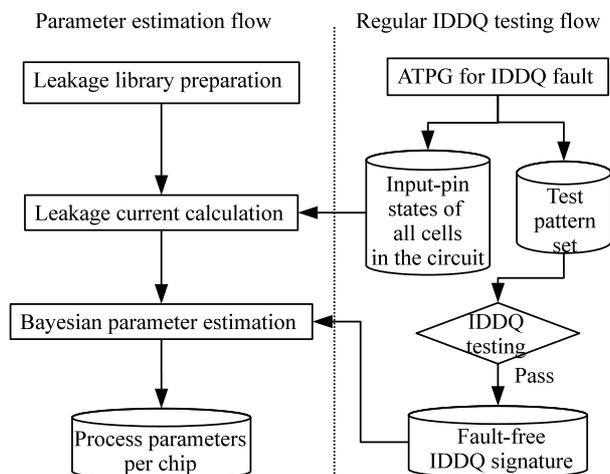
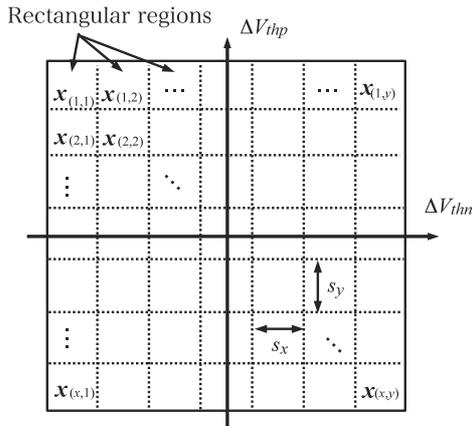


Fig. 1 Overall flow of the proposed parameter estimation technique.

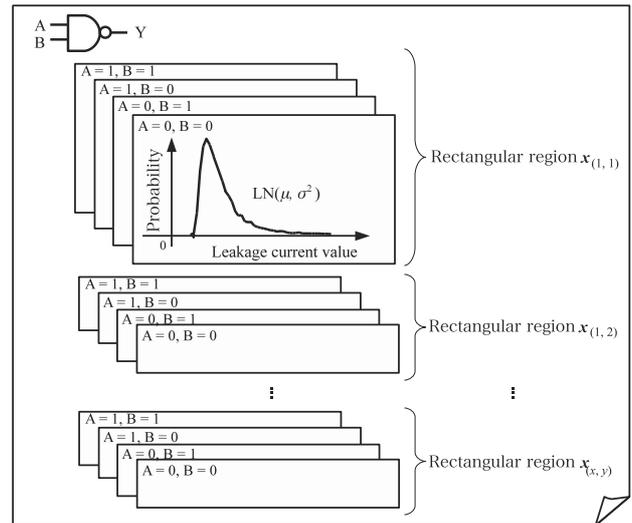


**Fig. 2** Segmentation of a two-dimensional device-parameter space into rectangular regions.

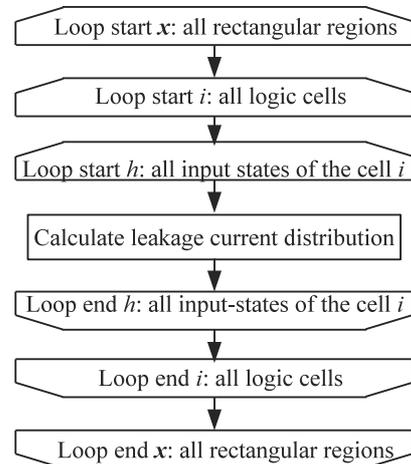
$\Delta V_{thp}$  are the deviation of threshold voltages of nMOS and pMOS transistors, respectively, from their typical values. The device-parameter space is divided into  $x \times y$  regions by  $s_x$  and  $s_y$  intervals, which are determined by a tradeoff between computational cost and required estimation accuracy. Hereafter,  $\mathbf{x}$  represents a *rectangular region*, which is global parameters that are specified by a region in the process space.  $\mathbf{x}$  is a  $d$ -dimensional vector, where  $d$  is the number of global process parameters that we are going to estimate. In the rest of this paper, we assume that  $\Delta V_{thn}$  and  $\Delta V_{thp}$  are the examples of global process parameters, i.e.,  $\mathbf{x}$  is a two-dimensional vector. We here note that other parameters, such as the channel length of a transistor, can also be estimated by extending our proposed method. In the case that three parameters are estimated, the dimension of the device-parameter space becomes three.

In the gate-level leakage library preparation step, a gate-level SLL is constructed. The library contains the leakage current distributions of the logic cells, which differ by their input signal values. Hence, to build the gate-level SLL, the leakage distributions are calculated for all logic cells with all combinations of their input signal values, for all rectangular regions. A conceptual illustration of the contents of the gate-level SLL for a 2-input NAND gate is presented in Fig. 3. For logic cells that have an internal state, such as flip-flop cells, the internal state is also considered as the input.

A leakage current distribution of a logic cell with an input combination at a rectangular region  $\mathbf{x}$  is calculated by Monte Carlo circuit simulations involving local variation of the parameters. The number of simulations in the Monte Carlo simulation is essentially determined by a required accuracy of the chip-level SLL, the relationship of which is described in Appendix. A procedure to obtain the leakage current distributions is shown in Fig. 4. By adding a random component of local parameter variation to the global component that is represented as a rectangular region  $\mathbf{x}$ , the device-parameters of each transistor are determined. Through circuit simulation, the leakage current distribution of a logic



**Fig. 3** An example illustration of the content of gate-level SLL. In the case of a 2-input NAND gate, probability density functions of leakage currents are calculated for all combinations of input signals and rectangular regions.



**Fig. 4** Procedural steps for gate-level SLL preparation.

cell at a particular parameter  $\mathbf{x}$  can be computed. Each leakage current distribution is then approximated to a log-normal distribution [20], [21].

In general, this is a very time-consuming process since it relies on Monte Carlo circuit simulations and the total number of combinations is large. However, this process is required only once for a given standard logic cell set. The current distributions in the gate-level SLL can be compactly represented by approximations. When a log-normal distribution is used for the approximation, only two parameters, the mean  $\mu$  and the variance  $\sigma^2$ , can be recorded, although recording all raw data is also possible.

## 2.2 Chip-Level Leakage Library Calculation

The steps for the chip-level leakage library calculation procedure are summarized in Fig. 5. The total leakage current

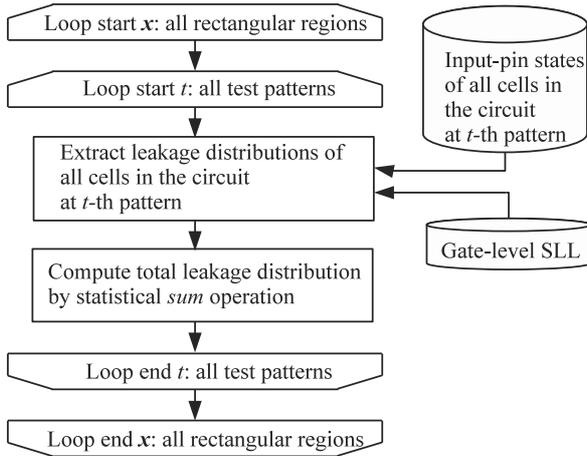


Fig. 5 Procedural steps for chip-level SLL calculation.

distribution  $I$  of a target circuit is obtained by adding the leakage current distributions for all gates,

$$I = I_{\text{gate}_1} + I_{\text{gate}_2} + \cdots + I_{\text{gate}_N}, \quad (2)$$

where  $N$  is the number of gates in the circuit and  $I_{\text{gate}_j}$  is the leakage current distribution of the  $j$ -th logic gate. In the above equation, “+” represents a statistical *sum* operation. This can be calculated either through analytical derivation [20], [21] or through Monte Carlo simulation. In the Monte Carlo simulation, the following two steps are repeated many times:

- (1) For each logic gate in the circuit, generate a random sample of a leakage current from the corresponding gate leakage current distribution stored in the gate-level SLL. The current distribution is determined by rectangular region  $\mathbf{x}$  and input signal values of the gate.
- (2) Add the leakage currents of all gates to obtain the total leakage current, which yields an instance of the total leakage current of the circuit.

After a sufficient number of leakage current instances are calculated, the histogram of the currents is then approximated to a log-normal distribution. We define the approximate probability density function (PDF)  $f_{(\mathbf{x};t)}(I)$  for a total leakage current  $I$  at the  $t$ -th test pattern when a chip belongs to a rectangular region  $\mathbf{x}$ .

Here, the leakage current distribution of each logic cell is calculated by considering local variations in addition to the rectangular region  $\mathbf{x}$ . The correlations resulting from global variations are considered correctly in the statistical sum operation. The leakage current distributions of the circuit for all test patterns at all the rectangular regions are calculated; these are represented as nested loops of rectangular regions  $\mathbf{x}$  and IDDQ test patterns  $t$  in Fig. 5. Since we already have a list of node voltages, i.e., input states of all cells contained in the circuit for each test pattern as a regular output of an ATPG tool in the IDDQ testing flow, calculation of the total leakage current distribution is efficiently conducted by consulting the chip-level SLL. Although the number of combinations is large, this is a fast process.

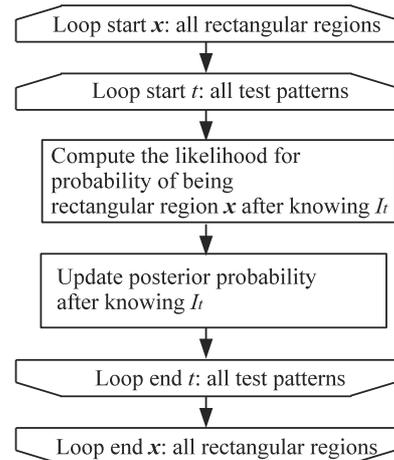


Fig. 6 Bayesian estimation procedure.

### 2.3 Bayesian Parameter Estimation

In the Bayesian estimation step, the rectangular region in which a chip belongs to is estimated. As we proceed with the test patterns, IDDQ currents are obtained. These currents can be considered as incremental information. According to Bayes’ theorem, as more information is available, more accurate estimation becomes possible. We here apply Bayes’ theorem for estimation. More specifically, our estimation is to obtain probabilities that a chip belongs to a particular region  $\mathbf{x}$  based on IDDQ currents.

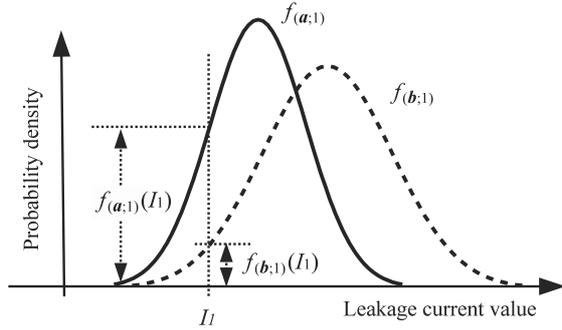
Let us consider a *generation probability* of an IDDQ current. When we observe a current for a particular IDDQ test pattern, we can define a generation probability that the current is from a chip that belongs to a region  $\mathbf{x}$ . Based on Bayes’ theorem, the generation probability can be incrementally updated as we incrementally obtain IDDQ currents for different test patterns. Figure 6 shows the procedure of our estimation. We compute the likelihood of a chip being a region  $\mathbf{x}$  based on the generation probability as a prior probability for Bayes’ theorem. Then, proceeding with the IDDQ measurements, the posterior probability will be updated every time after knowing the IDDQ current  $I_t$  of the  $t$ -th test pattern. At any time of this estimation step, we have the probability distribution of a chip as a function of  $\mathbf{x}$ .

In the beginning, we assume a prior probability of a chip that belongs to a device-parameter region  $\mathbf{x}$  as  $P(\mathbf{x})$ . Through Bayes’ theorem, the posterior probability  $P(\mathbf{x}|I_1)$ , after knowing an IDDQ current of  $I_1$  through the first IDDQ test pattern ( $t = 1$ ), is expressed as follows:

$$P(\mathbf{x}|I_1) = \frac{P(I_1|\mathbf{x})P(\mathbf{x})}{P(I_1)}, \quad (3)$$

where  $P(\mathbf{x}|I_1)$  is the probability that the IDDQ current is measured as  $I_1$  when the chip belongs to region  $\mathbf{x}$ . Since  $P(\mathbf{x}|I_1) \propto f_{(\mathbf{x};1)}(I_1)$  and the denominator of Eq. (3) is a constant for any  $\mathbf{x}$ , Eq. (3) is given as follows:

$$P(\mathbf{x}|I_1) \propto f_{(\mathbf{x};1)}(I_1)P(\mathbf{x}). \quad (4)$$



**Fig. 7** Concept of likelihood for an observed leakage current  $I_1$ . The rectangular region **a** is more probable to explain  $I_1$  than **b** is.

Here,  $f_{(x;1)}$  can be obtained by referencing the likelihood functions obtained in the previous step. The probability  $P(x|I_1)$  can be calculated as follows:

$$P(x|I_1) = \frac{f_{(x;1)}(I_1)P(x)}{\sum_x f_{(x;1)}(I_1)P(x)}, \quad (5)$$

where the denominator of Eq. (5) is a normalization constant.

Figure 7 illustrates the likelihood concept. In this figure, there are two candidate conditions from which the current  $I_1$  is observed. The likelihood expresses how likely it is for current  $I_1$  to come from a parameter region. The likelihood for region  $x$  can be obtained as  $f_{(x;1)}(I_1)$ . In Fig. 7,  $f_{(a;1)}(I_1)$  and  $f_{(b;1)}(I_1)$  of regions **a** and **b** are shown. In this example, it is more likely that the chip belongs to region **a** since  $f_{(a;1)}(I_1) > f_{(b;1)}(I_1)$ .

Next, we update the probability  $P(x|I_2)$  based on the second IDDQ current and the prior probability  $P(x|I_1)$ . Again, Eq. (3) is given by Bayes' theorem as

$$P(x|I_2) = \frac{P(I_2|x)P(x|I_1)}{P(I_2)}. \quad (6)$$

By substituting the conditional probability with the likelihood, Eq. (6) becomes

$$P(x|I_2) \propto f_{(x;2)}(I_2)P(x|I_1). \quad (7)$$

From Eq. (7), the posterior probability can be updated using the following equation:

$$P(x|I_2) = \frac{f_{(x;2)}(I_2)P(x|I_1)}{\sum_x P(x|I_2)f_{(x;2)}(I_1)} \quad (8)$$

Ideally, the posterior probability is expected to be more accurate using the additional information of the second IDDQ current,  $I_2$ . The update process can be applied for  $t \geq 3$ :

$$P(x|I_t) = \begin{cases} \frac{f_{(x;1)}(I_1)P(x)}{\sum_x P(x|I_1)f_{(x;1)}(I_1)} & (t = 1), \\ \frac{f_{(x;t)}(I_t)P(x|I_{t-1})}{\sum_x P(x|I_t)f_{(x;t)}(I_t)} & (t \geq 2). \end{cases} \quad (9)$$

Generation probabilities of each region are incrementally updated as newer IDDQ currents become available.

### 3. Experimental Results

#### 3.1 Experimental Setup

We conduct numerical experiments on ISCAS'89 benchmark circuits to evaluate the proposed estimation technique. The results for s38584 will be presented in this section. A commercial standard cell library of a 65-nm CMOS process is used throughout the evaluation.

##### 3.1.1 IDDQ Testing Flow

Test patterns are generated by a commercial ATPG tool [22]. A pseudo stuck-at fault model is used as the target fault model in the test pattern generation. The total number of test patterns is 49, with which the test coverage is 100%.

In this evaluation, measurement of the IDDQ current is simulated by the following process:

- (1) Determine a process region that a chip belongs to.
- (2) For each logic gate in the circuit, draw a leakage current randomly from the gate leakage current distribution in the gate-level SLL. The current distribution is determined by the process region of the chip and input signal values of the gate.
- (3) Accumulate all gate leakage currents to obtain the total leakage current of the chip.

This process gives an instance of leakage current considering both global variation  $x$  and random variation.

##### 3.1.2 Parameter Estimation Flow

In the leakage library preparation step, leakage currents are computed by 1,000 samples of Monte Carlo simulations using a SPICE simulator [23] at room temperature. The standard logic library consisting of 57 gates is used. Given all input signal combinations, the total number of log-normal distributions is 1218. We assume two parameter variations: threshold voltages of nMOS and pMOS transistors. The random component of the variations is assumed to follow a Pelgrom model [24]. Global variations of the nMOS and pMOS threshold voltages are denoted as  $\Delta V_{\text{thn}}$  and  $\Delta V_{\text{thp}}$ , respectively. We assume the global variability follows a normal distribution as reported in [8], and the standard deviation of the normal distribution is 26.7 mV. We set the ranges of the global variations are from  $-80$  to  $+80$  mV, for both  $\Delta V_{\text{thn}}$  and  $\Delta V_{\text{thp}}$ . We assume there is no correlation between the global variations. In our circuit simulation,  $\Delta V_{\text{thn}}$  and  $\Delta V_{\text{thp}}$  are given by an instance parameter DELVTO that is a shift in zero-bias threshold voltage. The segmentation interval is 10 mV, and thus the total number of rectangular regions is 289. For the rest of this section, we represent a region of the two-dimensional parameter space by putting the variations in parentheses, for example,  $(\Delta V_{\text{thn}}, \Delta V_{\text{thp}}) = (40 \text{ mV}, -40 \text{ mV})$ .

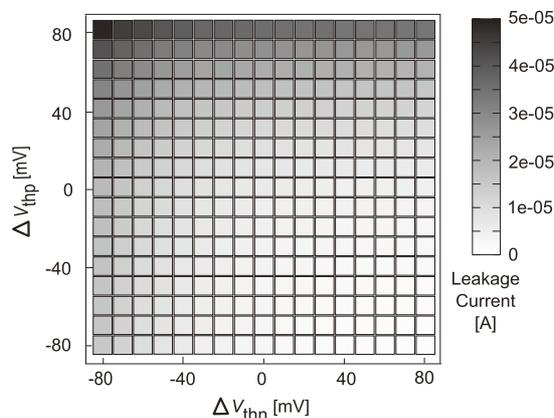
In the Bayesian parameter estimation, the initial prior

$P(\mathbf{x})$ , where  $\mathbf{x}$  is a vector of  $\Delta V_{\text{thn}}$  and  $\Delta V_{\text{thp}}$ , is assumed to be a joint probability of uniform distributions over the range of  $-80$  to  $+80$  mV.

### 3.2 Chip-Level SLL

Figure 8 shows a map of the leakage current of a realization of s38584 for test pattern  $t = 1$ . Figure 9 shows maps of the two parameters that describe log-normal approximations,  $\mu$  and  $\sigma^2$ , for total leakage current estimations of the same circuit. The figure is obtained as an output of the chip-level leakage current calculation step. In these figures, the horizontal and vertical axes represent  $\Delta V_{\text{thn}}$  and  $\Delta V_{\text{thp}}$ , respectively. The bottom-right corner represents a SS (slow-slow) condition where the switching speeds of both nMOS and pMOS transistors are slow, and the top-left corner is a FF (fast-fast) condition where the switching speeds of both transistors are fast. Similarly, the bottom-left and top-right corners represent FS and SF conditions, respectively.

In Figs. 8 and 9(a), we see a general trend that leakage current exponentially increases along a  $-45$  degree line, from slow to fast conditions. Along the top and left edges, the leakage current is particularly large. This means that a large leakage current will be observed when either nMOS or pMOS transistor is in fast condition. In CMOS gates, either the pMOS or the nMOS transistor is in an off state, and sum of leakage currents of those off-transistors determine the total leakage current. When the circuit is sufficiently large, about the half of the off-state transistors are pMOS and the other half are nMOS transistors, on average. When a chip is fabricated with fast nMOS transistors, half of the off-state transistors, that are nMOS transistors, are leaky. The same holds for fast pMOS transistors. This is why high leakage currents are observed at the top and left edges. In Fig. 9(b), large variation of the leakage current distribution is observed. Because the leakage currents of pMOS and nMOS transistors are different at these corners, a slight addition of random variation component significantly increases or decreases the total leakage current.



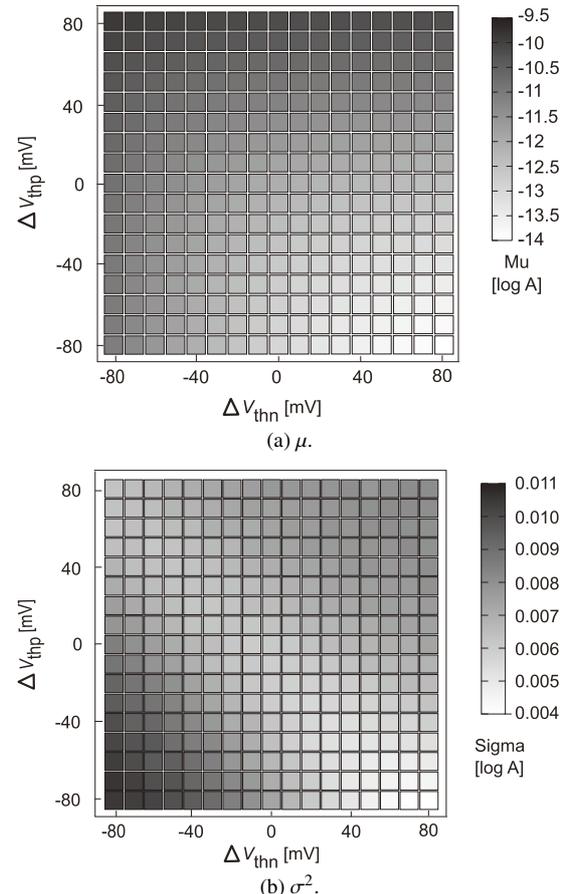
**Fig. 8** Leakage currents of a realization of s38584 for test pattern  $t = 1$  when the chip belongs to various device-parameters.

### 3.3 Estimation Results

The proposed method has been implemented in programming languages C and Ruby. Experiments were carried out using a computer with an Intel(R) Xeon(R) Processor X5570 (CPU: 2.93 GHz, 8 MB Cache) all in a single thread. The CPU times of each step of the proposed method are summarized in Table 1.

#### 3.3.1 Estimation of a Device-Parameters

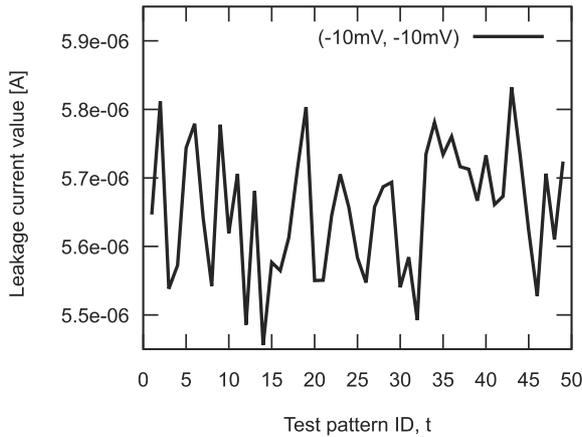
Figure 10 shows an example IDDQ current signature for a fictitious chip having the global parameter variation component of  $(-10$  mV,  $-10$  mV). The figure shows the leakage current of the chip as a function of the test pattern ID,  $t$ . We are going to recover the parameter as a rectangular region from the currents in Fig. 10 by using the proposed technique.



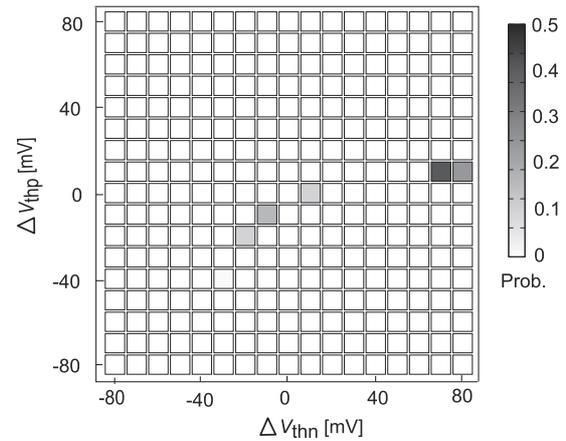
**Fig. 9**  $\mu$  and  $\sigma^2$  of log-normal distribution of the total leakage current of s38584 having different rectangular regions for test pattern  $t = 1$ .

**Table 1** CPU time breakdown.

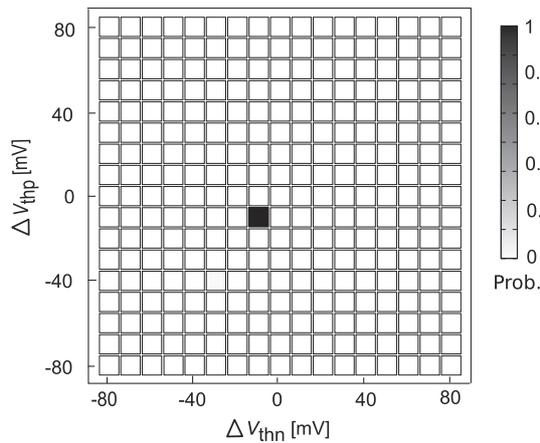
Process	Time (min.)
Gate-level leakage library preparation	17,640
Chip-level leakage library calculation	2,880
Bayesian parameter estimation	1



**Fig. 10** Leakage currents of a fictitious chip as a function of test pattern.



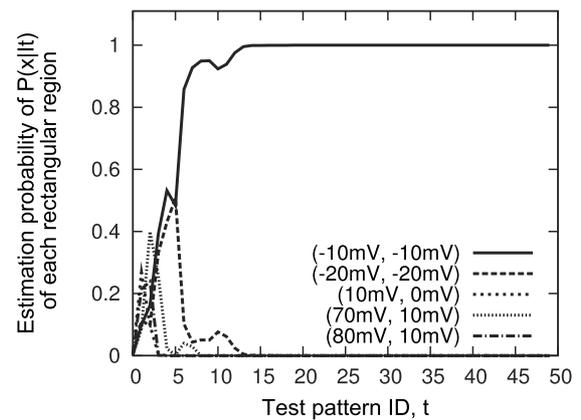
**Fig. 12** Parameter estimation result for the correct rectangular region of  $(-10 \text{ mV}, -10 \text{ mV})$  at  $t = 2$ .



**Fig. 11** Final parameter estimation result for the correct rectangular region of  $(-10 \text{ mV}, -10 \text{ mV})$ .

Figure 11 shows the estimated probability map  $P(\mathbf{x}|I_{49})$ . In this figure, the horizontal and vertical axes represent  $\Delta V_{\text{thn}}$  and  $\Delta V_{\text{thp}}$ , respectively. A square corresponds to a rectangular region of  $10 \text{ mV} \times 10 \text{ mV}$ . A white segment means zero probability, and a nonwhite segment means nonzero probability. As the estimation probability becomes higher, the color changes from white to black. In Fig. 11,  $(-10 \text{ mV}, -10 \text{ mV})$  have been estimated accurately with the proposed method. We also notice that only the correct segment is highlighted very sharply. The probabilities of the chip being in the other segments are close to zero. The estimation probability map at  $t = 2$  is presented in Fig. 12. At this test pattern, Bayesian estimation has not yet fully converged but the five segments including the correct segment of  $(-10 \text{ mV}, -10 \text{ mV})$  have high probability compared with other regions. In Fig. 12, the probability of  $(70 \text{ mV}, 10 \text{ mV})$  has the highest probability among all regions.

Figure 13 shows the change of estimation probabilities  $P(\mathbf{x}|I_t)$  as a function of test pattern ID,  $t$ . The vertical axis represents the estimation probability at the respective rectangular regions. The solid line expresses the change of prob-

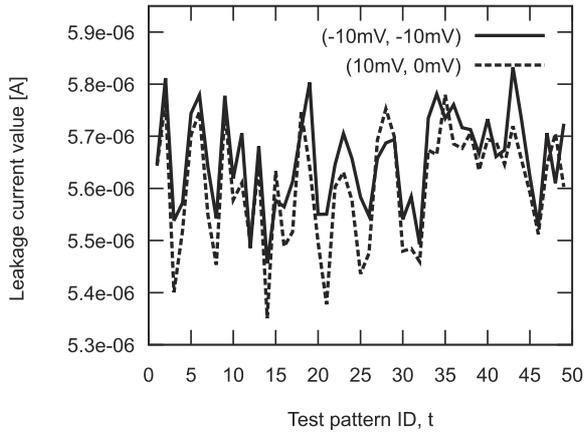


**Fig. 13** Estimation probabilities  $P(\mathbf{x}|I_t)$  as functions of the test pattern ID,  $t$ , for rectangular regions.

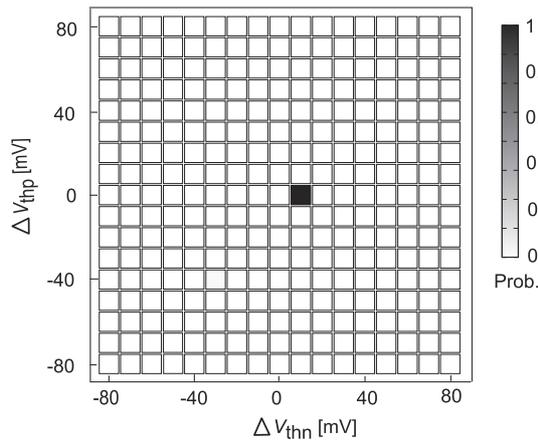
ability for the correct region of  $(-10 \text{ mV}, -10 \text{ mV})$ . Dashed lines express the ones for other four high probability regions in Fig. 12. At the correct region, starting from the initial joint uniform probability ( $t = 0$ ), probability increases rapidly to 1.0 within 15 test patterns. The change of probability is not necessarily monotonic. This is due to the effect of the random variation component and the existence of segments that have similar leakage current. As we increase the number of test patterns, estimation converges to the correct region.

### 3.3.2 Estimation of Two Chips Having Close IDDQ Signatures

Next, the estimation for  $(10 \text{ mV}, 0 \text{ mV})$  is also analyzed. Figure 14 shows two example IDDQ current signatures for two fictitious chips of  $(10 \text{ mV}, 0 \text{ mV})$  and  $(-10 \text{ mV}, -10 \text{ mV})$ . The solid and dashed lines correspond to leakage currents of chips from  $(-10 \text{ mV}, -10 \text{ mV})$  and  $(10 \text{ mV}, 0 \text{ mV})$  global variation regions, respectively. The solid line in Fig. 14 is the same as the one in Fig. 10. The goal of the experiments in this section is to distinguish the



**Fig. 14** Leakage currents of two fictitious chips as a function of test pattern at (10 mV, 0 mV) and (-10 mV, -10 mV).

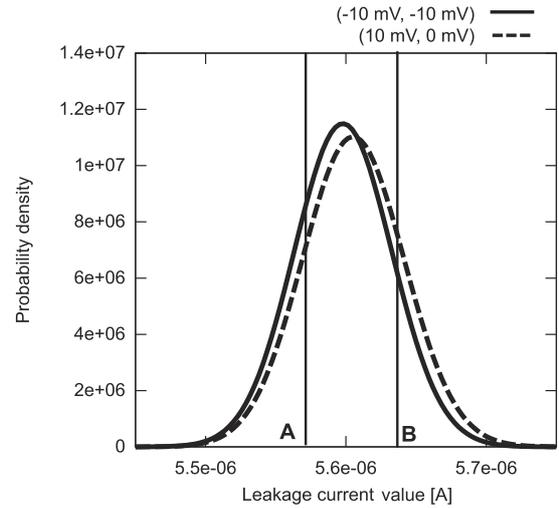


**Fig. 15** Final parameter estimation result for the correct rectangular region of (10 mV, 0 mV).

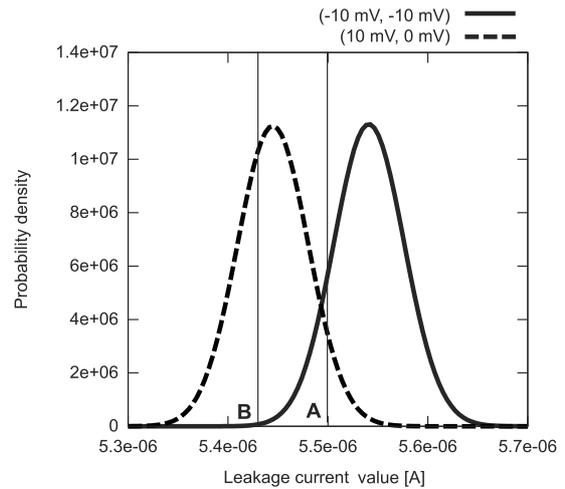
two different rectangular regions behind the signatures. This is a nontrivial task because IDDQ current signatures almost overlap each other and their averages are close.

Figure 15 shows the final estimation result of  $P(\mathbf{x}|I_{49})$  for the chip of (10 mV, 0 mV). The correct rectangular region is clearly indicated. From Figs. 15 and 11, we see that the IDDQ currents that look very similar but that have different global parameter variations have been successfully distinguished with the proposed method. As can be seen from Fig. 12, the region of (10 mV, 0 mV) has been highlighted at the intermediate patterns.

Figure 16 shows distributions of the total leakage currents for rectangular regions (-10 mV, -10 mV) and (0 mV, -10 mV) at  $t = 14$  and  $t = 20$ . These distributions are in the chip-level SLL. Horizontal lines denoted as A and B are the IDDQ currents observed by the respective test patterns when the correct regions are (-10 mV, -10 mV) and (10 mV, 0 mV), respectively. Although averages of the IDDQ current signatures in Fig. 14 are close to each other, their leakage current distributions are different. Consequently, the likelihoods of the respective correct regions are high and those of the wrong regions are low. This is the rea-



(a) At test pattern  $t = 14$ .



(b) At test pattern  $t = 20$ .

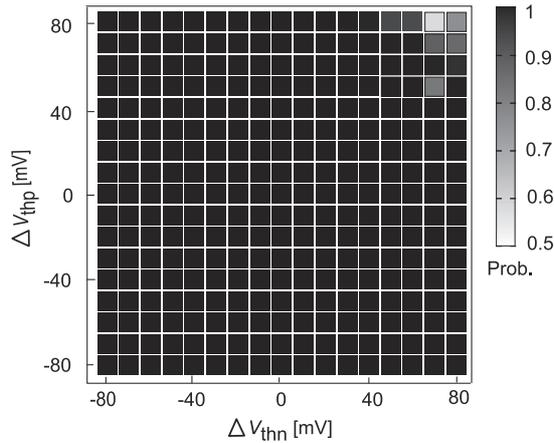
**Fig. 16** Total leakage current distributions and fictitious leakage currents of s38584 circuit when the device-parameter is at (-10 mV, -10 mV) and (10 mV, 0 mV).

son why the proposed method successfully distinguishes the different process regions of the chips having similar IDDQ current signatures.

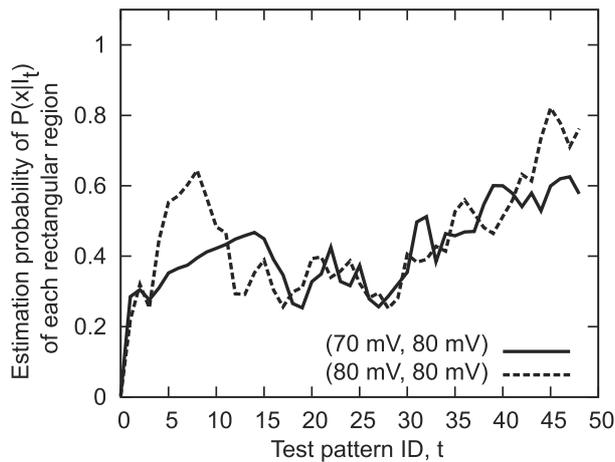
### 3.3.3 Comprehensive Estimation

Using the proposed estimation technique, we analyzed 289 chips, each belonging to a different global parameter region. These chips differ by the global components of the threshold voltage, i.e. parameter regions, and the random components. In this experiment, we would like to confirm that the estimation technique works correctly over all rectangular regions.

Figure 17 shows estimations comprehensively obtained for all 289 rectangular regions  $\mathbf{x}$  at the final probability  $P(\mathbf{x}|I_{49})$ . The color of the regions in the figure represents the probability of  $\mathbf{x}_{\text{correct}}$ , when  $\mathbf{x}_{\text{correct}}$  is the correct rectangular regions. With this definition, if the estimation of a region is completely correct, the corresponding square shows 1.0



**Fig. 17** Final parameter estimation result for each correct rectangular region.



**Fig. 18** Estimation probabilities  $P(x|I_t)$  as functions of the test pattern ID,  $t$ , for the correct rectangular regions of (70 mV, 80 mV) and (80 mV, 80 mV).

(colored as black). Estimation probabilities are 1.0 for almost all regions, indicating a good estimation accuracy regardless of the rectangular regions. A few regions at the top-right corner were not estimated as perfectly as other regions because the total current distributions of these regions are very close to one another. Figure 18 shows the change of estimation probability  $P(x|I_t)$  as a function of test pattern ID,  $t$ , of (70 mV, 80 mV) and (80 mV, 80 mV). In contrast to Fig. 13, convergence to 1.0 cannot be seen for the chips under these conditions because the distributions of these regions are even closer together than in Fig. 16. However, still, estimation probabilities of these regions are higher than 0.5 at  $t = 49$ , meaning that the estimation is correct. Overall, our estimation technique can be successfully used as the device-parameter estimator in adaptive techniques.

#### 4. Conclusion

In this paper, we proposed a novel device-parameter estimation technique. Through Bayes' theorem, it elicits infor-

mation contained in regular IDDQ current signatures, and thus no additional circuit nor modification in IDDQ testing flow is necessary, which is advantageous to existing techniques. Numerical experiments demonstrated that the proposed technique accurately estimates global components of threshold voltage variations within 10 mV. The application of this technique to real silicon measurements will be one of our future works.

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## Appendix

The accuracy of the SLL is determined by the number of samples used in Monte Carlo simulation. We briefly discuss required number of Monte Carlo samples to achieve target accuracy.

Consider a Monte Carlo simulation in which  $N$  samples are drawn from a normal distribution, for example, from the one obtained by the logarithms of the leakage current. Here, both the population average  $\mu_{\text{pop}}$  and the population variance  $\sigma_{\text{pop}}^2$  of the normal distribution are unknown. The theoretical distribution of the sample average follows a normal distribution,  $\bar{x} \sim N(\mu_{\text{pop}}, \sigma_{\text{pop}}^2/N)$ . Hence, when a 95% confidence interval is required for  $\bar{x}$ ,

$$\mu_{\text{pop}} - 1.96 \frac{\sigma_{\text{pop}}}{\sqrt{N}} < \bar{x} < \mu_{\text{pop}} + 1.96 \frac{\sigma_{\text{pop}}}{\sqrt{N}} \quad (\text{A} \cdot 1)$$

has to be satisfied. By substituting unknown variance  $\sigma_{\text{pop}}^2$  with unbiased sample variance  $u^2$ , Eq. (A·1) becomes

$$-1.96 \frac{u}{\sqrt{N}} \leq \bar{x} - \mu_{\text{pop}} \leq 1.96 \frac{u}{\sqrt{N}}. \quad (\text{A} \cdot 2)$$

This gives the estimation of difference from the true value,

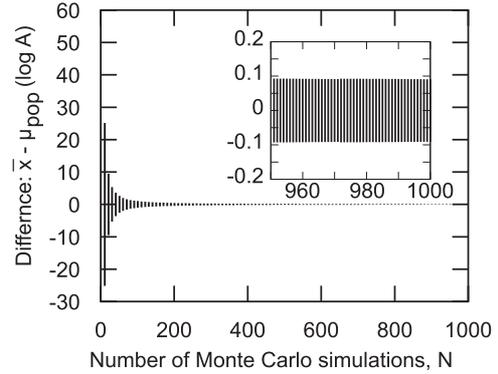


Fig. A.1 Ranges of 95% confidence interval of  $\bar{x} - \mu_{\text{pop}}$  by  $N$ .

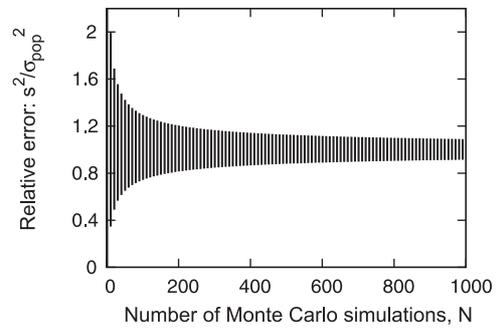


Fig. A.2 Ranges of 95% confidence interval of  $s^2/\sigma_{\text{pop}}^2$  by  $N$ .

$\bar{x} - \mu_{\text{pop}}$ . Figure A.1 shows the ranges of 95% confidence interval of the difference as a function of  $N$  for an inverter of a 65-nm process technology. We see that the confidence interval becomes smaller as we increase  $N$ . At  $N = 1000$ , 95% confidence interval is evaluated as  $|\bar{x} - \mu_{\text{pop}}| \leq 0.0907 \log A$ .

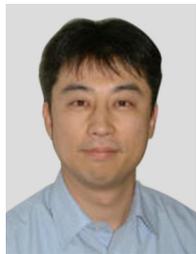
Next, we consider the distribution of sample variance,  $s^2$ . A relative error between  $s^2$  and  $\sigma_{\text{pop}}^2$  is evaluated by the ratio  $Ns^2/\sigma_{\text{pop}}^2$  that follows a  $\chi^2$  distribution with  $N - 1$  degrees of freedom. For example, 95% confidence interval is given as

$$\frac{X_{N-1}(0.025)}{N} \leq \frac{s^2}{\sigma_{\text{pop}}^2} \leq \frac{X_{N-1}(0.975)}{N}, \quad (\text{A} \cdot 3)$$

where  $X_{N-1}$  is a cumulative distribution function of the  $\chi^2$  distribution with  $N - 1$  degrees of freedom. Figure A.2 shows ranges of 95% confidence interval of  $s^2/\sigma_{\text{pop}}^2$ . At  $N = 1000$ , 95% confidence interval is evaluated as  $0.9142 \leq s^2/\sigma_{\text{pop}}^2 \leq 1.0895$ .



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