PAPER

State-Dependence of On-Chip Power Distribution Network Capacitance

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SUMMARY In this paper, the measurement of capacitance variation, of an on-chip power distribution network (PDN) due to the change of internal states of a CMOS logic circuit, is studied. A state-dependent PDN-capacitance model that explains measurement results will be also proposed. The model is composed of capacitance elements related to MOS transistors, signal and power supply wires, and substrate. Reflecting the changes of electrode potentials, the capacitance elements become state-dependent. The capacitive elements are then all connected in parallel between power supply and ground to form the proposed model. By using the proposed model, state-dependence of PDN-capacitances for different logic circuits are studied in detail. The change of PDN-capacitance exceeds 12% of its total capacitance in some cases, which corresponds to 6% shift of anti-resonance frequency. Consideration of the state-dependence is important for modeling the PDN-capacitance.

key words: *CMOS logic circuit, state-dependent capacitance model, capacitance measurement, PDN-capacitance, parasitic capacitance*

1. Introduction

Due to the recent trend of increasing clock-frequency and decreasing the supply voltage of electrical systems, simulation of the power distribution network (PDN) becomes particularly important to realize good system design. Supply-voltage fluctuation deteriorates signal integrity, which, in the worst scenario, may result in logic malfunctions [1]. Electro-magnetic interference caused by high-frequency currents in the PDN also deteriorates the quality of wireless communications [2].

In order to efficiently simulate the PDNs of electrical systems, the component models such as LSI, package, printed circuit board, etc., are required. Among others, the equivalent circuit model for the on-chip PDN is important because LSI is a source of current-noise. Thus, many studies have been conducted to obtain accurate equivalent circuit models for on-chip PDNs [3]–[5].

Figure 1 shows the representative equivalent circuit model, linear electrical circuit and current source (LECCS), which is composed of time-invariant linear components [3]. Using the LECCS model, electrical systems are simulated by combining LSI, package, and printed circuit board models. In those analyses, resonant and anti-resonant frequencies of total impedance are of particular interest. When the clock frequency of an LSI becomes close to those frequencies, a large voltage fluctuation may occur [6].

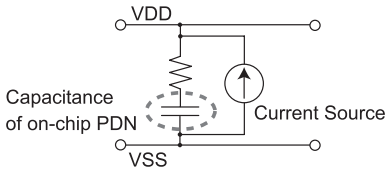

Fig. 1 LECCS model [3].

Here, the capacitance and resistance of the on-chip PDN is, in a strict sense, time-variant because connections of the gate, source, drain, and thus signal lines to the power supply/ground terminals become different according to the internal state of the circuit. Correspondingly, the anti-resonant frequency shifts as the change of logic-states. However, this state-dependence of the PDN-capacitance has not yet been studied.

In this paper, we pay careful attention to the capacitive component of the on-chip PDN model. Although other components, such as a resistor and current source are also very important for determining the characteristics of a PDN, we start by analyzing parasitic capacitance to understand the mechanism and the range of its variations. Our contribution is summarized as follows.

- We measure, for the first time, the variation of an on-chip PDN-capacitance caused by the state-change in a logic circuit.
- We propose a state-dependent capacitance model for on-chip PDNs and validate the model by comparing the measurement results.
- We conduct detailed component-analysis on the state-dependence of the PDN-capacitance by applying the proposed model to different logic circuits.

2. State-Dependent Capacitance Model for On-Chip PDNs

Capacitance-related components in a CMOS logic circuit

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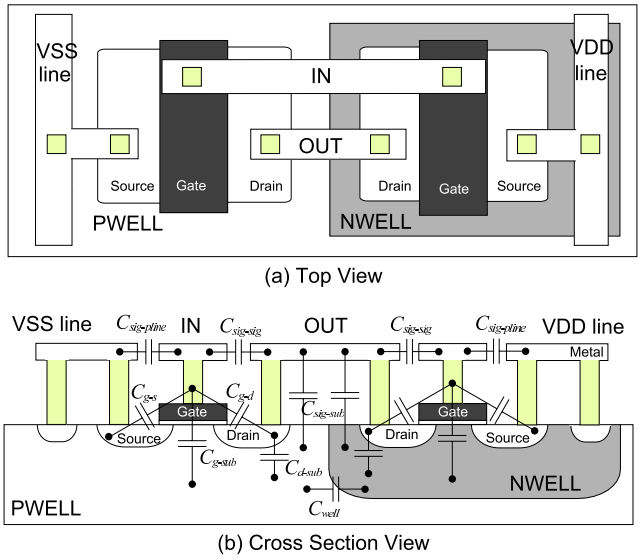


Fig. 2 Structure of an example standard cell (inverter).

are, in general, composed of MOS transistors, metal wires of power supplies and ground, n- and p-type wells, and substrate. Some components are directly connected to either a power supply (VDD) or ground (VSS), so their capacitance is insensitive to a logic state of the circuit. On the other hand, gate and drain electrodes of a transistor, and signal lines change their connection with VDD or VSS according to the state of the logic circuit. The PDN capacitance, or the capacitance between VDD and VSS, has to be calculated by not just as the summation of mutual capacitance of all components but considering its state-dependence. In contrast to the existing capacitance model [3], the salient feature of our model is to consider multiple capacitances which represent the state-dependence.

2.1 State-Dependent Capacitance Model for Standard Cell

At first, we look into a capacitance model for standard logic cells that are the fundamental components in cell-based logic circuits. Figure 2 depicts a simplified structure of an inverter cell.

Suppose that the input terminal "IN" in Fig. 2 is logical high, i.e. the voltage of "IN" is equal to VDD. The capacitance between the input and VSS wires $C_{\mathrm{sig-pline}}$ contributes to the total PDN-capacitance. Then again, when the terminal "IN" is logically low, the voltage of the input wire is equal to VSS. Capacitance $C_{\mathrm{sig-pline}}$ can be ignored because both ends of the capacitor are equi-potential and thus the stored charge becomes zero. In this manner, the capacitance between VDD and VSS of the standard cell changes according to its inputs.

Here, we assume the number of input pins of a cell as n. Because the total number of input combinations is 2^n, the PDN-capacitance of a standard cell takes different values of 2^n. For example, a two-input NAND cell has 2^2 PDN-capacitance values. A flip flop with n-inputs has 2^{n+1} PDN-capacitance values because the cell has an internal state in the circuit[†]. For example, a D-type flip flop having a D-input and a clock input has 2^3 PDN-capacitance values.

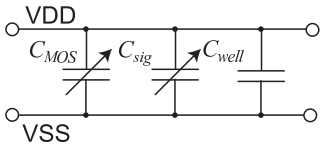


Fig. 3 State-dependent capacitance model for a standard cell.

From the structure of the standard cell, following capacitances can be ignored because they are generally very small.

- Capacitance between VDD and VSS wires.
- Capacitance between VDD wire and silicon surface, or between VSS wire and silicon surface, i.e., capacitances between VDD-nwell, VDD-pwell, VDD-substrate, VSS-nwell, VSS-pwell, and VSS-substrate.
- Capacitance between different MOS transistors.

Then, a capacitance model of a standard cell can be expressed by the following equations.

$$C_{\mathrm{scell}} = C_{\mathrm{MOS}} + C_{\mathrm{well}} + C_{\mathrm{sig}} \tag{1}$$

$$C_{\mathrm{MOS}} = \sum f(C_{\mathrm{g-s}}, C_{\mathrm{g-d}}, C_{\mathrm{g-sub}}, C_{\mathrm{d-sub}}) \tag{2}$$

$$C_{\mathrm{sig}} = \sum \{C_{\mathrm{sig-sig}} + C_{\mathrm{sig-pline}} + C_{\mathrm{sig-sub}}\} \tag{3}$$

Here, C_{scell} is the state-dependent capacitance model of a standard cell. C_{well} is the junction capacitance between n-well (p-well) and substrate. C_{MOS} is the effective parasitic capacitance related to MOS transistors, which is represented by a function of $C_{\mathrm{g-s}}$, $C_{\mathrm{g-d}}$, $C_{\mathrm{g-sub}}$, and $C_{\mathrm{d-sub}}$, the mutual capacitances between gate, source, drain and substrate, respectively. The connections of these capacitances are dependent on the connections between transistors, thus the function f does not have a simple analytical form. Determination of the C_{MOS} will be described in the later section.

Capacitances $C_{\mathrm{sig-sig}}$, $C_{\mathrm{sig-pline}}$, and $C_{\mathrm{sig-sub}}$ are defined in between signal wires, between a signal wire and power supply, and between a signal wire and substrate or n-well (p-well), respectively. Note here that the capacitances such as $C_{\mathrm{sig-sig}}$ are formed through the channels of transistors. Hence, the charge stored in the capacitor is dependent on the logic states, then the calculation of it requires a logic analysis such as the ones conducted in [7]. Figure 3 illustrates the capacitances of a standard cell. Because all components in Eqs. (2) and (3) change according to the voltages of each terminal, C_{MOS} and C_{sig} are state-dependent. Only C_{well} is independent of the logic states.

2.2 State-Dependent Capacitance Model for On-Chip PDN

In a similar manner, we then introduce a state-dependent capacitance model for on-chip PDN. A CMOS logic circuit is

[†]More generally, a flip flop with p internal states has 2^{n+p} different PDN-capacitances.

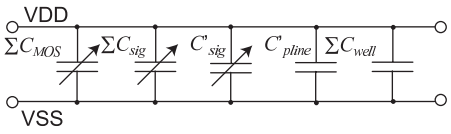


Fig. 4 State-dependent capacitance model for an on-chip PDN.

composed of standard cells, signal wires that connect standard cells, and power and ground-wires that connect supplies to the standard cells.

The total capacitance of the PDN is obtained as the sum of standard cell capacitances, and mutual capacitances between all combinations of standard cells, signal wires, power supply wires and substrate. Here, the vertical distance between wires in different layers are several times larger than the minimum space of the metal wires. Thus, in the rest of this paper, we ignore capacitances between the wires inside standard cells and the wires outside the standard cells, but those can be included for more accurate analysis.

The capacitance model of a chip can be expressed by the following equations.

$$C_{\text{total}} = \sum C_{\text{scell}} + C'_{\text{sig}} + C'_{\text{pline}} \tag{4}$$

$$C'_{\text{sig}} = \sum \{C'_{\text{sig-sig}} + C'_{\text{sig-pline}} + C'_{\text{sig-sub}}\} \tag{5}$$

$$C'_{\text{pline}} = \sum \{C'_{\text{pline-pline}} + C'_{\text{pline-sub}}\} \tag{6}$$

Here, C_{total} is the state-dependent capacitance model for the on-chip PDN. Prime "′" denotes that the capacitance is outside of the standard cells. $C'_{\text{pline-pline}}$ is the capacitance between VDD and VSS lines. $C'_{\text{pline-sub}}$ is the capacitance between VDD lines and substrate or that between VSS lines and substrate. $C'_{\text{sig-sig}}, C'_{\text{sig-pline}}, C'_{\text{sig-sub}}$ are the capacitances between a signal line and an another signal line, the one between a signal line and power line, and the one between a signal line and substrate, respectively.

As shown in Fig. 4, we combine the following capacitance components to define a chip-level state-dependent capacitance model. Each component is described as follows:

- $\sum C_{\text{MOS}}$: total capacitance of MOS transistors.
- $\sum C_{\text{sig}}$: total capacitance of signal lines in standard cells.
- $\sum C_{\text{well}}$: total capacitance of well-substrate junctions.
- C'_{sig}: capacitance between signal lines outside standard cells.
- C'_{pline}: capacitance of power lines outside standard cells.

Here, $\sum C_{\text{MOS}}$, $\sum C_{\text{sig}}$ and C'_{sig} are state-dependent. $\sum C_{\text{well}}$ and C'_{pline} are state-independent.

3. Measurement of State-Dependent Capacitance and Validation of the Proposed Model

In this section, through test-chip measurements, we experimentally show that the on-chip PDN-capacitance changes its value according to the change of logic states. By comparing the state-dependence of the measurements and the PDN-capacitance model, we also confirm the validity of the proposed state-dependent PDN-capacitance model. The following measurements are obtained from test-chips fabricated using a 180-nm, 6-metal layer CMOS process.

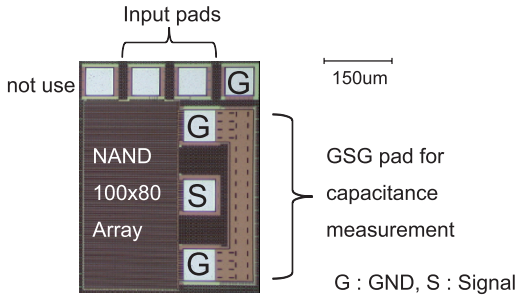


Fig. 5 Chip micrograph of a capacitance-measurement circuit for NAND cell.

3.1 State-Dependence of Standard Cell Capacitance

3.1.1 Test Chip Design and Measurement Procedure

The circuits consisting of eight different standard cells are implemented on a test chip for evaluating their state-dependence. Here, the standard cells include buffer (BUF), inverter (INV), 2-input NAND (NAND), 2-input NOR (NOR), 2-input exclusive NOR (XNOR), 4-input and-or-inverter (AOI), 4-input or-and-inverter (OAI), and scan D-flip flop (SDFF). A large number of standard cells are connected in parallel to form PDN-capacitance measurement circuits to enhance measurement accuracy. The number of the logic cells in a circuit is 1,200 to 12,000.

Figure 5 shows a chip micrograph of the capacitance-measurement circuit for the NAND cell. Output pins of all cells are left floating to avoid adding unnecessary capacitances. In order to eliminate parasitic capacitances of the wires connecting between standard cells, calibration circuits, in which the standard cells are completely removed but all the accessing wires to the array are preserved, are implemented for later compensation. The measurement sequence for an input state is defined as follows.

(1) Set input-pin voltages.
(2) Measure PDN-capacitance with the bias voltage of 1.8 V.
(3) Measure the parasitic capacitance of the calibration structure.
(4) Subtract the parasitic capacitance obtained in step (3) from the PDN-capacitance measured in step (2).
(5) Divide the capacitance by the number of the logic cells connected in parallel.

The state-dependent PDN-capacitance of the standard cells can be obtained by iterating the above sequence for all input-pin states. For the circuit of SDFF, the internal state-node voltage has been also set in step (1).

In this experiment, we measure input-impedance of the circuits' PDN by using a vector network analyzer. We approximate capacitance C through the following equation.

$$C = \frac{-1}{2\pi f \cdot \mathrm{Im}\{Z_m\}} \tag{7}$$

Here, Z_m is the measured PDN-impedance, $\mathrm{Im}\{x\}$ represents the imaginary part of x, and f is the frequency to define PDN-capacitance. In this experiment, the impedance at around 30 MHz is used for the calculation because capacitance becomes unstable below 10 MHz due to inaccuracies of the measurement due to highly reflective parameters. At around 100 MHz or above, the impedance of the capacitance and that of the resistance connected in series become close. Beyond that frequency, capacitance estimation through Eq. (7) also becomes inaccurate.

3.1.2 Model-Parameter Determination

State-dependent capacitance of a standard cell can be calculated through the frequency-domain analysis of a circuit simulator using parasitic-extracted netlist with different input-pin voltages. Following the proposed model equations, we determined capacitance components, C_{MOS}, C_{sig} and C_{well}, in a bottom-up manner.

Here, most extraction tools do not extract well–substrate junction capacitance C_{well}. Thus, this capacitance is determined by a separate measurement of a filler cell, which only contains a voltage biased well-junction layout, using a similar structure in Fig. 5. The measured capacitance C_{well} is adjusted for each standard cell according to its layout area. Also, most tools do not distinguish well potential, and thus capacitance between a signal line and substrate $C_{\mathrm{sig-sub}}$ is extracted as one capacitor. The tools consider n-well (p-well) and substrate to be equal potential, or AC ground. In this analysis, we assume that the half of extracted capacitance is connected to VDD, and the other half to VSS.

3.1.3 Comparison between Measurement and Analysis

Figure 6 compares the measured and calculated capacitances for all input states of the standard cells. Table 1 shows the correlation and average error. Good correlations larger than 0.98 and small maximum average errors of 6.7% are obtained.

From the above comparison, we can conclude that the PDN-capacitance varies according to the logic-state and that the proposed state-dependent capacitance model in Fig. 3 explains the state-dependence of the standard cells very well.

3.2 State-Dependence of On-Chip PDN-Capacitance

The similar measurement has been conducted on ISCAS 89 benchmark circuits, s1238 and s1488, to evaluate module- or chip-level state-dependence of the PDN-capacitance. Table 2 shows the specifications of the circuits implemented

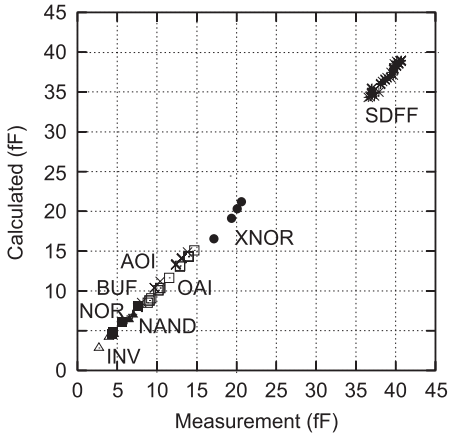


Fig. 6 Correlation between measured and calculated state-dependent capacitances.

Table 1 Correlation coefficients and average error between measured and modeled capacitance.

	number of states	correlation	average error[%]
BUF	2	-	2.0
AOI	16	1.00	6.7
SDFF	32	0.98	−5.5
OAI	16	1.00	0.6
NOR	4	1.00	6.6
XNOR	4	1.00	0.1
INV	2	-	5.5
NAND	4	1.00	−2.1

Table 2 Circuit profiles of s1238 and s1488.

	numbers			
	input pins	Flip-flops	standard cell	layout area (μm)
s1238	14	19	306	110.88 × 118.34
s1488	8	7	294	100.80 × 107.12

[8]. Comparison with the proposed state-dependent capacitance model in Fig. 4 is also carried out.

3.2.1 Test Chip Design and Measurement Procedure

Figure 8 shows the micrograph of the test chip for s1238. The input-pin voltages are set through a shift register. Scan chain for LSI test is used to directly determine the internal state of all flip-flops. The pads for the scan-chain are located at the bottom left. The state-dependent capacitance of on-chip PDN can be obtained by iterating the following procedure for arbitrary states.

(1) Set the all states of scan flip-flops.
(2) Set the input pin voltages.
(3) Measure the capacitance from GSG pads with 1.8 V bias voltage.

In this experiment, the vector network analyzer and Eq. (7) are used again. Figure 7 shows the capacitance measurement results of s1488 for 100 random internal states. Similar to the measurements of the standard logic cells, we choose

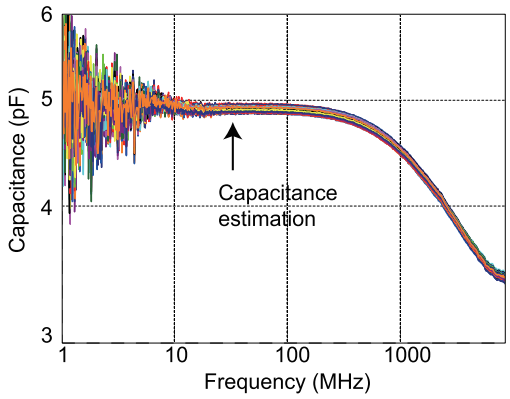


Fig. 7 Capacitance measurement results of s1488.

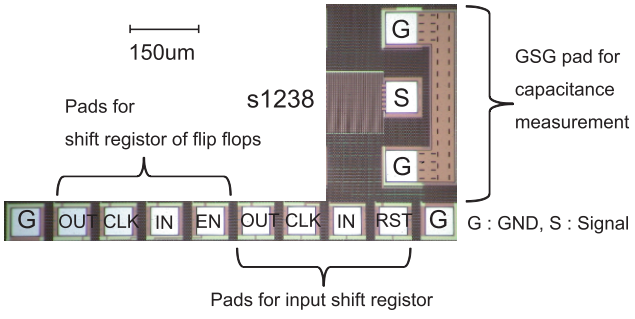


Fig. 8 Chip micrograph of s1238.

30 MHz as the extraction frequency.

In this experiment, we measure the capacitance when the clock is inactive. However, considering the actual operation of LSIs, the PDN-capacitance at the time of clock switching is interested. Suitability to apply the proposed capacitance model to the clock-switching case is one of our future works.

3.2.2 Model-Parameter Determination

State-dependent capacitance of a logic circuit can also be calculated by a circuit simulator by determining voltages of both input pins and the state nodes of flip-flops. However, the capacity of the circuit simulator is limited, and it is too slow to compute capacitances with various state combinations. Hence, in this paper, a lookup-table based capacitance calculation tool is utilized [9], [10]. The accuracy of the tool has been confirmed by the comparison with SPICE simulations. In order to concentrate on the objective of this paper, we limit ourselves to a brief introduction of the tool.

In the lookup-table based tool, we first prepare a lookup table for the capacitance components — $C_{\mathrm{MOS}}, C_{\mathrm{sig}}, C'_{\mathrm{sig}}, C_{\mathrm{pline}}$, and C_{well} of the proposed model shown in Fig. 4. Then, we obtain the logic states of all nodes in the target circuit through a logic simulation. Finally, by using the node voltages at the inputs for the combinational circuits, we add the capacitances of standard cells referring to the lookup tables. By using the lookup-table based tool,

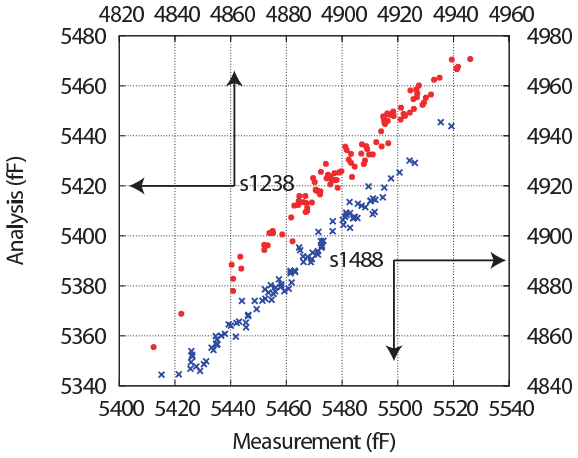


Fig. 9 Comparison of the measured and calculated capacitance of on-chip PDN.

Table 3 Correlation between measured and calculated state-dependent capacitances for circuits s1238 and s1488.

	correlation	average error(%)
s1238	0.988	−1.67
s1488	0.992	0.07

we can quickly obtain individual capacitance components of the target circuits.

3.2.3 Comparison between Measurement and Analysis

Figure 9 compares the measured and the calculated capacitances for 100 random states. Both the left and bottom axes are for the capacitances of s1238, and both the right and top axes represent the one of s1488. Table 3 shows the correlation coefficients and average error. Good correlation of about 0.99 and small average error within 2% has been obtained. The proposed state-dependent capacitance model in Fig. 4 again explains the state-dependence of the on-chip PDN-capacitance. By using the proposed model, we can investigate the state-dependence of the PDN-capacitance for any logic circuits.

We notice in Fig. 9 that errors in the absolute value exist in both circuits. The sources of the error have not yet been completely understood, but well-junction capacitance should be the primary cause. As stated earlier, we have characterized the well-junction capacitance using a dedicated test structure that includes well-junctions forming a rectangular boundary. In the layouts of s1238 and s1488, various logic cells are used. With the wells of different logic cells combined, the shape of the well boundary is not a simple rectangle but becomes more complex polygon because the well heights in different logic cells are not necessarily equal. With the changes of the arrangement of the standard logic cells, well boundary will change, which is not considered in the model calculation.

Note here that the well-junction capacitance is independent of the internal state of the circuit once the cell placement is fixed. Hence, inaccuracies of the well-junction ca-

pacitance does not affect the correlation between the model and the measurement. This is also confirmed by the fact that the capacitance ranges match well in both circuits. More accurate extraction of the layout-dependent well-junction capacitance is also one of our future works.

We would like to also mention that the precision of the measurement in Fig. 9 may not be fully sufficient. At 30 MHz, capacitances of 5400 fF and 5520 fF are 960 Ω and 980 Ω, respectively. These differences can be distinguishable using a vector network analyzer of 50 Ω reference impedance, so the overall correlation between the model and the measurement is correct. However, the capacitance differences of different internal states are about 1 fF. This capacitance corresponds to 0.2 Ω, which may not be completely repeatable although the measurements are conducted in a constant temperature in a short time. Because of this possible error, correlations may be slightly different.

4. Analysis of State-Dependence for On-Chip PDN Capacitance

In this section, we analyze the variation and components of state-dependent PDN capacitance in more detail by using the table-lookup based tool [10].

Table 4 shows the specification of benchmark circuits, s510 and s15850. We first estimate the range of capacitance variation of the on-chip PDN, and then examine its effect on the anti-resonance frequency. Then, to understand the source of the variation, we divide the capacitance into the components of the proposed model in Fig. 4.

4.1 The Range of Capacitance Variation

The number of states of s1488 is 2^{15}. Capacitances of s1488 can be exhaustively calculated to obtain the maximum and the minimum values. Other circuits, s510, s1238 and s15850, have too large number of states to thoroughly calculate capacitances of all states. For those circuits, we estimate the maximum and the minimum capacitances from the calculations of 10^5 random states.

Figure 10 shows the histograms of capacitance distribution. The circuits s510, s1238 and s1488 have distributions similar to Gaussian, while s15850 has two peaks. An analysis of the states revealed that the left and the right peaks correspond to the clock states "high" and "low," respectively. This is because the ratio of the number of flip-flops to that of total standard cells is about 20.8% in s15850, which is much larger than the other circuits. The flip-flop ratios for s410, s1238, and s1488 are 5.3%, 6.2%, and 2.4%, respectively. According to the above observation, we estimate the maximum and the minimum capacitance for s510 and s1238 by assuming their distributions as Gaussian. For s15850, the distributions are treated as two separate Gaussian distributions. The maximum and minimum capacitance $C_{\max}$ and $C_{\min}$ for n' states can be estimated by the following equation,

$$C_{\max}, C_{\min} = \mu \pm \sigma\sqrt{2(n'\log(2) - \log(\sigma\sqrt{2\pi}))}. \quad (8)$$

Here, μ and σ are the average and the standard deviation of the Gaussian distribution, respectively.

Table 5 show estimations of $C_{\max}$ and $C_{\min}$. With the Gaussian assumption, the capacitance range becomes wider as the number of states increases. The PDN capacitance can vary by about 12% in the case of s15850. This means that designers should consider the variation of resonance frequency of 6%, or more. Here, the anti-resonance frequency of a circuit made of an inductance L and a capacitance C in parallel is determined by $1/2\pi\sqrt{LC}$.

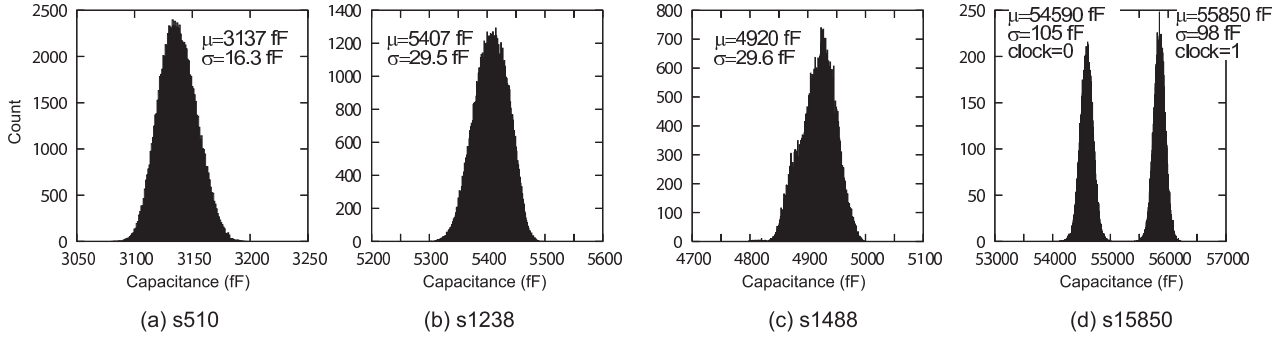
Commercial logic circuits often contain designed de-

Table 4 Profiles of the benchmark circuits.

	numbers			
	input pins	Flip-flops	standard cell	layout area (μm)
s510	19	7	133	95.76 × 100.52
s15850	77	535	2574	362.88 × 262.30

Table 5 Estimated maximum and minimum capacitance, $C_{\max}$ and $C_{\min}$.

	s510	s1238	s1488	s15850
μ (fF)	3137	5407	49200	55219
σ (fF)	16.3	29.5	29.6	98/105
(clock=0/clock=1)				
n'	26	33	15	612
$C_{\min}$ (fF)	3050	5230	4800	51500
$C_{\max}$ (fF)	3220	5590	5000	58500
$(C_{\max} - C_{\min})/\mu$(%)	5.5	6.7	4.1	12.7



(a) s510 (b) s1238 (c) s1488 (d) s15850

Fig. 10 Distribution of state-dependent PDN capacitance.

coupling capacitors and SRAM memory. Whereas the number of states is much larger than the logic circuits in our examples. Decoupling capacitor reduces the relative variation due to state-independence. SRAM cells are also supposed to reduce the relative variation because of the good symmetric property. On the other hand, under the Gaussian assumption, large number of states increase variation range. More detailed analysis of these effects on actual large scale logic circuit is necessary, and this is also in our future work list.

4.2 Capacitance Component Breakdown

With the aid of the lookup-table based tool [10], PDN capacitance can be separated into different components. Figure 11 shows how the total capacitance is made up. In the figure, numbers are the average capacitance of each component. The standard deviations are separately calculated for each component. The standard deviation for s15850 is the one when the clock input is logical "low."

The capacitance of signal lines outside standard cell C'_{sig} becomes a major component as the size of the circuit becomes large. In contrast, well junction capacitance C_{well} occupies smaller percentage for larger circuit. This can be explained by the Rent's rule [11], which states that the total length of signal lines connecting between standard cells increases exponentially as the increase of the number of terminals. The increase in the length of signal wire increases total capacitance.

The standard deviation of C'_{sig} also becomes rapidly large as the increase of the size of the circuit compared with that of the MOS transistors' (C_{MOS}). This is interesting because the average contribution of C_{MOS} is larger than that of C'_{sig}. The large standard deviation of C'_{sig} can be explained as follows. Both p-type and n-type transistors are used in CMOS standard cells. Capacitance variation is caused by the difference between parasitic capacitances between different transistors, which are always placed in a pair in a close proximity. On the other hand, signal lines can be routed anywhere on a chip so the parasitic capacitance to VDD and VSS tend to be unbalanced. Therefore, C'_{sig} can have larger capacitance variation even if the average capacitance is smaller than C_{MOS}. Considering the Rent's rule and the potential large variation of C'_{sig}, it is expected that the largest cause of variation would be signal lines that connect the standard cells for large logic circuits.

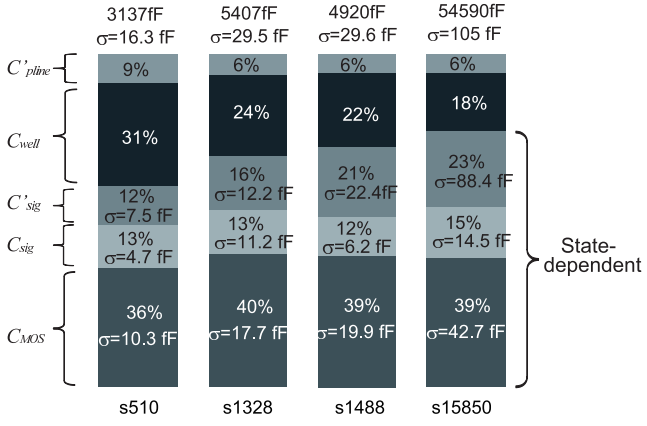


Fig. 11 Comparison of average and standard deviation of capacitance components.

5. Conclusion

The variation of on-chip PDN capacitance due to the state-dependence of CMOS logic circuit has been experimentally confirmed for the first time. The model that explains measured capacitance change has also been presented. The proposed capacitance model has five components, three of those are state-dependent and other two are state-independent. Analysis using the proposed model revealed that the PDN-capacitance of a circuit may vary more than 12%. The change of the capacitance can change anti-resonant frequency, which is one of the most important design parameters of the power supplies, by a maximum of 6%. By separating total PDN capacitance into the five components, the major cause of capacitance variation and the trend of capacitance variation has been explained. Although enhancement of the PDN-model is currently limited to capacitance only, we believe this is a necessary and important first step to improve overall accuracy of PDN-models.

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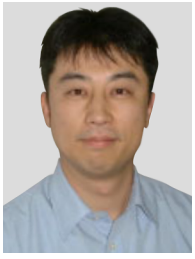

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