Reduction of interface state density in SiC (0001) MOS structures by post-oxidation Ar annealing at high temperature

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Reduction of interface state density in SiC (0001) MOS structures by post-oxidation Ar annealing at high temperature

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We found that post-oxidation Ar annealing at high temperature is effective in reducing the interface state density (D_{it}) near the conduction band edge (E_C) of SiC (0001) MOS structures. The D_{it} reduction effect is comparable to that of nitridation process (annealing in nitric oxide (NO)) which has been a standard in SiC MOS technologies, without introducing any foreign atoms into the interface/oxide. The generation of fast interface states, which have been pointed out as a problem of nitridation process, is suppressed in the case of Ar annealing. In the proposed method, the final D_{it} values are mainly determined by the Ar annealing temperature rather than the initial oxidation temperature. The D_{it} values are not sensitive to the cooling speed, which means that rapid cooling is not necessary in the proposed method. [http://dx.doi.org/10.1063/1.4980024]

Silicon Carbide (SiC) has been regarded as a candidate material for next-generation power devices, due to its superior material properties such as a wide bandgap, high critical electric field, and low intrinsic carrier concentration.[1,2] SiC metal-oxide-semiconductor field effect transistors (MOSFETs) are expected to exceed the Silicon (Si)-based power devices operating at relatively high voltages (0.6 -10 kV), in terms of on-state resistance, breakdown voltage, and switching loss.

SiC MOSFETs have, however, suffered from their low channel mobility (μ_{ch}) caused by the extremely high interface state density (D_{it}) of SiC/SiO_2 systems (~10^{13} $cm^{-2}eV^{-1}$).[2–5] Both the electron trapping effect by the interface states, and the Coulomb scattering effect from the trapped electrons contribute to the degradation of the field-effect mobility.[3–5]

Although the physical origin of the interface states is not clear, several passivation methods were found to improve the interface quality and/or channel mobility of the MOSFETs. For instance, interface nitridation (annealing in nitric oxide (NO[6–10])) and $POCl_3$ annealing (annealing in $POCl_3$, O_2, and N_2 gas mixture[11–13]) are effective both in reducing the D_{it} and in improving the channel mobility of MOSFETs. These methods are based on incorporation of foreign atoms into the interface (and/or oxide), and thus there remains a concern about the extrinsic defect generation and the degradation of oxide's reliability (such as breakdown field and threshold voltage instability). In the case of nitridation process, for example, generation of fast interface states[8] and oxide hole traps[9] has been reported. For $POCl_3$ annealing, generation of oxide electron (and hole) traps[12] was indicated.

It is more desirable if high-quality interface is obtainable without introducing foreign atoms into the interface/oxide. Recently, several challenges have been performed to improve the interface quality only by devising the oxidation process. For instance, super-high-temperature oxidation (> 1450°C)[14] and thin (~ 15 nm) oxidation with rapid cooling (> 600°C/min)[15] have been reported. Although these processes are effective in reducing the D_{it} to some extent, the improvement of channel mobility is not sufficient in the present stage. In Si MOS technology, the major origin of interface states was pointed

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out to be the P_b center (Si dangling bonds[16,17]), which can be passivated by hydrogen annealing.[16,17] It is important to collect more experimental facts regarding the interface defects of SiO_2/SiC in order to clarify the microscopic picture of SiC MOS systems.

In this study, we report that the post-oxidation (high-purity) Ar annealing is effective in reducing D_{it} near E_C. The results of several investigations such as the initial oxidation temperature dependence and cooling rate dependence are shown. Based on the results, the mechanism of the observed D_{it} reduction is discussed.

The samples employed in this study were MOS capacitors fabricated on 4H-SiC (0001) 4° off-axis epilayers. The doping density of the n-type epilayer was about 1×10^{16} cm^{-3}, and the oxide thickness was in the range of 90-110 nm. As a process flow, we first performed dry oxidation at either 1150°C for 20 h, or at 1300°C for 40 min or 1h 20 min. Subsequently, Ar annealing at either 1300°C or 1500°C was carried out for 1 - 10 min. We used two types of furnaces for Ar annealing, which were both different from the oxidation furnace; one was a resistive-heating furnace with a standard cooling rate (< 70°C/min), and another was an RF- induction heating furnace with a rapid cooling rate (> 600°C/min). We note that the measured oxygen concentration inside the resistive heating furnace was very low (< 1 ppm) during the Ar annealing process, which is very important to avoid the unwanted oxidation of SiC or sublimation of SiO_2 (via active oxidation) during the process. The diameter of circular Al electrodes was about 500 μm. In the capacitance-voltage (C-V) measurements, the frequency was varied in the range from quasi-static (QS) to 100 MHz, and the voltage sweep rate was about 0.1 V/s. In the conductance measurement, the frequency was varied from 1 kHz to 100 MHz.

Figure 1 shows the C-V characteristics obtained from the MOS capacitors treated in Ar at different annealing temperature. The annealing was performed in the resistive-heating furnace with a standard cooling rate (< 70°C/min). In Fig.1, the calculated theoretical C-V curve is also shown for comparison, and the initial oxidation before the Ar annealing was carried out at 1150°C. Both the C-V stretch-out and the positive voltage shift are observed in the as-oxidized sample, which are caused by the considerable amount of acceptor-like interface states near E_C. The stretch-out and voltage shift are reduced to some extent by 1300°C annealing. After high-temperature annealing at 1500°C, the C-V curve looks similar to the theoretical one, except for the negative voltage shift (corresponding to the positive effective fixed charge of 9.1×10^{11} cm^{-2}). Note that the effective oxide thickness (EOT) did not change with the annealing, which means that the additional oxidation or oxide sublimation was suppressed during the Ar annealing at 1500°C. The Ar annealing did not affect the dielectric properties of the oxide, and the breakdown field was about 9.2 $MVcm^{-1}$ (not shown).

Figures 2(a) and (b) depict the interface state density of Ar-annealed MOS structures evaluated by a conventional high(1 MHz)-low method.[17] In Fig.2(a), the results with different annealing furnaces owning different cooling rates (either < 70°C/min or > 600°C/min) are compared (the initial oxidation

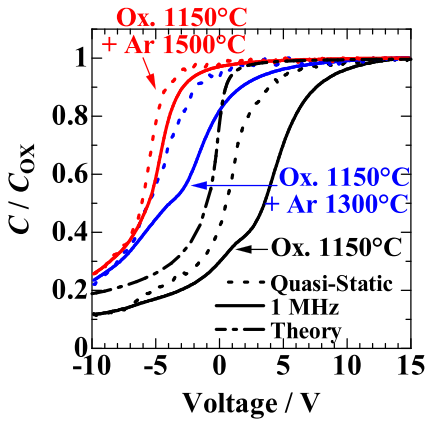

FIG. 1. C-V characteristics of the Ar-annealed MOS capacitors fabricated on 4H-SiC (0001). The initial oxidation temperature was fixed at 1150°C and the Ar annealing temperature was varied from 1300°C to 1500°C. The Ar annealing was carried out in the resistive-heating furnace with a standard cooling rate (< 70°C/min).

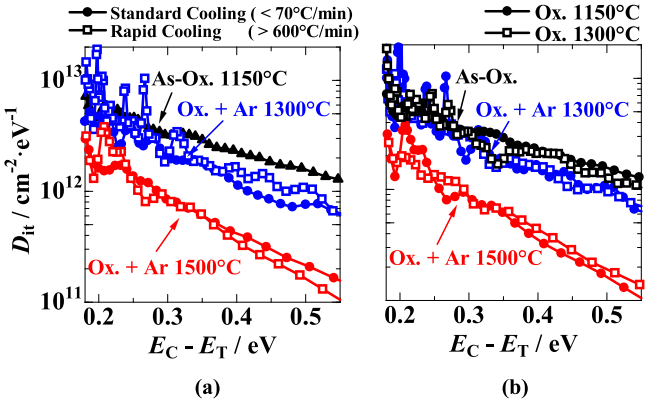

FIG. 2. Interface state density of Ar-annealed MOS structures evaluated by conventional high(1 MHz)-low method ((a) with different annealing furnaces owning different cooling rate (either < 70°C/min or > 600°C/min) where the initial oxidation temperature was fixed at 1150°C, (b) with different initial oxidation temperature (either 1150°C or 1300°C) where annealing was performed in the RF- induction heating furnace with a rapid cooling rate (> 600°C/min)).

temperature was fixed at 1150°C). The results with different initial oxidation temperature (either 1150°C or 1300°C) are compared in Fig.2(b) (the annealing was performed in the RF- induction heating furnace with a rapid cooling rate (> 600°C/min)). Note that in the high(1 MHz)-low method, only traps with relatively slow response (< 1 MHz) are detected.[18] As shown in Figs.2(a) and (b), D_{it} is reduced by high-temperature Ar annealing at 1500°C, which is consistent with the *C-V* behavior (shown in Fig.1). We can see that the D_{it} values are not sensitive to the cooling speed in Fig.2(a). Such feature is different from the method based on high-temperature oxidation where it is claimed that rapid cooling is important in order to avoid the unwanted low-temperature oxidation during the cooling process.[14] In Fig.2(b), the D_{it} values are not affected by the initial oxidation temperature (1150°C or 1300°C), and almost uniquely determined by the annealing temperature.

The effect of "re-annealing" was investigated and the D_{it} distributions are shown in Fig.3. Here, the sample was once annealed at high temperature of 1500°C, and subsequently annealed at a lower temperature of 1300°C. The annealing was performed in the furnace with a rapid cooling rate (> 600°C/min). In Fig.3, the D_{it} was evaluated by the high(1 MHz)-low method as in the case of Figs.2(a) and (b). As shown in Fig.3, the effect of re-annealing is very small (once the D_{it} is reduced by high-temperature annealing, it does not increase by subsequent annealing at low temperature).

Here, we discuss a candidate of interface defects in SiC MOS structures which may be substantially reduced by the present thermal effect. Carbon-associated byproducts have been widely argued as a possible candidate for interface defects in SiC MOS structures.[2,5,15,19,20] From ab-initio calculations, possible structure of carbon-related interface defects at the initial stage of oxidation

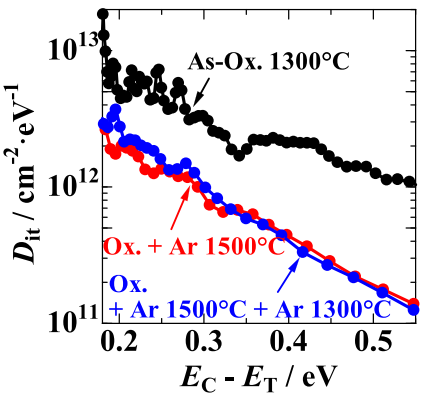

FIG. 3. Interface state density of Ar-annealed SiC MOS structures evaluated by a conventional high(1 MHz)-low method. The effect of "re-annealing" (after high temperature annealing of 1500°C, subsequent annealing is carried out at low temperature of 1300°C) is investigated.

was recently predicted.[20] The calculation indicates that carbon nanoclusters creating states near E_C (Fig.15(a) in Ref. 20) are dissociated into CO molecules by "pure" thermal annealing (without intervention of O_2)[20] to diffuse out of the system. However, further studies are required to clarify the physical origin of interface defects.

In Fig.4, the D_{it} distributions of the MOS structures evaluated by either high(100 MHz)-low method or C-ψ_S method[21] are shown. In these methods, the upper limitation of response time for detectable states is sufficiently high (or even no limitation in the case of C-ψ_S[21]) for SiC MOS structures, and most of the states existing in the given energy range near E_C (E_C–0.18 eV - E_C–0.55 eV) are detectable. The results for NO-annealed MOS structures (oxidized at 1300°C and annealed in NO at 1250°C; the sample details are shown elsewhere[22]) are also shown for comparison. As shown in Fig.4, the D_{it} reduction effect by high-temperature (1500°C) Ar annealing is comparable to that of nitridation process (annealing in NO), a standard in SiC MOS technologies, without introducing any foreign atoms into the interface/oxide.

Conductance signals (normalized by the electrode area) of MOS structures are shown in Fig.5 for (a) as-oxidized (1300°C), (b) oxidized + Ar annealed (1500°C), and (c) oxidized + NO annealed (1250°C) samples.[22] The signals were taken from the energy range of E_C–0.30 eV - E_C–0.51 eV. When we compare Figs.5(a) and (c), the reduction of slow states is achieved with NO annealing. However, generation of fast states responding to frequency over 100 MHz occurs at the same time by the NO annealing.[8] In the case of high-temperature Ar-annealing shown in Fig.5(b), reduction of slow states is not as sufficient as in the case of the NO annealed sample, but the generation of fast interface states is suppressed. Hence, when we compare the sum of interface states (slow + fast states), the D_{it} reduction effect of high-temperature Ar annealing is comparable to that of NO annealing, as shown in Fig.4.

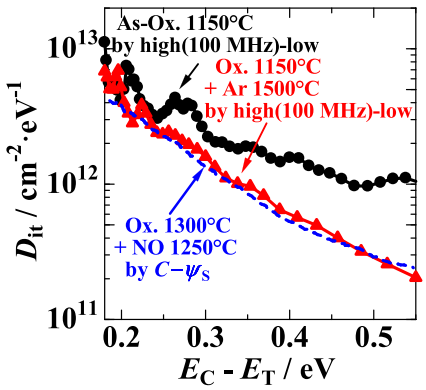

FIG. 4. Interface state density of SiC MOS structures evaluated by either high(100 MHz)-low method or C-ψ_S method 21. The results for NO-annealed MOS structures (oxidized at 1300°C and NO annealed at 1250°C; the sample details are described elsewhere 22) are also shown for comparison.

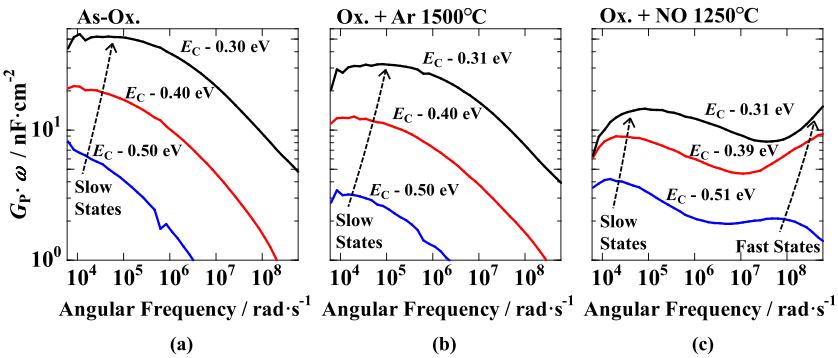

FIG. 5. Conductance signals (normalized by the electrode area) of SiC MOS structures. (a) As-oxidized (1300°C), (b) oxidized + Ar annealed (1500°C), and (c) oxidized + NO annealed (1250°C) samples.

In conclusion, we found that post-oxidation Ar annealing at high temperature is effective in reducing the interface state density (D_{it}) near the conduction band edge (E_C) of SiC (0001) MOS structures. The D_{it} reduction effect is comparable to that of nitridation process which has been a standard in SiC MOS technologies, without introducing any foreign atoms into the interface/oxide. This is attributable to the fact that the generation of fast states caused by nitridation is suppressed in the case of Ar annealing. The final D_{it} values are mainly determined by the Ar annealing temperature rather than the initial oxidation temperature. The D_{it} values are not sensitive to the cooling speed (< 70°C/min or > 600°C/min), which means that rapid cooling is not necessary in the proposed method.

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