Remarkable lattice recovery and low sheet resistance of phosphorus-implanted 4H–SiC $(11\bar{2}0)$

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High-dose ion implantation of phosphorus into 4H–SiC has been investigated. Phosphorus ion implantation with a 1×10^{16} cm^{-2} dose at 800 °C into 4H–SiC (0001) has resulted in a sheet resistance of 80 $\Omega/\square$ after annealing at 1700 °C. A similar sheet resistance of 110 $\Omega/\square$ was achieved even by room-temperature implantation when 4H–SiC $(11\bar{2}0)$ was employed, owing to excellent recrystallization of this face revealed by Rutherford backscattering channeling spectroscopy. The sheet resistance could be further reduced down to 27 $\Omega/\square$ by 800 °C implantation into 4H–SiC $(11\bar{2}0)$ followed by annealing at 1700 °C. 4H–SiC $(11\bar{2}0)$ showed a very flat surface after annealing. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1432745]

Silicon carbide (SiC) is an attractive material for high-power, high-temperature, and high-frequency devices owing to its superior properties such as wide band-gap, high breakdown field, high thermal conductivity, and high saturation electron drift velocity.[1] In SiC, successful selective doping can be made only by ion implantation, because the low diffusion coefficients of impurities in SiC make a diffusion process with proper masks very difficult.[2] To form selective n^+ regions in SiC, phosphorus ion (P^+) and nitrogen ion (N^+) implantations are commonly employed. Recently P^+ implantation has attracted increasing attention to obtain lower sheet resistances.[3–5] Minimum sheet resistances of P^+- and N^+-implanted regions ever reported were 51 $\Omega/\square$ (600 °C implanted and 1700 °C annealed)[5] and 290 $\Omega/\square$ (700 °C implanted and 1600 °C annealed),[6] respectively. P^+ implantation at an elevated temperature followed by annealing at a high temperature above 1600 °C is effective to reduce sheet resistances.[5] However, a recent report has shown that when activation annealing is performed at a high temperature in Ar, considerable roughening and macrostep formation are observed, which may adversely affect the mobility of inversion region in double implanted field-effect metal-oxide-transistors (DIMOSFETs) and specific on-resistances of many SiC devices.[7] To establish an implantation process similar to Si technology, the major challenges include successful implantation at room temperature (RT), reduction of annealing temperature, and keeping surface flatness during annealing processes. In this letter, the authors demonstrate that the use of 4H–SiC $(11\bar{2}0)$ may be a solution to meet these requirements.

The starting substrates were *n*-type 8° off-axis 4H– SiC (0001) from Cree, Inc. and on-axis 4H–SiC $(11\bar{2}0)$ from Nippon Steel, Co. Boron-doped (*p*-type) 4H–SiC epilayers grown by chemical vapor deposition (CVD)[1] in the authors' group were used in the present study. The net acceptor concentrations of (0001) and $(11\bar{2}0)$ were $6-10\times10^{16}$ and $0.8-2\times10^{16}$ cm^{-3}, respectively. Multiple implantation of P^+ was carried out at either RT or 800 °C to obtain a 0.45-

μm-deep box profile of P (energy: 10–360 keV, total dose: 1×10^{16} cm^{-2}). The implant energies and dose ratios were 360, 260, 180, 120, 80, 40, 20, 10 keV and 0.28, 0.20, 0.20, 0.12, 0.10, 0.06, 0.02, 0.02, respectively. Postimplantation annealing was performed in a CVD reactor at 800–1700 °C for 30 min in pure Ar ambience. The electrical properties of implanted regions were characterized by Hall effect measurements at RT using the van der Pauw configuration. For ohmic contacts, Al/Ti or Ni was evaporated on the surface through a metal mask followed by annealing at 900 °C in Ar. To avoid leakage current along the sample edges, mesa structures were fabricated by reactive ion etching. Implantation-induced damages were analyzed by Rutherford backscattering channeling spectroscopy (RBS) with a 2.0 MeV He^{2+} primary beam and a scattering angle of 170°.

Figure 1 shows the measured sheet resistance of P^+-implanted regions as a function of annealing temperature. The implantation was done with a dose of 1×10^{16} cm^{-2} at RT or 800 °C. In the case of 800 °C implantation into 4H–SiC (0001), the sheet resistance takes a minimum value of 80 $\Omega/\square$ after 1700 °C annealing, although the sheet resistance is 180 $\Omega/\square$ for the RT-implanted sample. These results suggest
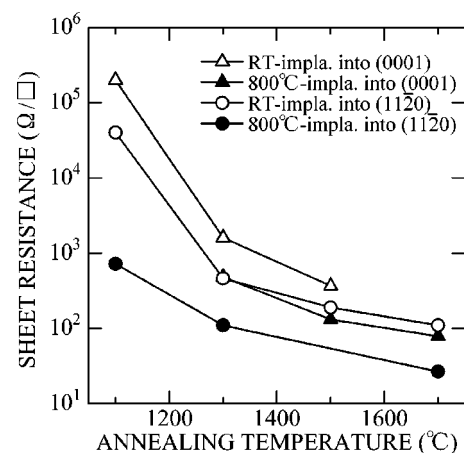

FIG. 1. Dependence of sheet resistance on annealing temperature for P^+ implanted 4H–SiC (0001) and $(11\bar{2}0)$.
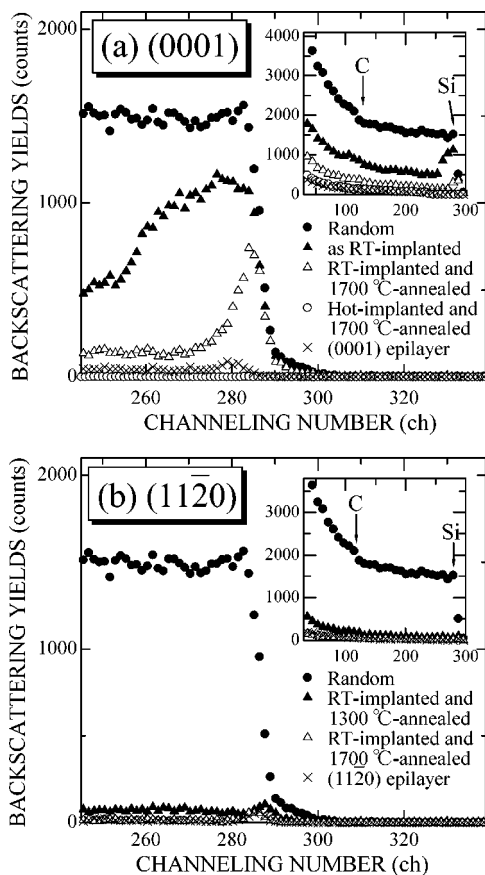

FIG. 2. RBS spectra of 4H–SiC before and after annealing. P^+ implantation was done at RT or 800 °C: (a) 4H–SiC (0001); (b) 4H–SiC (11$\bar{2}$0). The spectrum of a virgin sample is also shown as reference.

that P^+ implantation at elevated temperatures followed by high-temperature annealing is effective to form a heavily doped n^+ region with a low sheet resistance as in previous reports.[3–5] However, the sheet resistances increase considerably with decreasing annealing temperature regardless of implantation temperatures. On the other hand, when 4H–SiC (11$\bar{2}$0) epilayers were employed, a low sheet resistance of 110 $\Omega/\square$ has been achieved even by RT implantation followed by annealing at 1700 °C. A reasonable sheet resistance of 460 $\Omega/\square$ has been obtained by RT implantation followed by low-temperature annealing at 1300 °C. 800 °C implantation into 4H–SiC (11$\bar{2}$0) has resulted in a minimum sheet resistance of 27 $\Omega/\square$ after annealing at 1700 °C. To our knowledge, this is the lowest sheet resistance of implanted SiC ever reported. Hot implantation at 800 °C into 4H–SiC (11$\bar{2}$0) is effective to reduce annealing temperature. A low sheet resistance of 110 $\Omega/\square$ has been obtained even by 1300 °C annealing.

It is important to understand, from the view point of lattice damages, the reasons why RT implantation of P^+ into 4H–SiC (11$\bar{2}$0) brings a low sheet resistance while hot implantation is generally required in the case of 4H–SiC (0001). Figure 2(a) shows the aligned spectra of as-implanted and 1700 °C-annealed 4H–SiC (0001) samples. The aligned yields of the damaged region (channel number: 230–280) are close to the random yields in the case of RT implantation without annealing. Although the yields decrease by annealing at 1700 °C, severe damages near the surface
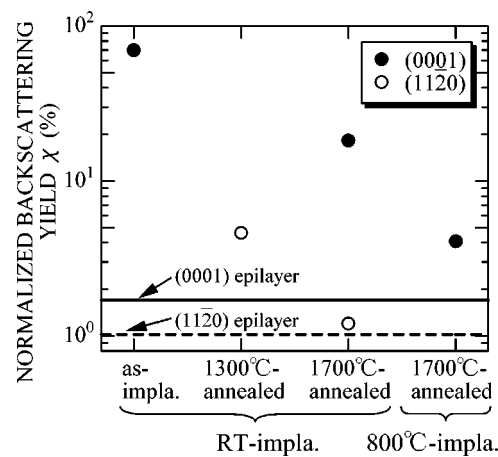

FIG. 3. Dependence of normalized backscattering yeild (χ) of 4H–SiC before and after annealing. P^+ implantation was done at RT or 800 °C.

still remain as reported by many groups. In contrast, the damage is considerably decreased for the 800 °C implanted and 1700 °C annealed sample. Figure 2(b) shows the aligned spectra of RT-implanted 4H–SiC (11$\bar{2}$0) samples followed by annealing at 1300 and 1700 °C. Implantation-induced damages are considerably decreased even by RT implantation followed by annealing at 1300 °C in the case of 4H–SiC (11$\bar{2}$0). The damages are reduced down to the virgin (epilayer) level by RT implantation and 1700 °C annealing. The figure demonstrates that implantation-induced damages are reduced down to the virgin (epilayer) level even by RT implantation followed by annealing at 1700 °C in the case of 4H–SiC (11$\bar{2}$0).

For the quantitative analysis of implantation-induced damages, the normalized backscattering yield χ was defined as the ratio of the aligned yields in the damaged region and the random yield. Figure 3 shows the normalized yield χ, for as-implanted, 1300, and 1700 °C-annealed samples. In the case of RT-implantation into 4H–SiC (0001), the χ value before annealing is higher than 70%, suggesting the formation of nearly amorphous region, and severe damages remained even after annealing at 1700 °C ($\chi = 18\%$). Implantation at 800 °C resulted in much smaller χ values of 4% after annealing at 1700 °C. These results are consistent with previous reports in which N^+ implantation into 6H–SiC at 800 °C is effective to reduce implantation-induced damages.[8,9] In the case of 4H–SiC (11$\bar{2}$0), a very low χ value of 1.2%, which is close to the value obtained from the virgin sample (1.0%), has been obtained for the RT-implanted sample after 1700 °C annealing. A lower χ value of 4.7% has been achieved even by 1300 °C annealing. This indicates that remarkable lattice recovery is realized in 4H–SiC (11$\bar{2}$0) than (0001), partly owing to a much faster recrystallization rate along the $\langle 11\bar{2}0 \rangle$ direction.[10] In addition, an implanted amorphous layer is recrystallized to the original polytype without the inclusion of foreign polytypes such as 3C–SiC in the case of 4H–SiC (11$\bar{2}$0).[11] The remarkable lattice recovery and noninclusion of foreign polytypes give the lower sheet resistance for 4H–SiC (11$\bar{2}$0). In the case of 800 °C implantation and 1700 °C annealing, the lattice damages were reduced to the detection limit of the RBS measurements for both 4H–SiC (0001) and (11$\bar{2}$0). However, the sheet resistances are superior for 4H–SiC (11$\bar{2}$0) as previ-
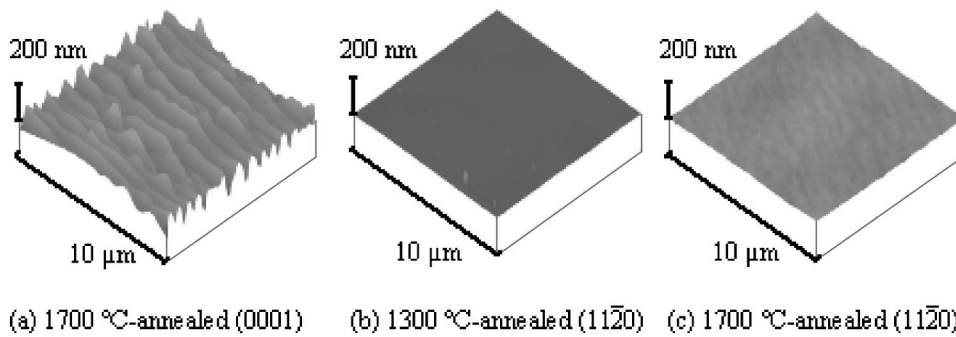
(a) 1700 °C-annealed (0001)   (b) 1300 °C-annealed (11$\bar{2}$0)   (c) 1700 °C-annealed (11$\bar{2}$0)

FIG. 4. AFM images of P$^+$ implanted 4H–SiC: (a) 800 °C implanted and 1700 °C annealed 4H–SiC (0001); (b) 800 °C implanted and 1300 °C-annealed 4H–SiC (11$\bar{2}$0); (c) 800 °C implanted and 1700 °C-annealed 4H–SiC (11$\bar{2}$0).

ously mentioned. These lower sheet resistances for (11$\bar{2}$0) are probably attributed to the following cause: 4H–SiC (0001) may contain more defects than (11$\bar{2}$0), which decrease the electron mobility in (0001). Thus, 4H–SiC (11$\bar{2}$0) may possess much potential to reduce implantation and annealing temperature.

Figure 4(a) shows an atomic force microscopy (AFM) image of 800 °C implanted and 1700 °C annealed 4H–SiC(0001) sample. Considerable roughening and macrostep formation are observed. The root-mean-square (rms) surface roughness is 13.7 nm ($10 \times 10 \ \mu m^2$). An AFM image of 800 °C implanted and 1300 °C-annealed 4H–SiC (11$\bar{2}$0) sample with a comparable sheet resistance ($\sim 100 \Omega/\square$) is shown in Fig. 4(b). The surface is mirror-like, and the value of rms surface roughness is as low as 0.99 nm ($10 \times 10 \ \mu m^2$). For the 1700 °C-annealed 4H–SiC (11$\bar{2}$0) sample shown in Fig. 4(c), the rms roughness is as low as 1.5 nm, which is much smaller than that of 4H–SiC (0001) with the same implantation and annealing temperatures. The surface flatness and remarkable lattice recovery of 4H–SiC (11$\bar{2}$0) may give the low sheet resistances. This brings considerable improvement in SiC device processing technology as well as device performance.[12]

In summary, multiple P$^+$ implantation into 4H–SiC (0001) at 800 °C followed by high-temperature annealing at 1700 °C is effective to form a heavily doped n^+ region with a sheet resistance of as low as 80 $\Omega/\square$. When 4H–SiC (11$\bar{2}$0) epilayers were employed, a low sheet resistance of 110 $\Omega/\square$ was obtained even by RT implantation. A reasonable sheet resistance of 460 $\Omega/\square$ was obtained by RT implantation followed by 1300 °C annealing. In the case of 800 °C implantation into 4H–SiC (11$\bar{2}$0), the sheet resistance took a minimum value of 27 $\Omega/\square$ at an annealing temperature of 1700 °C. A low sheet resistance of 110 $\Omega/\square$ was obtained even by 1300 °C annealing. Regardless of im-

plantation temperature, employing 4H–SiC (11$\bar{2}$0) is an effective method to reduce sheet resistances, to keep surface flatness, and to reduce annealing temperature.

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