A cause for highly improved channel mobility of 4H-SiC metal–oxide–semiconductor field-effect transistors on the $(11\bar{2}0)$ face

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4H-silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors fabricated on both $(11\bar{2}0)$ and (0001) faces were characterized at various temperatures. From the temperature dependence of channel mobility, carrier transport in the inversion layer at the SiO_2/4H-SiC$(11\bar{2}0)$ interface was found to be affected by phonon scattering ($\mu_0 \sim T^{-2.2}$), while that at the SiO_2/4H-SiC(0001) interface was thermally activated ($\mu_0 \sim T^{2.6}$) due to the decrease of Coulomb scattering by emission of electrons from acceptor-like interface states. From the temperature dependence of threshold voltage, the density of acceptor-like interface states near the conduction band edge seems to be low at the SiO_2/4H-SiC$(11\bar{2}0)$ interface, but quite high ($>10^{13}\,cm^{-2}\,eV^{-1}$) at the SiO_2/4H-SiC(0001) interface. The low density of acceptor-like interface states near the conduction band edge on the $(11\bar{2}0)$ face should be the primary cause for the high inversion-channel mobility. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1340861]

Among many polytypes in SiC, 4H-SiC has been recognized as the most attractive material for electronic devices in high-power, high-frequency, and high-temperature operations because of its wider band gap and higher electron mobility than other polytypes. Utilizing native oxide SiO_2, power metal–oxide–semiconductor field-effect transistors (MOSFETs) are expected to have much potential for high-speed and low-loss switching devices. However, several researchers reported extremely low inversion-channel mobilities (typically only few $cm^2/V\,s$)[1–5] in 4H-SiC MOSFETs fabricated on (0001) Si faces regardless of its high bulk mobility ($800\,cm^2/V\,s$). These low channel mobilities lead to high channel resistance resulting in much higher on-resistances in 4H-SiC inversion-mode power MOSFETs[6,7] compared to expected values from 4H-SiC material properties.

Recently, we reported a 17× improvement in inversion channel mobility ($96\,cm^2/V\,s$) of 4H-SiC MOSFETs by utilizing $(11\bar{2}0)$ faces instead of conventional (0001) Si faces ($5.6\,cm^2/V\,s$).[8–10] Also a threshold voltage of 7.8 V on the (0001) face was reduced to 4 V on the $(11\bar{2}0)$ face. In this letter, we examine the temperature dependence of MOSFET characteristics on both $(11\bar{2}0)$ and (0001) faces. The electron transport in inversion layers is quite different for each SiO_2/4H-SiC interface because of different interface state profile.

The starting materials were *n*-type 4H-SiC substrates with the $(11\bar{2}0)$ face orientation supplied by Nippon Steel Co. The $(11\bar{2}0)$ substrates were prepared by slicing parallel to the $(11\bar{2}0)$ face from $[000\bar{1}]$ grown ingots. For comparison, (0001) Si-face substrates with 8° off angle were also used in this experiment. Planar *n*-channel MOSFETs were fabricated on B-doped *p*-type epilayers grown in our group on each substrate. The thickness and the acceptor concentrations of epilayers were 4 μm and $5-10\times10^{15}\,cm^{-3}$, respectively. The source and drain regions were formed by selective ion implantation of N^+ at room temperature followed by activation annealing at 1550 °C for 30 min in Ar. Prior to gate oxidation, the samples were subjected to conventional RCA cleaning followed by additional H_2 annealing[1,3] at 1000 °C for 30 min. The gate oxide was formed by wet oxidation at 1100 °C for 1 h for the $(11\bar{2}0)$ face samples, resulting in an oxide thickness of about 40 nm. For the (0001) face samples, taking into account the slow oxidation rate,[11] wet oxidation was carried out at 1150 °C for 2 h to obtain the same oxide thickness. After the oxidation, all samples were subjected to annealing at the oxidation temperature for 30 min in Ar. The ohmic contacts for the source and drain electrodes were Al/Ti alloyed at 600 °C in Ar. After Al was evaporated and patterned to form the gate electrode, postmetalization annealing was performed at 400 °C in N_2 with 10%-H_2. The channel length (L) and width (W) were 30 and 200 μm, respectively. The directions of drain current are along $[1\bar{1}00]$ and $[000\bar{1}]$ for MOSFETs on the $(11\bar{2}0)$ face, and $[1\bar{1}00]$ for those on the (0001) face. $I-V$ characteristics were measured at various temperatures from 100 to 500 K in an electrically shielded probe station.

Figures 1(a) and 1(b) show drain current (I_D)–drain voltage (V_D) characteristics at a constant gate voltage (V_G) of 10 V for 4H-SiC MOSFETs on the $(11\bar{2}0)$ and (0001) faces at various temperatures. The drain current for MOSFETs on the $(11\bar{2}0)$ face decreases from 0.27 to 0.19 mA in the saturation region with increasing temperature from 307 to 416 K. The decreasing drain current in 4H-SiC MOSFETs at elevated temperatures is realized, for the first time, by utilizing the $(11\bar{2}0)$ face. On the (0001) face, on the contrary, the drain current increases from 0.01 to 0.07 mA with increasing temperature from 297 to 425 K. The decreasing drain current in Fig. 1(a) and increasing one in Fig. 1(b) imply that the channel mobility on the $(11\bar{2}0)$ face decreases and that on the (0001) face increases with increasing temperature, respectively.

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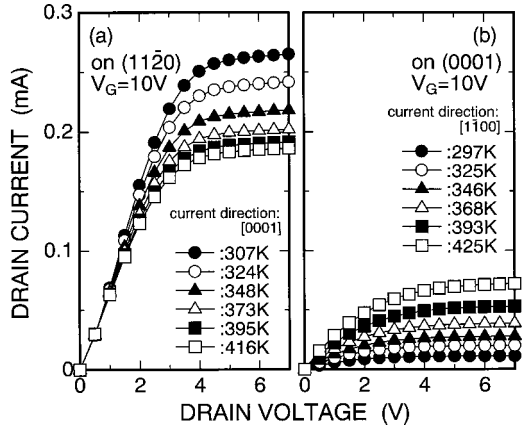

FIG. 1. I_D–V_D characteristics at a constant V_G of 10 V for 4H-SiC MOSFETs on (11$\bar{2}$0) [(a): left figure) and (0001)] [(b): right figure] above room temperature. Drain current flows along [0001] and [1$\bar{1}$00] directions, respectively, to indicate higher current for each case.

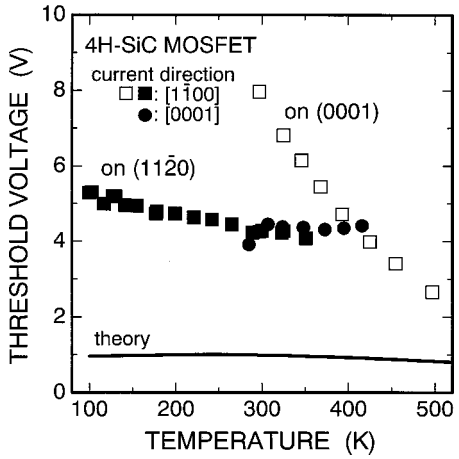

FIG. 3. Temperature dependence of threshold voltage for 4H-SiC MOSFETs on both (11$\bar{2}$0) and (0001).

The channel mobilities as a function of temperature are shown in Fig. 2 for 4H-SiC MOSFETs on both (11$\bar{2}$0) and (0001) faces. The channel mobility was determined from the slope of $I_D/g_m^{1/2}$–V_G plot[12] at V_D=0.1 V (g_m: transconductance). This mobility is called low-field mobility (μ_0), which is not affected by source and drain series resistances. Above 200 K, MOSFETs on the (11$\bar{2}$0) face show decreasing channel mobility in proportion to $T^{-2.2}$. On the (0001) face, however, the channel mobility increases with increasing temperature in proportion to $T^{2.6}$. So far there have been a few reports[13,14] related to temperature dependence of channel mobility in 4H-SiC MOSFETs, in which the channel mobility increased with increasing temperature, even in 4H-SiC MOSFETs with high channel mobility using a deposited oxide as a gate insulator.[14]

The temperature dependences of threshold voltages (V_T) obtained from the linear extrapolation method in I_D–V_G characteristics at V_D=0.1 V are also different for MOSFETs on the (0001) and (11$\bar{2}$0) faces, as shown in Fig. 3. On the (0001) face, the threshold voltages decrease significantly from 8 to 2.7 V at temperatures from 300 to 500 K. The threshold voltages of MOSFETs on the (11$\bar{2}$0) face, however, indicate a weak temperature dependence like the theoretical threshold voltage illustrated by the solid line in Fig. 3. The difference in threshold voltages between measured and theoretical values means the existence of effective fixed charges at the interface or in the oxide. These charges are negative in this case and are originated from both real negative fixed charges and electrons trapped at acceptor-like interface states. The large decrease in the threshold voltage on the (0001) face indicates that electrons trapped at acceptor-like interface states near the conduction band edge are emitted at elevated temperatures resulting in small amount of negative charges. On the other hand, the small change in the threshold voltage on the (11$\bar{2}$0) face for various temperatures up to 420 K (corresponds to an energy of 0.3 eV below the conduction band edge in the inversion condition) means that the density of acceptor-like interface states is low near the conduction band edge. The origin of effective negative charges at the SiO_2/SiC(11$\bar{2}$0) interface will be discussed later.

We simply estimated the interface state density (D_{it}) from the temperature dependence of negative charge density (Q_{nc}) at the interface obtained from Fig. 3, and the results are shown in Fig. 4. The negative charge density is given by

$$Q_{nc}=\frac{C_{ox}}{q}[V_T-V_T(\text{theory})], \tag{1}$$

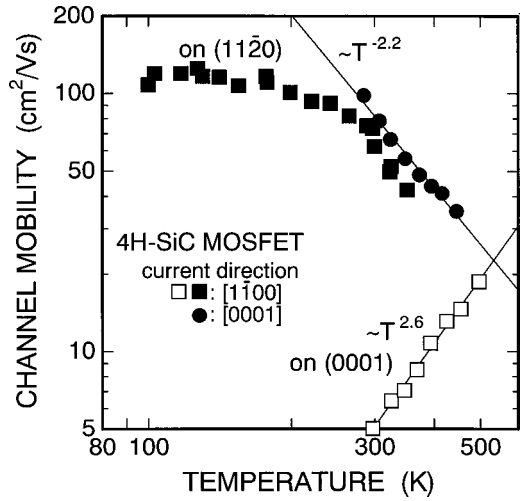

FIG. 2. Temperature dependence of channel mobility for 4H-SiC MOSFETs on both (11$\bar{2}$0) and (0001).

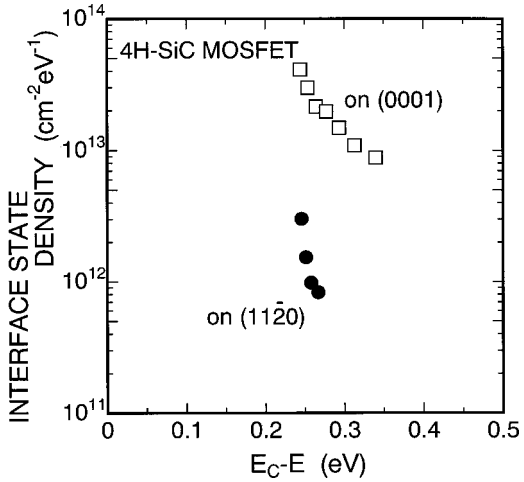

FIG. 4. Interface state density as a function of energy from the conduction band edge in 4H-SiC MOSFETs.

where C_{ox}, q, and V_T(theory) are the oxide capacitance, the electronic charge, and the theoretical threshold voltage, respectively. The interface state density can be calculated from the following formula:

$$D_{it}=\frac{\Delta Q_{nc}}{\Delta \psi_s}, \tag{2}$$

where ΔQ_{nc} is the change in the negative charge density and $\Delta \psi_s$ is the change in the surface potential at inversion. Those values are varied by changing the temperature. In this estimation, all interface states are assumed to be acceptor-like traps, which are negatively charged below the Fermi level. As Fig. 4 indicates, the SiO_2/4H-SiC$(11\bar{2}0)$ interface has much fewer interface state density near the conduction band edge than the SiO_2/4H-SiC(0001) interface. These results are opposite, at first glance, to the previous report on the SiO_2/6H-SiC$(11\bar{2}0)$ interface study.[11] Our study monitored the interface states at energies of approximately 0.3 eV below the conduction band edge, while the previous one did at relatively deeper energies of 0.7–0.8 eV below the conduction band edge. Recent reports[15–17] revealed that the interface state density at the SiO_2/4H-SiC interface on the (0001) face significantly increased ($>10^{13}\,cm^{-2}\,eV^{-1}$) near the conduction band edge. Hence, we suppose that the distributions of interface states for the SiO_2/4H-SiC interfaces on $(11\bar{2}0)$ and (0001) show different profiles: the interface state density does not increase significantly toward the conduction band edge for the SiO_2/4H-SiC$(11\bar{2}0)$ interface. In fact, we have confirmed smaller interface state density near the conduction band edge by high-frequency capacitance–voltage measurements for *n*-type 4H-SiC$(11\bar{2}0)$ metal–oxide–semiconductor structures at low temperatures.[18] Electrons in the inversion layer are easily affected by the interface states near the conduction band edge, and therefore the MOSFETs on the $(11\bar{2}0)$ face can exhibit much higher channel mobility than that on the (0001) face.

Considering the temperature dependence of channel mobility in Fig. 2 ($\mu_0 \sim T^{-2.2}$), the carrier transport in the inversion layer on 4H-SiC$(11\bar{2}0)$ face is affected by phonon scattering above room temperature as observed in the bulk crystal. At deeper energies, the SiO_2/4H-SiC$(11\bar{2}0)$ interface would show relatively higher density of acceptor-like interface states as reported at the SiO_2/6H-SiC$(11\bar{2}0)$ interface in Ref. 11. Therefore, the difference between measured and theoretical threshold voltages on the $(11\bar{2}0)$ face in Fig. 3 is originated from electrons trapped at acceptor-like interface states located at deeper energies below the Fermi level. These trapped electrons can not be emitted in the temperature range up to 420 K in this experiment. These results suggest that the dangling bond density and/or chemical states of bonds at the interface may be essentially different between the $(11\bar{2}0)$ and (0001) faces.

In conclusion, we have studied the carrier transport in the inversion layers of 4H-SiC MOSFETs on both $(11\bar{2}0)$ and (0001) faces at various temperatures. Almost a constant threshold voltage on the $(11\bar{2}0)$ face against temperatures suggests a low density of acceptor-like interface states near the conduction band edge. Therefore, high channel mobility at room temperature and decreasing channel mobility at elevated temperatures for MOSFETs on the $(11\bar{2}0)$ face are derived from the high-quality SiO_2/4H-SiC$(11\bar{2}0)$ interface. Also, carrier transport is affected by phonon scattering. In addition to the low interface state density, a flat surface of epilayer on the $(11\bar{2}0)$ face[19,20] is a promising feature for MOS devices. The decreasing threshold voltage with increasing temperature on the (0001) face is caused by the reduction of electrons trapped at acceptor-like interface states near the conduction band edge of 4H-SiC. MOSFETs on the (0001) face showed increasing channel mobility due to reduced Coulomb scattering by emission of electrons from acceptor-like interface states. A high density of acceptor-like interface states ($>10^{13}\,cm^{-2}\,eV^{-1}$) is the most significant factor to suppress the channel mobility to a very low value on the (0001) face.

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