PAPER Special Section on VLSI Design and CAD Algorithms

Analytical Stability Modeling for CMOS Latches in Low Voltage Operation**

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SUMMARY In synchronous LSI circuits, memory subsystems such as Flip-Flops and SRAMs are essential components and latches are the base elements of the common memory logics. In this paper, a stability analysis method for latches operating in a low voltage region is proposed. The butterfly curve of latches is a key for analyzing a retention failure of latches. This paper discusses a modeling method for retention stability and derives an analytical stability model for latches. The minimum supply voltage where the latches can operate with a certain yield can be accurately derived by a simple calculation using the proposed model. Monte-Carlo simulation targeting 65 nm and 28 nm process technology models demonstrates the accuracy and the validity of the proposed method. Measurement results obtained by a test chip fabricated in a 65 nm process technology also demonstrate the validity. Based on the model, this paper shows some strategies for variation tolerant design of latches.

key words: *latch, low voltage design, stability modeling*

1. Introduction

With continuous advancement of mobile information devices, low-power and low-voltage microprocessors are eagerly required. Since a large number of Flip-Flops (FFs) are used in microprocessors and they have typically a high activity factor, the energy consumed in the FFs occupies a large percentage of the energy consumed in the entire microprocessor [2]. Therefore, developing low-power FFs significantly contributes to designing low-power microprocessors. One of the most effective approaches is lowering the supply voltage (V_{DD}) of FFs since the active energy of the circuit is proportional to ${V_{DD}}^2$. However, as the supply voltage decreases, the impact of the process variation on the transistor's performance becomes significant [3], [4]. Fuketa et al. show that the minimum operating voltage (V_{DDmin}) of memory elements, such as FFs, is higher than that of other combinational logics in concern of a reasonable yield, hence FFs limit the V_{DDmin} of entire circuit [2]. This fact shows that lowering the V_{DDmin} of FFs has a strong impact on reducing the energy consumption of circuits. As a whole, it is a beneficial study to analyze the mechanism of FF's failure and to indicate the model that explains the stability of FFs for lowering the V_{DDmin}.

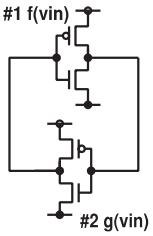

Fig. 1 Schematic of a cross-coupled inverter.

The retention failure of latches in FFs are the dominant factor to determine the stability of FFs in low voltage operation [5]. The stability analysis of latches, therefore, forms a basis for the stability analysis of FFs. The development of an analytical stability model for latches provides an insight for the development of design strategies for robust FFs in low voltage operation. Over several decades, a stability of latches has been widely studied as SNM (Static Noise Margin) [6]–[8]. However, the statistical characteristics of the stability of latches are still not fully understood.

This paper is an extension of our previous work [1]. In [1], we analyze cross-coupled inverters shown in Fig. 1, which are the essential elements of latches, and model the success probability of cross-coupled inverters to retain input value in an analytical way. We refer to this model as *stability model*. Then, we propose a method to estimate the yield of cross-coupled inverters using the derived stability model. We refer to this method as *stability analysis method*. Although latch circuits used in typical master-slave FFs are composed of one inverter and one clocked inverter in general, the target circuit analyzed in [1] is a simple cross-coupled inverter. In this paper, we extend the stability analysis for cross-coupled inverters to the stability analysis for latch circuits with clocked inverter shown in Fig. 2 by considering the clocked inverter to an equivalent inverter. Another extension from [1] is validation of our method with a real chip measurement. In [1], we run simulation targeting only a 28 nm process technology model. This paper demonstrates the validity and the accuracy of the proposed method by Monte-Carlo simulation targeting 65 nm and 28 nm process

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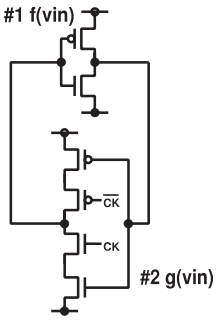

Fig. 2 Schematic of a latch.

technology models. We newly design latch array circuits for a real chip measurement. Measurement results obtained by a test chip fabricated with a 65 nm process technology also demonstrate the validity of the proposed method.

This paper is organized as follows: Section 2 explains related work and contributions of this work. In Sect. 3, we derive an analytical stability model for cross-coupled inverters from fundamental sub-threshold voltage-current characteristics of MOS transistors. In Sect. 4, we extend the stability model for cross-coupled inverters and propose a stability analysis method for latches. Section 5 verifies the proposed methods using transistor-level circuit simulation and test chip measurement. We show the simulation results targeting 65 nm and 28 nm process technology models and measurements results obtained by a test chip fabricated with a 65 nm process technology. Section 6 shows several design strategies for robust latches. Section 7 concludes this paper.

2. Related Work and Contributions of This Work

2.1 Related Work

There are a large number of early studies related to the stability of memory elements. In [9], analytical models for SNM of SRAM bit-cells are proposed. However, their models are valid only for super-threshold voltage operation and they do not consider the impact of process variation. Considering the use of recent low-power devices, transistors are required to be operated in near/sub-threshold voltage region. Moreover, by technology scaling and low voltage operation, the process variation becomes a non-negligible factor. This paper targets the statistical characteristics of latches operating in sub-threshold voltage region considering process variation. Calhoun, et al. evaluate the distribution of SNM of 6T SRAM operating in the sub-threshold voltage region [10]. They show that the SNM is distributed normally and that the dominant factor to affect the SNM variation is the threshold voltage (V_{TH}) fluctuation. Mizutani, et al. show a similar observation about the distribution of the SNM from measurement results of a recent process technology [11]. These works reveal the statistical characteristics of SRAM cells, however, the theoretical basis of the distribution has not been clarified enough. Like above all, the statistical characteristics of memory's stability have long been an important research topic. However, it has not been fully explained in an analytical way. In this paper, we analytically show the statistical characteristics of the stability by using our stability analysis method.

2.2 Contributions of This Work

The contributions of our work can be summarized as follows:

- We propose a stability analysis method for latches operating in a sub-threshold voltage region. Designers can estimate the yield of target latches from a fast calculation using the proposed method. Based on the yield estimation, we can easily obtain V_{DDmin} where the latches ensure a target yield. We demonstrate the effectiveness of the proposed method in 65 nm and 28 nm process technology models, and a several design of latches.
- We analytically clarify that the supply voltage where the latches ensure a specific yield is distributed normally. This means that the gradient of the yield becomes linear on a normal probability plot.
- We show measurement results of the stability of the latches in low voltage operation. The characteristics of the stability agree well with that obtained from the proposed method.
- We show design guidelines to help designers develop a robust latch circuit. For example, we show that the transistor sizes of the latches should be carefully tuned and the drive strength of the pMOS and nMOS transistors of the latches should be well-balanced for enhancing the robustness of the latches.

3. A Stability Analysis Method for Cross-Coupled Inverters

In this section, we present an analytical stability model for cross-coupled inverters based on sub-threshold characteristics of MOS transistors. Firstly, we explain characteristics of a target latch circuit that is analyzed in this paper. After that, we examine and formulate a failure mode that leads to a failure operation.

3.1 Target Circuit and Its Failure Condition

Conventional SRAM cells have a simple cross-coupled inverter and additional transistors for write and read accesses. Latches used in a typical master-slave FFs are composed of one inverter and one clocked-inverter in general. Therefore in this paper, we analyze the stabilities of cross-coupled inverters and latches respectively. Firstly, we analyze cross-coupled inverters in this section. After that, we analyze latches in Sect. 4.

We examine the failure operation of a cross-coupled inverter as follows. Figure 3(b) shows a VTC (Voltage Transfer Characteristics) of an inverter. $f(V_{in})$ gives the VTC of inverter #1, $g^{-1}(V_{in})$ gives the inverse VTC of inverter #2. The two-lobed curve is called as a butterfly curve. If the eye of the

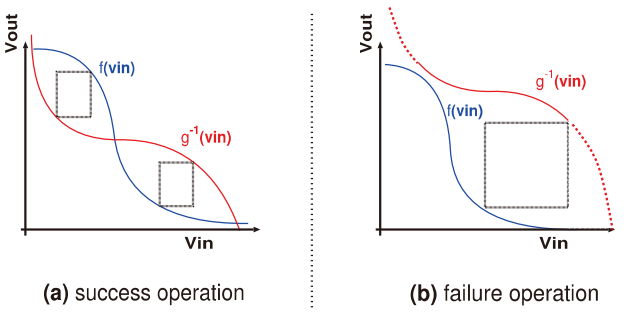

Fig. 3 The butterfly curve of cross-coupled inverters. (a) An example of success operations; (b) An example of failure operations.

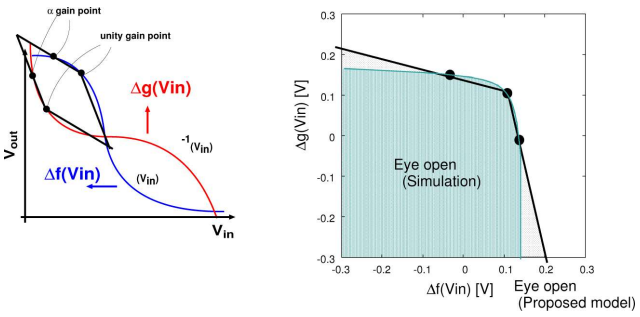

Fig. 4 Left figure: The concept of the proposed model. The eye diagram is approximated as parallelogram. Right figure: The comparison of failure conditions of the proposed model with that of simulation.

butterfly curves sufficiently opens, the cross-coupled inverter can hold the input voltage at either of the two stable points strongly. On the other hand, the cross-coupled inverter fails when the eye closes, for example, due to process variation. An example of this situation is shown in Fig. 3(c). This is the definition of the failure condition of the cross-coupled inverter in this paper.

3.2 The Idea of the Proposed Method

The butterfly curve itself cannot be expressed in a closed form. However, the unity-gain point (i.e., the point where the gradient of the curve becomes -1.) can be expressed analytically [4]. In addition, the point at which the gradient becomes a certain value between 0 and -1 can be expressed analytically with good accuracy. Therefore, we define the "α-gain point" where the gradient becomes $-\alpha$ ($0 < \alpha < 1$). The decision of α is discussed later in Sect. 3.4. With the help of the unity-gain point and the α-gain point, we can model the failure condition of the cross-coupled inverter such that the area of the parallelogram calculated by the unity-gain points and the α-gain points becomes negative. The left part of Fig. 4 explains this concept. This shows our idea for approximating the eye diagram as a parallelogram.

Before deriving the expression of the proposed model, we examine the validity of the idea of approximating the eye diagram as a parallelogram. Calhoun, et al. show that the VTC of the inverter #1 fluctuates horizontally and the inverse VTC of inverter #2 fluctuates vertically due to process variation [10]. We investigate the boundary where the eye closes due to the effects of the two fluctuations. We evaluate the VTC of a cross-coupled inverter shown in Fig. 3(a) by simulation. The curved line in the right figure of Fig. 4 shows the simulation result at $V_{DD} = 300$ mV targeting a 28 nm process technology model. $\Delta f(V_{in})$ is the horizontal fluctuation of $f(V_{in})$. $\Delta g(V_{in})$ is the vertical fluctuation of $g^{-1}(V_{in})$. Thereafter $f(V_{in})$ and $g^{-1}(V_{in})$ are moved through the distance $\Delta f(V_{in})$ and $\Delta g(V_{in})$, respectively, we examine the eye of the butterfly curve. The eye of the butterfly curve opens when the fluctuation is in the shaded area. The straight lines shown in the figure represent the boundary of the failure condition after the approximation. This figure indicates the accuracy of the proposed model. The threshold voltage of transistors can be assumed to be normally distributed. Since the inverter is composed of two transistors, the fluctuation of the VTC of the inverter has a bivariate normal distribution. The median of the distribution is $(0, 0)$, which means a condition without the threshold voltage variation. The proposed model provides good accuracy for the points around the origin where the occurrence probability is high, while the accuracy of the approximation degrades when the fluctuated point goes far from the origin $(0, 0)$ where the occurrence probability is negligibly small since the VTC fluctuation has a bivariate normal distribution. These facts imply that the error of the proposed model should be small.

3.3 The Unity-Gain Point of Inverters in Sub-Threshold Voltage Region

The expression of the sub-threshold voltage-current model of MOS transistors is as follows [12]:

$$I = k\frac{W}{L}\exp\left(-\frac{\Delta V_{TH}}{nv_T}\right) \times \exp\left(\frac{V_{GS} + \eta V_{DS} - k_\gamma V_{BS}}{nv_T}\right)\left(1 - \exp\frac{-V_{DS}}{v_T}\right), \quad (1)$$

$$k = I_0 \exp\left(\frac{V_{TH,0}}{nv_T}\right), \quad (2)$$

where I_0 is the drain current at $V_{GS} = 0$ and $V_{DS} = V_{DD}$, η is the DIBL (Drain Induced Barrier Lowering) coefficient, k_γ is the body effect coefficient, n is the sub-threshold swing parameter, v_T is the thermal voltage. We denote the threshold voltage without variation as $V_{TH,0}$ and ΔV_{TH} corresponds to threshold voltage fluctuation due to process variation, mainly caused by RDF (Random Dopant Fluctuation). I_0, η, k_γ, n and $V_{TH,0}$ are technology-dependent parameters. We denote the input voltage of the inverter as V_{in}, the output voltage of the inverter as V_{out}. By setting the output current of the pMOS transistor (I_p) and that of the nMOS transistor (I_n) to be equal and opposite, we can solve the VTC of the inverter. For simplicity, we assume $V_{BS} = 0$ in the following.

We denote the V_{in} and the V_{out} at the unity-gain points as V_{IL}, V_{OH}, V_{IH} and V_{OL} as shown in Fig. 5. Firstly, we derive the expression of V_{OH} and V_{IL}. When V_{in} is close to 0 and V_{out} is close to V_{DD}, $1 - \exp(-V_{out}/v_T)$ becomes close to 1.

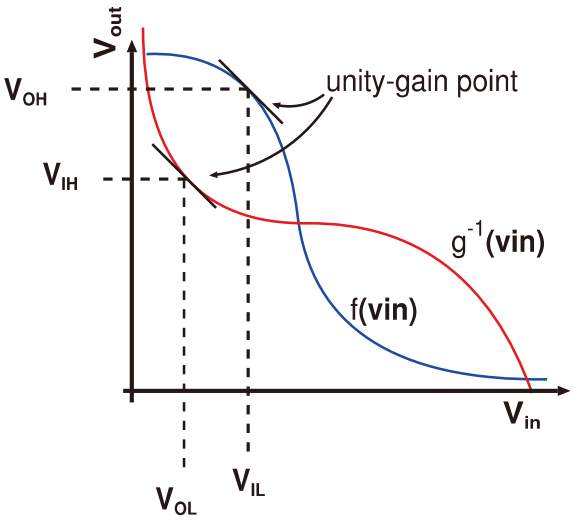

Fig. 5 The unity-gain points obtained from the butterfly curve.

Then we can approximate I_n as follows:

$$I_n \simeq k_n \frac{W_n}{L_n} \exp\left(-\frac{\Delta V_{TH,n}}{n_n v_T}\right) \exp\left(\frac{V_{in} + \eta_n V_{out}}{n_n v_T}\right). \quad (3)$$

By using the Taylor expansion around the point $V_{DD} - V_{out} = v_T \ln(n/2 + 1)$ and truncating at the first order, the following equation is derived:

$$1 - \exp\frac{-(V_{DD} - V_{out})}{v_T} \simeq \frac{n}{n+2} + \frac{1}{v_T}\frac{2}{n+2} \times \left\{V_{DD} - V_{out} - v_T \ln\left(\frac{n}{2} + 1\right)\right\}, \quad (4)$$

where $1/n = (1/n_p + 1/n_n)/2$. Since $\eta_p(V_{DD} - V_{out})/n_p v_T$ is close to 0, we can use the approximation below:

$$\exp\left\{\frac{\eta_p(V_{DD} - V_{out})}{n_p v_T}\right\} \simeq 1, \quad (5)$$

$$\exp\left(\frac{\eta_n V_{out}}{n_n v_T}\right) = \exp\left\{\frac{\eta_n(V_{out} - V_{DD} + V_{DD})}{n_n v_T}\right\} = \exp\left(\frac{\eta_n V_{DD}}{n_n v_T}\right) \exp\left\{\frac{\eta_n(V_{out} - V_{DD})}{n_n v_T}\right\} \simeq \exp\left(\frac{\eta_n V_{DD}}{n_n v_T}\right). \quad (6)$$

By using these approximations, the output current of the inverter in a steady state can be approximated as:

$$I_{out} = k_n \frac{W_n}{L_n} \exp\left(-\frac{\Delta V_{TH,n}}{n_n v_T}\right) \exp\left(\frac{V_{in} + \eta_n V_{DD}}{n_n v_T}\right) = k_p \frac{W_p}{L_p} \exp\left(-\frac{\Delta V_{TH,p}}{n_p v_T}\right) \exp\left(\frac{V_{DD} - V_{in}}{n_p v_T}\right) \times \left[\frac{n}{n+2} + \frac{1}{v_T}\frac{2}{n+2}\left\{V_{DD} - V_{out} - v_T \ln\left(\frac{n}{2} + 1\right)\right\}\right]. \quad (7)$$

We can express V_{IL} and V_{OH} by solving (7) for V_{out} and taking V_{in} and V_{out} at $(\partial V_{out}/\partial V_{in}) = -1$:

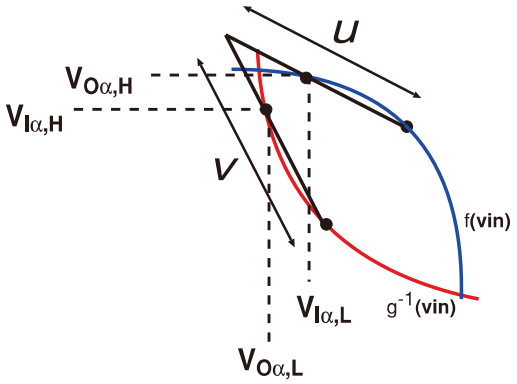

Fig. 6 The upper-left eye of the butterfly curve. Connecting the unity-gain points and the α-gain points makes a parallelogram.

$$V_{IL} = \frac{n}{2}\left(\frac{1}{n_p} - \frac{\eta_n}{n_n}\right)V_{DD} - \frac{n v_T}{2}\left\{\ln\left(\frac{2}{n} + 1\right) + \ln\frac{k_n \frac{W_n}{L_n}}{k_p \frac{W_p}{L_p}}\right\} + \frac{n}{2}\left(\frac{\Delta V_{TH,n}}{n_n} - \frac{\Delta V_{TH,p}}{n_p}\right), \quad (8)$$

$$V_{OH} = V_{DD} - v_T \ln\left(\frac{n}{2} + 1\right). \quad (9)$$

Then, $V_{DD} - V_{OH} = v_T \ln(n/2 + 1)$. Therefore, the error by the Taylor expansion around $V_{out} = V_{OH}$ in (4) can be small. We follow these derivations from early studies [4], [13], and improve the approximation.

V_{IH} and V_{OL} can be expressed by the same procedure in case that V_{in} is close to V_{DD} and V_{out} is close to 0. V_{IH} and V_{OL} can be expressed as:

$$V_{IH} = \frac{n}{2n_p}(1 + \eta_p)V_{DD} + \frac{n v_T}{2}\left\{\ln\left(\frac{2}{n} + 1\right) + \ln\frac{k_p \frac{W_p}{L_p}}{k_n \frac{W_n}{L_n}}\right\} + \frac{n}{2}\left(\frac{\Delta V_{TH,n}}{n_n} - \frac{\Delta V_{TH,p}}{n_p}\right), \quad (10)$$

$$V_{OL} = v_T \ln\left(\frac{n}{2} + 1\right). \quad (11)$$

3.4 The Expression of the Eye-Opening Condition

We express the area of the parallelogram shown in Fig. 4. Figure 6 shows the upper-left eye of the butterfly curve and the definitions of $V_{I\alpha,L}$, $V_{O\alpha,H}$, $V_{I\alpha,H}$ and $V_{O\alpha,L}$. These voltages represent the V_{in} or V_{out} at the α-gain points, respectively. These voltages can be derived from the same procedure for V_{IL},V_{OH}, V_{IH} and V_{OL} explained in the previous section.

Figure 6 shows the definitions for the parallelogram. u is the length of the top-and-bottom sides of the parallelogram, v is the length of the left-and-right sides of the parallelogram. We can find the intersection point of u and v using (8)–(11) and $V_{I\alpha,L}$, $V_{O\alpha,H}$, $V_{I\alpha,H}$, $V_{O\alpha,L}$. At last, u and v can be modeled as:

$$u = \frac{\sqrt{1 + x_\alpha^2}}{(1 - x_\alpha^2)}(x_\alpha V_{IH} + V_{IL} - x_\alpha V_{OH} - V_{OL}), \quad (12)$$

$$v = \frac{x_\alpha\sqrt{1+x_\alpha^2}}{(1-x_\alpha^2)}(V_{\mathrm{IH}} + x_\alpha V_{\mathrm{IL}} - V_{\mathrm{OH}} - x_\alpha V_{\mathrm{OL}}), \quad (13)$$

$$x_\alpha = \frac{2}{n}\frac{\ln\{(n+2)/(n\alpha+2)\}}{\ln\{\alpha(n+2)/(n\alpha+2)\}}, \quad (14)$$

where x_α becomes a certain negative value. Since the lengths of the parallelogram are expressed analytically, we can derive eye-opening condition for the parallelogram as follows:

"The area of the parallelogram becomes positive value"
$\Leftrightarrow$ "$u > 0$ and $v > 0$"
$\Leftrightarrow$ "$(x_\alpha V_{\mathrm{IH}} + V_{\mathrm{IL}} - x_\alpha V_{\mathrm{OH}} - V_{\mathrm{OL}} > 0)$
and $(V_{\mathrm{IH}} + x_\alpha V_{\mathrm{IL}} - V_{\mathrm{OH}} - x_\alpha V_{\mathrm{OL}} < 0)$". (15)

The shape of the parallelogram should be close to the shape of the eye of the butterfly curve. Equations (14) and (15) indicate that the probability of the eye opening depends on the value of α. Therefore, α should be carefully decided. The shape of the eye of the butterfly curve depends on the supply voltage. The eye shapes look like a square when the supply voltage is sufficiently high, and the eye becomes narrower as the supply voltage decreases. Let's assume α_0 represents the negative value of the VTC gradient at $V_{\mathrm{in}} = 0$. The amount of α_0 also changes according to the supply voltage. Therefore, α should be determined depending on the supply voltage for accurately modeling the eye diagram. The gradient of the VTC is -1 at the unity-gain point and it monotonically approaches α_0 as V_{in} decreases. Since the α-gain point exists between the unity-gain point and $V_{\mathrm{in}} = 0$, we use the α as the average of the unity-gain and α_{o} as:

$$\alpha = \frac{\alpha_0 + 1}{2}, \quad (16)$$

$$\alpha_0 = \frac{2}{n}\frac{1}{\frac{k_{\mathrm{p}}\frac{W_{\mathrm{p},1}}{L_{\mathrm{p},1}}}{k_{\mathrm{n}}\frac{W_{\mathrm{n},1}}{L_{\mathrm{n},1}}}\exp\left\{\frac{1}{v_{\mathrm{T}}}\left(\frac{1}{n_{\mathrm{p}}} - \frac{\eta_{\mathrm{n}}}{n_{\mathrm{n}}}\right)V_{\mathrm{DD}}\right\} - 1}. \quad (17)$$

Thus, we can successfully model the dependence of the supply voltage on the eye opening for the parallelogram.

3.5 A Stability Model for Cross-Coupled Inverters

We express the probability of the eye-opening of the butterfly curve. In the following, the characteristics of inverter #1 is identified by a subscript "1", that of inverter #2 is identified by a subscript "2". By applying the same procedure explained in Sect. 3.4 to the lower-right eye of the butterfly curve, we obtain the condition that the both of the eyes open as:

$$\begin{aligned} &x_\alpha V_{\mathrm{IH},2} + V_{\mathrm{IL},1} - x_\alpha V_{\mathrm{OH},1} - V_{\mathrm{OL},2} > 0 \\ &\text{and } V_{\mathrm{IH},2} + x_\alpha V_{\mathrm{IL},1} - V_{\mathrm{OH},1} - x_\alpha V_{\mathrm{OL},2} < 0 \\ &\text{and } x_\alpha V_{\mathrm{IH},1} + V_{\mathrm{IL},2} - x_\alpha V_{\mathrm{OH},2} - V_{\mathrm{OL},1} > 0 \\ &\text{and } V_{\mathrm{IH},1} + x_\alpha V_{\mathrm{IL},2} - V_{\mathrm{OH},2} - x_\alpha V_{\mathrm{OL},1} < 0. \end{aligned} \quad (18)$$

This equation can be divided to the variable terms and constant terms as follows:

$$\begin{aligned} &\Delta u < H_{\mathrm{const.}} \text{ and } \Delta v > L_{\mathrm{const.}} \\ &\text{and } \Delta u' < H'_{\mathrm{const.}} \text{ and } \Delta v' > L'_{\mathrm{const.}}, \end{aligned} \quad (19)$$

where, $\Delta u, \Delta v, H_{\mathrm{const.}}$ and $L_{\mathrm{const.}}$ are expressed as follows:

$$\begin{pmatrix} \Delta u \\ \Delta v \end{pmatrix} = \frac{n}{2}\begin{pmatrix} 1 & x_\alpha \\ x_\alpha & 1 \end{pmatrix}\begin{pmatrix} \frac{\Delta V_{\mathrm{TH,p},1}}{n_{\mathrm{p}}} - \frac{\Delta V_{\mathrm{TH,n},1}}{n_{\mathrm{n}}} \\ \frac{\Delta V_{\mathrm{TH,p},2}}{n_{\mathrm{p}}} - \frac{\Delta V_{\mathrm{TH,n},2}}{n_{\mathrm{n}}} \end{pmatrix}, \quad (20)$$

$$\begin{aligned} H_{\mathrm{const.}} = &\left\{-x_\alpha + (x_\alpha+1)\frac{n}{2n_{\mathrm{p}}} + x_\alpha\frac{n}{2n_{\mathrm{p}}}\eta_{\mathrm{p}} - \frac{n}{2n_{\mathrm{n}}}\eta_{\mathrm{n}}\right\}V_{\mathrm{DD}} \\ &+ v_{\mathrm{T}}(x_\alpha - 1)\left\{\ln\left(\frac{n}{2}+1\right) + \frac{n}{2}\ln\left(\frac{2}{n}+1\right)\right\} \\ &+ \frac{nv_{\mathrm{T}}}{2}\left\{\ln\left(\frac{k_{\mathrm{p}}\frac{W_{\mathrm{p},1}}{L_{\mathrm{p},1}}}{k_{\mathrm{n}}\frac{W_{\mathrm{n},1}}{L_{\mathrm{n},1}}}\right) + x_\alpha\ln\left(\frac{k_{\mathrm{p}}\frac{W_{\mathrm{p},2}}{L_{\mathrm{p},2}}}{k_{\mathrm{n}}\frac{W_{\mathrm{n},2}}{L_{\mathrm{n},2}}}\right)\right\}, \end{aligned} \quad (21)$$

$$\begin{aligned} L_{\mathrm{const.}} = &\left\{-1 + (x_\alpha+1)\frac{n}{2n_{\mathrm{p}}} + \frac{n}{2n_{\mathrm{p}}}\eta_{\mathrm{p}} - x_\alpha\frac{n}{2n_{\mathrm{n}}}\eta_{\mathrm{n}}\right\}V_{\mathrm{DD}} \\ &+ v_{\mathrm{T}}(-x_\alpha+1)\left\{\ln\left(\frac{n}{2}+1\right) + \frac{n}{2}\ln\left(\frac{2}{n}+1\right)\right\} \\ &+ \frac{nv_{\mathrm{T}}}{2}\left\{x_\alpha\ln\left(\frac{k_{\mathrm{p}}\frac{W_{\mathrm{p},1}}{L_{\mathrm{p},1}}}{k_{\mathrm{n}}\frac{W_{\mathrm{n},1}}{L_{\mathrm{n},1}}}\right) + \ln\left(\frac{k_{\mathrm{p}}\frac{W_{\mathrm{p},2}}{L_{\mathrm{p},2}}}{k_{\mathrm{n}}\frac{W_{\mathrm{n},2}}{L_{\mathrm{n},2}}}\right)\right\}. \end{aligned} \quad (22)$$

$\Delta u, \Delta v, \Delta u'$ and $\Delta v'$ are variable terms and $H_{\mathrm{const.}}$, $L_{\mathrm{const.}}$, $H'_{\mathrm{const.}}$ and $L'_{\mathrm{const.}}$ are constant terms. $\Delta u'$, $\Delta v'$, $H'_{\mathrm{const.}}$ and $L'_{\mathrm{const.}}$ are derived by swapping the subscript from Δu, Δv, $H_{\mathrm{const.}}$ and $L_{\mathrm{const.}}$, hence $\Delta u' = \Delta v$, $\Delta v' = \Delta u$. The probability that satisfies the condition (19) is expressed as:

$$\begin{aligned} &P(L'_{\mathrm{const.}} < \Delta u < H_{\mathrm{const.}}) \\ &\text{and } P(L_{\mathrm{const.}} < \Delta v < H'_{\mathrm{const.}}). \end{aligned} \quad (23)$$

Assuming that the threshold voltage variation is distributed normally and independently, (20) indicates that Δu and Δv follow correlated bivariate normal distributions. Therefore, the probability of (23) which represents the probability that the both of the eyes of the butterfly curve open is solved by integrating a function of a random variable which follows the bivariate normal distribution.

A jointing PDF $f(x, y)$ (Probability Density Function) of two random variables x and y, which follow the bivariate normal distribution can be expressed in general:

$$\begin{aligned} f(x,y) = &\frac{1}{2\pi\sigma_{\mathrm{x}}\sigma_{\mathrm{y}}\sqrt{1-\rho^2}}\exp\left[-\frac{1}{2(1-\rho^2)}\right. \\ &\left.\times\left\{\frac{(x-\mu_{\mathrm{x}})^2}{\sigma_{\mathrm{x}}^2} - 2\rho\frac{(x-\mu_{\mathrm{x}})(y-\mu_{\mathrm{y}})}{\sigma_{\mathrm{x}}\sigma_{\mathrm{y}}} + \frac{(y-\mu_{\mathrm{y}})^2}{\sigma_{\mathrm{y}}^2}\right\}\right], \end{aligned} \quad (24)$$

where ρ is a correlation coefficient between the two random variables. The CDF $\Phi(x, y)$ (Cumulative Distribution Function) of (24) is also expressed as:

$$\Phi(x,y) = \int_{-\infty}^{y}\int_{-\infty}^{x} f(u,v)dudv. \quad (25)$$

Fig. 7 A stability analysis method for cross-coupled inverter using proposed model (26).

The probability of (23) can be expressed using (25) as follows:

$$\int_{L_{\text{const.}}}^{H'_{\text{const.}}} \int_{L'_{\text{const.}}}^{H_{\text{const.}}} f(\Delta u, \Delta v) d\Delta u d\Delta v = \Phi(H_{\text{const.}}, H'_{\text{const.}}) - \Phi(H_{\text{const.}}, L_{\text{const.}}) - \Phi(L'_{\text{const.}}, H'_{\text{const.}}) + \Phi(L'_{\text{const.}}, L_{\text{const.}}). \quad (26)$$

Equation (26) expresses the probability that the both of the eyes open. We propose Eq. (26) as a stability model for cross-coupled inverters. While solving (26) needs to solve the bivariate Gaussian integral, it cannot be solved analytically. However, many algorithms to solve the bivariate Gaussian integral in a short time using numerical methods have been proposed [14], [15]. Hence, we can solve (26) easily by using numerical calculation. As a summary, an yield of latches can be quickly estimated by our method as summarized in Fig. 7.

4. A Stability Analysis Method for Latches

The stability model derived in the previous section is applicable only to cross-coupled inverter as shown in Fig. 1. In this section, we propose a stability model for latches shown in Fig. 2 by developing the model for cross-coupled inverters.

4.1 Equivalent Inverter Conversion

It is difficult to model the butterfly curve of latches since the voltage of the intermediate node between stacked two pMOS/nMOS transistors in a clocked inverter cannot be modeled analytically. Therefore in this paper, we use the idea of equivalent inverter conversion [4]. we convert the clocked inverter into an effective equivalent inverter. The latch works as a simple inverter when the clock is high and the latch is retention mode. The characteristics of the latch can be modeled using fitted process parameters n', k', and η' as shown in Fig. 8. The fitted parameters can be obtained through circuit simulation.

4.2 A Stability Model for Latches

Based on the idea of equivalent inverter conversion, we propose a stability analysis method for latches in the following steps:

1. Find n', $k'$and η' for pMOS/nMOS transistor respectively by fitting (1) and the simulation result in the target voltage region.
2. Assume that one of the inverters in the equivalent cross-coupled inverter has n, k, and η, and the other has n', k', and η'.
3. Estimate the yield of the latch using the stability analysis method for the cross-coupled inverter as shown in Fig. 7.

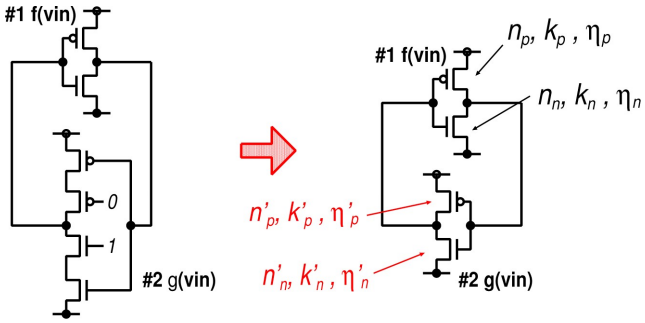

Fig. 8 Equivalent inverter conversion. Latches can be converted to cross-coupled inverters.

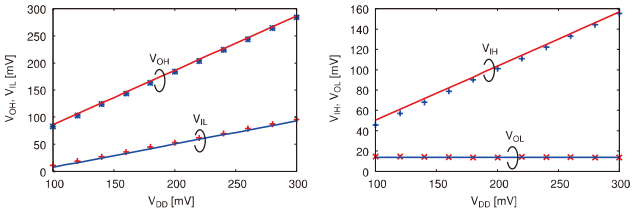

Fig. 9 Comparison of V_{IL}, V_{IH}, V_{OL}, and V_{OH} from the proposed model (linear lines) with simulation (dots).

5. Verification of the Proposed Methods

This section verifies the proposed stability analysis method. Firstly, we verify the methods for cross-coupled inverters and latches, respectively using transistor-level circuit simulation targeting commercial process technology models. After this, the measurement results also verify the methods.

5.1 Verification for Cross-Coupled Inverters

We evaluate the proposed stability analysis method (Fig. 7) for cross-coupled inverters by transistor-level circuit simulation targeting a commercial 28 nm process technology model with a foundry provided Monte-Carlo simulation package. The nominal supply voltage of this process technology is 1.0 V. The process dependent parameters for our model, n, η, k, can be obtained by fitting the parameters from DC analysis.

Figure 9 shows the validity of V_{IL}, V_{IH}, V_{OL} and V_{OH}. The lines represent the voltages obtained from the analytical models (8)–(11), and the dots represent the voltages obtained from the Monte-Carlo simulation results. The results indicate that the error introduced by approximations (3)–(6) is small.

The validation results for the proposed method (Fig. 7) is shown in Fig. 11. It shows a normal probability plot of the yield at each supply voltage. The vertical axis of Fig. 11 shows the eye-opening probability for the cross-coupled inverter operating at the supply voltage shown in the horizontal

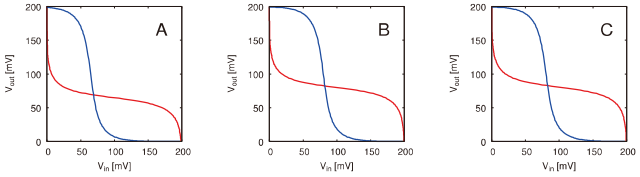

Fig. 10 Examples of the butterfly curves of circuit A, B and C. The supply voltage is 200 mV.

axis. In this verification, we assume two identical inverters are cross-coupled together. We run 100,000 Monte-Carlo trials for each of different voltage conditions. In order to evaluate the difference of the stabilities between cross-coupled inverters in different sizes, three different sets of transistor widths for the cross-coupled inverter are examined. The three sets of transistor widths W are:

A : W of pMOS/nMOS transistors are the minimum sizes allowed in the target process technology. Since the sizes of the transistors are minimum, the variability becomes the largest. Also, the P/N ratio is not balanced.

B : W of nMOS transistor is a minimum size and W of pMOS transistor is 1.5 times larger than that of nMOS transistors. Due to the increase of the pMOS transistor width, the P/N ratio is improved over A.

C : W of pMOS/nMOS transistors are the same sizes of those in 1X inverters. The 1X inverter is about 3 times larger than B. Note that the P/N ratio of B and that of C have almost same value. Due to the increase in the sizes of both transistors, the variability of C becomes smaller than that of A and B.

Figure 10 shows the butterfly curves of circuits A, B and C at 200 mV operation. Since the strength of nMOS transistor is weaker than that of pMOS transistor, the eye of the butterfly curve of A is unbalanced. The butterfly curve of B and that of C are quite similar. However, the transistor sizes of C is larger than B. C is expected to be more stable than B.

The yield estimated with the proposed method agrees well with that obtained from Monte-Carlo simulation. This fact means that the proposed method accurately expresses the stability of cross-coupled inverters.

We validate the proposed method using another process technology. The comparison results targeting a 65 nm process technology model is shown in Fig. 12. The simulation setup is the same as the experiment targeting the 28 nm process technology. Although circuit C exhibits a little larger error than circuits A and B, Fig. 12 indicates that our method is applicable not only to the 28 nm process technology, but also to the 65 nm process technology. The misfit of circuit C comes from the modeling error of (1) that estimates the drain current that is proportional to W. In reality, due to a narrow width effect, the drain current may not linearly proportional to the width in a transistor with a small width. The 65 nm process exhibits a stronger narrow width effect than the 28 nm process, and therefore the misfit becomes visible in circuit C with large-width transistors.

Figure 11 and Fig. 12 also show an important characteristic of the stability of cross-coupled inverters. The gradient of the proposed model and that of the simulations becomes constant in high-σ region. This result indicates that the operating voltage of the cross-coupled inverter for achieving a specific yield is distributed normally. This characteristic is consistent with the observations in early studies [5], [11], hence our model gives an analytical proof of these works.

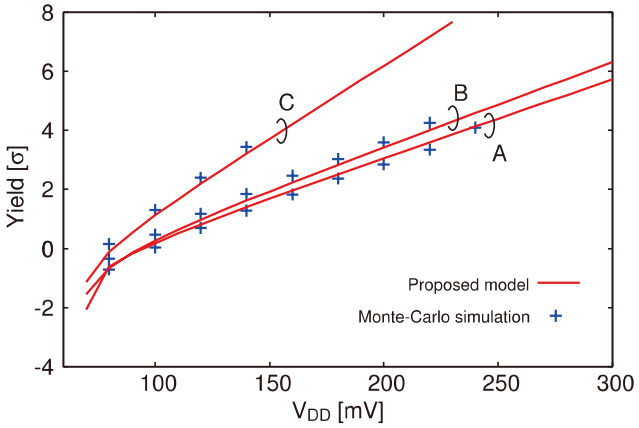

Fig. 11 Verification for the proposed method for cross-coupled inverters using a 28 nm process technology model.

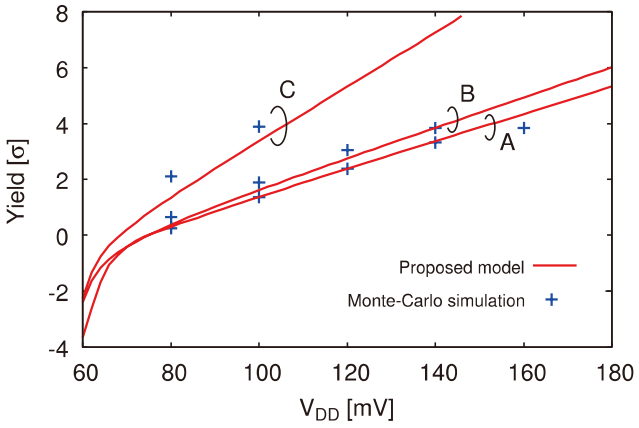

Fig. 12 Verification for the proposed method for cross-coupled inverters using a 65 nm process technology model.

5.2 Verification for Latches by Simulation

We evaluate the proposed stability analysis method discussed in Sect. 4 by Monte-Carlo simulation targeting a 65 nm process technology model. In this verification, the simulation setup is the same as the previous section and we assume that the gate widths of the stacked two pMOS/nMOS transistors in the clocked inverter are the same. Figure 13 shows the comparison results. Similar to the results of cross-coupled inverters, the estimated yield of latches agrees well with the Monte-Carlo simulation results. Therefore, the proposed method for latches accurately expresses the stability of the latches. Comparison of Fig. 12 and Fig. 13 indicates that the yield of latches is smaller than those of cross-coupled

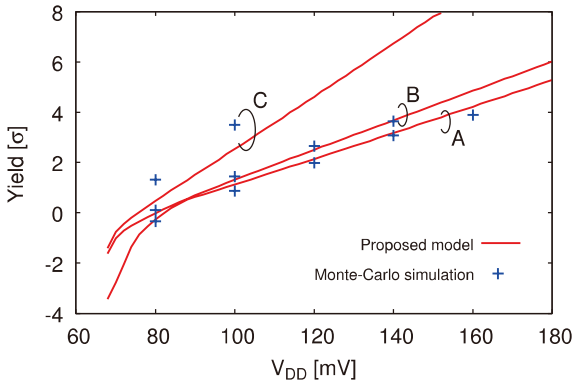

Fig. 13 Verification for the proposed method for latches using a 65 nm process technology model.

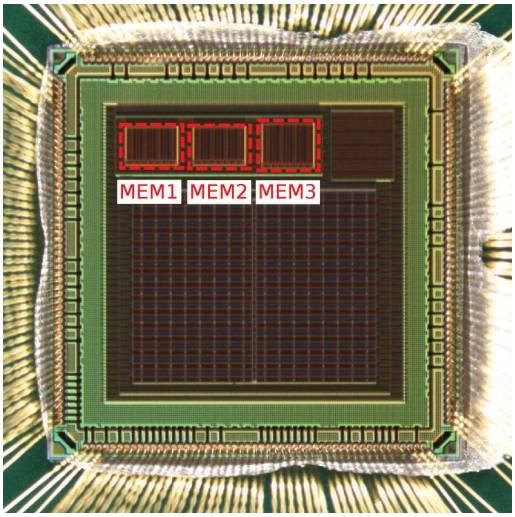

Fig. 14 Test chip micrograph.

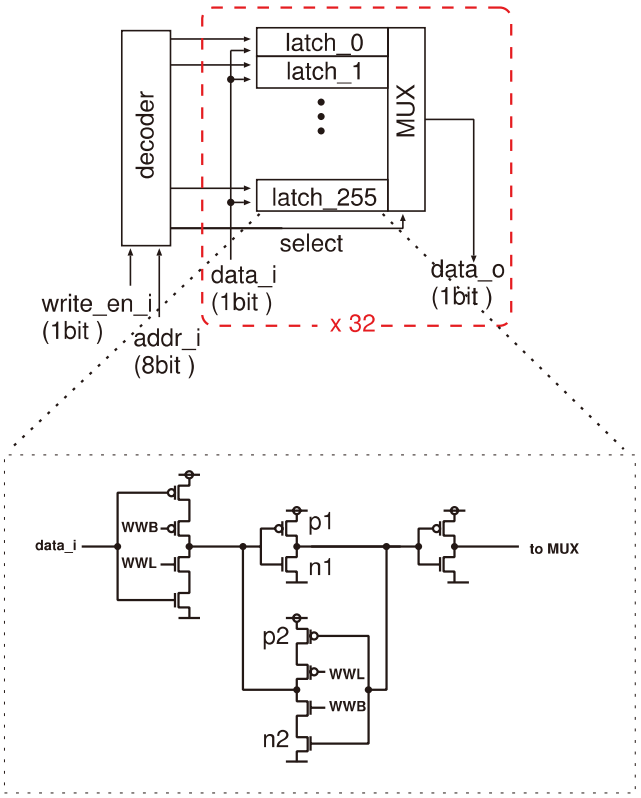

Fig. 15 Test circuit structure. Each test circuit contains 8,192 latches.

Table 1 Gate widths of the latches.

Memory	Normalized gate width (p1, n1, p2, n2)
MEM1	(1.5, 1, 1, 1.5)
MEM2	(1.5, 1, 1.5, 1)
MEM3	(4.5, 3, 4.5, 3)

inverters. This is because the driving strength of a clocked inverter with stacked transistors is weaker than that of an inverter with non-stacked transistors while both inverters exhibit similar amount of variability. This characteristic comes from the difference of the gate voltages in a clocked inverter and a normal inverter. The clocked transistors in a clocked inverter are driven to V_{DD} or 0 whereas the other transistors are driven to an intermediate voltage between V_{DD} and 0 at the boundary where retention failure happens. For this same reason, we cannot replace stacked transistors in a clocked inverter with a single transistor with $2L$ channel length, but the conversion to an equivalent inverter becomes necessary.

5.3 Test Chip Design

We design a test chip that integrates latch array circuits to evaluate the stability characteristics of actual latch circuits. The test chip is fabricated with a 65 nm process technology. Figure 14 illustrates the floorplan of the fabricated chip and Fig. 15 shows the structure of the latch array circuits [16]. 8,192 latches are integrated in the array. Read/write operation for each latch is possible. The test chip contains three types of latch array circuits and they are composed of latches with different gate width from each other as shown in Table 1. The value of gate width in Table 1 is normalized by the minimum transistor size allowed in the process technology and the gate widths of the stacked two pMOS/nMOS transistor are the same. The latches in MEM1 consists of two inverters with different P/N ratios. The latches in MEM2 and MEM3 consist of identical inverters with a well-balanced P/N ratio, and MEM3 has three times larger than MEM2, which corresponds to the cross-coupled inverters B and C in Sect. 5.1.

5.4 Verification for Latches by Measurement

We measured the latch array circuits in the following steps:

1. Write value 1 or 0 to all latches using a high supply voltage.
2. Decrease the supply voltage to V_α mV.
3. Return the supply voltage to the original high voltage.
4. Readout the values of the latches and compare them with the original values written beforehand. The ratio of latches that work correctly for both 1 and 0 is defined as an yield of the latches in V_α mV operation.

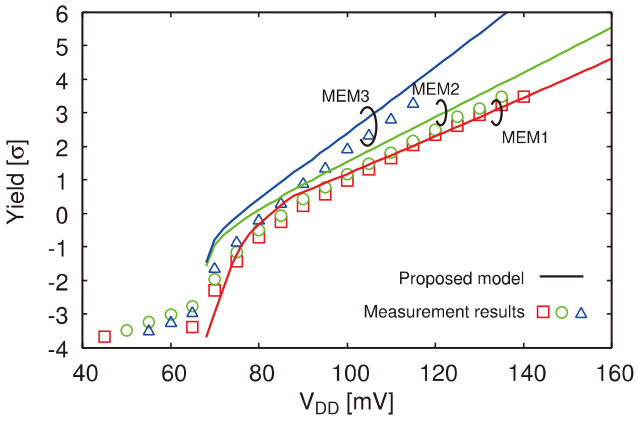

Fig. 16 Comparison with measurement results.

The proposed method needs the process variation information (i.e., *Pelgrom coefficient*). In this verification, we use a reasonable value inferred from the measurement results fabricated by the same process in a previous lot. Figure 16 shows the measurement results. The estimated yields predicted by the proposed method are smaller than the measured yields, but the discrepancy is small and the proposed method provides a good estimation over a wide range of σ values. A possible source of modeling error, besides the error in (1) explained in Sect. 5.1, is that the transistor characteristics used in the proposed method do not precisely represent those of a real chip. The comparison results indicate that our stability analysis method can be useful for the latches fabricated on a real silicon chip and more accurate process parameters can improve the accuracy of the estimated yield.

6. Design Strategies Obtained from the Proposed Model

Since we investigate the stability of latches analytically, some design strategies below can be available from the proposed model.

We confirm analytically that large transistors make the latches robust. The stability of the latches is determined by the distributions of Δu and Δv. Therefore, it is effective to make the standard deviations of Δu and Δv smaller. Since Δu and Δv depends on ΔV_{TH} shown as equation (20), to decrease ΔV_{TH} is effective. According to the Pelgrom's law [17], the standard deviation of V_{TH} is represented as an inverse proportion to the square root of the transistor size. From the above, a simple solution to design robust latches is to enlarge the gate sizes of transistor.

As expressed in Eq. (26), the yield of latches is the sum of four CDF terms. As general characteristic of the sum of CDFs, the largest one of the four CDFs in Eq. (26) becomes the dominant term to determine the yield. Therefore, the yield of latches can be roughly expressed as $\min\{|H_{\mathrm{const.}}|, |L_{\mathrm{const.}}|, |H'_{\mathrm{const.}}|, |L'_{\mathrm{const.}}|\}$. Assume that n_{p} and n_{p} are almost equal, $\min\{|H_{\mathrm{const.}}|, |L_{\mathrm{const.}}|, |H'_{\mathrm{const.}}|, |L'_{\mathrm{const.}}|\}$ is minimized when the drive strengths of the pMOS/nMOS transistors are equal and the P/N ratio of the two inverters in the latches are equal.

The discussion above leads to the following design strategies for enhancing stability of latches:

1. large gate sizes to decrease the variability of the transistors.
2. the well-balanced drive strength of the pMOS/nMOS transistors.
3. the well-equal P/N ratio of the two inverters in the latches

The experiment results explained in Sect. 5 show that the most stable latch circuit is C, followed in order by B, A. In case of measurement results, the most stable latch circuit is MEM3, followed in order by MEM2, MEM1. This result supports the design strategies showed above.

7. Conclusion

In this paper, we propose a stability analysis method for CMOS latches operating in sub-threshold voltage region. The proposed method is based on the idea that approximates the eye diagram of the butterfly curve as a parallelogram. The proposed method shows that the yield of latches can be expressed as the linear sum of the four CDFs of correlated bivariate normal distribution. Simulation results obtained targeting 65 nm and 28 nm process technology models demonstrate the accuracy of the proposed model. Finally, we summarize the design strategies for robust latches obtained from the proposed model.

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