LOW THERMAL EXPANSION OF ELECTRODEPOSITED

COPPER IN THROUGH SILICON VIAS

DINH VAN QUY

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(シリコン貫通電極での銅めっきと低熱膨張特性)

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CHAPTER 1: INTRODUCTION

1.1. Background of Research

1.1.1. Three-Dimensional Integrated Circuits (3DICs)

The progress of semiconductor devices is predicted by Gordon Moore's statement in 1965, known as Moore's law. According to Moore's law, the number of transistors per Integrated Circuit (ICs) doubles about every two years[1]. Significant efforts have been made to keep up with Moore's Law, and more and more transistors have been mounted on the same chip in the last 50 years. However, as transistor scaling reaches physical limits and the associated costs rise dramatically, continually increasing the number of integrated transistors requires new innovations in ICs. Three-Dimensional Integrated Circuits (3DICs) have emerged as a promising technology that has attracted much attention in recent years. Since transistors are located only on one side of silicon chip, the shortest way to connect the upper transistor to the lower transistor is Through Silicon Via (TSV) in 3DIC.
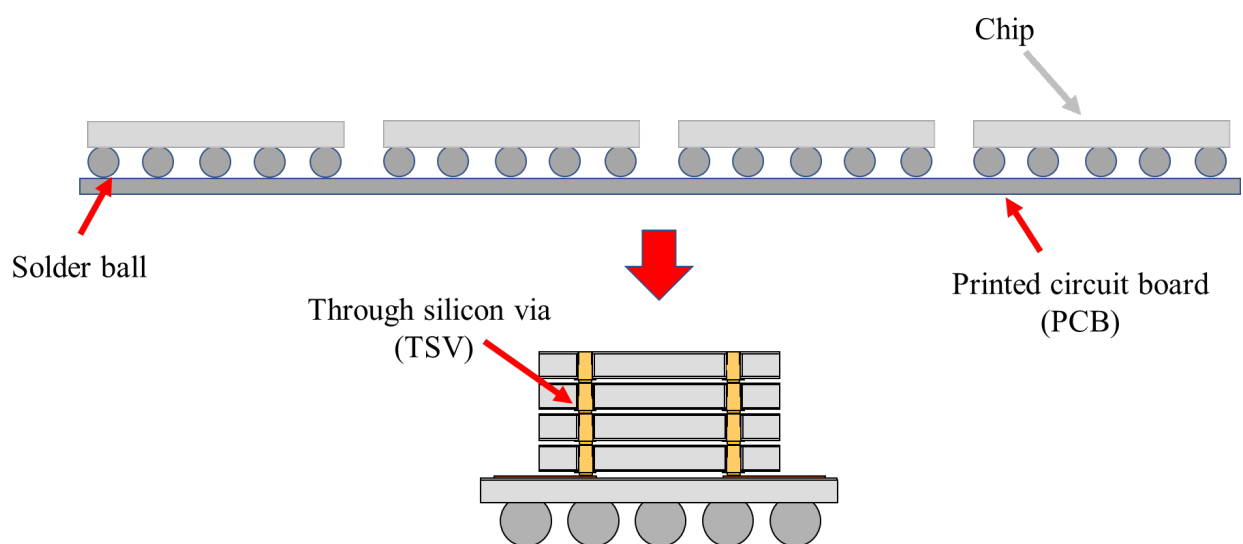

Figure 1. Schematic diagram showing the concept of 2DIC packaging and 3DIC packaging [2].

Figure 1 illustrates the schematic of traditional 2DIC packaging and 3DIC packaging[2]. The upper graph in Figure 1 is the concept of traditional 2D packaging, where four chips are mounted horizontally on a printed circuit board (PCB) by solder bumps. Assuming a chip size of 1 cm, the signal transmission length from the first chip to the fourth chip is 4 cm. On the other hand, the lower graph in Figure 1 illustrates the concept of 3D packaging where four chips are stacked vertically using TSV interconnects. Since four chips are stacked vertically, the packing size is reduced by a factor of four. In addition, since the thickness of silicon chip is only several tens micrometers, stacked chips with TSVs provide the shortest interconnection between different chips. Therefore, 3DIC packaging is the most promising technology that allow to achieve lower power consumption, smaller form factor, higher performance, and more functional devices[3,4]. For example, High Bandwidth Memory (HBM) is a TSV technology-based device. Samsung and SK Hynix are the leader in this market. Figure 2 shows a cross section image of the HBM device produced SK Hynix with 4 DRAM chips (dies) are interconnected through TSVs[5].
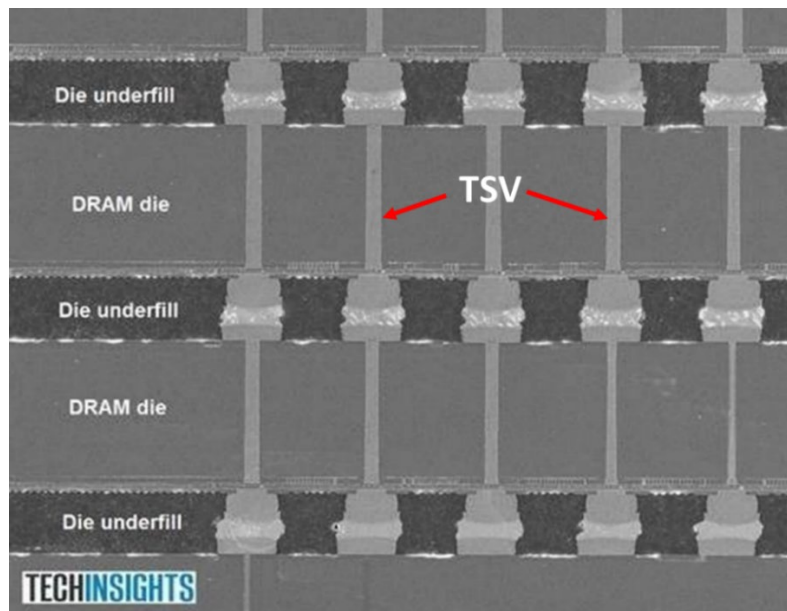

Figure 2. SEM image of HBM with TSV technology (Source: Package Analysis of the SK-Hynix HBM, TechInsights).

TSV technology packaging revenues (M$)

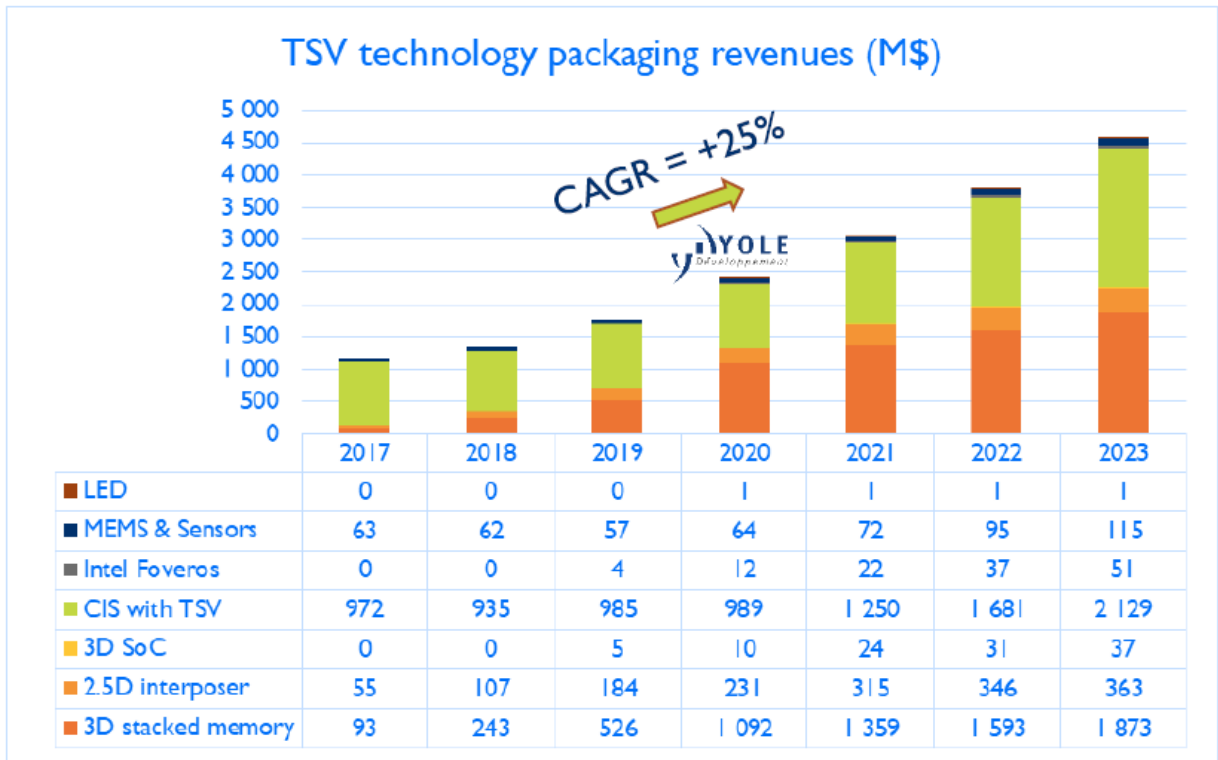|	2017	2018	2019	2020	2021	2022	2023
■ LED	0	0	0	1	1	1	1
■ MEMS & Sensors	63	62	57	64	72	95	115
■ Intel Foveros	0	0	4	12	22	37	51
■ CIS with TSV	972	935	985	989	1 250	1 681	2 129
■ 3D SoC	0	0	5	10	24	31	37
■ 2.5D interposer	55	107	184	231	315	346	363
■ 3D stacked memory	93	243	526	1 092	1 359	1 593	1 873

Figure 3. Global TSV technology packaging market (Source: 2.5D / 3D TSV & wafer-level stacking technology & market updates 2019 report by Yole Development.).

The global TSV technology packaging market given by Yole Development is shown in Figure 3. TSV technology has a bright future with a Compound Annual Growth Rate (CAGR) of 25%. In addition, TSV packaging revenue is estimated to increase to about $ 4.5 billion in 2023, as shown in Figure 3. TSVs is now the preferred interconnect choice for high performance 3D stacked memory and CMOS Image Sensor (CIS). They are also an enabling technology for heterogeneous integration of logic circuits with silicon interposers, Micro Electro Mechanical Systems (MEMS), and sensors. New players who historically were not TSV adopters, such as Intel, are entering TSV market. For example, Intel has entered the TSV market in 2019 with the introduction of Intel Foveros, an advanced 3D face-to-face die stacking packaging process. In the near future, TSVs will also enable Light Emitting Diode (LED) and photonics. CIS accounted for more than 80% of the TSV market in 2017, although this will fall to about 46% by 2023. This is mainly due to the growth of the other TSV applications, led by

3D stacked memories, silicon interposers, MEMS and sensors. The TSV markets for Intel Foveros and 3D System on Chip (SoC) are expected to reach around $51 million and $37 million by 2023, respectively.

1.1.2. Through Silicon Via (TSV)

1.1.2.1.Via First, Via Middle, and Via Last Process

Through-silicon via (TSV) is the core of 3DIC technology. The TSV concept was invented by William Shockley in 1956[6], and was further developed by in 1964 by IBM researchers M. Smith and E. Stern[7]. At the beginning, TSV was not originally intended for 3DIC. The first 3DIC stacked chips fabricated with a TSV process were invented in 1980s in Japan[8]. Depending on the order of TSV formation step to the transistor formation step (or FEOL: Front End of Line) and wiring step (or BEOL: Back End of Line), TSV fabrication is categorized as via first, via middle, and via last process.

Figure 4 shows the schematic flow of via first, via middle, and via last processes[9]. In the via first process, TSVs are fabricated before the transistor formation and wiring step. Meanwhile, TSVs are made between the transistor formation and wiring step in the via middle process. Finally, in the via last process, TSVs are manufactured after the formation of transistor formation and wiring step. Among these processes, via middle is the most common used in the industry for achieving the highest. The major drawback of the via middle process is that TSV is exposed to very high temperature (400-600°C) during insulator formation step. This high exposure temperature causes some serious reliability problems, leading to the failure of electronic devices. In addition, the TSV formation (especially, TSV etching, Cu electrodeposition, and Cu CMP) in via middle process is expensive. These problems are discussed in more detail in section "1.1.3. TSV challenges" of this thesis.
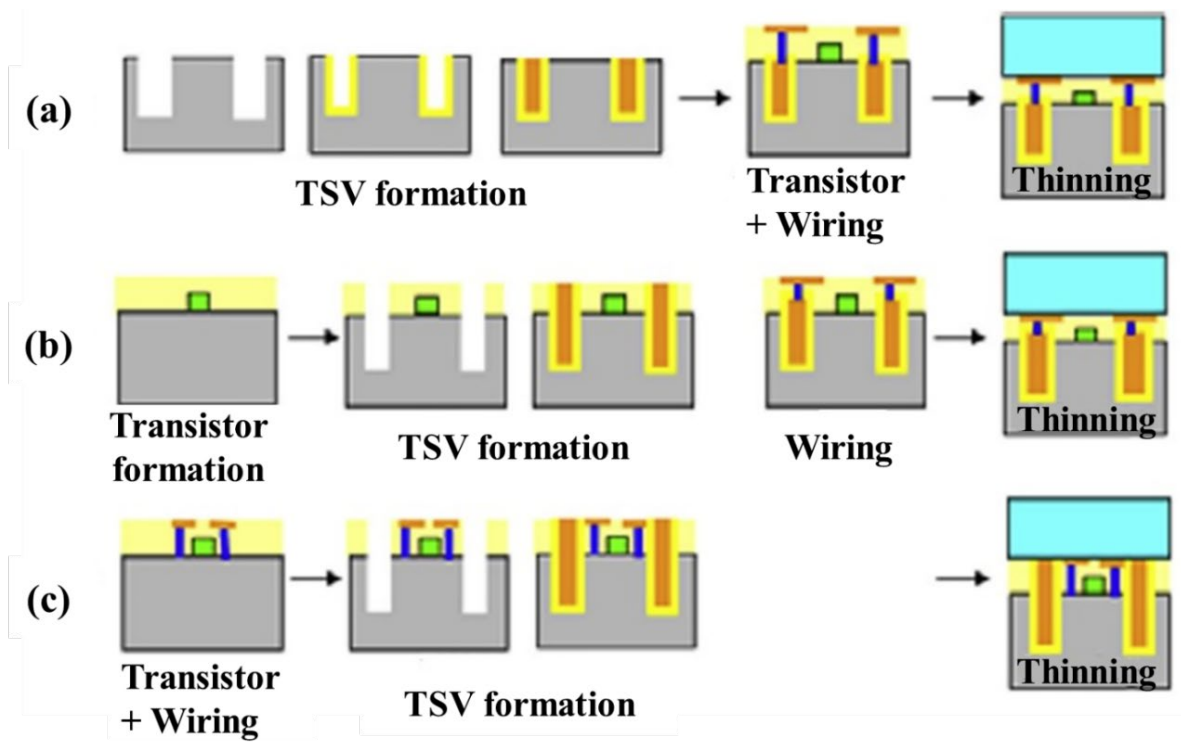
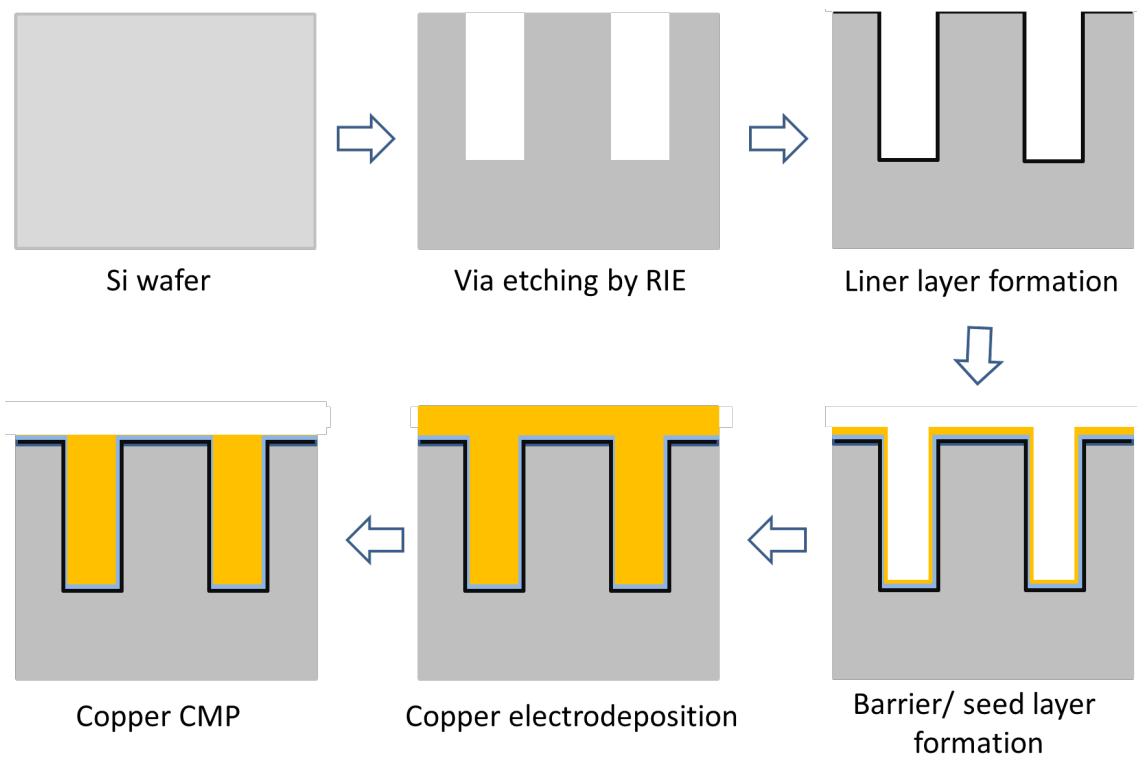*Figure 4. Schematic flow of (a) via first, (b) via middle, and (c) via last processes [9].*

Si wafer   Via etching by RIE   Liner layer formation

Copper CMP   Copper electrodeposition   Barrier/ seed layer formation

Figure 5. Schematic flow of TSV formation process.

Typical TSV formation process is shown in Figure 5. The first step is via etching by Reactive Ion Etching (RIE). Next, an insulator layer, a barrier layer, and a seed layer are formed. After that, TSV is filled by copper electrodeposition. Finally, TSV is polished to remove copper overburden by Chemical Mechanical Polishing (CMP).

1.1.2.2.1. TSV Etching

TSV etching is primarily done by using RIE to create high aspect ratio vias. The most commonly used process for TSV RIE is the Bosch process. The Bosch process basically executes two steps alternately, one etching step followed by a passivation step, as shown in Figure 6[10]. Sulfur hexafluoride (SF_6) is commonly used as an etchant for silicon etching in the etching step. Octafluorocyclobutane (C_4F_8) gas, on the other hand, is used in the passivation step and produces a good passivation film to prevent lateral silicon etching during the next etching step[10,11]. During the Bosch process, a residual passivation film remains at the bottom of the TSV as an etching byproduct[12,13]. The residual passivation film prevents subsequent metal deposition. Therefore, additional de-passivation step by using O_2 and Ar plasma is used to remove the residual passivation film at the bottom of the TSV[13].

TSV etching using the Bosch process has challenges, such as controlling the roughness of the sidewalls and the uniformity of via depth[14]. These challenges can be minimized by optimizing the processing parameters in both the etching and passivation steps, since the etching rate, uniformity, and selectivity are highly dependent on the processing parameters in both the etching and passivation steps.
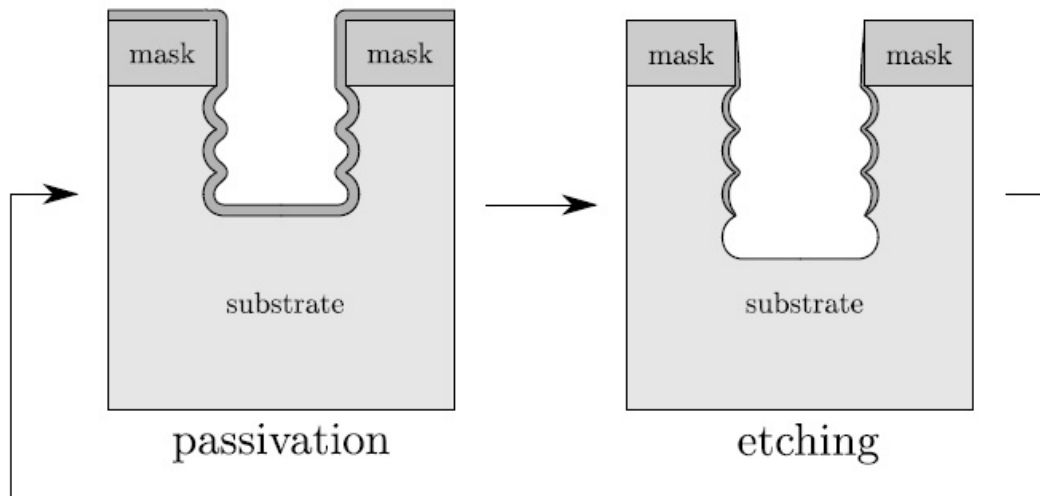
Figure 6. Schematic of Bosch process [10].

1.1.2.2.2. Dielectric Insulator Layer

To sufficient insulate the filled copper from the surrounding silicon substrate, a dielectric insulator is essential for the TSV. Typical requirements for a TSV dielectric layer include good step coverage and thickness uniformity, low stress, no leakage current, and high breakdown voltage[14,15]. The most commonly used material for TSV insulator is SiO_2[16–19]. The methods for depositing the SiO_2 insulator depends on the TSV integration process (via first, via middle, and via last process). There are basically two options for insulator deposition, namely: Plasma-Enhanced Chemical Vapor Deposition (PECVD) of SiO_2, Atmospheric Pressure Chemical Vapor Deposition (APCVD) of SiO_2. The PECVD process uses liquid tetraethyl orthosilicate (TEOS) $Si(OC_2H_5)_4$ as a source of silicon. The growth rates SiO_2 films by PECVD are high and the process temperature is lower than 400ºC[19]. The APCVD process uses tetraethyl orthosilicate (TEOS) $Si(OC_2H_5)_4$ and O_3 as the precursors. By using O_3 instead of O_2, the deposition temperature can be reduced in the range of 400ºC-600ºC[17,18]. However, since SiO_2 formed by APCVD has a high residual stress, the thickness of APCVD SiO_2 should be less than 0.5 μm[20].
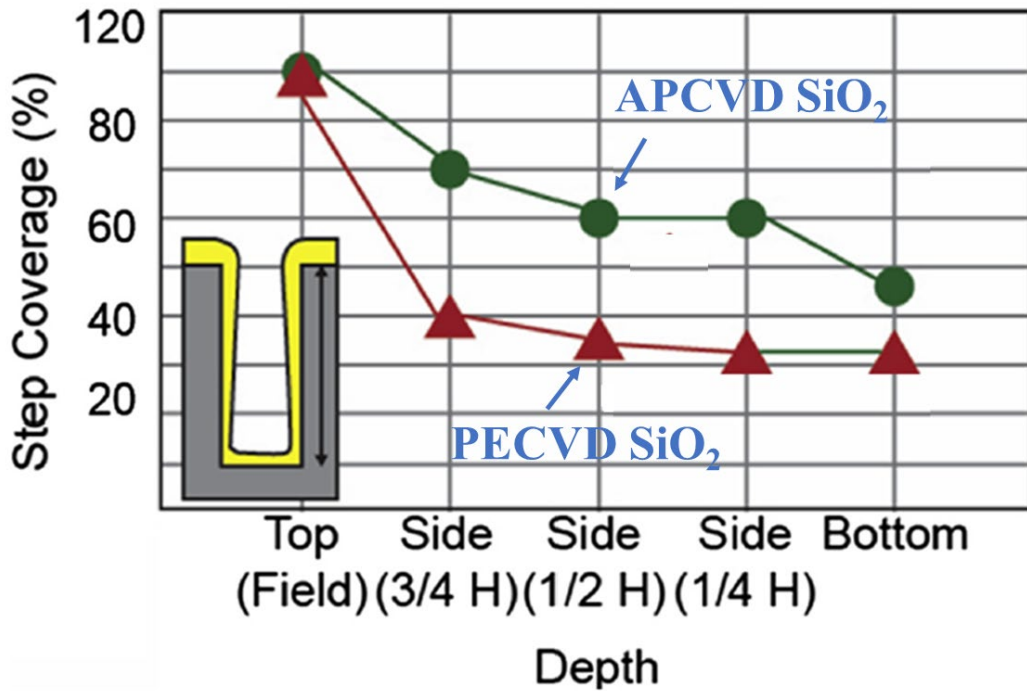
Figure 7. Comparison of step coverage of SiO₂ formed by APCVD and PECVD from top to

bottom of TSV [21].

Figure 7 compares step coverage of SiO$_2$ between APCVD and PECVD from the top

of the TSV, along the sidewalls, to the bottom[21]. The x-axis is the comparison position along

the TSV, and the y-axis is the step coverage. In Figure 7, the step coverage decreases

continuously for both PECVD and APCVD as the distance goes from top to bottom of the TSV.

However, it can be seen that the uniformity of SiO$_2$ formed by PECVD at all positions except

the top of the via is less than 50%. In contrast, APCVD SiO$_2$ has better step coverage than

PECVD SiO$_2$, and therefore APCVD is commonly used to form the SiO$_2$ insulator[16,19,21].

1.1.2.2.3. Barrier and Seed layer

After deposition of the dielectric insulator, a barrier layer is formed, followed by a

copper seed layer. The barrier layer not only acts as an adhesion layer between the dielectric

layer and the filled copper, but also prevents copper diffusion during the annealing process.

The commonly used materials as barrier layer are Ti, Ta, TiN, and TaN[22–24]. Depending on the

size of the TSV, Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD) are used to deposit the barrier layer. Ta and Ti barrier layers can be deposited using the PVD method. The advantage of the PVD method is that the temperature during deposition is low. However, for high aspect ratio TSVs (> 10: 1), PVD is inappropriate because of poor step coverage[25]. TiN or TaN barrier layers are typically deposited using the CVD method. Compared with the PVD method, the CVD method formed a more uniform barrier layer, but required a higher deposition temperature.

In the next step, copper seed is deposited on the barrier layer by PVD before filling the TSV with the copper electrodeposition process.

1.1.2.2.4. Copper Electrodeposition

After the barrier and seed layer deposition, the TSV is filled by electrodeposition. Copper is widely used as a filling material for TSV because of its low resistivity. There are three possibility of TSV filling profiles, as shown in Figure 8[26]. In the subconformal profile, the copper electrodeposition rate at the TSV opening is higher than at the via bottom. This difference in electrodeposition rate causes a narrowing of the TSV opening, leading to void formation when electrodeposition process is complete. In the conformal profile, copper is electrodeposited at the same rate on TSV opening, TSV sidewall, and TSV bottom. Subconformal electrodeposition results in the appearance of seams at the final stage of TSV filling. Subconformal and conformal profile are caused by the depletion limit of cupric ions inside the TSV[27]. Void and seam cause reliability problems. Therefore, the optimal filling profile is superconformal (or bottom-up filling) where the copper electrodeposition rate at the bottom of the TSV is greater than that at the TSV opening.
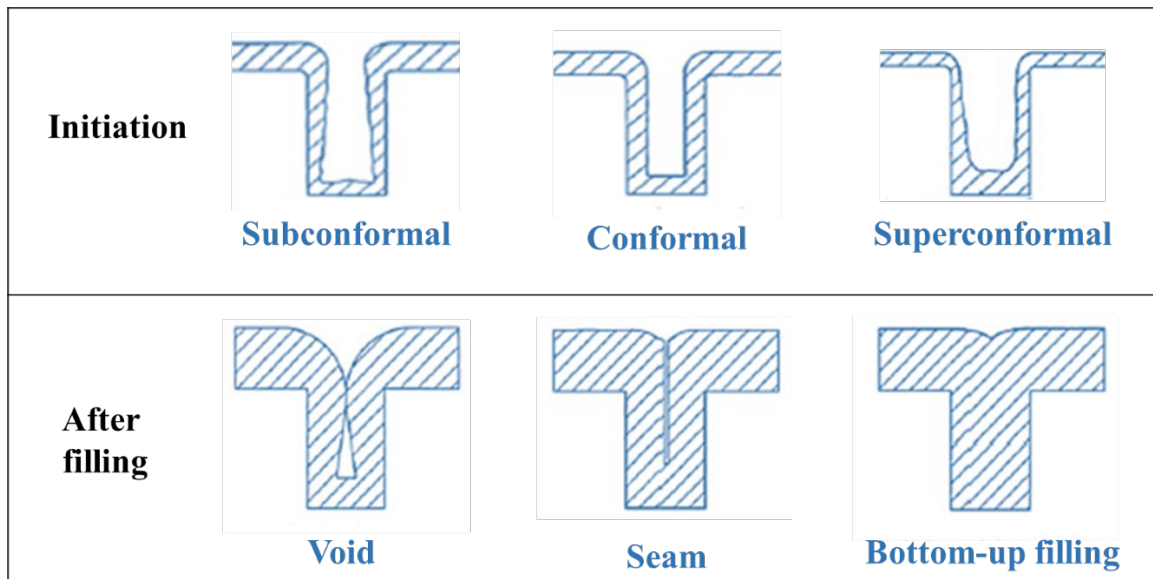
Figure 8. Common copper filling profiles in TSV [26].

Copper sulfate and sulfuric acid are the basic components of the electrolytes that are widely used in the industry for copper electrodeposition. Copper sulfate acts as the source of copper ions, and sulfuric acid increases the conductivity of the electrolyte. In addition, chloride ion, a set of organic additives (inhibitor, accelerator, and leveler), and Periodic Pulse Reverse (PPR) current are used to accelerate electrodeposition rate at the via bottom and inhibit the electrodeposition rate at the via outside.

Additives chemistry

The HCl serves as a source of Cl^- ions, plays an important role in electrodeposition of copper, including promoting accelerator and supporting inhibitor by forming the complexes with accelerator and inhibitor[28,29].

A first type of organic additive used for copper electrodeposition is the inhibitor (suppressor). Inhibitors are usually long-chain polymers (molecular weight 1000-20000). Inhibitor is mainly adsorbed on the via outside, on the via sidewall near the via opening, and inhibits copper electrodeposition at these positions. The most commonly used inhibitor is polyethylene glycol (PEG), which has the chemical structure shown in Figure 9. Inhibitors inhibit electrodeposition by adsorbing on the copper surface. However, PEG alone does not

readily adsorb to the copper surface. In the presence of Cl⁻ ions, the adsorption strength of PEG on the copper surface is greatly increased, resulting in a significant inhibition of copper electrodeposition. The formation of Cu-Cl-PEG complex has been widely used to explain the strong adsorption of PEG on copper surfaces in the presence of Cl⁻ ions[30–33]. Based on a surface-enhanced Raman spectroscopy study, Z. V. Feng et al. proposed a structural model for the Cu-Cl-PEG complex, as shown in Figure 10[33]. In this model, a cuprous center is complexed by two ether oxygen ligands from PEG and one Cl⁻ ligand.
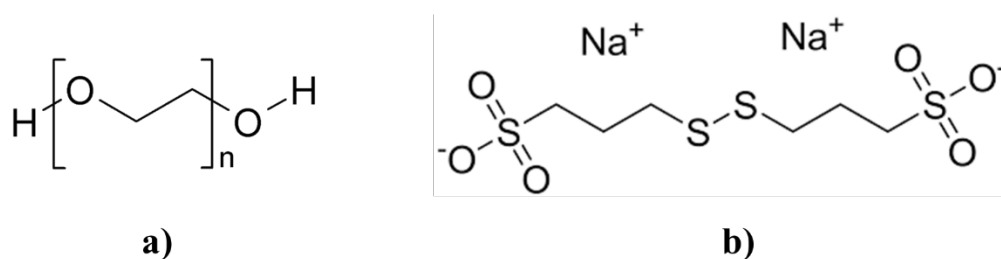
Figure 9. Chemical structures of (a) PEG, and (b) SPS.

Figure 10. Structural model of a Cu-Cl-PEG complex [33].

A second type of organic additive is the accelerator (brightener). Accelerators are small molecules, usually sulfur-containing compounds. The accelerator blocks the adsorption of the inhibitor and slowly replaces it. It also penetrates inside the via and increases the electrodeposition rate at the via bottom. A well-known accelerator used in the industry is Bis-

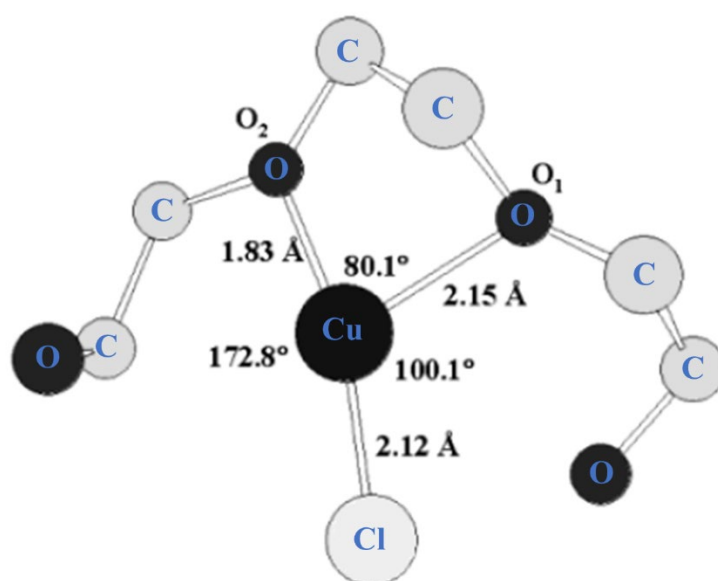(3-sulfopropyl) disulfide (SPS), as shown in Figure 9. Similar to PEG, SPS requires the support of Cl^- ion to accelerate copper electrodeposition. Several researches have been conducted on the acceleration mechanism of SPS[34–36]. The two famous mechanisms are curvature enhanced accelerator coverage proposed by T. P. Moffat et al.[34], and cuprous ion related mechanism proposed by K. Kondo et al.[36], as shown in Figure 11. First, SPS is reduced to MPS by the adsorbed chloride. Next, MPS reacts with cupric ions to form Cu(I)thiolate complex intermediate. After that, the Cu (I) thiolate complex floats to the via bottom due to the vortex. Cu(I)thiolate complex is then oxidized to SPS, releasing cuprous ion. The released cuprous ion is quickly electrodeposited as copper, causing acceleration at the bottom of the via.
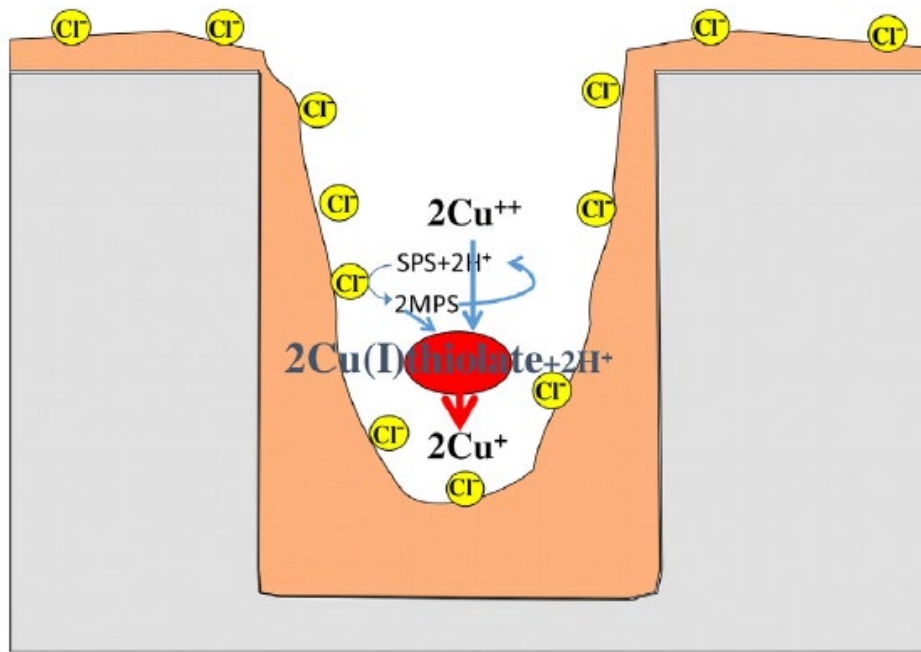
Figure 11. Model of SPS acceleration mechanism [36].

A third type of organic additive is the leveler. There are thousands of types of levelers, usually quaternary nitrogen compounds. Levelers disable the accelerator, and exhibit an inhibition effect during copper electrodeposition. Levelers are also used to reduce the thickness of the overburden to improve overall flatness. Figure 12 shows the changes in the surface of copper electrodeposited at different concentrations of the leveler[37]. Copper bumps are clearly

observed in the absence of the leveler, but disappear at the leveler of 60 µmol/L. For 800 µmol/L of leveler, the TSV is not completely filled and voids may form. This is probably due to excessive leveler diffusion into the TSV, reducing copper electrodeposition rate at the TSV bottom. Moreover, in the Chapter 3-5 of this thesis, I have found out that another function of the leveler is to reduce the thermal expansion of electrodeposited copper.
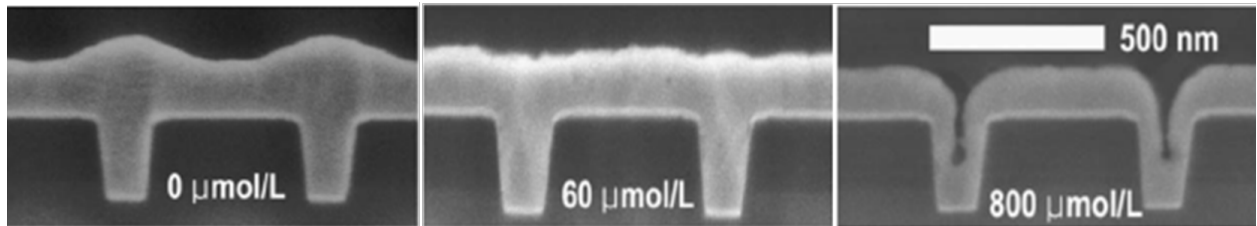

Figure 12. Leveler concentration dependence of electrodeposited copper surface. [37].

Periodic pulse reverse (PPR) current

Periodic pulse reverse (PPR) current has been widely in copper electrodeposition for TSV filling. Figure 13 illustrates a typical PPR current waveform. In Figure 13, i_{on} and i_{rev} stand for the cathodic current (or electrodeposition current) and anodic current (or stripping current), respectively, and t_{on}, t_{rev} and t_{off} stand for the electrodeposition time, stripping time and pause time, respectively.

The cuprous (Cu^+) ion plays very important role in the bottom-up TSV filling. K. Kondo et al. verified the relation between the Cu^+ ions and the acceleration effect of the accelerator at the via bottom[38]. Based on an electrochemical method, J. R. White found that the Cu^+ ions in copper dissolution were 1000 times higher than that during electrodeposition[39]. This means that as the reverse current of the PPR current increases, the Cu^+ ion concentration inside the via increases, and the bottom-up TSV filling is achieved[40]. All five parameters of the PPR current can be easily controlled, so the PPR current reduces voids and improves TSV filling performance.
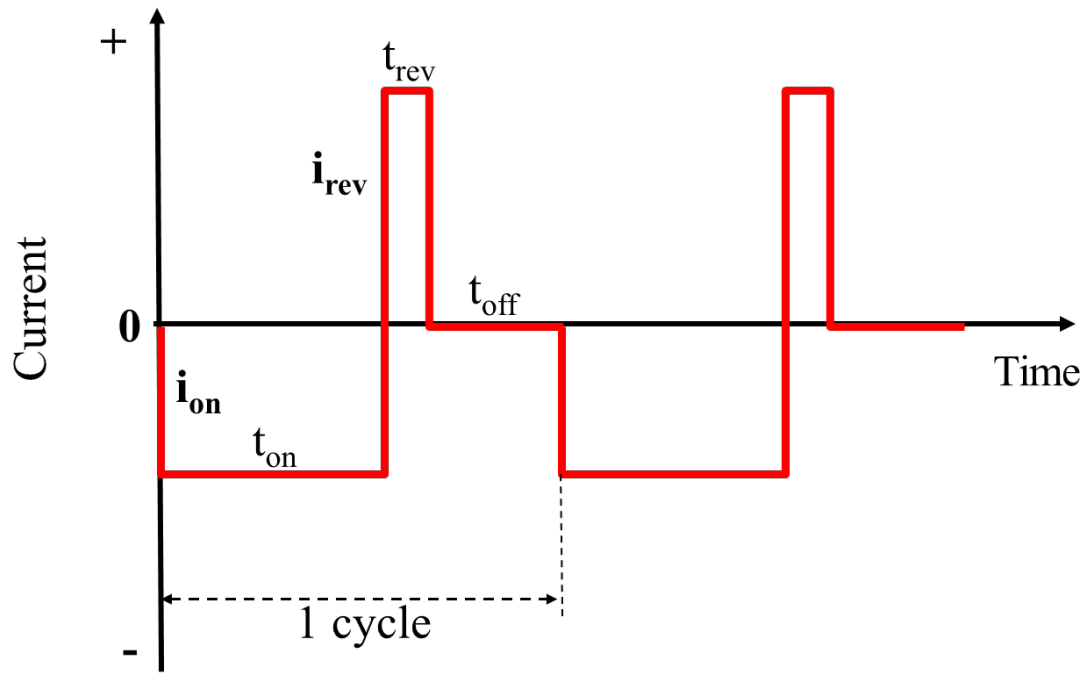
Figure 13. A typical periodic pulse reverse (PPR) current waveform.

1.1.2.2.5. Copper Chemical Mechanical Polishing (CMP)

After copper electrodeposition step, the copper overburden must be removed by a planarization process called chemical mechanical polishing (CMP). In CMP, the wafer is placed face down on a rotating pad where the slurry is dispensed. Normally, copper CMP consists of a minimum of two steps. The first step is the removal of copper overburden stopping at the barrier layer. The second step is to remove the barrier layer that stops at the dielectric insulator layer.

1.1.3. TSV Challenges

1.1.3.1. High Speed TSV Filling

Figure 14 is a pie chart of the breakdown of TSV production costs[41]. In Figure 14, copper electrodeposition, bonding, barrier/seed layer formation, and via etching costs account for 41%, 31%, 20% and 8% of total TSV production cost, respectively. In other words, copper electrodeposition is the most expensive step of TSV production process. Therefore, TSV cost savings are largely managed by copper electrodeposition cost reduction. There are several ways to reduce the cost of copper electrodeposition, including using latest electrodeposition tools and reducing the time required for electrodeposition. However, the latest electrodeposition tools are expensive. Furthermore, large clean room areas need to accommodate a large amount of electrodeposition tools. Therefore, electrodeposition time must be reduced to reduce TSV production costs. Increasing current density is a promising solution to reduce electrodeposition time. However, if the current density is too high, constriction occurs at the TSV opening and voids will be formed. Acid residues remaining in the voids can cause reliability problems. Therefore, high speed TSV filling without voids is important and it will be examined in this research.
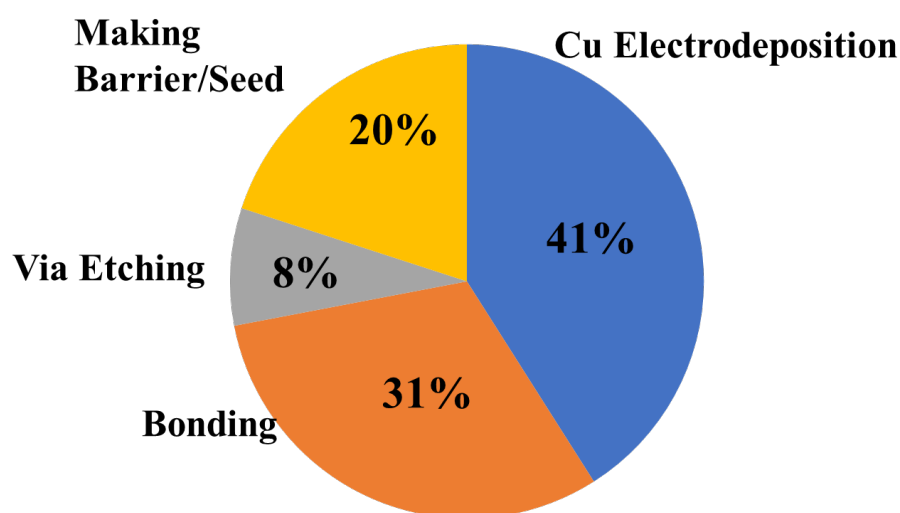

Figure 14. TSV production cost [41].

1.1.3.2. Thermal Expansion Coefficient (TEC) Mismatch Problems

Copper is widely used as a filling material for TSV because of its low resistivity. Despite the advantages of using copper as the filling material, copper TSV has its drawback due to thermal expansion coefficient (TEC) mismatch between copper and surrounding silicon. Copper has a high thermal expansion coefficient (TEC) of $17 \times 10^{-6}/°C$, while the TEC of silicon is only $2 \times 10^{-6}/°C$. During the SiO_2 formation of the wiring step in via middle process, copper TSV is exposed to a high temperature between $400°C$ and $600°C$. As shown in Figure 15, due to the large thermal expansion coefficient (TEC) mismatch between the silicon substrate and copper, copper expands much more than silicon, causing high thermal stresses in all directions during the manufacturing process. These thermal stresses can lead to failure of the microelectronic device.
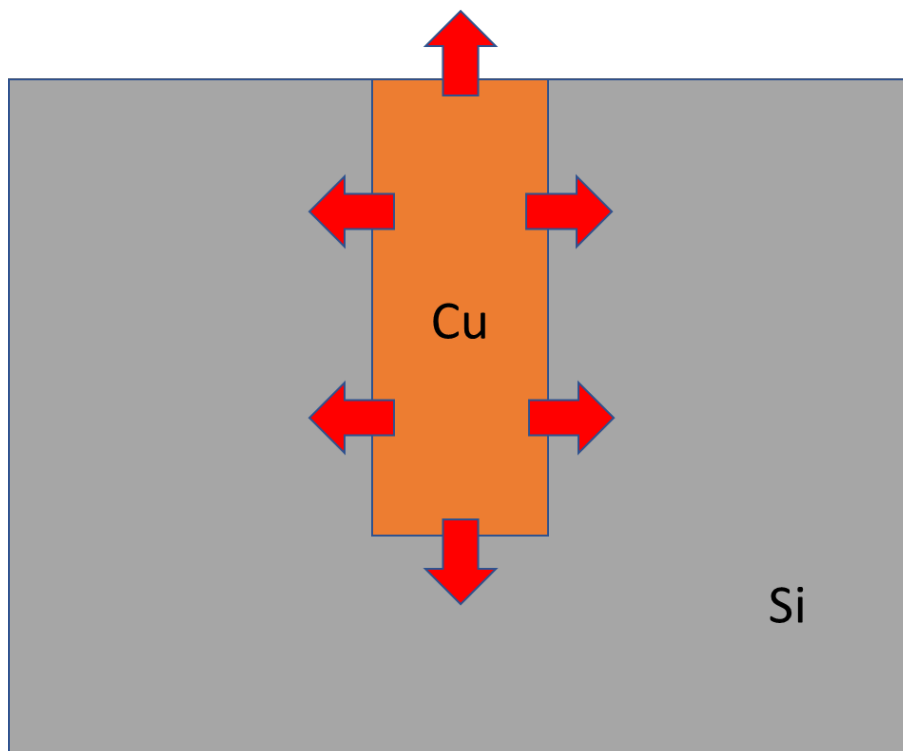

Figure 15. TEC mismatch induced thermal stress in TSV structure.

However, at the bottom corner of the TSV, the thermal stress due to the mismatch of TEC between copper and silicon cannot be released. The Thermal stress causes cracks in the

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silicon at the bottom corner of the TSV[42,43]. Figure 16 shows the cross-sectional SEM images of TSV after annealing at 200°C, and 400°C cyclic annealing. In Figure 16a, no cracks are observed in the bottom corner of TSV after post annealing at 200°C. However, when the annealing temperature rises to 400ºC, long cracks are seen in the silicon, as shown in Figure 16b. Crack in silicon can cause leakage currents into the silicon bulk, leading to serious TSV reliability problems.
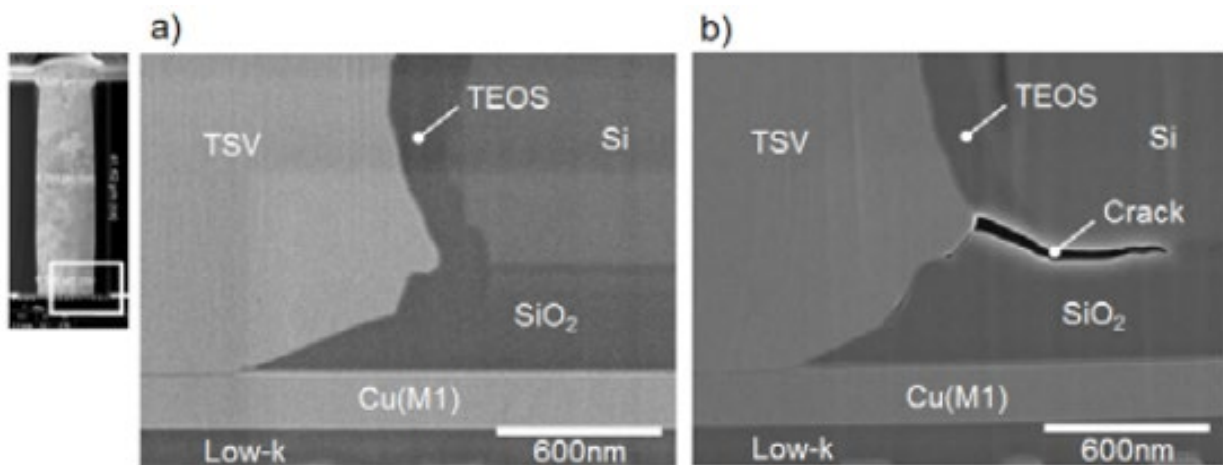
Figure 16. Cross sectional SEM image of TSV (a) after annealing at 200 °C, and (b) after 400 °C cyclic annealing [43].

In addition, thermal stress also causes voids and delamination[43–45] at the copper-silicon interface. Figure 17 shows a cross-sectional SEM images of the interface between copper and the dielectric layer after annealing at 200°C, and 400°C cyclic annealing. After annealing at 200°C, there are small voids along the interface between the copper and the dielectric layer, as shown in Figure 17a. Furthermore, as the annealing temperature rises to 400°C, voids become larger, causing delamination at the interface between the copper and the dielectric layer. Voids and delamination are attributed to the poor adhesion and poor coverage of the dielectric insulator layer.
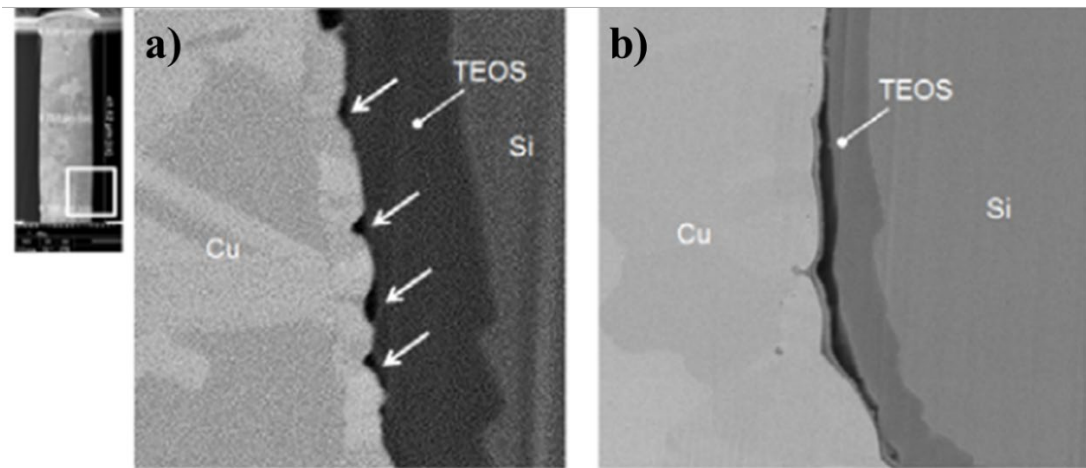
Figure 17. Cross sectional SEM image of interface between copper and dielectric layer (a)

after annealing at 200 °C, and (b) after 400 °C cyclic annealing [43].

The upward thermal stress in Figure 15 is partially relieved by copper pumping[46–48]. Figure 18 is a top-view SEM image of copper pumping by annealing and Figure 19 is the cross section of copper TSV after annealing. In both Figure 18 and 19, copper pumping is evident with the copper height is higher than the silicon surface when annealing. However, copper pumping destroys the wiring above the TSV. Therefore, copper pumping also raises reliability problems.

Figure 18. Top-view SEM image of copper pumping in TSV.

Figure 19. Cross-sectional SEM image showing copper pumping after annealing [48].

Figure 20. Keep out zone (KOZ) area around the TSV.

Due to the TEC mismatch between copper and silicon, the silicon surrounding the TSV of copper is also subject to significant thermal stress. The induced thermal stress changes the

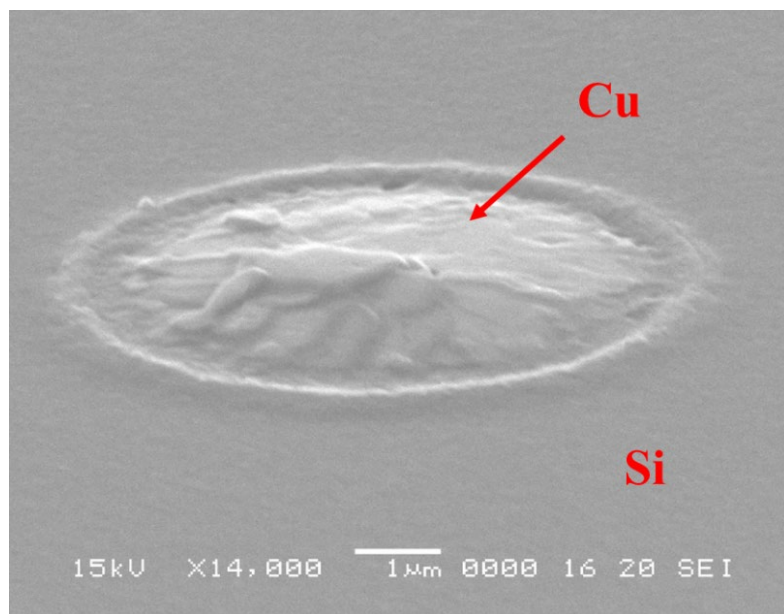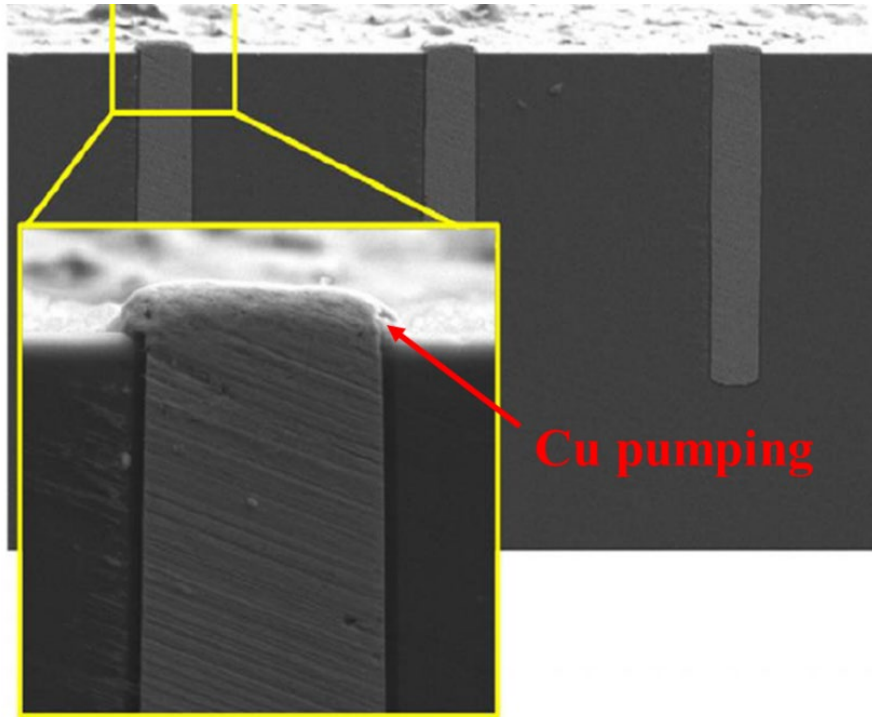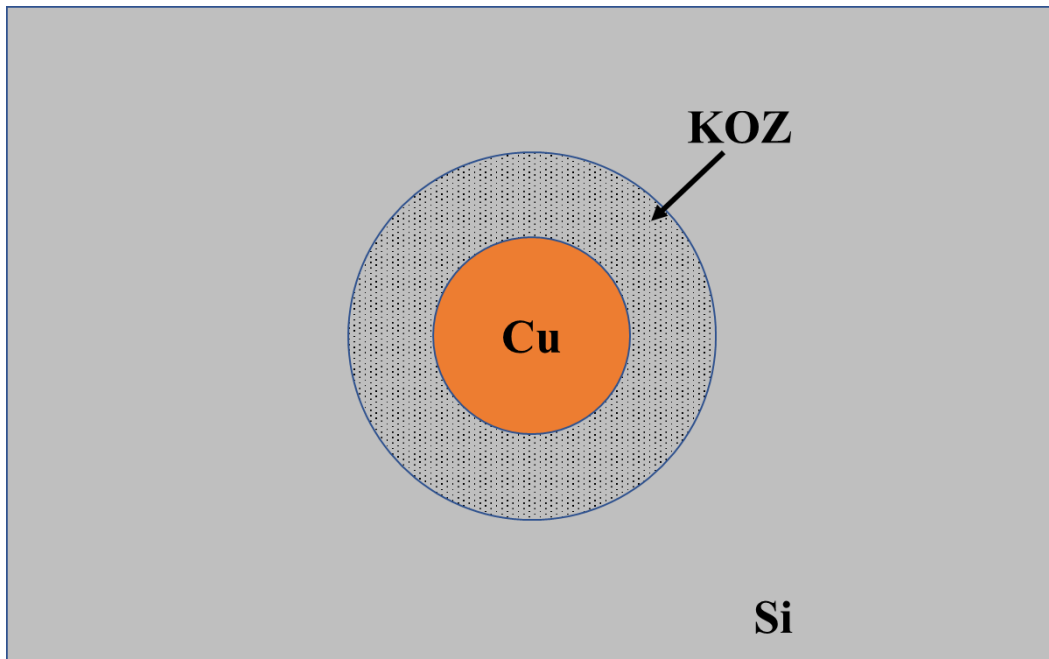electrical resistivity and mobility of silicon around the TSV[49]. The changes in mobility may result in timing violations in the circuit. Therefore, a keep out zone (KOZ) area[50–52] has to be properly defined. Technically, KOZ is defined as the area around a TSV where the transistors cannot be formed to prevent the effects leading to device failure. KOZ is usually considered to be an area around the TSV where mobility changes exceed 5%[52].

Among the aforementioned problems, copper pumping and KOZ are the main problems. Therefore, this thesis focuses on these problems.

1.2. Review of Existing Research

Two parts of researches are reviewed in this section. The first part is related to high speed TSV filling without voids to reduce the total TSV fabrication cost. The second main part is related to the researches based on the TEC mismatched problem such as copper pumping and thermal stress in copper TSV.

1.2.1. High Speed TSV Filling

Copper electrodeposition accounts for 41% of the total production cost of TSV and is the most expensive step in the TSV production process[41]. Thus, reduction of the copper electrodeposition cost is necessary. There are several ways to reduce the cost of copper electrodeposition, including using latest electrodeposition tools and reducing the time required for electrodeposition. However, the latest electrodeposition tools are expensive. Furthermore, large clean room areas need to accommodate a large amount of electrodeposition tools. Therefore, electrodeposition time must be shortened to reduce TSV production costs. Numerous studies have been investigated the factors that affect copper electrodeposition to reduce the filling time[53-72].

PPR current is one of the factors that can be used and optimized for high speed TSV filling[53–57]. For example, J.-J. Sun et al. first successful filled the 10×70 µm TSV in 12 hours[55].

K. Kondo et al. 's results showed that a 10×70 μm TSV was completely filled in 60 minutes by using optimized PPR current to remove voids at the TSV center[56]. In addition, S. C. Hong et al. achieved 80 minutes of filling time for 30×60 μm TSVs using a three-step PPR current[57].

Changing the TSV shape from conventional columnar to conical shape greatly reduced TSV filling time[58–60]. According to a K. Kondo et al. research[58], the filling time decreased from 60 minutes at −10 mA/cm^2 for 30×50 μm columnar TSVs to 20 minutes at −28 mA/cm^2. Also, H. Hoang and K. Kondo achieved completely filling of 3×27 μm and 2×16 μm conical TSVs in only 3 minutes[59] and 30 seconds[60], respectively.

Additives are the key for obtaining bottom-up TSV filling. Various accelerators, inhibitors and levelers have been investigated in previous studies for high speed TSV filling[61–72]. For example, T. Hayashi et al. introduced V-shaped bottom-up filling of 10×70 μm TSV in 35 minutes using diallylamine additive as leveler[70]. T. P. Moffat et al. reported donut-shape bottom-up filling of 8×56 μm columnar TSVs in 17 minutes using only Tetronic 701[71]. M. J. Kim et al synthesized new TEG-based levelers and achieved perfect 9x40 μm TSV filling within 750 seconds[72]. There are thousands of additives, each with different effects on TSV filling. Therefore, there is still room for reducing TSV filling times with new novel additives.

1.2.2. TEC Mismatch Challenges: Copper Pumping and KOZ

During the SiO$_2$ formation in via middle process, copper TSV is exposed to a high temperature between 400°C and 600°C. Due to the large thermal expansion coefficient (TEC) mismatch between the silicon substrate and copper, copper expands much more than silicon, causing high thermal stresses. Thermal stress has caused some serious reliability problems. Copper pumping and KOZ are the main reliability problems. Therefore, current researches on copper pumping and KOZ are reviewed here.

In this part, the research review is divided into three following fields: (1) Review of researches related to the effects of annealing condition and numerical studies. (2) Review of researches related to other TSV filling materials that are not pure electrodeposited copper. (3) Review of researches related to TSV geometry and TSV structure.

(1) Review of studies related to the effects of annealing condition and numerical studies.

The first field is a review of studies related to the effects of annealing condition, and numerical studies of thermal stress and copper pumping. After copper TSV fabrication, copper TSV is exposed to a high temperature between 400°C and 600°C during the SiO$_2$ formation in via middle process. Exposure to high temperatures changes the properties of electrodeposited copper. Several studies have used scanning electron microscope (SEM), nanoindentation, and electron backscatter diffraction (EBSD) to investigate the effects of annealing on changes in copper properties[73–77]. For instance, P. Saettler et al.[73] investigated the microstructure of electrodeposited copper in TSVs at different annealing temperatures. It can be seen that no significant grain growth is observed up to 250°C. At temperatures above 250°C, copper grain growth is appearance, and the size of the copper grains increases with the annealing temperature. T. Jiang et al. and J. D. Messemaeker et al. have studied the correlation between copper microstructure and copper pumping[75,78]. In addition, the effect of annealing conditions on copper hardness and elastic modulus was also studied by C. Okoro et al.[76]. Nanoindentation measurements showed that high temperature annealing reduces hardness and elastic modulus of electrodeposited copper.

There are many works that studied about copper pumping when annealing. Laser microscope, interferometer, atomic force microscopy (AFM) have been applied to study copper pumping. All of the above measurements showed that the copper pumping height increased with increasing annealing temperature[46,77,79–81]. Furthermore, I. D. Wolf et al. [81] reported that

multiple long time annealing and CMP can reduce the copper pumping. However, the CMP is a very expensive process.

Numerical models also are created to simulate copper pumping and thermal stress in silicon[46,47,82–84]. N. Nabiollahi et al. numerically simulated copper pumping during annealing by using finite element analysis[83]. B. Liu et al. simulation results showed that a von Mises stress peak appeared at the interface between silicon and copper TSV; and the von Mises stress gradually decreased as the distance from the TSV increased[46]. These numerical studies help understand the reliability problems of copper TSVs under various annealing conditions.

(2) Review of researches related to other TSV filling materials that are not pure electrodeposited copper.

The second field is review of researches related to TSV filling materials. It is necessary to find a fundamental solution to inhibit the copper pumping and thermal stress problem. One direct solution to reduce Cu pumping in TSVs is to minimize TEC mismatch between copper and silicon substrate. TEC mismatch can be minimized by replacing Cu by a metal having a lower TEC value than copper or alloying copper with a metal having a lower TEC value[85–88]. For example, Kikuchi et al. succeeded in depositing TSV uniformly with W metal which has TEC value of 4.5 x 10^{-6}/ºC[85]. M. H. Roh et al. tried to inhibit the copper pumping by using Cu-W alloys. The results showed that the TEC of Cu-7.6 %wt W was only 10.8×10^{-6}/ºC. The pumping height also decreased from 1.369 μm for Cu to 0.465 μm for Cu-7.6%wt W[86]. H. S. Jung et al. investigated the effect of Cu-Ni alloy on TSV pumping at various annealing temperatures. The 92% wt Cu-8% wt Ni alloy TSV showed low pumping height and low von Mises stress at temperatures below 350ºC. At temperatures above 350ºC, the pumping increased and the von Mises stress of the Cu-Ni via increased due to increased Cu creep

deformation[87]. However, the resistivity of these metal and alloys is higher than that of copper, and furthermore, etching is difficult.

Recently, silicon carbide (SiC) particles and carbon nanotubes (CNTs) have also been tested for TSV filling[89–93]. S.H. Kee et al.[89] attempted to reduce copper pumping of 30x60 μm TSVs by adding of SiC particles into the electrolyte. It was confirmed that the pumping height decreased from 1.12 μm for Cu TSV to 0.164 μm for Cu/SiC TSV. However, the aspect ratio of TSV is very low, and the resistivity of Cu/SiC composite is higher than that of copper. S. Sun et al.[92] filled the TSV with a novel CNT/Cu composite. CNT/Cu composite is a promising material because it has low resistivity and low TEC value. However, growing CNTs in TSV requires special techniques, and it is difficult to control the uniform distribution of CNTs.

(3) Review of researches related to TSV geometry and TSV structure.

The third field is review of researches related to TSV geometry and TSV structure. The thermal stress of copper TSV has been studied with different structural designs, such as the impacts of the diameter, the pitch, and the geometry of TSVs[94–96]. According to K. H. Lu et al.[94] and J. Pang et al.[95] researches, the larger the TSV diameter, the greater the stress acting on the surrounding silicon. Therefore, downsizing TSV diameter is a useful way to reduce the thermal stress. Also, J. Pang suggested that the TSV pitch should be larger than 3.5 times TSV diameter to prevent the interaction between two adjacent TSVs[95]. J. Zhou et al.[96] studied the role of different TSV geometry designs on the thermal stress. The results suggested that the stiffness of TSV sidewall has an important effect on the thermal stress of the copper TSV.

The liner layer functions as a buffer or cushion for thermal stress, as it mechanically bonds copper to silicon. Therefore, thicker liner or liner which has lower Young's modulus can relieve thermal stresses, reduce copper pumping and KOZ. Several researches have been conducted to investigate the effect of liner thickness and polymer liner on the reduction of

copper pumping and KOZ[97–102]. J. D. Messemaeker et al.[97] investigated the effect of the liner thickness and the liner elastic modulus on copper pumping and thermal stress. The results showed that the thickness of the liner O_3-TEOS SiO_2 had an opposite effect on copper pumping and thermal stress in 5x50 μm TSV. As the thickness of the O_3-TEOS SiO_2 liner increases from 50 to 630 nm, the residual pumping height decreases from (102 ± 7) nm to (11 ± 1) nm and the thermal stress increases from 220 to 610 MPa. In addition, J. D. Messemaeker et al.'s results also showed that the low-k dielectric liner effectively reduced residual copper pumping and thermal stress, compared to O_3-TEOS SiO_2 liner. However, an improvement in deposition conformality of low-k dielectric liner was necessary. T. T, Bui et al.[98,99] studies revealed the potential for using Parylene-HT as the liner layer in TSV. However, no copper pumping and thermal stress were addressed in Parylene-HT liner TSV. Another polymer used for TSV liner is benzocyclobutene (BCB)[100–102]. Q. Chen et al.[102] tried to solve thermal stress problem by developing TSV using benzocyclobutene (BCB) as liner layers. The result shows that BCB layers were able to reduce the stress in the silicon surrounding, but it increased the copper pumping. Recently, polyimide used as TSV liner has become more popular due to its low Young's modulus value (3-4 GPa) along with the TEC value of 20 ppm/°C which is close to the TEC of copper[103–108]. Murugesan et al.[105] study showed that the polyimide liner not only reduced the copper pumping height to more than half of the SiO_2 liner layer, but also affected the uniform copper pumping height that facilitated the rest of the integration process. In addition, the authors confirmed that the polyimide liner reduces thermal stress by a factor of five compared to the thermal stress in SiO_2 liner TSV.

1.3. Abstract of Research

Through Silicon Via (TSV) enabled by copper electrodeposition is the key technology of 3DIC packaging, which allow high packaging density, high speed signal transmission, and reduce power consumption. TSV technology has a bright future, with TSV packaging revenues

estimated to increase to about $ 4.5 billion in 2023 (Source: 2.5D / 3D TSV & wafer-level stacking technology & market updates 2019 report by Yole Development). However, TSV technology still has barriers including cost and reliability problems to overcome for higher volume production. These challenges are addressed in Chapter 1 and the solutions to these challenges have been investigated in Chapter 2-5 of this research. Chapter 6 summarizes the main contributions of this thesis.

Copper electrodeposition accounts for 41% of the total production cost of TSV and is the most expensive step in the TSV production process[41]. Thus, reduction of the copper electrodeposition cost is necessary. There are several ways to reduce copper electrodeposition costs, such as using a clean room area, improving electrodeposition tools, and reducing electrodeposition time. However, using the clean room area and the latest electrodeposition tools is expensive. Increasing current density, which means shorten the electrodeposition time, is a promising solution to reduce electrodeposition time. However, if the current density is too high, constriction occurs at the TSV opening and voids will be formed. Over the last decade, there are many studies looking at defect-free fast TSV filling solutions, such as using pulsed reverse currents, designing different TSV structures, investigating new additives, and optimizing additives concentration[53-72]. However, there are thousands of additives, each with different effects on TSV filling. Therefore, there is still room for reducing TSV filling times with new novel additives. In the Chapter 2 of this thesis, I have been investigated the chemical behaviors of Sulfonated Diallyl Dimethyl Ammonium Bromide Copolymer (SDDABC) in copper electrodeposition. Furthermore, SDDABC concentration optimization and TSV filling experiments at the optimal SDDABC concentration have been also performed.

Copper is commonly used for TSV filling because copper has the low resistivity value. However, copper TSVs pose reliability problems due to thermal expansion coefficient (TEC) mismatch between copper and surrounding silicon. The main mechanical reliability problems

include copper pumping, voiding, cracking, and delamination[42-48]. The residual stresses from the thermal annealing degrades the TSV mobilities through the piezoelectric effect, threatening TSV electrical performance. The residual stresses define a Keep Out Zone (KOZ) around the TSV where no active devices are located to prevent electronic devices failure[51,52]. The large TEC mismatch of about 15 x 10^{-6}/°C results in the accumulation of thermal stresses that cause copper pumping and KOZ, which have been investigated in a number of studies. For example, the microstructure of copper in TSV when annealing has been characterized by using SEM, nanoindentation and EBSD methods[73-77]. In addition, simulations also were performed to understand the effect of copper pumping and KOZ[46,47,82-84]. From this understanding, proper annealing conditions and multiple CMPs were performed to reduce copper pumping and KOZ. However, this method is not very effective and costly. Another way to minimize TEC mismatch between copper and silicon is to replace copper by alloying and compositing copper with other materials having a lower TEC values[85-93]. However, the resistivity of copper alloys and copper composites is higher than pure electrodeposited copper, and special methods may be required for electrodeposition. To reduce copper pumping and KOZ, TSV structural designs such as TSV diameter, pitch, geometry, and TSV liner materials were also investigated[94-108]. However, improvements in the adhesion and uniformity of the polymer liners were needed.

Reduction of copper pumping and KOZ by reducing the TEC of pure electrodeposited copper is of primary interest in this research. No one to date think or attempt to reduce the TEC of pure electrodeposited copper, thus this research is very original. Reducing the TEC of electrodeposited copper is a simply method to save costs while maintaining the resistivity of the electrodeposited copper. In Chapter 3, I have found out low TEC copper electrodeposited in a solution containing 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (2M5S) additive by measuring the thermal expansion of a copper pipe with the thermal expansion meter. In addition, the contraction mechanism of low TEC copper has been proposed

based on the detailed observations of electrodeposited copper when annealing. Thereafter, low TEC copper has been applied to fill the APCVD SiO_2 TSV in Chapter 4, and copper pumping at different annealing temperatures is measured using the in-situ heating SEM stage. Furthermore, the resistivity of low TEC copper before and after annealing is also measured and compared with conventional electrodeposited copper. Finally, the electrochemical behaviors of 2M5S and its interaction with other additives in the electrolyte have been investigated in Chapter 5. In addition, copper pumping and KOZ have been measured for conventional copper and low TEC copper in PECVD SiO_2 TSV. Finally, Chapter 6 summarizes the main contributions of this thesis.

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CHAPTER 2: BOTTOM-UP TSV FILLING USING SULFONATED DIALLYL DIMETHYL AMMONIUM BROMIDE COPOLYMER AS A LEVELER

2.1. Introduction

Through Silicon Via (TSV) enabled by copper electrodeposition is the key technology of 3-demintional integrated circuit (3DIC) packaging, which allow high packaging density, high speed signal transmission, and reduce power consumption. However, the TSV processing cost is still expensive. Copper electrodeposition accounts for 41% of the total production cost of TSV[1], so it is necessary to reduce copper electrodeposition cost. There are several ways to reduce the cost of copper electrodeposition, including using latest electrodeposition tools and reducing the time required for electrodeposition. However, the latest electrodeposition tools are expensive. Furthermore, large clean room areas need to accommodate a large amount of electrodeposition tools. Increasing current density, which means shorten the electrodeposition time, is a promising solution to reduce electrodeposition time. However, if the current density is too high, constriction occurs at the TSV opening and voids will be formed. Therefore, high speed TSV filling without void defects is required.

In this Chapter, a new leveler, sulfonated diallyl dimethyl ammonium bromide copolymer (SDDMABC), has been introduced for copper electrodeposition. SDDMABC leveler exhibits a strong inhibition effect and its super bottom-up TSV filling will be reported.

2.2. Experimental

The composition of a basic bath was 200 g/L $CuSO_4·5H_2O$ and 25 g/L H_2SO_4, 50 ppm of Cl^-, 2 ppm of SPS, and 25 ppm of PEG. SDDABC leveler which has only one positive charge head group and bromide as a counter ion is purchased from Nittobo Medical Co., Ltd. The chemical structure of SDDABC is shown in Figure 21. The solutions used for all

electrochemical measurements and TSV filling experiments were prepared by adding different concentrations of SDDABC to the basic bath.
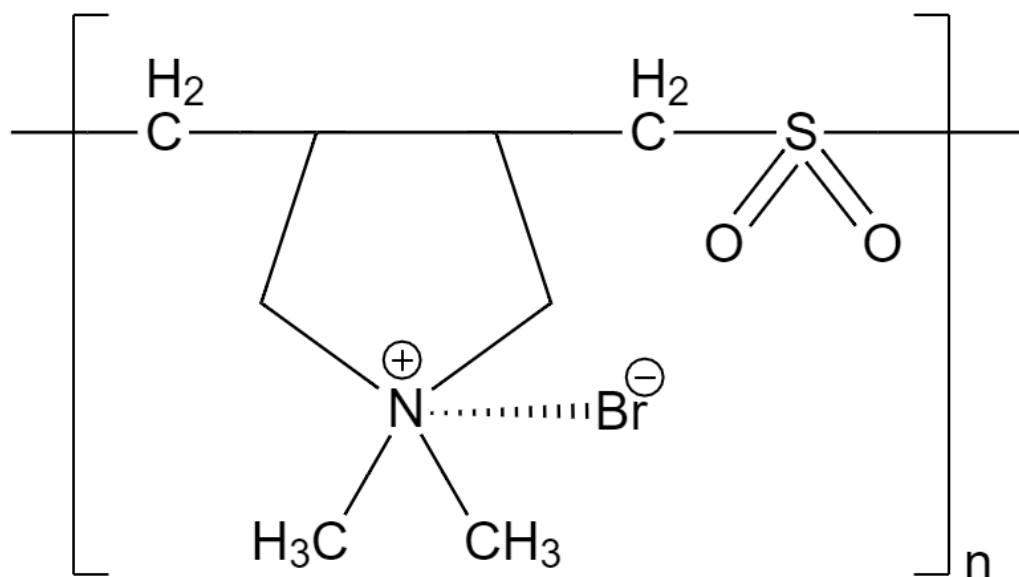

Figure 21. Structure of sulfonated diallyl dimethyl ammonium bromide copolymer (SDDABC).

Cyclic voltammetry stripping (CVS) measurements were performed at room temperature using a electrochemical measurement system (Hokuto Denko, HZ7000) equipped with a rotator (Hokuto Denko, HZAP1203n) in three electrodes glass cell containing 60 mL of electrolyte. A platinum rotating disk electrode (RDE) with a diameter of 5 mm were used as working electrode. The counter and reference electrodes were platinum wire and saturated calomel electrode (SCE electrode), respectively. In cyclic voltammetry stripping (CVS) measurement, potential was swept from 0.6V to -0.4V and then returned back to 0.6V. The potential sweep rate for CVS experiments was 10 mV/s.

Electrodeposition samples for filling experiments were silicon chip fragments with many TSVs. TSV with a diameter of 20 μm and a depth of 45 μm was used without knowing the detail structure of the TSV. A phosphorus containing copper bar was used as an anode. TSV filling experiments were carried out in a beaker containing 150 mL of electrolyte solution. The electrolyte was purged with oxygen for 30 minutes prior to electrodeposition. Silicon chip fragments were placed on a rotating cathode which rotated at 1000rpm during electrodeposition. A pulse reverse current was applied to copper electrodeposition. The pulse conditions were t_{off}: t_{on}: $t_{reverse}$ = 100: 200: 10 ms and i_{on}: $i_{reverse}$ = 1:3. The silicon chip fragments were polished using emery papers. Then, the TSV cross section was observed by SEM (JEOL, JSM-5500S).

2.3. Results and Discussion

Figure 22 shows cyclic voltammograms recorded at 1000 rpm from solutions containing 50 ppm Cl^-, 2 ppm SPS, 25 ppm PEG and different concentrations of SDDABC leveler. In the presence of 1 ppm of SDDABC, the reduction potential of cupric ion underwent a negative shift (arrow 1), along with the decrease in the anodic stripping peak (arrow 2). This means that addition of 1 ppm of SDDABC inhibits the copper electrodeposition. As expected with the increase of SDDABC concentration to 32 ppm, this inhibition effect of SDDABC is more clearly because SDDABC shifted the reduction potential to more negative values and dramatically decreased the anodic stripping area. Moreover, increasing the concentration of SDDABC leveler from 16 ppm to 32 ppm did not significantly change the cathodic potential and anodic stripping area, indicating that saturation inhibition is almost reached at 16 ppm of SDDABC. This inhibition is due to the adsorption of SDDABC leveler molecule on the cathode surfaces[2,3].
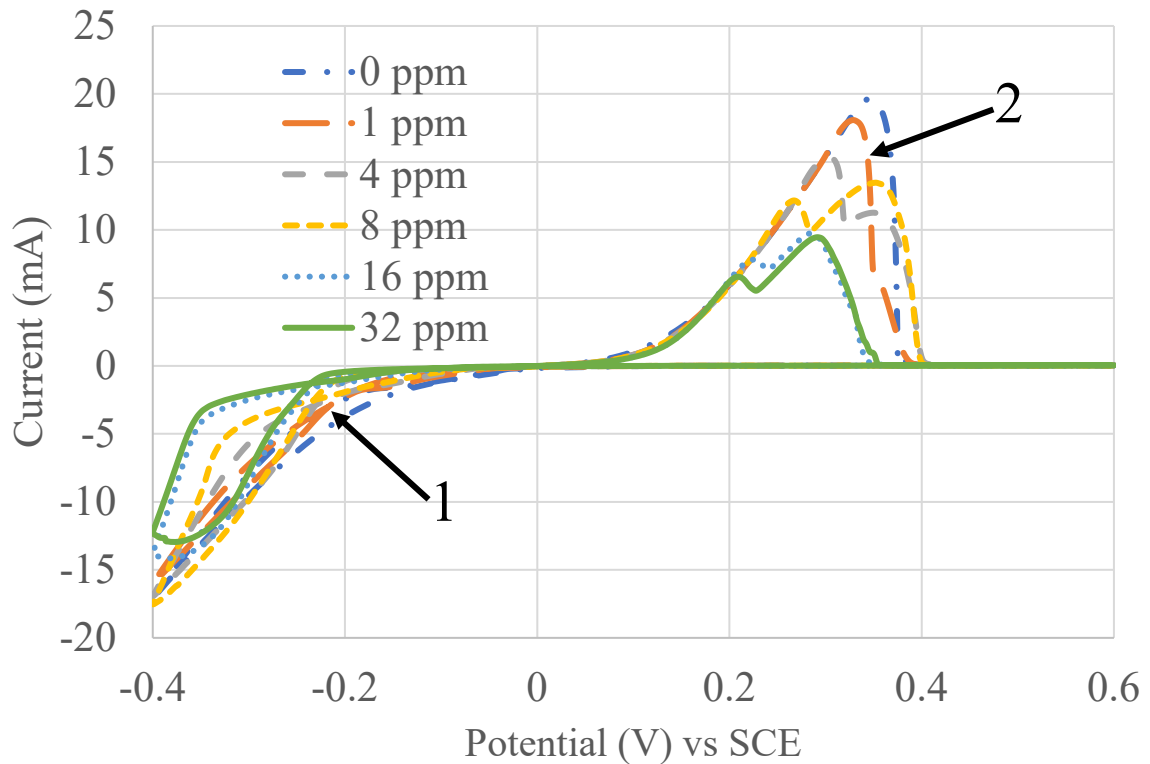
Figure 22. Cyclic voltammograms in the presence of different concentrations of SDDABC.

Because TSV is deep and narrow, the convection outside TSV is high flow velocity, while that inside the TSV is slow flow velocity during filling process. Therefore, I assume that 1000 rpm of rotating disk electrode (RDE) represents the convection condition at the via outside, 10 rpm of RDE represents the convection at the via bottom. To understand the inhibition effect of SDDABC leveler for copper electrodeposition during TSV filling process, the changes of RDE rotation speed in the presence of SDDABC were studied. Figure 23 shows the influence of rotation speed on anodic stripping area (Ar) obtained from CVS measurement with 1 ppm (■ symbol) and 16 ppm (● symbol) of SDDABC. For both 1 ppm and 16 ppm of SDDABC, the Ar values decrease faster at low rotation speeds than that at high rotation speeds. This rotation dependent behavior indicates that the copper deposition is inhibited strong at the via outside and sidewall near via opening, while the acceleration effect at the via bottom is

strong. Moreover, the Ar values at high rotation speeds (above 400 rpm) of 16 ppm SDDABC were about 150 mC, while the values of 1 ppm of SDDABC were 250 mC. That means 16 ppm of SDDABC inhibits the copper electrodeposition at via sidewall and outside much stronger than 1 ppm of SDDABC. In other words, 16 ppm of SDDABC must have better TSV filling performance than 1ppm of SDDABC.
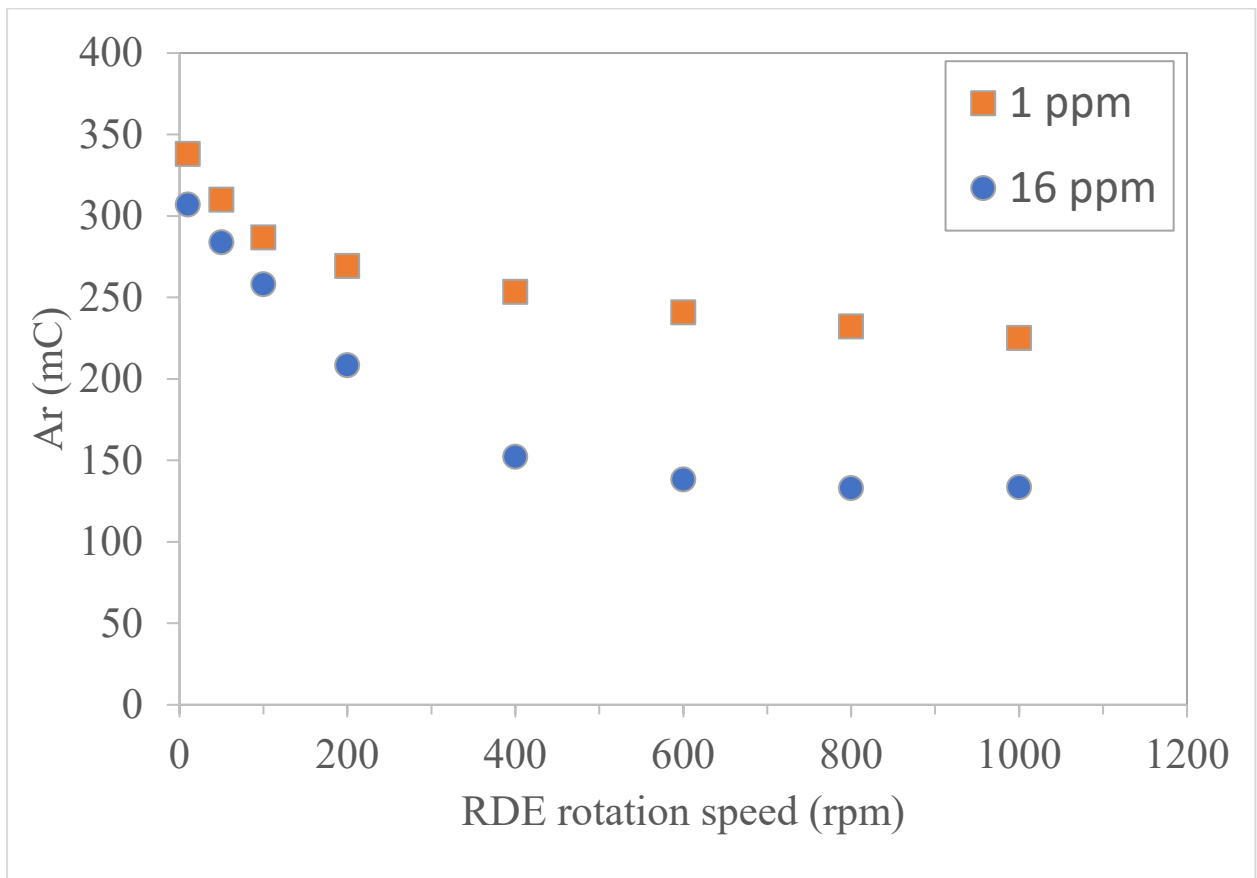

Figure 23. Influence of RDE rotation speed on anodic stripping charge of copper electrodeposition at 1 and 16 ppm of SDDABC.

Figure 24 shows the cross sections of TSV filled with 1 ppm and 16 ppm of SDDABC at different electrodeposition times. The current density is 25 mA/cm^2. Figure 24a shows the

filling profiles over times with 16 ppm of SDDABC and the electrodeposition time is 1 min, 2 min, 3 min, 4 min, and 5 min, respectively. In this case, deposition rate at the via sidewall is very small (arrow in Figure 24a at 1 min) and super bottom-up TSV filling is observed. This is only possible when inhibition layer formed by 16 ppm of leveler cover the via sidewall and strongly inhibit the copper electrodeposition on the via sidewal[4-6]. In addition, it takes only 5 min to completely fill the TSV in the presence of 16 ppm SDDABC. Figure 24b is the cross sections of TSV filled with 1 ppm of SDDABC and the electrodeposition time is 5 min, 10 min, 15 min, 20 min, and 25 min, respectively. The V- shape bottom-up filling with thick deposited copper at the via bottom and sidewall near the via bottom (arrow in Figure 24b at 5 min) and relatively thick deposited copper at the sidewall near the via outside (double arrows in Figure 24b at 10 min) forms with 1 ppm of SDDABC. This V- shape has been reported in several studies[2,7]. The V-shape filling attributes to the gradually decrease inhibition effect along the via depth direction and strong acceleration effect of accelerator at the via bottom. With increasing time, the filling ratio reached 100% with 25 min.
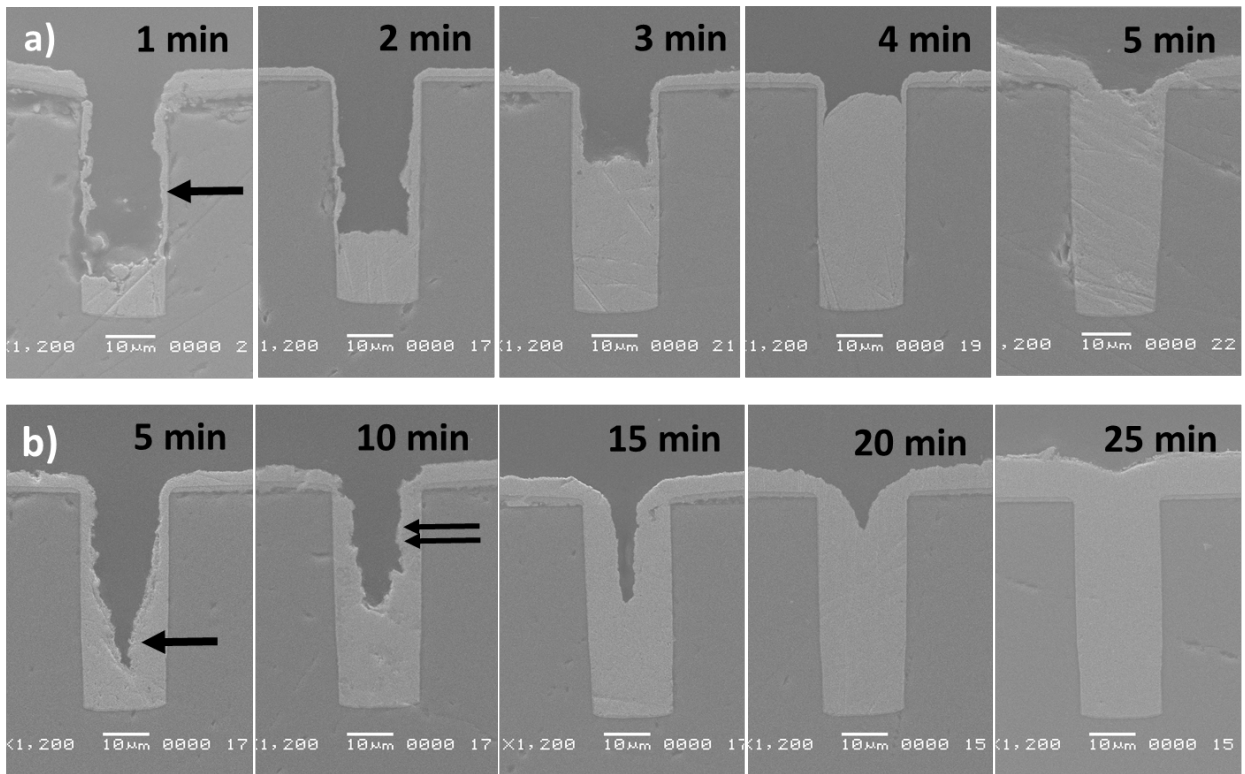
Figure 24. Cross sections of TSV filled with a) 16 ppm and b) 1 ppm of SDDABC at different filling times.

2.4. Conclusions

In this chapter, sulfonated diallyl dimethyl ammonium bromide copolymer (SDDABC) was used as a leveler. The leveler behavior was characterized by CVS method with different concentrations at different RDE rotation speeds. SDDABC forms a strong inhibition layer on copper surface when 16 ppm concentration is added. Super bottom-up TSV filling with nearly no deposited on TSV sidewall was achieved with 16 ppm of SDDABC. This super bottom-up filling is 5 times faster than that with V-shape.

2.5. References

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CHAPTER 3: LOW THERMAL EXPANSION ELECTRODEPOSITED COPPER AND ITS CONTRACTION MECHANISM BY ANNEALING

3.1. Introduction

Copper is widely used as a filling material for TSV because of its lowest resistivity, next to silver[1]. Despite the advantages of using copper as the filling material, copper TSV has its drawback due to thermal expansion coefficient (TEC) mismatch between copper and surrounding silicon. Copper has a high thermal expansion coefficient (TEC) of $17 \times 10^{-6}/{}^{\circ}C$, while the TEC of silicon is only $2 \times 10^{-6}/{}^{\circ}C$. During the SiO_2 formation in via middle process, copper TSV is exposed to a high temperature between $400{}^{\circ}C$ and $600{}^{\circ}C$. Due to the large thermal expansion coefficient (TEC) mismatch between the silicon substrate and copper, copper expands much more than silicon, causing high thermal stresses in all directions during the manufacturing process. These thermal stresses inside copper TSV cause copper pumping, voiding, cracking, and delamination. Copper pumping can destroy the wiring above the copper TSV and lead to the failure of electronic device. Moreover, the induced thermal stress, which caused by the TEC mismatch between copper and silicon, changes the electrical resistivity and mobility of silicon around the TSV. Technically, KOZ is defined as the area around a TSV where the transistors cannot be located to prevent device failure. Copper pumping and KOZ are serious reliability problems that need to be resolved.

No one to date think or attempt to reduce the TEC of pure electrodeposited copper, thus this research is very original. In this chapter, I have found out low TEC copper electrodeposited in a solution containing 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (2M5S or Lev A) additive by measuring the thermal expansion of a copper pipe with the

thermal expansion meter. In addition, the contraction mechanism of low TEC copper has been proposed based on the detailed observations of electrodeposited copper when annealing.

3.2 Experimental

The base electrolytes for the copper electrodeposition were $CuSO_4.5H_2O$ and H_2SO_4. The additives used in this study consisted of a leveler, accelerator, inhibitor, Cl^-, and 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (Lev A)[2].

Copper pipes were made for measuring the TEC of the electrodeposits. Figure 25 shows the procedure used to form a copper pipe. An aluminum pipe was used as the cathode. First, gold was sputtered on the aluminum pipe. Copper was electrodeposited on the gold then the pipe was immersed in a sodium hydroxide solution to dissolve the aluminum and form the copper pipe.
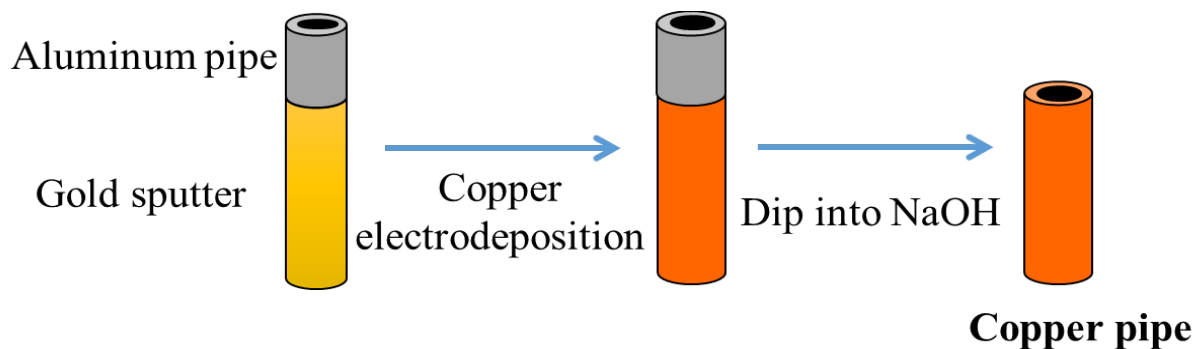
Figure 25. Procedure to form the copper pipe.

Figure 26 is a schematic illustration of the thermal expansion meter (TD5020SA, NETZSCH). The copper pipe was heated in an argon atmosphere with quartz as the reference. The copper pipe expansion lengths were measured.
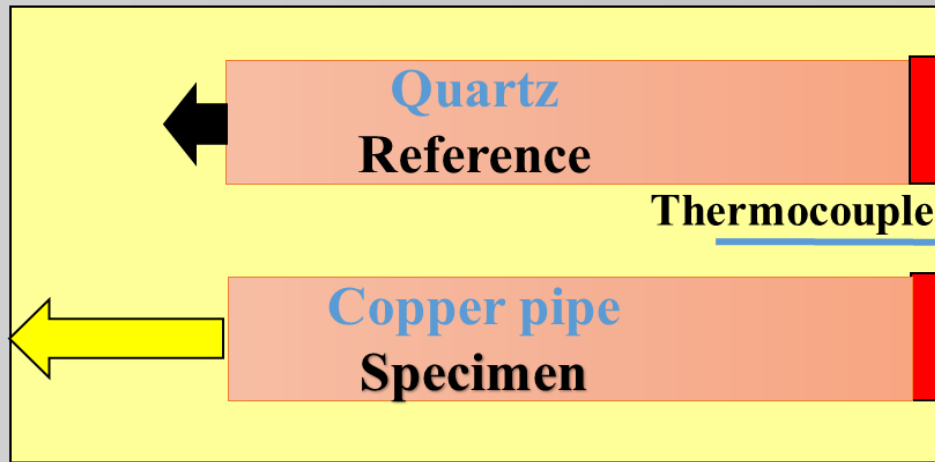
Figure 26. Schematic illustration of the thermal expansion meter.

Figure 27 is the in-situ SEM heating stage (HSEA-500, TSL solutions). (a) is a cross sectional illustration and (b) is the digital camera image. The sample was heated by a ceramic heater.

Field Emission Auger Electron Spectroscopy (FE-AES) was carried out using a Model 680(Ulvac-phi) operated at 10kV acceleration voltage and 10nA specimen current. X-ray diffraction (XRD) profiles were measured by a Ringaku SmartLab X-Ray Diffractometer using Cu Kα radiation (λ = 1.5406 Å) operated at 45 kV, 200 mA and a scanning speed of 5°/min. The carbon contents were measured by combustion method using a model CS LS600 (LECO Japan).
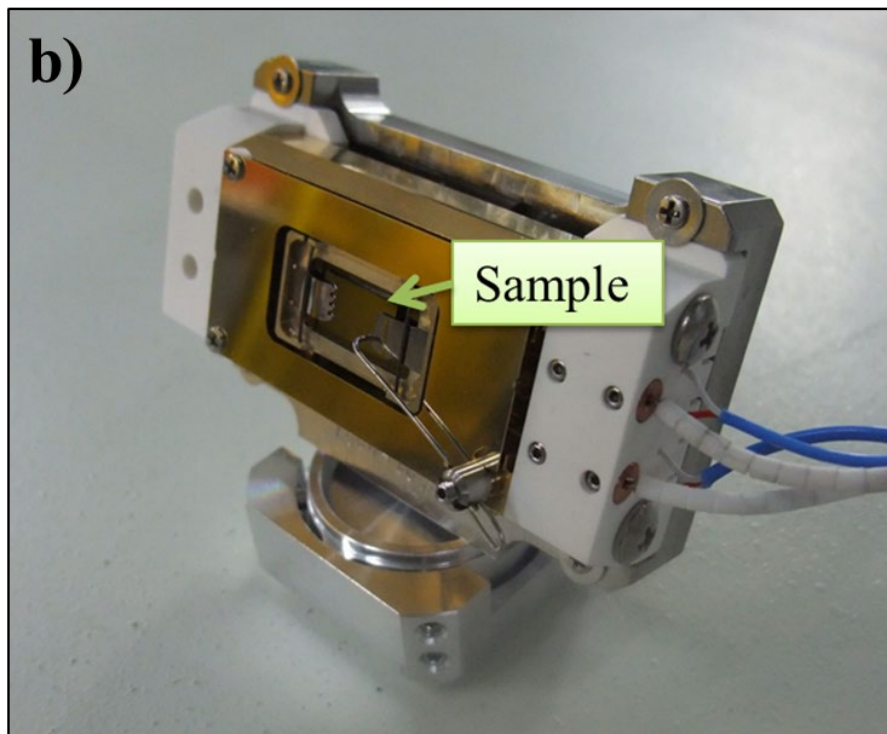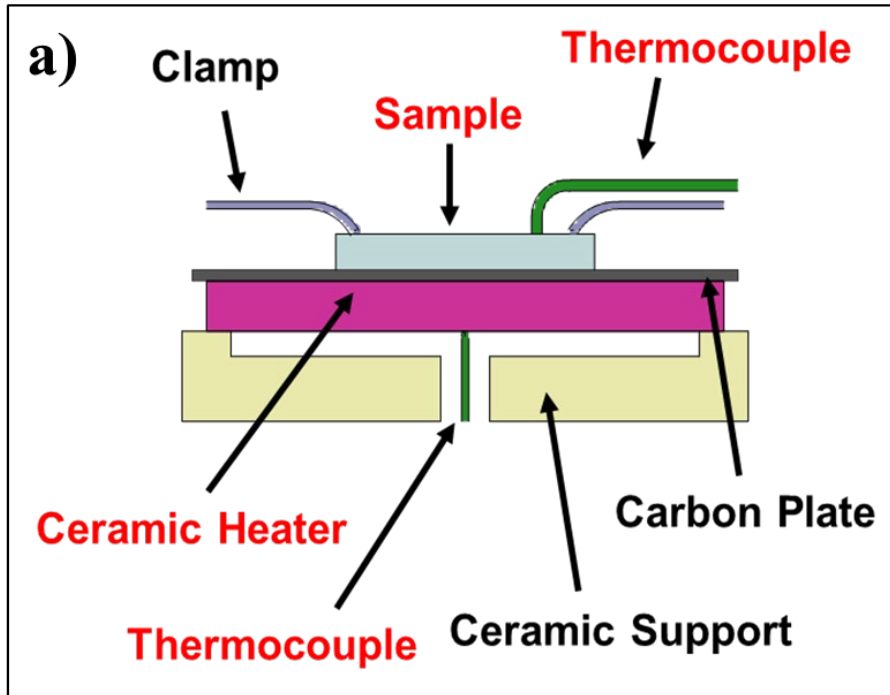
Figure 27. In-situ SEM heating stage (TSL solutions, HSEA-5000)

a) Cross sectional illustration   b) Digital image.

3.3. Results and Discussion

Figure 28 shows the thermal expansions of the conventional copper and

electrodeposited copper with the low TEC additive. For the conventional copper, the expansion length linearly increased with the temperature (red line). The thermal expansion coefficient, or the slope, is constant with the temperature. With the low TEC additive, the electrodeposited copper starts to contract at 120°C (blue curve). The difference between red line and blue curve increases in the range temperature from 203°C to 310°C. This difference becomes much greater at about 47μm at 400°C.
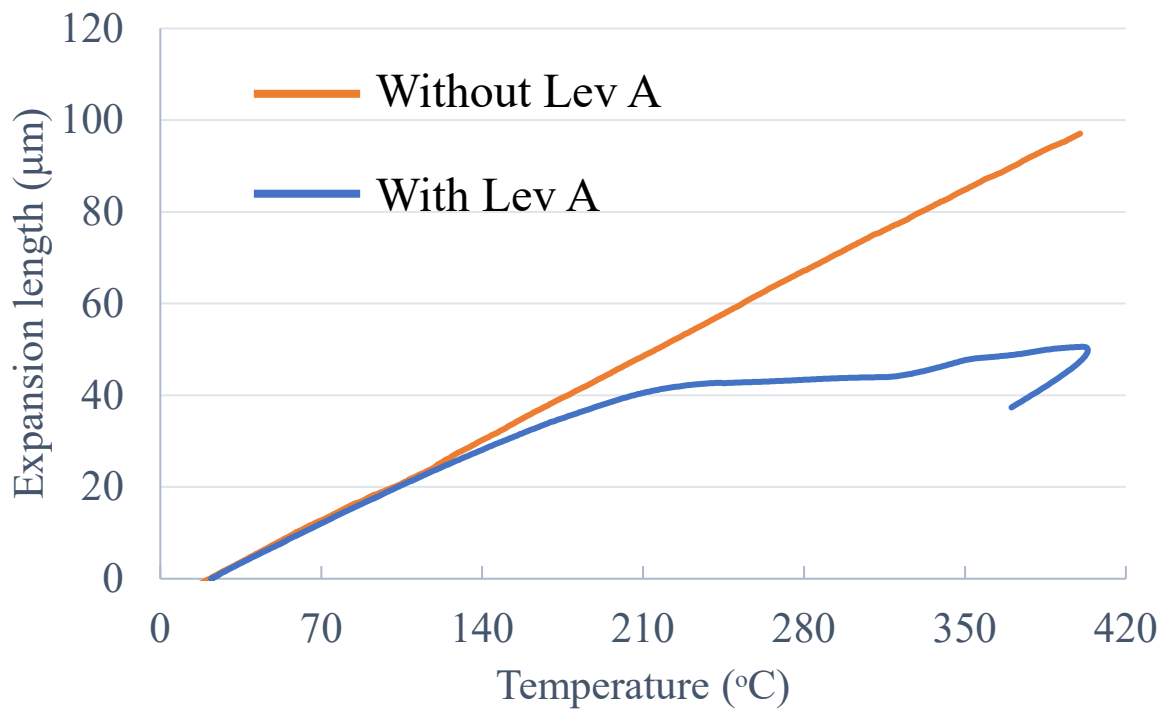

Figure 28. Thermal expansions of electrodeposited copper with and without low TEC additive (Lev A).

Figure 29 shows the in-situ SEM micrographs of the electrodeposited copper at the different annealing temperatures. Micrograph a is 203°C, b is 310°C, c is 350°C and d is 450°C. Micrographs are obtained at the high temperatures using an in-situ SEM heating stage (Figure 27). In Figure 29a, about 1 μm of electrodeposited copper grains are observed. No dark spot is observed at 203°C. Several 100 nm dark spots start emerging when the annealing temperature

was 310ºC (Figure 29b). These dark spots form at the grain boundaries and at the triple grain points. The number of dark spots increased with the increase in the temperature as shown in Figure 29c at 350ºC and Figure 29d at 450ºC.
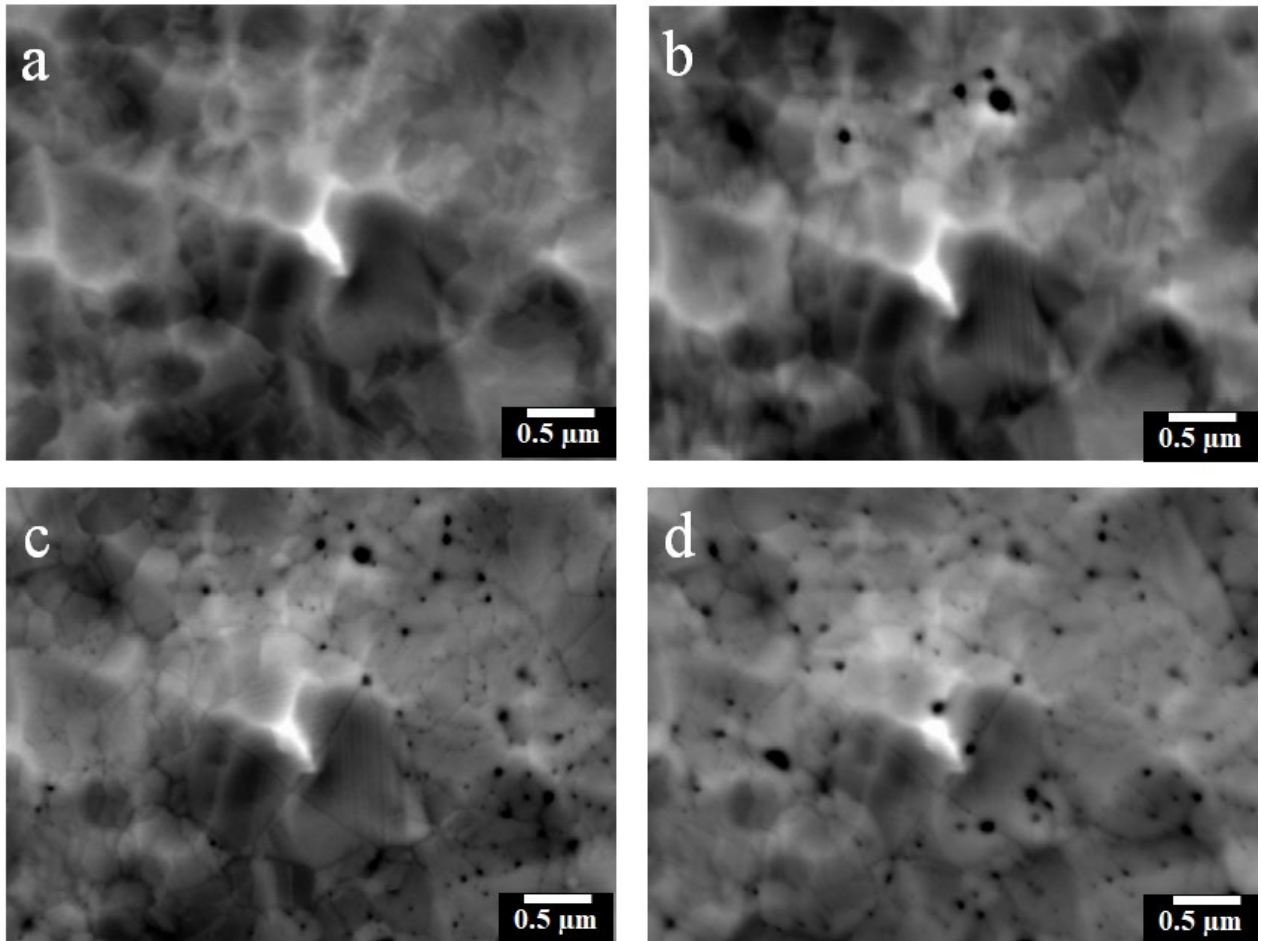
Figure 29. SEM micrographs of the electrodeposits with annealing
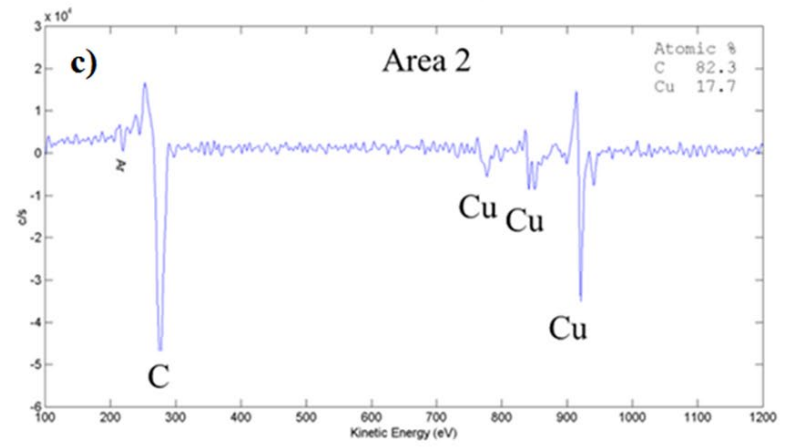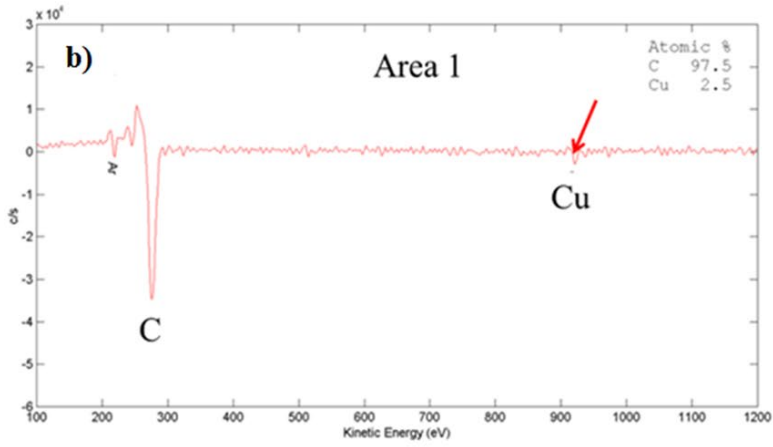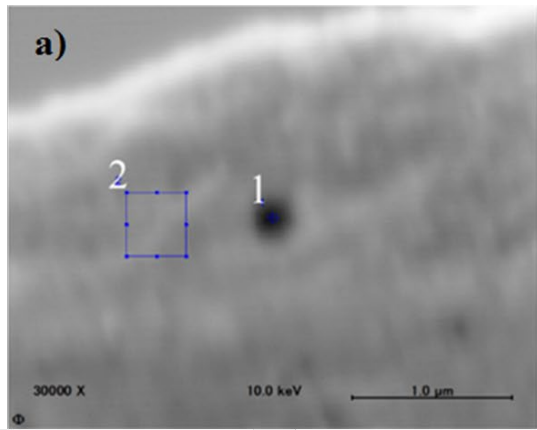*a)203ºC, b) 310ºC, c)350ºC, d)450ºC.*

Figure 30. FE-AES analysis.

Figure 30 is the FE-AES analysis of several 100 nm dark spots and other portions of the electrodeposit. Area 1 is a 100 nm dark spot and area 2 is the other portion of the electrodeposit. The two below figures are quantitative FE-AES results of area 1 at the dark spot (Figure 30b) and area 2 at the other electrodeposited portion (Figure 30c). In Figure 30b, the intensity of the copper peak at 910eV is very low (as indicated by the red arrow). However, the intensity for the carbon at 280eV is very high. Hence, the 100 nm dark spot is a carbon precipitate. For area 2, both the copper intensity at 910eV and carbon intensity at 280eV are high. Moreover, the other Cu peaks at 778eV and 850eV are clearly visible. It is known that FE-AES detects a metal`s outermost surface. On the metal`s outermost surface, atmospheric carbon is adsorbed very easily. This is the reason of for the high carbon intensity in area 2.
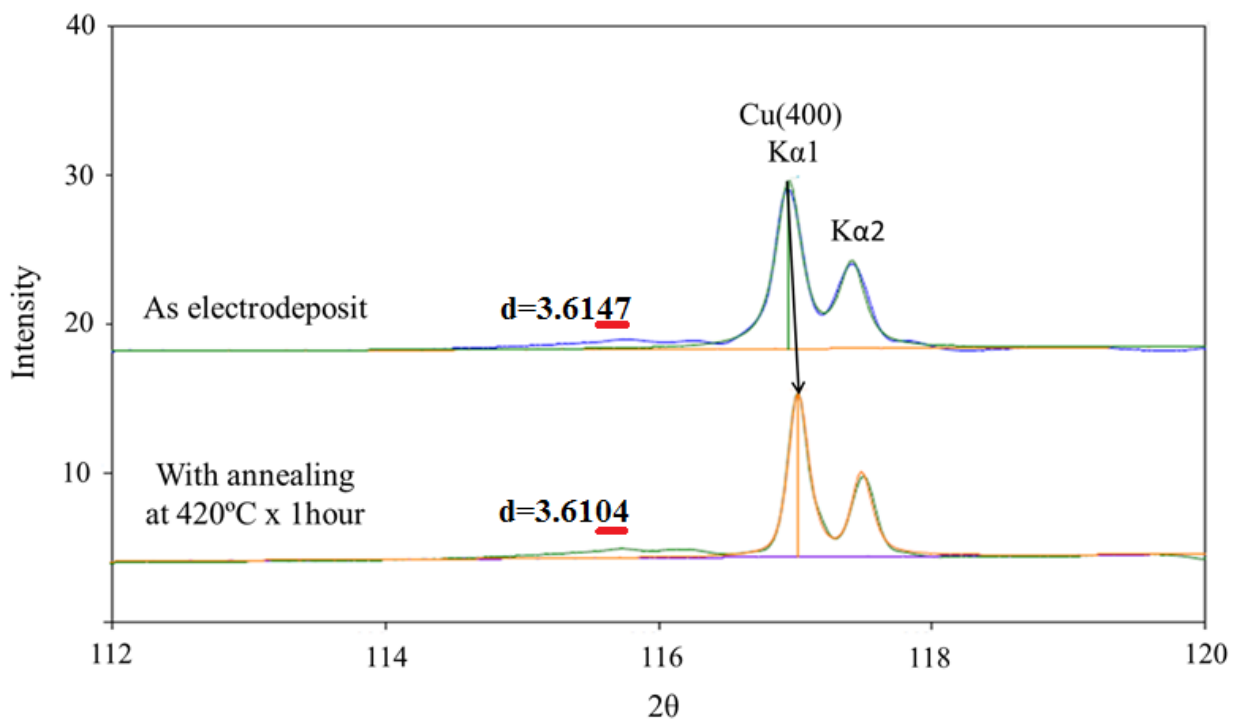

Figure 31. X-ray diffractions of electrodeposited copper with and without annealing.

Figure 31 shows the X-ray diffraction results of the electrodeposited copper with the low TEC additive as a deposit and after annealing at 420ºC for 1 hour. Cu (4 0 0) $_{Kα1}$ and Cu (4 0 0) $_{Kα2}$ are selected at the high 2θ in order to indicate the significant difference in the 2θ. The position of the (4 0 0) $_{Kα1}$ peak is shifted to a higher 2θ value from 116.950º for the electrodeposited copper to 117.180º after annealing at 420ºC for 1 hour. This shift in the 2θ value corresponds to a change in the lattice constants from d= 3.61_47_Å for the electrodeposited copper to d= 3.61_04_Å after annealing at 420ºC for 1 hour. The decrease from 47 to 04 in third and fourth decimal places indicates that the copper lattices contract due to the annealing at 420ºC for 1 hour.
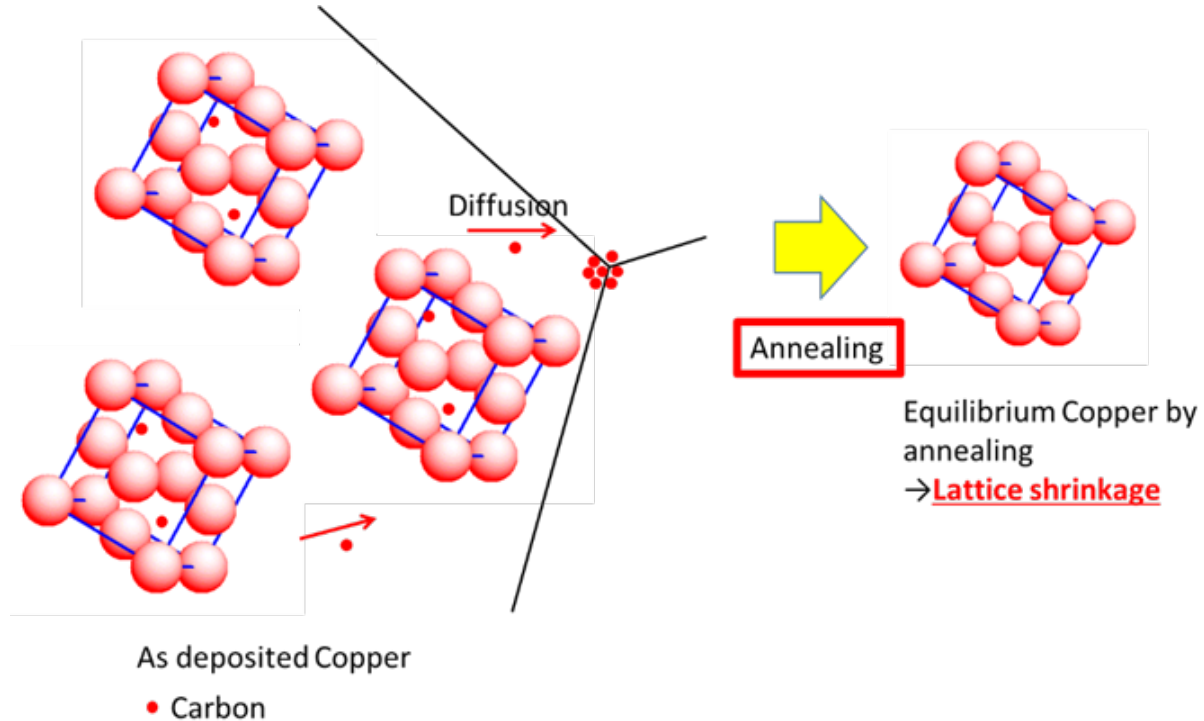

Figure 32. Mechanism of copper lattice shrinkage by annealing.

Figure 32 is the mechanism for the lattice contraction by annealing. As shown in Figure 32, the electrodeposited copper has carbon inclusion within the copper lattice. This carbon inclusion lattice is the non-equilibrium phase and the lattice constant is greater than the equilibrium

lattice constant. During annealing, carbon diffuses out of the lattice and the non-equilibrium lattice transforms into the equilibrium lattice with no carbon inclusion. The carbon diffuses to the triple grain points and form about several 100nm dark spot precipitates (Figure 29b, c, d). The non-equilibrium to equilibrium lattice transformation occurs during annealing and lattice constant contracts. This is the mechanism for the low TEC copper electrodeposition.

The as-deposited copper with the low TEC additive has 0.018wt% carbon compared to 0.004wt% without the additive. About five times more carbon is contained in the electrodeposit with the low TEC additive when compared to the electrodeposit without the low TEC additive. Furthermore, the TEC measurement and x-ray diffraction are consistent. The ratio of the expansion length between room temperature and after annealing at 400oC and the copper pipe original length is 47/15000, since the copper pipe`s original length is 15000 μm. The ratio of the lattice constant difference at room temperature and after annealing at 420°C and as deposit lattice constant is 0.0043/3.6147. The order of magnitude of these two ratios are in good agreement. It is well-known that X-ray diffraction is non-destructive, without enforcing the force to the sample.

3.4. Conclusions

The effect of 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (Lev A) on reduction of thermal expansion of electrodeposited copper were studied by scanning electron microscopy (SEM), FE Auger, and X-ray diffraction. The results obtained are summarized as follows.

(1) With the low TEC additive, the electrodeposited copper starts to contract at 120°C. The difference in expansion length between conventional copper and copper electrodeposited with the low TEC additive becomes greater with annealing. This difference is about 47μm at 400°C.

(2) Dark spots exist in the SEM micrograph at 310ºC and their number increases with the increasing annealing temperature.

(3) Based on the FE-AES analysis, several 100nm dark spots are carbon precipitates.

(4) Based on the X-ray diffraction, the lattice constant contracts by annealing at 420ºC for 1 hour.

(5) The as-deposited copper has carbon inclusions in the lattice. The carbon diffuses out at high temperature, hence contracting the lattice constant. This non-equilibrium to equilibrium transformation by annealing causes copper contraction during the annealing.

3.5. References

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CHAPTER 4: THERMAL STRES REDUCTION OF COPPER THROUGH SILICON VIA (TSV) WITH ANNEALING.

4.1. Introduction

Three-dimensional (3D) packaging is a novel technique for obtaining improved packaging density, reduced signal delay, and reduced power consumption. 3D packaging is manufactured by vertically stacking the silicon wafers. Transistors are formed on only one side, not both sides of a silicon wafer. Therefore, through silicon via (TSV) is necessary to connect the upper transistors to lower transistor in the shortest distance. Copper is widely used for TSV filling due to its low resistivity.

However, in the TSV manufacturing process, copper TSV encounters the thermal stress problem. Via middle process is currently a most adopted process for 3D packaging. During wiring step in via middle process, dielectric layer SiO_2 is form by thermal chemical vapor deposition (CVD) under a high range of temperature between 400°C and 600°C. Hence, copper TSV also is exposed this high temperature. Unfortunately, the thermal expansion coefficient (TEC) of copper is 17×10^{-6}/^{o}C, nearly nine times greater than that of silicon (2×10^{-6}/^{o}C). That large mismatch in TEC between copper and silicon generates the thermal stress inside and surround the copper TSV. A part of thermal stress in the upper region of copper TSV is released by the copper pumping. However, the copper pumping destroys the overlying wires above the copper TSV and causes the devices failure.

In chapter 3, I found out the low TEC copper and its contraction mechanism with annealing. Thereafter, I tried to use this low TEC copper to fill the TSV with atmospheric pressure chemical vapor deposition (APCVD) SiO_2 liner in this chapter. Copper pumping in low TEC copper TSV

at different annealing temperatures is measured by using the in-situ heating SEM stage. Furthermore, the resistivity of low TEC copper before and after annealing is also measured and compared with conventional electrodeposited copper.

4.2. Experimental

The basic electrolyte contained $CuSO_4.5H_2O$, H_2SO_4, and Cl^- ion from HCl form. An accelerator bis-3-sulfopropyl disulfide (SPS), a inhibitor polyethylene glycol (PEG, average molecular weight of 10000) and two levelers namely: sulfonated diallyl dimethyl ammonium chloride copolymer (SDDACC) and 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (Lev A) were added into the basic electrolyte. In this study, two combinations of additives were used. The first combination consisted of basic electrolyte, SPS, PEG, SDDAC, and it was called a conventional bath is widely used in the industry. The other bath was a low TEC bath consisting of basic electrolyte, SPS, SDDAC and Lev A.

The electrochemical analyses were performed in a 250 mL three electrodes cell using electrochemical measurement system HZ-7000 (Hokuto Denko). Platinum rotating disk electrode (RDE) with diameter of 5 mm was used as a working electrode. The counter and reference electrodes were a platinum wire and a saturated calomel electrode (SCE), respectively. Cyclic voltammetry stripping (CVS) was carried out from 0.5V to -0.3V and back again 0.5V with a scan rate of 12 mV/s at 10 rpm and 1000 rpm rotating speeds.

The 2 cm x 2 cm silicon chips containing many TSVs were used as plating samples. The diameter of the TSV was 5 μm and the depth of the TSV was 20 μm. The TSV sidewall was first covered with a conformal dielectric liner layer of APCVD SiO_2. The thickness of this dielectric liner layer was 500nm. Subsequently, a Ti layer having a thickness of 300nm was used as a barrier layer. Next, a 200nm thickness copper seed layer was sputtered on the Ti layer before TSV filling

was performed. The TSV was filled using periodic pulse reverse current generated by pulse generator HA-211, Hokuto Denko and Galvanostat/Potentiostat HA-301, Hokuto Denko in a beaker containing 150 mL plating solution. A phosphorus-containing copper bar was used as the anode. The TSV chip was attached to cathode holder that rotated at 1000rpm to produce a good convection.

The thermal expansion length of electrodeposited copper was measured using a thermal expansion meter (TD5020SA, NETZSCH). In-situ copper pumping measrements at high temperatures were characterized by using scanning electron microscopy (SEM) (JSM 5500S, JEOL) with a 70° tilted heating SEM stage. If the electron beam is perpendicular to sample surface, it is very difficult to detect the different in height between the pumping of copper and the surrounding silicon. Therefore, the heating SEM stage were tilted 70° for better copper pumping observation.

The copper films were prepared by electrodeposition on glass substrate with sputter gold as a seed layer. The resistivity of electrodeposited copper was investigated first in the as-deposited state on the substrates and at different annealing temperatures after stripping them from the glass substrates. These resistivity values were measured by using low resistivity meter (Loresta-AX MCP-T370, Mitsu Chemical Analytech).

4.3. Results and Discussion

Figure 33 shows the effect of Lev A concentration against anodic stripping areas of CVS measurement at different rotation speeds. In this experiment, other additives such as Cl-, SPS, SDDAC were added and their concentrations were maintained. On the other hand, Lev A concentration was changed to investigate the effect of its concentration on the anodic stripping area. Anodic stripping areas at 10 rpm and 1000 rpm are denoted by A10, 10 rpm and A1000, 1000
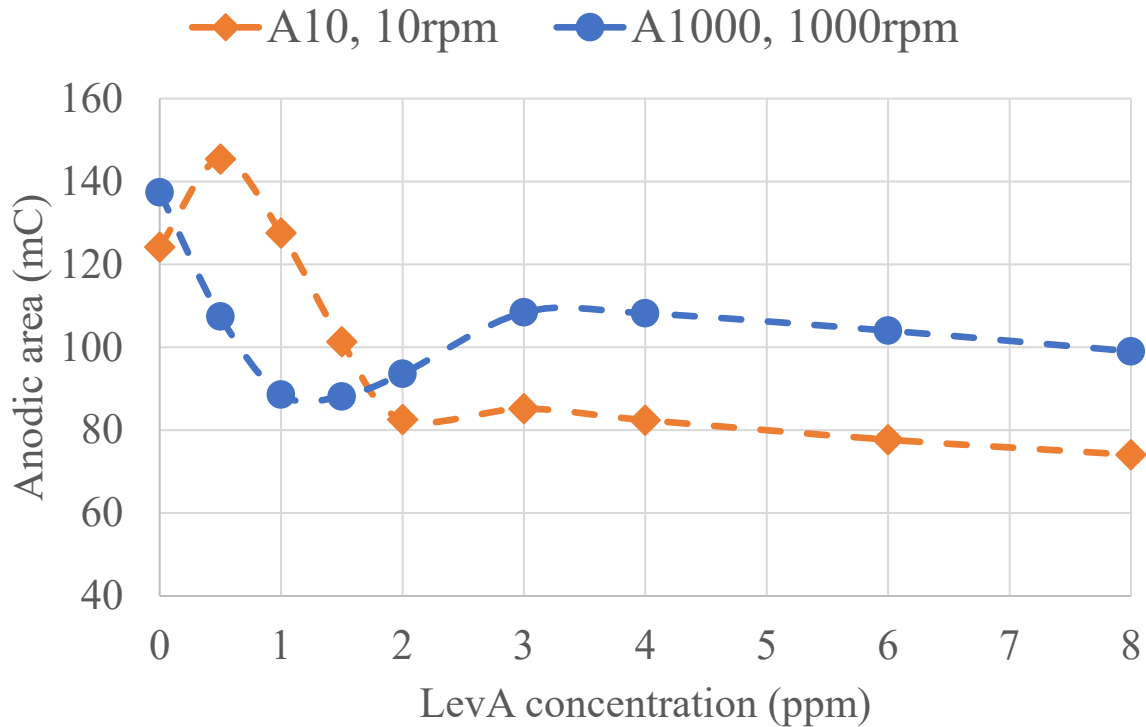
Figure 33. Relationship between the Lev A concentration and anodic area in CVS measurement at rotation speeds of 10 rpm and 1000 rpm.

rpm, respectively. In case of the copper TSV filling, the silicon chip is mounted to a cathode holder rotating at high rotation speed. Thus, the convection at the via outside is very strong. However, since the via is very depth and narrow, the convection condition at the via bottom is very weak. Therefore, it is assumed that 1000 rpm rotating speed of rotating electrode represents the convection condition at outside surface of the via, while 10 rpm rotating speed of rotating electrode is the convection condition at the via bottom in CVS measurement. At the same electrolyte bath composition, if the anodic stripping area at 10 rpm of rotation speed is larger than that at 1000 rpm, the current density at the via bottom is larger than that at the via outside. Thus, filling rate at the via bottom is higher than that at the via outside and perfect bottom up TSV filling is expected. In Figure 33, without Lev A, the anodic area at 10 rpm is smaller than that at 1000 rpm. However,

when concentration of Lev A is in range of 0.5 ppm to 1.5 ppm, the anodic stripping area at 10 rpm is much larger than the one at 1000 rpm. It means that Lev A concentrations from 0.5 ppm to 1.5 ppm can be used to fill the TSV. Therefore, Lev A concentrations from 0.5 ppm to 1.5 ppm were used for the following experiment.

Figure 34 shows TEC measurement results of conventional copper and low TEC copper electrodeposited with different concentrations of Lev A. The expansion length of conventional copper is linear with the temperature, as shown by line a in Figure 34. However, with 0.5 ppm to 1.5 ppm of Lev A, low TEC copper electrodeposits (curve b, c, and d) start to shrink at 120°C and their expansion lengths are all lower than that of copper. The reason for the reduction in expansion
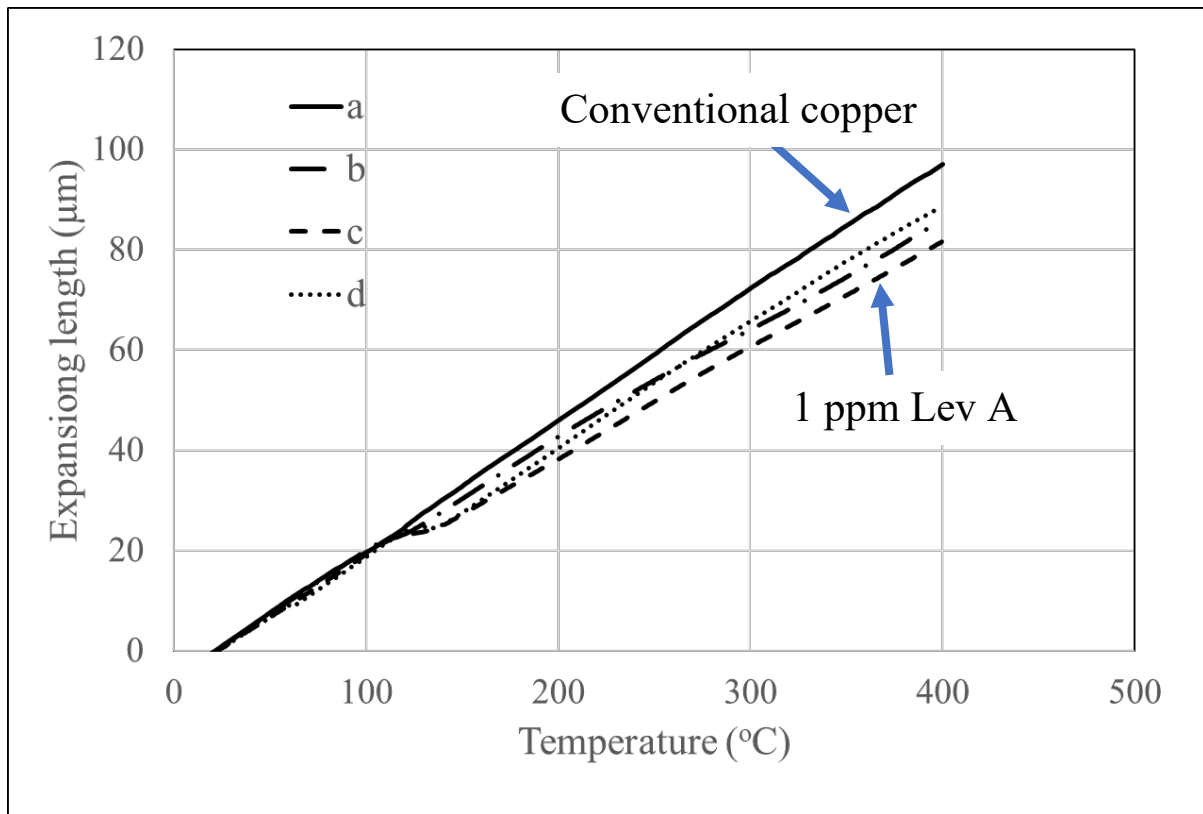

Figure 34. TEC measurement of electrodeposited copper at different concentrations Lev A.

a) conventional copper, b) 0.5 ppm Lev A, c) 1 ppm Lev A and d) 1.5 ppm Lev A.

length of copper electrodeposited with Lev A is the incorporation of carbon in the copper lattices. When annealing, carbon start diffusion out from copper lattices to the grain boundary and leaving the copper lattices in the equilibrium form without incorporated carbon[1]. Furthermore, at 1 ppm Lev A, the lowest expansion length of electrodeposited copper is obtained. Therefore, 1 ppm of Lev A was chosen for filling the TSV and then measuring copper pumping.
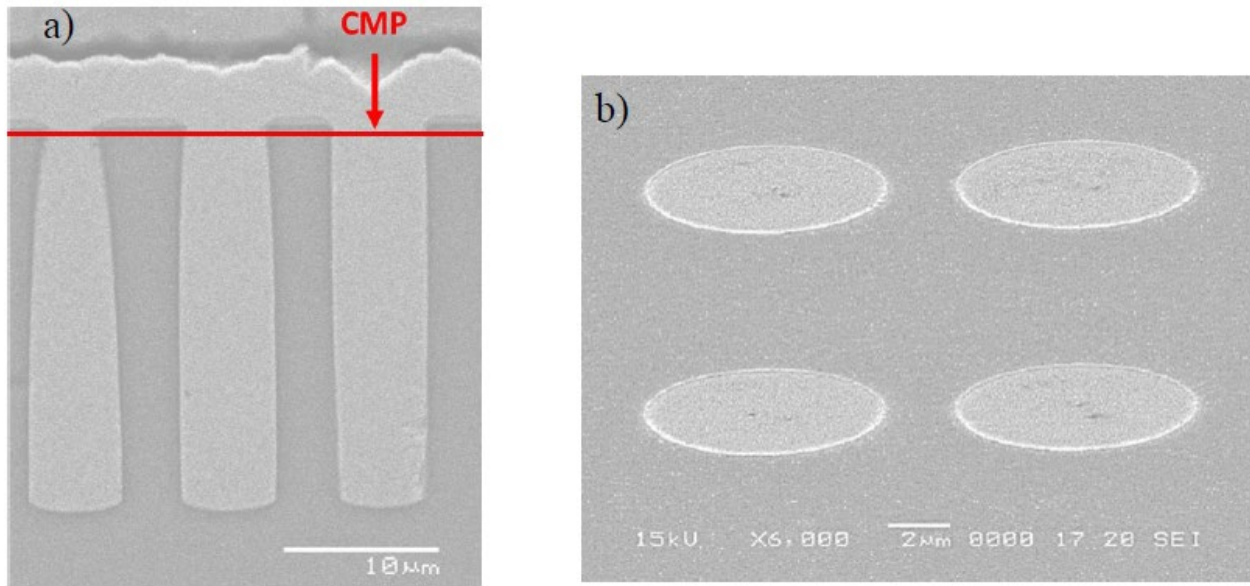

Figure 35. SEM images of low TEC copper TSV. a) cross sectional view, b) top view after CMP.

Figure 35 indicates the SEM images of copper TSV filled with 1 ppm of Lev A. The diameter and the depth of the via are 5 μm and 20 μm, respectively, corresponding to an aspect ratio of 4. As shown in Figure 35a, at 1 ppm of Lev A, perfect TSV filling has been achieved at 3mA/cm^2 with the following pulse reverse current conditions: $i_{reverse}= 6 \, |i_{on}|$ and $t_{on}: t_{off}: t_{reverse} = 200ms: 100ms: 10ms$. This result is in good agreement with the CVS result shown in Figure 33. After that, in order to remove the copper overburden for copper pumping observation, the silicon chip was subjected to chemical mechanical polishing (CMP) to the line as shown in Figure 35a.

Figure 35b is the top view SEM image of copper TSV surface after CMP. There is no difference in height between copper and surrounding silicon after CMP.

Figure 36 shows the top-view SEM images of conventional copper TSV at different annealing temperatures. The heating SEM stage was tilted 70° for better observing the copper pumping. Figure 36a shows the flat surface of the copper TSV after CMP. In Figure 36b, it is hardly to observe the copper pumping by eyes at 200°C. However, the pumping of copper is clearly viewed at center of the via at 300°C as shown in Figure 36c. When temperature increased to 400°C (Figure 36d), copper pumping is not only at the via center, but it also happens at the surrounding of the via. At 450°C and 500°C, the copper pumping is higher at both via center and via edge. In brief, copper pumping happens at both via center and via surrounding during annealing. The pumping height of copper increases with the increase of temperature. This high copper pumping height will destroy the wiring above the TSV in wiring process and let to the failure of the chips. Therefore, it is necessary to reduce the copper pumping or reduce the TEC of copper.
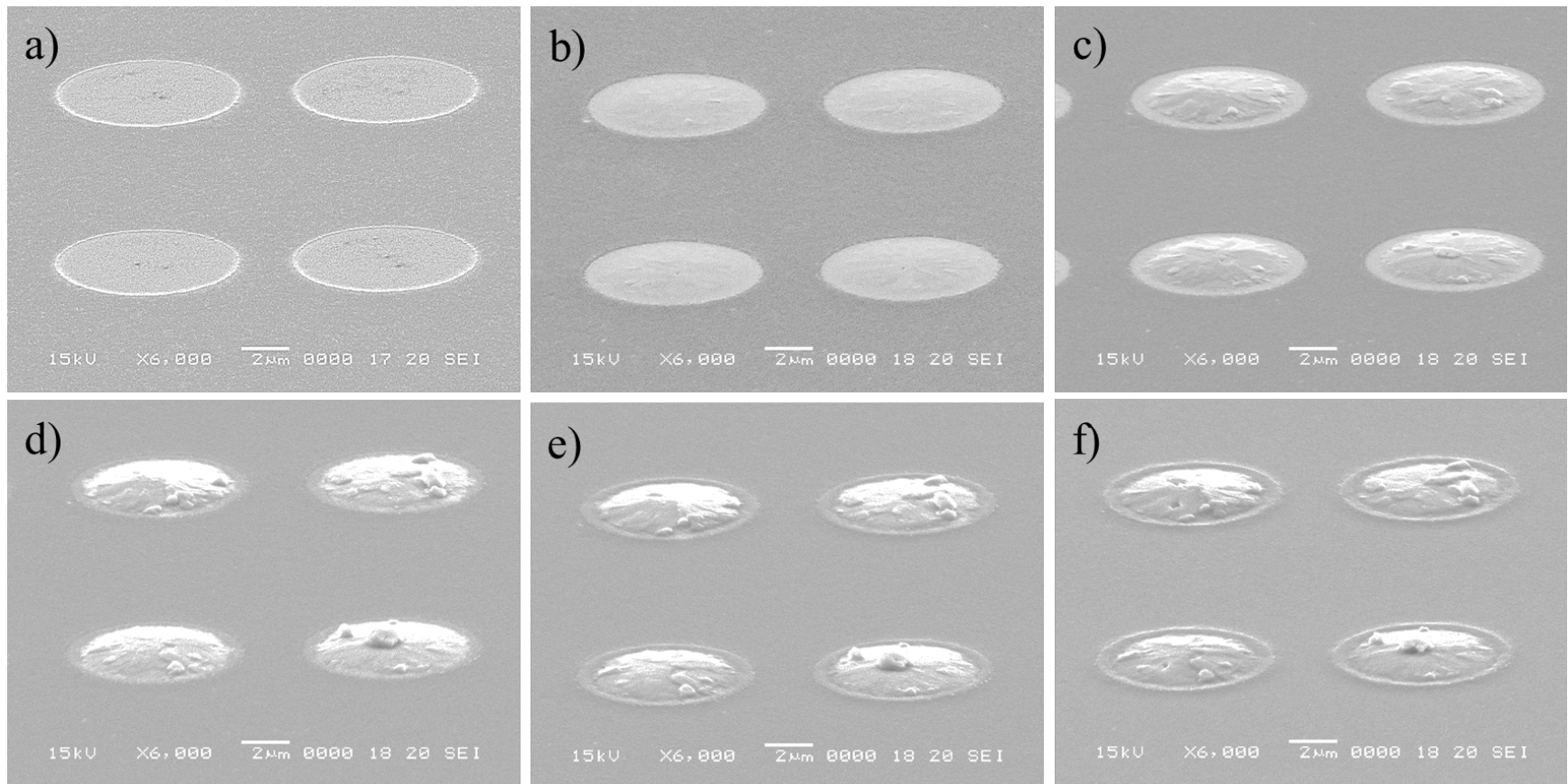
Figure 36. Tilted SEM images of conventional copper TSV pumping at various annealing temperatures.

a) 25ºC, b) 200ºC, c) 300ºC, d) 400ºC, e) 450ºC and f) 500ºC.

Figure 37 compares the copper pumping of conventional copper TSV and low TEC copper TSV at of 300°C and 500°C annealing temperatures. For conventional copper TSV, the copper pumping of is clearly viewed at the via center at 300°C as shown in Figure 37a. When temperature increased to 500°C (Figure 37b), not only the copper pumping height is higher at the via center, but it also happens at the surrounding of the via. From Figure 37c and 37d, the copper pumping height of low TEC copper TSV also increases with increasing temperature. However, its pumping height is much lower compare to that of conventional copper TSV.
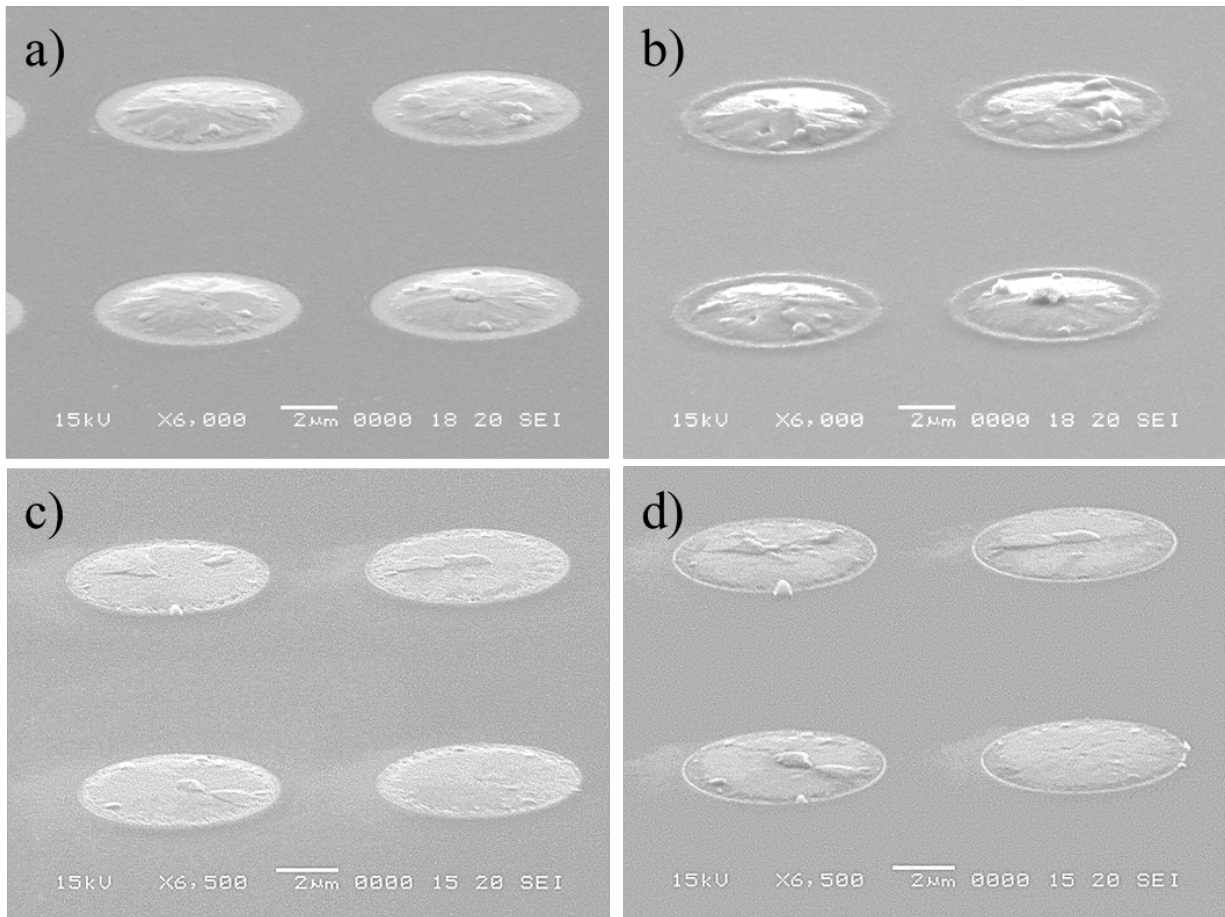

Figure 37.Comparison of copper pumping of conventional copper TSV and low TEC TSV copper at 300°C and 500°C. (a) conventional copper at 300°C, (b) conventional copper at 500°C (c) low TEC copper at 300°C, and (d) low TEC copper at 500°C.
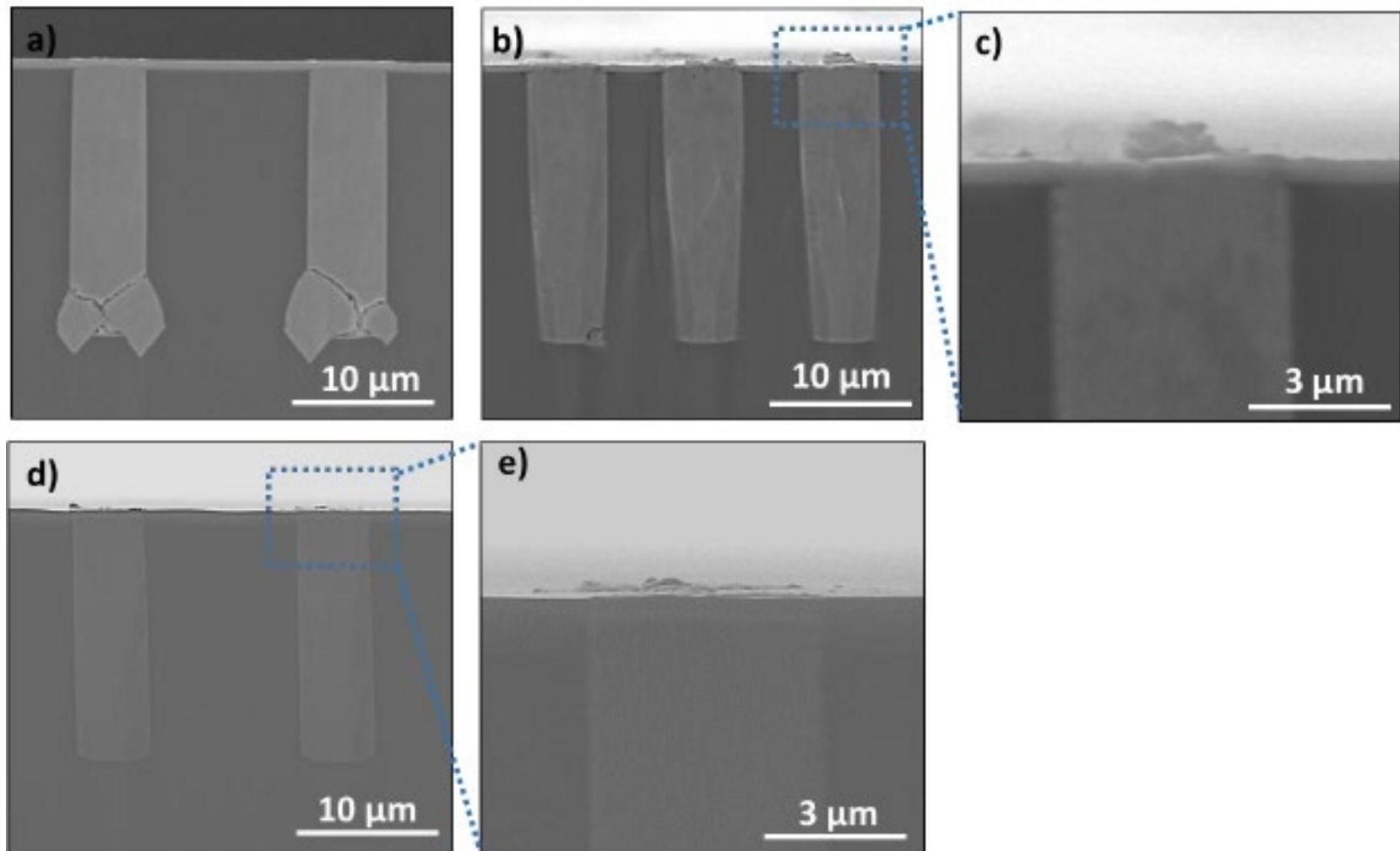
Figure 38. Cross-section SEM images of copper TSVs after annealing at 500ºC.

- *a, b, c) conventional copper TSV*
- *d, e) low TEC copper*

Figure 38 illustrates the cross-sectional view of copper TSVs after annealing at 500℃. Figure 38a, 38b and 38c are cross sections of conventional copper TSVs. Figure 38d and 38e are the cross sections of low TEC copper TSVs. In Figure 38a, there are cracks at the bottom corner of the via and the copper pumping height is very low as 0 µm. The crack in silicon at the bottom corner of the TSV also has been reported by H. Kitada et al.[2] and S. D. Cho et al.[3]. By using numerical simulation, J. S. Hwang et al.[4] and B. Liu et al.[5] found that the stress at the via bottom is concentrated at the lower region of the TSV, especially at via bottom corner. In the upper region of the TSV, stress is released by the pumping of copper when annealing. However, at the bottom part, the stress due to the mismatch in TEC between copper and silicon cannot be released. That high stress is the reason for the cracks at the bottom corner of the TSV. However, when no crack is observed at the via bottom corner, the copper pumping height is very high, about 1.2 µm (as shown in zoom-in Figure 38c). In Figure 38d and 38e of low TEC copper TSV, no crack is observed at the via bottom corner. Moreover, the copper pumping height is only 0.3 µm.

Figure 39 compares the resistivity values of conventional copper and low TEC copper in as electrodeposited copper and after annealing at different temperatures. The x-axis is the temperature and the y-axis is the resistivity in µΩ.cm. There is a trend that the resistivity values of both conventional copper and low TEC copper decreased with the increase of annealing temperature. This reduction of resistivity is caused by the growth of copper grain size by annealing. For conventional copper, the resistivity value slightly reduced after annealing at 250℃, then dramatically decreased when annealing temperature increased to 350℃ and 450℃. Meanwhile, the resistivity of low TEC decreased gradually by annealing temperature. Moreover, it is clear that the resistivity values of low TEC copper are always lower than that of conventional copper before and after annealing at different temperatures. In as electrodeposited copper, the resistivity of low
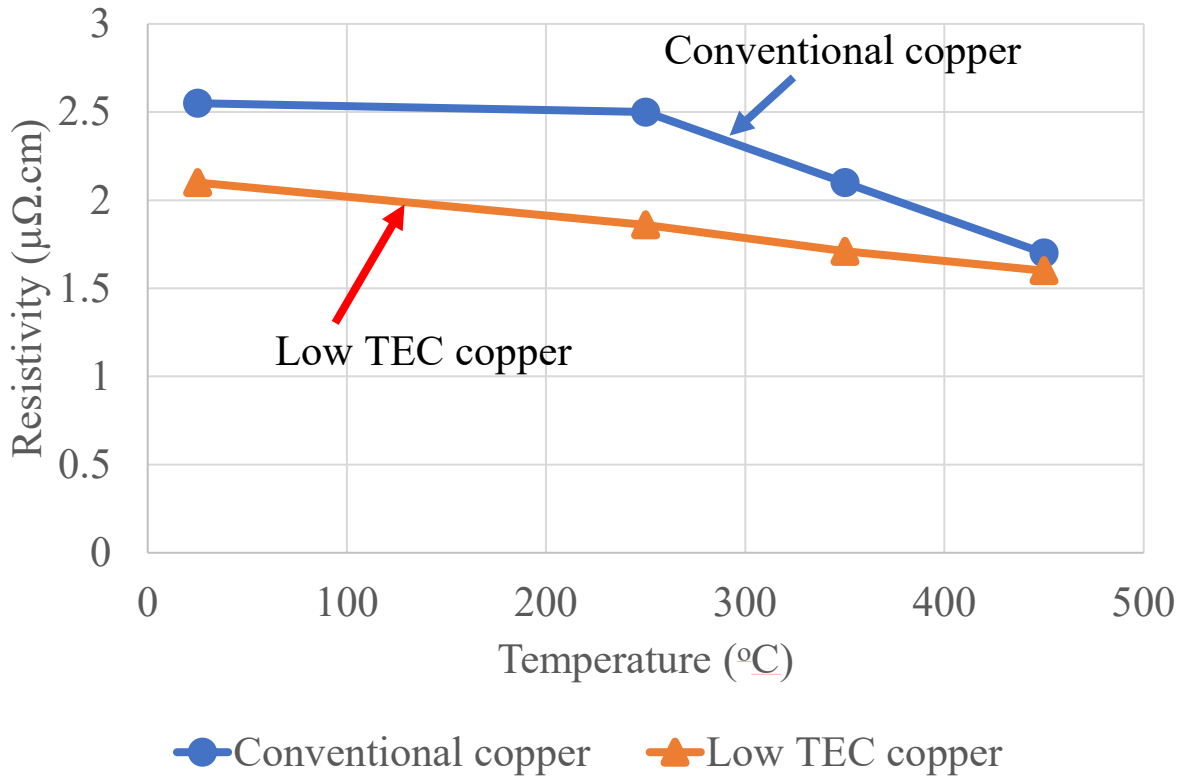
Figure 39. Resistivity of conventional copper and low TEC copper before and after annealing at different temperatures.

TEC copper is much lower than that of conventional copper, however, its value is slightly smaller at 450°C of annealing temperature. These results described above show that the low TEC copper is not only good at reducing thermal stress in TSV due to annealing but also decrease the resistivity of the TSV.

4.4. Conclusions

Electrodeposited copper is widely used in TSV filling due to its low resistivity. Unfortunately, its TEC of 17 x 10^{-6}/°C causes thermal stress during annealing due to the mismatch with silicon TEC of 2x10^{-6}/°C.

In the upper region of the TSV, stress is released by the pumping of copper when annealing. The results showed that the copper pumping height of TSV increases with the increase of temperature and the pumping height is about 1.2 μm at 500°C for conventional copper TSV. Also, the thermal stress due to the mismatch in TEC between copper and silicon is accumulated. That stress is the reason for the cracks at the bottom corner of the conventional copper TSV.

With our low TEC copper, the copper pumping height of decreases to only 0.3 μm and no cracks occur at the via bottom corner. In addition, the resistivity values of low TEC copper are always lower than that of conventional copper in as electrodeposited copper and after annealing at different temperatures. The results suggested that the low TEC copper is not only reduces the thermal stress in TSV due to annealing but also decreases the resistivity of TSV.

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CHAPTER 5: ELECTROCHEMICAL BEHAVIOR OF 2M5S AND ITS INFLUENCE ON REDUCTION OF COPPER PUMPING AND KEEP-OUT ZONE

5.1. Introduction

In chapter 3, I have reported the low thermal expansion coefficient (TEC) copper electrodeposited in solution containing 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (2M5S or Lev A). In chapter 4, I filled the atmospheric pressure chemical vapor deposition (APCVD) SiO_2 liner TSV with low TEC copper to reduce the copper pumping in TSV. In this chapter, electrochemical measurements will be used to study the electrochemical behavior of 2M5S and its interaction with other additives during copper electrodeposition. Moreover, the effects of various additive combinations on the thermal expansion of electrodeposited copper and TSV filling performance will be investigated. In section "1.1.2.2.2. Dielectric Insulator Layer" of this thesis, it is noticed that SiO_2 liner layers produced by atmospheric pressure chemical vapor deposition (APCVD) and plasma enhanced chemical vapor deposition (PECVD) have the different properties. SiO_2 formed by APCVD has a high residual stress and the deposition temperature is high ($400^{o}C$-$600^{o}C$). Meanwhile, the deposition temperature to form SiO_2 by PECVD is lower than $400^{o}C$. SiO_2 liner layers with different properties can have different effects on copper pumping and thermal stress in the surrounding silicon. Therefore, copper pumping and thermal stress in silicon of PECVD SiO_2 liner TSV filled with low TEC copper will be studied.

5.2. Experimental

A virgin makeup solution (VMS) consisting of 70 g/L $CuSO_4.5H_2O$, 75 g/L H_2SO_4 was prepared as an additive-free electrolyte. Various combinations of additives were dissolved into VMS solution for electrochemical measurement and TSV filling. 50 ppm Cl^- was added in form of HCl acid. Bis-sodium sulfopropyl-disulfide (SPS) and Sulfonated diallyl dimethyl ammonium chloride copolymer (SDDACC) (Nittobo Medical co., ltd.) were chosen as an accelerator and a leveler at concentrations of 2 ppm and 1.5 ppm, respectively. 1 ppm of 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (2M5S) (Wako Chemical) was also added as a second leveler for investigation in order to reduce the thermal expansion of electrodeposited copper. In addition, a conventional electrolyte containing 200 g/L $CuSO_4.5H_2O$, 25 g/L H_2SO_4, 50 ppm Cl^-, 2ppm SPS, 25ppm PEG (average m.w.10000), and 1.5 ppm SDDACC also was used to fill the TSV. This conventional copper TSV serves as a reference for comparing copper pumping and stress in silicon.

All electrochemical measurements were performed with an electrochemical system Hokuto Denko HZ7000 in a three-electrode glass cell containing 60 mL of solution. A 5 mm diameter Pt rotating disk electrode (RDE) was used as the working electrode. The rotation speed of the RDE was controlled by Hokuto Denko HZAP1203n and the rotation speed of RDE was between 10 rpm and 1000 rpm. Pt wire was used as the counter electrode. All measured potentials are referenced to a saturated calomel electrode (SCE) electrode. Cyclic voltammetry (CVS) was carried out by sweeping the potential from 0.5V to -0.3V and back to 0.5V. Linear sweep voltammetry (LSV) was swept from 0.15V to -0.3V. The scan rates of both CVS and LSV were 20 mV/s.

A 15 mm copper pipe was made to measure the thermal expansion of the electrodeposit. Then, the expansion length of the copper pipe was measured using a thermal expansion meter

(TD5020SA, NETZSCH). The detailed procedure used to form a copper pipe and how to measure the thermal expansion of copper pipe were mentioned in the section "3.2. Experimental" of chapter 3 in this thesis.

A fragment silicon chip containing many TSVs was used as a plating sample. The TSV diameter and depth are 5μm and 20μm, respectively. The details of the TSV structure are as follows: 500 nm SiO_2 as a dielectric layer, 300nm Ti as a barrier layer, 200nm Cu as a seed layer. In this study, the SiO_2 dielectric layer was formed by plasma-enhance chemical vapor electrodeposition (PECVD) of Tetraethyl orthosilicate (TEOS). TSV filling experiments were carried out in a beaker containing 150 mL of electrolyte solution. The electrolyte was purged with oxygen for 30 minutes prior to electrodeposition. A phosphorus-containing copper bar was used as the anode. The TSV chip was attached to cathode holder that placed in the beaker about 2 cm below the electrolyte surface and rotated at 1000 rpm to produce a good convection. The TSV was filled using periodic pulse reverse current generated by Pulse generator HA-211, Hokuto Denko and Galvanostat/Potentiostat HA-301, Hokuto Denko. The pulse conditions were t_{off}: t_{on}: $t_{reverse}$ = 100: 200: 10 ms and i_{on}: $i_{reverse}$ = 1:6. After filling, the silicon chip fragment was polished by using emery paper and the TSV cross section was observed.

Prior to copper pumping measurements, commercial CMP was performed to remove copper over burden and obtain a flat surface. A scanning electron microscope (SEM) with a 70° tilted heating SEM stage (JSM 5500S, JEOL) was used for in situ copper pumping measurements. To evaluate the stress in silicon, Raman measurement was performed with a commercial Jobin Yvon U1000 Raman spectrometer. A 457.9 nm Ar^+ laser and charge-coupled device (CCD) were used as excitation light and detector, respectively.

5.3. Results and Discussion

Addition of 2M5S. − The influence of adding 2M5S additive to the VMS solution during a CVS measurement recorded at an RDE rotation speed of 1000 rpm is shown is Figure 40. In case of the VMS solution only, a small peak is observed at -0.1 V on the negative-going sweep direction. This peak is due to the formation of copper nanoparticles on the Pt working electrode[1]. When adding 2M5S to the VMS solution, the inhibition of Cu electrodeposition is evident, with a decrease in both cathodic current and anodic stripping area. In addition, the cathodic peak observed in the voltammogram of the VMS-2M5S solution shifts to a more negative potential compared to that of VMS solution, indicating that 2M5S acts as an inhibitor by increasing the overpotential of copper electrodeposition. 2M5S can form an inhibitor film consisting of a Cu(I)2M5S complex on the copper surface via a thiol group or N atoms in the five-membered ring[2,3].
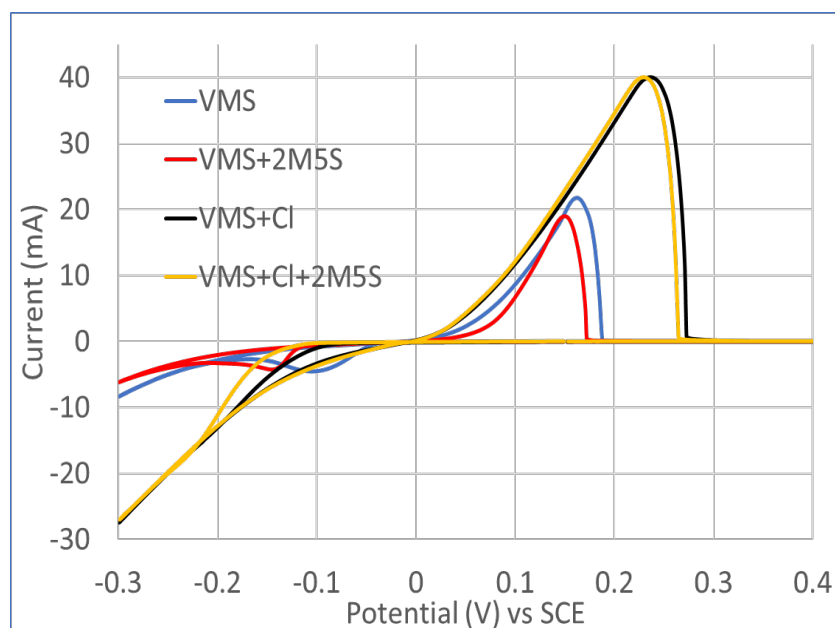

Figure 40. Cyclic voltammograms of different solutions measured at 1000 rpm. VMS solution contains 70g/L CuSO4.5H$_2$O, 75g/L H$_2$SO$_4$.
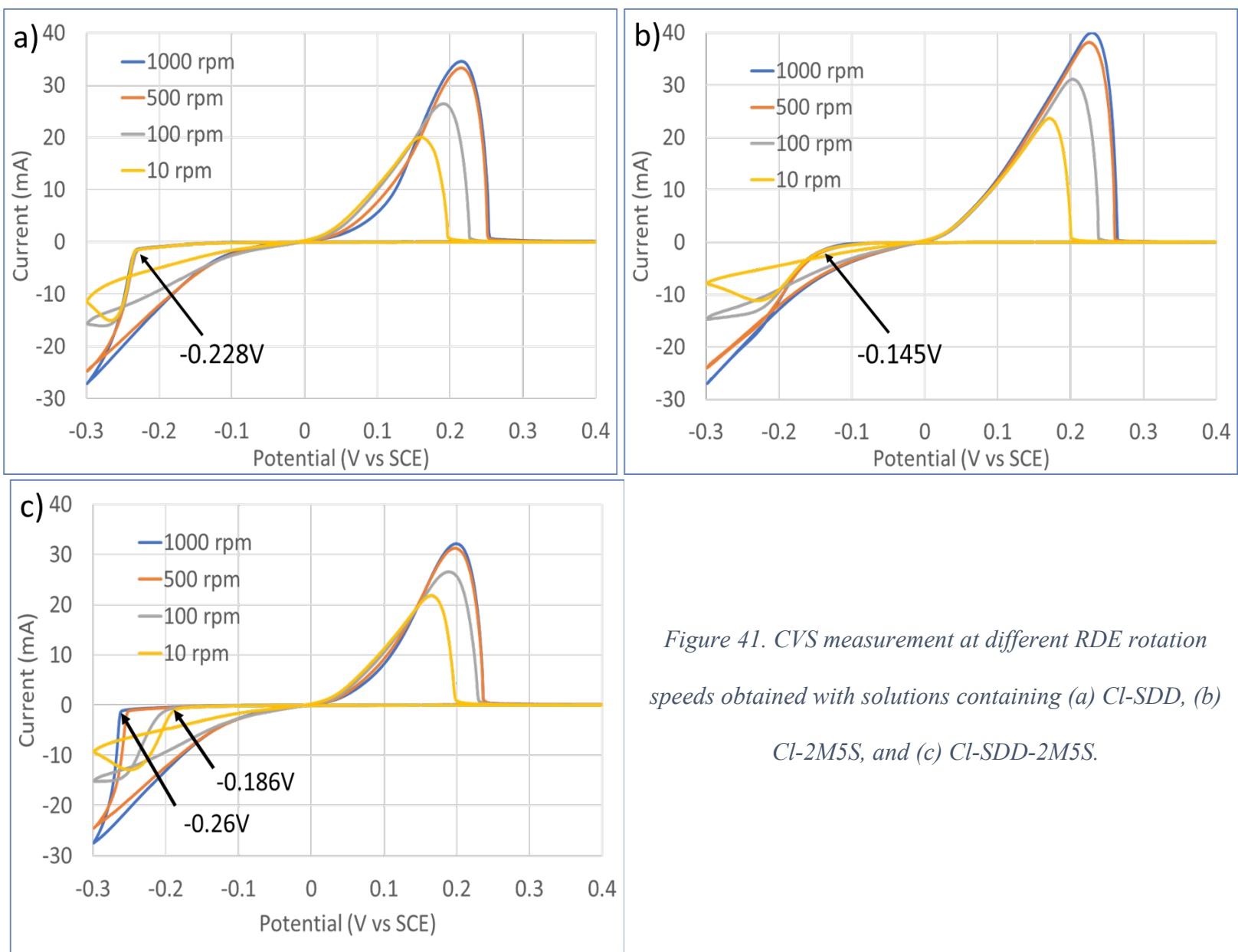
70

Figure 41. CVS measurement at different RDE rotation speeds obtained with solutions containing (a) Cl-SDD, (b) Cl-2M5S, and (c) Cl-SDD-2M5S.

Addition of Cl-2M5S. − Cl⁻ ions play an important role in electrodeposition of copper, including promoting accelerator and supporting inhibitor[4,5]. The effect of adding Cl-2M5S was also investigated and is shown in Figure 40. Compared to the voltammogram of the VMS solution individually, the acceleration of copper electrodeposition is evident with a significant increase in cathodic current and anodic stripping area in the voltammogram of the VMS-Cl solution, as shown in Figure 40. This acceleration effect of Cl⁻ has been reported in the literature[6,7]. In contrast, addition of 2M5S to the VMS solution in the presence of 50 ppm Cl⁻ increased the inhibition of copper electrodeposition on the negative going sweep, along with the decrease of anodic stripping peak. This indicating that addition of chloride does not disrupt the inhibition of copper deposition of 2M5S.

Addition of Cl-SDD-2M5S. − Next, Figure 41 shows the CVS measurement results of a solution containing Cl-SDDACC, Cl-2M5S, and Cl-SDDACC-2M5S at different RDE rotation speeds. In solution containing Cl-SDD, the breakdown of significant inhibition is apparent as the potential is scanned below −0.228V (Figure 41a). In addition, the Cl-SDDACC solution shows a lower cathodic current and smaller anodic stripping area at lower rotation speeds, indicating that the inhibition of copper electrodeposition decreases with the decrease of rotation. Similarly, in Figure 41b, it is obvious that the breakdown potential at all the RDE rotation speeds is -0.145V, and the inhibition also decreases monotonically with RDE rotation speed in the solution containing Cl-2M5S. However, compared to the breakdown potential of solution containing SDDACC, the breakdown potential of solution containing 2M5S is more positive, meaning the inhibition effect of 2M5S is much weaker.

In Figure 41c, when both SDDACC and 2M5S were added in the solution, the breakdown potential of Cu reduction obtained from the combination of SDDACC and 2M5S is more negative

than those obtained from the individual additions of SDDACC and 2M5S at 500, 1000 rpm. Meanwhile, the breakdown potential of Cu reduction obtained from the combination of SDDACC and 2M5S at 10 and 100 rpm are observed between those from the individual additions of SDDACC and 2M5S. If SDDACC and 2M5S are co-adsorbed or competitively adsorbed, the breakdown potential of solution containing SDDACC and 2M5S would have been observed at only more negative or only between those from the individual additions of the SDDACC and 2M5S, respectively. This result suggested that the SDDACC and 2M5S could form a new composite to inhibit the electrodeposition of copper, and the inhibition of the new SDDACC-2M5S composite is strongly depend on the convection conditions.

Addition of Cl-SPS-SDDACC-2M5S. − In order to investigate the interactions between the organic additives, and their dependency on the convection conditions, linear sweep voltammetry was performed under RDE rotations of 1000 and 10 rpm.

In Figure 42a, the potential-current curves of SPS-SDDACC, SPS-2M5S, and full chemistry SPS-SDDACC-2M5S at 1000 rpm is identical to that SDDACC, 2M5S and SDDACC-2M5S, respectively. This indicating that the adsorption of SPS on the copper surface is negligible and the copper electrodeposition is governed by the adsorption of SDD-2M5S only without SPS at 1000 rpm or via outside convection condition.

In contrast, at 10 rpm, the potential-current curves of SPS-SDDACC and SPS-2M5S are different from two individual curves of SDDACC and 2M5S, suggesting that there is competitive adsorption between SPS and SDD; SPS and 2M5S on the copper surface at low convection condition. Furthermore, compared with the potential-current curve SDDACC-2M5S, the potential-current curve of full chemistry SPS-SDDACC-2M5S shifts to more positive potential. It means that copper reduction at the TSV bottom with negligible convection is controlled with the

adsorption or acceleration of SPS. In summary, the combination of the inhibition effect of SDDACC-2M5S at the via outside and the acceleration effect of SPS at the via bottom could lead to perfectly TSV filling.
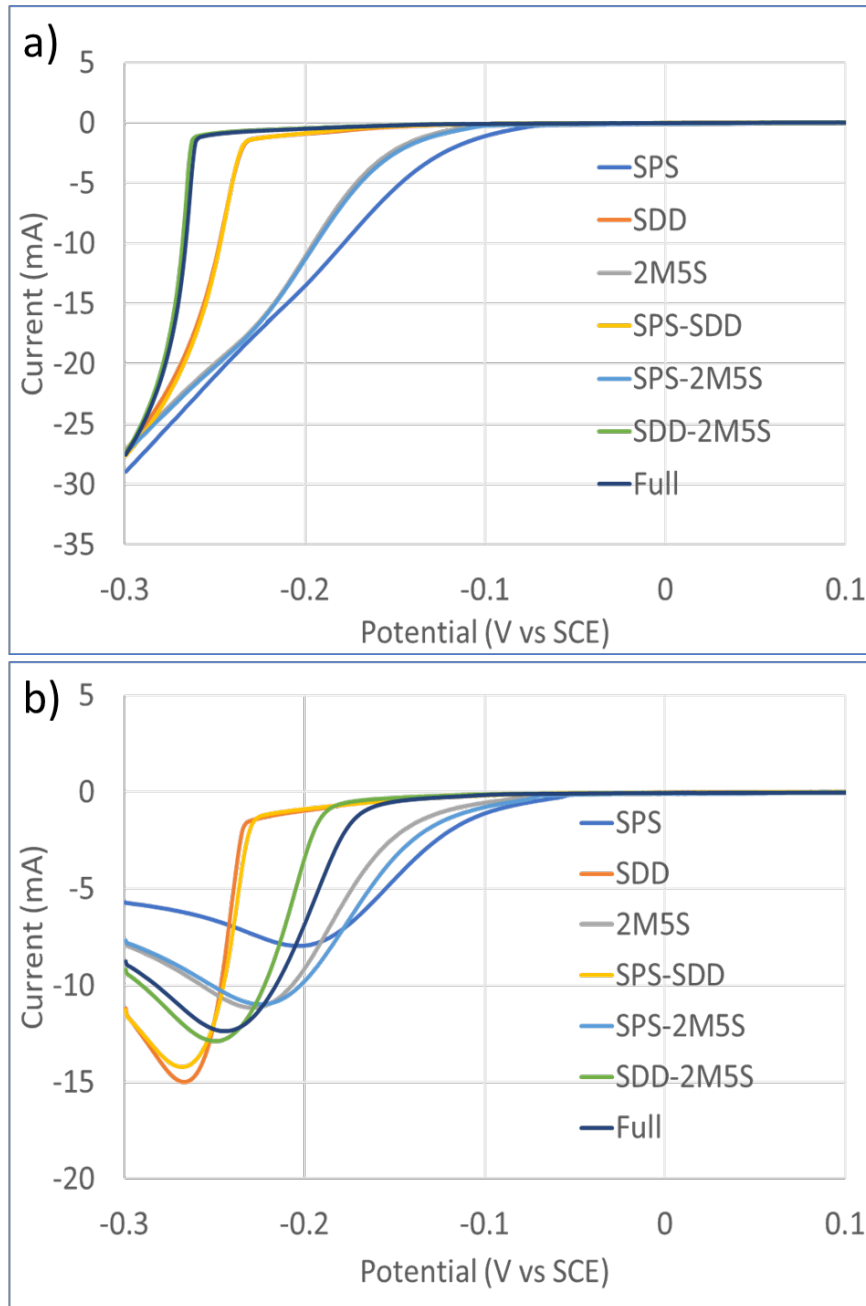

Figure 42. Linear sweep voltammograms of all combinations of SPS, SDD, and 2M5S at (a) 1000 rpm and (b) 10 rpm.

Thermal expansion measurement. − The 15 mm copper pipes were electrodeposited in the solution containing different combinations of additive. The thermal expansions of these copper pipes were measured in range of RT - 400°C and are shown in Figure 43. The expansion of copper pipes electrodeposited on VMS and VMS-Cl-SPS-SDDACC solutions is nearly identical to each other and increases linearly with temperature. It indicates that Cl-SPS-SDDACC has negligible effect on the thermal expansion of electrodeposited copper. The effect of the addition of Cl⁻ and 2M5S on the expansion of electrodeposited copper is evident through the reduction of copper expansion, with the expansion value of 88 µm at 400°C. It seems that 2M5S incorporates in copper and reduces the expansion of electrodeposited copper. Addition of SDDACC and 2M5S further reduces the expansion of electrodeposited copper. This further expansion reduction is attributed to the enhance adsorption of new composite in electrodeposited copper as seen in Figure 41. Finally,
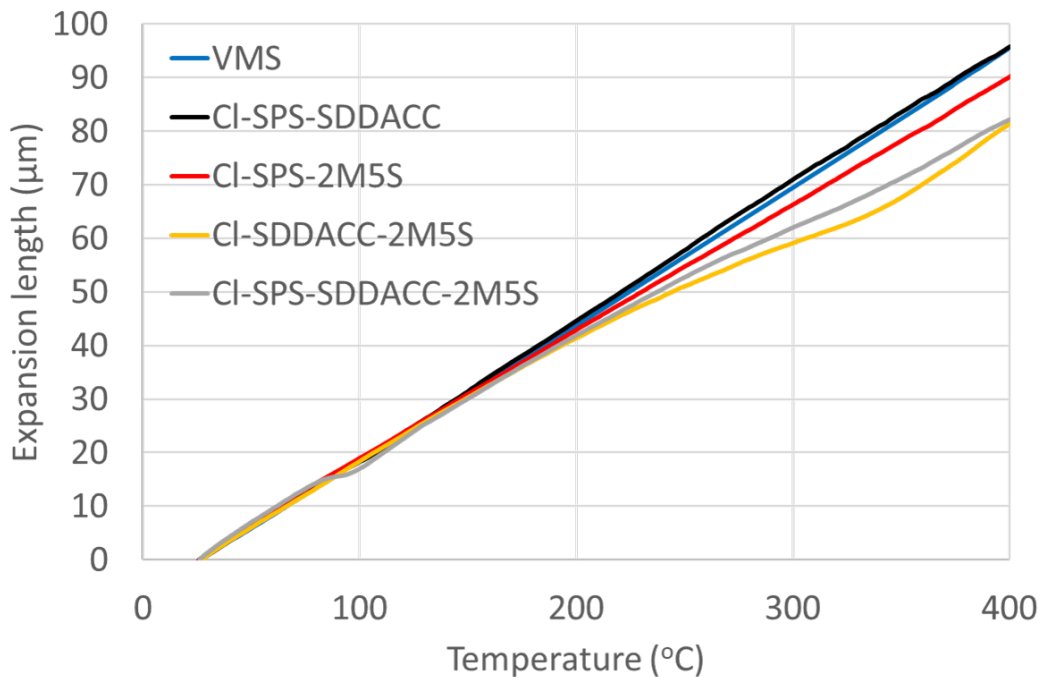

Figure 43. Thermal expansion of copper pipes electrodeposited with different additive

combinations.

compared to Cl-SDDACC-2M5S curve, addition of full chemistry Cl-SPS-SDDACC-2M5S increases the thermal expansion of copper slightly. The competitive adsorption between SPS and SDDACC- 2M5S as shown in Figure 42b may cause less amount of SDDACC-2M5S incorporated in the electrodeposited copper, leading to the slightly increase of copper thermal expansion.

TSV Filling experiment. − Figure 44 shows a cross section of a TSV filled with a solution containing various additive combinations. In all cases, Cu was electrodeposited at ions = -3 mA / cm^2 for 75 minutes. According to Figure 44, a change in the additive combination caused a change in the TSV filling profile. In solution containing SPS and SDDACC, the long seam defects are observed at the center of the TSVs, as shown in Figure 44a. In Figure 44b, the addition of SPS and
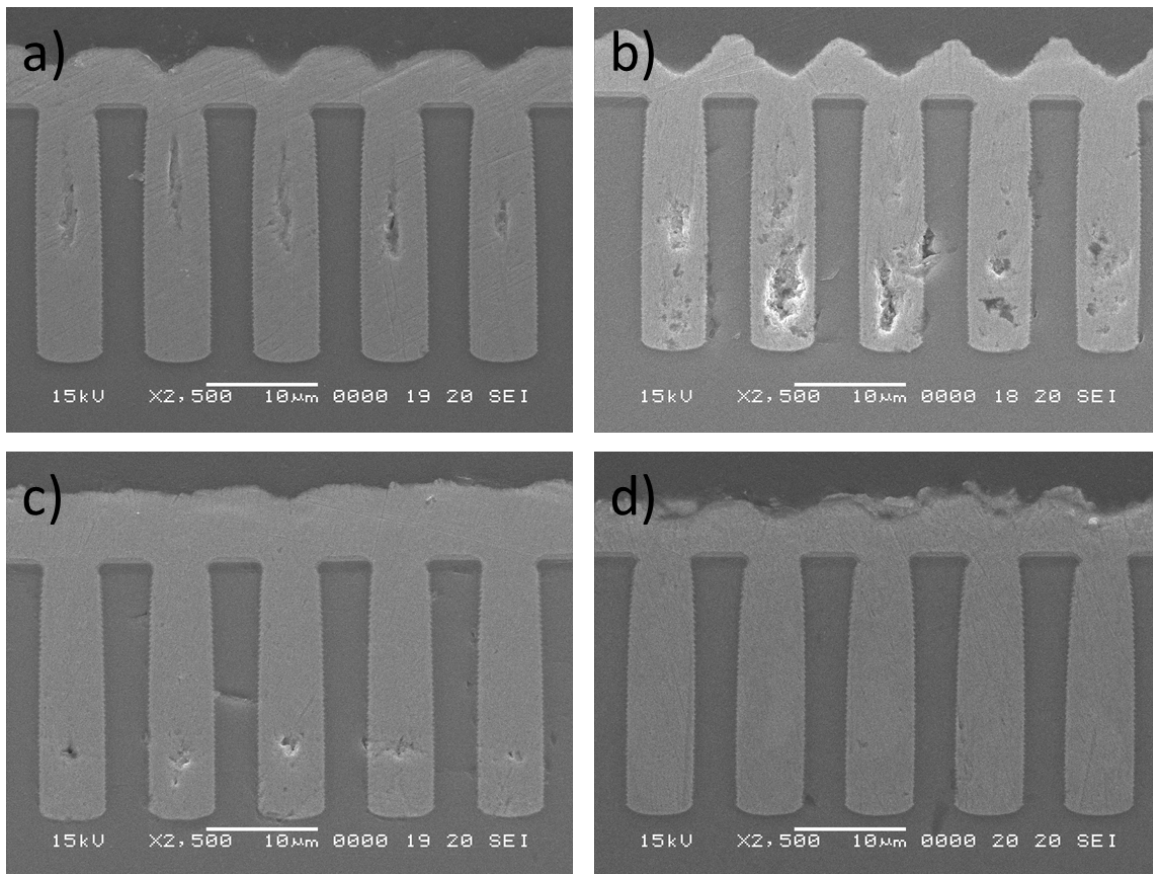

Figure 44. Cross sections of TSV filling with different solutions: (a) SPS-SDD, (b) SPS-2M5S, (c) SDD-2M5S and (d) SPS-SDD-2M5S.

2M5S causes the large voids in the TSVs. In case of solution containing SDDACC-2M5S, the small voids are observed at the bottom of the TSVs. These filling profiles are understandable because the inhibition effect of 2M5S is weaker than the inhibitory effect of SDDACC and inhibition of effect of SDDACC-2M5S depends on the convention conditions, as mentioned in Figure 41. However, in the presence of full additives (SPS-SDDACC-2M5S), the TSVs were fully filled without any seams and voids, as shown in Figure 44d. The perfect TSV filling profile is attributed to the acceleration effect of SPS at the via bottom and strong inhibition effect SDDACC-2M5S composite at the via outside, as mentioned in Figure 42.

Copper pumping measurement. − After filling the TSV, the silicon chip was CMP for copper pumping measurement. For comparison, copper pumping measurements in a conventional copper TSV were also performed as a reference. Figure 45 shows the in-situ copper pumping measurement results of conventional copper and low TEC copper TSVs at different temperatures. As seen in Figure 45a, after CMP, copper and silicon surfaces are flat at room temperature. When annealing to 300°C, the copper pumping is clearly viewed at the center of TSVs. With further increased the annealing temperature to 400°C and 500°C, copper pumping height becomes higher. It was reported by other authors that the pumping height increases with increasing annealing temperature[46,47]. This high copper pumping will cause reliability problem during fabrication process. Moreover, as seen in Figure 45a, the copper pumping is not uniform, with some TSVs having higher copper pumping and some TSVs having lower TSV pumping. In case of low TEC copper in Figure 45b, the copper pumping is visualized at 300°C. On the other hand, even if the annealing temperature is further increased to 500°C, it is difficult to determine the further increase of copper pumping height. In short, the low TEC copper TSVs sample showed much less pumping height in comparison to conventional copper TSVs sample when annealing.
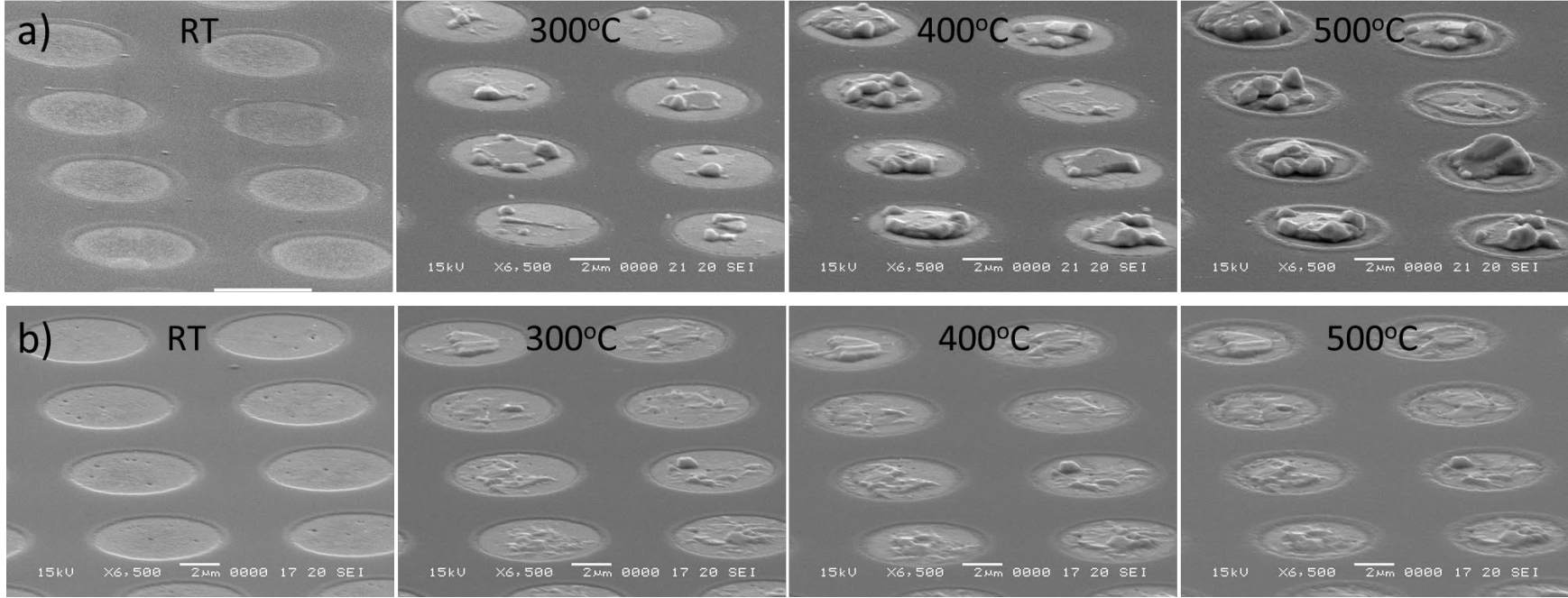
Figure 45. In-situ Cu pumping measurement at different temperatures (a) Conventional copper and (b) low TEC copper in PECVD SiO₂ TSV.

Figure 46 shows the cross section of conventional copper TSV (Figure 46a) and low TEC copper TSV (Figure 46b) after measuring copper pumping at 500°C. In Figure 46a, the copper pumping height in PECVD SiO_2 TSV is about 2 μm. Compared with copper pumping height of 1.2 μm in APCVD SiO_2 TSV in the chapter 4, the copper pumping height in PECVD SiO_2 TSV is much higher (about 0.8 μm). However, unlike APCVD SiO_2 TSV, no crack was observed in case of PECVD SiO_2 TSV. According to J. Foggiato, the SiO_2 liner fabrication with PECVD and APCVD had the different properties such as hardness and Young's modulus[8]. Therefore, different liner layers have different effects on copper pumping. In Figure 46b, the copper pumping height of low TEC copper PECVD SiO_2 TSV is only 0.5 μm. This means that low TEC copper effectively reduces the copper pumping.
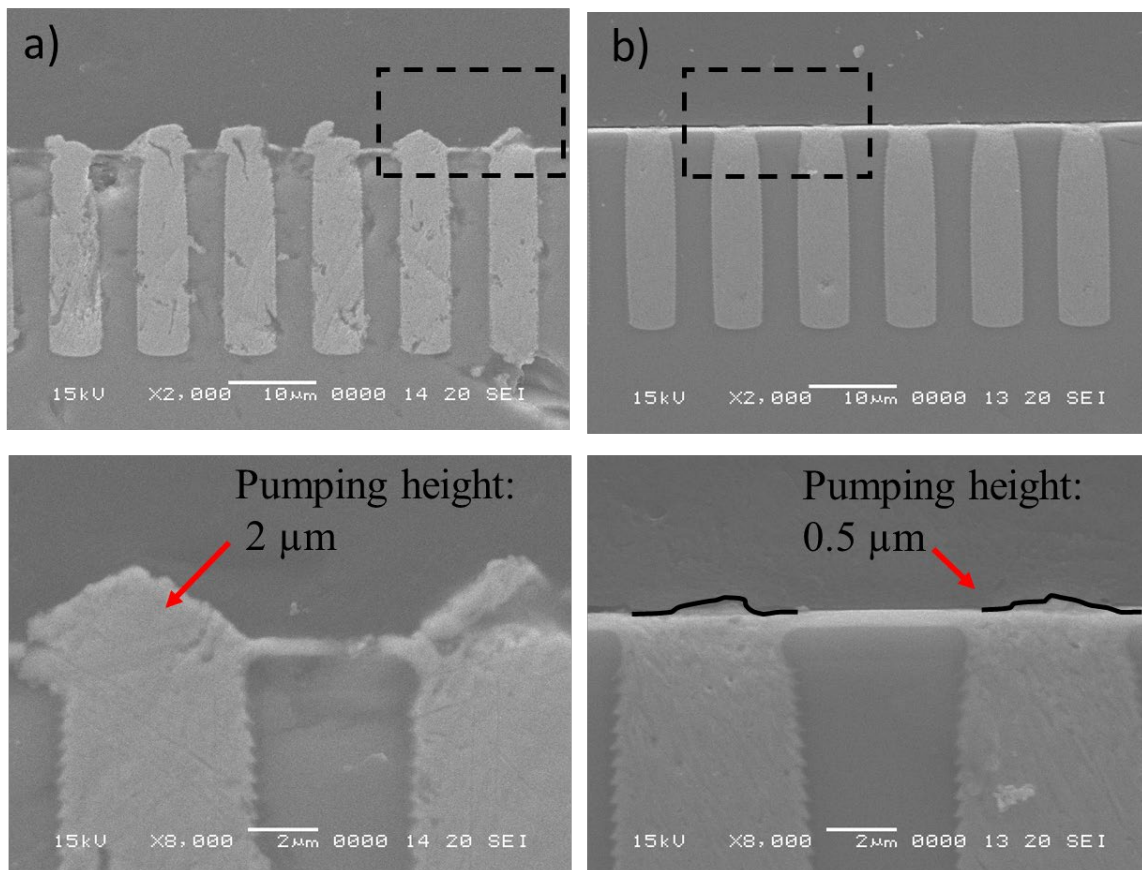

Figure 46. TSV cross sections of (a) conventional copper and (b) low TEC copper TSV after annealing at 500°C.

KOZ measurement. −Micro-Raman spectroscopy is known as a non-destructive method for investigating stress induced by TSV. Figure 47a shows the stress measurement position of micro-Raman spectroscopy. Line scan micro-Raman spectroscopy was performed on the top surface between the two TSVs, and the distance between the two TSVs was 8.2 μm. The Si
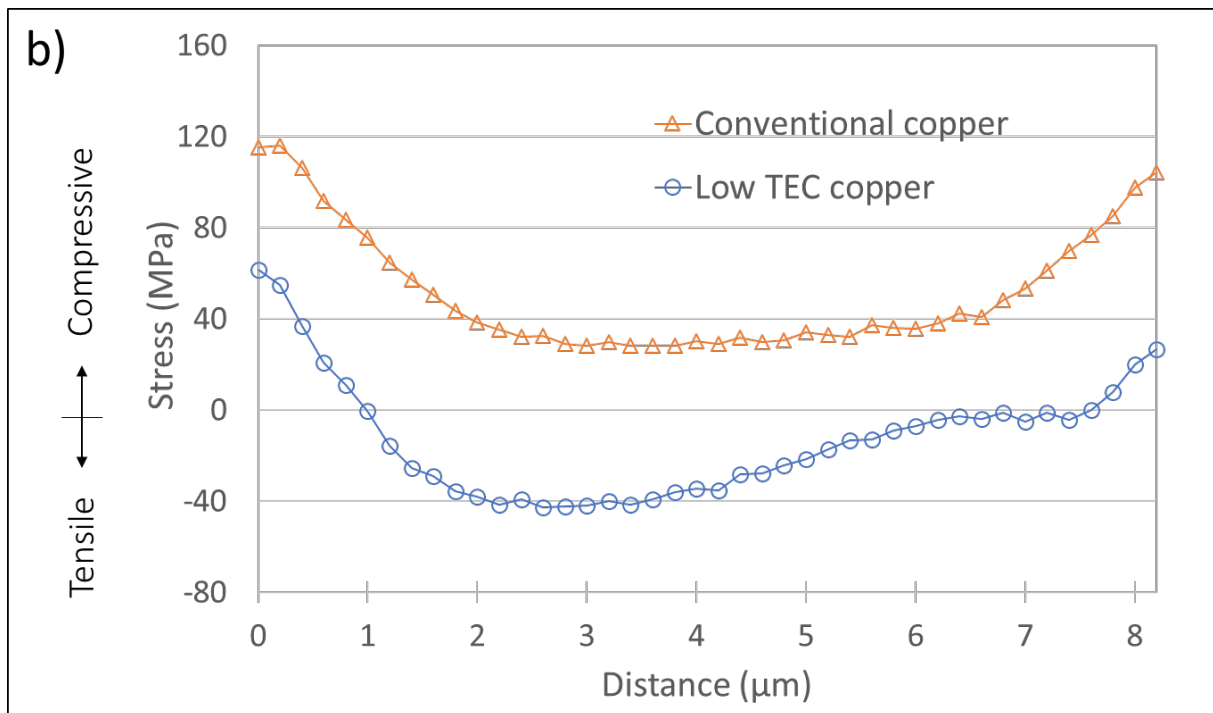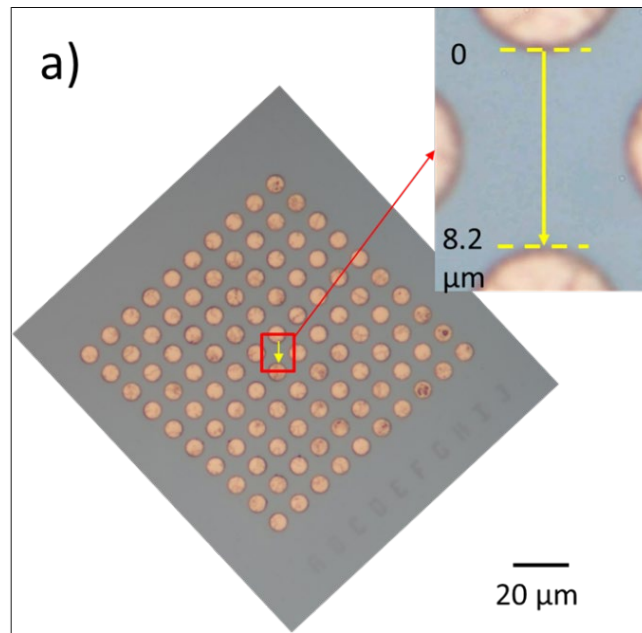

Figure 47. Stress measurement by micro-Raman spectroscopy

(a) measurement line, (b) measurement result.

peak position of unstressed silicon is assumed to be zero and the stress graph is plotted based on Raman peak shift. Figure 47b shows the line scan stress results for conventional (red curve) and low TEC copper TSV (blue curve) samples after annealing at 500°C. For a conventional copper TSV, the stress curve suggests that the stress in the silicon area between the two Cu TSVs is positive, indicating that the Si is under compressive stress. It is observed that the maximum stress was concentrated at the edge of the Cu TSV. As the distance between the Cu TSV and the measurement point increases, the stress decreases, reaching a steady state of 40 MPa at the intermediate distance between two adjacent TSVs. This trend is consistent with the one observed in literature[9,10]. In the region less than 2 µm from Cu TSV, the stress in silicon is relatively large and 2 µm can be defined as KOZ region of conventional copper TSVs. This large stress is mainly caused by the large mismatch in TEC between Cu and Si. A similar trend is observed in case of low TEC copper TSVs. The stress curve starts with compression at the TSV edge, reaches zero, and becomes tensile as the distance to the TSV increases. Compared with thermal stress curve in Si around the conventional copper TSV, thermal stress curve in Si around the low TEC copper TSVs was much lower and the KOZ also was reduced to about 1 µm. This means that low TEC copper not only reduces copper pumping but also effectively reduces the thermal stress in Si around the TSVs.

5.4. Conclusions

In this chapter, I investigated the electrochemical behavior 2M5S additive by CVS and LSV measurements. The 2M5S additive showed an inhibition effect during electrodeposition of copper, both in the absence and presence of Cl⁻. Using a combination of the 2M5S leveler with another SDDACC leveler and SPS accelerator, the thermal expansion of copper was reduced and the TSV was filled without defects. After the TSV was perfectly filled, copper pumping measurements and micro-Raman measurements were performed on low TEC copper TSV electrodeposited in a solution containing 2M5S and conventional copper TSV. The SEM

results showed that the copper pumping height of low TEC copper in PECVD SiO$_2$ TSV was only 0.5 μm. Meanwhile, the copper pumping height of reference conventional copper in PECVD SiO$_2$ TSV was about 2 μm. Furthermore, compared with thermal stress curve in silicon around the conventional copper TSV, thermal stress curve in silicon around the low TEC copper TSV was much lower and the KOZ also was reduced to about 1 μm.

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CHAPTER 6: SUMMARY

Through Silicon Via (TSV) enabled by copper electrodeposition is the key technology of 3DIC packaging, which allow high packaging density, high speed signal transmission, and reduce power consumption. TSV technology has a bright future, with TSV packaging revenues estimated to increase to about $4.5 billion in 2023 (Source: 2.5D / 3D TSV & wafer-level stacking technology & market updates 2019 report by Yole Development). However, TSV technology still has some challenges to solve for mass production. The first challenge is the high TSV production cost, especially copper electrodeposition. There are several ways to reduce the cost of copper electrodeposition, including using latest electrodeposition tools and reducing the time required for electrodeposition. However, the latest electrodeposition tools are expensive. Furthermore, large clean room areas need to accommodate a large amount of electrodeposition tools. Increasing current density, which means shorten the electrodeposition time, is a promising solution to reduce electrodeposition time. However, if the current density is too high, constriction occurs at the TSV opening and voids will be formed. The second challenge is related to the large mismatch in thermal expansion coefficient (TEC) between copper and silicon. Due to the large TEC mismatch between the copper and silicon substrate, copper expands much more than silicon during the annealing process, causing high thermal stresses inside copper TSV and in surrounding silicon. The thermal stress inside the copper TSV cause some reliability problems such as copper pumping, voiding, cracking, and delamination. The thermal stress also causes the degradation in silicon surrounding the copper TSV. Keep Out Zone (KOZ) is defined as the area around the TSV where transistors cannot be located to prevent device failure. These challenges are detail addressed in chapter 1 and the solutions to these challenges have been investigated in chapter 2-5 of this thesis.

In chapter 2, sulfonated diallyl dimethyl ammonium bromide copolymer (SDDABC) was used as a leveler. The leveler behavior was characterized by CVS method with different concentrations at different RDE rotation speeds. SDDABC forms a strong inhibition layer on copper surface when 16 ppm concentration is added. Super bottom-up TSV filling with nearly no deposited on TSV sidewall was achieved with 16 ppm of SDDABC. With this super bottom-up TSV filling, a 20 x 45μm TSV was filled in 5 minutes. This is 5 times faster than that with V-shape.

In chapter 3, I have found out low TEC copper electrodeposited in a solution containing 2-Mercapto-5-benzimidazolesulfonic acid sodium salt dihydrate (2M5S) additive by measuring the thermal expansion of a copper pipe with the thermal expansion meter. In addition, the contraction mechanism of low TEC copper has been proposed based on the detailed observations of electrodeposited by SEM, FE-Auger, and X-ray diffraction. The as-deposited copper has carbon inclusions in the lattice. The carbon diffuses out at high temperature, hence contracting the lattice constant. This non-equilibrium to equilibrium transformation by annealing causes copper contraction during the annealing.

In chapter 4, I have applied low TEC copper, which was found in chapter 3, to fill the atmospheric pressure chemical vapor deposition (APCVD) SiO_2 TSV. Copper pumping measurements of APCVD SiO_2 TSV were performed using a heating SEM stage. The copper pumping height was reduced from 1.2 μm for conventional copper to only 0.3 μm at 500°C for low TEC copper and no cracks occur at the via bottom corner. In addition, the resistivity values of low TEC copper are always lower than that of conventional copper in as electrodeposited copper and after annealing at different temperatures

In chapter 5, the electrochemical behaviors of 2M5S in the electrolyte have been investigated using cyclic voltammetry stripping (CVS) and liner sweep voltammetry (LSV) measurements. The 2M5S additive exhibited an inhibition effect during electrodeposition of

copper, both in the absence and presence of Cl$^-$. Using a combination of the 2M5S leveler with another SDDACC leveler and SPS accelerator, the thermal expansion of copper was reduced and the TSV was filled without defects. After the TSV was perfectly filled, copper pumping measurements and micro-Raman measurements were performed on low TEC copper TSV electrodeposited in a solution containing 2M5S and conventional copper TSV. The SEM results showed that the copper pumping height of low TEC copper in PECVD SiO$_2$ TSV was only 0.5 μm. Meanwhile, the copper pumping height of reference conventional copper in PECVD SiO$_2$ TSV was about 2 μm. Furthermore, compared with thermal stress curve in silicon around the conventional copper TSV, thermal stress curve in silicon around the low TEC copper TSV was much lower and the keep out zone (KOZ) also was reduced to about 1 μm.

Acknowledgements

List of Publications

1. V. Q. Dinh and K. Kondo, "Low Thermal Expansion Coefficient Electrodeposited Copper and Its Contraction Mechanism with Annealing", *J. Surf. Finish. Soc. Japan*, vol. 68, no. 2, pp. 113–114, 2017.

2. V. Q. Dinh, K. Kondo, "Low Thermal Expansion Coefficient Electrodeposited Copper and Its Contraction Mechanism by Annealing", *ECS J. Solid State Sci. Technol.*, vol. 6, no. 8, pp. P566-P569, 2017.

3. V. Q. Dinh, K. Kondo, T. Hirato, "Reduction of Thermal Stress in Copper TSV due to Annealing by Low TEC Copper", *ECS Trans.*, vol. 86, no. 8, pp. 17-21, 2018.

4. V. Q. Dinh, V. H. Hoang, K. Kondo, T. Hirato, "Thermal Stress Reduction of Copper Through Silicon Via (TSV) with Annealing", *ECS J. Solid State Sci. Technol.*, vol. 7, no. 11, pp. P689-P692, 2018.

5. V. Q. Dinh, V. H. Hoang, K. Kondo, T. Hirato, "Bottom-Up TSV Filling Using Sulfonated Diallyl Dimethyl Ammonium Bromide Copolymer as a Leveler", *J. Electrochem. Soc.*, vol. 166, no. 12, pp. D505-D507, 2019.

6. V. Q. Dinh, K. Kondo, T. Hirato, "Electrochemical Behavior of 2M5S and Its Influence on Reduction of Cu Pumping and Keep-Out Zone", *J. Electrochem. Soc.*, vol. 167, no. 6, p. 062504, 2020.

List of Presentations

1. Van Quy Dinh, Kazuo Kondo, " Low thermal expansion coefficient electrodeposited copper and its contraction mechanism by annealing", The Surface Finishing Society of Japan 136th Lecture Meeting, Kanazawa Institute of Technology Ohgigaoka Campus, Nonoichi, Japan, September 14, 2017 (Oral).

2. Van Quy Dinh, Kazuo Kondo, and Tetsuji Hirato, "Reduction of stress due to annealing of copper TSV by the low TCE copper", The Surface Finishing Society of Japan 137th Lecture Meeting, Shibaura Institute of Technology, Tokyo, Japan, March 12, 2018 (Oral).

3. Dinh Van Quy, Kazuo Kondo, and Tetsuji Hirato, "Reduction of TSV thermal stress by low TCE electrolyte", AiMES 2018 (ECS and SMEQ Joint International Meeting), Cancun, Mexico, September 30 - October 4, 2018 (Oral).
   (Student Oral Presentation Award)

4. Van Quy Dinh, Kazuo Kondo, and Tetsuji Hirato, " Reduction of TSV thermal stress by low TCE electrolyte", The Surface Finishing Society of Japan 20th Kansai Branch Forum, Konan University Port Island Campus, Kobe, Japan, November 22, 2018 (Oral).

5. Dinh Van Quy, Kazuo Kondo, and Tetsuji Hirato, "Reduction of Copper TSV Pumping", IEEE 2019 International 3D Systems Integration Conference, Sendai, Japan, October 8 - 10, 2019 (Poster).

6. Van Quy Dinh, Kazuo Kondo, and Tetsuji Hirato, " Sulfonated diallyl dimethyl ammonium bromide copolymer as a leveler for high-speed copper TSV filling", The Surface Finishing Society of Japan 21th Kansai Branch Forum, Konan University Port Island Campus, Kobe, Japan, November 22, 2019 (Oral).