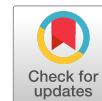


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Design and formation of SiC (0001)/SiO₂ interfaces via Si deposition followed by low-temperature oxidation and high-temperature nitridation

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We report an effective approach to reduce defects at a SiC/SiO₂ interface. Since oxidation of SiC may inevitably lead to defect creation, the idea is to form the interface without oxidizing SiC. Our method consists of four steps: (i) H₂ etching of SiC, (ii) Si deposition, (iii) low-temperature (~750 °C) oxidation of Si to form SiO₂, and (iv) high-temperature (~1600 °C) N₂ annealing to introduce nitrogen atoms. The interface state density estimated by a high (1 MHz)-low method is in the order of 10¹⁰ cm⁻² eV⁻¹, two orders of magnitude lower than that of an interface formed by SiC oxidation.

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Development of high-efficiency power devices is indispensable for meeting the growing requirements of power consumptions and for realizing a sustainable society. In this perspective, silicon carbide (SiC) has been widely accepted as an alternative to silicon (Si) because of its unique material properties (i.e. wide bandgap, high critical electric field, and high thermal conductivity).^{1,2} In particular, SiC metal-oxide-semiconductor field effect transistors (MOSFETs) are promising for low-loss and fast power switches.^{1–3} The performance of MOSFETs is nevertheless limited by the quality of SiC/silicon dioxide (SiO₂) interfaces; the interface state density (D_{IT}) at SiC/SiO₂ interfaces near the conduction band edge (E_C) of SiC (10¹²–10¹³ eV⁻¹ cm⁻²) is at least two orders of magnitude higher than that of typical Si/SiO₂ systems (~10¹⁰ eV⁻¹ cm⁻²).^{4,5} A significant portion of electrons at the inversion layer of MOSFETs are thereby trapped by the interface states, resulting in low effective channel mobility (μ_{CH}).^{6–8}

Prior studies have indicated various methods to reduce the D_{IT} at a SiC/SiO₂ interface. The methods are classified into two groups: methods that rely on impurity incorporation and those do not (i.e. oxidation/annealing only). The former approach includes impurities such as nitrogen (N),^{9–12} phosphorus (P),^{13,14} boron (B),¹⁵ sodium (Na),^{16,17} and barium (Ba).¹⁸ Among them, incorporation of N by nitric oxide (NO)^{9,10} or nitrous oxide (N₂O)^{11,12} annealing has been a standard processing step. By introducing N atoms, the D_{IT} near E_C is reduced to ~10¹¹ eV⁻¹ cm⁻² while not significantly degrading the oxide reliability. However, since the reduction in D_{IT} is insufficient, it is shown that the carrier trapping effect by the interface states is severe even after proper NO annealing.⁸ Although remarkable increase in the μ_{CH} (>80 cm² V⁻¹ s⁻¹) is reported for other impurities (i.e. P, B, Na, and Ba), there remains a concern on the oxide reliability. For instance, incorporation of P, Na, and Ba leads to the generation of oxide traps,¹⁹ threshold voltage instability,¹⁶ and degradation in the insulating property,²⁰ respectively. The latter approach involves thin (~15 nm) oxidation with rapid cooling (>600 °C min⁻¹),²¹ high-temperature oxidation (>1400 °C),^{22,23} and post-oxidation annealing in low-oxygen-partial-pressure

ambient at high-temperature (~1500 °C).²⁴ Although reduction in D_{IT} is achieved by these methods, a high-mobility MOSFET is not reported so far. These facts indicate a reasonable hypothesis that the oxidation of SiC inevitably leads to degradation of interface properties via introduction of carbon defects^{4,25–27} and/or fluctuations in the conduction band.^{28–30}

In this paper, we present an alternative pathway to reduce defects at SiC (0001)/SiO₂ interfaces. To avoid the oxidation-induced interface degradation, the idea is to form SiC/SiO₂ structures without oxidizing SiC. In brief, our method proceeds in four stages: (i) hydrogen (H₂) etching of a SiC surface, (ii) Si deposition, (iii) low-temperature (~750 °C) oxidation of Si, and (iv) high-temperature (~1600 °C) nitrogen (N₂) annealing. A SiC/SiO₂ interface with substantially low D_{IT} is obtained in this manner. Based on the results, we offer guidelines to form high-quality SiC/SiO₂ interfaces.

The process flow of gate oxide formation is summarized in Fig. 1(a). We start with 4°-off-axis *n*-type SiC (0001) epilayers with a donor density of 10¹⁵–10¹⁶ cm⁻³. After cleaning the samples by the standard RCA procedure, H₂ etching of the samples' surface was performed under 0.1 MPa at 1300 °C for 3 min. Afterward, Si was deposited on the surface by introducing silane (SiH₄) and H₂, without exposing the surface to the air. The deposition was carried out under 173 Pa at 630 °C for 1.5 min, resulting in a Si thickness of typically 19–26 nm. Finally, we oxidized the samples either at 750 °C for 24 h or at 950 °C for 12 h and subsequently annealed the samples in N₂ at 1350 °C for 4 h, at 1400 °C for 45 min, or at 1600 °C for 1 min. To investigate the impact of post-oxidation treatment, we also prepared a sample where NO (10% diluted in N₂) annealing at 1250 °C for 70 min was performed instead of N₂ annealing. Besides, samples formed by oxidation of SiC were prepared; i.e. as-oxidized SiC samples and those followed by NO^{9,10} or N₂ annealing.^{31,32} H₂ etching was not performed for these thermally-oxidized SiC samples. The equivalent oxide thickness (t_{OX}) of the samples was in the range of 26–44 nm. For MOS structures, we employed circular aluminum (Al) electrodes with a diameter of about 300–500 μm.

First, we focus on the structural properties of samples formed by the proposed method. Figure 1(b) depicts the



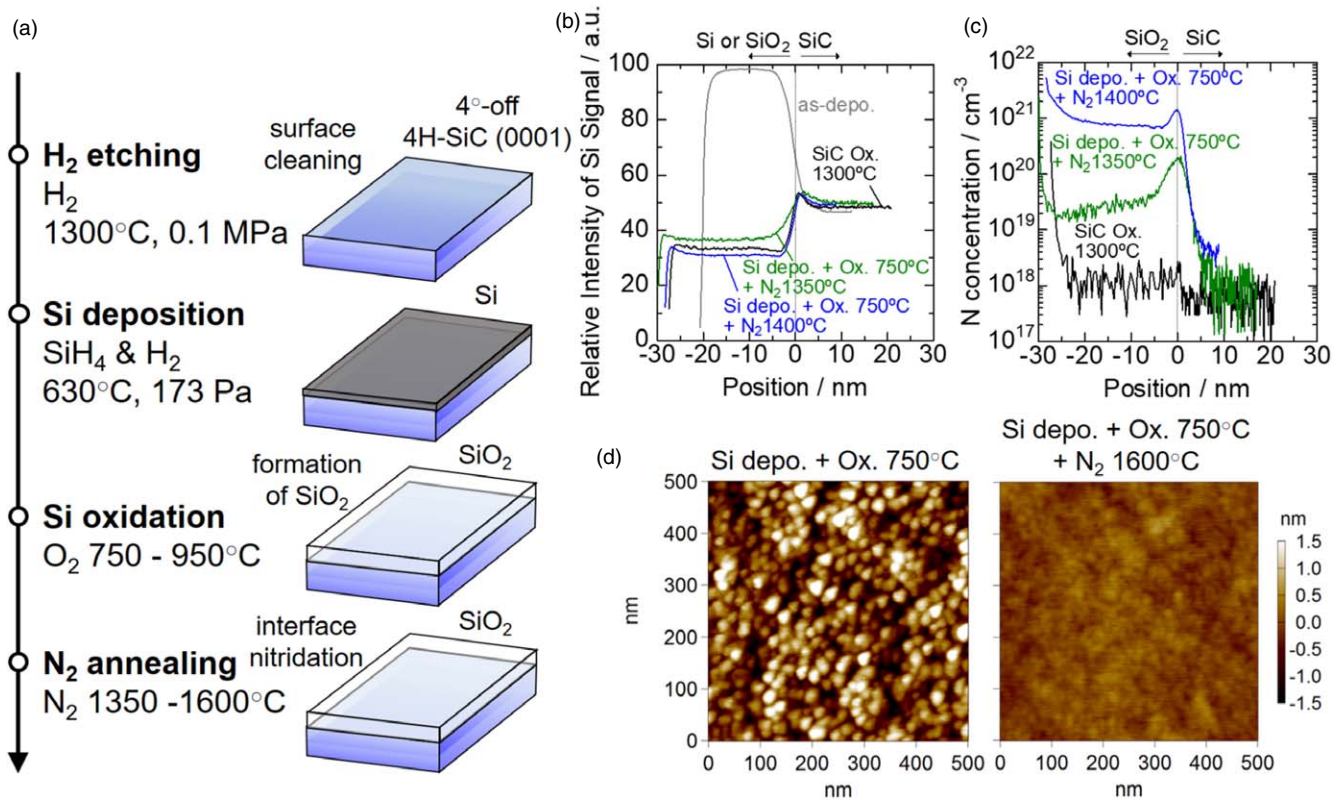


Fig. 1. (Color online) (a) Schematic process flow of forming SiC/SiO₂ structures in the present study. The conditions (i.e. temperature and pressure) and roles of each process are described in the figure. (b) SIMS profiles of Si signal intensity for SiC/SiO₂ and SiC/Si structures. The data were shifted along the x-axis so that the interface of SiC and SiO₂ (or Si) is located at the position “0 nm”. (c) SIMS profiles of N concentrations for SiC/SiO₂ structures. The data were shifted along the x-axis in the same manner as in (b). The sharp increase in the N concentrations observed near the outermost SiO₂ surfaces is likely an artifact of SIMS measurements. (d) Surface morphology of SiC/SiO₂ structures in an area of 500 × 500 nm² obtained by atomic force microscopy.

secondary ion mass spectrometry (SIMS) profiles of Si signal intensity for SiC/Si and SiC/SiO₂ structures. With Si deposition, a layer with high Si intensity (thickness ~20 nm) is indeed formed on the top of SiC. After subsequent oxidation and N₂ annealing, the Si intensity profiles become identical to that of an as-oxidized SiC sample, indicating that the deposited Si is converted into SiO₂. Here, the position of SiC/SiO₂ interfaces was determined as the point where carbon (C) signal intensity approximately becomes half of that in SiC. Even when the interface positions were defined based on oxygen (O) intensity, the positions hardly changed (within ~0.6 nm). Thus, at least within the accuracy of SIMS measurements, the deposited Si is completely oxidized with the oxidation at 750 °C for 24 h. Figure 1(c) depicts the N concentration profiles of SiC/SiO₂ samples measured by SIMS. With N₂ annealing, N atoms are distributed in the oxide, piling up at the interface of SiC and SiO₂. The N concentration increases by elevating the temperature of N₂ annealing and reaches 10²¹ cm⁻³ after annealing at 1400 °C. In this way, N atoms are introduced at the interface without proceeding the oxidation of SiC. Figure 1(d) shows typical atomic force microscope images for samples after oxidation (750 °C) and that followed by N₂ annealing (1600 °C). The root mean square surface roughness of samples before and after N₂ annealing is estimated as 0.7 nm and 0.2 nm, respectively. A rather smooth SiO₂ surface is eventually obtained, owing to the structure reconstruction of SiO₂ during high-temperature N₂ annealing.

We now focus on the electric characteristics of MOS structures. The quasi-static and 1 MHz capacitance–voltage

(C–V) characteristics of the MOS structures are shown in Fig. 2. Large frequency dispersion observed for the as-oxidized SiC sample is significantly reduced in samples formed by the proposed method, implying a strong reduction in the D_{IT} . Meanwhile, negative flat band voltage shifts are observed for the samples formed by the present method, corresponding to the effective fixed charge density of $+3.9 \times 10^{11}$, $+3.1 \times 10^{12}$, and $+2.3 \times 10^{12}$ cm⁻² for samples annealed in N₂ at 1350 °C, 1400 °C, and 1600 °C, respectively. Since more N atoms are introduced into the oxide with N₂ annealing at higher temperature [Fig. 1(c)], the

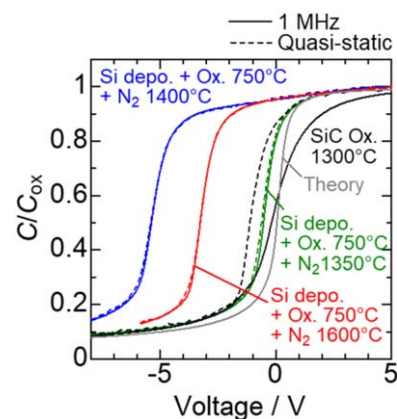


Fig. 2. (Color online) Quasi-static and 1 MHz C–V characteristics of SiC MOS structures. Theoretical deep-depletion capacitance^{33,34} assuming a donor density of 10¹⁶ cm⁻³ and oxide thickness of 30 nm is also shown for comparison. The capacitance values were normalized by the oxide capacitance (C_{ox}).

positive charge likely originates from the incorporated N atoms.

For a quantitative discussion, the energy distributions of D_{IT} were estimated by a high (1 MHz)–low method.³³⁾ The results are summarized in Figs. 3(a)–3(c). First we investigate the impact of N_2 annealing temperature in Fig. 3(a), where the result for an as-oxidized SiC sample is also shown for comparison. As expected from the C – V characteristics (Fig. 2), the samples prepared by the present method exhibit lower D_{IT} than that formed by oxidation of SiC. The D_{IT} is effectively reduced when increasing the temperature of N_2 annealing; e.g. the D_{IT} values at E_C -0.3 eV are about 1.7×10^{11} , 3.2×10^{10} , and $1.8 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ [possible error: $\pm (2-3) \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$] for samples annealed at 1350 °C, 1400 °C, and 1600 °C, respectively. Although the role of H_2 etching is uncertain, N_2 annealing plays the key role in obtaining low D_{IT} ; high-temperature N_2 annealing should be performed to introduce sufficient N atoms at the interface [Fig. 1(c)].

In Fig. 3(b), we compare the obtained D_{IT} with samples formed by thermal oxidation of SiC. As a result, the D_{IT} values near the E_C (e.g. E_C -0.3 eV) for a sample obtained by the proposed method is about ten times lower than that formed by typical methods; i.e. oxidation of SiC followed by NO ^{9,10)} or N_2 annealing.^{31,32)} Furthermore, it is confirmed that low-temperature oxidation (750 °C) followed by N_2 annealing (1600 °C) has a limited effect on a sample formed by oxidation of SiC. Since oxidation of SiC leads to the generation of defects that cannot be easily passivated, the deposition of Si is a vital step towards reducing the D_{IT} . A clearer evidence is observed in Fig. 3(c), where the impacts of Si oxidation temperature and post-oxidation treatment are investigated. When we increase the oxidation temperature of Si up to 950 °C, by which not only the deposited Si but also the SiC beneath it might be slightly oxidized, considerable increase in the D_{IT} is observed. Thus, low oxidation temperature (~ 750 °C) is necessary to guarantee that the oxidation of SiC does not take place. For oxidation at 750 °C for 24 h, we indeed confirmed that even a bare SiC sample was hardly oxidized. Although SiC/SiO₂ structures were also formed by Si deposition and subsequent oxidation in a previous study, the oxidation temperature there was rather

high (1100 °C).³⁵⁾ In such a case, it is likely that not only the deposited Si but also SiC is oxidized. As shown in Fig. 3(c), the post-oxidation treatment is also particularly important; when the annealing is performed in NO instead of N_2 , the D_{IT} increases due to additional SiC oxidation during NO annealing. After all, the process condition has to be carefully designed so as to oxidize Si but not SiC.

Here we discuss the cause of the observed defect passivation upon N_2 annealing. The role of N atoms has been extensively discussed in literature; e.g. passivation of carbon defects,^{9,36–39)} suboxide bonds,^{36,38)} and dangling bonds at/near a SiC/SiO₂ interface.⁹⁾ Since we avoided oxidation of SiC, the generation of carbon defects should be suppressed. Passivation of carbon defects are thereby unlikely in our case. In contrast, the passivation of suboxide bonds and/or dangling bonds might be plausible. Indeed, a theoretical study suggested that Si–Si bonds (with various length) in near-interface SiO₂ form antibonding levels near the E_C of SiC, which could be passivated by N atoms.³⁸⁾ Studies based on X-ray photoelectron spectroscopy have indicated Si \equiv N bonds in SiC/SiO₂ structure prepared by NO ^{9,39)} or N_2 ⁴⁰⁾ annealing, suggesting that Si dangling bonds could also be passivated by N atoms.⁹⁾ Hence, we speculate that high-temperature N_2 annealing lets the interface structure to reconstruct and passivates the suboxide bonds and dangling bonds at/near the interface, leading to the significant reduction in D_{IT} [Fig. 3(a)].

Finally, we characterized the reliability of an oxide obtained by proposed method. As shown in Fig. 4, the time-zero-breakdown field of the sample was estimated as 9.8 MV cm^{-1} , only slightly degraded compared to that formed by NO annealing (10.9 MV cm^{-1}). As a result of bi-directional 1 MHz C – V measurement at 200 °C, the hysteresis was negligibly small (<0.1 V) by applying positive (negative) bias stress at $+10$ V (-10 V), where $+10$ V corresponds to an oxide field of about $+3.3 \text{ MV cm}^{-1}$.

In conclusion, we developed an effective method to reduce defects at SiC (0001)/SiO₂ interfaces. The key is to form SiC/SiO₂ structures without oxidizing SiC and to perform high-temperature N_2 annealing afterwards; we deposited Si on SiC and subsequently oxidized the Si at low-temperature (~ 750 °C) to form SiO₂. High-temperature N_2 annealing

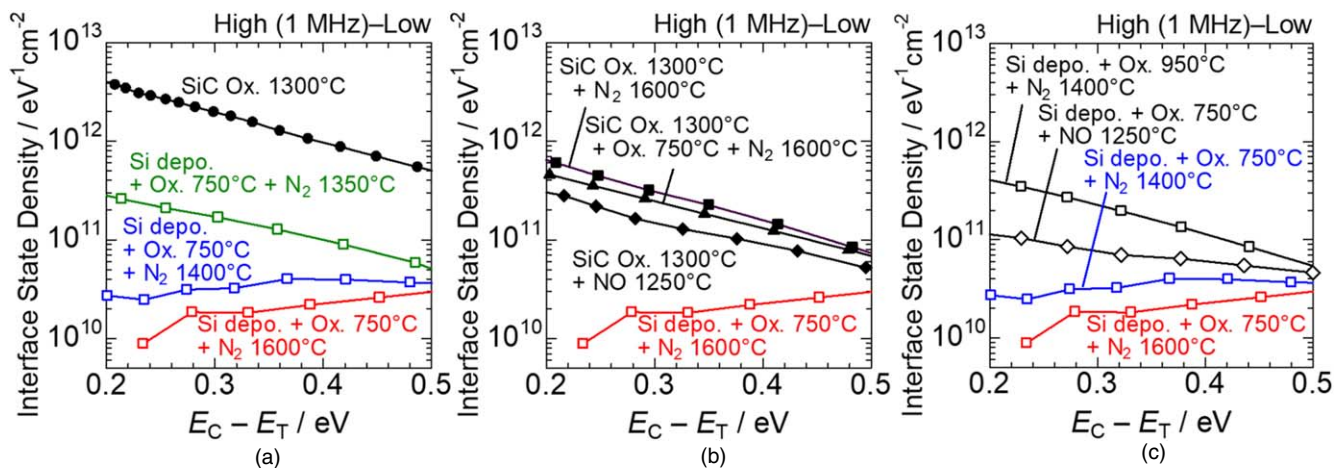


Fig. 3. (Color online) Energy distribution of D_{IT} for SiC MOS structures obtained by a high (1 MHz)–low method;³³⁾ (a) impact of N_2 annealing temperature, (b) comparison with typical methods (NO and N_2 annealings), and (c) impacts of oxidation temperature and post-oxidation treatment. The possible error in the D_{IT} values is estimated as about $\pm (2-3) \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$.

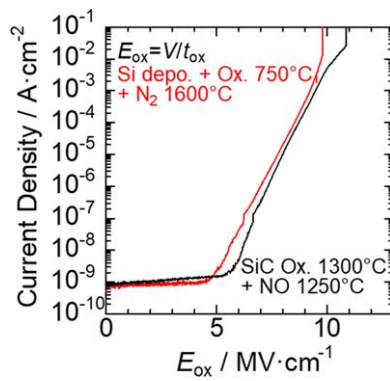


Fig. 4. (Color online) Current density–oxide field characteristics of SiC MOS structures. The oxide field (E_{ox}) was calculated by dividing the applied gate voltage (V) by the equivalent oxide thickness (t_{ox}).

($\sim 1600^\circ\text{C}$) was then performed to let the interface structure to reconstruct and to passivate the suboxide bonds and/or dangling bonds by N atoms. In this way, SiC/SiO₂ interface with substantially low defect density ($\sim 10^{10}\text{ cm}^{-2}\text{ eV}^{-1}$) was formed. The time-zero-breakdown field of the oxide was about 9.8 MV cm^{-1} , only slightly degraded compared to that formed by NO annealing (10.9 MV cm^{-1}).

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