A Feasible Design of Power Packet Dispatching System

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A Feasible Design of Power Packet Dispatching System

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Abstract

The shift from centralized fossil fuel power generation to distributed renewable generation pushes direct current (DC) power systems to use. DC power systems with distributed sources require energy management to balance supply and demand and improve efficiency. Information and communication technologies (ICT) play essential roles in management. ICT-aided energy management systems, consisting of power and communication systems, have challenges keeping the simultaneity of two systems. The lack of simultaneity can induce severe performance deterioration. Among ICT-aided energy management systems, the power packet dispatching system ensures simultaneity with its transmission method.

This dissertation addresses the design of the power packet dispatching system based on the experimental facts. The system is divided into layers as an analogy of reference models in information networks. On each layer, the performance limitations on power packet transmission are examined. The examination ranged from the hardware to the power packet transmission between sources and loads. The contribution of this dissertation is summarized as follows.

Firstly, the performance limitations of power packet transmission due to hardware are examined. A power packet router (router) is a key component in the power packet dispatching system. The developed routers in the preceding studies are reviewed. The review points out that the adopted power packet generation method had a bottleneck on the amounts of power and information per power packet. This dissertation proposes a router without the bottleneck. The proposed router generates a single power packet collaboratively manipulating multiple switches. The collaborative manipulation allows deciding the ratings of power and information per power packet independently. An experimental verification confirmed the power packet transmission with the proposed router. The proposal also shows that each part of power packets can be designed independently.

Secondly, the required information for the power packet transmission is studied. The decentralized control of the power packet dispatching system is proposed and verified.

The control is a vital part of the power system to keep the supply and demand balance. The proposed decentralized control divides the system into subsystems. Each subsystem operates independently to keep sufficient energy in its storage. The on-demand power packet transmission is experimentally verified with a wireless feedback loop. The verification includes a substantial delay due to communication. The bidirectional communication is experimentally verified through a single power line to shorten the delay. Then, the multidirectional power packet transmission is examined. The multidirectional transmission requires a protocol to avoid the collision of power that can induce a short circuit between sources. Three medium access control (MAC) protocols are adopted, referring to information networks. The bidirectional transmission is experimentally verified with one of the MAC protocols. The multidirectional transmission is discussed to estimate the amount of information required to achieve it. The evaluations are conducted on the required amount of information and their effects on power transmission. These results show that the required amount of information depends on the kinds of power packets to distinguish for each connection.

Thirdly, the power transmission between a source and a load is examined. The output characteristics of the system are examined on the cascading connection of routers. Power packets are routed from a source to a load. The connections of routers and transmission timings affect the output. The experimental and simulation studies on power transmission show that a one-to-one connection and an underdamped condition are desirable to guarantee power supply. The power transmission is analyzed following the condition. A cascading connection is analyzed as a chain of one-to-one connections. The analysis reveals that the voltage waveform of the storage is reconstructed from its highest and lowest voltages at a periodic steady state. A linear formula is derived from the analysis. Solving the formula estimates storage voltages from the circuit constants, the source voltage, and the minimum voltage of the load. The validity of the estimation is confirmed through the comparison with the simulation.

Finally, a feasible design of the power packet dispatching system is proposed with the voltage estimation method. The design combines the method and numerical optimization. It provides requirements on the switch, durations of information and power, and storage. Thus, a design of the system can be obtained from the placements of power sources, loads, and routers. The proposed design ensures the power supply at the required voltage.

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Contents

Notations and acronyms

Notations

Notation	Usage	Meaning
$\mathbb{Z}$		Set of integer numbers
$\mathbb{N}$		Set of natural numbers
e		Napier's constant
$\in$	$a \in A$	a is an element of A
$\dfrac{\mathrm{d}}{\mathrm{d}t}$	$\dfrac{\mathrm{d}\boldsymbol{x}}{\mathrm{d}t}$	Time derivative of $\boldsymbol{x}$
$\top$	$\boldsymbol{x}^\top, A^\top$	Transpose of a vector $\boldsymbol{x}$ or a matrix A
$\lfloor\cdot\rfloor$	$\lfloor a \rfloor$	Floor function: $\lfloor a \rfloor = \max\{n \in \mathbb{Z} \,\vert\, n \leq a\}$
$\lceil\cdot\rceil$	$\lceil a \rceil$	Ceil function: $\lceil a \rceil = \min\{n \in \mathbb{Z} \,\vert\, a \leq n\}$

Acronyms

Acronym	Meaning
DC	Direct Current
AC	Alternate Current
ICT	Information and Communication Technology
PWM	Pulse Width Modulation
PDM	Pulse Density Modulation

CPL	Constant Power Load
TDM	Time Division Multiplexing
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
ADC	Analog-Digital Converter
FET	Field-Effect Transistor
JFET	Junction Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
OSI	Open Systems Interconnection
TCP/IP	Transmission Control Protocol/Internet Protocol
MAC	Medium Access Control
CSMA/CD	Carrier Sense Multiple Access/Collision Detection
CW	Contention Window
MLCC	Multi-Layer Ceramic Capacitor
ESR	Equivalent Series Resistance
ZCS	Zero Current Switching

Chapter 1

Introduction

There was a battle on whether the direct current (DC) or alternating current (AC) was better for power distribution. The battle, known as "the battle of currents," was concluded in favor of AC more than 100 years ago [1]. As a result, today's power systems are mainly powered by AC. DC is used in limited applications such as submarine transmission and is not as widely used as AC [2]. One reason is that AC is more compatible with thermal, hydroelectric, and nuclear power sources, which use synchronous generators to extract power from turbines [3]. There are also advantages in power transmission, such as the voltage conversion by transformers [1]. AC is widely accepted with these compatibilities and advantages.

However, the recent global climate change has requested to reduce carbon dioxide emissions from power generation [4]. A shift from centralized thermal power plants to distributed renewable power sources is underway. Here, DC is attracting attention [5–9]. Photovoltaic power generation, an example of renewable energy, outputs DC power. In addition, batteries, which are indispensable for smoothing output fluctuations of renewable energies, are also charged and discharged by DC [10,11]. In addition to the situations on the source side, an increasing number of loads operate on DC with the development of power electronics and semiconductor technologies [3]. As the compatibility of DC with sources and loads has improved, DC is being used in various applications. There is a shift from AC power transmission from centralized power plants to DC power transmission from distributed sources. As a result of the shift, research on energy management in DC electrical systems including distributed sources has been actively conducted.

The objective of energy management includes to maintain the supply and demand balance and the efficient use of energy [12, 13]. To achieve the objective, it is necessary

to monitor the state of charge (SOC) of batteries and to control power flow [5]. One of the characteristics of energy management in a system including distributed sources is that it must respond to fluctuations on a short time scale. Distributed sources do not have large inertia like turbines in thermal power plants [14]. The time scale of their output fluctuation is shorter than that of conventional power plants. Information and communication technology (ICT) plays an important role in managing distributed sources by fast communication and data processing [15, 16]. We discuss two of the challenges in energy management with ICT. One of the challenges is the intricate power flow. It originates from the power distribution system. The increase in the number of so-called power electronics loads, such as constant power loads, is a factor for the complexity. Another challenge is the feasibility of the control. The intended control will be performed when the control and the power system are synchronized [3, 17, 18]. For example, the control that is not physically feasible, such as the control that ignores transient response, is unlikely to achieve the expected performance. As the number of sources and loads increases, the power flow and control will become more complex, so it is important to address these challenges. This research focuses on the concept of packetization of power and addresses them.

This dissertation proposes a design of the power packet dispatching system based on the experimental facts. Among the ICT-aided energy management systems, the power packet dispatching systems have advantages such as the simultaneity of power and information [19–21]. The simultaneity is essential in the energy management. If it does not hold, the system can run into the undesirable operation state [17, 18]. The simultaneity ensures the realization of the desired operation in the actual application. Prof. Toyoda's research group proposed the foremost concept of power packetization in the 1990s [22]. Based on the concept, power packetization by physically integrated information tags has been proposed [19–21]. The physical integration ensures the simultaneity during transmission. In the preceding studies, the prototype of the power packet dispatching system has been developed and verified power packet transmission [19, 23–26]. The design of the systems has been studied with numerical or theoretical approaches. This dissertation tries to show a design based on the experimental results. In the following of this chapter, the ICT-aided energy management is described (Sec. 1.1). In Sec. 1.2, the foremost concept of power packet dispatching system is presented. Sec. 1.2.1 introduces the preceding studies on the power packet dispatching system. The power packet dispatching system studied

in this dissertation is explained in Sec. 1.2.2. The outline of the following chapters are given in Sec. 1.3.

1.1 ICT-aided energy management

ICT has been developed with semiconductor technologies [13–15, 27, 28]. With the development of ICT, energy management using ICT has attracted much attention, and various proposals have been made. The development in semiconductor technology provides high data processing capabilities at a low cost. Microcomputers and field-programmable gate arrays (FPGA) are examples. ICT provides high-speed and large-capacity communication at a low cost with them. Layering based on reference models makes it easy to configure communication networks [29]. The well-known reference models are the Open Systems Interconnection (OSI) model and Transmission Control Protocol/Internet Protocol (TCP/IP). The OSI model has seven layers, from the physical to the application layers. Each layer in the model serves the higher layer and is served by the lower layer. The hierarchy simplifies the design and implementation of the network. Therefore, ICT-aided energy management systems can utilize the computational devices and high-speed communication medium at a low cost with small labor.

In the commercial power grid, the voltage, frequency, and phase in the system are collected with ICT [30]. In addition to the conventional control mechanisms like droop control, collected data is utilized to improve efficiency [6, 31]. In DC systems with distributed sources, ICT plays an essential role in keeping the system stable than in the conventional power grid [15, 32]. It owes to the fast fluctuations of distributed sources and the difference between AC and DC.

Here we discuss two of the challenges in ICT-aided energy management. In DC systems, voltage gradient and impedance decide the current flow. One of the challenges is that they get complex with distributed sources and power electronics loads. In the past, power was supplied from the centralized power source to the load in a single direction. However, distributed sources cause multidirectional power flow in the system [10, 13–15, 27]. Power is a product of voltage and current. Multidirectional power flow affects both voltage and current. Power electronics loads have time-variant impedances. The constant current load, as its name suggests, pulls out the stable current from the system. Its equivalent impedance depends on its voltage. The increase in the number of power electronics

loads further complicates the power flow. The increase is confirmed in applications like an increasing number of sensors in vehicles. Another challenge is the feasibility of the control [33]. The intended control will be performed when the control and the power system are synchronized. For example, the control that is not physically feasible, such as the control that ignores transient response, is unlikely to achieve the expected performance [17, 18]. Simplifying power flow and synchronization of cyber and physical layers are necessary for ICT-aided energy management to address these challenges.

1.2 Power packet dispatching system

The concept of power packet was proposed by Prof. Toyoda's group in the 1990s [22, 34]. They tried to ease the management and delivery of electric energy in the commercial power grid. The power in the grid is virtually tied with its related information, such as the source and price. Their concept implements batteries and superconducting magnetic energy storage as the storage devices into the grid. They keep the energy balance and control the power flow. The accompanied information networks autonomously manage the power. Unfortunately, their concept was difficult to realize due to the inadequately developed batteries, power electronics, and communication technologies. Inspired by their concept, several research groups have independently proposed power packetization and its management since the late 2000s [19–21, 35].

1.2.1 Research related to power packetization

Studies based on the power packetization concept are roughly divided into two approaches. The first one applies the methods and theories in information networks to the power packet dispatching systems [21, 36–39]. The other approach has developed prototype hardware and experimentally verified the power packet transmission [19, 24, 26, 40]. These approaches largely owe to the development of ICT and wide band gap semiconductor technologies. This dissertation tries to bridge the gap between these approaches from the latter approach.

Erol Gelenbe and his research group proposed Energy Packet Networks (EPN) [21, 36]. They employed the first approach. They applied a queuing theory in the information networks for EPN and addressed the optimal distributions of power and the workload for the computers [37]. Ma, *et al.* also stood on the first approach and formulated the

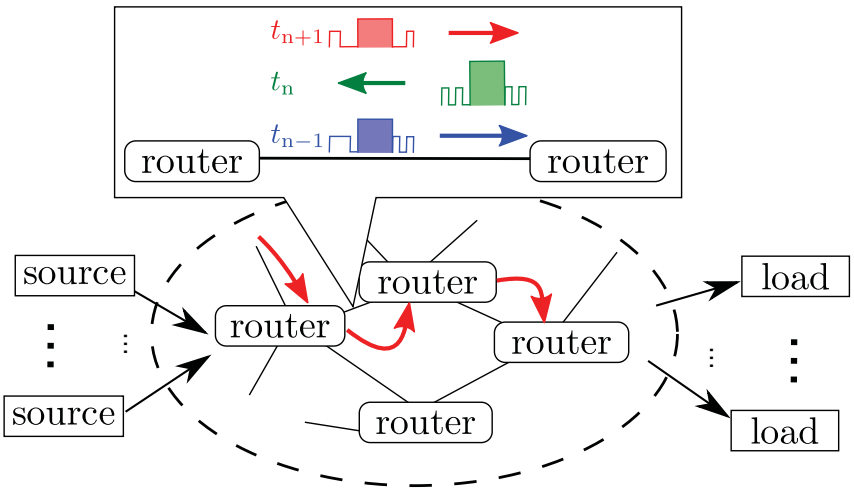


Figure 1.1: Concept of power packet dispatching network.

optimal power packet dispatching problem as a matching problem between sources and loads [39]. They used a heuristic algorithm and verified the optimal matching by the simulation. Studies on the first approach have handled the network with multiple routers or general networks by assuming that a unit power packet transmits a specific amount of energy [21, 39]. The assumption makes the power packet transmission similar to an IP packet. It follows the target of the foremost power packetization concept.

The author's research group has stood on the latter approach. The hardware that realizes power packet transmission has been developed [19, 24, 26, 40]. It will be explained in Sec. 1.2. Y. Okabe's research group experimentally verified the virtual integration of power and information with developed power packet routers [41]. They used resonance circuits for power distribution and an accompanied wired network for communication. These studies have verified power packet transmission by the experiment. Stephan S. Eaves and his company proposed and implemented "Energy Packet" (EP) for DC power distribution [42]. They focused on the safety feature of TDM power transmission. The pulse length and voltage of an EP are designed not to kill a person by electric shock. They use the dead time to communicate and monitor the power line. If any faults are detected, the power transmission is immediately stopped. The safety of the power transmission system by EP is ensured by the mechanisms.

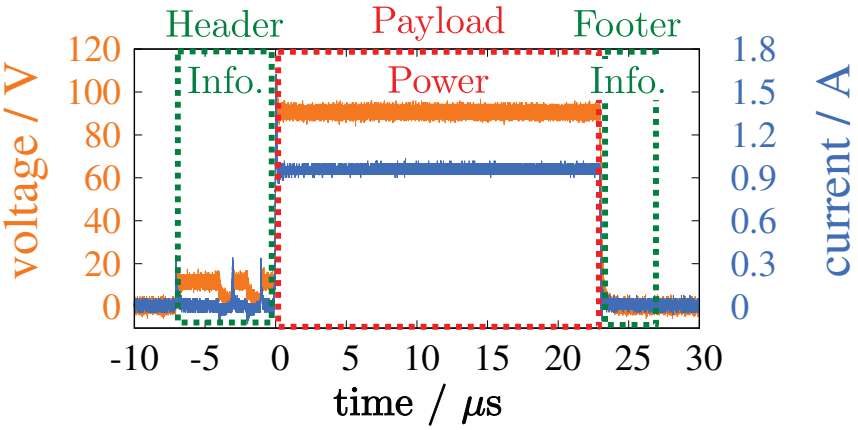


Figure 1.2: Example waveforms of unit power packet.

1.2.2 Physically integrated power packet and its dispatching system

Figure 1.1 shows the concept of a power packet dispatching system [19]. Figure 1.2 depicts example waveforms of a unit power packet. The system consists of multiple sources, loads, and power packet routers (routers). The networked structure provides robustness against hardware problems such as a ground fault and short circuits [43]. The routers provide power packet transmission in a time-division multiplexing (TDM) scheme [24]. TDM enables power with multiple voltages to share the same power lines [23, 25]. In conventional power systems, many sources and loads are connected to the same power line called the bus. The typical rating voltages of the bus include 400 V and 24 V [8]. All of the sources and loads connected to it have to cooperate to keep the voltage and quality [6,33]. TDM can minimize the interference between sources and loads. The bus transmission requests some sources and loads to implement power converters to send or receive power. In contrast, TDM can deliver power with multiple voltages. It allows sources and loads to omit their power converters whose purpose is to send or receive power at a specific voltage. Sharing of power converters is another possibility. The sharing is expected to flatten the output of the shared converter compared to the individual converters. It is called the smoothing effect [44, 45]. The effect is studied in solar power plants and power grids [44, 45]. They show that connecting numbers of independent sources or loads decreases the fluctuation as a whole. The fluctuation of the demand from loads will negate each other. Thereby the output of the shared converter will not fluctuate as much as a demand from a load does. The stable output will improve

the efficiency of the shared converter since a converter has its best output in terms of efficiency [46].

Generally, the disadvantage of TDM is the dead time and switching losses. The power packet dispatching network utilizes the dead time for communication. Detecting faults is another possibility [42]. TDM also limits the amount of energy transmitted in a single pulse. Limiting it provides safety against electric shock. Thus, dead time is not always the disadvantage in the power packet dispatching system. The switching losses are inevitable. However, the improvement in the efficiency by such as the sharing of converters is expected to compensate for it. The bit configuration of the power packet also contributes to decreasing the switching losses [19].

1.2.3 Areas of study

Among the studies on power packet dispatching systems, this work focuses on the control of the sub-ms power transmission. It is achieved high speed switching of wide-gap semiconductors [47]. In the control, we have to consider the transient response of the system. The assumption of the fixed amount of energy does not hold [21, 36–39]. As ratings of power, we handle less than 1 kW. It is because the power packet transmission has been verified 1.5 kW in a preceding study [48]. Possible applications include electric vehicles and in-home power distribution.

The capacitor is selected as the storage device from the duration of transmission and the rating power. The charge and discharge to the capacitor do not require converters. Converters can control the current during transmission, but their conversion losses decrease the efficiency of the system. They also experience transient states in start-ups. Their impacts on the sub-ms power transmission will not be negligible. Thus, we assume no converters in the network except for the interface with the source and the load.

We also assume that the load is a resistor. To hold the assumption in actual applications, there is required an appropriate interface between the system and the load [40, 49]. Power factor correction (PFC) converter is a candidate of the interface. In fact, when the load is a motor, “the router for motor drive” has been developed and experimentally verified [40]. The intermittent power supply by power packets is smoothed with the storage connected to the interface or load. Therefore the power flow depends on the storage voltages and the load during the power packet transmission. If the effect of the load is negligible during the transmission, the storage voltages decide the power flow.

1.3 Outline of the dissertation

This dissertation addresses the design of the power packet dispatching based on the experimental results. The design is based on the following assumptions.

1. Sources, loads, allocations of routers are given

2. Power lines are short enough to be modeled by lumped constants

Also, we do not deeply examine the control and performance since the best control and performance of the network are not known. Following the OSI model, a protocol hierarchy of the information networks, this dissertation is arranged as follows. Chapter 2 examines the hardware. The router is improved, and its limitation on the power packet transmission is discussed. Chapters 3 and 4 examine the communication and control of the power packet transmission between two routers. The studies on the network and the feasible design are in Chapters 5 and 6.

Chapter 2 develops a router and examines the hardware limitation of the power packet generation. A router is a key component in the physical layer of the power packet dispatching system. The preceding studies used a single switch to generate a unit of power packet. The generation method of power packets was the bottleneck to enhance the performance of power packet transmission. The performance depends on the amount of power and information per power packet. This chapter focuses on the coexistence of power and information. A power packet generation method is proposed to extend the amount. A router with multiple types of switches is developed to verify the method. Its operation is experimentally verified. The verification shows that the router achieves both 1Mbps data transmission and 100V power transmission. It proves that the performance of power packet transmission largely depends on the ratings of the switches.

Chapter 3 describes the decentralized control of the power packet dispatching network. As an electric energy network, the control is necessary to deliver sufficient energy to the load. The decentralized control is expected to enhance the advantages of the network. Flexibility and robustness against faults are examples. The length of the signal is expected to be shorter under the decentralized control than the centralized control. A decentralized control method of the power packet dispatching network is proposed. Its operation is described, compared with the centralized operation. The experimental verification is performed with the wireless feedback. The simulation follows the experiment. Then, the decentralized control is verified with wired feedback to minimize the feedback delay. The

wired feedback is realized with the inverse-parallel connection of unidirectional switches. The inverse-parallel connection blocks the unintentional backflow current without control. On-demand power packet transmission is examined with the switches.

Chapter 4 examines the bidirectional power packet transmission. The bidirectional power packet transmission enables control through a single pair of power lines. It allows the power flow from the load. Chapter 3 focuses on the bidirectional communication with the inverse-parallel connection of unidirectional switches. The connection inherits the voltage drop by the diode. The bidirectional power packet transmission is achieved by the back-to-back connection of MOSFETs. It requires a collision avoidance method. A MAC protocol is proposed for the power packet transmission based on the collision-free MAC protocol. The experimental verification shows that the protocol prevents the collision of power. The bidirectional power packet transmission is performed on a single pair of power lines. Then, the multi-directional power packet transmission on the bus line is studied. The results show that the required amount of signal depends on the kinds of power packets to distinguish and the MAC protocol on each connection.

Chapter 5 investigates the dependency of the output on the connections of routers. The circuit switching performs the power packet routing. The experimental results in Chapter 4 reveal that the connection timings affect the output of the network. Focusing on the cascaded connection of the routers, we examine the dependency of the output on the connection. The simulation and experiment confirm that the output follows the characteristics of the buck converter operating in DCM. They show that the circuit in the power packet transmission network is regarded as a series of RLC filters. The simulation results suggest that the capacitors in the network are designed as a part of an RLC filter. They also suggests that the best condition of the power packet transmission seems difficult to find.

Chapter 6 analyzes the power packet transmission from a source to a load. Chapter 5 suggests that the circuits in the network are analyzed as an RLC filter. This chapter analyzes the network as a series of RLC filters assuming the hop-by-hop power packet transmission. The hop-by-hop transmission intends that a router gets connected with one neighboring router at a time. Firstly, the payload transmission is analyzed by a step input. The step response of an RLC filter is roughly classified into over and under damping. With the underdamped condition, the zero-current turn-off is experimentally verified. The zero-current turn-off reduces the surge voltage at the end of the payload.

Then, the relationships among storage voltages before and after payload transmission are analyzed. The analysis gives the linear formula of storage voltages. Solving the formula with circuit constants, source voltage, and the minimum voltage of the load, the storage voltages are estimated. Finally, a feasible design of the power packet dispatching system is proposed with the voltage estimation method.

Chapter 2

Power packet router and its limitation on power packet transmission

In the OSI model, the physical layer provides standards of hardware and transmission medium [29]. In this chapter, we study hardware in the physical layer by extension. The power packet dispatching network predominantly consists of routers and transmission lines. This chapter examines the router and its limitation on the power packet transmission. Related to the hardware, the power transmission properties of the line were examined in [50, 51]. These studies pointed out that the gaussian voltage waveform suits long-distance transmission [50, 51]. The definition of long-distance was that the distributed-element model was necessary to analyze the power transmission. If the model is not necessary, the rectangle and gaussian voltage waveforms do not have much difference in the power transmission efficiency. Based on the results, our project has employed the rectangle voltage waveform for the payload transmission.

The router is the key component in the power packet dispatching network. Its store and forward operations achieve the power packet transmission keeping their simultaneity [24]. A router is proposed to extend the performance of power packet transmission in this chapter. Routers in the preceding studies are classified by their switches. Firstly, we review the configurations and operations of the uni and bidirectional routers. Second, based on their performance, there is pointed out a bottleneck of the performance is pointed out. A router is then proposed to break the bottleneck, and its operation is experimentally verified. Its operation proves that the combination of the switches can extend the amount of power and information of a unit power packet with keeping their simultaneity. It also

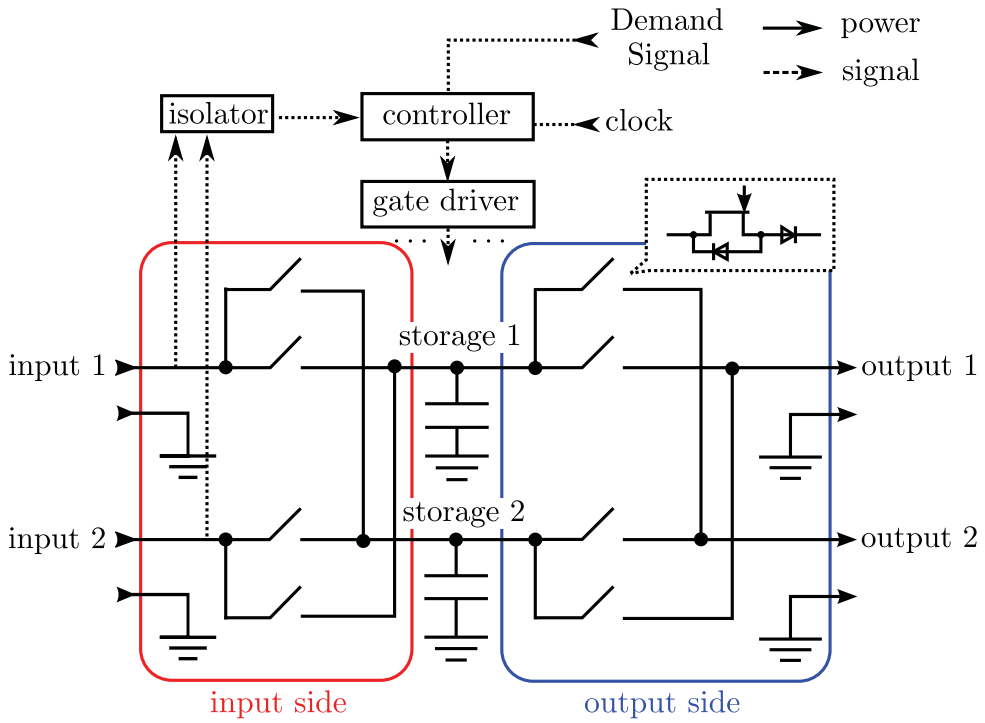


Figure 2.1: Schematic diagram of unidirectional router [24].

implies that we can design the amounts of power and information independently by their corresponding switches.

2.1 Review of developed routers

We review the routers developed in earlier researches [24, 26]. Their circuit configurations and operations are explained.

2.1.1 Unidirectional router

Figure 2.1 shows the schematic of an unidirectional router proposed in [24]. The router consists of the controller, isolators, and switching circuit. It implements Silicon Carbide (SiC) Junction Field-Effect Transistor (JFET) and Silicon (Si) diode as a unidirectional switch. Unidirectional switches block undesirable inputs without control. The SiC JFET was depression type, so the signal from the controller is inverted [19,52]. They used JFETs since SiC JFETs outperformed SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) at that time. The isolator consists of a voltage divider circuit and a photocoupler. The controller is an FPGA board. The switching circuit is divided into the input

and output sides. Storage devices are implemented between them. The device is selected to hold a sufficient amount of energy. We implement a capacitor as the storage. The numbers of input, output, and storage ports are not restricted. The number of switches is given by the multiplications of the number of ports. As a variation of the unidirectional router, a router with four input, four output, and four storage ports [53] was developed. It implemented 32 pairs of GaN FETs (EPC2014) and Si diodes as unidirectional switches and achieved the operation frequency of 10 MHz.

The operation of the router is explained. A router (transmitter) starts sending a power packet to the neighboring router (receiver) by generating the header signal. The signal is delivered to the controller in the receiver and processed. The signal "1" is generated by turning on the switch, and "0" is off. The power line voltage is pulled down by the resistors of the isolators. According to the information, the receiver drives a designated switch to receive the following payload. The transmitter also turns on the switch. The payload is delivered to the storage in the receiver. After the duration of the payload, the transmitter starts to send the footer signal. When the receiver reads the footer signal, it turns off the switch. The sequence above achieves the store and forward operation of power packets.

2.1.2 Bidirectional router

In order to achieve bidirectional power flow in the network, a router with bidirectional switches has been proposed [26, 54]. Some configurations are available to make bidirectional switches. One is the inverse-parallel connection of unidirectional switches [55]. Another is the back-to-back connection of MOSFETs [26,54]. The inverse-parallel connection blocks unintentional backflow current during sending. However, it requires more components compared to the back-to-back connection. The voltage dropdown due to diodes is another disadvantage of the inverse-parallel connection. The back-to-back connection can avoid it. The circuit configuration and operation of the inverse-parallel connection are described in Sec. 3.4

Yoshida, *et al.* [26] implemented a pair of back-to-back SiC MOSFETs as a bidirectional switch. The bidirectional router verified a bidirectional power flow in the router and the power regeneration from a DC motor. The disadvantage of the back-to-back switch is that the transmitter and receiver have to share the payload length ahead of its transmission [26, 54]. When a back-to-back switch is ON, and the current is zero, both

sides of the switch have the same voltage. If the receiver router does not know the payload length beforehand, the power line voltage after the payload transmission is the same as the storage voltage. In that case, the receiver can not identify the end of the payload. The ways to avoid it are to decide the length to a fixed value [26, 54] or to include the information of the length in the header signal. We adopt both of the methods in this dissertation depending on the setup.

2.1.3 Trade-off relation in power packet generation

A power packet is required to send both power and information. The amounts of power and information per power packet decide the performance of the power packet transmission. The performance of the transmission largely depends on the routers. Routers in Sec. 2.1.1 and 2.1.2 used a single switch to generate a unit of power packet. The generation method ensures the simultaneity of power and information by the switch. It is a reliable way to ensure the simultaneity. On the other hand, it inherits the performance trade-off. The maximum switching frequency decreases as the rating power increases since the switching is performed by the charging of the input capacitance and a high-power switch tends to have a large input capacitance. The router in [53] achieved the 10 MHz operation with the 12 V payload. When the payload voltage was 80 V in [40], the data transmission was performed by 20 kHz signals. As these results show, the extension of both amounts is difficult with the generation method.

2.2 Router with power and signal switches for a single power packet

Focusing on the receiving of power packets, we find that the power and information are separately stored in the router. It means that the simultaneity should be ensured only during the transmission. Based on it, we propose a router without the trade-off in the preceding researches. The power and information require different properties of the switch. The power is the product of voltage and current. The maximum ratings of the switch limit the amount of transmittable power [1]. Information is transmitted as a sequence of rectangle voltage waveforms. The switching frequency decides the amount of information. As described in Sec. 2.1.1, the rating power of the switch has relationships

[1] In reality, the amount of power per power packet depends on the voltage gradient of the circuit.

with its switching frequency. The switch with a high absolute maximum voltage tends to have a low switching frequency. It implies that a switch with a high absolute maximum voltage suits the payload and a high switching frequency the signals.

We propose a router that aims to increase the amount of power and information during transmission with multiple types of switches. The proposed router combines multiple switches to generate a power packet for improving performance. It is aimed at achieving 100 V power and 1 Mbps data transmission for future applications. We ensure the simultaneity of power and information by their physical integration and the operation of the router. The router collaboratively manipulates the switches to generate a single power packet. We employed bi and unidirectional switches for power and for signal, respectively, adopting both advantages. Unidirectional switches use the same power source for the router to generate the header and footer. The router must have the source. Its voltage is low enough to feed the controller. Low voltage power sources are appropriate to generate signals from the viewpoint of data rate. However, the back-flow current to the source should be prohibited. Unidirectional switches suit to avoid it. The back-to-back bidirectional switches generate the payload. They realize multidirectional power transmission. The collaborative manipulation of these switches ensures the simultaneity of power and information. The operation of the switches is controlled by an FPGA board. Its operation frequency is high enough to finish the calculation in transmitting one bit. The fast calculation and the transmission through a single power line ensure the simultaneity.

Figure 2.2 shows the schematic diagram of the proposed bidirectional router. The router consists of a controller, gate drivers, storages, and a switching circuit. The controller is an FPGA board (Avnet, MiniZed), which contains Zynq SoC chip (Xilinx, XC7Z007S-1CLG225C). The gate driver consists of a digital isolator (Silicon Labs, Si8610BC) and MOSFETs (Rohm, US6M1). The storage device is selected to meet the power rating of the router. In the router, capacitors are employed as the storage. Storages are connected between two O/I ports (e.g., between port11 O/I and port21 O/I). The router use *clock in* and *clock out* to synchronize with other routers for reading signals. The rating frequency of the clock is set at 1 MHz. The clock synchronization can be achieved by the additional signal before the header of the power packet [56].

Figures 2.3 to 2.5 show the switching circuit and units in it. Figure 2.3 shows the schematic diagram of the switching circuit. The bidirectional switches consist of the back-to-back connections of SiC MOSFETs (Rohm, SCT3022AL). We selected their rating

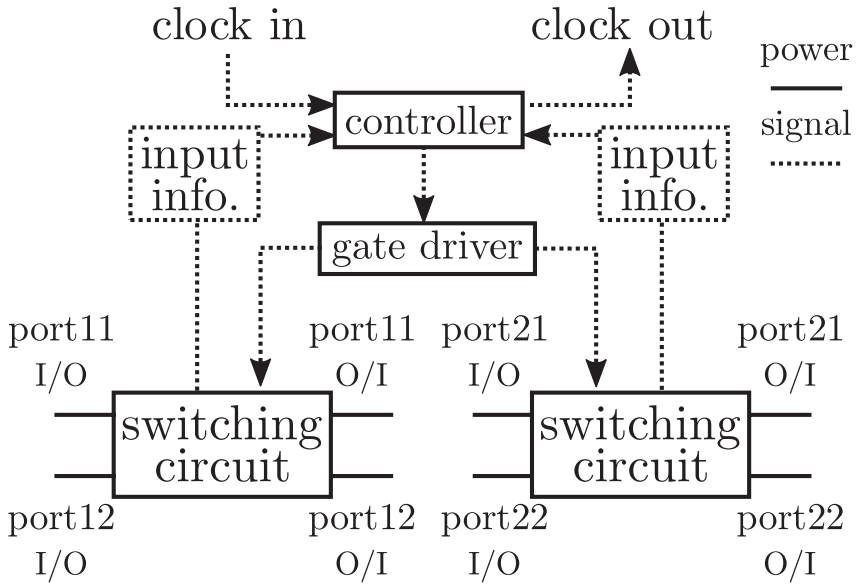


Figure 2.2: Schematic diagram of proposed bidirectional power packet router ©2020 IEEE.

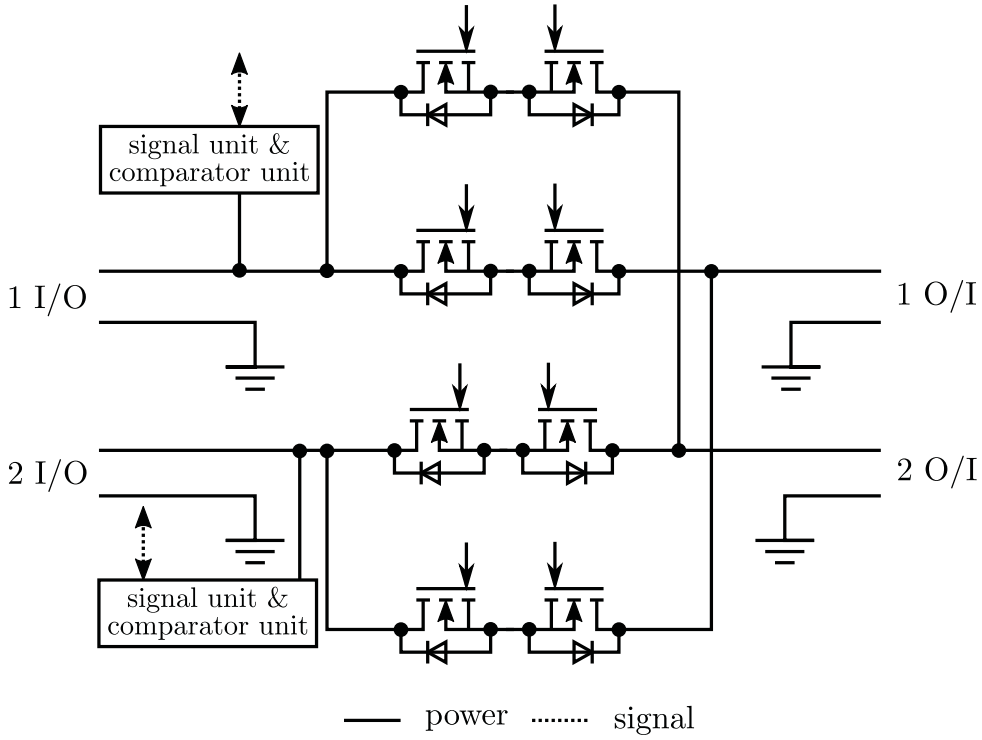


Figure 2.3: Switching circuit of proposed router. MOSFETs are SiC MOSFETs (SCT3022AL) ©2020 IEEE.

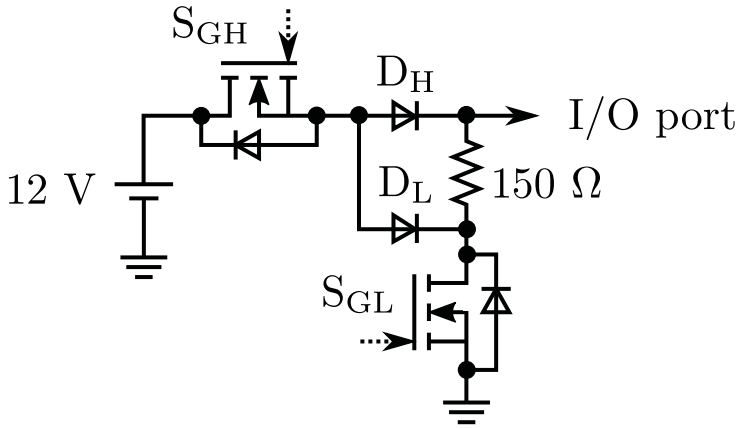


Figure 2.4: Schematic diagram of signal unit. FETs are EPC2010 and diodes are MBRS3201T3G. 12.0 V source is the same as the source of the router ©2020 IEEE.

Table 2.1: Absolute maximum ratings of switches [57–59].

SCT3022AL	Drain - Source voltage	650 V
	Continuous drain current (25 °C)	93 A
	Pulsed drain current	232 A
EPC2010	Drain - Source voltage	200 V
	Continuous drain current	12 A
	Pulsed drain current	60 A
MBRS3201T3G	Peak repetitive reverse voltage	200 V
	Average rectified forward current	3 A

voltages to be sufficiently higher than 100 V. Their ratings are shown in Tab. 2.1. This circuit has the same topology as the bidirectional power packet router proposed in the preceding research [26]. Power from an I/O (O/I) port can be transferred to any O/I (I/O) ports through one switch and the other I/O (O/I) ports through two switches, respectively.

Figure 2.4 shows the schematic diagram of the signal unit. The unidirectional switches consist of the GaN FETs (Efficient Power Conversion, EPC2010) and Si diode (ON Semiconductor, MBRS3201T3G). We chose the rating voltage of S_{GL} and diodes (D_H and D_L) to be larger than 100 V. Because they have to withstand the payload voltage. Their ratings are shown in Tab. 2.1. S_{GH} generates the "1" of the header and footer using the 12.0 V power source. The 12.0 V power source is the same power source as the router. S_{GL} sends the bit of '0. It lowers the source voltage of S_{GH} through D_L and the power line voltage through 150 Ω resistor. D_H prevents the reverse current to the voltage source. D_L

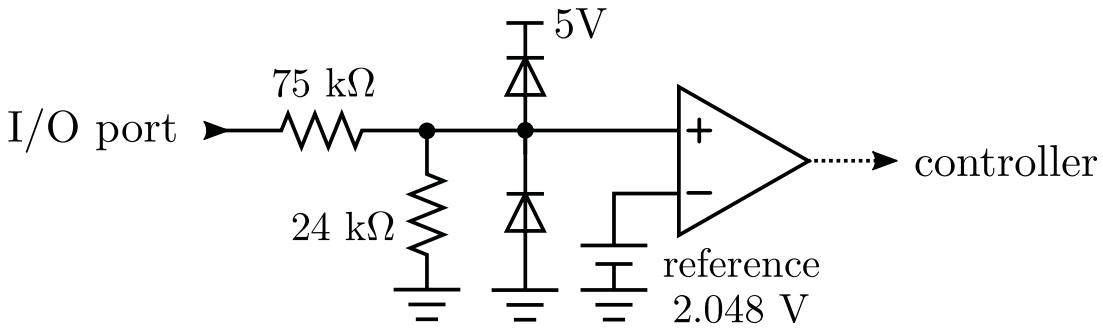


Figure 2.5: Schematic diagram of comparator unit. Comparator is LT1713. 5.0 V source is the same as the source of the router ©2020 IEEE.

also prevents it and helps decrease the source voltage of S_{GH}. This topology contributes to both the high-speed signal generation [60] and the protection of S_{GL} from the surge current on the power line. The dead time between S_{GH} and S_{GL} is set at 50 ns. In order to simplify the dead time control, we chose the same GaN FETs to S_{GH} as S_{GL}.

Figure 2.5 shows the schematic diagram of the comparator unit. The comparator unit consists of voltage divider resistors, voltage-clamp diodes (Toshiba, 1SS226), a reference voltage source (Linear Technology, LT6654-2.048), a comparator (Linear Technology, LT1713), an isolator (Silicon Lab, Si8640BC), and a bus transceiver (Texas Instruments, SN74LVC4245A). The threshold voltage of the comparator unit is set at 8.5 V. The router reads the signal of "1" when the power line voltage exceeds the threshold. The diodes protect the comparator from overvoltage. The transmission delay of the comparator unit is estimated at around 18 ns in the worst case. It is short enough to read the signal in transmitting one bit.

2.3 Experimental verification on power packet transmission

The operation of the proposed router is experimentally verified. The routing of power packets is achieved by store and forward operations. These operations are verified in an experimental system.

2.3.1 Experimental setup

Figure 2.6 shows the experimental circuit with proposed routers. This circuit consists of one source, two routers, and a load of 430 Ω. Dotted arrows show the connections to

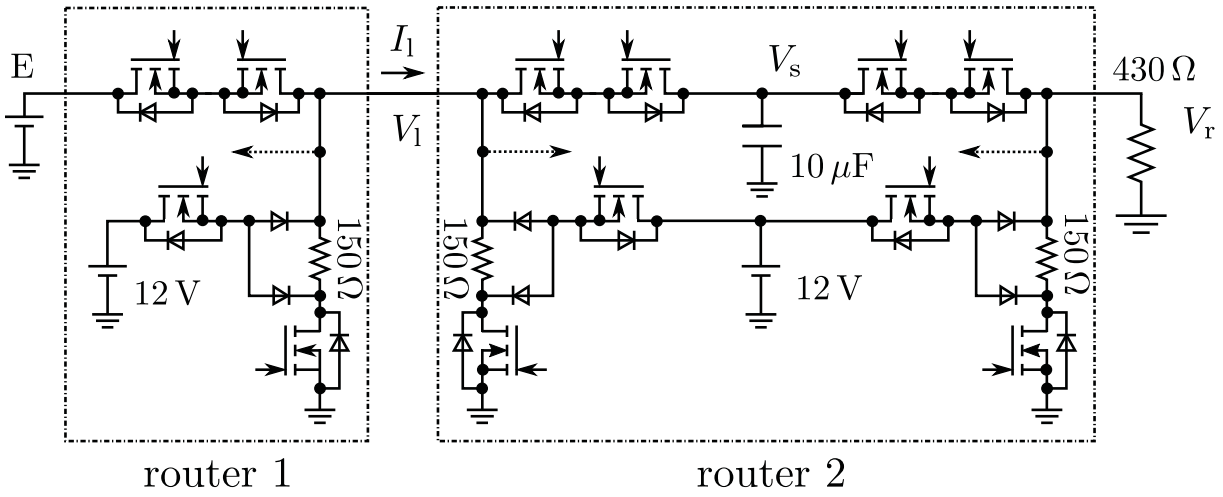


Figure 2.6: Experimental circuit configuration with one power source and one load. The source voltage E is set at 100.0 V. Dotted arrows show the connections to the comparator units ©2020 IEEE.

Table 2.2: Bit assignment of power packet.

	Header	Payload	Footer
Length	7 bits	24 bits	3 bits
Bit	"1110101"	"111...11"	"000"

the comparator unit. In this circuit, router 1 transmits power packets. Then, router 2 receives them and transmits the same power packets to the load. The source voltage E is set at 100.0 V. Table 2.2 shows the bit assignment of power packets. The header sends the start of a power packet and its destination. The experimental circuit has only one load, so router 2 can identify the destination on receiving a power packet. The footer does not transmit information. Its duration corresponds to the time to decrease the power line voltage through S_{GL}. The routers send power packets continuously. The duration was set at 1 bit between router 1 starts sending a power packet and router 2 starts. The clock was set at 1.0 MHz. The routers are synchronized through the clock line with respect to power packet transmission. We measured the voltage and current of the power line between routers (V_l, I_l) and the voltages of the storage (V_s) and the load (V_r). V_s was measured with the DC voltage offset of 80.0 V to reduce the effects of noise.

Practically, a port of a router can be connected to not only one port. Such situations are called multiple access in information networks. The problems which arise from the multiple access are the congestion and the collision of packets. They can make a

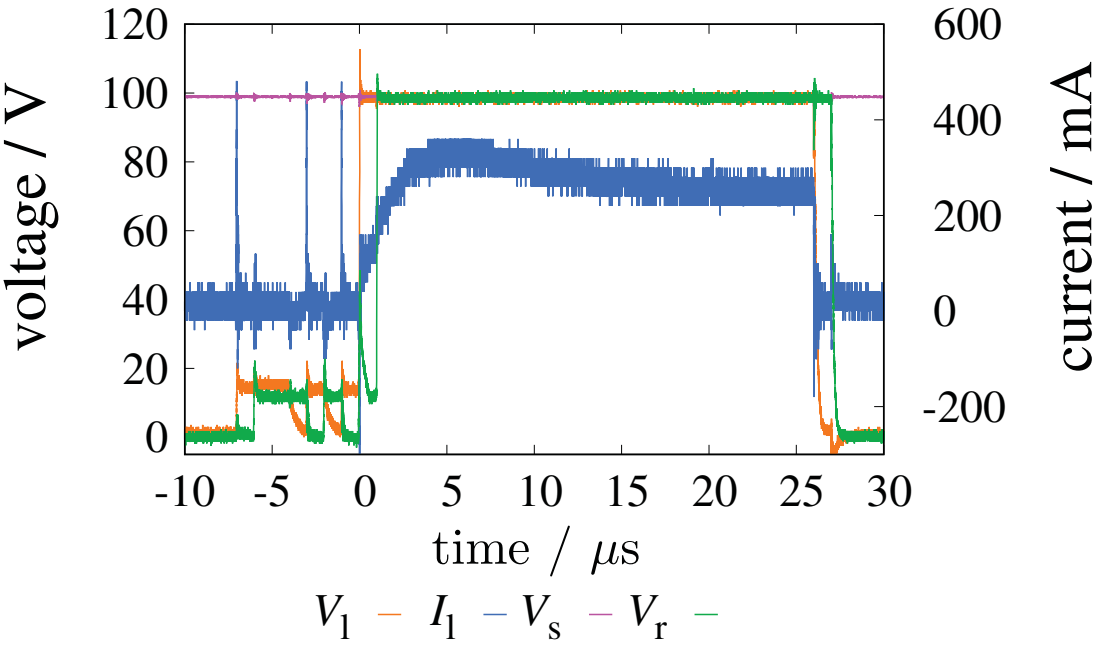


Figure 2.7: Example of experimental waveforms. V_l and I_l show the voltage and the current waveforms of the power line between the routers. V_s and V_r show the voltage waveforms of the storage and the load, respectively. V_s was measured with DC offset of 80 V to reduce the effects of noise ©2020 IEEE.

chance for a source or a storage to have an unintentional connection with other sources or storages in power packet dispatching networks. They can be solved in similar ways in information networks [23,55,61]. For instance, N. Fujii *et al.* [23] demonstrated the power packet transmission on a system with a branch on the wire. These solutions request some additional rules to the signals and do not need any changes to the hardware. Thus, the experimental setup meets the necessary condition to verify the operation of the router. This chapter focuses on the power packet generation method and hardware of the router to achieve it. The experimental setup here meets the condition to verify its operation. The congestion is discussed in Chapter 4.

2.3.2 Experimental results

Figure 2.7 shows examples of experimental voltage and current waveforms. First, the operations of the proposed router are confirmed. V_l shows the logical value of the power packet sent to the router. The header signal starts at -7 μs. The logical value is confirmed as same as the settings shown in Tab. 2.2. This result is also shown in V_r. Therefore, we can verify that the routers send the same power packets in the duration

of 1 bit. I_l shows that the current starts flowing at $0\,\mu s$ when the payload starts, except the surge current. This result indicates that router 2 reads the header signal of the power packet and receives the payload. These results verify that the proposed router achieves routing of power packets, and the simultaneity of power and information is kept during the transmission based on different aims of switches.

Then, we can confirm the values of the measured waveforms. I_l converges to around 230 mA at $25\,\mu$s. It is caused by the source voltage to the load resistance. V_s is 98.8 V on average. Here, we see the voltage drop across the power switch. The voltage drop limits the number of hops during routing. In order to decrease the voltage fluctuation due to the switching, we calculated the average in 10 to $20\,\mu$s. The averaged voltage difference between V_s and V_r is 0.31 V. Using unidirectional switches, the voltage drop between the storage and the router output is around 0.6 V when the current is 90 mA due to the diode [23]. It clearly shows that the voltage drop with the switches is less than the previous studies.

There appears the surge current at -7, -3, and -1 μs. They are caused by the switching of GaN FETs. They do not affect the operation of the proposed router in this experiment. Needless to say, they should be suppressed from the viewpoint of EMC and protecting the router hardware. The expected countermeasures include the waveform shaping of the power packet [62] and the soft switching technique [63].

The combination of switches used in the experiment is not optimized for generating power packets on the target voltage and data rate. The prototype router should be improved. The appropriate circuit design can improve the ratings of the routers. Also, developed functions of power packet routers should be implemented, such as energy harvesting [64] and modulation for security [65].

2.4 Summary

In this chapter, a power packet router is newly proposed to extend the performance of the power packet transmission. The developed router is firstly reviewed. The advantages and disadvantages of the unidirectional and bidirectional routers are discussed. They ensured the simultaneity of power and information by generating the whole power packet with a single switch. The generation method is a reliable way of guaranteeing the simultaneity but difficult to extend the amounts of power and information per power packet.

The proposed router ensures the simultaneity of power and information by introducing the power packet generation method with the switches for power and signal. The topology accepts a combination of switches with different ratings to meet the target voltage and data rate. Thereby the proposed router enhances the amount of power and information per power packet. The operation of the router was experimentally verified. The proposed router achieved 100 V power transmission and 1 Mbps data transmission.

This router verifies that the simultaneity of power and information is kept by its generation method when different types of switches are employed. The experimental results imply that we can independently design the capacities of power and information per power packet. In the rest of the dissertation, we examine the information and power part of the power packet separately.

Chapter 3

Decentralized control of power packet dispatching system

This chapter discusses the control of the power packet dispatching network in this chapter. As a power distribution system, the power packet dispatching system has to keep the supply and demand balance between sources and loads. The control is necessary for the objective. The control in the network is roughly divided into centralized and decentralized control. The preceding studies on power packet dispatching networks have been assumed the centralized control [19]. It requests to collect all data in the network, including the voltage or demand of loads and power distribution in the network. This dissertation proposes a decentralized control method. The decentralized control is expected in the robustness and shortening of the bit length. The flexibility of the system is another advantage. The experimental verification is performed with wireless communication. Then, we verify the bidirectional communication as a means of feedback control to improve the feedback delay.

3.1 Decentralized control in power packet dispatching network

To keep the supply and demand balance, The system responds to the demands of loads with the control. The amount of power required from a load depends on its state and environment. The output power of a source, too, fluctuates with time. In order to take balance between the output from sources and demands from the loads, feedback control is necessary. In conventional DC power systems, the power flows continuously depending on the voltage gradient and impedance. It is governed by Kirchhoff's law and

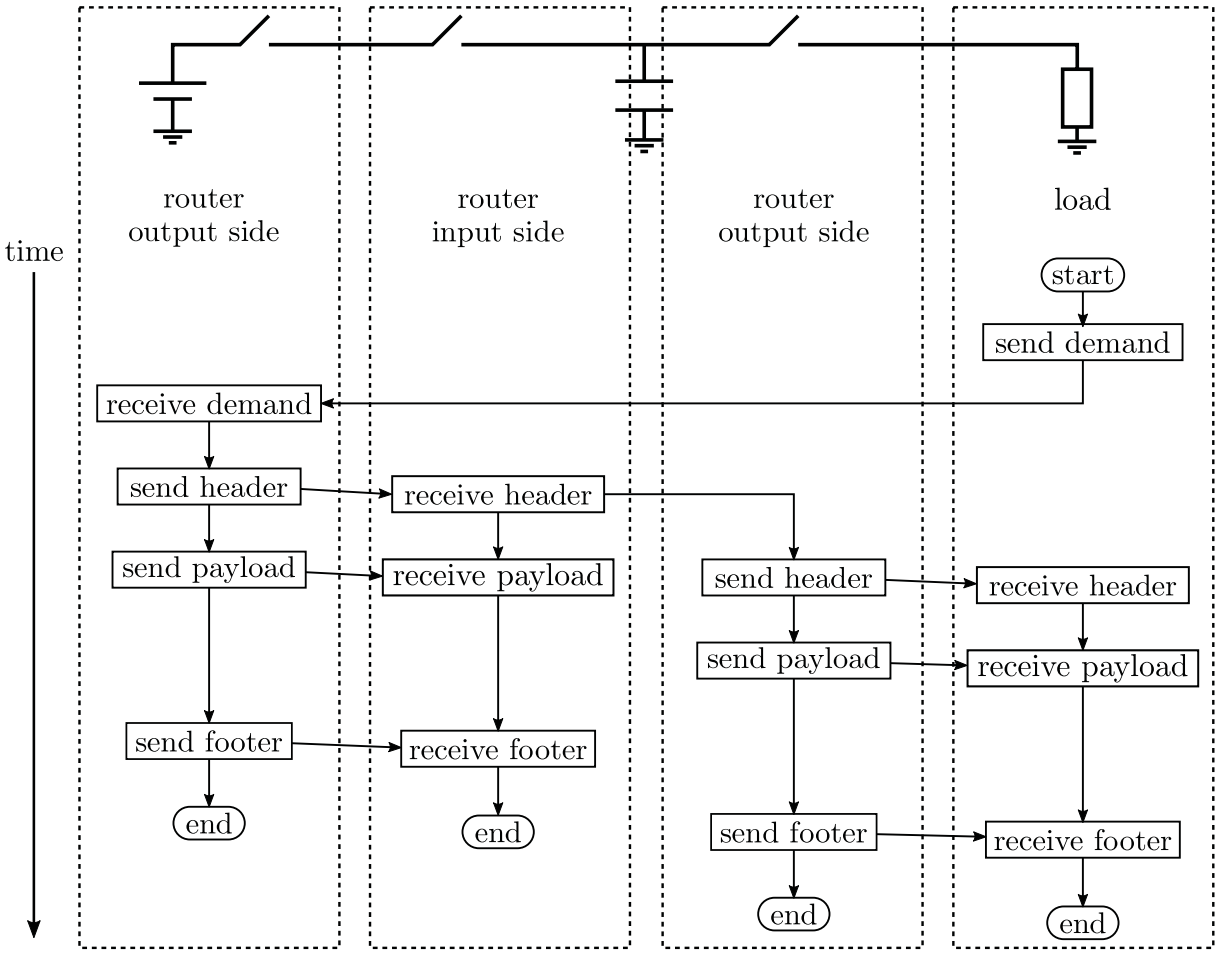


Figure 3.1: Flowchart for system operation of centralized energy on demand control. Whole system works on the same time base.

Ohm's law. In the power packet dispatching system, spatial connections of routers control discontinuous power flow. In addition to the continuous power flow during transmission, the spatiotemporal connection of routers controls the discontinuous power flow.

Preceding studies have employed the centralized control method [19]. The centralized control has a single controller, and it governs the whole system. Figure 3.1 shows a flowchart of on-demand power packet transmission under the centralized control. A demand from a load is transmitted to the corresponding router, which governs the whole system. Then, the router sends a power packet as a response. The power packet is transmitted to the load, routed among the network. The routing requires the time to recognize the destination on each router, resulting in the delay. They are observed in the previous studies [23, 66].

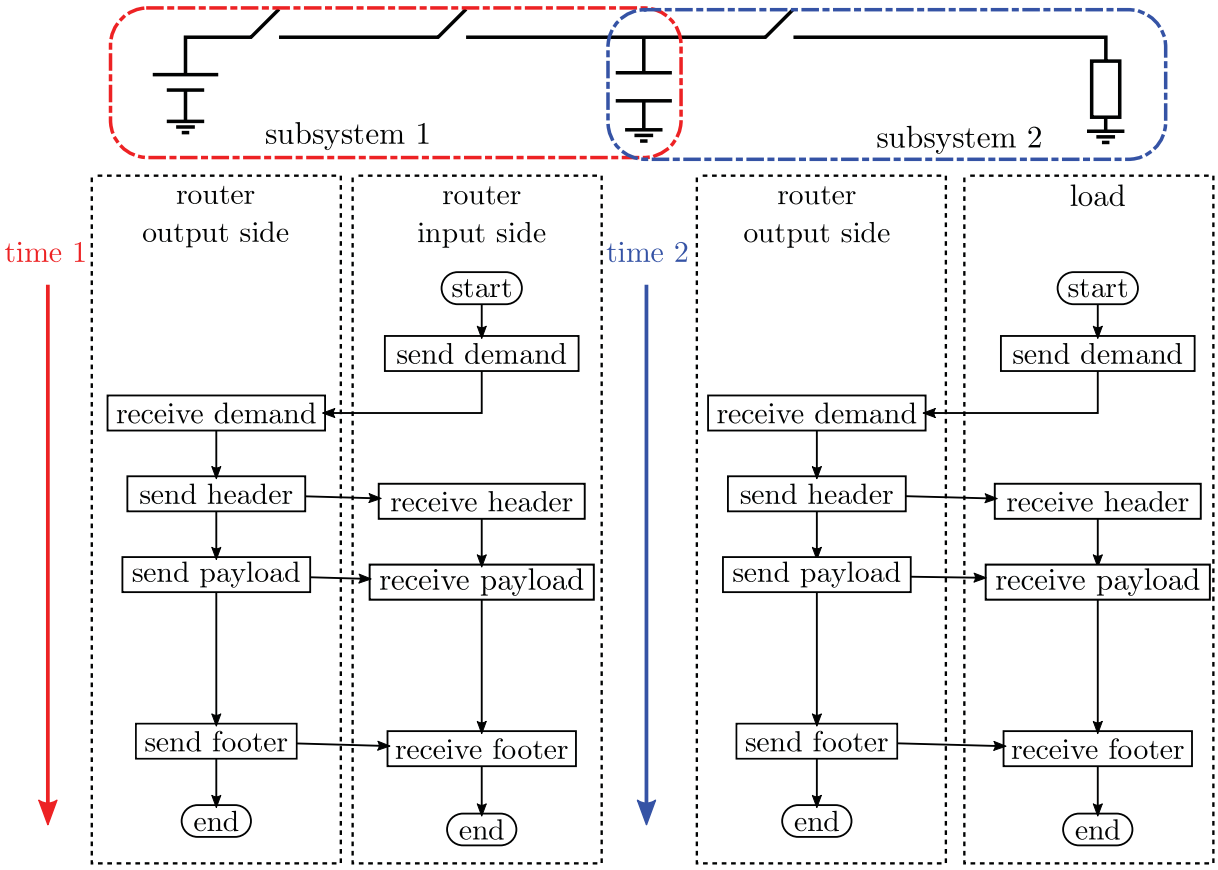


Figure 3.2: Flowchart for system operation of decentralized energy on demand control. Times 1 and 2 are independent of each other, and subsystems 1 and 2 work on the different time bases.

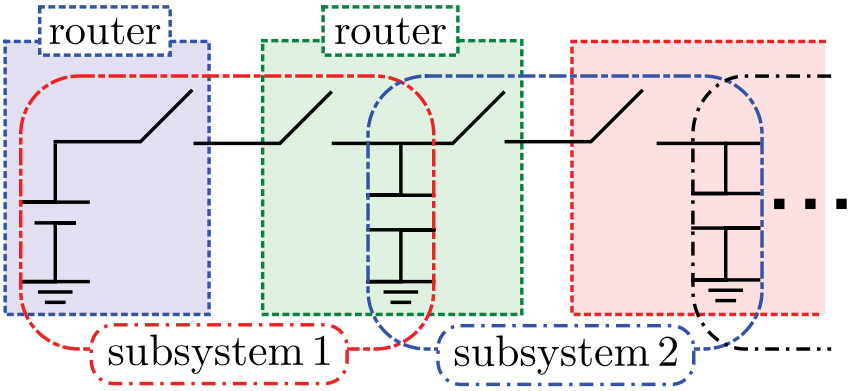


Figure 3.3: Schematic diagram of the subsystems and connections of subsystems.

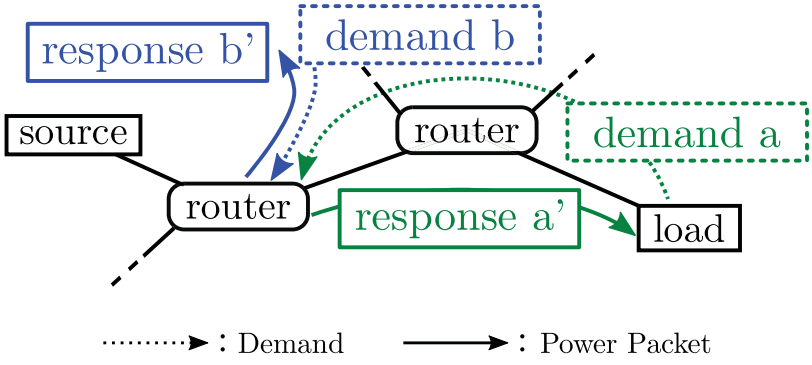
This paper proposes a decentralized control. The flowchart of the control is shown in Fig. 3.2. Under the control, the whole network is divided into subsystems. Figure 3.3

shows the concept of subsystems. The proposed decentralized control divides a router into the input and output sides. A unit of subsystem contains an input side of a router, an output side of its neighboring router, their power source and storages, and their connection. Neighboring subsystems share the source and storage. Each subsystem works independently. The demand from a load is transmitted to the neighboring router in the same subsystem. The neighboring router responds to the demand with its stored energy. When the stored energy is insufficient, the router demands the energy to other routers (s). Thereby the demand finally reaches the source. The proposed control utilizes the stored energy distributed in the network and minimizes the delay of the control.

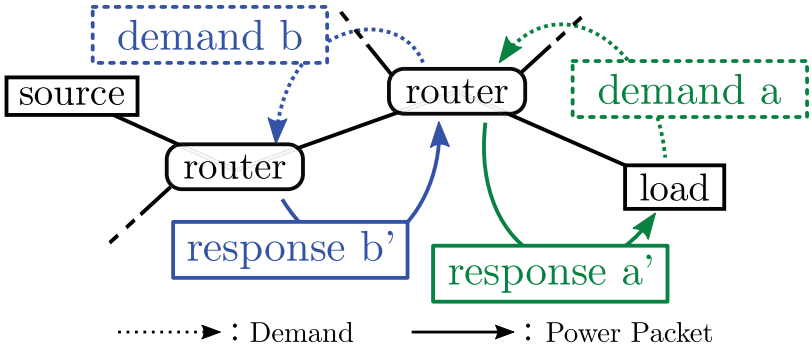
3.1.1 Comparison of centralized and decentralized controls

Let us compare the centralized and decentralized controls. Figure 3.4a and 3.4b depict the operation concepts of the centralized control and the proposed decentralized control. The responses shown by a' and b' are transmitted to the demands a and b, respectively. The responses consists power packets, but the demands accepts any form.

Being apart from the control operation, the proposed decentralized control is expected in the following aspects. The first one is the length of the signal. The centralized controller recognizes the whole loads and their addresses or routes to them. Thus, the length of the addresses or indexes of routes depends on the number of loads under control. The decentralized control requires the controller to process the demands from the neighboring routers and loads. The number of routers and loads under a single decentralized controller is equal to or less than the centralized controller. It helps decrease the time to communicate and improve the response time. The decrease in the communication time also increases the time to transmit power, since power and information share the same power line. The second aspect is the flexibility of the network. The modifications in the network are expected to be easier by the proposed decentralized control. The centralized control will deliver the modification information to all relevant network elements—for instance, a new load and its specifications should be notified to all routers. On the other hand, the decentralized control requires the subsystems to recognize the connecting information. Thus, a new connection is informed only to the neighboring router. In addition to them, the robustness against breaking down is expected to be high.



(a) Concept of demand-response operation based on centralized control.



(b) Concept of demand-response operation based on decentralized control.

Figure 3.4: Operations of demand-response power packet transmission.

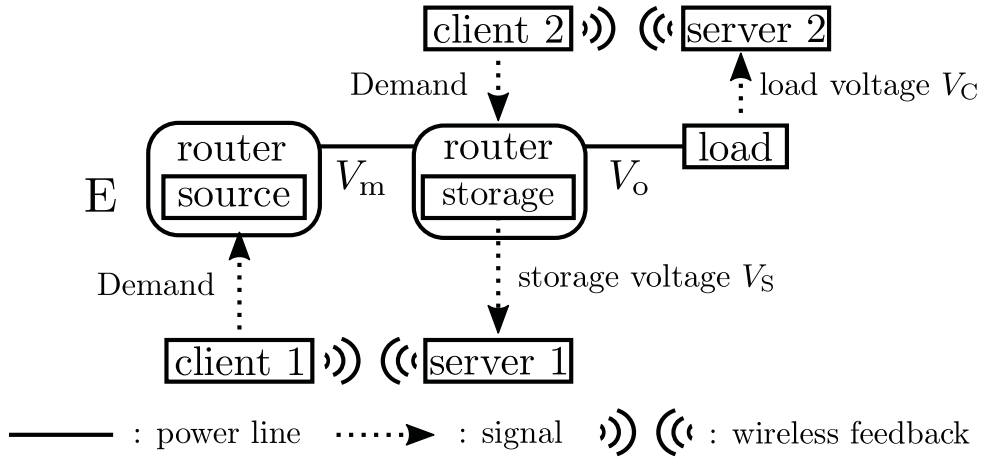


Figure 3.5: Concept of power packet dispatching network.

3.2 Experimental verification with wireless feedback

Figure 3.5 shows the schematic diagram of the experimental system. The system consists of a source, two routers, and a load. The circuit configuration of the load is

Table 3.1: Parameters of experimental system.

Name	Symbol	Value
Source voltage	E	9.0 V
Load	R_L	330 Ω
Storage capacitance	C_s	100 μF
Load capacitance	C_c	470 μF
Series resistance	R_s	33 Ω

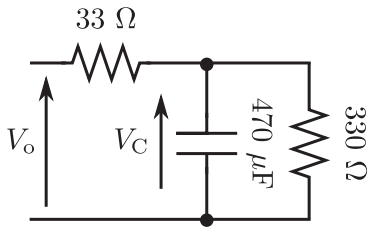


Figure 3.6: Experimental circuit of load.

given in Fig. 3.6. The parameters of the system are listed in Tab. 3.1. We used the uni-directional router proposed in [24]. The source voltage E is set below the rating voltage of the router, 12.0 V. The series resistance R_s decreases the inrush current to the storage. Two subsystems are included in the system. The wireless feedback through Wi-Fi is implemented by microcomputers (Intel®Edison Kit for Arduino). Server 1 and 2 transmit data over Wi-Fi to client 1 and 2, respectively. Clients communicate with the routers through the General Purpose Input Output (GPIO). Servers also measure the corresponding storage voltages by their analog-digital converters (ADCs). ADC has a resolution of 10 bits, and its input range is 0 to 5.0 V. E is 9.0 V, so the storage voltage V_S and the load voltage V_C will exceed the input range of ADC. A voltage divider circuit is implemented to meet the input range of ADC. The circuit consists of resistors and an operational amplifier (OPA627). It divides the storage voltage by 5. Server 1 and server 2 measure the divided voltages $V_{s1}(= V_S/5)$ and $V_{s2}(= V_C/5)$, respectively. A unit power packet consists of 100 bits. The time duration of 1 bit was set at 20 μs. The bit assignment of a power packet is shown in Tab. 3.2.

A simple on-demand power distribution control is adopted to the experimental system. It sets threshold voltages to V_{s1} and V_{s2}. The threshold voltages are set at $V_{t1} = 1.17$ V and $V_{t2} = 1.07$ V. They correspond to 5.85 V for V_S and 5.35 V for V_C. When V_{s1} undergoes V_{t1},

Table 3.2: Bit assignment of power packet.

Start signal	Address	Payload	Footer
3 bits	4 bits	91 bits	2, bits
"101"	"0000"	"11...11"	"00"

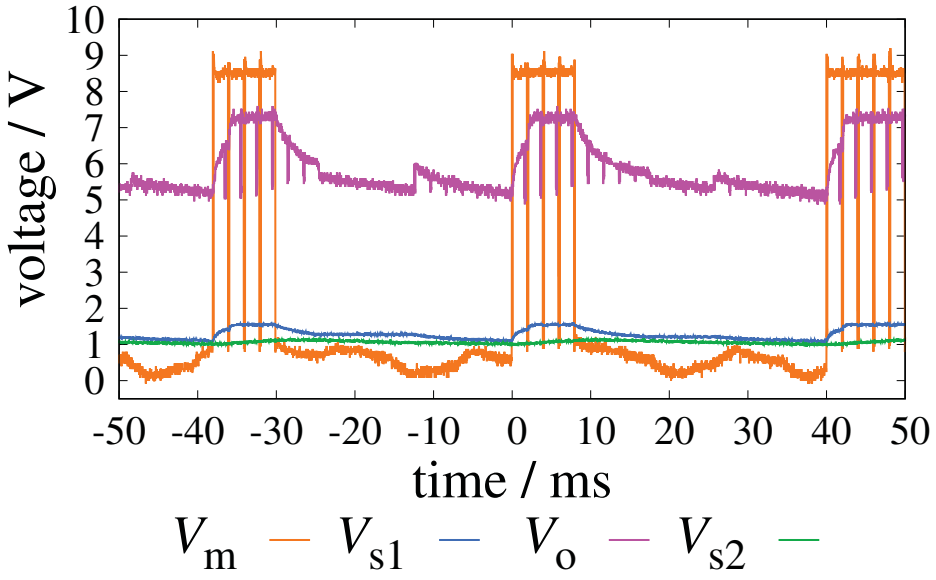


Figure 3.7: Measured voltage waveforms for $V_1 = 9.0\,V$, $V_{ts1} = 1.17\,V$, $V_{ts2} = 1.07\,V$.

server 1 demands the power packet transmission to client 1. The demand is continuously transmitted until V_{s1} reaches to V_{t1}.

Figure 3.7 shows examples of the experimental results. We measure the power line voltage V_m, the output voltage V_o, V_{s1}, and V_{s2}. The short pulses on V_m and V_o are the voltage waveforms of power packets. The highest voltage of V_m is around 8.4 V, which is 0.6 V lower than E. The voltage dropdown owes to the diode. V_m fluctuates at 60 Hz around 0 V when no power packet is transmitted. The fluctuation is recognized as the ground noise from the source. It is confirmed that the noise does not affect the experiment. V_o does not reach the ground level when the power packet transmission is stopped. The output port of the router is directly connected to the load. The load capacitor keeps the load voltage during the interval of power packet transmission. It also keeps the load voltage at V_o. It is shown that V_{s1} and V_{s2} are kept around their threshold voltages V_{ts1} and V_{ts2}. The delay of the implemented feedback control is estimated around 5.0 ms.

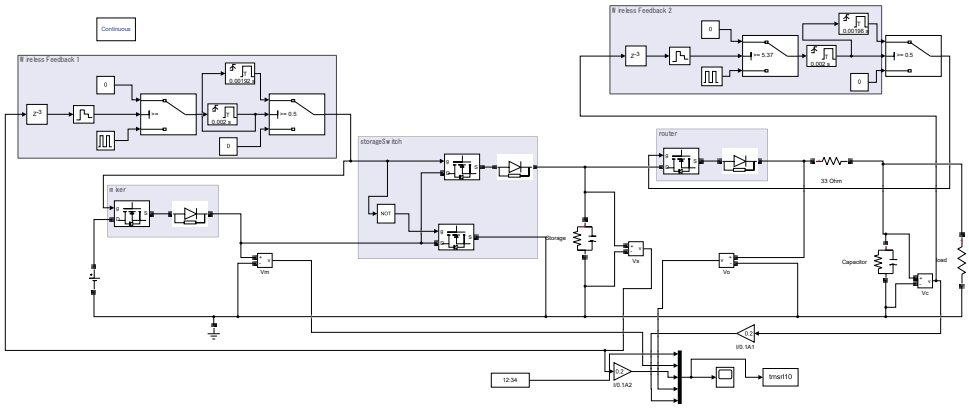


Figure 3.8: Simulation model of experimental system with two subsystems.

Table 3.3: Parameters of switches in simulation.

On resistance of FETs	$0.7\,\Omega$
Voltage drop of diodes	$0.6\,\mathrm{V}$

The sampling interval is shorter than 2.0 ms. V_m and V_o show that the router transmits more power packets than the router. It confirms that the proposed decentralized control method is realized experimentally. The on-demand power transmission keeps the target storage voltages around their threshold voltages.

3.3 Simulation verification

We also conduct a simulation to verify the experimental results. The experimental system was modeled in MATLAB/Simulink as in Figure 3.8. The device parameters are set at the same values as Tab. 3.1. In the simulation, we fixed the on-resistance of the MOSFET and voltage drop of the diode as shown in Tab. 3.3. The power line is assumed to be ideal. Power packets are given by rectangle voltage pulses to evaluate the storage voltages under the proposed decentralized control. The wireless feedback loop was simulated by the comparator and delay blocks in MATLAB/Simulink. The delay block samples and holds the voltage at the interval of 1.67 ms. With the block, the comparator reads the voltage of three samples before. The total delay is at 5.0 ms.

Figure 3.9 shows the simulation results. It quantitatively coincides with the experimental results. The estimated duration of delay was also verified by the simulation. In the

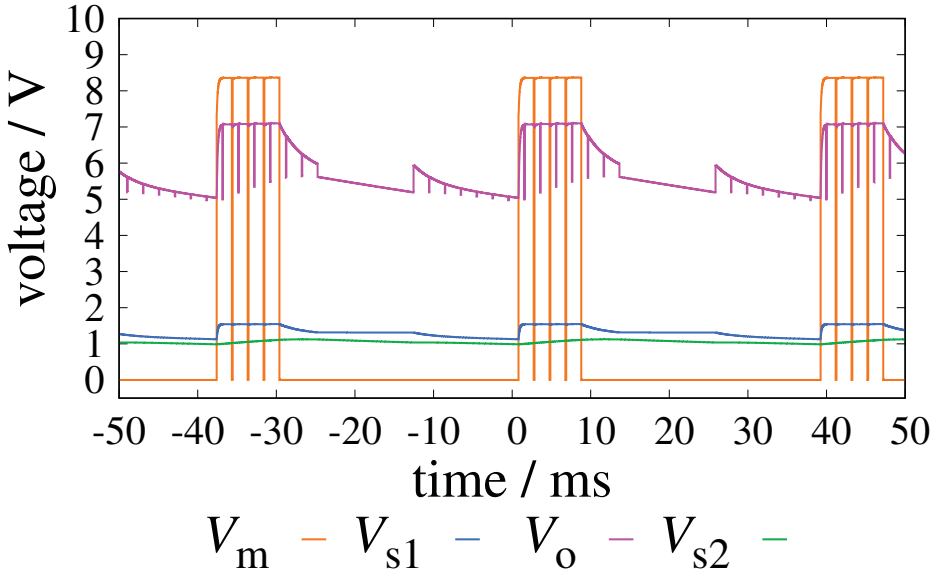


Figure 3.9: Simulated voltage waveforms for $V_1 = 9.0\,V$, $V_{ts1} = 1.7\,V$, $V_{ts2} = 1.07\,V$.

simulation, V_o steeply increases than the experimental results. The power line is the cause of the steep increase. The simulation assumed the ideal power line without impedance. The inductance prevented the sharp increase in the experiment.

The proposed decentralized control allows that each router operates independently. The feedback loop implemented by the wireless communication had a delay of around 5.0ms. The duration was about 2.5 times longer than a power packet. It requires each load to have a large capacitor to maintain the power supply.

3.4 Wired feedback

This section experimentally verifies energy-on-demand control over a single power line to decrease the feedback delay. The bidirectional switches are configured with an inverse-parallel connection of SiC JFETs and fast recovery diodes. This configuration prevents unintentional short circuits of sources.

Figure 3.10 shows the circuit configuration for power packet transfer by the energy-on-demand. It consists of two sources, two routers, and one load. Parameters of passive components are shown in Fig. 3.10. Router 1 is connected to two energy sources and Router 2 to two capacitors. Source 1 is set at 15.0 V and Source 2 at 14.0 V. The switch between Storage 1 and the load is always kept ON. Storage 1 holds the energy specified to

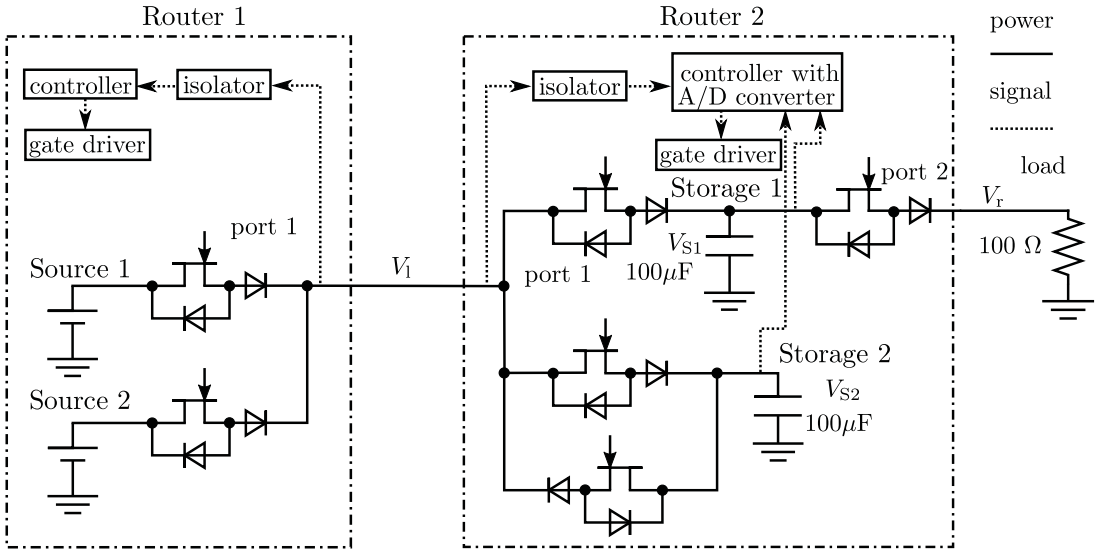


Figure 3.10: Schematic of experimental setup.

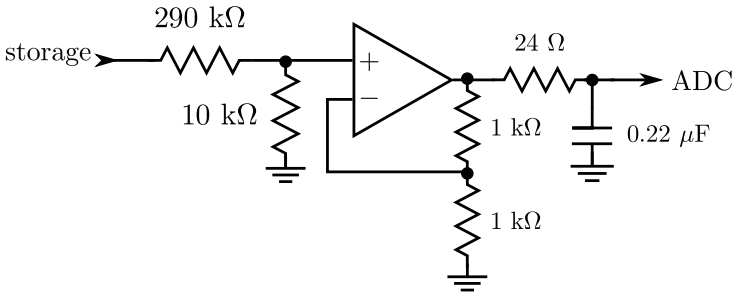
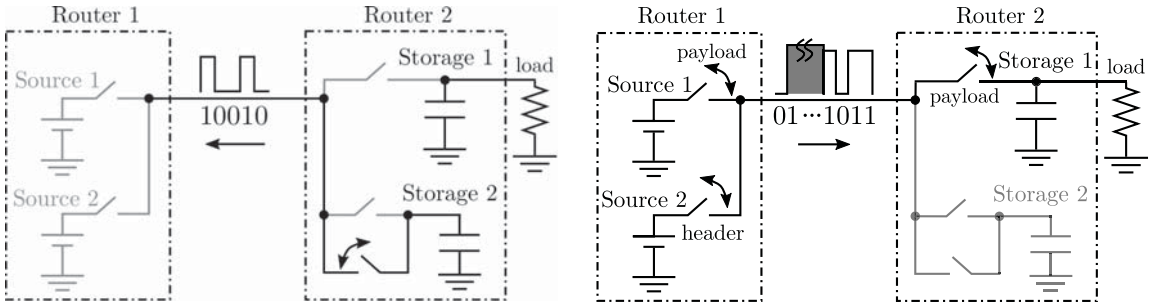


Figure 3.11: Schematic of voltage divider circuit.

Source 1 and Storage 2 to Source 2. Source 2 is also used to generate the information tags of the generated packet. Each storage voltage is set as a criterion for energy-on-demand control. A threshold voltage is independently set to storage. When the storage voltage becomes less than the threshold, a power packet is sent to Router 1 with null payload as a demand signal, using power from Storage 2. Router 1 generates and sends a power packet to Router 2 according to demands. This is the proposed scheme. The threshold voltages are 11.3 V for Storage 1 and 10.3 V for Storage 2. Storage 2 is prioritized over Storage 1. When both of the storage voltages become less than the thresholds, the demand of Storage 2 is sent first. This is because the power of Storage 2 is the source of the demand signals. The controller of Router 2 is used to measure the storage voltages. A 12-bit ADC at the range from 0 to 1 V with a sampling rate of 1 MHz is implemented in the controller. The controller measures the voltage of storages 1 and 2 alternately so that

Table 3.4: Configuration of power packet and demand signal.

	Start signal	Address	Payload	Footer
Power packet	"11"	"10" or "01"	"11" ... "11"	"0"
Demand signal	"10"	"10" or "01"	—	"0"
Length	2 bits	2 bits	30 bits	1 bit



(a) Sending demand signal from Router 2.

(b) Power packet transmission as a response to the demand.

Figure 3.12: Operation of demand–response power packet transmission.

the sampling rate is 500 kHz for each storage. The circuit shown in Figure 3.11 divides the storage voltage by 15 to meet the rating of ADC. An operational amplifier (OPA627, TEXAS INSTRUMENTS) is used. The cutoff frequency of the low pass filter is designed sufficiently lower than the Nyquist frequency of the sampling frequency.

Table 3.4 shows the configuration of power packets in the experiment. Demand signals are configured without payload. Address "01" is fixed to Source 1 (or Storage 1) and "10" to Source 2 (or Storage 2), depending on the direction of packet transfer. Routers can distinguish the address of the source (or storage) in the start signal. Figure 3.12 shows the system operation. When Router 2 demands the power of Source 1 to Router 1, "10010" is sent to Router 1(Fig. 3.12a). Then, "110111...110" is sent after it (Fig. 3.12b). The duration of a bit is set at 0.01 ms. Router 1 supplies a clock synchronization signal to Router 2. This clock synchronization can be achieved by attached preamble signal to power packets [56].

Figure 3.13 shows the voltage waveforms at the port of Router 2 ($V_{\rm I}$), Storage 1 ($V_{\rm S1}$), Storage 2 ($V_{\rm S2}$), and the load ($V_{\rm r}$). It is found that the proposed scheme maintains $V_{\rm S1}$ and $V_{\rm S2}$ around their thresholds and achieves power supply to the load. Figures 3.14a and

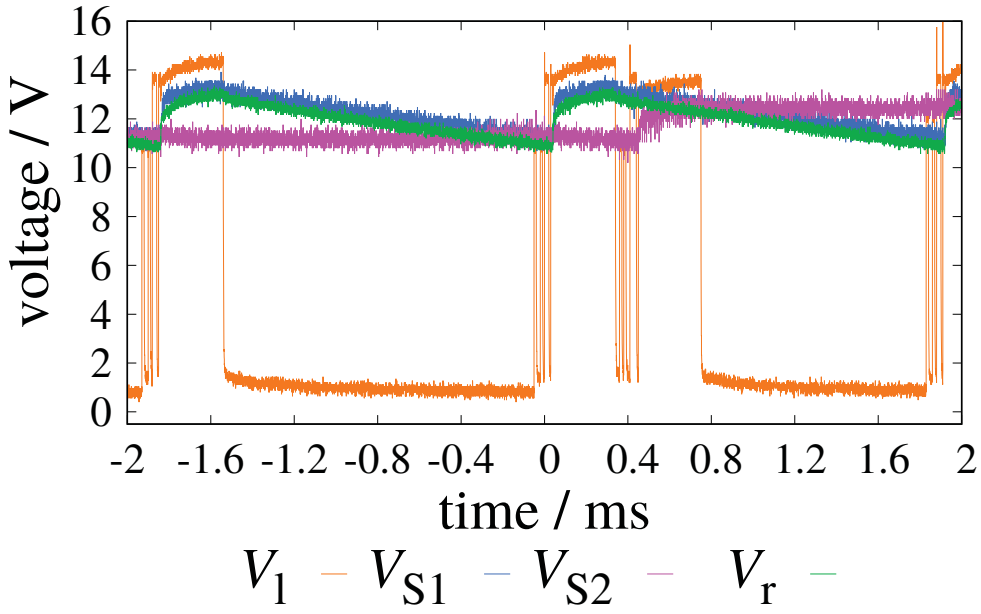
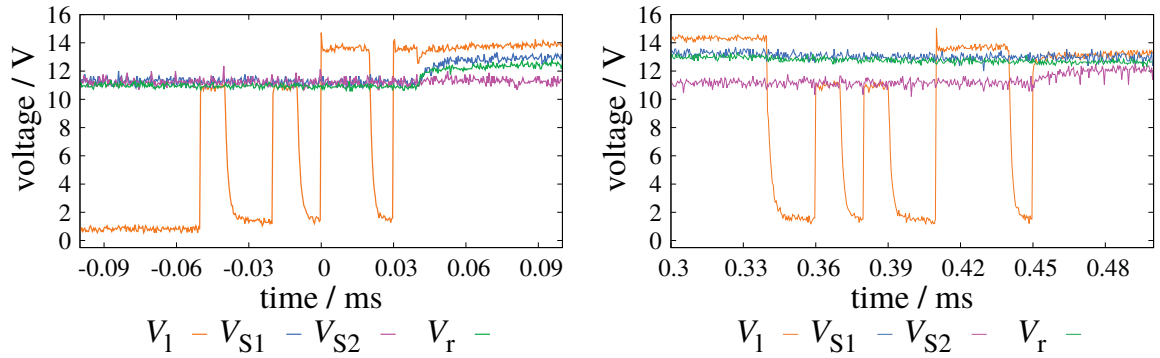


Figure 3.13: Experimental results.



(a) Detailed view of demand signal for Storage 1.

(b) Detailed view of demand signal for Storage 2.

Figure 3.14: Detailed views of Fig. 3.13.

3.14b show the extension of Fig. 3.13. They show the information tags of power packets exchanged between Router 1 and Router 2. Obviously, the information tags of demand signals and power packets are the same as in Tab. 3.4. In addition, we find the voltages of information tags are the same and about 14 V in Figs. 3.14a and 3.14b. It indicates that the information tags are generated by Source 2. In Fig. 3.14a, a demand signal "10010" is sent to Router 1 using the power of Storage 2. Receiving the demand signal, Router 1 sends a power packet tagged "11101". The result shows that the bidirectional wired communication between Router 1 and Router 2 follows the settings. It is also confirmed

by Fig. 3.14b. In addition, information tags and the voltage of payload and storages have the relationships as shown in Tab. 3.4. Figures 3.14a and 3.14b show that the demand signals are sent when V_{S1} or V_{S2} becomes less than each threshold and power packets are sent according to the demands. It implies that the bidirectional power packet transfer exactly realizes the proposed scheme and the energy-on-demand control via a single power line.

3.5 Summary

The decentralized control of the power packet dispatching system was proposed in this chapter. The proposed decentralized control divides the system into subsystems. Each subsystem operates independently. The control is expected in the flexibility of the network, the length of the signal, and the response time. The experimental verification was performed with the on-demand power packet transmission by the wireless feedback mechanism. The on-demand transmission was implemented based on storage voltages. Under the proposed control, the subsystems in the network operate independently. The simulation also verified the operation. The results with the wireless feedback revealed that the feedback delay was longer than a power packet.

In order to shorten the delay of the feedback, the bidirectional wired communication was verified. The bidirectional communication via a single power line was implemented with the inverse-parallel connection of switches. The connection avoids the collision of power. The experimental results verified the on-demand power packet transmission without significant delay. They also showed that the bidirectional communication in the power packet dispatching system. These results verified the decentralized on-demand power distribution in the power packet dispatching system.

The subsystems operate independently under the proposed decentralized control. On each connection, power packets should be distinguished at least by their voltages to avoid the short circuit. Because the number of voltages to transmit on a connection is not the same, we can design the signal part of the power packet separately for each connection. Based on the idea, we consider the power packet transmission between routers in the next chapter.

Chapter 4

Multidirectional power packet transmission

This chapter examines what amount of information is required to achieve power packet transmission between routers. First, we verify bidirectional power packet transmission through a single power line (half-duplex transmission). The experimental results in Sec. 3 showed that bidirectional signal transmission is available. In order to achieve bidirectional power packet transmission, we have to prevent the collision of power. The collision of power can result in a short circuit between sources and is not acceptable. We adopt a medium access control (MAC) protocol to avoid the collision of power. A power packet dispatching protocol that corresponds to the network layer protocol in OSI reference model was proposed [67]. Likewise, this study implements a MAC protocol for the power packet transmission. The bidirectional power packet transmission is experimentally verified with the proposed MAC protocol. Then, by extension of the bidirectional transmission, the multidirectional power packet transmission is studied. Two additional MAC protocols are adopted to the system. They are evaluated in terms of required bits and their impacts on power transmission. These results indicate the amount of required information for the power packet transmission between routers.

4.1 Bidirectional power packet transmission

The bidirectional power packet transmission is verified. The bidirectional power flow in a router was experimentally verified [26]. The bidirectional communication in one-to-one connection can be achieved by full or half-duplex communication. Full-duplex wired communication uses at least two pairs of wires. It allows both transmitters to send

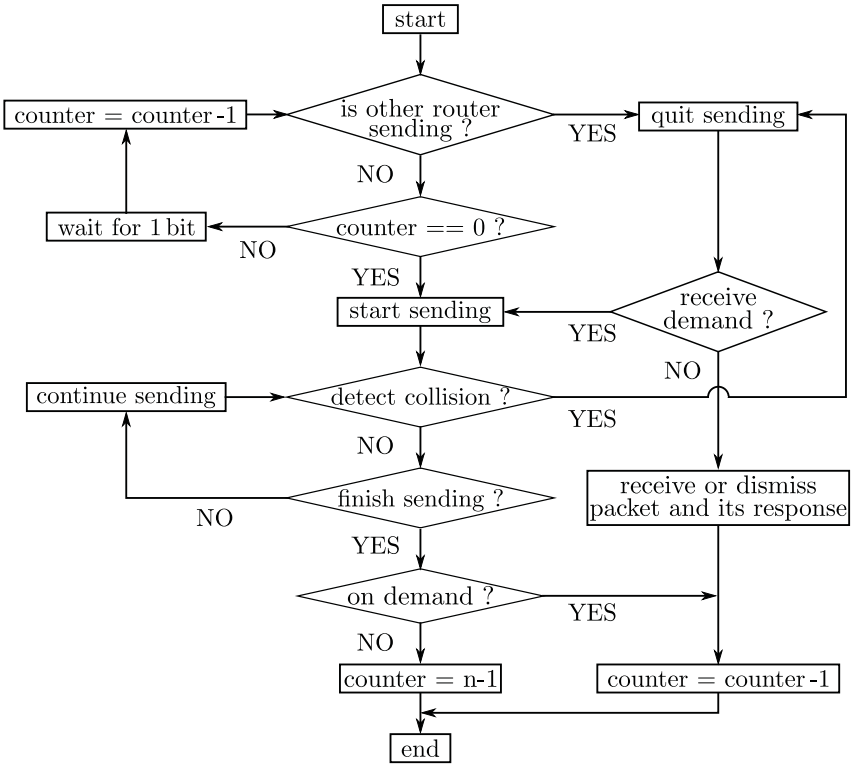


Figure 4.1: Flowchar of proposed MAC protocol.

packets without any concern about collisions. Half-duplex wired communication uses one pair of wires. It allows only one transmitter to send a packet at one time in order to avoid collisions. It leads to a reduction in the number of wires that also reduces the weight and resources of the system. The half-duplex communication is achieved by a MAC protocol in information networks. The power packet dispatching system also needs a MAC protocol to achieve half-duplex transmission. In communication, the collision of packets decreases the traffic performance. It is also true in the power packet dispatching system. In addition, the collision of power may induce a short circuit in the power packet dispatching system. Therefore, the MAC protocol for the half-duplex power packet transmission must prevent the collision of power.

4.1.1 MAC protocol for power packet transmission

We propose a MAC protocol for the half-duplex power packet transmission. Figure 4.1 shows the flowchart of the protocol. “n” in the flowchart means the numbers of routers connected to the same power line. The protocol is based on two algorithms used in

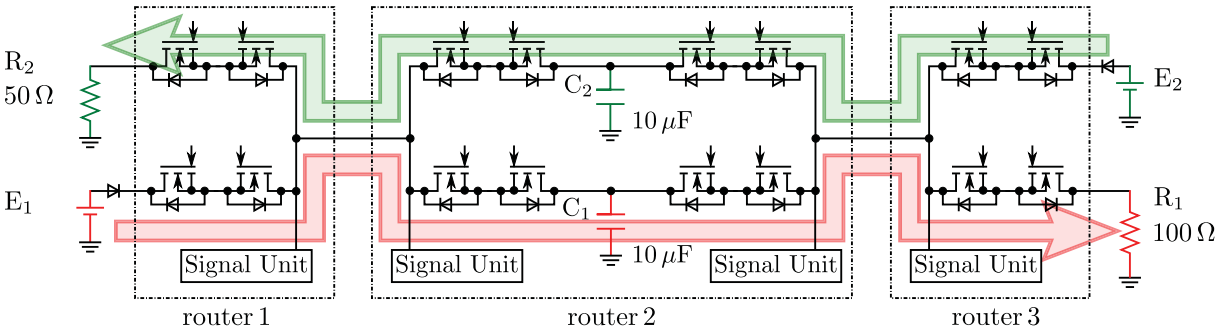


Figure 4.2: Schematic diagram of experimental systems with two sources, two loads, and three routers.

Table 4.1: Configurations of power packets and demand signals.

	Start signal	Address	Length	Payload	Footer
Power packet	3 bit	2 bit	2 bit	40/60 bit	3 bit
Demand signal	3 bit	2 bit	—	—	2 bit

information networks [29]. The binary countdown algorithm detects collisions of signals (the header signals). The round-robin algorithm solves the contention. When the signals are designed appropriately, the algorithm allows all routers except for one router to detect the collision of signals. The one router which cannot detect the collision continues sending. The other routers quit sending, and receive the incoming power packet. We allow header signals to collide with each other to know the existence of other power packets. The round-robin algorithm gives priority to sending packets to the routers [68]. The prioritization is realized by modifying signals or putting some delay to the transmission.

When the following two assumptions are satisfied, the proposed protocol prevents collisions of power. The first assumption is that all routers connected to the same power line are synchronized with regard to the power packet transmission. The assumption ensures that routers can detect the collisions with the binary countdown algorithm. In addition, it ensures that the round-robin algorithm works appropriately. The second is that bit errors do not occur. These assumptions ensure the collision detection.

4.1.2 Experimental verification

The half-duplex power packet transmission is experimentally verified under the proposed MAC protocol. Figure 4.2 shows the experimental circuit configuration. The values of the circuit elements are also shown in Fig. 4.2. The circuit consists of two power sources,

Table 4.2: Bit assignment of power packets and demand signals.

Transmitter	Receiver	Power packet	Demand signal
router 1	router 2	"11001101...1000"	"1001000"
router 2	router 1	"11010011...1000"	"1000100"
router 2	router 3	"11001011...1000"	"1001000"
router 3	router 2	"11010101...1000"	"1000100"

two loads, and three routers. The DC power sources E_1 and E_2 supply power to R_1 and R_2, respectively. The power is relayed by the storage S_1 and S_2 in router 2, respectively. The DC power sources of 12 V are the power sources of routers. 12 V is high enough to ignore the noise in reading signals.

The routers send power packets in response to demands. We set demand signals to achieve it. Table 4.1 shows the bit assignment of power packets and demand signals. A power packet consists of the start signal, address, length, payload, and footer. The start signal, address, and length form the header signal. The start signal tells the start of the power packet. The address and length transmit the destination and the bit length of the payload. The footer tells the end of the power packet or demand signal. It pulls down the power line voltage to the ground level. A demand signal does not contain the length and the payload. The bit rate of the system was set at 1 Mbps. The routers share the same clock signal of 1 MHz and thus are synchronized concerning the signal transmission. The bit rate was low enough to satisfy the second assumption in reading signals of power packets.

Each router tries to send as many demand signals as possible. The proposed MAC protocol controls the transmission. According to the protocol, transmission priority is given to two routers alternately. As a result, two routers send demand signals and respond to them alternately. The experimental system is under the proposed decentralized control in Chapter 3. Two subsystems in the network operate independently. The voltages of E_1 and E_2 were set at 18.0 V and 24.0 V in case 1 and 24.0 V and 18.0 V in case 2. The voltage and current waveforms of the power line between router 1 and 2 (V_{l1}, I_{l1}) and router 2 and 3 (V_{l2}, I_{l2}) were measured in two cases above. I_{l1} and I_{l2} take positive values when they flow from router 1 to 2 and router 2 to 3, respectively. Then, we also measured the storage voltages V_{C_1} and V_{C_2}.

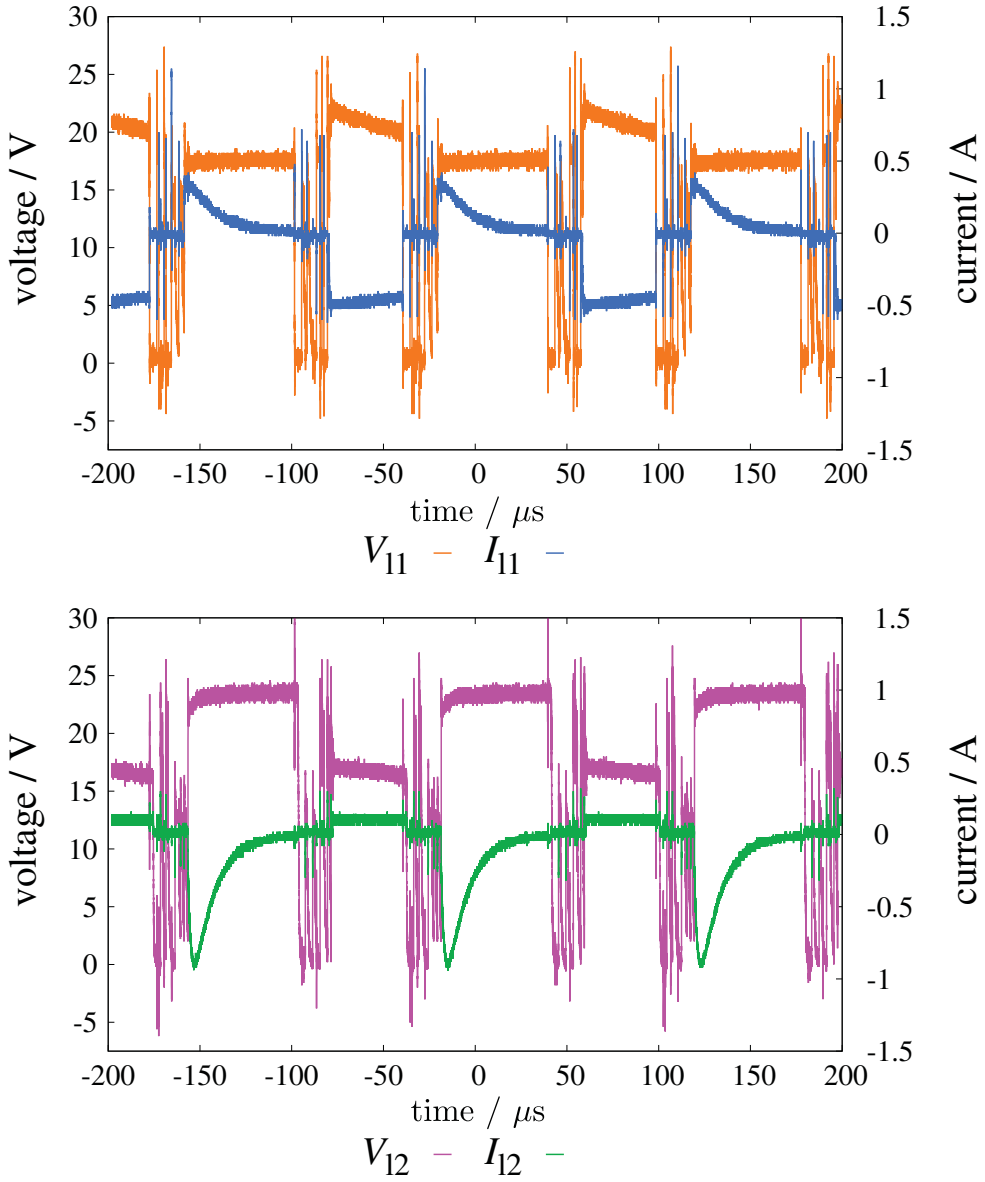


Figure 4.3: Experimental voltage and current waveforms.

4.1.3 Experimental results

Figure 4.3 shows the voltage and current waveforms. Figure 4.4 gives detailed views of V_{l1} and I_{l1} around -50 to 50 μs. The logical values of V_{l1} are confirmed in Fig. 4.4. A demand signal starts at -36 μs. Its logical value is "1000100", which means that router 2 sends the signal. The response power packet starts at -27 μs. The response has the header "11001101". I_{l1} flows from router 1 to 2. We can confirm that router 1 sends the power packet. Figure 4.3 shows that I_{l1} and I_{l2} change their directions alternately. V_{l1} and V_{l2}

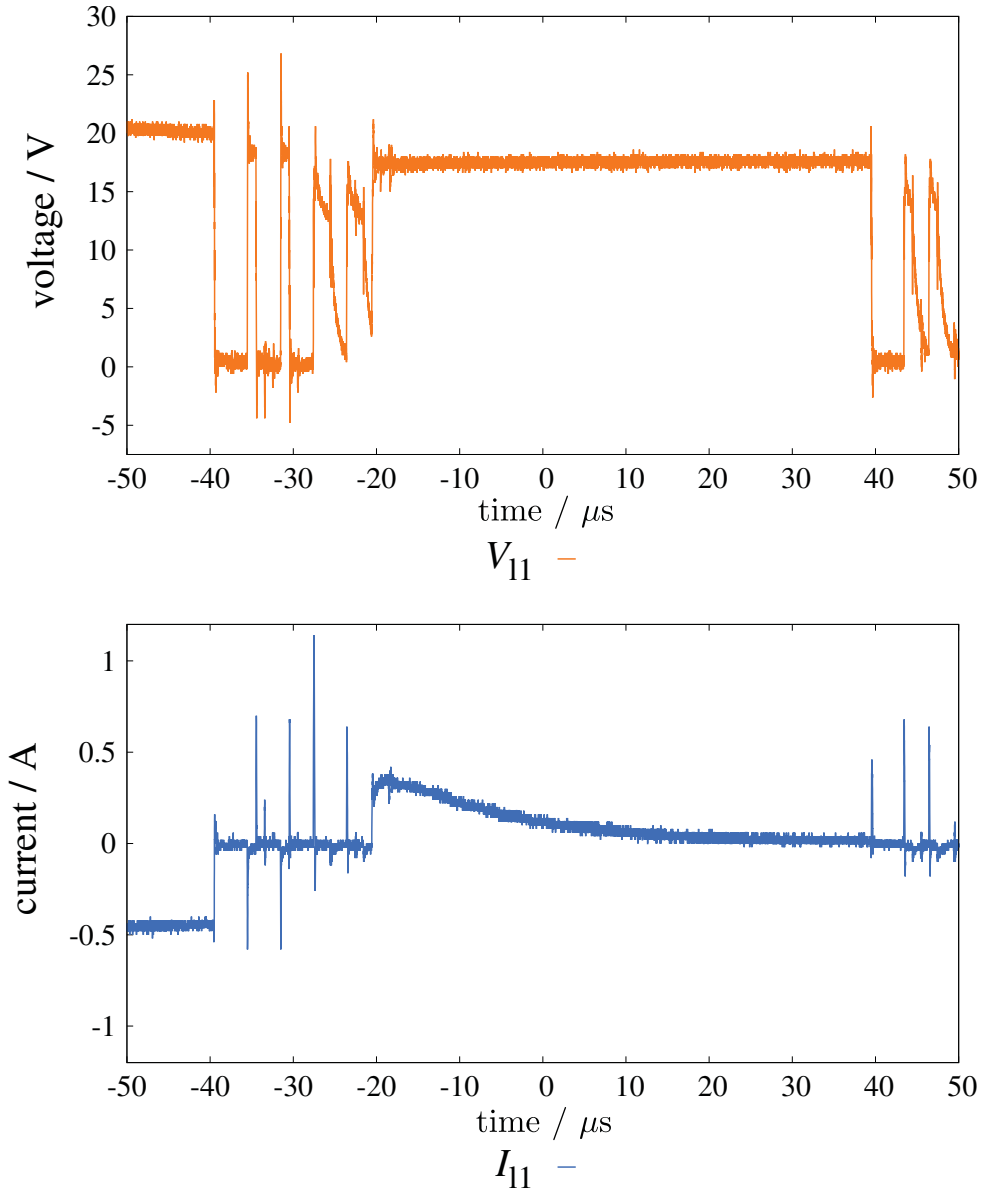


Figure 4.4: Detailed view of the experimental voltage and current waveforms between router 1 and 2.

are always positive when the current flows. Therefore, they show that the transmitted power also changes their directions alternately. The results clarify that the half-duplex power packet transmission is achieved on the both connections.

Figures 4.5 and 4.6 show the experimental voltage waveforms in cases 1 and 2, respectively. Comparing the results, we find that the fluctuations of V_{C_1} and V_{C_2} are larger in case 1 than in case 2. We discuss the reason for it seeing the system operation. V_{l1} and V_{l2}

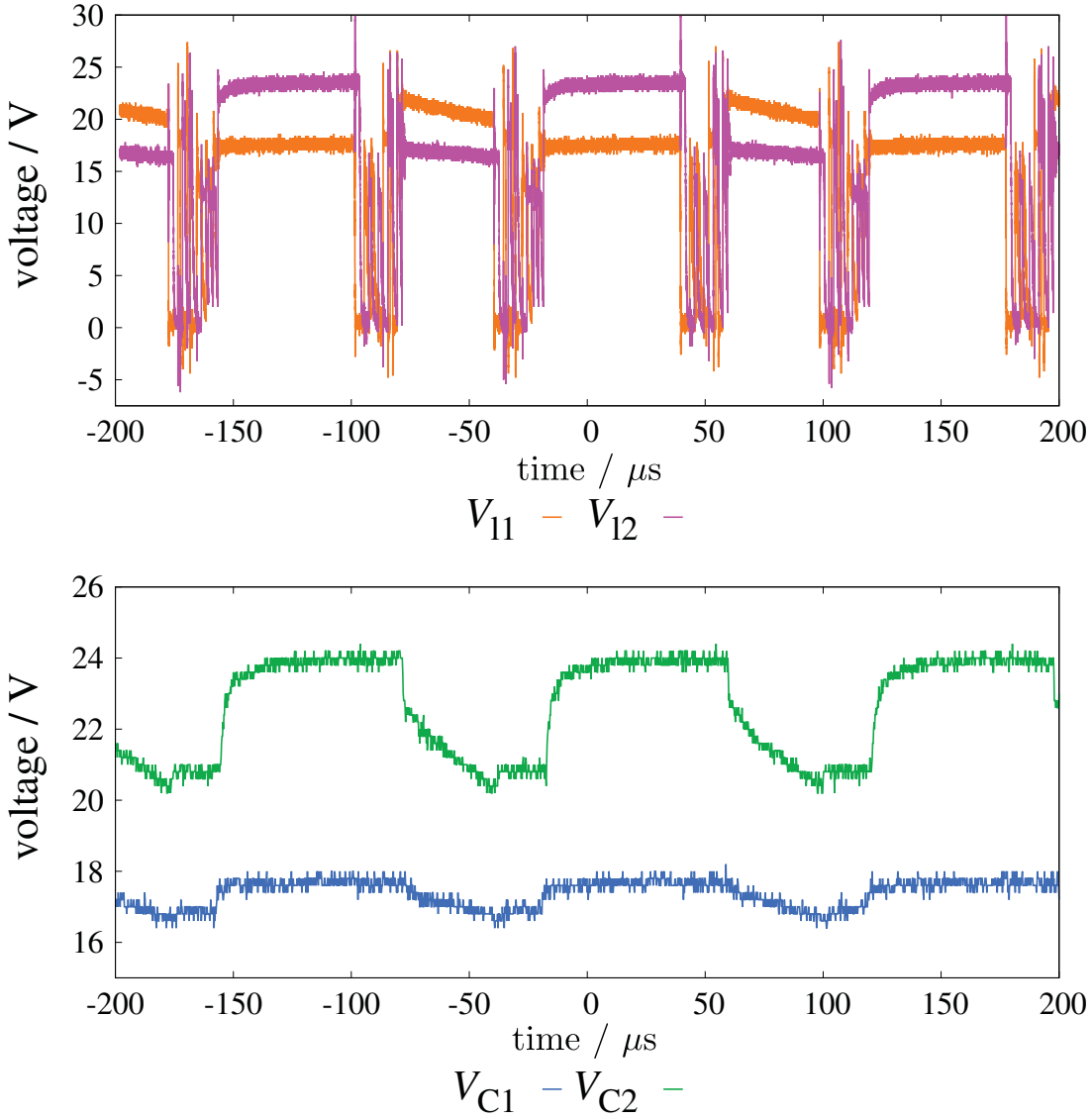


Figure 4.5: Experimental voltage waveforms in case 1.

show that the difference between these cases owes to the timings of the transmission. In case 1, the power packets with the 40-bit-payload are transmitted simultaneously. That is, routers 1 and 3 transmit power packets simultaneously. Thus, the sources and loads are connected indirectly. In case 2, they are connected directly since routers 1 and 2 transmit payload at the same time. The storage works as a source in case 1, but as a decoupling capacitor in case 2. It indicates that the connection in the network affects the storage voltages and outputs.

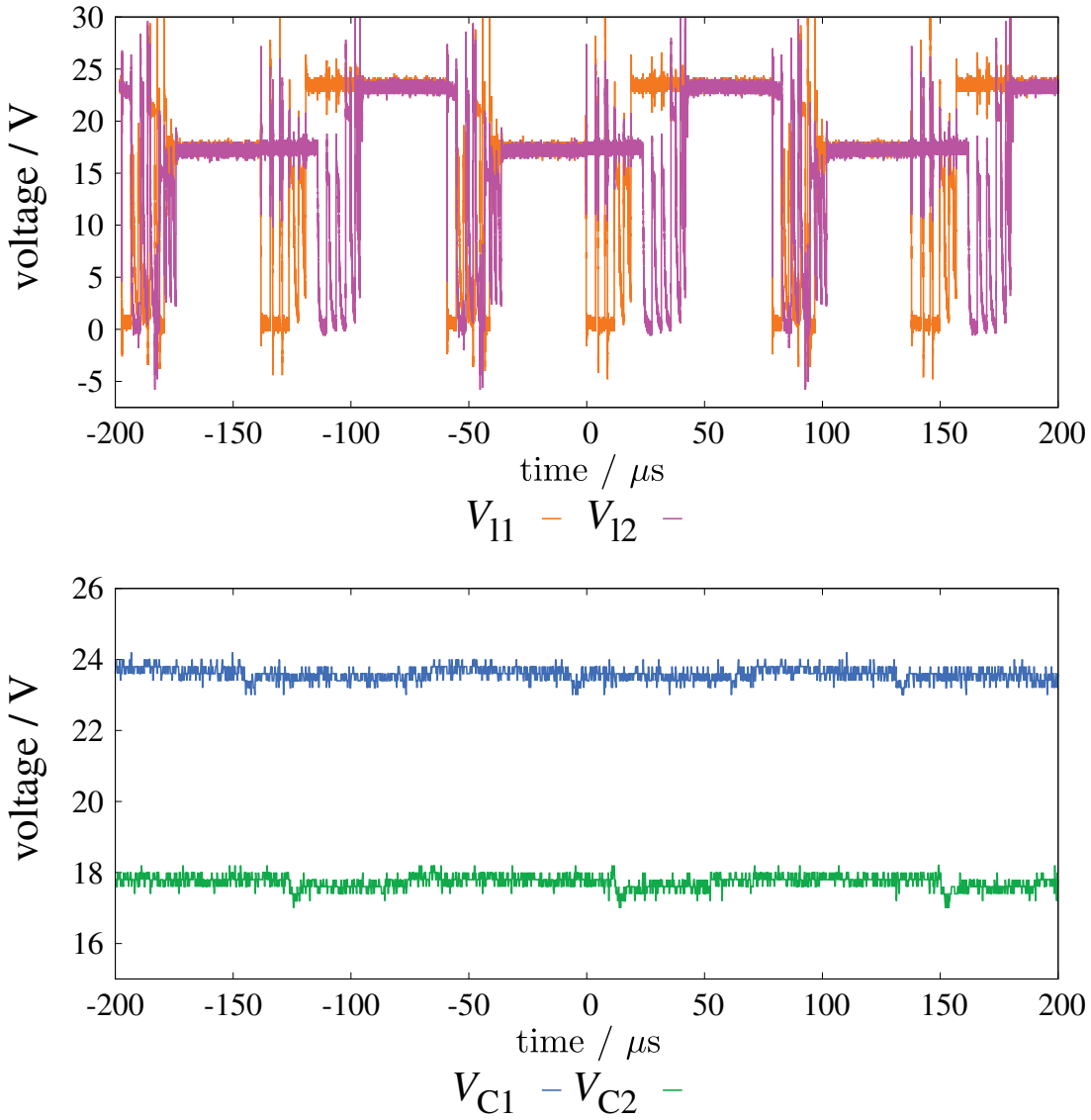


Figure 4.6: Experimental voltage waveforms in case 2.

4.2 Multidirectional power packet transmission

Based on the bidirectional transmission technique, we extend it to the multidirectional transmission. The advantages of multidirectional transmission include energy efficiency. We check it in a simple example. Fig. 4.7 shows three topologies in which two pairs of routers transmit power packets diagonally. In a bus topology, multidirectional transmission is necessary. A power packet reaches the destination without a relay. On the other hand, the star and ring topologies require a power packet to be relayed by a router. It results in the increase in transmission loss. The multidirectional transmission is achieved

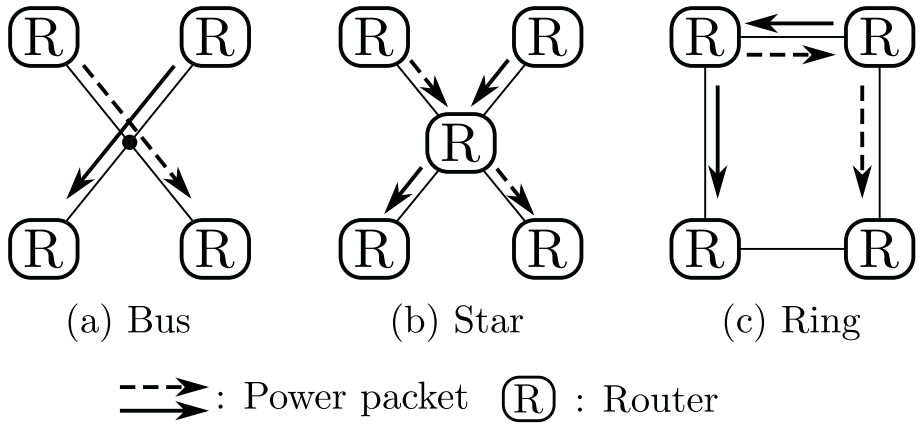


Figure 4.7: Comparison topologies with two pairs of routers placed diagonally.

by adding transmission control signals. The bit length of the signal depends on the kinds of power packets to distinguish. The bus topology increases the kinds. It is one of the disadvantages of the topology. This section examines the bit length required for multidirectional transmission. The amount of information is evaluated, and its effect on the transmitted power is evaluated.

4.2.1 Adopted MAC protocols

In addition to the experimentally verified MAC protocol, we introduce two protocols to compare their performances. Adopted protocols are the Carrier Sense Multiple Access/Collision Detection (CSMA/CD) and bit-map protocols [29]. They and the verified protocol, binary countdown protocol, serve the same function to the system but provide it with different mechanisms. Comparing their performances, we can examine the effect of the mechanisms. The flowcharts of CSMA/CD and bit-map protocols are shown in Figs. 4.8 and 4.9.

CSMA/CD employs the jamming technique. Fig. 4.8 shows the flowchart of the CSMA/CD protocol. When a router experiences a collision, a jamming signal is sent. The signal indicates the occurrence of a collision of signals to the other routers. Routers select their back-off times from their Contention Window (CW) at random on receiving the signal. At the expiration of the back-off time, the router sends a power packet. CW gets longer with repeated collisions. It is initialized to 4 bits with a successful transmission. The maximum length of CW is set at 2^7 bits. To adopt this mechanism in the power packet transmission, at least an additional bit is needed in the header for routers to find

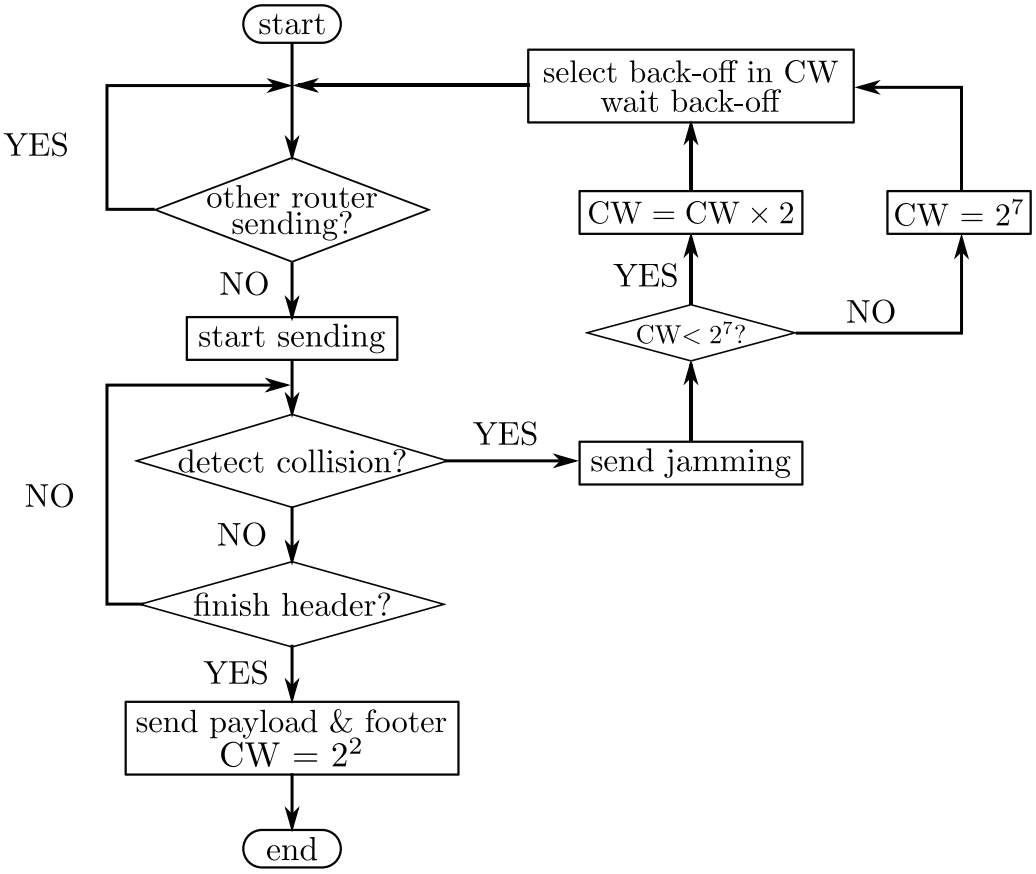


Figure 4.8: Flowchart of CSMA/CD protocol for power packet transmission.

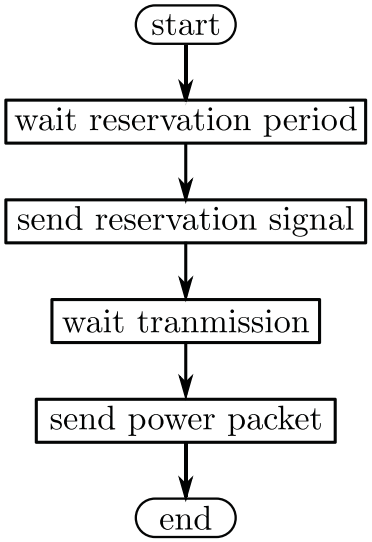


Figure 4.9: Flowchart of bit-map protocol for power packet transmission.

Table 4.3: Bit length of header signal and reservation period for adopted protocols.

Protocols	N_{H}(bit)	N_{R}(bit)
Binary countdown	$1 + 2 \times \lceil \log_2 N \rceil$	—
CSMA/CD	$1 + \lceil \log_2 N \rceil + 1$	—
Bit-map	$1 + \lceil \log_2 N \rceil$	N

the jamming signal. Such a bit is referred to as a jamming bit. It is attached to the last part of the header to notify the collision before transmitting power. This protocol will examine the effect of the randomness in the MAC protocol on the power transmission.

The bit-map protocol is the simplest one in the adopted three protocols. The flowchart of the bit-map protocol is shown in Fig. 4.9. It divides the time into a reservation period (or contention period) and a contention-free period. In the reservation period, each router reserves its power packet transmission in the next contention-free period sending a reservation signal, "1". Thus, the bit length of the reservation period must be longer than the different power packets transmitted. In the contention-free period, the routers transmit power packets following the last reservation. The reservation period and the contention-free period are repeated continuously. It is selected as a collision-free protocol.

4.2.2 Comparison of bit length

The adopted three MAC protocols work under different mechanisms. They require specific signal architectures. The header of the power packet is designed to be as short as possible to maximize the duration of power transmission. The header length N_{H} of each protocol is shown in Tab. 4.3. The header contains the start signal, the address, and the unique signal for each protocol. Here N denotes the kinds of power packets with different voltages. The first bit of the header signal is assigned to the start signal "1". The power packets must be distinguished with different addresses to avoid a short circuit. The length of the address should either be the same as or greater than $\lceil \log_2 N \rceil$ when the equal length coding is used[1]. The binary countdown protocol has the priority signal as its unique signal. Its length is the same as the address. CSMA/CD contains the jamming bit. N_{R} denotes the length of the reservation period of the bit-map protocol and is set to N bits. The bit-map protocol does not have a unique signal in the header signal.

One power packet is transmitted repeatedly as the power converter does. We assume

[1]Here, $\lceil x \rceil$ is an integer which satisfies $x \leq \lceil x \rceil < x + 1$.

Table 4.4: Bit length of intervals with adopted protocols.

Protocols	$N_\mathrm{s}(N,m)$ (bit)	$N_\mathrm{s}(8,5)$ (bit)
Binary countdown	$m \times (1 + 2 \times \lceil \log_2 N \rceil + n_\mathrm{pay} + n_\mathrm{f})$	150
CSMA/CD	$m \times (1 + \lceil \log_2 N \rceil + 1 + n_\mathrm{pay} + n_\mathrm{f}))$	143
Bit-map	$m \times (1 + \lceil \log_2 N \rceil + n_\mathrm{pay} + n_\mathrm{f}) + N$	140

m of N kinds of power packets are transmitted repeatedly. In that situation, the length of the signal is multiplied by m. We denote the bit length to send m kinds of power packets by N_s. The bit length of the payload and the footer signal are represented by n_pay and n_f, respectively. n_pay and n_f are assumed to be the same. Table 4.4 shows the general form of N_s and examples with $(N, m) = (8, 5)$. The examples are calculated by $n_\mathrm{pay} = 20$ and $n_\mathrm{f} = 3$ The general forms of N_s show that the CSMA/CD and bit-map protocol have the same N_s when $N = m$. Likewise, the binary countdown and bit-map protocols have the same N_s when $m \times \lceil \log_2 N \rceil = N$. In the case of $(N, m) = (8, 5)$, as confirmed in Tab. 4.4, the CSMA/CD protocol has the shortest N_s in them. CSMA/CD protocol is the best in the adopted protocols in terms of the bit length.

4.2.3 Simulation evaluation on power transmission

The performances of the protocols on power transmission are evaluated by simulation. We construct simulation models with five pairs of routers on MATLAB/Simulink. Fig. 4.10 shows the schematic diagram of the model. E_1 to E_5 and W_1 to W_5 are the DC sources and constant power loads (CPLs), respectively. The storage C_1 to C_5 are set at $10.0\,\mu$F. Power packets are transmitted between each pair of routers with the same subscript. The transmitted power packets are assumed to have different voltages and should be distinguished. The estimated N_s of the adopted protocols are the same as the examples by setting $N = 8$. The duration of 1 bit t_u is set at $1\,\mu$s. The power packet transmission is performed under the simple control as the same as in Sec. 3.4. A receiver router demands the power packet to the corresponding transmitter. The demand is transmitted when the storage voltage undergoes the threshold voltage V_th. In this section, we implement bidirectional routers. They do not need the demand signal like in Sec. 3.4 to achieve on-demand power packet transmission. The power flow depends on the voltage gradient and is independent of the signal transmission direction. With bidirectional routers, the on-demand power packet transmission control is achievable without additional signals.

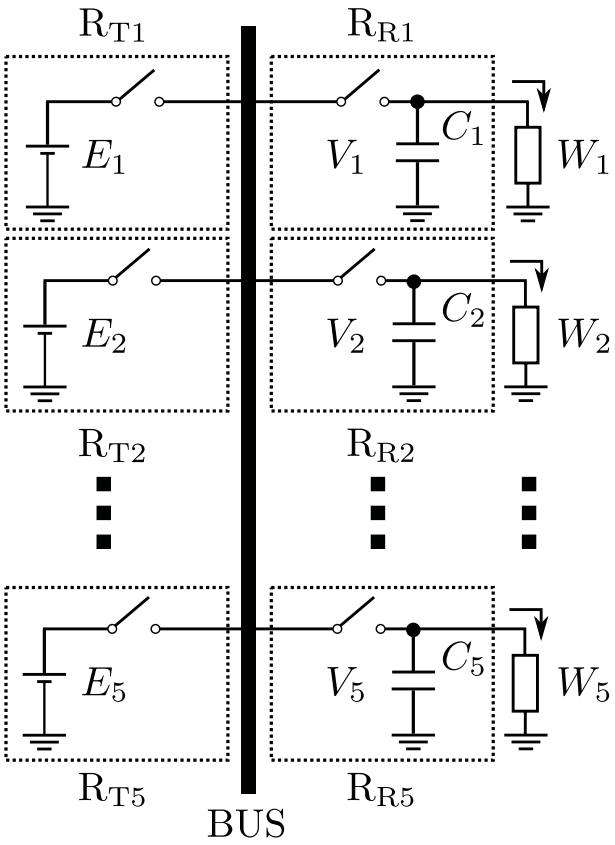


Figure 4.10: Schematic diagram of a connection with five pairs of routers.

The simulation is performed by changing V_{th} to see the effect of the control. They are given as the proportions of the corresponding storage voltages to their source voltages. The proportion was ranged from 80 to 100 %. $\mathrm{E_i}$ and $\mathrm{W_i}$ are designed so that each pair of routers have the same power transmission cycle. We compare the standardized storage voltages V_{pi}. It satisfies the following relationship

$$V_{\mathrm{pi}} = \frac{V_{\mathrm{i}}}{E_{\mathrm{i}}} \quad (\mathrm{i} = 1 \ldots 5). \tag{4.1}$$

V_{pi} keeps the relationship, when routers $\mathrm{R_{Ri}}$ receives power packets in the same cycle.

Figures 4.11 to 4.12 show the simulation results of V_{pi}. It can be seen that V_{pi} has almost the same values in Fig. 4.11. They are along with V_{lc} and V_{lp}. V_{lc} and V_{lp} are the maximum performances limited by the on-demand control and the bit length. V_{lc} is a function of the proportion of the threshold voltage to the source voltage $x(= V_{\mathrm{th}}/E)$. It is calculated by the ideal voltage waveform of the storage. When the control works perfectly, the storage is charged up to the source voltage by receiving the payload. Then,

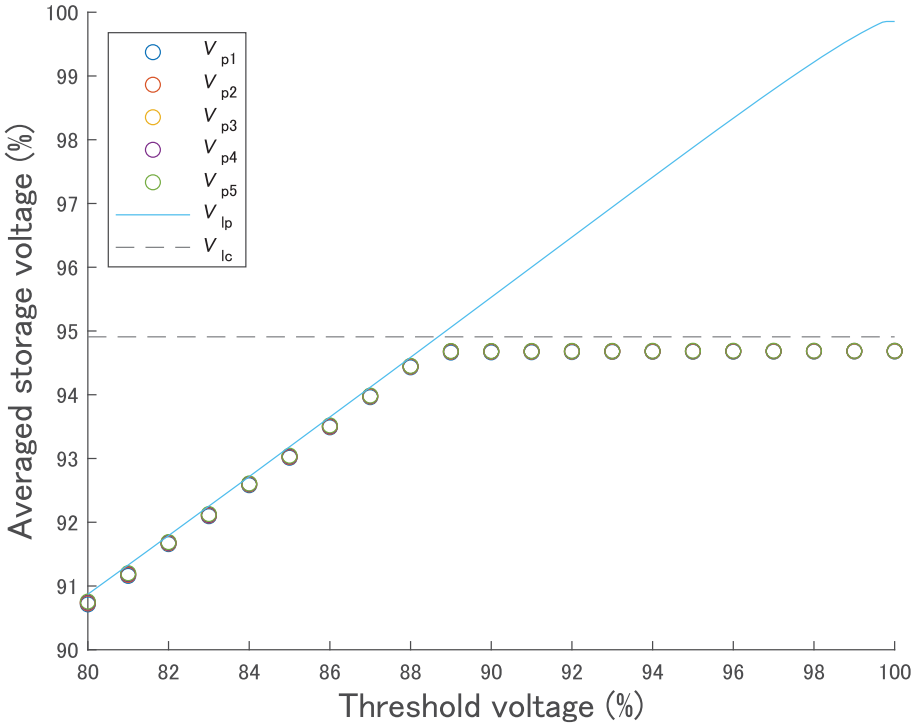


Figure 4.11: Simulation results of V_{pi} with binary countdown protocol.

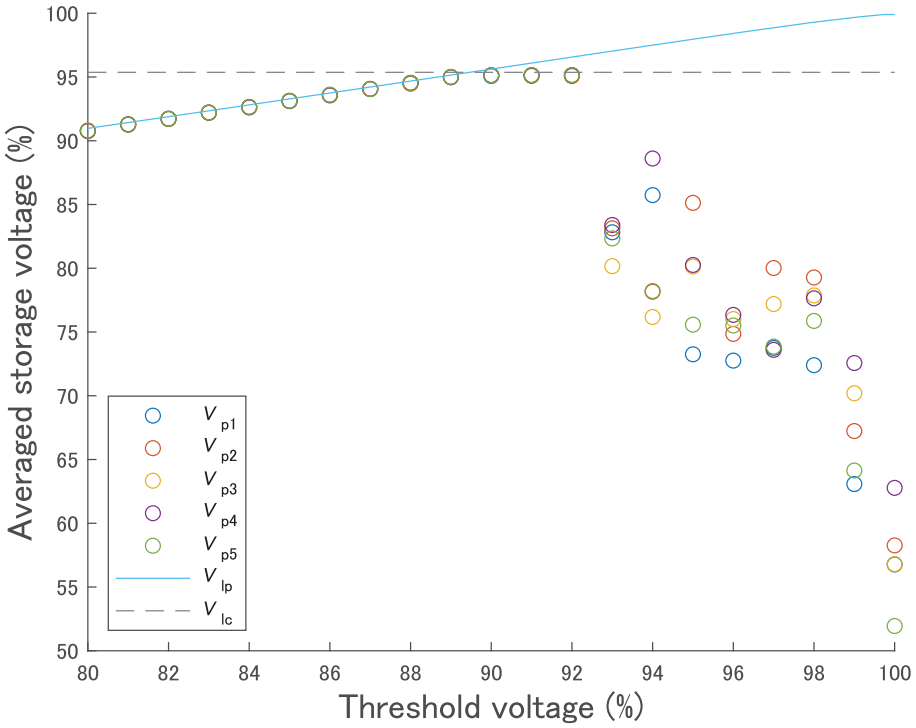


Figure 4.12: Simulation results of V_{pi} with CSMA/CD protocol.

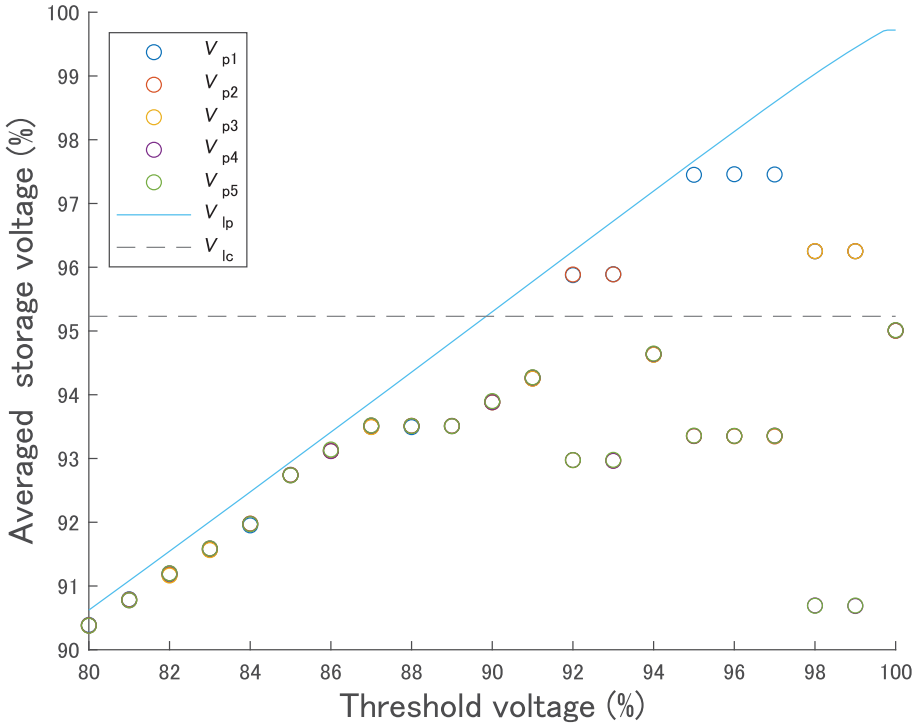


Figure 4.13: Simulation results of V_{pi} with bit-map protocol.

Table 4.5: The proportion V_{lp} of V_{ai} to E_{i}.

Protocols	Proportion
Binary countdown	94.9 %
CSMA/CD	95.4 %
Bit-map	95.2 %

the storage voltage decreases to V_{th} as the load consumes the stored energy. V_{lc} is derived from the situation and described as

$$V_{\mathrm{lc}} = \frac{t_{\mathrm{u}} n_{\mathrm{pay}} + \frac{2}{3} T_{\mathrm{E}} \left\{ 1 - \left(x^2 + \frac{t_{\mathrm{u}} N_{\mathrm{H}}}{T_{\mathrm{E}}} \right)^{\frac{3}{2}} \right\}}{t_{\mathrm{u}} n_{\mathrm{pay}} + (1 - x^2) T_{\mathrm{E}} + t_{\mathrm{u}} N_{\mathrm{H}}}. \tag{4.2}$$

Here, T_{E} satisfies

$$T_{\mathrm{E}} = \frac{1}{2} \frac{C_{\mathrm{i}} E_{\mathrm{i}}^2}{W_{\mathrm{i}}}. \tag{4.3}$$

V_{lp} is decided by N_{s}. It shows the maximum V_{pi} when the power packets are densely transmitted. V_{lp} is calculated as Tab. 4.5 from the setup.

Figure 4.11 indicates that the binary countdown protocol can always achieve the best performance in the evaluated range. When the threshold voltage is higher than 90 %,

V_{pi} is around 94.7 %. The value is slightly below the calculated value of 94.9 %. This difference, which also occurs in the results of other protocols, is due to the on-resistance of the switch.

V_{pi} does not always have similar values in Figures 4.12 and 4.13. CSMA/CD protocol has a random back-off time. The randomness makes the V_{pi} have different values for threshold voltages higher than 93 %, as shown in Fig. 4.12. The frequent collision elongates CW and reduces the storage voltage. In this range, it is challenging to keep the power supply. CPLs sometimes stop their operations due to low storage voltages. The transmission interval can be almost the same in the case where the collision rarely occurs. When the threshold voltage is less than or equal to 92 %, V_{pi} has similar values around V_{lc} or V_{lp}. It indicates that the power packet transmission is conducted without collision in the range. V_{pi} with CSMA/CD protocol in the range is higher than that with another protocol.

In Fig. 4.13, when the threshold voltages are 98 and 99 %, $V_{\mathrm{p1}}, V_{\mathrm{p2}}$, and V_{p3} are higher than V_{p4}, V_{p5}, and V_{lp}. This is because $\mathrm{R_{R1}}$, $\mathrm{R_{R2}}$, and $\mathrm{R_{R3}}$ can reserve the transmission every reservation period, while others can reserve once every two or more reservation periods. The continuous repetition of the reservation and contention-free periods makes the reservation period too early for $\mathrm{R_{R4}}$ and $\mathrm{R_{R5}}$ to reserve every time. Likewise, $\mathrm{R_{R1}}$ can reserve every time for the threshold voltage 95–97 %. The fairness of PPT is not kept at 1 despite the setup. In the 94 % threshold case, all routers reserve once every two reservation periods. Thus, V_{pi} have almost the same values but are lower than V_{lp}. It indicates that avoiding the collision of signals increases the interval in some situations. A similar situation can be seen when the threshold voltage is less than 94 %. The difference in the values of the V_{pi} can be solved with control. A predictive control, for instance, can achieve a looking-ahead reservation based on the estimated storage voltage at the future transmission.

4.3 Summary

In this chapter, we examined the power packet transmission and control between routers. The half-duplex power packet transmission was verified by the experiment. The half-duplex transmission requires a protocol to prevent the collision of power. A MAC protocol was proposed based on the binary countdown protocol in information networks.

Two routers connected to the same power line transmitted demands signals alternately under the protocol. The experimental results show that the proposed protocol is valid in collision avoidance.

Based on the verified bidirectional transmission, we considered the multidirectional transmission. The multidirectional transmission can improve power transmission efficiency. One concern is the increase in the length of the signal. To see the influence of the increased signal length, we built simulation models and evaluated the performance of the protocol. Two additional protocols, the bit-map and CSMA/CD protocols, were also implemented to the power packet transmission. They serve the same function but follow different mechanisms. Comparing their performances, we evaluated MAC protocols. The evaluation of the bit length showed that the CSMA/CD protocol has the shortest signal. The bit-map and binary countdown protocols follow it. In the evaluation of power transmission, the binary countdown protocol was found to provide the best performance when collisions of power packets frequently occur. The best performance is decided by the configuration of the signal and the control. The results indicate that the appropriate protocol can decrease the time to transmit information and increase the time to transmit power.

The required bit length was discussed in Chapters 3 and 4. The length of the signal depends on the kinds of power packets to distinguish and the protocol. When the route of power packet transmission is given, the required amount of information can be calculated by the results of this chapter. Then, we look into the power transmission from the source to the load in the following two chapters.

Chapter 5

Output voltage of power packet dispatching system

We focus on the power transmission from the sources to the loads. The power transmission characteristics of the system have been studied numerically with the consensus dynamics [69–73]. The circuit has similar circuit configuration to the LC ladder circuit. The frequency response of the ladder circuit is studied [74–76]. However, the discontinuous pulse transmission is not studied in detail. In this chapter, we examine the output voltage of the network. The experimental results in Chapter 4 indicate that the output and the storage voltages depend on the connections of routers. In addition, the output of the network has been controlled by pulse width modulation (PWM) and pulse density modulation (PDM) controls. We assume PWM control and examine the connection dependency of the output. The examination is started from the smallest network. The smallest power packet dispatching network is compared with the buck converter. The results indicate that the circuit in the network can be analyzed as an RLC filter. With the overdamped condition, the output of the network monotonically increases as the pulse width increases. Then, we consider a cascaded network with three routers. The connection of the router is another control variable in the network. The experiment and the corresponding simulation examine the output.

5.1 One-to-one connection

The smallest power packet dispatching network is a one-to-one network. The circuit configuration of the smallest network is shown in Fig. 5.1a. The power line is shown as an inductor in Fig. 5.1a. The modeling is valid in the short-range power transmission

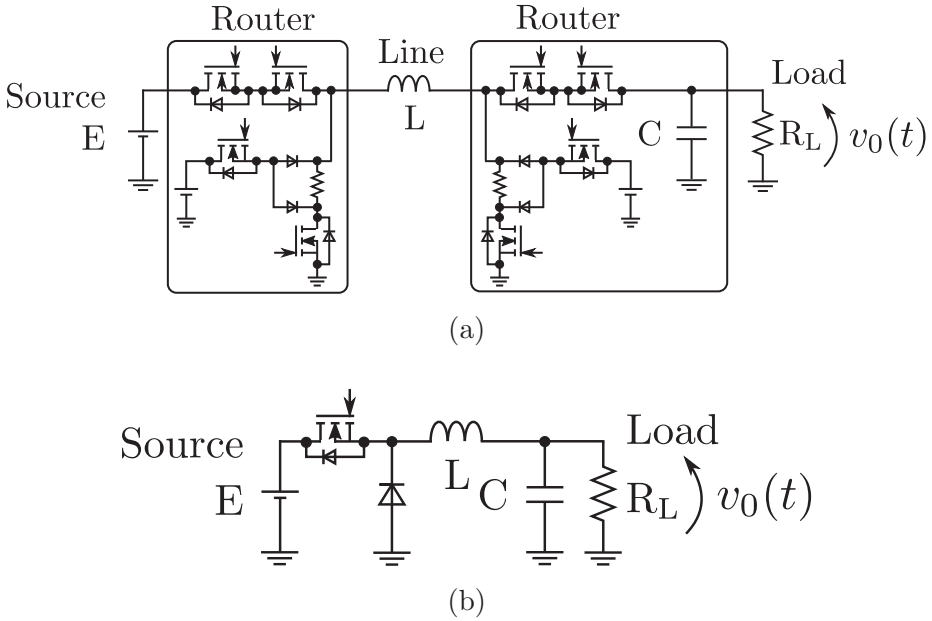


Figure 5.1: Circuit diagrams of (a) the smallest power packet dispatching network and (b) buck converter. In (a), signal units are not shown for simplicity.

compared to the wavelength of the voltage waveform. It is a similar circuit configuration to the buck converter shown in Fig. 5.1b. The buck converter operates in a continuous conduction mode (CCM) or a discontinuous conduction mode (DCM) depending on the inductor current. In the DCM, the inductor current does not always flow. The power packet dispatching network uses TDM to transmit both power and information. Thus, the smallest power packet dispatching network is expected to have similar output characteristics to the buck converter operating in DCM.

5.1.1 Circuit analysis based on filter theory

Based on the buck converter, we design the capacity of the storage for the power packet dispatching system. In the buck converter design, the RLC filter is designed to smooth the rectangle input. The RLC filter in the power packet dispatching network consists of the on-resistances of the switches, the parasitic resistances, the power line inductance, and the storage capacitance. R includes the equivalent series resistance of the storage $R_{\rm esr}$ and the on-resistance of the switches $R_{\rm on}$. When the storage is a multilayer ceramic capacitor (MLCC), $R_{\rm esr}$ is in the range of some hundreds of mΩ. In the case of aluminum electrolyte capacitors, it is around several Ω. The switch is SCT3022AL [77]. The typical

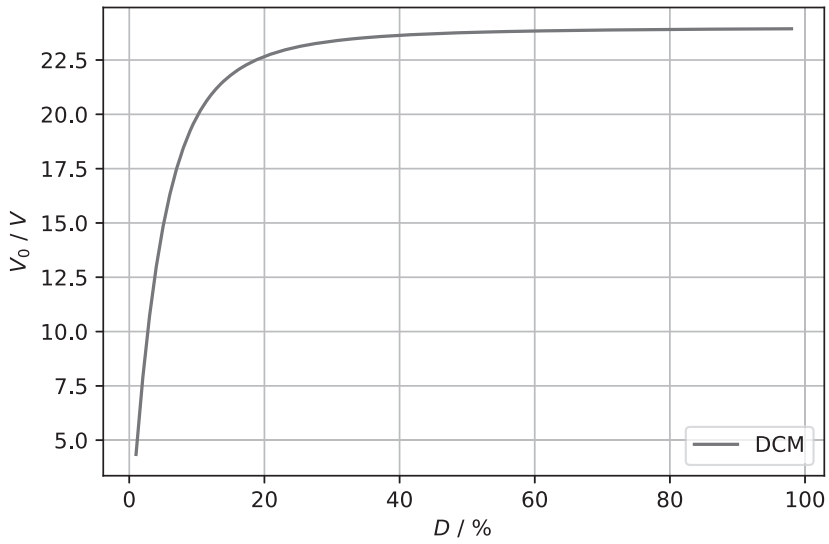


Figure 5.2: Averaged output voltage of buck converter operating in DCM. The value is calculated by Eq. (5.2) with $E = 24\,\mathrm{V}$, $L = 10\,\mu\mathrm{H}$, $\mathrm{R_L} = 100\,\Omega$, and $T_\mathrm{s} = 100\,\mu\mathrm{s}$.

value of R_on is $25\,\mathrm{m}\Omega$ [57]. The value of L is given as the equivalent inductance of the power line. It implies that the value is pre-defined by the spatial restrictions of the actual applications. This paper assumes the small community and/or in-home power distribution as applications. The length of the line is assumed to be less than 10 m. When the power line is the 1.6 mm two core vinyl insulated vinyl sheathed flat-type (VVF) cable[1], which is popular in Japan for in-home power distribution, the value of L is about 500 nH/m. These values are assumed to be used in the frequency band considered in this study. The storage capacitance is designed from these values. Its capacitance is selected to satisfy the overdamping condition of an RLC filter. The condition is widely used in the converters. The condition is given by

$$C \geq \frac{4L}{R^2}. \tag{5.1}$$

Therefore, the capacitance is estimated in the range of several μF to mF.

The averaged output voltage V_0 of a buck converter operating in DCM is given by Eq. (5.2) [78]

$$V_0 = \frac{2D\mathrm{E}}{D + \sqrt{D^2 + 8L/\mathrm{R_L}T_\mathrm{s}}}. \tag{5.2}$$

Here, E, $D, \mathrm{R_L}, T_\mathrm{s}$ represent the source voltage, duty cycle, load resistance, and switching

[1] Also called Polyvinyl chloride (PVC) cable. The rating current of 1.6 mm 2 core VVF cable is 15 A.

Table 5.1: Simulation setup.

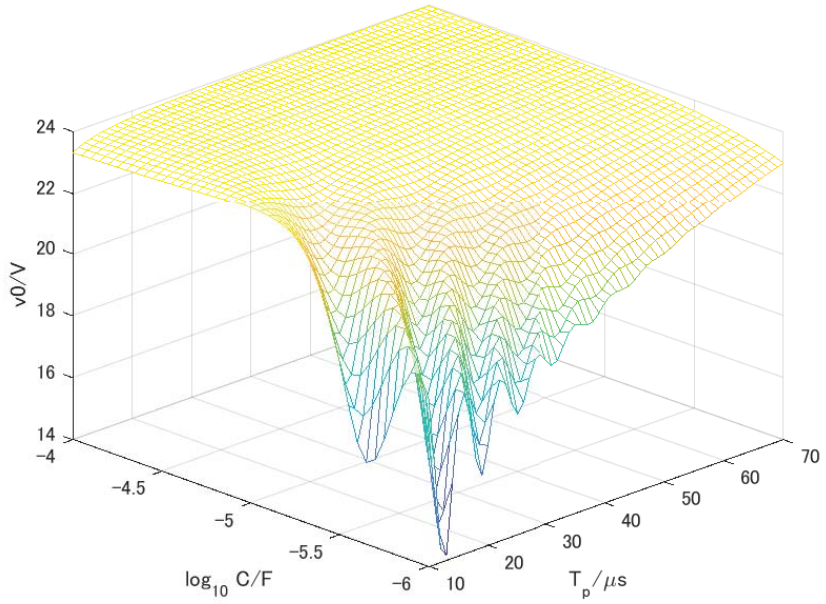
Name	Symbol	Value
Source voltage	E	24 V
Load resistance	R_L	100 Ω
Storage ESR	R_{esr}	100 mΩ
On resistance	R_{on}	25 mΩ
Line inductance	L_0	1.0 μH
Switching cycle	T_s	100 μs

cycle, respectively. Equation (5.2) is valid when the fluctuation of the output voltage is negligible. Figure 5.2 shows an example of the output voltage characteristics of the buck converter operating in DCM. The circuit constants are set at E = 24 V, L = 10 μH, and R_L = 100 Ω. The PWM control is assumed, then the switching period T_s is set at 100 μs. As Fig. 5.2 shows, the output voltage monotonically increases with the duty cycle. The monotonical characteristics simplify the output control.

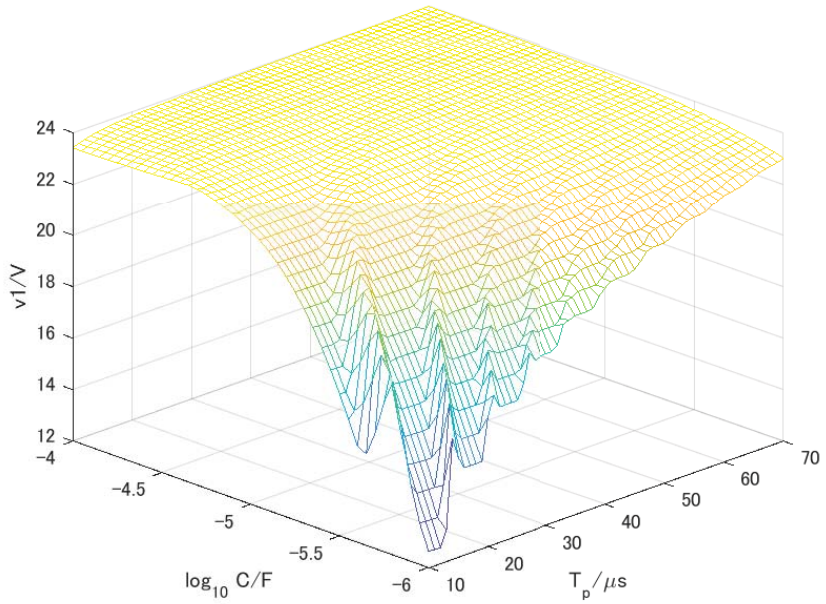
5.1.2 Simulation

We compare the outputs of the one-to-one network and the buck converter operating in DCM to verify the analysis above. The simulation was performed on MATLAB/Simulink. Based on the description above, the circuit constants are decided. The constants are tabulated in Tab. 5.1. In the simulation, the pulse width T_p and the storage capacitance C are taken as parameters. The simulation was run for 100 ms. The simulation time was long enough for the model to get periodically stable states. The last two periods were used to calculate the averaged output voltage V_0.

Figure 5.3 shows the simulation results of the one-to-one network and the buck converter. Their V_0 have quite similar characteristics against parameters. The estimated monotonical characteristics are seen when C is larger than 44 μF. The value is numerically in a good match with the estimated 40 μF. The results show that the capacitor design based on the filter theory can be applied to the power packet dispatching network.



(a)



(b)

Figure 5.3: Simulation results of (a) the one-to-one network and (b) buck converter.

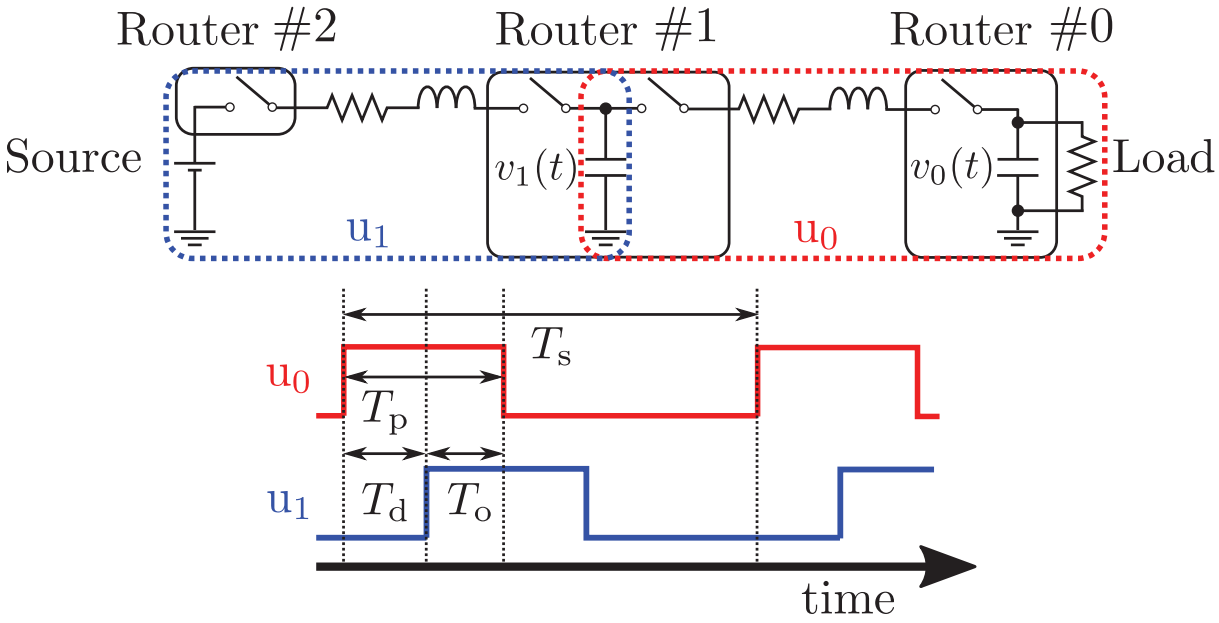


Figure 5.4: Cascaded router network with three routers and their switching functions.

5.2 Cascaded network

We examine the output of the cascaded network. The cascaded connection always appears on the power transmission from the source to load. When there are connected more than three routers in the network, the power transmission on each pair of the routers follows the specific switching function. Figure 5.4 shows the circuit diagram of the cascaded three routers with one source and one load. The switching function u_0 (u_1) decides the connection between Router #0 – #1 (#1 – #2). u_0 and u_1 decide the temporal and spatial energy flow in the network. In general, they can follow the different modulation methods and have independent switching and duty cycles. This paper assumes that they follow PWM and have the same T_p and T_s of 100 μs for simplicity. In this case, the control parameters of the power transmission are the duty cycle D and the time difference T_d between the rising edges of u_0 and u_1. Here, D is proportional to T_p since T_s is fixed under PWM control. T_o represents the duration when both u_0 and u_1 are ON. The averaged storage voltages V_0 and V_1 can be calculated in one switching cycle. The output voltages against T_p and T_d are measured by the experiment.

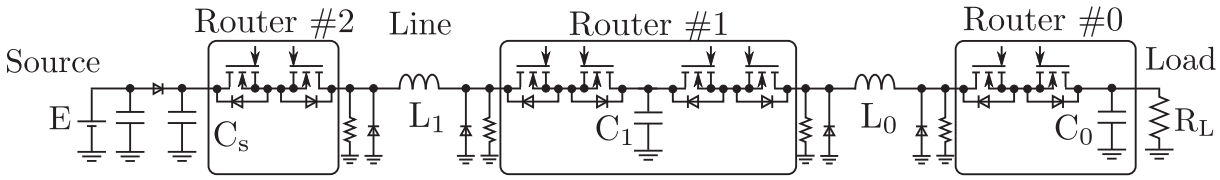


Figure 5.5: Experimental circuit diagram of cascaded network with three routers.

Table 5.2: Experimental setup.

Name	Symbol	Value
Source voltage	E	24 V
Load resistance	R_L	100 Ω
Storage capacitance	C_0, C_1	40 μF
Line length	L_0, L_1	1.0 m
Switching cycle	T_s	100 μs

5.2.1 Experiment

Figure 5.5 shows the circuit diagram of the experimental system. The details of the router are described in Chapter 2. Instead of the signal unit, diodes and resistors of 1.0 kΩ are implemented on the ports of the router. In this experiment, the payload is transmitted without the header and footer signals. It will not lose the physical validity. A single FPGA controls the whole experimental system. Thereby the information part of the power packet is not necessary for this experiment. MLCCs are implemented as storage. Their ESR is in the order of 100 mΩ at the frequency band for the experiment. The diode and capacitors of 10 μF (C_s) implemented between the power source and router block the reverse current to the source and compensate for the power supply. The circuit parameters are shown in Tab. 5.2. The storage capacity follows the designed value in Sec. 5.1. PWM control is adopted. T_s is set at 100 μs. In the power packet dispatching network, many power packets with different voltages can share the power line. One kind of power packet can use the power line for a limited duration. Thus, T_p is changed from 10 to 70 μs. The power line is a 2-core VVF cable with a core wire diameter of 1.6 mm. The storage voltages $v_0(t)$ and $v_1(t)$, and the power line voltage $v_{l0}(t)$ and $v_{l1}(t)$ are measured.

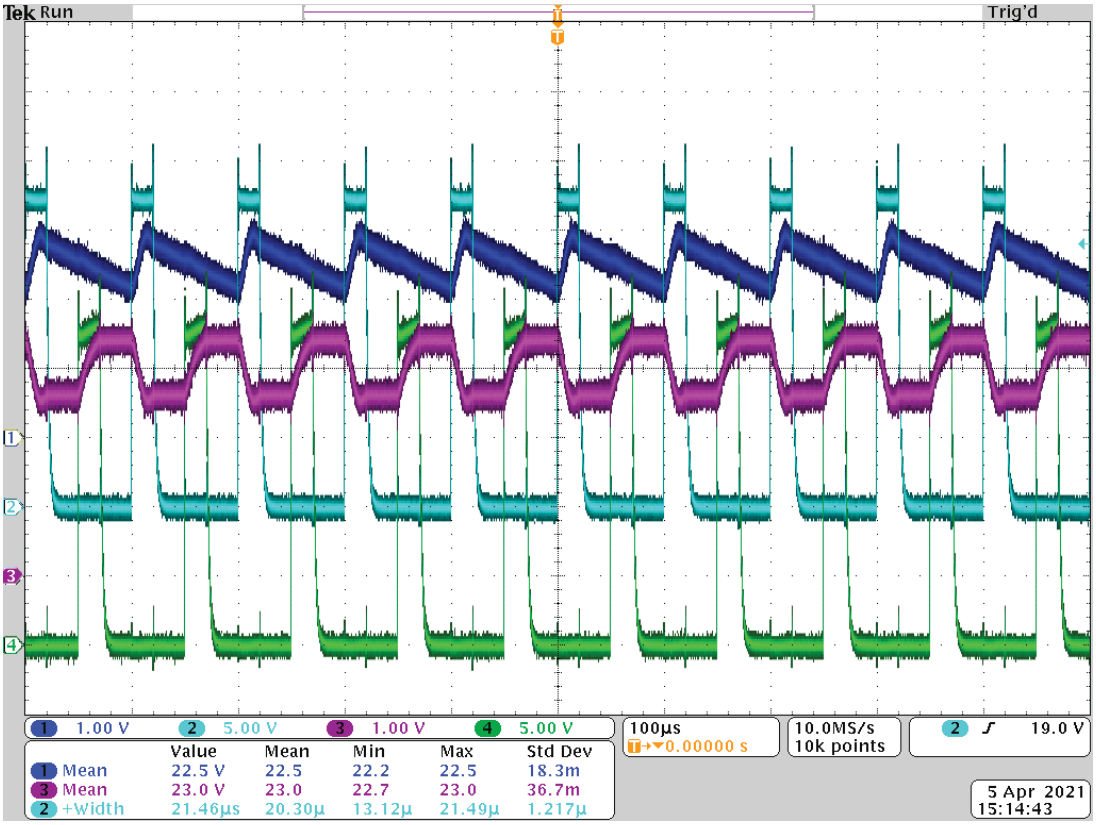
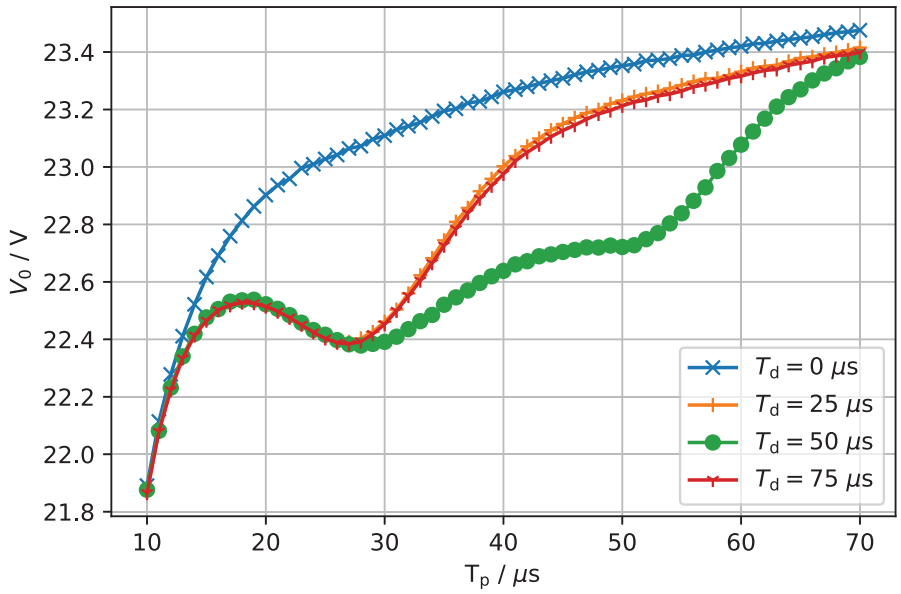


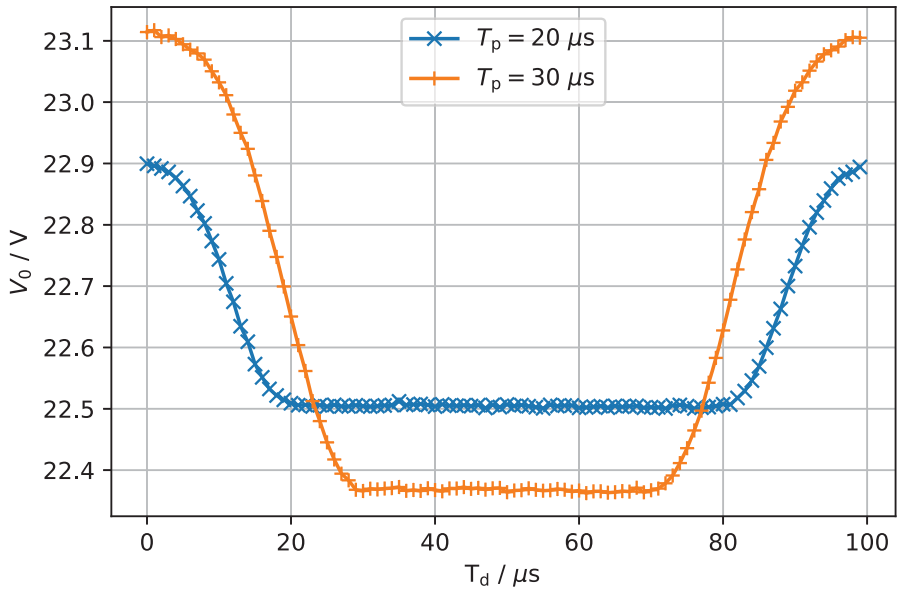
Figure 5.6: Experimental voltage waveforms when $T_\mathrm{p} = 21\,\mu$s and $T_\mathrm{d} = 50\,\mu$s. $v_0(t)$ (CH1) and $v_1(t)$ (CH3) show the voltage of the storages with the offset of 20.0 V. $v_{l0}(t)$ (CH2) and $v_{l1}(t)$ (CH4) show the voltage of the power lines.

5.2.2 Experimental results

Figure 5.6 shows the examples of the voltage waveforms of $v_0(t)$ (CH1), $v_1(t)$ (CH3), $v_{l0}(t)$ (CH2), and $v_{l1}(t)$ (CH4). $v_0(t)$ and $v_1(t)$ are measured with the offset of 20.0 V. The averaged voltages V_0 and V_1 are calculated from $v_0(t)$ and $v_1(t)$. The measured voltages are periodically stable. Their periods are the same as T_s. Figure 5.7 shows V_0. Figures 5.7a and 5.7b show V_0 against T_p and T_d, respectively. V_0 monotonically increases by T_p at $T_\mathrm{d} = 0\,\mu$s. It indicates that the designed storage capacity was sufficiently large to obtain the monotonical increase. In the other cases, V_0 does not always show the monotonical increase to T_p. In the cases, V_0 increases after T_p becomes longer and u_0 overlaps u_1. Thus V_0 behaves similarly when $T_\mathrm{d} = 25$ and $75\,\mu$s. Figure 5.7b confirms that V_0 is symmetric with $T_\mathrm{d} = 50\,\mu$s. The averaging calculation mitigates the difference among the voltage waveforms of $v_0(t)$ when $T_\mathrm{d} = 25$ and $75\,\mu$s. It means that T_o affects V_0 due to averaging.



(a)



(b)

Figure 5.7: Experimental results. (a) and (b) show the V_0 against T_p at $T_d = 0, 25, 50,$ and $75\,\mu$s, and T_d at $T_p = 20$ and $30\,\mu$s, respectively.

These results indicate that V_0 at $T_\mathrm{d} = 50\,\mu$s shows the lowest case. It agrees with natural speculations.

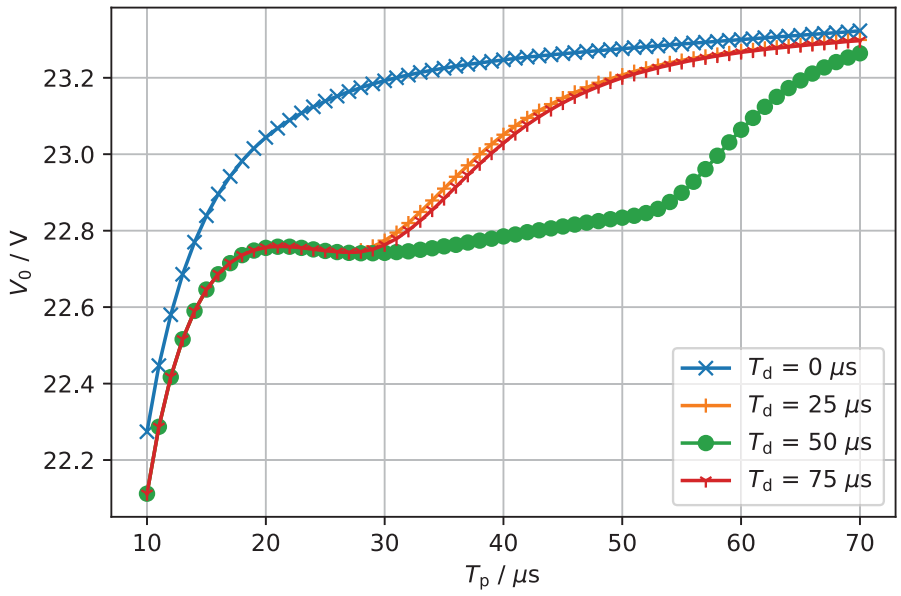
T_d affects the output power. When T_o is 0, the power is kept in the network. The length of T_d does not affect the output within $T_\mathrm{o} = 0$. The power packet dispatching network uses the line to the communication, too. Thus, the time to transmit power should be shortened as long as the sufficient power supply is achieved. In that sense, the power flow control in the network should increase T_o first rather than T_p. The application of the methods in communication such as routing protocols will help increase the output.

5.3 Simulation

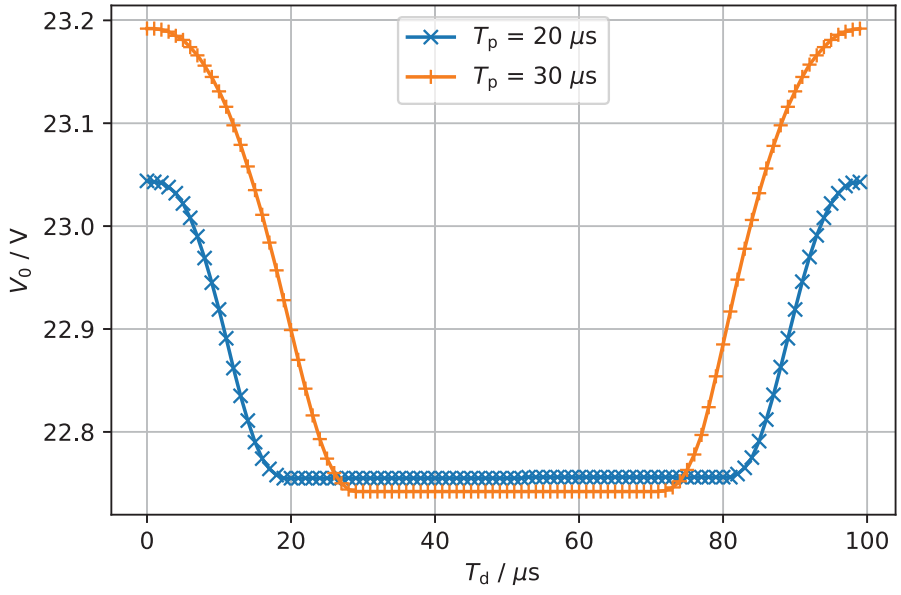
The experimental results are verified in the simulation. As performed in Sec. 5.1.2, the simulation model was built on MATLAB/Simulink. The circuit parameters are set at the same values on Tab. 5.1. T_p and T_d are changed in the same range as the experiment. The simulation was executed for 100 ms, and the averaged output V_0 was calculated from the last two periods.

Figure 5.8 shows the simulation results. They are in a good match with the experimental results in Figures 5.8a and 5.8b. It is qualitatively seen in the inflection points of V_0. For example, V_0 decreases when T_p is between 19 to 28 μs. The simulation results have higher V_0 than the experimental results. The dynamical characteristics of MOSFETs and MLCC are the reasons. When T_p is short, the switching dynamics of MOSFETs have larger impacts on the results. It results in the low V_0 in the experiment, especially when T_p is shorter than 20 μs. In addition, MLCC decreases its capacitance with DC voltage bias. It is not modeled in the simulation and thought to be a cause of the low V_0 in the experiment.

There are found a good match between the experiment and the simulation. We conduct simulations to examine the effects of the circuit parameters. The line inductances and storage capacitances are changed to see their effects. The line inductances are changed to L_0 =1.0 μH and L_1 = 5.0 μH. The storage capacitances are set at 40.0 μF in case 1 and 10.0 μF in case 2. The other circuit constants are the same in Tab. 5.1. Figure 5.9 shows the simulation results of V_0. In case 1, V_0 increases monotonically at T_d = 25 and 75 μs. The storage capacitances of 40.0 μF are not large enough to make V_0 increase monotonically when L_1 = 1.0 μF. By setting L_1 = 5.0 μF, the simulation model satisfies

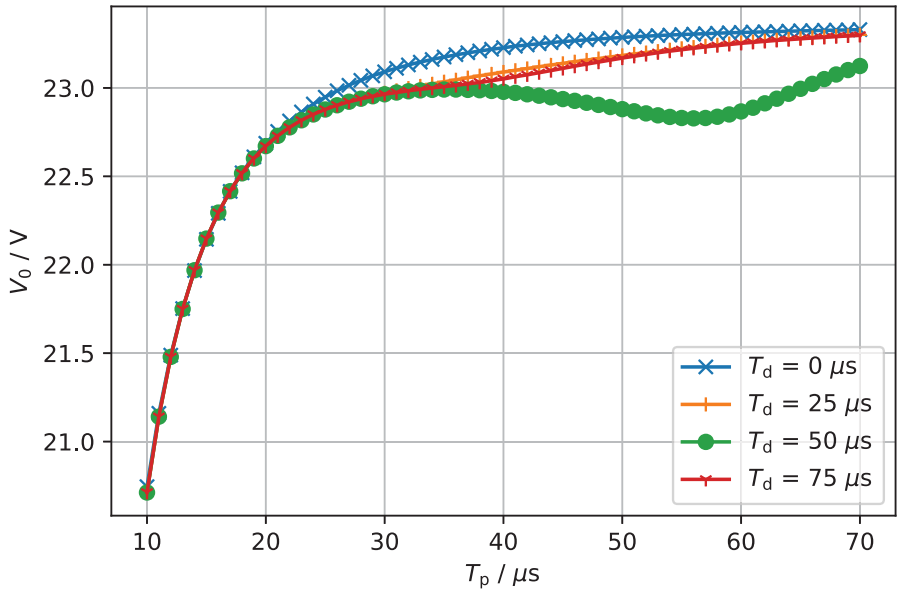


(a)

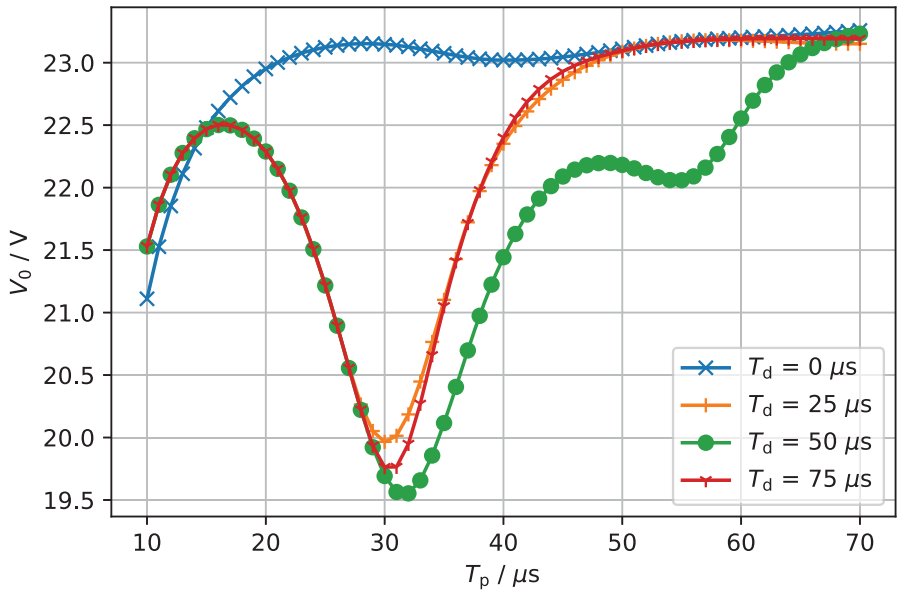


(b)

Figure 5.8: Simulation results. (a) and (b) show V_0 against T_p at $T_\mathrm{d} = 0, 25, 50$, and $75\,\mu$s, and T_d at $T_\mathrm{p} = 20$ and $30\,\mu$s, respectively.



(a)



(b)

Figure 5.9: Simulation results with different inductances. (a) shows V_0 when 40 μF capacitors are used as the storage (b) 10 μF capacitors.

the overdamped condition. When the model satisfies the underdamped condition, V_0 does not show a monotonical increase with T_p. The most crucial point is that the case of $T_\mathrm{d} = 0\,\mu$s. $T_\mathrm{d} = 0\,\mu$s is not always the best condition to get the highest V_0 in Fig. 5.9b. At the condition, V_0 with $10\,\mu$F capacitors is higher than $40\,\mu$F capacitors. These results indicates that the underdamped condition has an advantage in transmitting power in a short time. If the sufficient power supply is achievable with the underdamped condition, the time to communication increases in the power packet dispatching system. In addition, the condition $T_\mathrm{o} = 0\,\mu$s is expected to be easier to achieve than $T_\mathrm{d} = 0\,\mu$s.

5.4 Summary

This chapter examined the output voltage on the cascaded power packet dispatching network. The connections of the routers are additional control parameters of the network compared to the converters. In addition to the pulse width, the connection dependency of the output was examined in the experiment and the simulation.

Firstly, the network with a single connection was analyzed, compared with the buck converter operating in DCM. The simulations were performed to compare their outputs. Based on the similarity of the current waveforms between the power packet transmission and the buck converter which is operating in DCM, the experimental system could be designed as an RLC filter. Second, we examined the network of cascaded three routers with one source and one load. The designed capacity of the storage was large enough to obtain the monotonical characteristics of V_0 in the cascaded network at $T_\mathrm{d} = 0\,\mu$s. In other cases, V_0 did not show the monotonical increase with T_p. From the T_d characteristics, it was shown that V_0 depends only on T_o. The conjecture was also verified in the simulation. Finally, we examined the effects of circuit parameters by the simulation. The line inductance and storage capacitances were included. The results indicated that $T_\mathrm{d} = 0\,\mu$s does not always give the highest V_0. It shows that the underdamped condition and $T_\mathrm{o} = 0\,\mu$s are suitable for the power packet transmission in terms of the time duration for power transmission.

Chapter 6

Analytical method of voltage estimation and design

Chapter 5 concludes that a one-to-one connection and underdamped responses of the circuit are suitable for power transmission in a short duration. Based on the results, we propose a feasible design of the power packet dispatching system. Here, we focus on the connection and response above. The response had lower output compared to the over-damped responses in many cases in Chapter 5. From the viewpoint of circuit design, low outputs have a beneficial aspect for guaranteeing the output. In the following, we analyze and verify the payload transmission on a one-to-one connection with an underdamped condition. Then, the power packet dispatching system is analyzed. The analysis gives a voltage estimation method without the simulation. The method is combined with the results of the dissertation, and a feasible design of the system is proposed.

6.1 Power transmission with underdamped pulse

6.1.1 Theoretical analysis

A concept of the power packet routing between a source and a load is shown in Fig. 6.1. Routers connect a source and a load with a cascaded topology. A connection j ($= 0, 1, \ldots,$ N-1) consists of routers # j, # j+1, and the power line L_j. Router # j has a capacitor C_j as storage. Router # N is directly connected to the source and does not have storage. L_j also shows the self-inductance of the line. The current on L_j is represented by $i_j(t)$. r_j shows C_j's equivalent series resistance (ESR). Here we assume that the power packet follows the hop-by-hop routing; that is, each router connects to a single neighboring router

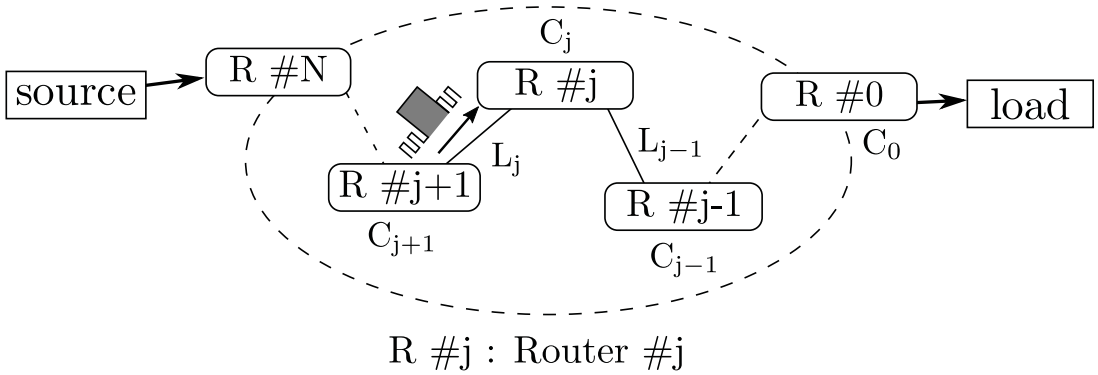


Figure 6.1: Concept of power packet routing in power packet dispatching system.

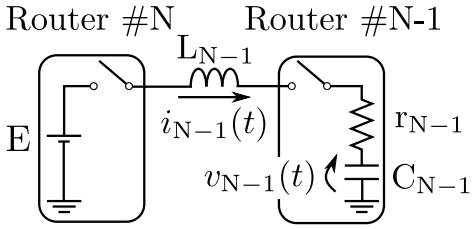


Figure 6.2: Schematic of a connection between a router and a source.

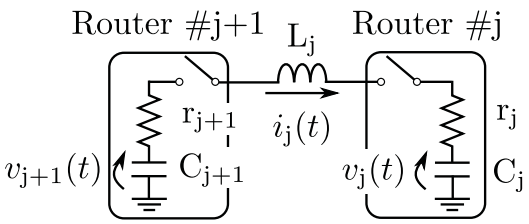


Figure 6.3: Schematic of a connection between two routers.

at one time [1]. In that case, a power packet transmission can be analyzed with the two relevant routers. The circuits relevant to the power transmission are classified into the two patterns shown in Figs. 6.2 and 6.3. The two circuits are analyzed in the following.

Figure 6.2 shows the connection with a source. It has a similar circuit configuration to a buck converter. The power line, storage, on-resistance of the switch, and parasitic resistances form an RLC filter. In this dissertation, we consider ESR of the storage capacitor as a parasitic component. Thus, the differential equations of Fig. 6.2 are written as follows,

$$\mathrm{C_{N-1}}\frac{\mathrm{d}v_{\mathrm{N-1}}(t)}{\mathrm{d}t} = i_{\mathrm{N-1}}(t), \tag{6.1}$$

$$(2\mathrm{r_{on}} + \mathrm{r_{N-1}})i_{\mathrm{N-1}}(t) + \mathrm{L_{N-1}}\frac{\mathrm{d}i_{\mathrm{N-1}}(t)}{\mathrm{d}t} = \mathrm{E} - v_{\mathrm{N-1}}(t). \tag{6.2}$$

Where E denotes the voltage of the source and $\mathrm{r_{on}}$ corresponds to the on-resistances of the switch. The payload transmission should be analyzed as the step input. The step response of the RLC filter is roughly divided into overdamped and underdamped responses. This chapter adopts the underdamped condition in the following. We set $t = 0$ to be the

[1] The payload transmission on the connections of three routers is analyzed in Sec. A.1

beginning of the payload transmission. Given the initial condition, $i_{\mathrm{N}-1}(t)$ is shown as follows,

$$i_{\mathrm{N}-1}(t) = \frac{\mathrm{E} - v_{\mathrm{N}-1}(0)}{\mathrm{L}_{\mathrm{N}-1}\omega_{\mathrm{N}-1}\sqrt{1-{\zeta_{\mathrm{N}-1}}^2}} \exp(-\zeta_{\mathrm{N}-1}\omega_{\mathrm{N}-1}t)\sin(\omega_{\mathrm{N}-1}\sqrt{1-{\zeta_{\mathrm{N}-1}}^2}t). \tag{6.3}$$

Here, $\zeta_{\mathrm{N}-1}$ and $\omega_{\mathrm{N}-1}$ are

$$\zeta_{\mathrm{N}-1} = \frac{2\mathrm{r_{on}} + \mathrm{r}_{\mathrm{N}-1}}{2}\sqrt{\frac{\mathrm{C}_{\mathrm{N}-1}}{\mathrm{L}_{\mathrm{N}-1}}}, \tag{6.4}$$

$$\omega_{\mathrm{N}-1} = \frac{1}{\sqrt{\mathrm{L}_{\mathrm{N}-1}\mathrm{C}_{\mathrm{N}-1}}}. \tag{6.5}$$

The underdamped condition is satisfied when $\zeta_{\mathrm{N}-1} < 1$. Equation (6.3) shows that $i_{\mathrm{N}-1}(t)$ oscillates at the frequency of $\omega_{\mathrm{N}-1}\sqrt{1-{\zeta_{\mathrm{N}-1}}^2}$. With the underdamped response, the current takes zero at $T_{\mathrm{N}-1,n} = n\pi/\omega_{\mathrm{N}-1}\sqrt{1-{\zeta_{\mathrm{N}-1}}^2}$. Turning off the switches at $T_{\mathrm{N}-1,n}$, we can end the power transmission with zero current. This study uses $n = 1$ in the following. It is because the reverse current during $T_{\mathrm{N}-1,2m-1}$ to $T_{\mathrm{N}-1,2m}(m \in \mathbb{N})$ decreases the storage voltage and increases the conduction loss. The zero current condition is ideal for suppressing the surge voltage and current. The storage voltage at $T_{\mathrm{N}-1,1}$ is

$$v_{\mathrm{N}-1}(T_{1,1}) = v_{\mathrm{N}-1}(0) + (\mathrm{E} - v_{\mathrm{N}-1}(0))\left\{1 + \exp\left(-\frac{\zeta_{\mathrm{N}-1}\pi}{\sqrt{1-{\zeta_{\mathrm{N}-1}}^2}}\right)\right\}. \tag{6.6}$$

Figure 6.3 shows a connection between two routers in the network. The differential equations are

$$\mathrm{C_j}\frac{\mathrm{d}v_{\mathrm{j}}(t)}{\mathrm{d}t} = i_{\mathrm{j}}(t), \tag{6.7}$$

$$\mathrm{C}_{\mathrm{j}+1}\frac{\mathrm{d}v_{\mathrm{j}+1}(t)}{\mathrm{d}t} = -i_{\mathrm{j}}(t), \tag{6.8}$$

$$(2\mathrm{r_{on}} + \mathrm{r}_{\mathrm{j}+1} + \mathrm{r_j})i_{\mathrm{j}}(t) + \mathrm{L_j}\frac{\mathrm{d}i_{\mathrm{j}}(t)}{\mathrm{d}t} = v_{\mathrm{j}+1}(t) - v_{\mathrm{j}}(t). \tag{6.9}$$

We assume that $i_{\mathrm{j}}(t)$ is plus when it flows from $\mathrm{C}_{\mathrm{j}+1}$ to $\mathrm{C_j}$. The current is calculated as,

$$i_{\mathrm{j}}(t) = \frac{v_{\mathrm{j}+1}(0) - v_{\mathrm{j}}(0)}{\mathrm{L_j}\omega_{\mathrm{j}}\sqrt{1-{\zeta_{\mathrm{j}}}^2}} \exp(-\zeta_{\mathrm{j}}\omega_{\mathrm{j}}t)\sin(\omega_{\mathrm{j}}\sqrt{1-{\zeta_{\mathrm{j}}}^2}t). \tag{6.10}$$

Here, ζ_{j} and ω_{j} are

$$\zeta_{\mathrm{j}} = \frac{2\mathrm{r_{on}} + \mathrm{r}_{\mathrm{j}+1} + \mathrm{r_j}}{2}\sqrt{\frac{\mathrm{C_jC}_{\mathrm{j}+1}}{\mathrm{L_j}(\mathrm{C_j} + \mathrm{C}_{\mathrm{j}+1})}}, \tag{6.11}$$

$$\omega_{\mathrm{j}} = \sqrt{\frac{(\mathrm{C_j} + \mathrm{C}_{\mathrm{j}+1})}{\mathrm{L_jC_jC}_{\mathrm{j}+1}}}. \tag{6.12}$$

Therefore, at the time of $T_{\mathrm{j},n} = n\pi/\omega_\mathrm{j}\sqrt{1-{\zeta_\mathrm{j}}^2}$, the current is zero. When a payload with the duration of $T_{\mathrm{j},1}$ is transmitted, the storage voltages after sending/receiving the payload are

$$v_{\mathrm{j}+1}(T_{\mathrm{j},1}) = v_{\mathrm{j}+1}(0) - \frac{\mathrm{C_j}(v_{\mathrm{j}+1}(0) - v_\mathrm{j}(0))}{\mathrm{C_j} + \mathrm{C_{j+1}}} \left\{ 1 + \exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}} \right) \right\}, \tag{6.13}$$

$$v_\mathrm{j}(T_{\mathrm{j},1}) = v_\mathrm{j}(0) + \frac{\mathrm{C_{j+1}}(v_{\mathrm{j}+1}(0) - v_\mathrm{j}(0))}{\mathrm{C_j} + \mathrm{C_{j+1}}} \left\{ 1 + \exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}} \right) \right\}. \tag{6.14}$$

When the load current is negligible during the payload transmission, Eq. (6.10) is also valid for the connection to the load[2].

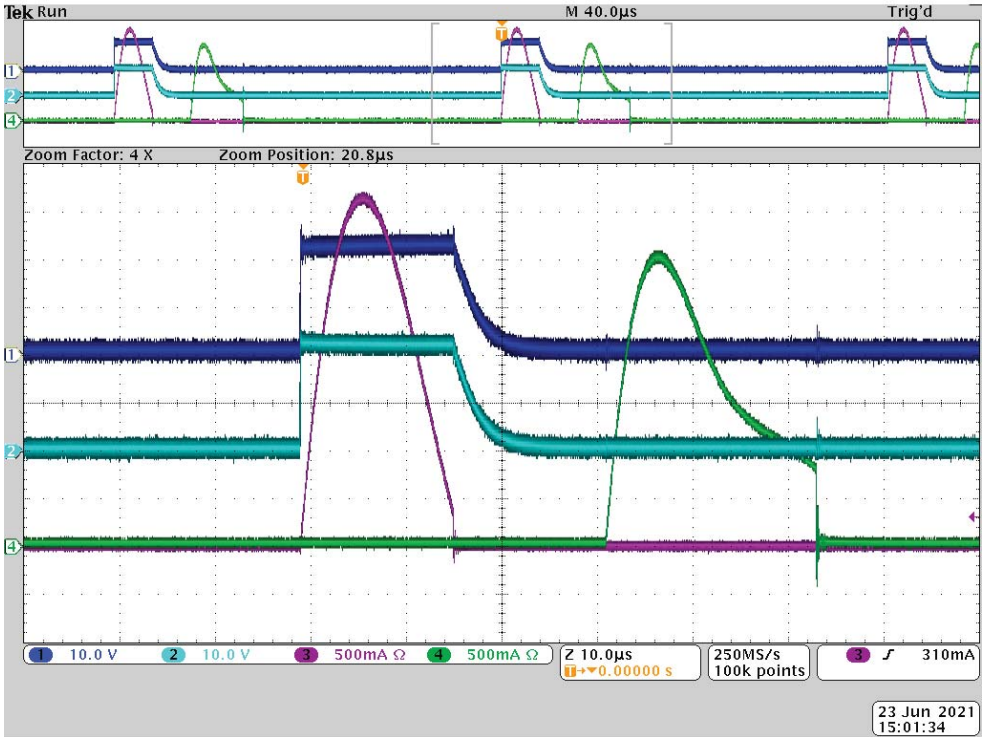
From the Eqs. (6.3) and (6.10), the payload with the duration of $T_{\mathrm{j},n}$ $(\mathrm{j}, n \in \mathbb{N})$ is expected to transmit power with small switching losses. We call the payload *underdamped payload* in the following. $T_{0,1}$ can be estimated from the experimental results. In Fig. 5.8a, T_p at the first local peak voltage in $T_\mathrm{d} = 50\,\mu$s corresponds to $T_{0,1}$. The storage voltages after sending/receiving an underdamped payload are shown in Eqs. (6.6), (6.13), and (6.14). They give the parameters $(\zeta_\mathrm{j}, \zeta_\mathrm{j})$ from circuit constants. Therefore, the relationships between storage voltages after and before sending/receiving an underdamped payload are linear equations. Combining these relationships in the network gives the voltage distribution as the solution of the linear equations.

6.1.2 Experimental verification of underdamped payload transmission

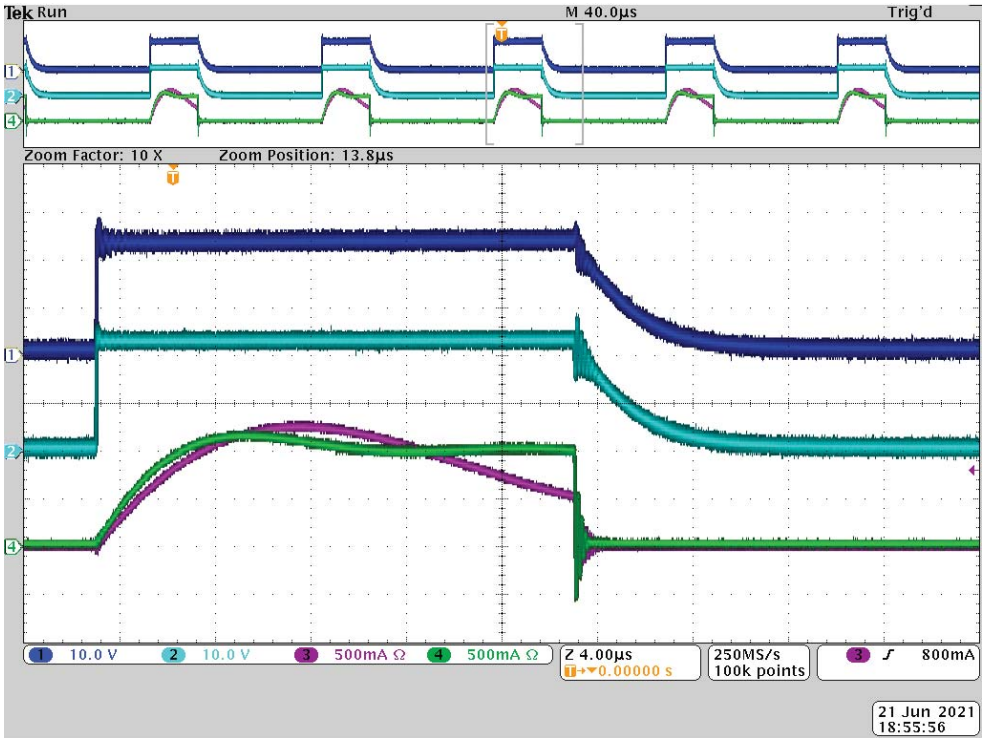
We verify the underdamped payload transmission in the experiment. The verification is performed on the same circuit as Fig. 5.5. The circuit parameters are also the same as Tab. 5.2. The line current i_0 and i_1, the voltages of the transmitter and receiver sides of the line v_{t0} and v_{r0} are measured. The underdamped payload transmission and the zero-current switching (ZCS) are verified in the results. Then, the storage voltages v_0 and v_1 with the underdamped payload transmission are measured.

Figure 6.4 shows the payload transmission at underdamped and overdamped conditions. The payload transmission is finished with less than 400 mA of i_0 in Fig. 6.4a. The surge voltages are not found on v_{t0} and v_{r0}. The duration of the payload between Router

[2]Sec. A.2 provides the analysis including the load current



(a)



(b)

Figure 6.4: Experimental results of v_{t0} (CH1), v_{r0} (CH2), i_0 (CH3), and i_1 (CH4) with (a) underdamped condition and (b) overdamped condition.

0 and # 1 $T_{0,1}$ was set at 16.0 μs. It is shorter than the estimated $T_{0,1}$ 18.9 μs. The difference owes to the switching dynamics and DC characteristics of MLCC. In Fig. 6.4b, the duration of the payload is longer than Fig. 6.4a, but i_0 is higher than 500 mA at the end of the payload. It results in the surge voltages on v_{t0} and v_{r0}. The results confirm that the underdamped payload transmission is applicable to the surge suppression.

The underdamped condition uses the resonance in the circuit but is different from Class-E switching converters [63]. Class-E converters can also achieve zero-derivative switching (ZDS) and thus are expected to be more efficient than the underdamped payload[3]. The underdamped payload transmission requires circuit constants to find $T_{\mathrm{j},n}$. It implies that $T_{\mathrm{j},n}$ can be found on the existing circuits. Also, $T_{\mathrm{j},n}$ can be found in the experimental results. When the circuit parameters are unknown or depend on their voltages, we can control the pulse width to meet $T_{\mathrm{j},n}$. On the other hand, Class-E converters require tuning or numerical simulations to find the optimal switching conditions and circuit parameters [63, 79–81]. In this sense, the underdamped payload is a simple method to suppress surge voltages and decrease switching losses.

Figure 6.5 depicts the fluctuations of storage voltages with the underdamped payload transmission. v_0 and v_1 are in periodically stable states. Focusing on the waveform of v_1, we can find that it consists of the two stable voltages and the step responses. The two stable voltages are the highest and lowest voltages of v_1. They are represented by $v_{1\mathrm{H}}$ and $v_{1\mathrm{L}}$ in the following. As Eqs. (6.3) and (6.10) show, the step responses are described by the initial condition of the storage voltages and the circuit parameters. In addition, Eqs. (6.13) and (6.14) show that $v_{1\mathrm{L}}$ the highest voltage of storage #0 ($v_{0\mathrm{L}}$) are calculated from $v_{1\mathrm{H}}$ and the lowest voltage of storage #0 ($v_{0\mathrm{H}}$). The relationships among $v_{1\mathrm{L}}$, $v_{1\mathrm{H}}$, $v_{0\mathrm{L}}$, and $v_{0\mathrm{H}}$ are represented by the linear equations when the power transmission is performed by the underdamped payload. Thus, what we have to know are the highest and lowest voltages of each storage to describe the storage voltages at any instant.

6.2 Analytical estimation of storage voltages

Let us consider a cascaded network with N connections, as shown in Fig. 6.1. The voltage distribution is analyzed with v_{jH} and v_{jL}. v_{jH} and v_{jL} represent the highest and lowest voltages of storage #j. The results of Sec. 6.1 show that the voltage distribution

[3] ZDS and ZCS can not be achieved both turn-on and turn-off [79]

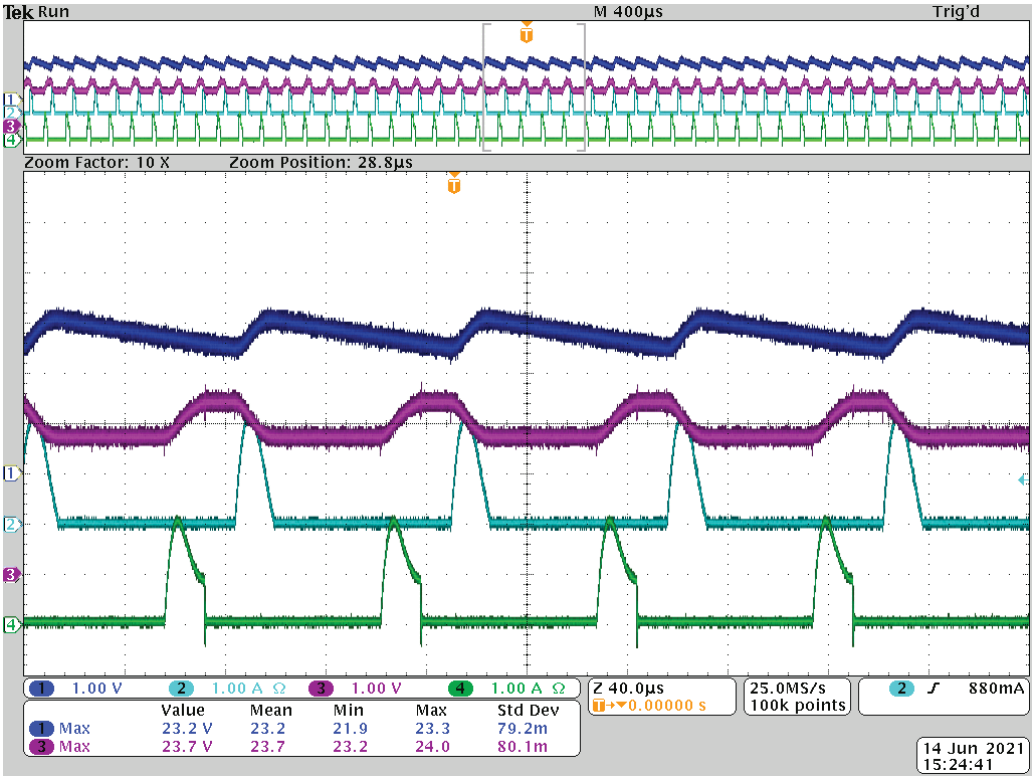


Figure 6.5: Experimental results of v_0 (CH1), v_1 (CH2), i_0 (CH3), and i_1 (CH4) with underdamped condition on i_0.

of the network can be described by linear equations. For the cascaded network with N connections, the equations are organized to be

$$\boldsymbol{M}_{\mathrm{N}}\boldsymbol{v} = \boldsymbol{e}_{\mathrm{s}}. \tag{6.15}$$

Here, $\boldsymbol{v}$ and $\boldsymbol{e}_{\mathrm{s}}$ are vectors of 2N elements. They are

$$\boldsymbol{v} = (v_{0\mathrm{L}}, v_{0\mathrm{H}}, v_{1\mathrm{L}}, \ldots, v_{\mathrm{N}-1\mathrm{L}}, v_{\mathrm{N}-1\mathrm{H}})^{\top}, \tag{6.16}$$

$$\boldsymbol{e}_{\mathrm{s}} = (v_{0\mathrm{L}}, 0, 0, \ldots, 0, e_{\mathrm{N}-1}\mathrm{E}/\mathrm{C}_{\mathrm{N}-1})^{\top}. \tag{6.17}$$

$\boldsymbol{M_N}$ is a matrix of 2N × 2N. Here, the components of $\boldsymbol{M_N}$ are written with the indices $j = 0, 1, \ldots, \mathrm{N}-1$ as follows

$$M_{2\mathrm{j}+2,2\mathrm{j}+1} = \frac{1}{\mathrm{L_j C_j}{\omega_\mathrm{j}}^2}\left\{1+\exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}}\right)\right\}-1, \tag{6.18}$$

$$M_{2\mathrm{j}+3,2\mathrm{j}+1} = -\frac{1}{\mathrm{L_j C_{j+1}}{\omega_\mathrm{j}}^2}\left\{1+\exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}}\right)\right\}, \tag{6.19}$$

$$M_{2\mathrm{j}+2,2\mathrm{j}+4} = -\frac{1}{\mathrm{L_j C_j}{\omega_\mathrm{j}}^2}\left\{1+\exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}}\right)\right\}, \tag{6.20}$$

$$M_{2\mathrm{j}+3,2\mathrm{j}+4} = \frac{1}{\mathrm{L_j C_{j+1}}{\omega_\mathrm{j}}^2}\left\{1+\exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}}\right)\right\}-1, \tag{6.21}$$

$$M_{2\mathrm{j}+1,2\mathrm{j}+1}, M_{2\mathrm{j}+2,2\mathrm{j}+2} = 1. \tag{6.22}$$

The other components of $\boldsymbol{M_N}$ are 0. For example, $\boldsymbol{M_3}$ becomes

$$\boldsymbol{M_3} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ -1+e_0/\mathrm{C_0} & 1 & 0 & -e_0/\mathrm{C_0} & 0 & 0 \\ -e_0/\mathrm{C_1} & 0 & 1 & -1+e_0/\mathrm{C_1} & 0 & 0 \\ 0 & 0 & -1+e_1/\mathrm{C_1} & 1 & 0 & -e_1/\mathrm{C_1} \\ 0 & 0 & -e_1/\mathrm{C_2} & 0 & 1 & -1+e_1/\mathrm{C_2} \\ 0 & 0 & 0 & 0 & -1+e_2/\mathrm{C_2} & 1 \end{pmatrix}. \tag{6.23}$$

For simplicity, we put e_j as

$$e_\mathrm{j} = \frac{1}{\mathrm{L_j}{\omega_\mathrm{j}}^2}\left\{1+\exp\left(-\frac{\zeta_\mathrm{j}\pi}{\sqrt{1-{\zeta_\mathrm{j}}^2}}\right)\right\}. \tag{6.24}$$

$\boldsymbol{M_N}$ is calculated from the circuit components. It does not depend on the states of the circuit. When $\boldsymbol{M_N}$ is non-singular, Eq. (6.15) has a unique solution. The solution gives the voltage distribution in the network at a periodic steady state. The voltages at any instance are calculatable with the solution.

6.2.1 Numerical verification

The solution of Eq. (6.15) estimates the storage voltages with the underdamped payloads. The accuracy of the estimation is examined with the circuit simulation. Figure 6.6

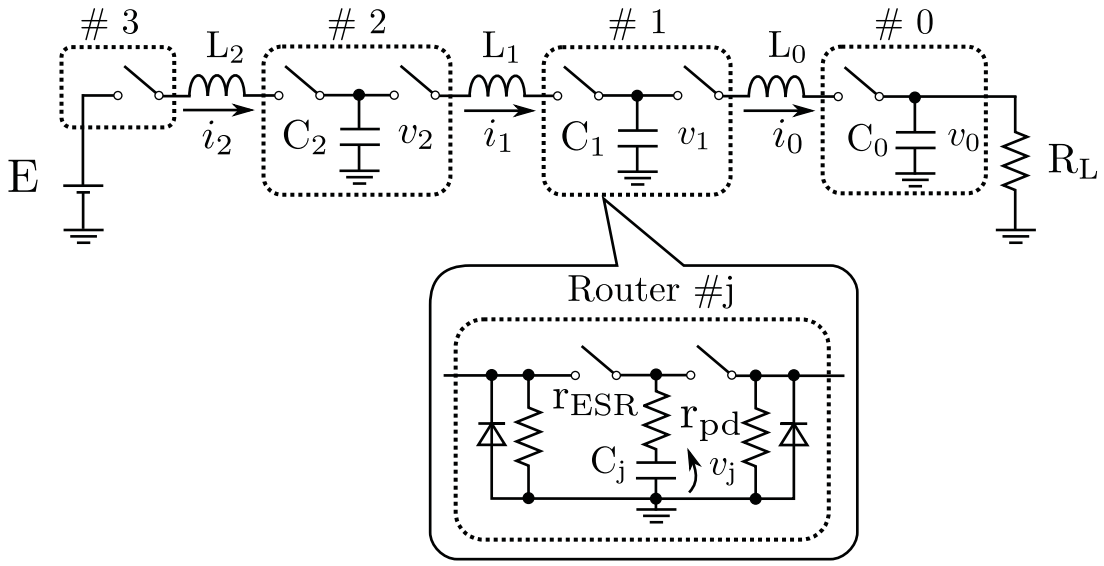


Figure 6.6: Schematic diagram of cascaded network with three connections. Detailed diagram of router is shown below the network.

Table 6.1: Simulation setup.

Name	Symbol	Model	Value
Source voltage	E	DC source	24.0 V
Load resistance	R_L	Resistor	100 Ω
Storage	C_0, C_1, C_2	Capacitor	1.0, 10, 20, 40 μF
Capacitor ESR	r_{ESR}	–	100 mΩ
Power line	L_0, L_1, L_2	Inductor	1.0 μH
MOSFETs	–	SCT3022AL	–
Freewheeling diode	–	UF4002	–
Pulldown resistance	r_{pd}	Resistor	30.0 kΩ

shows the schematic diagram of the cascaded router network with three connections. The circuit configuration of the router follows Fig. 5.5. The circuit model was made with LTSpice XVII. The device models and simulation parameters are shown in Tab. 6.1. Instead of the signal unit, a freewheeling diode and a resistor are placed at each port of routers. They simplify the simulation model and shorten the simulation time. It is confirmed beforehand that the replacement has little impact on the results compared to the model with signal units. The capacitors and a diode between the source and network are also omitted for simplicity. v_{0L} is set at 21.6 V, 90 % of E. The time duration of the underdamped payload is calculated for each connection. In the simulation, the duration

Table 6.2: Comparison of estimated storage voltages and simulation results with 20.0 μF capacitors.

	$v_{0\mathrm{L}}$	$v_{0\mathrm{H}}$	$v_{1\mathrm{L}}$	$v_{1\mathrm{H}}$	$v_{2\mathrm{L}}$	$v_{2\mathrm{H}}$
Estimation (V)	21.60 V	22.72 V	22.34 V	23.47 V	23.09 V	24.21 V
Simulation (V)	21.40 V	22.58 V	22.10 V	23.49 V	22.93 V	24.26 V

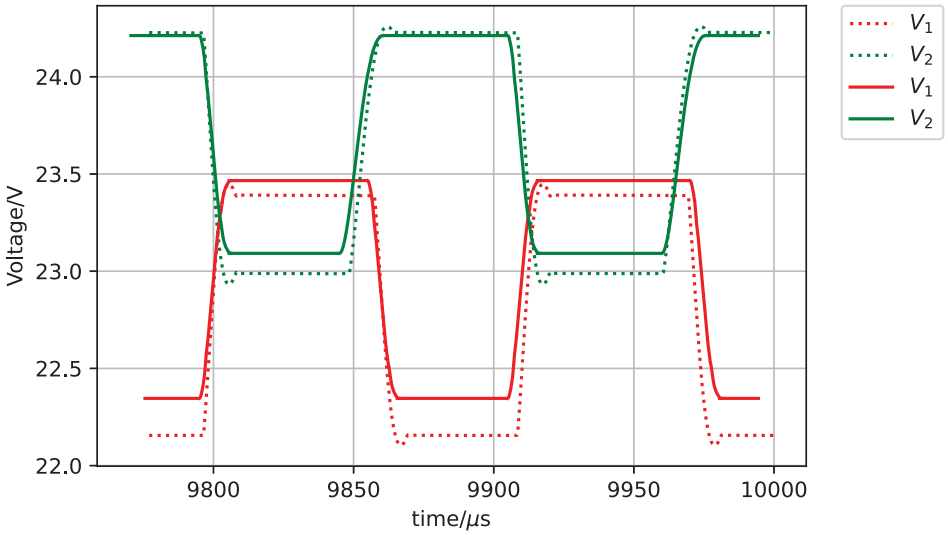


Figure 6.7: Comparison of reconstructed v_1 and v_2 from estimated storage voltages by Eq. (6.15) and simulation results with 20 μF capacitors. Dotted lines show simulation results. Solid lines are reconstructed from estimated storage voltages and step responses.

of $T_{\mathrm{j},1}$ is represented by the bit length of the payload. The time duration of one-bit $\mathrm{t_u}$ is set at 1.0 μs from the verification in Chapter 2. The bit length $B_{\mathrm{j},1}$ of $T_{\mathrm{j},1}$ is set to satisfy $B_{\mathrm{j},1} = \lfloor T_{\mathrm{j},1}/\mathrm{t_u} \rfloor$ The switching period T_{s} was decided by the load and the storage directly connected to it. It was calculated by

$$T_{\mathrm{s}} = (\mathrm{R_L} + \mathrm{r_{ESR}})\mathrm{C}_0 \log\left(\frac{v_{0\mathrm{H}}}{v_{0\mathrm{L}}}\right) + T_{01}. \tag{6.25}$$

T_{s} is represented by the bit length $B_{\mathrm{s}}(= \lfloor T_{\mathrm{s}}/\mathrm{t_u} \rfloor)$, too. The simulation was run for 10 ms, and the averaged storage voltages were calculated with the last two periods. 10 ms is long enough for the simulation setup to get a periodically stable state. The initial storage voltages are set at the solution of Eq. (6.15). The simulation was run several times with different capacities of C_0, C_1, and C_2.

Table 6.2 shows v_{jH} and v_{jL} in the case of 20 μF storage. Though the analysis does not

Table 6.3: Comparison of solution of the modeling and simulation.

C_0, C_1, and C_2	Averaged V_{dif}	RMSE	T_{s}	$T_{0,1}$
$1.0\,\mu$F	2.91 V	1.93×10^{-2}	$13.98\,\mu$s	$2.23\,\mu$s
$10\,\mu$F	1.58 V	7.05×10^{-3}	$70.65\,\mu$s	$7.42\,\mu$s
$20\,\mu$F	1.28 V	6.44×10^{-3}	$112.37\,\mu$s	$11.16\,\mu$s
$40\,\mu$F	1.06 V	6.28×10^{-3}	$183.10\,\mu$s	$18.36\,\mu$s

pay attention to the dynamics of the switches, it shows a good match at the periodical steady states. The voltage difference between v_{jH} and v_{jL} is almost the same in the three routers. It is because the capacitances of the storage are set to be the same. $v_{0\mathrm{L}}$ is smaller than 21.6 V in the simulation. It is due to the ignorance of the power transmission to the load during receiving payloads. In order to increase $v_{0\mathrm{L}}$, T_{s} can be set shorter than Eq. (6.25). $v_{2\mathrm{H}}$ is higher than E. It is also one of the characteristics of an underdamped response. $v_{2\mathrm{H}}$ takes higher voltage as the voltage difference between $v_{2\mathrm{H}}$ and $v_{2\mathrm{L}}$ increases. Figure 6.7 shows storage voltages $v_1(t)$ and $v_2(t)$. The dotted lines are the simulation results, and the solid lines are reconstructed from the estimated voltages. The reconstruction used v_{jH}, v_{jL}, and Eq. (6.10). The reconstructed voltage waveforms show the similar waveforms to the simulation results. The comparison of waveforms clearly confirms that the estimation method is applicable to analyze the storage voltage.

The results of other parameters are summarized in Tab. 6.3. For each case, the averaged voltage difference V_{dif} between v_{jH} and v_{jL} is calculated from the simulation result. The result shows that the averaged V_{dif} decreases as the storage capacitance increases. It indicates that the storage connected to the load requests a large capacitance to reduce the voltage ripple. The root square mean errors (RMSEs) between the solution of the modeling and simulation are calculated from the result. For each v_{jH} and v_{jL}, their difference are normalized by E. RMSE is calculated from the normalized difference. RMSE decreases as the capacitance get larger. In the case of $1.0\,\mu$F, RMSE is about two times larger than the $10\,\mu$F case. It is because the proportion of the time difference between $B_{\mathrm{j},0}\mathrm{t_u}$ and $T_{\mathrm{j},0}$ against $T_{\mathrm{j},0}$ decreases as the storage increases. It the case of small capacitances, the accuracy of the estimation is not confirmed yet.

The advantage of Eq. (6.15) is the required time to estimate voltages. For example, Eq. (6.15) with three connections can be solved in a second by a computer. In contrast,

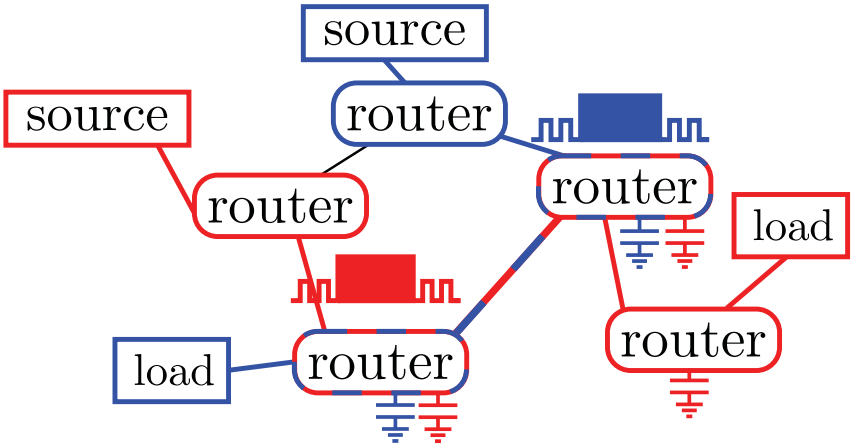


Figure 6.8: Example of designed network in Step 7.

the 10 ms-simulation took some minutes by the same machine. The network with three connections is the second smallest one. The time to get the steady-state depends on the simulation environment and the number of routers. The voltage estimation method will be a useful tool to design a network with multiple connections. The method is also compatible with the PDM control. Appendix B describes the output characteristics under the PDM control. The results in Appendix B clearly show that the output control is achievable with PDM. Therefore, the system can dynamically respond to the demand from the load.

6.3 Proposal of power packet dispatching system design

Here we propose a design of the power packet dispatching system based on the experimentally verified performance limitations. The results of Chapter 2 ensure that the information and power transmission part of a power packet can be designed separately. Based on it, Chapter 3 and 4 discussed the necessary bit length through the verification of the decentralized control and the bidirectional power packet transmission. Chapter 6 analyzed the voltage distribution in the network theoretically based on the results of Chapter 5. The proposed voltage estimation method above calculates the distribution of storage voltages from the circuit parameters, the source voltage, and the minimum voltage of the load.

Here we can propose a feasible design of the power packet dispatching system based

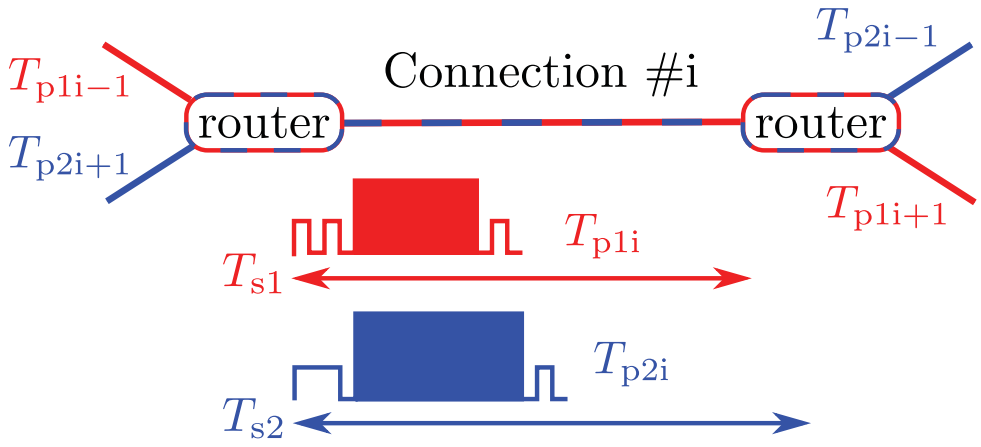


Figure 6.9: Concept of design Step 8.

on the results as described below.

Step 1. Get source voltages, minimum load voltages, and allocations of sources, loads, and routers

Step 2. Decide routes between sources and loads

Step 3. Decide switches of routers

Step 4. Calculate required communication time for each connection

Step 5. For each route, set an arbitral target value e.g. efficiency

Step 6. Decide storage capacitances within the underdamped condition on each route by heuristics methods

Step 7. Get required durations of payload transmission and their cycles on each connection

Step 8. Check whether all power packets are transmittable within their cycles without overlap

Step 9. If transmittable, the power packet transmission will be performed as intended

Step 10. If the power packet transmission is not realized, back to Steps 1., 2., or 5. and reconsider the design

Steps 1. and 2. are assumed to be predefined in this dissertation. Step 3. is based on the results of Chapter 2. We can decide the power switches to stand the highest voltage

handled by the router. From the results of Chapters 3 and 4, we can obtain the amount of information in Step 4. Figures 6.8 and 6.9 show the concept of the corresponding design steps. When a design is proceeded to Step 7., there are some connections where multiple types of power packets are transmitted. In Step 8., we check whether they can be transmitted. On the connection #i with multiple types of power packets, one type of power packet k ($k \in \mathbb{N}$) has its cycle T_{sk} and duration T_{pki} from the former steps. If their transmissions are possible within their cycles without overlaps, the system can work as intended. Here, when the transmission is unable to conduct within the cycle, the output voltage can not keep the intended output anymore.

6.4 Summary

This chapter proposed a feasible design of the power packet dispatching system. The power packet transmission between two routers was analyzed as an RLC filter. Based on the step response of the RLC filter, the underdamped payload transmission was proposed. The payload gives linear relationships between storage voltages before and after sending/receiving the payload. The experiment verified the underdamped payload transmission and confirmed that the surge voltages are not seen at the end of the payload.

It is found that linear equations describe the voltage distribution in the network. The highest and lowest voltages were set for each storage. Linear equations give the relationships between these voltages. The solutions of the equations estimate the storage voltages at the periodically stable state. The estimated storage voltages are compared with the simulation results. The estimated voltages are in good match with the simulation when the storage capacity was larger than $10\,\mu$F. In the case of $1.0\,\mu$F, the error between the estimation and simulation increases. It indicates that the estimation method is accurate enough to use in design.

A feasible design of the power packet dispatching system was finally proposed. The proposed design requires the voltages of sources and loads and the allocations of routers. The design gives the hardware specifications of the router, the capacities of the storage, and the bit length of each part of power packets. The design is proposed with the heuristics methods utilizing the proposed voltage estimation method. When all power packets are transmittable within their cycles in all connections, the designed system delivers power as intended.

Chapter 7

Conclusions and future directions

In this dissertation, we tried to propose a feasible design of the power packet dispatching system. The system is divided into some layers refer to the OSI model in information networks. For each layer, we examined the limitations and their factors on power packet transmission. The required amounts of information and power are obtained. This chapter summarizes the contributions of each chapter, then discuss the future directions.

7.1 Summary of contribution

In Chapter 2, we proposed a power packet router that can extend the amounts of information and power per power packet. It collaboratively operates the multiple types of switches to generate a single power packet. The proposed router ensures the simultaneity of power and information by its generation method. The proposed router achieved 100 V and 1 Mbps power packet transmission in the experiment. The experimental results verify that the signal and power switches in the router can be selected independently. The results also verify that the information and power parts can be separately designed. Based on the results, the following sections focused on the information or power part of power packets.

In Chapter 3, we focused on the information part and proposed the decentralized control of the power packet dispatching system. The preceding experimental studies on the power packet dispatching system employed the centralized control. It is expected to require a long length of address to distinguish all loads or routes between sources and loads. The proposed decentralized control can shorten the address. The decentralized control divides the system into subsystems. Each subsystem operates independently. First, the decentralized control was examined with the wireless feedback. It verified the

decentralized operation but had an unacceptable feedback delay. Then, the wired feedback was verified to minimize the feedback delay.

In Chapter 4, we considered the required data length to realize multidirectional transmission. As a fundamental technique to study multidirectional transmission, we verified half-duplex power packet transmission. A MAC protocol was adopted to avoid the collision of power. The experiment was performed with the adopted protocol. The experimental results show that the half-duplex power packet transmission is available with the MAC protocol. The transmission timing was found to influence the output. The multidirectional power packet transmission was studied based on the half-duplex transmission. It is expected to improve efficiency. The limitations on power transmission due to the protocols were evaluated from the required data length and power viewpoints. The results indicate that an appropriate protocol can minimize the data length and increase the amount of transmittable power.

In Chapter 5, we examined the connection dependency of the output voltage in the cascaded power packet dispatching network. First, we analyzed the smallest one-to-one network compared with the buck converter operating in DCM. The output increases monotonically with the increase in the duty cycle. The monotonical characteristics are obtained when the storage capacity is designed as a component of an RLC filter. Then, based on the design, the cascaded network with two connections was examined. The pulse width and the connection timing were modulated, and the output was measured in the experiment and simulation. The results show that the overlap duration of transmissions is another control variable in the power packet dispatching system. The simulation results on various parameters indicated that the best transmission condition would be challenging to find.

In Chapter 6, we proposed a feasible design of the power packet dispatching system with the underdamped condition. The underdamped condition was found to have the lowest output voltage in many cases in Chapter 5. The characteristics are helpful in guaranteeing the output of the system. We first experimentally verified the payload transmission under the underdamped condition. We call the payload underdamped payload. The underdamped payload achieved surge less turn-off with the zero-current condition. Then, we analyzed power transmission with the underdamped payload. The relationships between storage voltages are described by linear equations with the underdamped payload transmission. The analysis set the high and low states voltages to each storage.

Their relationships are arranged in simultaneous equations. The solution of the equations estimates the storage voltages at a periodically stable state. The estimated voltages were compared with the simulation. The estimation was revealed to be applicable to design. Finally, we proposed a feasible design of the power packet dispatching system based on the voltage estimation method.

7.2 Future directions

As future directions, we point out the following three viewpoints. The first point is the future works of this dissertation. The second point is the outlook of the advances in elemental technologies in this dissertation. The last one is the directions on the power packet dispatching system.

Firstly, The proposed feasible design in Chapter 6 is not the best one. Further studies on the design can increase the efficiency of the system. The improvement would require a generalization of the proposed design. By the generalization, the design, including the placements and number of routers, will be available that were assumed predefined in this dissertation. Circuit simulations is possibly combined with the proposed method. A circuit design with numerical methods and circuit simulators have been proposed for class-E converters [80, 81]. Likewise, a design with circuit simulators is applicable to the power packet dispatching system. The simulation helps pay attention to the dynamics of switches and devices. The control is another factor to be included in the design. Studies on the feedback control under data-rate constraints will give the required data rate for the control [82–84].

Secondly, the underdamped pulse transmission and the induced voltage estimation method are possibly applied to other applications. The possible applications include DC solid-state circuit breakers [85, 86] and DC-DC converters [87, 88]. If a circuit can be converted to an RLC filter, it is a candidate for the application. ZCS is one of the conditions to achieve class-E switching [63]. ZCS condition is obtained theoretically with the underdamped condition. It is an advantage of the underdamped pulse. The voltage estimation method proposed in Chapter 6 can strictly estimate the storage voltages in the ideal system. In general, the storage voltages are obtained by simulation or numerical integration. The proposed method gives the states of the system by solving linear equations. In this sense, it is one of the linearization methods.

Lastly, the power packet dispatching system should be compared with AC and DC systems. The power packet dispatching system is often pointed out to be inefficient due to the switching and conduction losses and has never been compared numerically with them. Also, there were no methods for the analysis and design like the per-unit method in AC systems. This dissertation addressed the challenges above. Underdamped payload transmission is expected to decrease the switching loss and provides the analysis and design methods. The comparisons will be available based on the proposed design. In comparison, a new evaluation method or index will be required. The proposed design takes communication into account. However, efficiency, the widely accepted evaluation index of power systems, shows the output power over input power at a periodic steady state. It does not consider the control and communication. To include the communication, there is needed a new evaluation method or index. Measuring data traffic, delay, and jitter along a specific scenario are possible indexes to evaluate the required control and communication. Through the comparison, the advantages and limitations of the power packet dispatching systems will also be revealed.

Appendix A

Analysis on simultaneous connection and connection to load

A.1 Simultaneous connection of three routers

We consider the payload transmission in the cascaded network with three routers. Here, we analyze the simultaneous connection shown in Fig. A.1. When the routers get connected simultaneously, all the switches turn on or off at the same time. Setting the

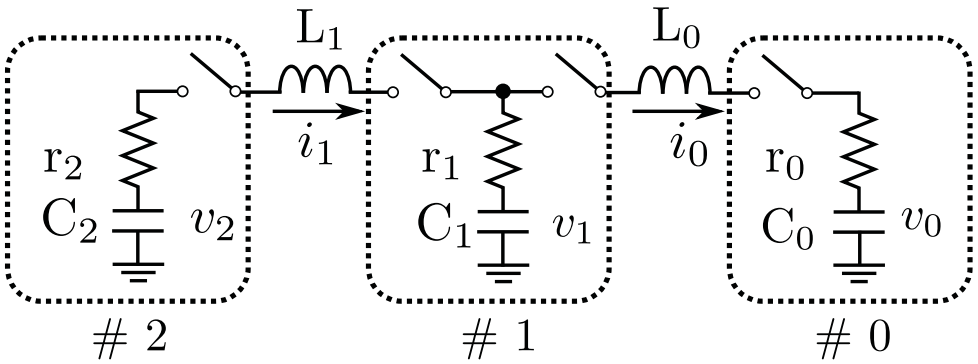


Figure A.1: Schematic diagram of cascaded network with three routers. All switches are driven simultaneously.

switches turn on at $t = 0$, we can describe the following differential equations,

$$\mathrm{C}_0 \frac{\mathrm{d}v_0}{\mathrm{d}t} = i_0, \tag{A.1}$$

$$\mathrm{C}_1 \frac{\mathrm{d}v_1}{\mathrm{d}t} = i_1 - i_0, \tag{A.2}$$

$$\mathrm{C}_2 \frac{\mathrm{d}v_2}{\mathrm{d}t} = -i_1, \tag{A.3}$$

$$v_2 - v_1 = (r_2 + \mathrm{r}_1) i_1 - \mathrm{r}_1 i_0 + \mathrm{L}_1 \frac{\mathrm{d}i_1}{\mathrm{d}t} \tag{A.4}$$

$$v_1 - v_0 = -\mathrm{r}_1 i_1 + (\mathrm{r}_1 + \mathrm{r}_0) i_0 + \mathrm{L}_0 \frac{\mathrm{d}i_0}{\mathrm{d}t}. \tag{A.5}$$

These equations are arranged as,

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} v_0 \\ v_1 \\ v_2 \\ i_0 \\ i_1 \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1/\mathrm{C}_0 & 0 \\ 0 & 0 & 0 & -1/\mathrm{C}_1 & 1/\mathrm{C}_1 \\ 0 & 0 & 0 & 0 & -1/\mathrm{C}_2 \\ -1/\mathrm{L}_0 & 1/\mathrm{L}_0 & 0 & -(\mathrm{r}_0 + \mathrm{r}_1)/\mathrm{L}_0 & \mathrm{r}_1/\mathrm{L}_0 \\ 0 & -1/\mathrm{L}_1 & 1/\mathrm{L}_1 & \mathrm{r}_1/\mathrm{L}_1 & -(\mathrm{r}_1 + \mathrm{r}_2)/\mathrm{L}_1 \end{pmatrix} \begin{pmatrix} v_0 \\ v_1 \\ v_2 \\ i_0 \\ i_1 \end{pmatrix}. \tag{A.6}$$

We can find that Eq. (A.6) does not have a unique solution. The unique solution is calculated with the energy conservation law. The voltage waveforms are generally calculated by the circuit simulation.

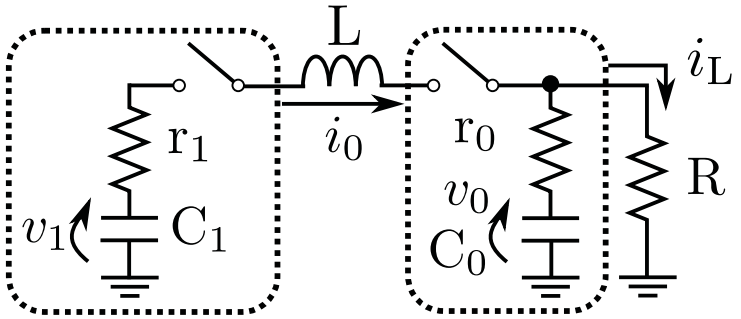


Figure A.2: Schematic diagram of one-to-one connection and load.

A.2 Connection with load

Likewise, a one-to-one connection with a load is considered. The differential equations are described as follows:

$$\mathrm{C}_0\frac{\mathrm{d}v_0}{\mathrm{d}t} = i_0 - i_\mathrm{L}, \tag{A.7}$$

$$\mathrm{C}_1\frac{\mathrm{d}v_1}{\mathrm{d}t} = -i_0, \tag{A.8}$$

$$\mathrm{L}\frac{\mathrm{d}i_0}{\mathrm{d}t} = v_1 - v_0 - i_0(\mathrm{r}_0 + \mathrm{r}_1) + \mathrm{r}_0 i_\mathrm{L}, \tag{A.9}$$

$$v_0 = (\mathrm{R} + \mathrm{r}_0)i_\mathrm{L} - \mathrm{r}_0 i_0. \tag{A.10}$$

The initial and final values are

$$i_0(0) = 0, \tag{A.11}$$

$$v_0(0) = (\mathrm{R} + \mathrm{r}_0)i_\mathrm{L}(0), \tag{A.12}$$

$$i_0(\infty) = v_1(\infty) = v_0(\infty) = 0. \tag{A.13}$$

Substituting Eq. (A.10) to Eq. (A.7) gives,

$$\frac{\mathrm{d}i_0}{\mathrm{d}t} = -\frac{i_0}{\mathrm{C}_0\mathrm{r}_0} + \frac{i_\mathrm{L}}{\mathrm{C}_0\mathrm{r}_0} + \frac{\mathrm{R} + \mathrm{r}_0}{\mathrm{r}_0}\frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t}. \tag{A.14}$$

Then, we can eliminate $\mathrm{d}i_0/\mathrm{d}t$ using Eqs. (A.8) and (A.14), and obtain,

$$\frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t} = -\frac{\mathrm{L} + \mathrm{C}_0\mathrm{R}\mathrm{r}_0}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}i_\mathrm{L} + \frac{\mathrm{L} - \mathrm{C}_0\mathrm{r}_1\mathrm{r}_0}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}i_0 + \frac{\mathrm{C}_0\mathrm{r}_0}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}v_1. \tag{A.15}$$

Substituting i_L from Eq. (A.9) to Eq. (A.15) gives,

$$-\frac{\mathrm{L}}{\mathrm{R}}\frac{\mathrm{d}^2 i_0}{\mathrm{d}t^2} + \frac{1}{\mathrm{R}}\frac{\mathrm{d}v_1}{\mathrm{d}t} - \frac{\mathrm{r}_1}{\mathrm{R}}\frac{\mathrm{d}i_0}{\mathrm{d}t} = -\frac{\mathrm{L} + \mathrm{C}_0\mathrm{R}\mathrm{r}_0}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}i_\mathrm{L} + \frac{\mathrm{L} - \mathrm{C}_0\mathrm{r}_1\mathrm{r}_0}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}i_0 + \frac{\mathrm{C}_0\mathrm{r}_0}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}v_1. \tag{A.16}$$

In the same way, we can eliminate i_L from Eq. (A.16) by substituting i_L from Eq. (A.9). The equation becomes,

$$\frac{\mathrm{d}^2 i_0}{\mathrm{d}t^2} + \frac{\mathrm{L} + \mathrm{C}_0(\mathrm{R}\mathrm{r}_0 + \mathrm{R}\mathrm{r}_1 + \mathrm{r}_0\mathrm{r}_1)}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}\frac{\mathrm{d}i_0}{\mathrm{d}t} + \frac{\mathrm{R}(\mathrm{C}_1 - \mathrm{C}_0) + \mathrm{r}_1\mathrm{C}_1 - \mathrm{r}_0\mathrm{C}_0}{\mathrm{L}\mathrm{C}_0\mathrm{C}_1(\mathrm{R} + \mathrm{r}_0)}i_0 - \frac{1}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}v_1 = 0. \tag{A.17}$$

By taking the differential of time and substituting $\mathrm{d}v_1/\mathrm{d}t$, we have,

$$\frac{\mathrm{d}^3 i_0}{\mathrm{d}t^3} + \frac{\mathrm{L} + \mathrm{C}_0(\mathrm{R}\mathrm{r}_0 + \mathrm{R}\mathrm{r}_1 + \mathrm{r}_0\mathrm{r}_1)}{\mathrm{L}\mathrm{C}_0(\mathrm{R} + \mathrm{r}_0)}\frac{\mathrm{d}^2 i_0}{\mathrm{d}t^2} + \frac{\mathrm{R}(\mathrm{C}_1 - \mathrm{C}_0) + \mathrm{r}_1\mathrm{C}_1 - \mathrm{r}_0\mathrm{C}_0}{\mathrm{L}\mathrm{C}_0\mathrm{C}_1(\mathrm{R} + \mathrm{r}_0)}\frac{\mathrm{d}i_0}{\mathrm{d}t} + \frac{1}{\mathrm{L}\mathrm{C}_0\mathrm{C}_1(\mathrm{R} + \mathrm{r}_0)}i_0 = 0. \tag{A.18}$$

For simplicity, we represent Eq. (A.18) as follows,

$$\frac{\mathrm{d}^3 i_0}{\mathrm{d}t^3} + a_2 \frac{\mathrm{d}^2 i_0}{\mathrm{d}t^2} + a_1 \frac{\mathrm{d}i_0}{\mathrm{d}t} + a_0 i_0 = 0. \tag{A.19}$$

Equation (A.19) is a third order ordinally differential equation. The general solution of Eq. (A.19) under the condition Eq. (A.11) is represented by,

$$i_0(t) = -(C_a + C_b)\exp(-\lambda_0 t) + C_a \exp(-\lambda_r - \lambda_i)t + C_b \exp(-\lambda_r + \lambda_i)t \tag{A.20}$$

Here, C_a and C_b are constants. λ_0 and $\lambda_r \pm \lambda_i$ are the solutions of the equation,

$$x^3 + a_2 x^2 + a_1 x + a_0 = 0. \tag{A.21}$$

λ_0 and $\lambda_r \pm \lambda_i$ can be obtained by Cardano's method. They are,

$$\begin{aligned} \lambda_0 &= -\frac{a_2}{3} + \frac{b}{3\sqrt[3]{2}} \\ &\quad + \frac{\sqrt[3]{2}(3a_1 - {a_2}^2)}{3b}, \end{aligned} \tag{A.22}$$

$$\begin{aligned} \lambda_r \pm \lambda_i &= -\frac{a_2}{3} + \frac{(1 \mp j\sqrt{3})b}{6\sqrt[3]{2}} \\ &\quad + \frac{(1 \pm j\sqrt{3})(3a_1 - {a_2}^2)}{3\sqrt[3]{4}b}. \end{aligned} \tag{A.23}$$

Here, b is an constant, represented by

$$b = \sqrt[3]{-2{a_2}^3 + 9a_1a_2 - 27a_0 + \sqrt{4(3a_1 - {a_2}^2)^3 + (-2{a_2}^3 + 9a_1a_2 - 27a_0)^2}}. \tag{A.24}$$

C_a and C_b can be calculated by substituting λ_0 and $\lambda_r \pm \lambda_i$ into Eq. (A.20). They have complex formula and depend on the initial conditions. Therefore, when the load is connected to the storage directly, the voltage estimation method proposed in Sec. 6.2 is not strict. The validity of the method is limited in the case where the load is light enough to ignore i_{L} during the payload transmission.

Appendix B

PDM control with underdamped payload

Here we examine the output under the PDM control with the underdamped payload. The experimental circuit is the same as Fig. 5.4. The circuit constants are, too, set at the same values as Tab. 5.2. We change the transmission cycle T_s and measure averaged output voltage V_0. The current on the line L_0 follows the underdamped waveform, but the current on L_1 does not. It is affected by the diode aimed to protect the source. The pulse width T_p was set at 15 μs, which was decided by the preliminary experiment. T_p is shorter than the estimated T_0 of 18.3 μs. The difference owes to the switching dynamics and DC characteristics of MLCC, which were not considered in the estimation. The payload transmission was performed so that no overlap happens. When $T_\mathrm{o} = 0$, T_d does not affect V_0, as confirmed in Sec. 5.2.2. The duty cycle D is changed from 5 to 30 %. T_s is given by $\lfloor T'_\mathrm{s} \rfloor$. Where, $T'_\mathrm{s} = 100T_\mathrm{p}/D_\mathrm{target}$. D_target is the target duty cycle. T_p and T_s are controlled in the unit of bit (1.0 μs). For example, when D_target is set at 23 %, T_s is 50 μs and D is 23.1 %. As it shows, D does not always satisfy $D = D_\mathrm{target}$.

Figure B.1 shows the experimental results. The plotted points do not have equal intervals since $D \neq D_\mathrm{target}$. V_0 increases monotonically as D increases. It differs from the experimental results in Chapter 5. As Fig. 5.7a shows, when the overlap duration $T_\mathrm{o} = 0$, V_0 does not always increase monotonically as D increases with the PWM control. It is because the underdamped response can flow back the energy to the source side. The PDM control examined here employs T_0 as the pulse width. The underdamped payload finishes its transmission with small backflow energy. The experimental results indicate that the PDM control is applicable for the output control with the underdamped payload.

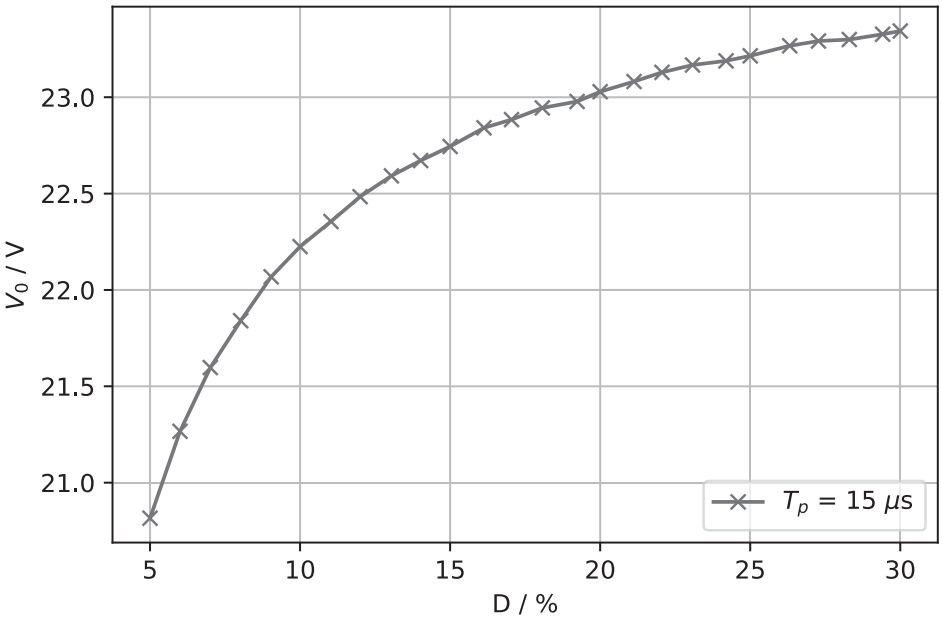


Figure B.1: Experimental results of V_0.

Note that when we apply the PDM control with the underdamped payload to a power packet dispatching network, the pulse width is set differently for each connection. For example, the pulse width was set at 18 μs on the connection between Router #0 and #1, and #1 and #2, but 24 μs between Router #2 and #3 in Chapter 6 when capacitors were 40 μF. On the other hand, the switching cycle is decided only by the load and the storage directly connected to it. When the load is a resistor, we can set the switching cycle from the estimated $v_{0\mathrm{H}}$, $v_{0\mathrm{L}}$, the resistance, and the storage capacitance. The same switching cycle and different pulse widths result in the different duty cycles on each connection. The target load voltage is achieved when the underdamped payload transmission is realized on all connections at the same switching cycle. As far as the condition is held, the transmission timing is decided freely.

Bibliography

[1] Thomas P. Hughes, *Networks of power: Electrification in western society, 1880-1930*. The Johns Hopkins University Press, 1983, pp. 97–139.

[2] E. Planas, J. Andreu, J. I. Gárate, I. Martínez De Alegría, and E. Ibarra, "AC and DC technology in microgrids: A review," *Renewable and Sustainable Energy Reviews*, vol. 43, pp. 726–749, March 2015.

[3] C. K. Tse, "Power grids in the midst of rapidly increasing penetration of power electronics," in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS*, Online, October 2020, pp. 1–5.

[4] A. Hirsch, Y. Parag, and J. Guerrero, "Microgrids: A review of technologies, key drivers, and outstanding issues," *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 402–411, July 2018.

[5] B. Wang, M. Sechilariu, and F. Locment, "Intelligent DC microgrid with smart grid communications: Control strategy consideration and design," *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 2148–2156, December 2012.

[6] Q. Shafiee, T. Dragičević, J. C. Vasquez, and J. M. Guerrero, "Hierarchical control for multiple DC-microgrids clusters," *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 922–933, December 2014.

[7] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids - Part I: A review of control strategies and stabilization techniques," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876–4891, July 2016.

[8] B. Nordman and K. Christensen, "DC local power distribution: Technology, deployment, and pathways to success," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 29–36, June 2016.

[9] N. Ertugrul and D. Abbott, "DC is the future," *Proceedings of the IEEE*, vol. 108, no. 5, pp. 615–624, May 2020.

[10] E. Reihani, M. Motalleb, R. Ghorbani, and L. Saad Saoud, "Load peak shaving and power smoothing of a distribution grid with high renewable energy penetration," *Renewable Energy*, vol. 86, pp. 1372–1379, February 2016.

[11] M. G. Molina, "Energy storage and power electronics technologies: A strong combination to empower the transformation to the smart grid," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2191–2219, November 2017.

[12] S. Anand, B. G. Fernandes, and J. Guerrero, "Distributed control to ensure proportional load sharing and improve voltage regulation in low-voltage dc microgrids," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1900 – 1913, April 2013.

[13] M. Yazdanian and A. Mehrizi-Sani, "Distributed control techniques in microgrids," *IEEE Transactions on Smart Grid*, vol. 5, no. 6, pp. 2901–2909, November 2014.

[14] D. E. Olivares, A. Mehrizi-Sani, A. H. Etemadi, C. A. Cañizares, R. Iravani, M. Kazerani, A. H. Hajimiragha, O. Gomis-Bellmunt, M. Saeedifard, R. Palma-Behnke, G. A. Jiménez-Estévez, and N. D. Hatziargyriou, "Trends in microgrid control," *IEEE Transactions on Smart Grid*, vol. 5, no. 4, pp. 1905–1919, July 2014.

[15] B. Nordman and K. Christensen, "The need for communications to enable dc power to be successful," in *Proceedings of IEEE 1st International Conference on DC Microgrids, ICDCM*, Atlanta, GA, USA, June 2015, pp. 108–112.

[16] F. Kurokawa and J. Wang, "Topics of digital control approaches for future-oriented power converters," *Nonlinear Theory and Its Applications, IEICE*, vol. 9, no. 3, pp. 306–321, June 2018.

[17] M. Saleh, Y. Esa, and A. Mohamed, "Effect of wireless communication delay on dc microgrids performance," in *Proceedings of IEEE Energy Conversion Congress and Exposition, ECCE*, Portland, OR, USA, September 2018, pp. 5164–5168.

[18] ——, "Impact of communication latency on the bus voltage of centrally controlled dc microgrids during islanding," *IEEE Transactions on Sustainable Energy*, vol. 10, no. 4, pp. 1844–1856, October 2019.

[19] T. Takuno, M. Koyama, and T. Hikihara, "In-home power distribution systems by circuit switching and power packet dispatching," in *Proceedings of 1st IEEE International Conference on Smart Grid Communications*, Gaithersburg, MD, USA, October 2010, pp. 427–430.

[20] R. Abe, H. Taoka, and D. McQuilkin, "Digital grid: Communicative electrical grids of the future," *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 399–410, June 2011.

[21] E. Gelenbe, "Energy packet networks: Adaptive energy management for the cloud," in *Proceedings of the 2nd International Workshop on Cloud Computing Platforms - CloudCP '12*, Bern, April 2012, pp. 1–5.

[22] J. Toyoda and H. Saitoh, "Proposal of an open-electric-energy-network (OEEN) to realize cooperative operations of IOU and IPP," in *Proceedings of International Conference on Energy Management and Power Delivery*, March 1998, pp. 218–222.

[23] N. Fujii, R. Takahashi, and T. Hikihara, "Networked power packet dispatching system for multi-path routing," in *Proceedings of IEEE/SICE International Symposium on System Integration*, Tokyo, Japan, December 2014, pp. 357–362.

[24] R. Takahashi, K. Tashiro, and T. Hikihara, "Router for power packet distribution network: Design and experimental verification," *IEEE Transactions on Smart Grid*, vol. 6, no. 2, pp. 618–626, March 2015.

[25] S. Mochiyama, R. Takahashi, and T. Hikihara, "Close-loop angle control of stepper motor fed by power packets," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E100-A, no. 7, pp. 1571 – 1574, July 2017.

[26] N. Yoshida, R. Takahashi, and T. Hikihara, "Power regeneration from DC motor with bidirectional router in power packet dispatching system," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3088–3092, December 2020.

[27] L. Chaari, N. Masmoudi, and L. Kamoun, "Electronic control in electric vehicle based on CAN network," in *Proceedings of IEEE International Conference on Systems, Man and Cybernetics*, vol. 7, Yasmine Hammamet, Tunisia, October 2002, pp. 65–68.

[28] C. N. Papadimitriou, E. I. Zountouridou, and N. D. Hatziargyriou, "Review of hierarchical control in DC microgrids," *Electric Power Systems Research*, vol. 122, pp. 159–167, May 2015.

[29] A. S. Tanenbaum and D. J. Wetherall, *Computer Networks*, 5th ed. Pearson, 2011.

[30] M. Yigit, V. C. Gungor, G. Tuna, M. Rangoussi, and E. Fadel, "Power line communication technologies for smart grid applications: A review of advances and challenges," *Computer Networks*, vol. 70, pp. 366–383, September 2014.

[31] A. M. Bouzid, J. M. Guerrero, A. Cheriti, M. Bouhamida, P. Sicard, and M. Benghanem, "A survey on control of electric power distributed generation systems for microgrid applications," *Renewable and Sustainable Energy Reviews*, vol. 44, pp. 751–766, 2015.

[32] C. Dou, D. Yue, Z. Zhang, and K. Ma, "MAS-based distributed cooperative control for DC microgrid through switching topology communication network with time-varying delays," *IEEE Systems Journal*, vol. 13, no. 1, pp. 615–624, March 2019.

[33] Y. Liu, Z. Qu, H. Xin, and D. Gan, "Distributed real-time optimal power flow control in smart grid," *IEEE Transactions on Power Systems*, vol. 32, no. 5, pp. 3403–3414, September 2017.

[34] H. Saitoh, S. Miyamori, T. Shimada, and J. Toyoda, "A study on autonomous decentralized control mechanism of power flow of open electric energy network," *Transactions of IEE*, vol. 117-B, no. 1, pp. 10 – 18, 1997 (in Japanese).

[35] M. He, E. Reutzel, X. Jiang, R. Katz, S. Sanders, D. Culler, and K. Lutz, "An Architecture for local energy generation, distribution, and sharing," in *Proceedings of IEEE Energy 2030 Conference*, Atlanta, GA, November 2008, pp. 1–6.

[36] E. Gelenbe, "Energy packet networks: ICT based energy allocation and storage," in *Proceedings of Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering*, 2012.

[37] E. Gelenbe and E. Ceran, "Energy packet networks with energy harvesting," *IEEE Access*, vol. 4, pp. 1321–1331, March 2016.

[38] H. Zhang, H. Zhang, L. Song, Y. Li, Z. Han, and H. V. Poor, "Peer-to-peer energy trading in dc packetized power microgrids," *IEEE Journal on Selected Areas in Communications*, vol. 38, no. 1, pp. 17–30, January 2019.

[39] J. Ma, L. Song, and Y. Li, "Optimal power dispatching for local area packetized power network," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 4765–4776, September 2018.

[40] S. Mochiyama and T. Hikihara, "Packet-based feedback control of electrical drive and its application to trajectory tracking of manipulator," *International Journal of Circuit Theory and Applications*, vol. 47, no. 4, pp. 612–632, April 2019.

[41] H. Nakano and Y. Okabe, "Design and implementation of power packet routers," in *Proceedings of Multimedia, Distributed, Cooperative, and Mobile Symposium*, 2017, pp. 1875–1880 (in Japanese).

[42] S. S. Eaves, "Network remote powering using packet energy transfer," in *IEEE International Telecommunications Energy Conference, INTELEC*, Scottsdale, AZ, USA, September 2012, pp. 1–4.

[43] R. Takahashi, S. Azuma, M. Hasegawa, H. Ando, and T. Hikihara, "Power processing for advanced power distribution and control," *IEICE Transactions on Communications*, vol. E100.B, no. 6, pp. 941–947, June 2017.

[44] N. Kawasaki, T. Oozeki, K. Otani, and K. Kurokawa, "An evaluation method of the fluctuation characteristics of photovoltaic systems by using frequency analysis," *Solar Energy Materials and Solar Cells*, vol. 90, no. 18-19, pp. 3356–3363, November 2006.

[45] T. E. Hoff and R. Perez, "Quantifying PV power output variability," *Solar Energy*, vol. 84, no. 10, pp. 1782–1793, October 2010.

[46] M. Parvez, A. T. Pereira, N. Ertugrul, N. H. Weste, D. Abbott, and S. F. Al-Sarawi, "Wide bandgap DC-DC converter topologies for power applications," *Proceedings of the IEEE*, vol. 109, no. 7, pp. 1253–1275, July 2021.

[47] K. Nagaoka, K. Chikamatsu, A. Yamaguchi, K. Nakahara, and T. Hikihara, "High-speed gate drive circuit for SiC MOSFET by GaN HEMT," *IEICE Electronics Express*, vol. 12, no. 11, pp. 1–8, May 2015.

[48] S. Mochiyama, T. Okuda, and T. Hikihara, "Power packet dispatching with shared power line: Experimental verification for industrial applications," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 2, pp. 164–172, April 2021.

[49] S. Mochiyama, N. Fujii, R. Takahashi, and T. Hikihara, "A study on trajectory control of manipulator using power packet dispatching," in *Proceedings of IEEE International Telecommunications Energy Conference, INTELEC*, Osaka, Japan, October 2015, pp. 1–5.

[50] T. Kajiyama, T. Okuda, R. Takahashi, and T. Hikihara, "An experimental study on pulse shape and cable characteristics for power packet transmission," *IEICE Technical Report*, vol. EE–112, no. 167, pp. 45–49, 2012 (in Japanese).

[51] T. Kajiyama, R. Takahashi, and T. Hikihara, "An estimation of electric power transmission on pulse wave," in *The papers of technical meeting on electronic circuits*, 2013, pp. ECT–13–062 (in Japanese).

[52] T. Takuno, T. Hikihara, T. Tsuno, and S. Hatsukawa, "HF gate drive circuit for a normally-on SiC JFET with inherent safety," in *Proceedings of 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–4.

[53] R. Araumi, K. Asada, and T. Yokoyama, "An experiment on lighting control of LEDs by power packet dispatching system," in *Proceedings of IEEE 3rd International Future Energy Electronics Conference and ECCE Asia*, Kaohsiung, Taiwan, June 2017, pp. 1120–1125.

[54] R. Takahashi, N. Yoshida, and T. Hikihara, "Power packet dispatching system and router for bi-directional dispatching," in *Proceedings of 3rd IEEE International Conference on DC Microgrids, ICDCM*, Matsue, Japan, May 2019, pp. 1–3.

[55] S. Katayama and T. Hikihara, "Energy-on-demand control for power packet dispatching via single power line," in *Proceedings of IEEE International Telecommunications Energy Conference, INTELEC*, Torino, Italy, October 2018, pp. 1–5.

[56] Y. Zhou, R. Takahashi, N. Fujii, and T. Hikihara, "Power packet dispatching with second-order clock synchronization," *International Journal of Circuit Theory and Applications*, vol. 44, no. 3, pp. 729–743, June 2016.

[57] ROHM, "SCT3022AL Datasheet Rev.E," April 2018.

[58] Efficient Power Conversion, "EPC2010 datasheet," February 2013.

[59] ON Semiconductor, "MBRS3201T3G/D," August 2017.

[60] S. Mochiyama and T. Hikihara, "Experimental implementation of power packet density modulation to close-loop control of manipulator," in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, Amalfi, Italy, June 2018, pp. 762–767.

[61] R. Takahashi, Y. Zhou, N. Yoshida, S. Nawata, N. Fujii, and T. Hikihara, "A study on physical behavior of power packet congestion in power packet router," in *Proceedings of International Symposium on Nonlinear Theory and Its Applications, NOLTA*, Tarragona, Spain, September 2018, p. 79.

[62] R. Takahashi, T. Kajiyama, T. Okuda, and T. Hikihara, "A study of pulse shape suitable for power packet dispatching on power transmission line," in *International Symposium on Nonlinear Theory and Its Applications*, Yugawara, Japan, November 2016, pp. 87–88.

[63] N. O. Sokal and A. D. Sokal, "Class E - A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE Jounal of Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, June 1975.

[64] N. Yoshida, S. Nawata, R. Takahashi, and T. Hikihara, "A study on energy harvesting for power router in power packet dispatching system," in *IEICE General Conference*, Fukuoka, Japan, March 2016, pp. A–1–27 (in Japanese).

[65] Y. Zhou, R. Takahashi, and T. Hikihara, "Power packet dispatching with features on safety," *Nonlinear Theory and Its Applications, IEICE*, vol. 7, no. 2, pp. 250–265, April 2016.

[66] Y. Ikuma, T. Huynh, K. Kuroda, and M. Hasegawa, "Design and implementation of a routing protocol for power packet network," in *Proceedings of International Symposium on Nonlinear Theory and Its Applications*, Yugawara, Japan, 2016, pp. 82 – 85.

[67] T. Matsuda, J. Ma, and M. Hasegawa, "Design and implementation of a power packet network protocol for flexible power routing," *Nonlinear Theory and Its Applications, IEICE*, vol. 10, no. 4, pp. 455–464, October 2019.

[68] G. Cena and A. Valenzano, "Achieving round-robin access in controller area networks," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 6, pp. 1202–1213, December 2002.

[69] H. Ando, S. Azuma, and R. Takahashi, "Consensus dynamics in switching networks for distributing power packets," *IFAC-PapersOnLine*, vol. 49, no. 22, pp. 351–354, 2016.

[70] H. Ando, R. Takahashi, S. Azuma, M. Hasegawa, T. Yokoyama, and T. Hikihara, "A resource sharing model in a power packet distribution network," in *International Power Electronics Conference, IPEC-Niigata - ECCE Asia*. Niigata, Japan, May 2018, pp. 3665–3669.

[71] S. Baek, H. Ando, and T. Hikihara, "Automata modeling on power packet distribution network for power flow analysis," in *Proceedings of International Symposium on Nonlinear Theory and Its Applications*, Tarragona, Spain, September 2018, pp. 464–467.

[72] ——, "Consensus-based distribution of power packets and decentralized control for routing," *Chaos*, vol. 30, no. 3, pp. 1–9, March 2020.

[73] ——, "Decentralized algorithms for consensus-based power packet distribution," *Nonlinear Theory and Its Applications, IEICE*, vol. 12, no. 2, pp. 181–193, October 2020.

[74] N. Nagai and T. Yahagi, "On complex power propagating in one-dimensional crystal," *Jounal of Signal Processing*, vol. 17, no. 3, pp. 87–93, May 2013 (in Japanese).

[75] N. Nagai, J. Ren, and T. Yahagi, "Eigen oscillation obtained from LC ladder circuit and unit elements," *Journal of Signal Processing*, vol. 17, no. 5, pp. 207–213, September 2013 (in Japanese).

[76] M. T. Tran, A. Kuwana, and H. Kobayashi, "Ringing test for third-order ladder lowpass filters," in *Proceedings of 11th IEEE Annual Ubiquitous Computing, Electronics and Mobile Communication Conference, UEMCON*, New York, NY, USA, October 2020, pp. 440–446.

[77] S. Katayama and T. Hikihara, "Power packet router with power and signal switches for a single power packet," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3242 – 3246, December 2020.

[78] B. Choi, "Buck converter in discontinuous conduction mode," in *Pulsewidth Moculated DC-to-DC Power Conversion : circuits, dynamics, and control designs.* IEEE Press, 2013, pp. 89–98.

[79] M. K. Kazimierczuk, "Class E tuned power amplifier with nonsinusoidal output voltage," *IEEE Jounal of Solid-State Circuits*, vol. 21, no. 4, pp. 575–581, August 1986.

[80] H. Sekiya, J. Lu, and T. Yahagi, "Design of generalized class E2 dc/dc converter," *International Journal of Circuit Theory and Applications*, vol. 31, no. 3, pp. 229–248, May 2003.

[81] H. Sekiya, T. Ezawa, and Y. Tanji, "Design procedure for class E switching circuits allowing implicit circuit equations," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3688–3696, December 2008.

[82] W. S. Wong and R. W. Brockett, "Systems with finite communication bandwidth constraints - I: State estimation problems," *IEEE Transactions on Automatic Control*, vol. 42, no. 9, pp. 1294 – 1299, September 1997.

[83] ——, "Systems with finite communication bandwidth constraints—II: Stabilization with limited information feedback," *IEEE Transactions on Automatic Control*, vol. 44, no. 5, pp. 1049–1053, May 1999.

[84] G. N. Nair, F. Fagnani, S. Zampieri, and R. J. Evans, "Feedback control under data rate constraints: An overview," *Proceedings of the IEEE*, vol. 95, no. 1, pp. 108–137, January 2007.

[85] L. Liljestrand, M. Backman, L. Jonsson, E. Dullni, and M. Riva, "Medium voltage DC vacuum circuit breaker," in *Proceedings of 3rd International Conference on Electric Power Equipment - Switching Technology, ICEPE-ST*, Busan, Korea (South), October 2015, pp. 495–500.

[86] Y. Wu, F. Yang, M. Rong, Y. Hu, and Z. Wu, "Bidirectional current injection MVDC circuit breaker: Principle and analysis," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1536–1546, June 2020.

[87] B. Sahu and G. A. Rincon-Mora, "A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 443–452, March 2004.

[88] Y. K. Cho and K. C. Lee, "Noninverting buck-boost DC-DC converter using a duobinary-encoded single-bit delta-sigma modulator," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 484–495, January 2020.

List of Publications

Journal articles

1. S. Katayama, R. Takahashi, and T. Hikihara, "Experimental verification of distributed energy on demand control using wireless communication on power packet dispatching system," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. J102-A, no. 9, pp. 240–248, 2019 (in Japanese).

2. S. Katayama and T. Hikihara, "Power packet router with power and signal switches for a single power packet," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3242–3246, 2020.

3. S. Katayama and T. Hikihara, "Analytical voltage estimation in power packet dispatching network," *Nonlinear Theory and its Applications, IEICE*, under review.

Peer-reviewed international conference proceedings

3. S. Katayama and T. Hikihara, "Energy-on-demand control for power packet dispatching via single power line," in *Proceedings of IEEE 40th International Telecommunication and Energy Conference, ICDCM*, Torino, Italy, October 7–11, 2018, pp. 1–5.

4. S. Katayama and T. Hikihara, "Experimental verification of half-duplex power packet transmission," in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS*, Online, October 10–21, 2020, pp. 1–5.

5. S. Katayama and T. Hikihara, "Connection dependency of output voltage in cascaded power packet dispatching network," in *Proceedings of IEEE International Conference on DC Microgrids, ICDCM*, Online, July 18–21, 2021, pp. 1–6.

Other conference proceedings and presentations

6. S. Katayama, R. Takahashi, and T. Hikihara, "An experimental study of power regulation by power packet mixer using wireless feedback," in *Proceedings of IEICE General conference*, NBS-1-1, Nagoya, Japan, March 23, 2017 (in Japanese).

7. S. Katayama, R. Takahashi, and T. Hikihara, "Experimental study on application of wireless feedback to power packet dispatching system," in *Proceedings of the 61st Annual Conference of the Institute of Systems, Control and Information Engineers (ISCIE)*, 133-3, Kyoto, Japan, May 23, 2017 (in Japanese).

8. S. Katayama, R. Takahashi, and T. Hikihara, "A simulation model for decentralized control of power packet dispatching system with wireless feedback," in *IEICE Technical Report*, EE2017-31, Sendai, Japan, October 16, 2017 (in Japanese).

9. S. Katayama, S. Baek, and T. Hikihara, "Numerical study of power line usage rate on power packet dispatching system," in *Proceedings of IEICE General conference*, N-2-1, Tokyo, Japan, March 21, 2018 (in Japanese).

10. S. Katayama and T. Hikihara, "Fundamental experiment on half-duplex power packet transmission," in *Proceedings of Kansai-section Joint Convention of Institutes of Electrical Engineering*, G-10-9, Osaka, Japan, December 1, 2018 (in Japanese).

11. S. Katayama and T. Hikihara, "A study on voltage fluctuation of buffers in distributed power packet routing," in *IEICE Technical Report*, EE2019-33, Shiga, Japan, October 10, 2019 (in Japanese).

12. S. Katayama and T. Hikihara, "Application of collision-free protocol to half-duplex power packet transmission," in *Proceedings of Kansai-section Joint Convention of Institutes of Electrical Engineering*, P-24, Osaka, Japan, November 30, 2019 (in Japanese).

13. S. Katayama, M. Hasegawa, and T. Hikihara, "Numerical Study of MAC Protocols on Power Packet Dispatching Network," in *Proceedings of IEICE General conference*, N-2-6, planned at March 18, 2020, due to COVID-19, no presentation was given, (in Japanese).

14. S. Katayama and T. Hikihara, “A numerical study on output voltage of cascaded power packet routers,” in *IEICE Technical Report*, NLP2020-49, Online, January 22, 2021 (in Japanese).