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Selective Transfer of Si Thin-Film Microchips by SiO_2 Terraces on Host Chips for Fluidic Self-Assembly

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Abstract: Fluidic self-assembly is a versatile on-chip integration method. In this scheme, a large number of semiconductor microchips are spontaneously deposited onto a host chip. The host chip typically comprises a Si substrate with an array of pockets at the designated microchip placement sites. In this study, we installed an SiO_2 layer on the terrace region between the pockets of the host chip, to reduce the attraction with the Si microchips. By the SiO_2-topped terrace scheme, we demonstrated a significant enhancement in the deposition selectivity of the Si microchips to the pocket sites, relative to the case of the conventional Si-only host chip. We theoretically explained the deposition selectivity enhancement in terms of the van der Waals interaction. Furthermore, our quantitative analysis implicated a potential applicability of the commonly used interlayer dielectrics, such as HfO_2, silsesquioxanes, and allyl ethers, directly as the terrace component.

Keywords: semiconductor; silicon; thin film; layer transfer; self-assembly; integration; device; interface; fluid; liquid

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1. Introduction

Scaling down, high-density integration, and low-cost and high-throughput production are highly demanded in various optoelectronic devices, such as electronic large-scale-integration chips, light-emitting-diode displays, and photonic integrated circuits [1–7]. The conventional pick-and-place integration method, however, has limitations for these required factors. Fluidic self-assembly is a technique to integrate microscale chips released from multiple functional wafers onto a single host chip with selective bonding of each functional microchip to the designated site of the host chip in liquid phase [8–15]. For fluidic self-assembly, a large number of microscale chips can be simultaneously integrated, in contrast to the pick-and-place method. We recently carried out fluidic self-assembly of submicron-scale Si chips, by utilizing thin-film transfer from commercially available silicon-on-insulator (SOI) wafers, as a technical step towards ultrahigh-density integration [16]. A prospective process flow of Si fluidic self-assembly is conceptually depicted in Figure 1. However, in our previous experiments, the microchips deposited not only inside the designated pockets of the host chip, but also on the terrace region between the pockets. We thus had no surficial selectivity for the microchip deposition between the pockets and the terrace region, relying only on the geographical stability inside the pockets represented by the attractive van der Waals force from the side walls. Through the field of semiconductor fluidic self-assembly, to the best of our knowledge, there has been no passive method for the deposition-site selection without energy-consuming active control by electric [11] or magnetic [17,18] fields, either. In the present study, we realize a scheme to provide the deposition-site selectivity by a simple surface coating. Specifically, we install an SiO_2 layer on top of the terrace region of the host chip to reduce the attraction with the Si microchips. We thus aim to provide higher probability for the Si microchips to be transferred into the pockets of the host chip rather than onto the terrace region by the reduction in the adhesive van der Waals interaction between the Si microchip and the terrace surface. We

statistically demonstrate the selectivity enhancement of microchip deposition into the host-chip pockets by this SiO_2-terrace scheme. Additionally, we provide a theoretical explanation of the observed selectivity in terms of the van der Waals interaction based on the Hamaker constants of the interacting materials in the fluidic system. Our quantitative analysis also implicates the synergetic use of common interlayer dielectrics directly as terrace components. The scheme proposed and demonstrated in this study could lead to high-throughput, low-cost on-chip integration for electronic and photonic devices.

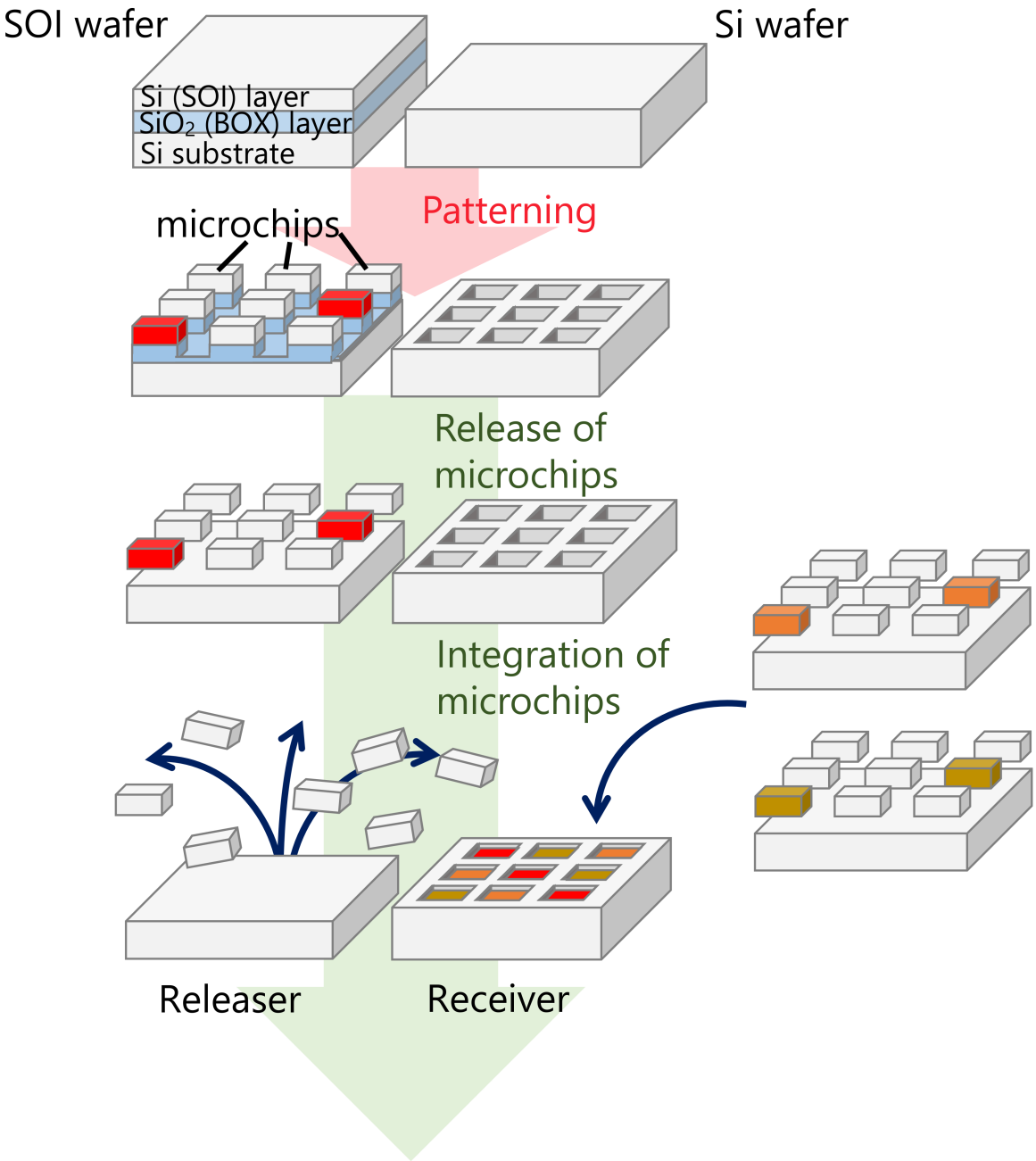

Figure 1. Schematic illustration of a prospective process flow of Si fluidic self-assembly. In practical applications, various-functional microchips from multiple kinds of wafers can be integrated into a single host chip. Different colors of the chips indicate different types of functions of the chips to be assembled.

2. Materials and Methods

For the microchip generator ("releaser"), we used a single-side-polished *p*-on-*n*-type SOI wafer (diameter: 6 inch, SOI-layer thickness: 205 nm, crystalline plane orientation: <100>, dopant: boron, doping concentration: ~1×10^{15} cm^{-3}, buried-oxide (BOX) layer thickness: 200 nm, Si-substrate thickness: 625 μm, crystalline plane orientation: <100>, dopant: phosphorus, doping concentration: ~1×10^{15} cm^{-3}). For the host chip ("receiver"), we used a single-side-polished *p*-type Si wafer with a thermally oxidized layer atop (diameter: 6 inch, SiO_2-layer thickness: 2 μm, Si-substrate thickness: 625 μm, crystalline plane orientation: <100>, dopant: boron, doping concentration: ~1×10^{14}–10^{17} cm^{-3}). For the reference receiver without a SiO_2 layer, we used a single-side-polished *p*-type Si wafer (diameter: 6 inch, thickness: 625 μm, crystalline plane orientation: <100>, dopant: boron, doping concentration: ~1×10^{14}–10^{17} cm^{-3}).

The square pillar- and pocket-shaped patterns of the releaser and receiver were photolithographically defined on the SOI and Si wafers, respectively, by dry etching, and the details are described in the following. Figure 2 shows a schematic flow diagram of the fabrication process of the releaser. The SOI wafer was, firstly, spin-cleaned by an H_2SO_4–H_2O_2 solution (5:1 vol.) for 20 s, followed by being dried on a hotplate (110 °C, 5 min). Subsequently, a photoresist film (TDMR-AR80-5cp, Tokyo Ohka Kogyo Corp., Tokyo, Japan) with a thickness of 1.3 μm was spin-coated onto the SOI wafer with a rotation velocity of 800 rpm, followed by a soft baking at 90 °C for 90 s on a hotplate. The SOI wafer with the photoresist was exposed to a 365-nm Hg lamp in an *i*-line stepper through a photomask for 380 msec. The photoresist on the SOI wafer was then developed by a tetra-methyl-ammonium-hydroxide aqueous solution (TMAH aq.). The areal region of the SOI wafer not covered by the photoresist was dry-etched by SF_6 and C_4F_8 to a depth of approximately 300 nm (i.e., about the middle of the BOX layer). The residual photoresist on the SOI wafer was finally removed by oxygen plasma. Figure 3a presents a cross-sectional scanning electron microscope image of the releaser piece.

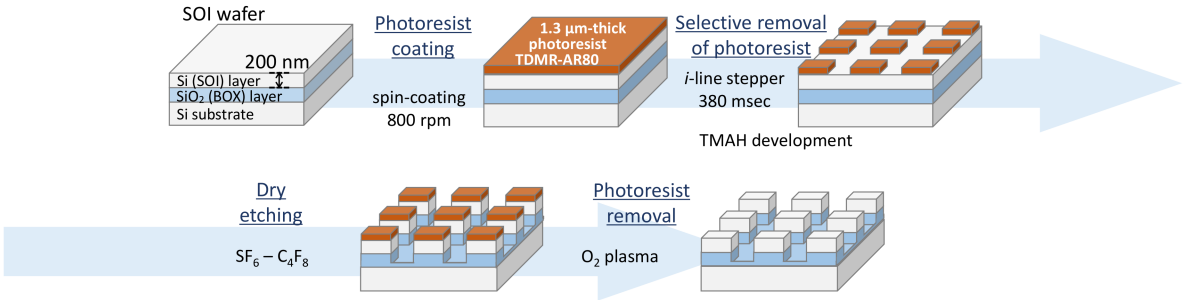

Figure 2. Schematic flow diagram of the fabrication process of the releaser.

For the receiver, after being cleaned in the same manner as the SOI wafer, the SiO_2-topped Si wafer was spin-coated with a photoresist film (TCIR-ZR8800, Tokyo Ohka Kogyo Corp., Tokyo, Japan) of a thickness of 3.6 μm with a rotation velocity of 2900 rpm. After the same soft baking as that for the SOI wafer, the SiO_2-topped Si wafer with the photoresist was exposed in the same manner for 300 msec, followed by a development by TMAH aq. The areal region of the SiO_2-topped Si wafer not covered by the photoresist was dry-etched by CHF_3 and C_4F_8 to a depth of approximately 2 μm, to the exposure of Si substrate underneath the SiO_2 layer. The residual photoresist on the SiO_2-topped Si wafer was removed by a dip in acetone with ultrasonication. Figure 3b,c present a bird's-eye-view and cross-sectional scanning electron microscope images of the receiver piece with an SiO_2 terrace, respectively.

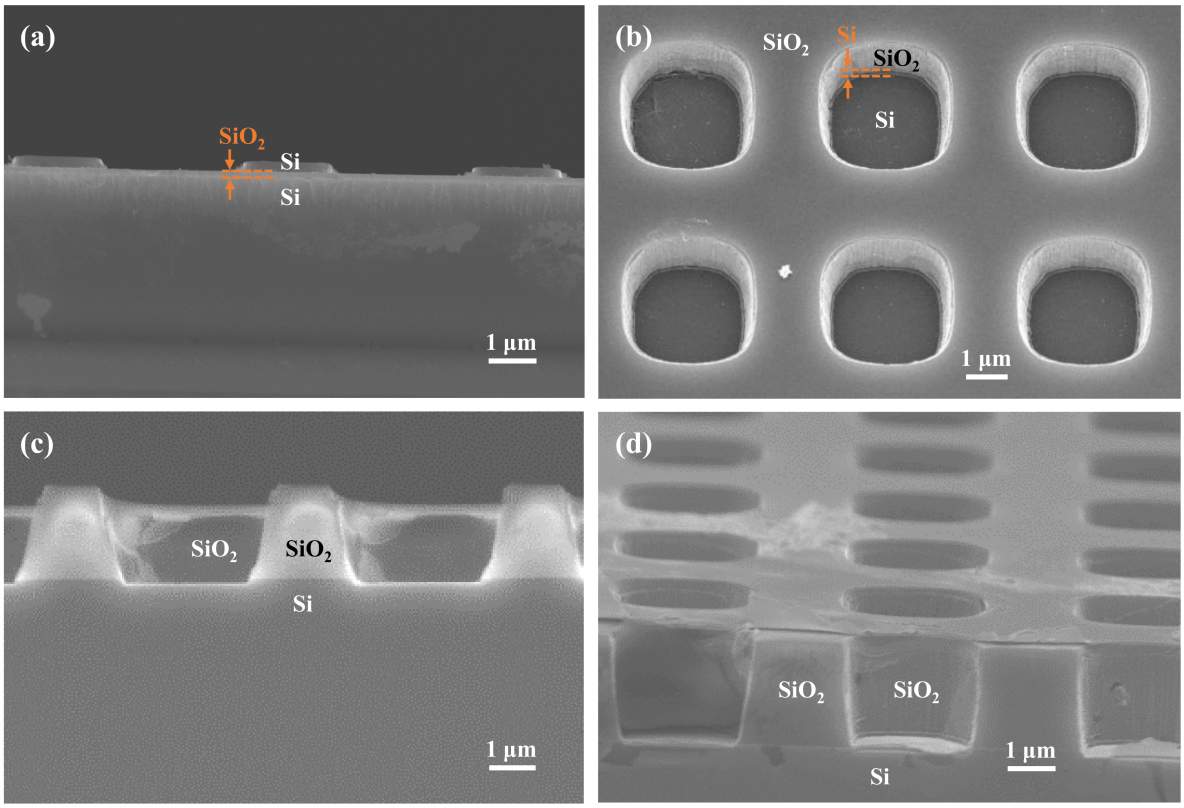

Figure 3. (**a**) Cross-sectional scanning electron microscope image of the releaser piece, (**b**) bird's-eye-view and (**c**) cross-sectional scanning electron microscope images of the receiver piece with an SiO_2 terrace before the submergence process, and (**d**) bird's-eye-view scanning electron microscope image of the receiver piece with an SiO_2 terrace after the submergence process.

For the reference receiver, after the cleaning, the Si wafer was spin-coated with a TDMR-AR80-5cp photoresist film of a thickness of 1.3 μm with a rotation velocity of 800 rpm. After the soft baking, the Si wafer with the photoresist was exposed in the same manner as the SOI wafer for 420 msec, followed by a development by TMAH aq. The areal region of the Si wafer not covered by the photoresist was dry-etched by SF_6 and C_4F_8 to a depth of approximately 2 μm. The residual photoresist on the Si wafer was removed by oxygen plasma. To clarify the structural difference between the SiO_2-terrace receiver and the reference Si-only receiver, Figure 4 depicts schematic bird's-eye views and cross-sectional views of these two types of receivers.

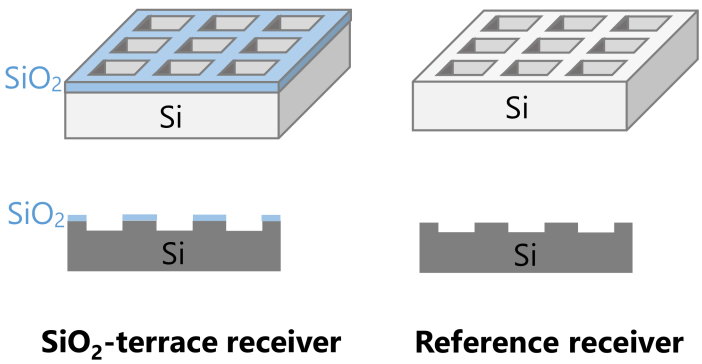

Figure 4. Schematic bird's-eye views and cross-sectional views of the SiO_2-terrace receiver and the reference Si-only receiver.

The patterned releaser and receiver wafers were diced into ~1-cm^2- and 25-mm^2-area pieces, respectively. A releaser piece was submerged, with its patterned face up, in a mixture solution of 2-mL hydrofluoric acid (HF) and 8-mL ethanol with ultrasonication at room temperature for 30 min, to release Si microchips into the solution by chemical etching of the BOX layer by HF. Subsequently, 40-mL ethanol and a receiver piece were added to the solution, and the solution was statically left without ultrasonication, with the receiver's patterned face up, at room temperature for 3 h, to deposit the Si microchips onto the receiver piece. By such a dilution of HF with the additional ethanol, we suppressed undesirable chemical etching of the terrace SiO_2 layer on the receiver piece. Figure 3d presents a bird's-eye-view scanning electron microscope image of the receiver piece with an SiO_2 terrace after the submergence process. As observed, the terrace SiO_2 layer on the receiver piece sufficiently survived in the submergence process. The receiver piece was then taken out of the solution with no cleaning process, and naturally dried in the atmosphere. In the submergence process, the SOI layer of the releaser piece is separated from the substrate by the selective dissolution of the BOX layer over Si by HF. Subsequently, the separated Si thin-film microchips (originally the SOI layer) are transferred in the solution and integrated onto the receiver piece.

3. Results and Discussion

Figure 5 shows typical plane-view scanning electron microscope images of the SiO_2-terrace receiver and the reference receiver. As observed in the scanning electron microscope image, some Si microchips were transferred into the pockets of the receiver piece. At this preliminarily stage of our experimental work, the yields of the process were observed as approximately 2% and 1% for the cases of the SiO_2-terrace receiver and the reference Si-only receiver, respectively, based on the fraction of the pockets of the receiver piece that are filled with the microchips. The poor statistics is a result of the random distribution of the microchips in a large volume of solution against a limited surface area of the receiver piece to deposit. Optimization of the submersion process, including the method of rinsing, may improve the yield in our future research. In practical applications, affinity force by electric [11] or magnetic [17,18] field could also be utilized, with proper installation of metal pads in the pockets of the receiver. Figure 6 presents the observed selectivity of the deposition of the Si microchips, depending on the area of the pockets of the receiver piece. We defined the deposition selectivity as the fraction of the number of the Si microchips observed in the pockets out of that on the whole surface of the receiver (i.e., pockets + terrace):

$$Deposition\ selectivity \equiv \frac{Number\ of\ chips\ deposited\ in\ pockets}{Total\ number\ of\ deposited\ chips}$$

We conducted two experimental runs for each of the main experiments with the SiO_2-terrace receivers (four kinds of pocket area) and the reference experiments with the Si-only receivers (five kinds of pocket area). The statistical data for Figure 6 were acquired from five independently separated parts for each of (two runs × nine conditions). For each part of the data acquisition, we counted more than two hundred deposited Si microchips. For the Si microchips, we used a single size of 2 μm × 2 μm × 200 nm throughout the experiments. Because of the constant size of the Si microchips to be transferred, it is natural to observe that as the area of the receiver's pockets increases, the deposition selectivity will increase. For the pocket sizes of around 6 μm^2, the deposition selectivities for the SiO_2 and Si (reference) terraces were about 0.6 and 0.2, respectively. For the pocket sizes of around 15 μm^2, the deposition selectivities were observed to be about 0.8 (SiO_2 terrace) and 0.6 (Si terrace). It is thus clearly observed that the employment of Si receivers with thermal oxide atop significantly enhances the deposition selectivity onto the designated pocket sites. In addition, the observed absolute selectivity value about 0.8 for the pocket size about 15 μm^2 for the SiO_2-terrace receiver is encouragingly high in terms of the practical realization of semiconductor fluidic self-assembly.

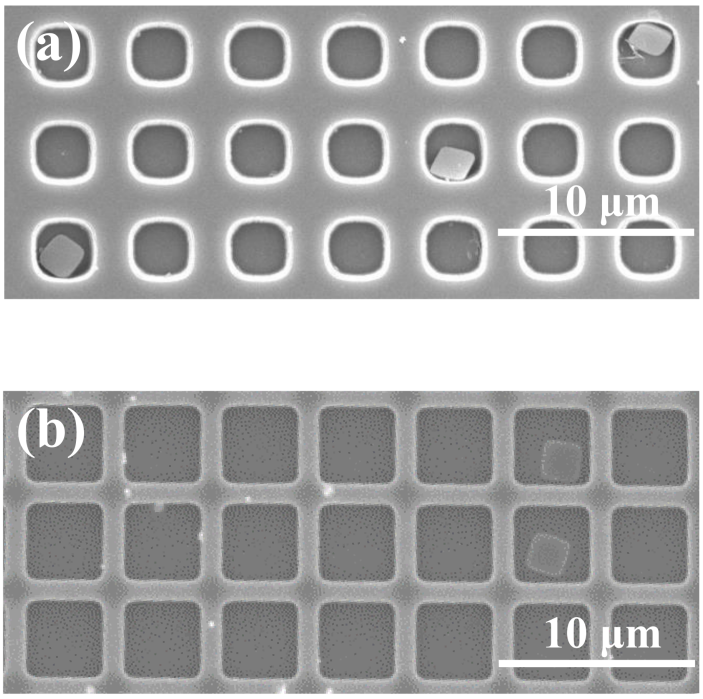

Figure 5. Typical plane-view scanning electron microscope images of (**a**) the SiO_2-terrace receiver and (**b**) the reference receiver.

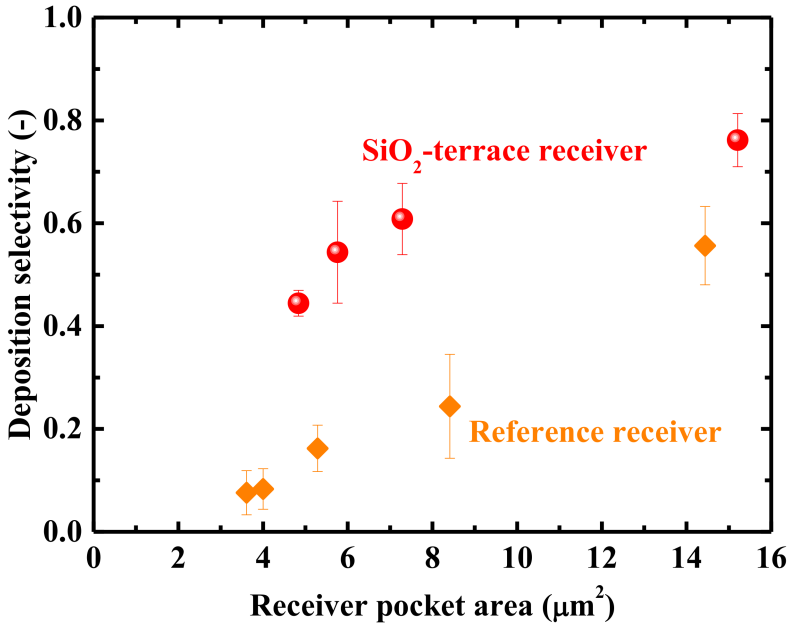

Figure 6. Deposition selectivity, defined as the fraction of the number of the Si microchips observed in the pockets out of that on the whole surface of the receiver (pockets + terrace), on the area of the receiver's pockets.

Let us quantitatively analyze the mechanism of the observed difference in the deposition selectivities between the cases of the SiO_2 and Si terraces on the receivers. It is thought that there are to be mainly three types of surface forces acting between two solids in sufficient proximity: the van der Waals force, the electrostatic Coulombic force, and the capillary force [19]. The electrostatic Coulombic force usually becomes unimportant in the presence of water, which partly compensates the charges on the surfaces [19]. The capillary

force is also considered insignificant when the solids are entirely submerged in a liquid. This is because the capillary force stems from the difference in the environmental phases on the inner and outer surfaces, e.g., when a narrow gap between two substances in a vapor is filled by a condensed liquid [19]. Therefore, we assume that the van der Waals force is the major interaction force in our experimental system. For simple two-body systems, the van der Waals force, F_{vdW}, can be expressed as follows [20].

$F_{vdW} = -\frac{A}{6D^2}\left(\frac{R_1R_2}{R_1+R_2}\right)$ (unit: force) for two spheres,
$F_{vdW} = -\frac{A}{6\pi D^3}$ (unit: force per area) for two flat surfaces facing each other, and
$F_{vdW} = -\frac{AR}{6D^2}$ (unit: force) for a sphere and a flat surface,

where R_1, R_2, and R are the radii of the spheres, D is the distance between the interacting bodies, and A is the Hamaker constant of the system. A negative F_{vdW} implies attraction (A positive), a positive F_{vdW} means repulsion (A negative). As seen in these equations, F_{vdW} is proportional to A, irrespective of deposition situation: surface-to-surface, corner-to-surface, or corner-to-corner. A is calculated as:

$$A = (\sqrt{A_1} - \sqrt{A_m})(\sqrt{A_2} - \sqrt{A_m})$$

where A_1, A_2, and A_m are the Hamaker constants of one of the materials in the system, the other material in the system, and the surrounding medium or fluid, respectively [20]. By using this equation, we calculated A for several representative systems. For the Hamaker constants of the materials used for the calculations, we employed the literature values [20–25]. We chose Si_3N_4, HfO_2, and ZrO_2 as representative of high-k dielectrics, and silsesquioxanes and allyl ethers as representative of low-k dielectrics. Because we could not find a value of the Hamaker constants of silsesquioxanes, we assumed it as 5.5×10^{-20} J deduced from the values of 5.5×10^{-20} J and 5.4×10^{-20} J for disiloxane and hexamethylcyclotrisiloxane, respectively [25]. Similarly, we assumed the representative Hamaker constant of allyl ethers as 4.5×10^{-20} J from the values of 4.1×10^{-20} J and 4.9×10^{-20} J for dipropyl ether and allyl acetate, respectively [25]. Appendix Table A1 presents the calculation results. The situation of our experimental system may lie between the cases that the medium is water and ethanol. The value of A of around 1.5 for the case that the interacting bodies are Si and SiO_2, corresponding to our main experiment, is significantly smaller than that of around 5.5 for the Si–Si case, corresponding to our reference experiment. This significant difference in A clearly explains the experimentally observed deposition selectivity. As a representative of existing materials with low permittivities, we tested for Teflon, and the resulted negative value of A for its case indicates a repulsive force between Si microchips and a Teflon-coated terrace and would be highly effective for selective self-assembly. From the list of Appendix A Table A1, the commonly used high-k material of HfO_2 and low-k materials of silsesquioxanes and allyl ethers exhibit significantly smaller values of A than the Si–Si case, owing to their significantly lower permittivities than that of Si. Therefore, it is implied that such common interlayer dielectric materials can be directly used as a terrace component of host chips in fluidic self-assembly. In contrast, incidentally, metals are inapplicable for this purpose because they have much higher absolute permittivities and thus larger Hamaker constants [20,22,23].

4. Conclusions

In this work, we fabricated Si receiver pieces with thermal oxide atop the terrace region between the pockets. We then statistically demonstrated an enhancement in the selectivity of microchip deposition to the designated pocket sites, relative to the case of the conventional Si-only receivers. The deposition selectivity increases with the size of the receiver pockets from approximately 0.4 to 0.8, which is larger than that of the Si-only receiver (0.1 to 0.6). We quantitatively analyzed the van der Waals force based on the Hamaker constants of the interacting materials in the fluidic system in relation to the observed selectivity. Additionally, from the analysis, we obtained an implication of synergetic use of the common interlayer dielectrics as terrace components.

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Appendix A

Table A1. Calculated Hamaker constants ($\times 10^{-20}$ J).

Material 1	Material 2	Medium	A_1	A_2	A_m	A
Si	Si	Water	18.65	18.65	3.7	5.74
Si	Si	Ethanol	18.65	18.65	4.2	5.15
Si	SiO_2	Water	18.65	6.50	3.7	1.50
Si	SiO_2	Ethanol	18.65	6.50	4.2	1.13
Si	Teflon	Water	18.65	2.75	3.7	−0.64
Si	Teflon	Ethanol	18.65	2.75	4.2	−0.89
Si	Si_3N_4	Water	18.65	16.70	3.7	5.18
Si	Si_3N_4	Ethanol	18.65	16.70	4.2	4.62
Si	HfO_2	Water	18.65	5.63	3.7	1.08
Si	HfO_2	Ethanol	18.65	5.63	4.2	0.73
Si	ZrO_2	Water	18.65	20	3.7	6.10
Si	ZrO_2	Ethanol	18.65	20	4.2	5.50
Si	Silsesquioxanes	Water	18.65	5.5	3.7	1.01
Si	Silsesquioxanes	Ethanol	18.65	5.5	4.2	0.67
Si	Allyl ethers	Water	18.65	4.5	3.7	0.47
Si	Allyl ethers	Ethanol	18.65	4.5	4.2	0.16

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