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Nanoscale silicon fluidic transfer for ultrahigh-density self-assembled integration

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Abstract

Fluidic self-assembly is an efficient fabrication technique that a large number of semiconductor chips are spontaneously integrated. However, the integrated chips in the experiments reported so far had dimensions of several tens of micrometers for the side lengths and thickness, hindered by the severe adhesiveness of smaller chips to their original substrates. Here we demonstrate fluidic transfer of submicron-scale chips. Simultaneous release and deposition of silicon thin-film chips are conducted in a blended solution of hydrofluoric acid and ethanol with ultrasonication, in relation to the surface tension. The mechanical bonding stability of the thin-film chips to the host chip is confirmed. Our scheme could lead to high-throughput, low-cost, and ultrahigh-density on-chip integration for electronic and photonic devices.

1. Introduction

Scaling down, high-density integration, and low-cost and high-throughput production are highly demanded in various optoelectronic devices, such as electronic large-scale-integration chips, light-emitting-diode displays, and photonic integrated circuits. The conventional pick-and-place integration method, however, has limitations for these required factors. Semiconductor wafer bonding is a skillful integration method, widely used in optoelectronics [1–6]. Fluidic self-assembly is a technique to integrate microscale chips released from multiple functional wafers onto a single host chip with selective bonding of each functional microchip to the designated site of the host chip in liquid phase [7–14]. For fluidic self-assembly, a large number of microscale chips can be simultaneously integrated, in contrast to the pick-and-place method. However, experiments of fluidic self-assembly in earlier studies have been carried out for semiconductor chips with dimensions of several tens of micrometers for both the areal size and thickness [7–14]. This dimensional status is presumably because of the severe, undesirable adhesion or re-adsorption of smaller chips to the surfaces of their original substrates. In the present study, we realize fluidic self-assembly of submicron-scale chips, towards ultrahigh-density integration.

2. Experimental

Figure 1 shows a schematic flow diagram of our experimental process of fluidic self-assembly. We used a silicon-on-insulator (SOI) ⟨100⟩ wafer with an SOI layer and buried-oxide (BOX) layer with thicknesses of both 200 nm and a silicon (Si) ⟨100⟩ wafer, for the microchip generator ('releaser') and the host chip ('receiver'), respectively. The square pillar- and pocket-shaped patterns of the releaser and receiver were photolithographically defined on the SOI and Si wafers, respectively, by dry etching. The etching depths were around 300 nm (i.e., about the middle of the BOX layer) and 1 μm for the SOI and Si wafers, respectively. Figure 2 shows typical plane-view scanning electron microscope images of the releaser and receiver wafers. Then, the patterned SOI and Si wafers were diced into ~1-cm^2- and 25-mm^2-area pieces, respectively. A pair of the releaser and receiver pieces was adjacently submerged, with their patterned faces up, in 10 ml of 10-% hydrofluoric acid (HF) aq. (HF : deionized water = 1:4 vol.) or a mixture solution of HF and ethanol (1:4 vol.) at room temperature for 3 h, as schematically shown in the inset of

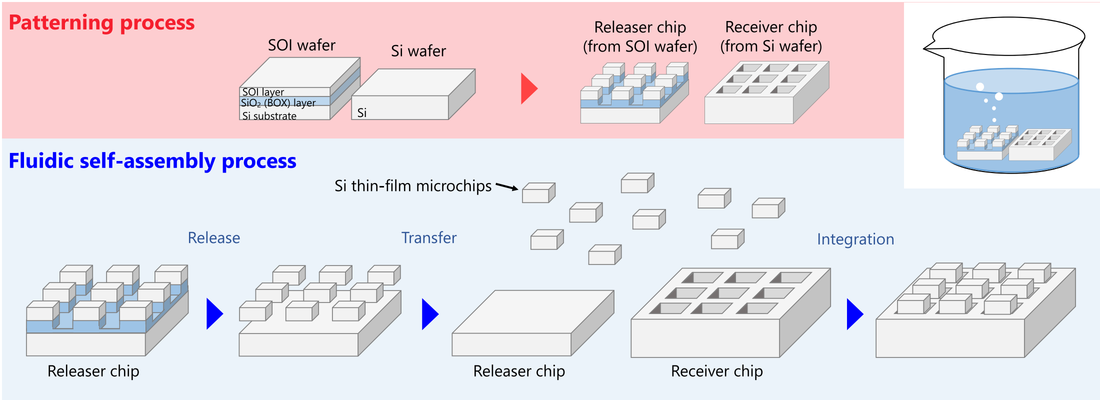

Figure 1. Schematic flow diagram of the experimental process of fluidic self-assembly. In practical applications, various-functional microchips from multiple kinds of wafers can be integrated into a single host chip, by site-selective transfer discussed in a later section. Inset illustrates the experimental configuration in the submergence process.

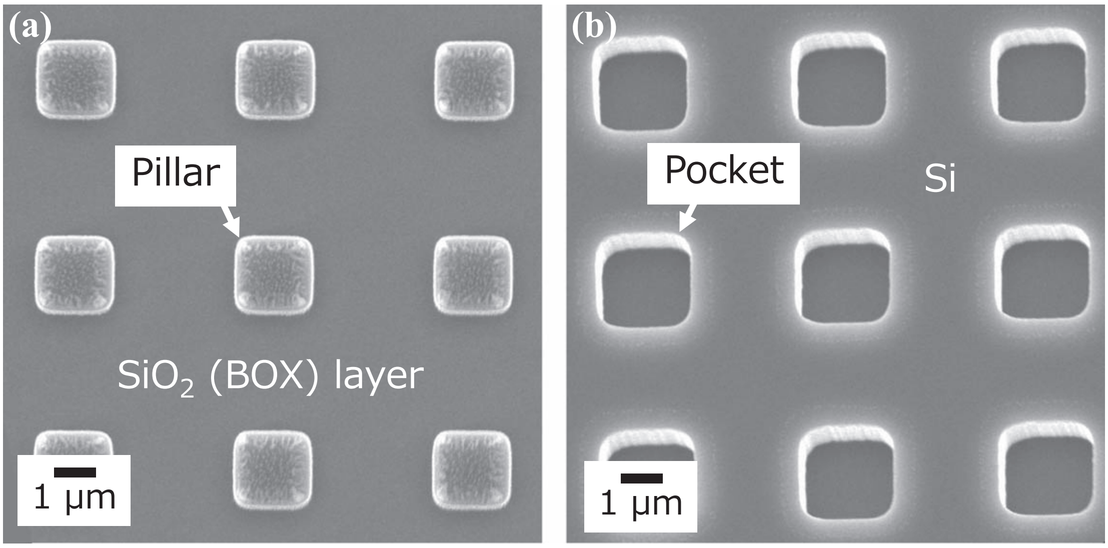

Figure 2. Plane-view scanning electron microscope images of the (a) releaser and (b) receiver wafers.

figure 1. The receiver piece was then taken out of the solution with no cleaning process, and naturally dried in the atmosphere. Note that the surface of the SOI and Si pieces becomes hydrophobic in the submergence owing to HF, and thus no apparent liquid existed on the pieces in taking out. In the submergence process, the SOI layer of the releaser piece is separated from the substrate by the selective dissolution of the BOX layer over Si by HF. Subsequently, the separated Si thin-film microchips (originally the SOI layer) are transferred in the solution and integrated onto the receiver piece. In this manner, the release, transfer, and integration of microchips are simultaneously conducted in a single step, leading to an efficient production process. To promote the separation of the microchips from the SOI wafer, we tested several external-force application methods: solution stirring, ultrasonication, heating, convective boiling, gravitational force by placing the releaser piece upside down, and nudging the releaser piece by tweezers. To test the mechanical stability of the bonded microchips on the receiver piece, we blew the samples after the fluidic self-assembly experiments, with a regular blower gun sourced by a house compressed-air supply gas line, for 1 min. The air velocity was set as 10 $m \cdot s^{-1}$, calibrated by a regular anemometer positioned at the equivalent distance from the blower gun.

3. Results and discussion

Figure 3 presents a cross-sectional scanning electron microscope image of the releaser piece submerged in the HF aq. for 10 min. It is observed that the BOX layer in the releaser structure is selectively etched over the top SOI layer and the bottom Si substrate. This selective dissolution or undercut of the BOX layer leads to the separation

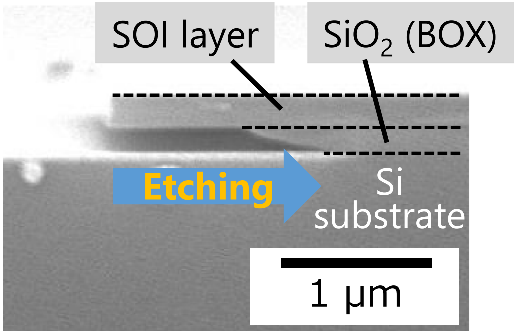

Figure 3. Cross-sectional scanning electron microscope image of the releaser piece submerged in the HF aq. for 10 min.

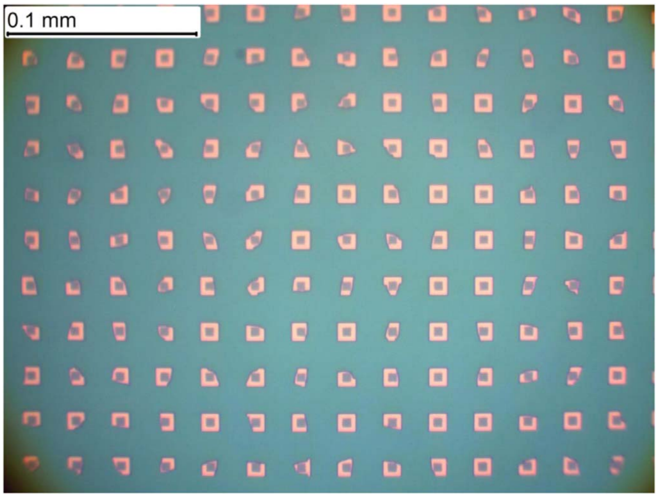

Figure 4. Plane-view optical microscope image of the releaser piece submerged in the HF aq. with ultrasonication. The bright parts and the grayish parts at the center of the bright parts correspond to the SOI and BOX layers, respectively.

of the SOI layer, as the transferred microchip in fluidic self-assembly. However, after the entire dissolution of the BOX layer, it was observed that most of the Si thin-film microchips (lifted-off SOI layer) adsorbed onto the Si substrate of the SOI wafer, and thus could not be released in the solution. After this situation, any of the abovementioned external-force application methods did not work for the separation of the thin-film microchips, except that nudging the releaser piece by tweezers partially separated the microchips, but with severely breaking them. This consequence can be attributed to the fact that the attractive van der Waals surface force is relatively large for such thin films (thickness: 200 nm), and therefore the Si surfaces easily stick to each other, hindering the planned release of the microchips. Then, we applied ultrasonication during, but not after, the submergence process in the HF aq., which worked, and the Si thin-film separation was conducted. However, partial breakage of the Si thin-film microchips was observed particularly for the microchips larger than several micrometers (figure 4). To address this issue, we found that a blend of HF and ethanol, rather than the conventional HF aq., effectively works for the separation of Si thin films from the SOI wafer with no damage. This result could be attributed to the difference in the surface tension between the solutions (water: 72.9 $mN{\cdot}m^{-1}$, ethanol: 22.4 $mN{\cdot}m^{-1}$ at room temperature [15]). Figure 5(a) presents a plane-view scanning electron microscope image of the transferred Si thin-film microchips into the pockets of the receiver piece, in the HF-ethanol solution with ultrasonication. The yield of the process was approximately 1%, based on the fraction of the pockets of the receiver piece that are filled with the microchips. The orientations of the microchips that entered the pockets of the receiver piece were observed to be random. We also observed the microchips adsorbed onto the terrace region between the pockets of the receiver piece, but not inside the pockets. At the present stage, we have no surficial selectivity for the microchip deposition between the pockets and the terrace region, relying only on the geographical stability inside the pockets represented by the attractive van der Waals force from the side walls. In actual applications, inertial force [16] or tunable affinity force by electric field [10], magnetic field [17, 18], or DNA [19, 20] can be used for selective attachment of each functional category of thin-film pieces into the designated spots. By combining with the earlier fluidic self-assembly of GaAs [7–10], or potentially other semiconductor

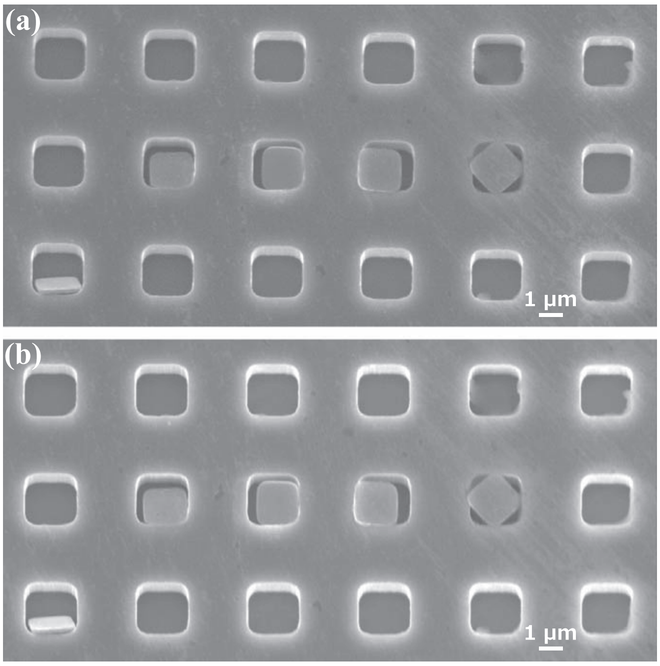

Figure 5. Plane-view scanning electron microscope images of the transferred Si thin-film microchips (a) before and (b) after air blowing at the velocity of 10 m·s^{-1} for 1 min.

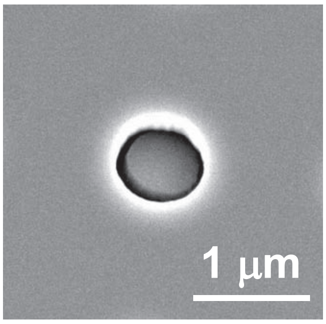

Figure 6. Plane-view scanning electron microscope image of the transferred submicron-scale Si thin film.

materials, the scheme of the present study can be applied for heterogeneous integrations, such as III–V-on-Si structures [4–6].

Figure 5 presents plane-view scanning electron microscope images of the transferred Si thin-film microchips before and after air blowing at the velocity of 10 m·s^{-1} for 1 min. The endurance, represented by the apparent invariance, of the sample against such a gusty wind verifies the sufficient interfacial mechanical bonding stability of the microchips for practical device applications. As a demonstration towards ultrahigh-density integration, we fabricated smaller releaser and receiver patterns. Figure 6 presents a plane-view scanning electron microscope image of a transferred smaller Si chip. As observed, a Si thin-film chip with a diameter of 0.8 μm was transferred to a pocket of the receiver piece. Incidentally, the rounded shape of the transferred chip and the receiver pocket is simply owing to the limitation of the spatial resolution in the photolithography process. Thus, the applicability of our fluidic self-assembly scheme for the integration of nanoscale chips is indicated.

4. Conclusions

In this study, fluidic self-assembly of submicron-scale chips was realized. The dimensions of the transferred Si thin-film chips were 800 nm in diameter and 200 nm in thickness, at the smallest. Simultaneous release and transfer of the thin-film chips were realized in a single step, in a single solution. Ultrasonication was observed to effectively suppress the re-adsorption of the released thin-film chips onto the mother Si substrate. A mixture solution of HF and ethanol, rather than the conventional HF aq., was found to minimize the damage on the thin-film chips by ultrasonication, by the control of surface tension. The mechanical bonding stability of the thin-film chips to the host chip was verified. Our scheme could lead to high-throughput, low-cost, and ultrahigh-density on-chip integration for electronic and photonic devices.

Acknowledgments

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