The Magnetic Tape System of the Kyoto University Digital Computer KDC-I

By

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This paper describes the details of the magnetic tape system of the Kyoto University Digital Computer KDC-I with emphasis on the design features and problems. The system was developed and built in collaboration with Hitachi, Ltd., and was attached to the main part of the computer in October 1960.

The tape is used only as a secondary memory and not as an input/output medium at present. The tape system includes magnetic tape handlers and a magnetic tape control unit which contains a high speed magnetic core memory. The main features of the tape system are:—concurrent operations of the tape and of the main part of the computer, a new block number system which was named a variable block number system, an instruction system which enables a simple treatment of the drop-out problem of magnetic tape, noise suppression and the correction of time displacement error by using the KDC-I basic logic circuits, and so on.

In spite of difficulties at the time of the design of the system, the completed tape system satisfies the required functions and is utilized almost daily at the Kyoto University Computation Center.

1. Introduction

In this paper, the details of the magnetic tape system which is connected to the main part of the Kyoto University Digital Computer KDC-I are presented with emphasis on design features and problems[1]. A brief description of the subject, however, was given in a previous paper in connection with the description of the computer[2].

The magnetic tape system as well as the central processing unit was developed and built in collaboration with Hitachi, Ltd. The authors contributed mainly to the system design and the logical design of the magnetic tape system, while the construction of the system was made by the manufacturer. The authors also co-operated in the adjustment and testing of the system, and

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are now helping in the maintenance of the system.

The magnetic tape of the KDC-I is used for the storage of intermediate results and is also used for permanent storage of programs and data. At present the magnetic tape cannot be used as an input/output medium. The system includes magnetic tape handlers and a magnetic tape control unit which contains a high speed magnetic core memory. Up to four magnetic tape handlers can be connected to the magnetic tape control unit; this unit is connected to the main part of the computer. At present two magnetic tape handlers are connected and utilized[3].

The magnetic tape system was attached to the main part of the computer in October 1960. The adjustment of the tape system until various magnetic tape test programs produced by the Kyoto University Programming Group[4] were operating correctly consumed almost three months owing to lack of experience. Thus the adjustment ended in December 1960. However, some faults were found afterwards and were corrected in May 1961. Since then the magnetic tape system has been in constant use. The high speed magnetic core memory in the tape control unit is fully utilized since the memory of the main part of the computer is a medium speed magnetic drum memory.

The system design of the tape system was carried out as a part of the design of the whole system. The logical design of the tape system was completed by October 1959. Owing to lack of experience and because the manufacture of the system should have been officially completed by March 1960, the functions of the system were not made too complex. Nevertheless various trials were made. The main features of the tape system can be said to be the concurrent operation of the tape and of the main part of the computer, a new block number system which was named a variable block number system[5] and an instruction system which enables a simple treatment of the drop-out problem of magnetic tape.

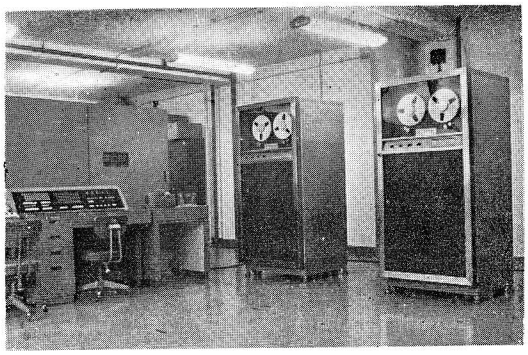

Fig. 1. View of the magnetic tape system of the KDC-I.
From left to right; the central processing unit and the operator's console, the tape control unit, and the two magnetic tape handlers.

The magnetic tape system of the KDC-I is believed, so far as the authors are aware, to be the first successfully operating

tape system in a domestic computer. In Fig. 1 a view of the magnetic tape system of the KDC-I is shown.

The magnetic tape system of the KDC-I is at present a secondary memory. Since the output capability of the computer is weak, it is strongly hoped that the magnetic tape can serve as an input/output medium. However, this plan has not been realized, mainly for economic reasons.

The following abbreviation will often be used in this chapter:

CPU : Central Processing Unit or Main Part of the Computer.
TCU : Magnetic Tape Control Unit.
MTH: Magnetic Tape Handler.
MT : Magnetic Tape.
CB : Core Buffer or Magnetic Core Matrix Memory.
LP : Load Point of the Magnetic Tape.
TE : Tape End.
TC : Tape (Parity) Check.

2. Organization of the Magnetic Tape System

Various tape systems were suggested. However, the following system was proposed and constructed. The main points will be described in turn.

(1) The use of the magnetic tape whose width is approx. 12.7 mm (1/2″), with length approx. 1,100 m (3,600 ft.), and which is capable of storing as many as 7,000 50-word blocks.

(2) The use of the magnetic tape handlers whose magnetic tape operation speed is approx. 150 cm/sec (60 inches/sec) in both forward and backward directions, and whose magnetic tape starting and stopping time is approx. 7 ms. The MTH has an 8-channel read/write head and an erase head which is situated approx. 6 mm apart from the read/write head. The main controlling mechanism is composed of an electromechanical control mechanism and a pneumatic one. Up to four MTH's may be connected to the computer; two of them were actually made.

(3) The biggest problem with regard to design was the use of MT as an input/output medium. This plan has not been realized mainly for economic reasons.

(4) The next important problem was the selection of the type of buffer storage. Two plans were suggested. One was the use of a portion of the drum memory for buffer storage. The other was the use of the magnetic core matrix memory. The former plan was apparently more economical than the latter. Nevertheless the latter plan has an im-

portant merit. Since the instruction system of the computer is one-and-a-half address and the memory of the main part of the computer is a medium speed magnetic drum, the problem of the access time of the memory was very serious, even though a delay-line type quick access memory was made. Thus by installing a high speed core matrix memory, even if the capacity were small, the processing speed of the computer could be expected to become much faster than in the case of the former plan. The latter plan was finally accepted, and a 50-word core matrix was decided upon for construction. The capacity of 50 words is almost a minimum feasible limit for this type of computer and was chosen mainly for economic reasons.

(5) The block diagram of the system was thus decided upon to be the one shown in Fig. 2. Up to four MTH's can be connected to the TCU, which is then connected to the main part of the computer. At present only two MTH's are connected. The TCU contains a 50-word magnetic core matrix buffer storage or core buffer (CB).

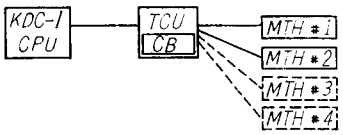

Fig. 2. Block diagram of the magnetic tape system.
Dotted lines show the units scheduled for installation.
CPU : Central Processing Unit,
TCU : Tape Control Unit,
CB : Core Buffer,
MTH : Magnetic Tape Handler.

(6) The CB is used not only as a buffer storage, but also as high speed storage registers, whose addresses are from 4,200 to 4,249, and whose access time is 50μs.

(7) The concurrent operation of the magnetic tape and of the main part of the computer should be possible. Thus the processing speed is expected to increase.

(8) The rewind operation should be done concurrently with other tape operations.

(9) The magnetic tape code should be the same as the paper tape code, though for the time being only numerical characters are used. Thus the design of various off-line units is expected to become easier.

(10) Information is written on MT as a 50-word block mainly because the capacity of the core buffer is 50 words.

(11) To ensure the reliability of the magnetic tape system, an odd parity bit is added to each character code (In the case of the magnetic tape system the sprocket is counted as a bit while in case of paper tape it is

not counted) and an even parity bit is added to the end of each channel of a block. The former will be called a character parity, and the latter a channel parity.

In case of reading, both parity bits are examined. If a parity error is detected, a Tape Check indicator (TC-indicator) is turned on, but the computation does not stop. The state of the TC-indicator can be examined by an instruction. Thus by programming, various treatments for this situation become possible, e.g., to try to read once again, or erase that portion of MT, and so on.

In the TCU, the parity and validity checks are made. In the core buffer, every digit has an even parity bit. They are examined when reading and writing.

(12) A new block number system which is named a variable block number system was adopted. Any four-digit block number can be written at the head of a 50-word block during the write operation on the magnetic tape. Thus the block number is not fixed on the MT beforehand like other systems. Flexibility concerning the use of the block number is expected to increase.

(13) Nine computer instructions are added for the operation of magnetic tapes. Two more instructions are also made for the block transfer of information between the core memory and the drum memory. Briefly the operations of these tape instructions are: writing, reading, testing, erasing, rewinding, and detecting the tape end and parity error. Under this instruction system, it is possible to avoid defective portions of the magnetic tape, to detect the file end by using the block number, and so on, by suitable programming.

(14) The control panel is attached to the TCU, which is used for the local supervision of the operations of the TCU and of the MTH's, the TCU check and local adjustment, though most of the magnetic tape operations can be supervised at the operator's console.

3. Magnetic Tape (MT)

Various length of MT whose width is 12.7 mm can be used. Both ends of the MT are perforated for the purpose of sensing the load point and the tape end. The speed of the MT is 150 cm/sec in case of reading and writing. On the MT, a 50-word block is written as a unit. The block length on the MT is approx. 11 cm. The inter-block gap is approx. 4 cm. The read/write head is expected to be situated in the middle of the inter-block gap when

the MT is stopped (2 ± 0.2 cm from the end of a block or from the beginning of a block).

A standard reel for the MTH contains 1,100 m (3,600 ft.) of MT, which can store as many as 7,000 blocks or 350,000 words.

1. Magnetic Tape Character Coding

The same codes as for paper tape are used; however, the arrangement and the variety of codes used are different. The position of the character parity is at the edge of the MT. All these codes are written magnetically by the instruction BTP. Since the magnetic tape is used only as an auxiliary memory, not as an input/output at present, 16 varieties of codes are used. In Fig. 3 the magnetic tape character coding is shown.

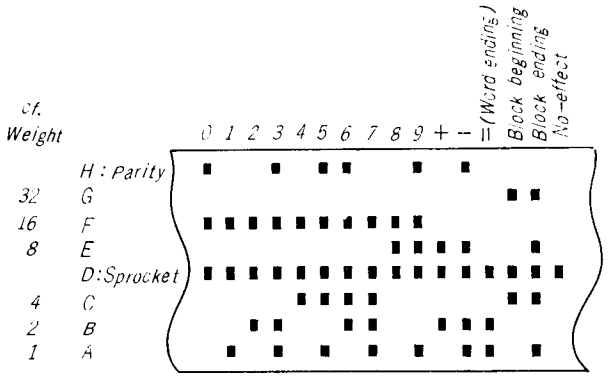

Fig. 3. Magnetic tape character coding.

2. Layout of a Block on the Magnetic Tape

A 50-word block is written on the MT by the operation of the instruction BTP. A brief drawing of the layout of a block on the MT is shown in Fig. 4.

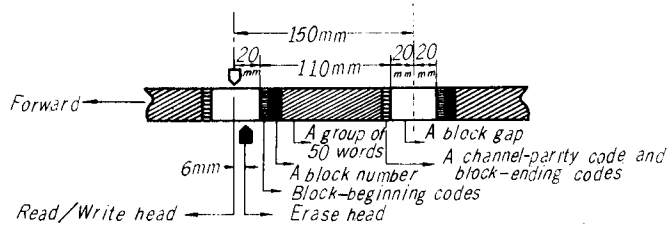

Fig. 4. Layout of a block on the magnetic tape.

The information is written in the following way:

(1) four block-beginning codes.

(2) one no-effect code.
(3) four numerical codes as a 4-digit block number.
(4) one no-effect code.
(5) 50 words of information, the arrangement of which is shown in Fig. 5. (each word is terminated by the word-ending mark ||).

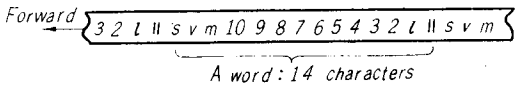

Fig. 5. Layout of a word in the block.
s : Sign bit, v : Overflow bit,
m: 11th or most significant digit,
l : 1st or least significant digit,
|| : Word-ending mark.

(6) one no-effect code.
(7) a channel parity code ; in each channel, the number of 1's is made even by this code.
(8) after these seven kinds of codes, four block-ending codes are written at the end of a block.

The block-beginning codes and the block-ending codes are used for controlling the movement of the MT.

The block number and the sprocket bits are not written beforehand, but are written at the time of the operation of the instruction BTP. Any 4-digit block number can be written. The block number is used for the search and the confirmation of a block in programming.

3. Read and Write Operations

An 8-bit code of each character is written simultaneously through an 8-channel read/write head of an MTH with a density of 64 characters per cm by the biased NRZ (Non-Return-to-Zero) method. The principle of this method

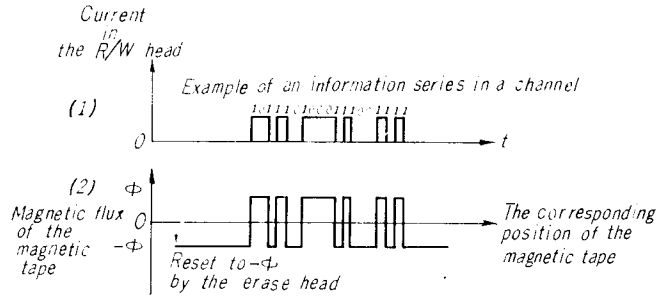

Fig. 6. Principle of the write operation.

is illustrated in Fig. 6. The erase head erases the MT and sets its magnetic flux $-\phi$; the current in the read/write head flows as shown in Fig. 6 (1). Then the magnetic flux of the MT becomes as shown in Fig. 6 (2); the flux is changed only when "1" is written, and is unchanged when "0" is written.

When reading information from the MT, the derivative of the flux is detected at the read/write head, the polarity is rearranged, and the waveform is reshaped, as shown in Fig. 7.

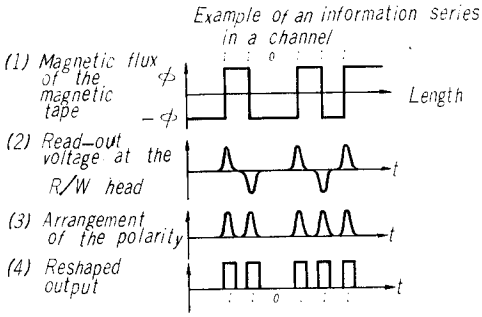

Fig. 7. Principle of the read operation.

The information density per channel is thus 6.4 bits/mm, or 3.2 pulses/mm, while the speed of a read/write operation is 9,600 characters/sec. Since these operations are performed through one read/write head and one erase head, simultaneous read and write operations are not possible.

4. Magnetic Tape Handlers (MTH's)

An MTH is a mechanical device in which a reel of MT is placed and used. The main parts of the MTH are a controlling mechanism, a read/write head, an erase head, a tape-end (TE) detector, a load-point (LP) detector, the file protector, and the ready indicator. The controlling mechanism is composed of electro-mechanical and pneumatic control mechanisms.

The position of the MT is shown schematically in Fig. 8.

The movement of the MT is controlled automatically by the computer, but if necessary it can be controlled manually at the MTH. Both ends of the MT are perforated for the purpose of sensing the tape-end and the load-point of the MT, and are detected by the TE or LP detector, and if detected, the movement of the MT is automatically stopped.

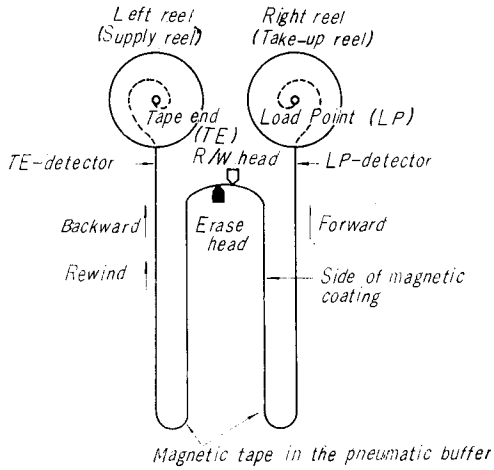

Fig. 8. Position of the magnetic tape in the MTH mechanism (A front view).

In either forward or backward motion of the MT, the MT is driven at the constant speed of 150 cm/sec except for a few milliseconds while starting and stopping. In the case of the rewind motion of the MT, the MT is rewound to its load point, and the motion cannot be interrupted if once initiated. The time needed for the rewind depends upon the length of the MT to be rewound, but roughly, the average speed of the rewind is assumed to be three times faster than the ordinary 150 cm/sec.

5. Magnetic Tape Control Unit (TCU)

All magnetic tape operations are controlled mainly by the TCU. The magnetic core memory in the TCU is used as a high speed memory whose locations are from 4,200 to 4,249, and also as a buffer storage for read and write operations of the magnetic tape.

If an instruction concerning the magnetic tape operation is decoded by the main part of the computer, it will be transmitted to the TCU, and the execution begins under the control of the TCU; the computer takes the next instruction in sequence and proceeds from there concurrently if the instruction does not refer to the TCU or the MTH under operation. If this is not the case, the execution of the next instruction is delayed until the execution of previous instructions finishes. Therefore by suitable programming it is possible to

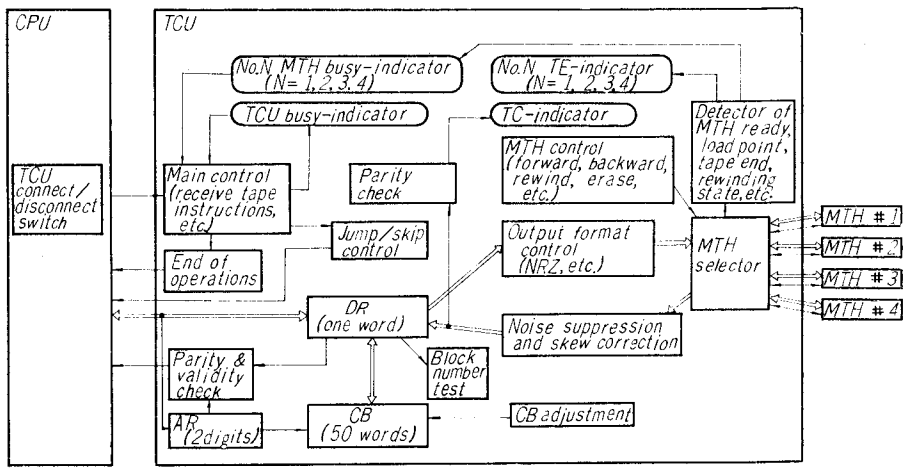

Fig. 9. Block diagram of the TCU of the KDC-I.
CPU: Central Processing Unit, TCU: Magnetic Tape Control Unit, MTH: Magnetic Tape Handler, CB: Core Buffer, DR: Distributor Register, AR: Core Address Register, TE: Tape End, NRZ: Non-Return-to-Zero form of output signal,
⟺: Information, ↔: Control signals.

increase the processing speed. In programming, however, instructions should be regarded as executed one after another in sequence.

In Fig. 9 a block diagram of the TCU is shown. Each small block in the diagram is classified accoding to the function it performs. Thus the name which is given to each block represents one of the followings: the name of a function unit, a register or an indicator, or the function of a block.

The details of the TCU are now explained; most of the functions of the blocks are also described.

(1) The same type of transistorized dynamic circuit used for the CPU is also used for most of the circuits in the TCU, because it is simple to connect the TCU to the CPU, the logical design can be done in the same way, and moreover there was little time available for developing a suitable static circuit. However, it was foreseen that the use of static circuits for the whole TCU would have simplified the logic circuits.

(2) The CB has the capacity of 50 words with 50μs (or one word time) access time. One word or 12 decimal digits has 60 bits since each dight has a parity bit. The actual CB is of a current-coincidence type and consists of 100 30-parallel-bit words with 17.4μs access time, and for 60 bits of information two cycles are used. The structure of the core matrix is of 4×25 (address)$\times30$ (parallel bits), with five 4×25 matrices constructed in each plane; Thus six planes are used in all. The S-1 type ferrite cores of the General Ceramic Co. were used since domestic cores did not fully satisfy requirements at the time of the design.

(3) The selection of a particular MTH out of the four MTH's is made by using reed relays whose operation time is of the order of a few milliseconds. At present there is no problem concerning the noise and life of the relays. However, the use of an electronic switch would be better from the standpoint of the above mentioned factors though the use of mechanical relays for this circuit are more economical even at present.

(4) There are two important registers in the TCU, i.e., a Distributor Register (DR) and a Core Adress Register (AR). All information read from or written to the magnetic core memory or the magnetic tape memory is stored temporarily in the DR. The DR has 12 digits, the capacity of a word. Moreover each dight has a parity bit. The main functions of the DR are the series-parallel conversion and the buffering action between the tape and the CB. The even parity and the validity of the code are examined at the DR, and since all information flows in the DR, error checking for the operation of the CB is made by this checking circuit.

The AR is used to specify the location of the core memory. Since it is used only for the 50-word core memory, the AR has a 2-dight capacity, and the two least significant dights of the core location are stored in the AR. The validity checking is also made here.

(5) The output format is controlled in the TCU. The NRZ (Non-Return-to-Zero) signal is generated by flip-flops in the TCU, transmitted to the MTH, amplified and reshaped in the MTH, and written on the MT.

The even channel parity code at the end of a block is made by resetting the final state of the flip-flops since the flip-flops are modulo 2 counters. The odd character parity on the even channel parity is realized by properly arranging the number of characters in a block. All these check codes are examined in the case of reading. Characters are written at the rate of 9,600 characters/sec, that is, every 104μs (every two-word time) a character is written.

(6) In Fig. 10 the input circuit of a channel in the TCU is shown. There are eight such input circuits in all. The read-out signal from the read/write head is amplified and reshaped in the MTH, and then transmitted to the TCU by a coaxial cable (RG 58A/U and less than 10 meters long). After passing the relay MTH selector circuit, the signal is applied to the basic logic circuit of the computer. Then the duration of the signal or pulse is measured by the counter or the logic circuit SAi and SBi. If the pulse count is greater than 4 or the duration of the pulse at the

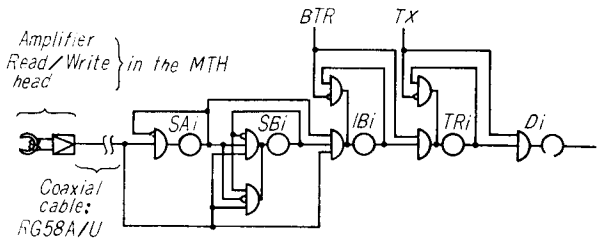

Fig. 10. Input circuit of a channel in the TCU.

output of the amplifier exceeds approx. 17.4μs, the pulse is recognized as a signal and temporarily stored in IBi, otherwise it will be recognized as a noise. The circuit is a sort of a digital integration circuit used for the suppression of noise. Since there would be a time displacement error among the timing of signals in each channel, and skewness of the MT would probably cause a great deal of error, the output signal from the sprocket channel which is in the center of the MT is used as a reference.

Since the signal comes approximately once every 104μs, and the signal at the IBi must be read into the DR in synchronization with the timing of the DR, the signal temporarily stored in the IBi should be tranferred to another temporary storage TRi which functions as a synchronization buffer. The transfer timing BTR is given 52μs after the sprocket signal is detected at the output of the noise suppression circuit. Thus the permissible time displacement error is approx. $\pm 40\mu$s with reference to the sprocket signal. Moreover the permissible limit concerning the instantaneous compression of the timing of the signal is approx. 60μs. Any degree of expansion of the timing is permissible in so far as the time displacement error is within this range. The signal in the TRi is transferred into the DR with the necessary timing, say, Tx as shown in the figure.

(7) Parity checking is made on all information which is utilized. For example in the case of the instruction BLS or Block Search, the character parity of all block numbers tested is examined in addition to the parity check of the object block. If parity error is detected in the case of reading, the TC-indicator is turned on, but the computation does not stop.

If parity or validity error is detected at the DR at the time of reading information from the MT, the TC-indicator is also turned on. Except in the above case, the error will cause the computation to stop.

The channel parity is examined by the same flip-flops which are used for making the NRZ output signal, i.e., by counting the input signal in modulo 2 fashion.

(8) The concurrent operation of the CPU is performed by introducing two kinds of busy-indicators, i.e., a TCU busy-indicator and No. N MTH busy-indicators (N=1, 2, 3, 4). By most of the tape operations, both TCU and MTH busy-indicators are turned on. But in the case of rewinding the MT, only a particular MTH busy-indicator is turned on.

(9) Since the TCU has rather an independent control function, it was simple to add an adjustment circuit. In the main control circuit of the TCU there are several flip-flops which receive tape instructions from the CPU. It was made possible to trigger these flip-flops manually at the control panel. Thus in the case of local adjustment, most of the magnetic tape instructions can be executed by depressing the corresponding buttons on the panel.

The CB adjustment circuit was also attached to the TCU. The function of the circuit is to reset the contents of all core memory, read all contents repeatedly, write all zeros, all ones, or else two of the very

unfavorable patterns into the core memory (when reading, the S/N ratio is believed to be the lowest).

Thus most of the adjustment of the CB and the tape operations can be done at the TCU control panel. This function of the TCU has actually been utilized since the TCU was constructed and it had to be adjusted without the CPU after the CPU was installed at the University.

6. Magnetic Tape Operations

The reliability of the MT was still an unknown factor at the time of the design. However it could easily be foreseen that there would be some defective spots on the MT and that the number of such spots might increase during use.

Thus after writing, the information on the MT should be tested (parity checking), and, if error is detected, that portion should be erased.

Nine instructions are added to the computer for the operation of the MT. Two more instructions are also made for the block transfer of information between the core memory and the drum memory.

Block number

A new block number system was adopted in which any 4-digit block number can be written at the time of writing information on the MT. Since a block number is not fixed on a particular portion of the MT and can be changed if necessary, this block number system was called *a variable block number system*[5].

This system can be applied in the following way:

(1) Sequential numbering is possible.

(2) An index number of data or a number converted from the orginal index number may be used as a block number. For example, the storage of subroutines can be made in this way.

(3) The use of MT as an addressable memory can be performed by writing suitable block numbers on the MT beforehand. The sequence of the numbers can be selected arbitrarily.

(4) The use of a certain number as a special control code is possible.

(5) A quick access memory can be realized by storing the same information with the same block number on several portions of the MT.

(6) If a portion of MT becomes defective it is possible to rewrite the same information on another good portion of the MT without changing the block number.

Details of the operations of the magnetic tape instructions

The definition of the operations of the magnetic tape instructions is now given. The numerical code, the symbolic code, the name of an instruction, and the operation time in ms are written first. The instruction system of the KDC-I is one-and-a-half address, consisting of a 3-digit function part and a two-digit index part (which is used not only for the specification of an index register, but also for the specification of the number of the MTH), a 1-digit break-point part, and a 4-digit address part.

The operation time is unchanged whether or not the modification of the address of an instruction takes place. The time for the modification is included in the operation time. For the instructions which permit concurrent operation, the time needed for the CPU is written first, the time needed for the TCU second, and the time needed for the MTH third. Ai stands for the instruction access time, and Aa the data access time. The symbol ♯ is used to show the modification of an address. Other symbols and abbreviations used are commonly accepted ones; however, full details can be found in the previous paper[2].

Next the definitions follow, and some notes are added if necessary.

910 **BTP NJ A** "Buffer to Tape" (0.45+Ai; 220)

The erasure of the MT of the MTH specified by N begins, and the MT is started forward. A block number ♯JA and 50 words in the core memory are written as a block on the successively erased portion of the MT.

Next the MT is stopped and the erasure is also stopped.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N MTH busy-indicator is in "on" state by previous instructions, until both are restored to the "off" state.

2. After 0.45 ms from the beginning of the execution, the next instruction in sequence becomes operative concurrently. During the operation, the TCU and the No. N MTH busy-indicators are on, i.e., for 220 ms.

3. If the No. N TE-indicator has been on, the operation is equivalent to NOP. If the No. N TE-indicator is not on during the write operation, the MT stops only after finishing the operation.

4. If the MT starts from its load point, the writing of information begins after the MT leaves the load point.

936 **ETP N· -** "Erase Tape" (0.45+Ai; 220)

This instruction erases the MT for the length of a block and an inter-block gap.

N.B. 1. The same operation as that of BTP is done except that this instruction does not write on the MT. Thus only erasure takes place.

912 **TPB NJ A** "Tape to Buffer" (17.0+Ai; 220)

The MT of the MTH specified by N is started forward. The nearest block is to be read. A block number is read and compared with #JA; if it is equal, the control skips the next instruction in sequence; if it is not equal, the sequence is normal. The next instruction in sequence becomes operative concurrently from this time on (approx. 17 ms from the begining of the execution). A block of information is read and stored in the core memory. Next the MT is stopped. During the operation, the TCU and No. N MTH busy-indicators are on, i.e., for 220 ms in the usual case.

If errors in the character parity and/or the channel parity are detected, the TC-indicator (and the lamp on the console) is set on, but the computation dose not stop.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N MTH busy-indicator is in the "on" state by previous instructions, until both are restored to the "off" state.

2. If the No. N TE-indicator has been on, the operation is equivalent to NOP. If the No. N TE-indicator is set on during the read operation, the operation is still performed as usual.

3. If no block can be found, the computer searches until the tape end is detected, and the operation becomes NOP.

914 **BLS NJ A** "Block Search" (0.45+Ai; 100×n+120)

The MT of the MTH specified by N is started foreward. A block whose block number #JA is searched for reading. Each block number is successively read and compared with #JA, and when a block number equals to #JA for the first time, this block of information is read and stored in the core memory. Next the MT is stopped.

The character parity is examined for all the block numbers which are read and compared. The character parity and the channel parity are examined on the block information whose block number is #JA. If parity error is checked, the TC-indicator (and the TC-indicator lamp on the console) is set on, but the computation does not stop.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N MTH busy-indicator is in the "on" state by previous instructions, until both are restored to the "off" state.

2. After 0.45 ms from the beginning of the operation, the next instruc-

tion in sequence becomes operative concurrently. During the operation, the TCU and the No. N MTH busy-indicators are on. The time needed depends upon the place of the block, and is roughly equals to (100 ms) × (a number of blocks passed under the reading head) + 120 ms.

3. If the TE-indicator has been on, the operation is equivalent to NOP. If the TE-indicator is set on during the reading of the object block, BLS is performed as usual.
4. If no object block can be found, the instruction searches until the TE is detected, and the operation becoms NOP. If the computer fails to detect the block, it is often useful to depress the HALT button and the TE-button on the console; then the current BLS operation becomes NOP and the computation stops.

934 **TTP N· -** "Test Tape" (0.45+Ai; 220)

The MT of the MTH specified by N is started forward. The nearest block is read only for checking the character parity and the channel parity without storing the information in the core memory. The MT is then stopped. If parity error is detected, the TC-indicator (and the lamp on the console) is set on, but the computation does not stop.

N.B. 1. The same notes as for TPB (N.B. 1. 2, 3) are applicable.

2. After 0.45 ms from the beginning of the execution, the next instruction in sequence becomes operative concurrently. During the operation, the TCU and No. N MTH busy-indicators are on (ordinary approx. 220 ms).

932 **BST N· -** "Backspace Tape" (0.45+Ai; 220)

The MT of the MTH specified by N is started backward. The nearest block is read backward only for checking the character parity and the channel parity without storing the information in the core memory. The MTH is then stopped. If parity error is detected, the TC-indicator (and the lamp on the console) is set on, but computation does not stop.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N MTH busy-indicator is in the "on" state by previous instructions, until both are restored to the "off" state.

2. After 0.45 ms from the beginning of the execution, the next instruction in sequence becomes operative concurrently. During the operation, the TCU and the No. N MTH busy-indicators are on (ordinary approx. 220 ms).

3. If the MT is at load point, the operation is equivalent to NOP. During the BST operation, the load point is never detected (c.f. N.B. 5. of BTP) in the usual case.
4. If no block can be found, the computer searches until the load point is detected, and the operation becomes NOP.
5. As a result of the backward motion, the No. N TE-indicator is turned off.

930 **RWD N·** - "Rewind" (0.45+Ai; 20; av. approx. 450 cm/sec)

This instruction causes the MTH specified by N to rewind the MT to its load point.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N MTH busy-indicator is in the "on" state by previous instructions, until both are restored to the "off" state.
2. If the MT is at load point, the operation is equivalent to NOP.
3. As a result of the backward motion, the No. N TE-indicator is turned off.
4. After 0.45 ms from the begining of the execution. the next instruction in sequence becomes operative concurrently. After approx. 20 ms (=time for TCU busy) from the beginning of the execution, a MTH other than No. N can be used concurrently.
5. The time needed for the rewinding of the MT (=time for No. N MTH busy) depends upon the length of the MT to be rewound. As a very rough estimate the speed of the rewind is about three times faster on the average than the ordinary 150 cm/sec.

950 **JTG ·J A** "Jump on Tape Good" (0.45+Ai)

The control jumps to loc. ♯JA if the TC-indicator is off (the MT is supposed to be good), otherwise it moves in normal sequence. The TC-indicator is turned off at the end of the operation.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N MTH busy-indicator is in the "on" state by previous instructions, until both are restored to the "off" state.
2. The time needed for the execution is 0.45 ms.

952 **JTE NJ A** "Jump by Tape End" (0.45+Ai)

If the TE-indicator of the MTH specified by N is on, the control jumps to ♯JA, otherwise it moves in normal sequence. The TE-indicator is not affected by this instruction.

N.B. 1. The execution of the instruction is delayed, if the TCU or the No. N

MTH busy-indicator is in the "on" state by previous instructions, until both are restored to the "off" state.

2. The time needed for the execution is 0.45 ms.

920 **DMB ·J A** "Drum to Buffer" (2.90+Ai+Aa)

c(E), ···, c(EL) → c(4200), ···, c(4200+EL−E).

E=♯JA, $0 \leqq EL-E < 50$, and $EL \equiv 49$ in modulo 50.

The c(E) replace the c(4200), ···, and the c(EL) replace the c(4200+EL−E). Thus a group of words is transferred to the core memory from the drum memory (both normal and quick access bands.).

N.B. 1. Contents of registers other than the c(4200), ···, c(4200+EL−E) are unchanged.

2. If $4200 \leqq E \leqq 9999$, zeros replace the c(4200), ···, c(4200+EL−E).
3. A number in the Xx part is neglected in the operation.
4. If the core memory has been busy with some tape operations, the execution is done after the busy-indicator is off.

922 **BDM ·J A** "Buffer to Drum" (2.90+Ai+Aa)

c(4200), ···, c(4200+EL−E) → c(E), ···, c(EL).

E=♯JA, $0 \leqq EL-E < 50$, and $EL \equiv 49$ in modulo 50.

The c(4200) replace the c(E), ···, and the c(4200+EL−E) replace the c(EL). Thus a group of words is transferred to the drum memory (both normal and quick access bands) from the core memory.

N.B. 1. Contents of registers other than the c(E), ···, c(EL) are unchanged.

2. If $4200 \leqq E \leqq 9999$, the operation equals NOP (514).
3. A number in the Xx part is neglected in the operation.
4. If the core memory has been busy with some tape operations, the execution is done after the busy-indicator is off.

7. Conclusion

The details of the magnetic tape system of the KDC-I have been described with emphasis on design features and problems.

In spite of difficulties at the time of the design of the system, the completed magnetic tape system is satisfying the required functions and is utilized almost daily at the Kyoto University Computation Center. A large scale problem was solved by using the magnetic tape system for more than one hundred hours.

Several comments obtained from the experience of designing and the operation of the system should now be added.

(1) The time displacement error is corrected to a satisfactory degree in the input circuit of the TCU; thus it did not cause any difficulties.

(2) The variable block number is utilized in various ways, as already noted.

(3) The repertory of tape instructions is not very rich; however, it is almost enough for this type of computer.

(4) Since the MTH has an erase head and all portions of the MT are erased, high tolerance of the deviation of the relative position of the read/write head and the MT can be permitted, thus a better S/N ratio for read-out signals can be expected.

(5) In actual operating experience, parity checking has been found to be very reliable.

(6) A two-gap head in which one gap of the head is for writing and another for reading should be used for better operation. However, in the present system information is written in the forward direction of the MT, tested backward, and so on. Thus the operation of the system sometimes very much resembles a life test of the MT and the MTH.

(7) The block beginning and ending codes are used as an information for stopping the MT. But it would be better to use the information, "the MT is started", and "information is no longer read out", for this purpose.

(8) The number assigned to the MTH cannot be changed by the switch in this system. But it has become clear that this is more inconvenient than was foreseen.

(9) The length of the MT between the read/write head and the tape end sensors is not constant since there is a pneumatic tape buffer between them. It would be more convenient if this length could be kept constant.

(10) The MT is stopped approx. 200 ms after the tape end is detected by the use of a time-delay relay circuit. Thus it is possible to write normally if the tape end is being detected during write operations. But it would be better if the MTH could detect these two stages of tape end in relation to a certain fixed position of the MT. This and the former items are, however, not so important since tape ends are rarely used because of a strong probability of damage during handling of the tape.

(11) A large percentage of the starting and stopping time of the MTH (7 ms) consists of the operation time of the relays in the MTH. It would be possible to achieve a much higher operation speed of the MTH.

(12) Many relays are used in the MTH, some of them at a rather high current level. The micro-relays at the pneumatic tape buffers are operated very often; moreover the life of relays of this type is not very long. Most

of the difficulties occurring during the operation of the system have been caused by malfunction of the relays. It is strongly recommended that an electronic circuit should replace them.

(13) It is true that almost all kinds of presently available MTH's are not satisfactory from the standpoint that the MT should not be damaged by the malfunction of the MTH, though this is rare. There are indeed many cases where an MTH handles MT whose contents are hard to reproduce.

(14) The shielding of the read/write head and the relay circuits had to be done well beforehand. It can be said that the adjustment of the system began with the work of suppressing noise and ended with the some work.

(15) The use of suitable static circuits would have been more economical than the use of dynamic flip-flop circuits in the TCU. The main reason for this comes from the difference between the operation time needed for the control of the MTH and the operation time of the dynamic flip-flop circuit.

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