Time Delay Devices for Low-Speed Electronic Surge Analyser

By

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In this paper, the authors introduce three kinds of time delay devices, which they have planned and developed extending over about the last ten years, to be applied to the low-speed surge analysers to analyse the surge performances on the transmission and distribution systems, which are composed of the time delay device and the low-speed electronic analog computer and can do away with the unavoidable defects of the conventional surge analysers. In addition, the authors simply illustrate the working principles of their surge analyser with examples of the single-conductor systems.

1. Introduction

In order to investigate, on a small scale in the laboratory, the abnormal transient performances of travelling waves on the transmission and distribution systems, several types of surge analysers have been developed. The most important element of the surge analyser is the time delay one, which corresponds to the transmission or distribution line. The cascade connection of a large number of the lumped inductance L-the capacitance C circuits, which simulates a no-loss line, is most conveniently and widely used. The performances of impulse waves on such delay line have been readily discussed[1)2)], and for example, it is wellknown that the L-C delay line has the following demerits:—(a) the steep and discrete wave front is not able to be formed, (b) the generation of the pulsating oscillation are not avoidable, and (c) the true propagation velocity cannot exist. However this type delay line is very frequently and widely used for the power line, because the production and make of the L-C line are easy and its cost is cheap, and its characteristics are considerably improved if the number of the L-C circuits is increased.

Next, the surge analyser, which has the high frequency cables as the delay elements, was expressed in the reference 3). Though the circuit construction of

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this type surge analyser is relatively simple, it. too, has several defects as follows:— (a) as the surge impedance of the cable is very low, the large power source capacity is required, (b) the special delay lines with the high impedance have to be adopted for the system containing the lines which have the different surge impedances, for instance, cable and overhead conductors, and (c) it is very difficult for the cable to give the appropriate rate of the surge attenuation and distortion corresponding to any line length.

In recent years, the surge analyser[4] with the herical winding type delay lines has been developed. As we can relatively easily make such delay lines of the different surge impedance, the demerits (a) and (b) of the cable type delay line have been done away with, but there still remains the defect (c).

To remove the several defects which cohere to the above described surge analysers, the authors have invented the new type surge analyser with the special electronic delay device[5][6][7][8][9].

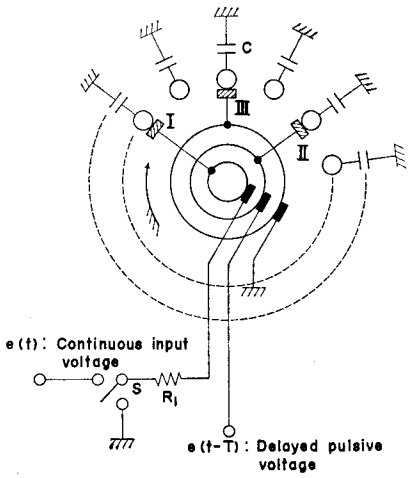
In this case, by setting up the electronic analog computer circuits due to the theoretical expressions, which should analyse the attenuation and distrotion of the travelling waves, the refraction and reflection of them at the transition points on the lines, and by using the combination of these computer circuits and the delay devices, i.e. the surge analyser circuits, we can indirectly and theoretically compute the surge performances.

In the following sections, first we shall describe the three delay devices, which we have invented, and next the computation principle of the low speed surge analyser with the delay devices.

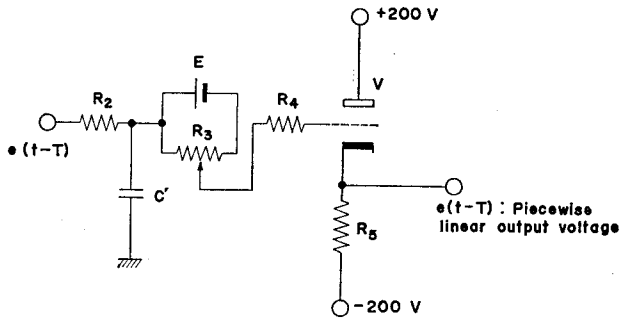
2. A-type Delay Device

The 1 channel of the A-type delay device, which the authors developed, consists of many condensers circularly arranged on a good insulating plate, namely acreyl resin plate and the rotating input and output brushes and the other elements as shown in Fig. 1.

First of all, in Fig. 1(a), the input brush I comes into contact with the terminals of the storage condensers one after another, and then the condensers are successively charged due to the input voltage $e(t)$ through the I. Next via the output brush II, which comes in contact with the condenser terminals at time T after the I passes on them, the charged voltages are drawn out from condensers and sent into the next circuit elements as inputs. The leakages of the storage condensers must be very small, so that the stored charges may not discharge during delay period. The grounded third brush III is the discharging one, through which the residual charges



(a) Delay element



(b) Output amplifier

Fig. 1. Circuit diagrams of 1 channel of A-type delay device.

within the condensers are discharged into the earth before the condensers charged.

The relay switch S is inserted into the input circuits containing the brush I and grounds it before the computation begins so that the disturbing voltages may not come into the main delay circuits. The resistance R_1 is inserted so that it may limit the rush currents from input signal circuit, which are generated because the condenser impedance transiently is very low immediately after beginning to charge the condensers, and so that it may protect the computing amplifiers before the input element of the delay circuit, and so that all the surge computer circuits may not become unstable.

As the storage and holding elements are the condensers C's and C' respectively, we are not able to get the complete output, because the voltages of the condensers rapidly decrease, if the impedance of the output circuit of the delay is not high

enough. Therefore we have to insert the buffer circuit between the output brush II and the output terminal of the whole delay circuit as shown in Fig. 1(b). In our delay circuit we use the simple cathode follower amplifier as the buffer, whose grid is connected to the brush II. As the II keeps the floating posture between the contactors of the two storage condensers, the voltages at the II are pulsive. The condenser C' is inserted to make the pulsive voltage $e(t-T)$ piecewise linear. We insert the resistor R_2 so that it may guard the circuits from the shock due to the transfer of power from C to C'. Next, the battery E and the variable resistor R_3 are fitted to adjust the zero point of the output amplifier, and the resistor R_4 is connected to prevent the grid currents of the vacuum tube. In the results of many discussions and tests, we determined to adopt the values of the condensers, resistors and the battery voltage as follows:

$$\left.\begin{aligned} C &= 0.1\ \mu\text{f}, \\ C' &= 0.001\ \mu\text{f}, \\ R_1 &= 5\ \text{k}\Omega, \\ R_2 &= 5\ \text{M}\Omega, \\ R_3 &= 500\ \text{K}\Omega, \\ R_4 &= 30\ \text{M}\Omega, \\ R_5 &= 100\ \text{K}\Omega, \\ E &= 22.5\ \text{V}. \end{aligned}\right\} \qquad (1)$$

Here we used the triode 6SL7 as V, whose grid current is very little.

Next, as we take the delay device with the low speed electronic analog computer in computations of the surge performances on the power systems, it is required that the voltage drop due to the leakage in the circuit containing the condensers should be so very small that the long delay time may be chosen. In this connection, we chose the time lag to be 2 to 20 seconds in 1 delay channel. Moreover, in order to approach the piecewise linear wave form of output voltage to in the original form, we use as many condensers as possible, namely 60 per one delay channel. Our device consists of 10 delay channels, of which each has the construction as mentioned above.

3. B-type Time Delay Device[7]

For the A-type delay device mentioned in the preceding section, we have to prepare the mechanical speed control apparatus to vary the rotating speed of each channel. Also we can change the number of the storage condensers during the delay time only by means of manually varing the angle between the input and

output brushes. In order to do away with such difficulties, we thought of availing the rotary line finders, which are used on the automatic telephone exchange equipment, as the input and output devices, though they generate considerable acoustic noise. As the rotary line finder is electromagnetically driven by the pulses, we don't need the mechanical driving devices for the brushes. Fig. 2 illustrates the scheme of the contactors and the brushes of the rotary line finder. The 25 contactors are semicircularly arranged around the brush axis on the upper and lower levels respectively. As the 2 brushes point at inverse directions to each other, the brush II begins to slide on the contactors of the lower level as soon as the brush I has completed sliding on the ones of the upper level. Therefore, if we connect conductively the I and II, both brushes slide in series on 50 contactors per one revolution in co-operation with each other.

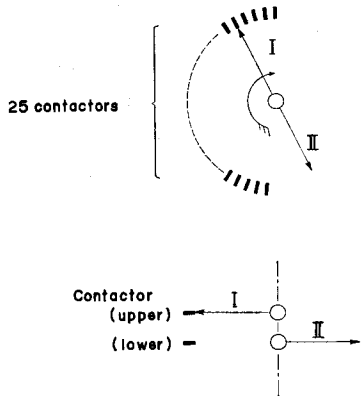


Fig. 2. Illustration of rotary line finder.

Fig. 3 illustrates the Block diagram of the

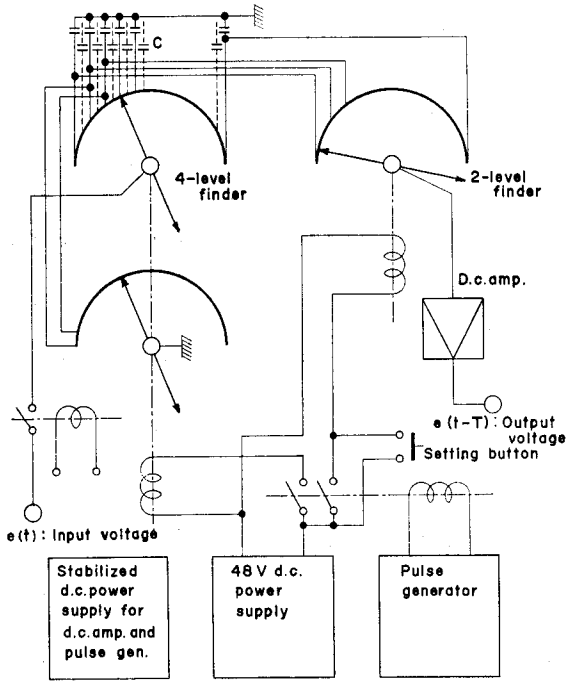


Fig. 3. Block diagram of 1 channel of B-type delay device.

1 channel of the *B*-type delay device. As shown in the figure, we use the 4-level finder for the input and 2-level one for the output. The contactors belonging to the 2-levels of the 4-level finder are connected in parallel with the contactors of the 2-level finder as in Fig. 3. The storage condensers are inserted between each contactor and the earth, and via the brushes of the 4-level finder, the input signals are applied to the delay circuit, and after any time lag, the output signals taken out through the brushes of the 2-level finder. By using the contactors belonging to the other 2-levels of the input rotary line finder, the storage condensers are shorted and the residual charges are dissipated before charging the condensers with the input signals.

The input and output rotary line finders are synchronously revolved by the common driving pulses. We can change at will the number of the storage condensers and therefore the delay time in the control range of the number of the contactors, if we change the mutual position of the input and output brushes before computing. Also we are able to vary the delay time, in the wide range, by means of altering the revolution of the brushes due to changing the period of the driving pulses. As high power pulses are required to work the rotary line finder, and to operate the finders directly by the electronic pulse generator is very uneconomical, we adopted the indirect driving method, in which the finders are operated by the other 48V d.c. source interrupted by the driving relay operated by the pulse generator as shown in Fig. 3.

We choose the capacitance of the storage condenser 0.1 μF as well as in the A-type and use the styrol condensers which have very good characteristics and whose number is 50 per one channel.

In the B-type delay device as well as in the A-type, buffer circuit with high input impedance as the output element is required. However with respect to the simple cathode follower amplifier in the A-type delay device, its voltage gain is a little less than 1, and it is necessary to compensate the cathode voltage, which is positive even when the input voltage is 0. Considering these defects of the A-type

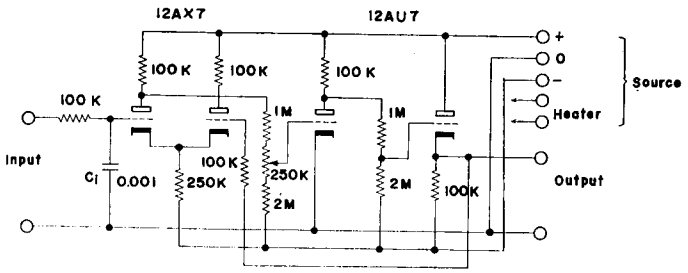


Fig. 4. Circuit diagram of d.c. amplifier for B-type delay device.

device, we make the voltage gain 1 in the B-type, by applying the negative feedback to the simple d.c. amplifier as shown in Fig. 4. Our B-type delay device is composed of 10 delay channels, of which one is presented in Fig. 3 and 4 and the whole elements are taken in one rack.

Last, the ratings of the elements used in the device are as follows:

$$\left.\begin{aligned} &C = 0.1\ \mu\text{f}, \\ &C' = 0.001\ \mu\text{f}, \\ &\text{input series resistance} = 5\ \text{k}\Omega, \\ &\text{delay time } T = 2 \text{ to } 50 \text{ sec}, \\ &\text{maximum number of samplings} = 47\ . \end{aligned}\right\} \qquad (2)$$

4. C-Type Delay Device

Though many condensers are available as the storage elements in this delay device as well as in the previously described A- and B-types, it has a special mirror type hold circuit, which consists of a condenser and a high gain d.c. amplifier. Namely the storage condensers are not only used for memory, but also they are worked as hold elements. In additon, though the C-type delay device is similar to the one developed in U.S.A., we have given the many original ideas to the circuit elements of the C-type devices.

Now Fig. 5 shows the circuit diagram of the 1 channel of the C-type delay device. Applying Kirchhoff's law to the circuit of the figure, we obtain the following equations:

$$\frac{e_i - e_s}{R} - \frac{e_s - e_A}{R} = Cp(e_s - e_0)\ , \qquad (3)$$

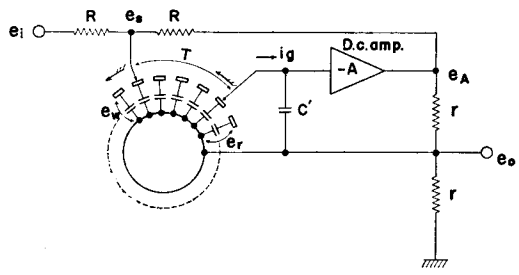


Fig. 5. Circuit diagram of 1 channel of C-type delay device.

$$\frac{e_0}{r} - \frac{e_A - e_0}{r} = Cp(e_s - e_0)\,, \tag{4}$$

$$e_w = e_s - e_0\,, \tag{5}$$

$$e_A = -A(e_r + e_0)\,, \tag{6}$$

Where e_i and e_0 are the input and output voltage respectively, e_s and e_A the voltages at the two nodes shown in the circuit diagram, e_w the voltage of the condenser, which is being charged at present, and e_r the one of the condenser after T seconds from the completion of charge, if it is assumed that the amplifier gain A is large enough, we obtain

$$e_w = \frac{E_i}{2}\{1 - \varepsilon^{-2t/C(R+r)}\}H(t)\,, \tag{7}$$

$$e_0 = -e_r\,, \tag{8}$$

where we put that $e_i = E_i H(t)$.

If it is assumed that the time which is taken to charge the condenser if much larger than the charging time constant $C(R+r)/2$, we have

$$e_w = \frac{E_i}{2}\,.$$

In other words, the terminal voltage of a condenser becomes half of the input one and then this half voltage is kept within the condenser, when the condenser is floated. After the delay time T, this voltage is picked up via the reading-out contactor, and sent into the output circuit. Therefore, putting the voltage $e_w(t)$, which is written into a chain of condensers, the reading-out voltage is expressed by $e_w(t-T)$, if the voltage drop of the condensers due to their leakage during the delay time T can be neglected.

Now putting the input voltage $e_i(t)$, the output voltage becomes approximately as follows:

$$e_0(t) = -e_w(t-T) = -\tfrac{1}{2}e_i(t-T) \tag{9}$$

Fig. 6 shows the block diagram which gives the outline of construction of the C-type delay device. One memory element is composed of one storage condenser, the one relay for writing-in and the other one for reading-out. Moreover 2 unit delay circuit is formed of the 10 memory elements and the dual 10-step counters. By connecting in series the appropriate number of unit delay circuits or moving suitably the starting positions of the writting-in and reading-out counters, we can at will select the number of the memory condensers of one delay channel. Also, by changing the period of the clock pulses, we are able to vary widely the delay time

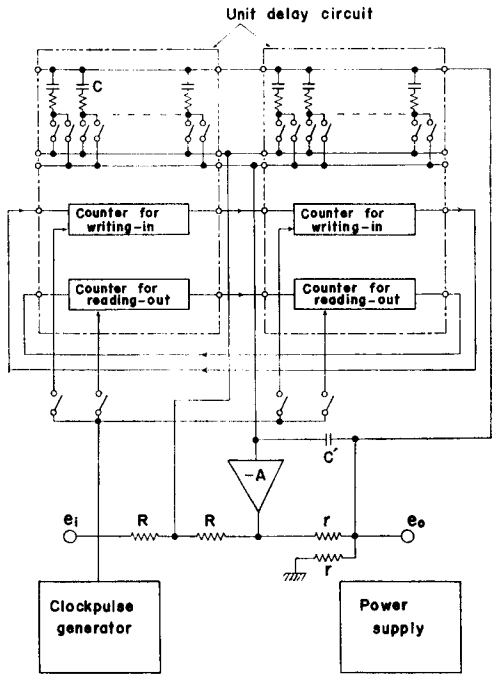


Fig. 6. Block diagram giving outline of C-type delay device construction.

to the same number of samples. Fig. 6 illustrates the state in which the 2 unit delay circuits are connected in series. In the trial production, we made the 20 units, which can be used separately as well as in series. With respect to the only 4 units of the 20 ones, the number of the condensers is able to be changed from 1 to 10. By using these 4 units, we can choose more conveniently the number of the condensers of the 1 channel of the delay device.

We use the clock pulse generator to originate the pulses which drive the writting-in and reading-out counters. In order to stabilize the period of the pulses and to obtain the stable and accurate delay time, we use the quartz oscillator.

With respect to this delay device as well as the A- and B-types, it is necessary to prevent discharges in the storage condensers by maintaining highly the insulating resistance of the writting-in and reading-out relays to the earth. So in the C-type delay device, we use the new type read-relays enclosed in small glass tube.

The ratings of the C-type delay device are chosen as follows:

$$\left.\begin{aligned} &C=0.1\ \mu\text{F}, \quad C'=0.001\ \mu\text{F} \\ &\text{numbers of d.c. amplifiers}=10, \\ &\text{maximum input voltage}=\pm 100\text{V}, \\ &\text{maximum output voltage}=\pm 50\text{V}, \\ &\text{delay time } T=0.05 \text{ to } 19 \text{ sec (When used as 100 channels)}, \\ &\qquad\qquad =0.05 \text{ to } 199 \text{ sec (When used as 1 channel)}. \end{aligned}\right\} \tag{10}$$

Fig. 7(a′) and (b′) show the piecewise linear output voltage waveforms, when the sine wave and the triangular wave voltage, which are plotted in (a) and (b) in the figure respectively, are applied to the C-type delay device, where $T=7$ sec. Though these are only two examples, you will see that the C-type device has very good characteristics.

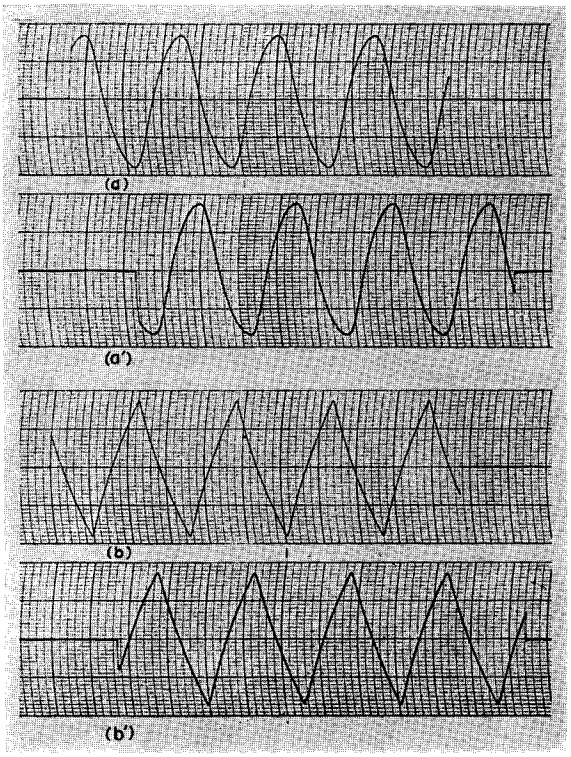


Fig. 7. Two examples of the piecewise linear output voltages compared with the continuous input voltage, which were obtained in use of the C-type delay device.
(a) e_i, (a') e_0, (b) e_i, (b') e_0

5. Computation Principle of Surge Analyser

Fig. 8 shows the simple principle diagram as surge analyser circuit for a single-conductor system. In the figure, E_i and E_0 are the input and output voltage respectively, and the relation between E_i and E_0, as the characteristics of the delay circuit $D(T)$ is given by $\exp(-pT)$, is given by

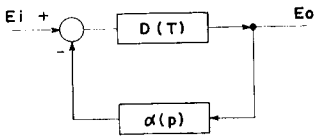


Fig. 8. Simple example of principle diagram as surge analyser circuit for a single-conductor system.

$$E_0 = \frac{e^{-pT}}{1+\alpha(p)\varepsilon^{-pT}} E_i$$

$$= \sum_{n=0}^{\infty} (-1)^n \{\alpha(p)\}^n \varepsilon^{-npT} E_i \varepsilon^{-pT}. \tag{11}$$

In these equations, the cases, that $\alpha(p)=1$ and $\alpha(p)=-1$, correspond to the conditions grounding and floating the final end of the line respectively.

Next Fig. 9 shows an example of the principle diagram of the surge analyser construction for a single-conductor system. In the figure

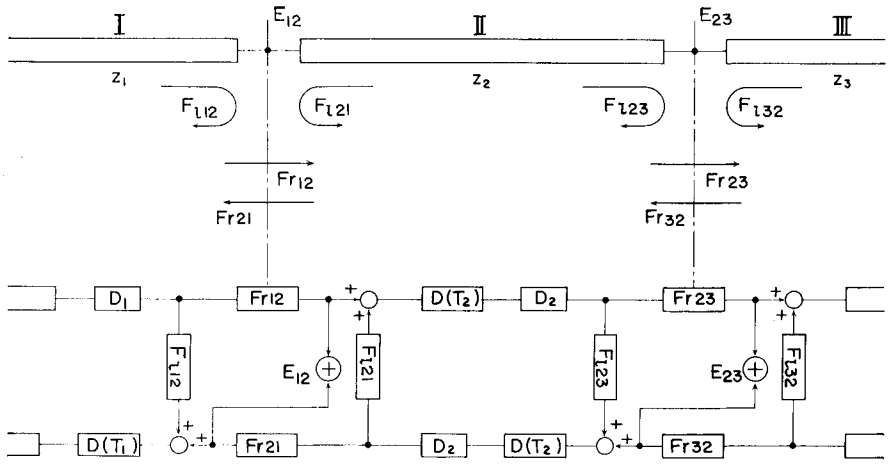


Fig. 9. An example of principle diagram of the surge analyser construction for a single-conductor system.

Z_i: surge impedance of the i-th system,

D_i: attenuation or distortion factor,

$F_{r_{ij}}$: refraction coefficient corresponding to the case where the waves travel from the i-th system into the j-th.

$F_{l_{ij}}$: reflection coefficient corresponding to the same case,

i, j=I, II, III, ……

When we treat a single-conductor system with our surge analyser, we need separate delay channels for going and returning of the travelling waves. However, when we shall analyse the surge performances along the no loss lines, we can omit 1 delay channel by being twice the delay time of remaining one. In this case, as we have no need of the computing elements for attenuation and distortion, we can simply compose the computating circuits with the delay circuits $D(T)$'s, adders and potentiometers. By using our surge analyser, as above mentioned, we can very conveniently and automatically do the analyses of the transient performances of the

surges not only on the single-conductor systems but also the more complex multi-conductor systems[11].

6. Conclusions

In the preceeding sections, the authors have described the good characteristics of the three types, namely A-, B- and C-type time delay devices used for the electronic surge analyser, which they developed over a long period of years, and also they have introduced some applications of the devices to the analyses of the surge performances on the single-conductor system. In this connection, as previously mentioned, using our surge analyser, we are able to treat the more practical transmission or distribution systems, that is to say, the multiconductor systems.

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