Review

High-voltage SiC power devices for improved energy efficiency

By Tsunenobu KIMOTO[*1,†]

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Abstract: Silicon carbide (SiC) power devices significantly outperform the well-established silicon (Si) devices in terms of high breakdown voltage, low power loss, and fast switching. This review briefly introduces the major features of SiC power devices and then presents research works on breakdown phenomena in SiC pn junctions and related discussion which takes into account the energy band structure. Next, recent progress in SiC metal-oxide-semiconductor field effect transistors, which are the most important unipolar devices, is described with an emphasis on the improvement of channel mobility at the SiO_2/SiC interface. The development of SiC bipolar devices such as pin diodes and insulated gate bipolar transistors, which are promising for ultrahigh-voltage (>10 kV) applications, are introduced and the effect of carrier lifetime enhancement is demonstrated. The current status of mass production and how SiC power devices can contribute to energy saving are also described.

Keywords: silicon carbide (SiC), power device, field-effect transistor, avalanche breakdown, channel mobility, carrier lifetime

1. Introduction

In the modern world, it is essential to seek more energy-efficient technologies, which can reduce greenhouse gas emission and fossil fuel consumption. Among various kinds of energies, the fraction or the role of electrical energy is steadily increasing and reduction of the electric power dissipation is a crucial challenge in all the electric and electronic systems. In electric power flow, about 2–15% of the total power is wasted as heat at every power conversion stage such as DC(direct current)–AC(alternate current) and AC–DC conversion.[1)] For example, the electric power generated by solar cells is DC and this power must be converted to AC for connection to standard power lines. A battery output is also DC and this output is often modulated (*e.g.*, pulse-width modulated) and supplied to drive three-phase AC induction motors. The power conversion between AC and DC is usually done by using electronic circuits, called power converters or inverters, that consist of power semiconductor devices, such as switching transistors and diodes. This field of electric power control is known as "power electronics" and has received increasing attention in recent years.[2)]

Since the conversion efficiency of converters and inverters is mainly determined by the performance of the power semiconductor devices, the progress of power electronics depends mainly on advances in the power devices. Silicon (Si, bandgap: 1.1 eV) has been almost exclusively the most popular semiconductor material used for fabrication of power devices. Owing to the availability of high-quality and large-diameter Si wafers combined with advanced device processing and simulation technologies, Si-based power devices have been strongly adopted in this field because of their high performance, high reliability, and low cost.[1),3)] However, Si power devices are now so mature that their performance is approaching the limit determined by the material properties.

To overcome the limitation of Si power devices, wide bandgap semiconductors, which can withstand higher electric fields, have attracted much attention in the last two decades. Among various wide bandgap semiconductors, silicon carbide (SiC),[4)–10)] gallium nitride (GaN),[11),12)] and more recently gallium oxide (Ga_2O_3)[13),14)] are promising candidates which could significantly outperform the Si counterparts. The

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features of SiC (bandgap: 3.3 eV) include the availability of high-quality and high-purity SiC epitaxial layers[15] on single crystalline SiC wafers with a large diameter of 150 mm grown by a seeded sublimation method.[16),17] SiC is an exceptional wide bandgap semiconductor, the doping (both n- and p-type) density of which can be controlled over a wide range (10^{14}–10^{20} cm^{-3}) by either impurity doping during epitaxial growth[15),18] or ion implantation.[19),20] In addition, SiC has an indirect-transition band structure, and thereby a long carrier lifetime is expected, which is beneficial for development of bipolar-type power devices such as insulated gate bipolar transistors (IGBTs) and pin diodes.

Regarding crystal structure, SiC can crystallize in many (more than 100) different forms called "polytypes", where the stacking sequence of Si-C pairs along one direction varies for different polytypes.[21] For electronic applications, we must identify the most suitable SiC polytype and must grow high-quality and large single crystals without inclusions of foreign polytypes. The early development of SiC was devoted to polytype control in SiC bulk and epitaxial growth.[22] In the early 1990s, 3C-SiC (cubic phase) and 6H-SiC (hexagonal phase) were exclusively investigated, and the first 1 kV SiC Schottky barrier diode (SBD) was fabricated with 6H-SiC.[23] In 1994, it was discovered that the 4H-SiC polytype (another hexagonal phase) is much superior to 3C-SiC and 6H-SiC, having a much higher electron mobility and wider bandgap.[24)–26] After this discovery, 4H-SiC has been exclusively investigated and produced for power device applications.[8] In this paper, 4H-SiC is denoted as SiC for simplicity.

Based on extensive studies on growth, material characterization, and device processing technology especially in Japan, United States, and Europe, production of SiC SBDs and metal-oxide-semiconductor field effect transistors (MOSFETs) has started. However, the performance of SiC power MOSFETs is still far from the full potential of the material. In addition, many of the important intrinsic properties and the nature of defects are unknown. The physical understanding of carrier transport, carrier recombination, and breakdown phenomena in SiC is also poor. The unique hexagonal crystal structure, wide bandgap, and complicated band structure of this material make it very difficult to characterize the physical properties and appropriately interpret the acquired data. Preparing appropriate sample structures or device structures for characterization is also hard due to the high mechanical hardness and chemical inertness of the material.

In this paper, recent progress in SiC power devices and material issues mainly obtained by the author's group is reviewed. In section 2, the major features of SiC power devices are briefly introduced. In section 3, the breakdown phenomena, which are crucial for designing and fabricating SiC devices, are described. In section 4, the prospects and performance-limiting factors of SiC power MOSFETs are explained, and a recent innovation in SiC MOS technology is presented. In section 5, development of SiC bipolar devices, which are attractive for ultra-high-voltage applications, are described. Section 6 briefly shows impacts of SiC power devices in real systems. Finally, a summary is given in section 7.

2. SiC power devices

Typical structures of SiC power devices are schematically shown in Fig. 1. Figures 1(a) and (b) show, respectively, a Schottky diode and a p$^+$n diode (often called "pin diode"), where a metal anode or a p$^+$-anode is formed on a relatively thick n-layer (voltage-blocking region), which is connected to the bottom low-resistivity n$^+$-substrate with its ohmic contact. These diodes must allow the current to flow smoothly with a low on-resistance when a positive voltage is applied to the anode (forward bias

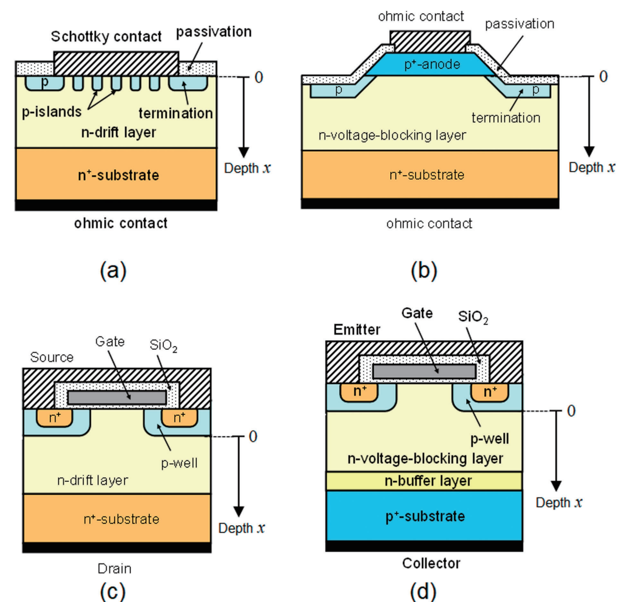

Fig. 1. Schematic structures of typical SiC power devices. (a) Junction-Barrier Schottky diode (modified structure of Schottky barrier diode), (b) p$^+$n diode (pin diode), (c) planar-type vertical MOSFET, and (d) insulated gate bipolar transistor (IGBT).

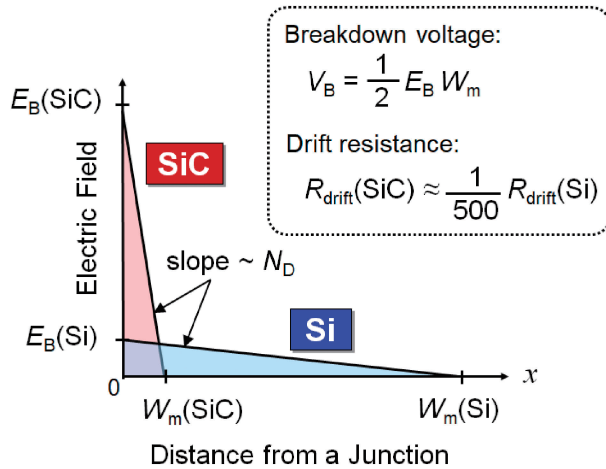

Fig. 2. Schematic distributions of electric field strength at breakdown under reverse bias in Schottky barrier diodes or p^+n diodes of Si and SiC with the same breakdown voltage. Here E_B, V_B, and W_m denote the critical (breakdown) electric field strength, breakdown voltage, and thickness of the n-layer (voltage-blocking region). The area of the right-angle triangle in this figure corresponds to the breakdown voltage.

condition), whereas they must fully block the current when a negative voltage is applied to the anode (reverse bias condition). To fully block the current in Si-based diodes when a high negative voltage is applied, a relatively thick n-layer is needed to lower the electric field inside the diode below its critical value so that the breakdown phenomena (or the onset of the current) are prevented. The electric field inside a Si diode at breakdown under the reverse bias is shown by a blue triangle in Fig. 2 as a function of distance from the junction, *i.e.*, the interface between the anode and the n-layer. The situation is quite different for a SiC diode, since SiC sustains a much higher electric field (the breakdown field or critical electric field), about a factor of ten greater than that of Si. As a result, the n-layer in the SiC diode can be about ten times as thin as that of a Si diode to achieve the same breakdown voltage, as shown by a red triangle in Fig. 2. Here the area of the right-angle triangle in Fig. 2 corresponds to the breakdown voltage. Furthermore, the doping density of the n-layer, which is proportional to the slope of the plot in Fig. 2, can be increased by a factor of 100 with SiC. Because of the thinner and more heavily-doped n-layer, the resistance of the n-layer for SiC devices is about 400–800 times lower than for Si devices at a given breakdown voltage. This is the prime reason why SiC devices exhibit much lower on-state resistance (on-resistance) and thereby achieve significant reduction of Joule heating during device operation.

Figures 1(c) and (d) show basic structures of two major power transistors, namely a vertical MOSFET and an IGBT, respectively. In the vertical MOSFET, the n^+-region and p-region are locally formed near the surface of the n-layer grown on the bottom n^+-substrate, as shown in Fig. 1(c). Furthermore, a thin oxide, the gate (usually low-resistivity polycrystalline Si) and source contacts are formed on the top. A positive voltage is applied to the drain contact connected to the bottom n^+-substrate while the source contact is grounded. When a sufficiently large positive voltage (typically 10–20 V) is applied to the gate, a thin conduction channel (inversion channel) consisting of electrons is formed at the surface of the top p-region beneath the gate/oxide stack. Under this bias condition, a high current flows from the drain to the source through the n^+-substrate, n-layer, the conduction channel, and the top n^+-region, which is the "on-state" of this switching device. Since only electrons in a series of n-type semiconductor regions are involved in the current flow, a MOSFET is known as a "unipolar device" (an SBD is also a unipolar device). When the gate is grounded, the conduction channel is not formed and the junction consisting of the p-region/n-layer is reverse-biased because a positive voltage is applied to the drain. The reverse-biased pn junction blocks the current as in the case of a pn diode, which is the "off-state" of the device. In other words, the on/off switching of the MOSFET can be controlled by adjusting the gate voltage.

The IGBT structure is similar to that MOSFET except that the bottom substrate is p^+-type in an IGBT, instead of n^+-type in a MOSFET. In an IGBT, the three terminals are called the emitter, the gate, and the collector, as shown in Fig. 1(d). A positive voltage is applied to the collector while the emitter is grounded. As in the case of a MOSFET, a conduction channel is formed at the surface of the top p-region beneath the gate/oxide stack when a positive voltage is applied to the gate, which initiates electron conduction or current flow. One striking feature of an IGBT is that the pn junction consisting of the bottom p^+-substrate and the n-layer is forward-biased under this condition, and holes are injected from the p^+-substrate to the n-layer, leading to reduction of the n-layer resistance in the on-state of the IGBT. Since both electrons and holes contribute to the current in an IGBT, an IGBT is a "bipolar device" (a pn diode is also a bipolar device). The off-

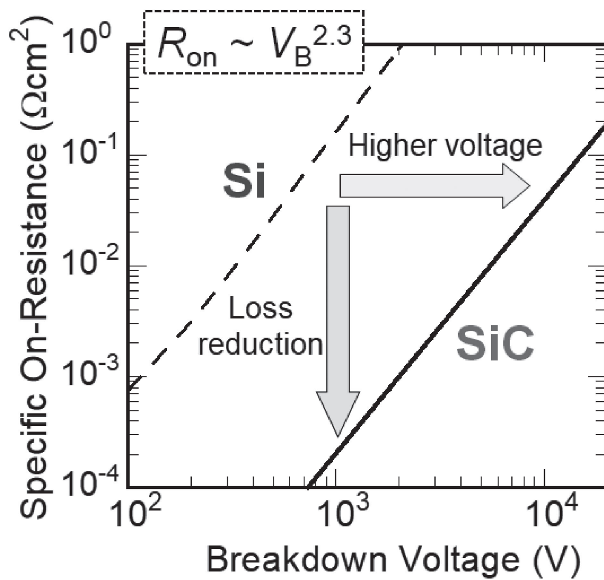

Fig. 3. Trade-off relationship between the specific on-resistance (R_{on}) and the breakdown voltage (V_B) for Si and SiC unipolar power devices, which were calculated using several physical properties such as the impact ionization coefficients and electron mobility.

state of an IGBT is quite similar to that of a MOSFET, and the reverse-biased junction consisting of the p-region/n-layer near the surface blocks the current when a positive voltage is applied to the collector under the zero-gate bias.

In all these power transistors and diodes, both the resistance in the on-state and the breakdown voltage in the off-state are mainly determined by the thickness and donor density of the thick n-layer (voltage-blocking layer, also called "drift layer" in unipolar devices), as long as the channel resistance is low enough. Figure 3 depicts the relationship between the on-resistance (R_{on}) for a unit area (cm^2) and the breakdown voltage (V_B) for Si and SiC unipolar power devices, which were calculated by using several physical parameters such as the impact ionization coefficients and electron mobility. When the material is fixed, a thicker and more lightly-doped voltage-blocking region is required to increase the breakdown voltage (to increase the triangle area in Fig. 2). Both factors (thickness increase and doping decrease) naturally increase the resistance of the voltage-blocking region when achieving a higher breakdown voltage. Thus, the trade-off relationship shown in Fig. 3 is often called the material limit (unipolar limit) for each material. In the figure, the updated "SiC limit",[27] which takes account of the optimal punch-through structures and higher electron mobility along the $\langle 0001 \rangle$ direction, is plotted as the solid line. This SiC limit is expressed by the following equation (unit of V_B: V):

$$R_{on} = 2.95 \times 10^{-11} \, V_B{}^{2.28} \, \Omega\text{cm}^2. \quad [1]$$

Since the on-resistance of Si unipolar devices becomes unacceptably high when the breakdown voltage is increased to about 1 kV or higher, Si bipolar devices, which utilize injection of minority carriers to reduce the on-resistance, are employed for such high-voltage applications.[28] The major drawbacks of high-voltage Si bipolar devices include a slow switching speed and large switching loss, because the injected carriers in the on-state must be removed to reach the off-state. By using SiC, unipolar devices can be adopted even for high-voltage (at least, 1–6 kV) applications, owing to the extremely low on-resistance mentioned above. This enables fast and low-loss switching characteristics, thanks to the absence of minority-carrier injection. This is another advantage of SiC unipolar power devices. The intrinsic carrier density of SiC is more than ten-orders-of-magnitude lower than that of Si due to its wide bandgap. This fact indicates that the leakage current of SiC devices can be extremely low even at high temperature, because the leakage current density of a pn junction is proportional to the intrinsic carrier density. Since self-heating is a crucial issue in terms of device reliability, the high-temperature operation capability of SiC devices positively influences the reliability of SiC power devices.

It is expected that 600–6500 V SiC power MOSFETs and SBDs will replace mainly Si IGBTs and Si pin diodes with the same blocking voltage.[9),10] SiC IGBTs and pin diodes are attractive in the very high-voltage (>6.5 kV) blocking range, as explained in subsection 5.1. The current status of individual SiC power devices is described in sections 4–6.

3. Breakdown phenomena in SiC devices

3.1. Avalanche breakdown. In general, power devices must sustain substantially high voltage in their off-state. The current is usually kept negligibly small in reverse-biased diodes and off-state transistors, but it increases to a sizable level if the applied voltage exceeds the so-called breakdown voltage. In case of lightly-doped semiconductors, this breakdown process is caused by the avalanche phenomenon of carriers, whereas in heavily-doped materials it results from the Zener tunneling process. To clarify these breakdown processes in SiC, systematic studies were made on various pn diodes, as described below. Note

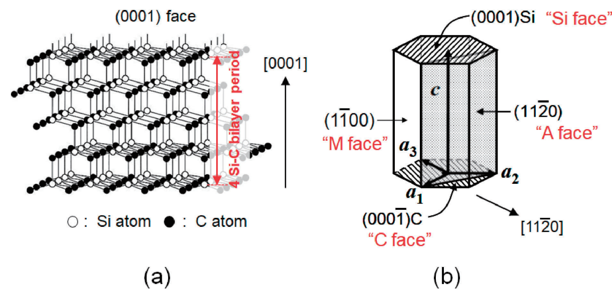

Fig. 4. (a) Schematic illustration of the 4H-SiC structure in a ball-stick model. (b) Several major faces and orientations in the hexagonal cell of SiC. In this figure, (0001) is the basal plane and this is the face of all the commercial SiC wafers.

that the complicated and anisotropic aspects of the band structure of SiC as well as dislocations are likely to affect the breakdown processes.

Since SiC is not an isotropic material, the crystal faces and orientations are of importance in academic studies as well as device development. Figure 4 shows (a) an illustration of the crystal structure of SiC (4H-SiC) in a ball-stick model and (b) several major faces and orientations in the hexagonal cell of SiC. In this figure, (0001) is the basal plane and is the face of all the commercial SiC wafers at present, because the growth of high-quality SiC ingots with a large diameter is easy on the {0001} face.[22] Thus, both the current flow in the on-state and the electric field direction in the off-state in SiC power devices are mainly along the *c*-axis (⟨0001⟩), as the substrate surface shown in Fig. 1 is (0001), although the channel conduction of electrons in power transistors shown in Figs. 1(c) and 1(d) is normal to the *c*-axis.

Avalanche breakdown, which is dominant in lightly-doped junctions, is determined by the impact ionization coefficients of electrons and holes. The impact ionization coefficient is defined as the number of electron-hole pairs generated by impact ionization under a certain electric field. In spite of a few studies on the impact ionization coefficients in SiC,[29),30)] the accurate values for wide ranges of electric field and temperature are still unavailable. The author's group designed and fabricated many different pn diodes with either punch-through or non-punch-through structures to extract the impact ionization coefficients.[31)–33)] Here pn diodes and np diodes (inverted structures) were prepared to separately determine the electron- and hole-initiated carrier multiplication. The diodes were fabricated on SiC(0001) or $(11\bar{2}0)$ substrates in order to determine the ionization coefficients parallel or perpendicular to the *c*-axis, respectively. Since SiC$(11\bar{2}0)$ substrates are not commercially available, we prepared custom substrates from SiC ingot crystals and grew homoepitaxial layers on the substrates.[34)] In reverse-biased diodes, electric field crowding usually takes place along the junction edge (periphery), which results in the decrease of the breakdown voltage. Since this phenomenon disturbs the impact ionization process, it was minimized by forming mesa structures with an edge termination structure, as shown in Fig. 1(b). Current–voltage characteristics of the fabricated diodes were measured under the reverse-bias condition with above-bandgap light (wavelength: 250–280 nm) illumination. By dividing the photocurrent at high reverse voltages by the base current (unmultiplicated current) in a low-voltage region, the multiplication factors of carriers were determined as a function of the reverse voltage (or the electric field). The impact ionization coefficients were extracted by analyzing the electric field dependence of the multiplication factors.[31)]

Figure 5(a) plots the impact ionization coefficients for electrons (α_n) and holes (α_p) along ⟨0001⟩ and $\langle 11\bar{2}0\rangle$ as a function of the inverse of the electric field strength at 293 K. In the initial study, we selected dislocation-free diodes (diode area: $3\text{–}7 \times 10^{-4}\,\text{cm}^2$) for the measurements to exclude the impacts of dislocations, where the dislocation density of the base materials was about $3\text{–}5 \times 10^3\,\text{cm}^{-2}$. However, it turned out that the obtained results were insensitive to the presence of 1–4 dislocations inside the measured diodes. This fact can be ascribed to the extremely low intrinsic carrier density of SiC, which gives very low generation current via a dislocation in the pn junction.[10)] As shown in Fig. 5, the impact ionization coefficients in SiC reach $100\,\text{cm}^{-1}$ for the field in the MV/cm range, whereas those in Si take similar values in the 100–200 kV/cm range (not shown), indicating that an electric field about ten times higher is required to initiate impact ionization in SiC.

One striking feature in Fig. 5 is the large anisotropy in the electron impact ionization coefficient (α_n): The electron impact ionization coefficient along ⟨0001⟩ is lower than that along $\langle 11\bar{2}0\rangle$ for a given electric field by more than two orders of magnitude. Along $\langle 11\bar{2}0\rangle$, the impact ionization coefficient of electrons is close to that of holes at 293 K, and both the coefficients decrease at elevated temperatures (at least up to 440 K), which is naturally ascribed to the enhanced phonon scattering at high temperature. A similar temperature dependence was observed for the impact ionization

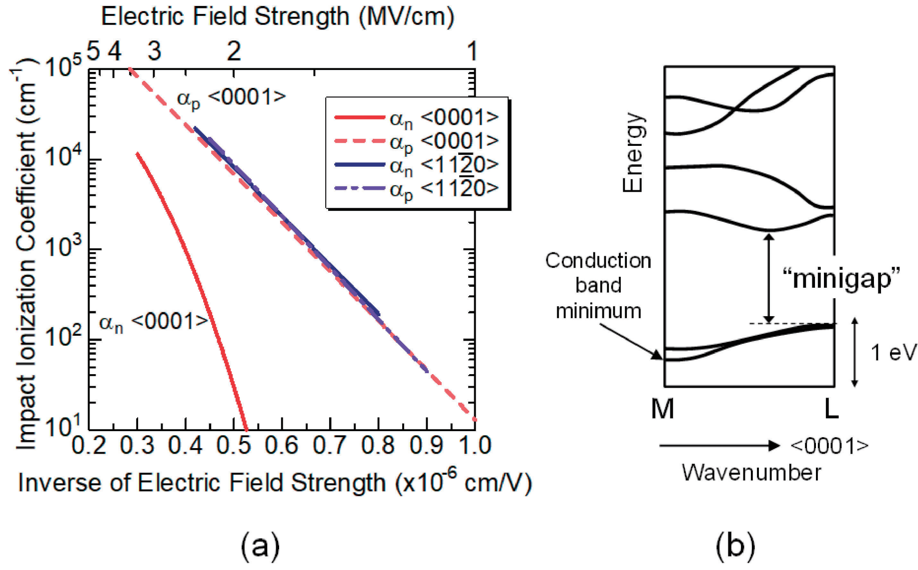

Fig. 5. (a) Impact ionization coefficients for electrons (α_n) and holes (α_p) along ⟨0001⟩ and ⟨11$\bar{2}$0⟩ in SiC at 293 K as a function of the inverse of electric field strength experimentally determined. (b) Electron energy–wavenumber dispersion curves along ⟨0001⟩ in the k-space near the bottom of the conduction band of SiC.

coefficient of holes along ⟨0001⟩ in the temperature range up to 670 K. In contrast, the coefficient of electrons along ⟨0001⟩ is unusually low and is almost independent of the temperature in the range from 156 to 460 K, and it exhibits a slight increase with elevating temperature above 500 K.[32] Thus, impact ionization caused by high-energy electrons traveling along ⟨0001⟩ is unusual.

The ratio of effective mass of electrons perpendicular to ⟨0001⟩ ($m^*_\perp = 0.40m_0$, m_0: electron rest mass) and that parallel to ⟨0001⟩ ($m^*_{//} = 0.33m_0$) near the band bottom of SiC is known to be 1.21.[8] This effective mass anisotropy is an important origin of the mobility anisotropy of electrons at low-fields in lightly-doped SiC, which are 1,020 and 1,210 cm^2/Vs for the direction perpendicular and parallel to the ⟨0001⟩ axis, respectively.[35),36] However, the large anisotropy in the electron impact ionization coefficients cannot be explained simply by this relatively small anisotropy in the effective mass near the conduction band bottom and it may originate from the unique structure of the conduction band of SiC.[37] Because of the peculiar ⟨0001⟩ stacking structure of SiC with a four Si-C bilayer period (Fig. 4(a)), there exist a few minigaps along ⟨0001⟩ in the k(wavevector)-space inside the conduction band, as shown in Fig. 5(b). These minigaps should hinder the energy gain of electrons under a high electric field, leading to the very low impact ionization coefficient of electrons along ⟨0001⟩. It is noted that such minigaps do not exist perpendicular to ⟨0001⟩ and electrons can be smoothly accelerated under high electric field. Another possible cause for the unusual coefficient of electrons along ⟨0001⟩ is the substantial increase in the electron effective mass along ⟨0001⟩ with increasing electron energy in the lowest subbands of the conduction band, as also indicated in Fig. 5(b). This effective mass increase lowers the acceleration process of electrons and must contribute to the unusually small ionization coefficient of electrons along ⟨0001⟩. To cause impact ionization, however, the energy of an accelerated electron must be higher than the bandgap, which means that only the electrons located 3.3 eV (or higher) above the conduction band bottom contribute to the impact ionization in SiC. Hence, the relatively large minigaps (maximum: 1.3 eV) may be a major obstacle for creating very hot electrons. A full band Monte Carlo simulation using a simplified band structure suggests that the presence of a minigap inside the band decreases the impact ionization coefficient by several orders of magnitude.[38] At elevated temperature, these minigaps shrink, which results in a higher probability for an electron to be excited to a higher energy band. These factors may be the reasons for the extremely low impact ionization coefficient of electrons along SiC ⟨0001⟩ and its positive temperature dependence at high temperature (>500 K).

Figure 6 depicts the breakdown voltage and critical electric field strength versus the doping

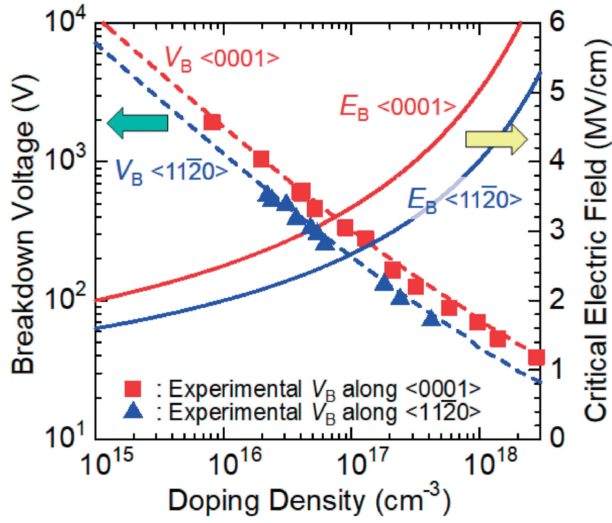

Fig. 6. Breakdown voltage and critical electric field strength plotted against the doping density of the voltage-blocking region for SiC(0001) and ($11\bar{2}0$) pn junctions at 293 K. The theoretical breakdown voltage and critical electric field strength were calculated by using the impact ionization coefficients shown in Fig. 5. In the figure, the breakdown voltages experimentally obtained for SiC(0001) and ($11\bar{2}0$) pn diodes are also plotted by red squares and blue triangles, respectively, which show very good agreement with the theoretical values.

density of the voltage-blocking region for SiC(0001) and ($11\bar{2}0$) pn junctions. The theoretical breakdown voltage and critical electric field strength were calculated by using the experimental impact ionization coefficients shown in Fig. 5. The carrier multiplication factor M caused by an avalanche phenomenon, which is directly linked to the increase of leakage current, is given by the following equation.[28]

$$M = \frac{1}{1 - \int_0^{W_m} \alpha_p \exp\left\{-\int_0^{x} (\alpha_p - \alpha_n)\mathrm{d}x'\right\}\mathrm{d}x}. \quad [2]$$

Here the origin of the coordinate is set to the junction interface and W_m is the edge of a space-charge region as shown in Fig. 2. When the donor density of the n-layer is fixed, the electric field profile can be calculated as a function of the reverse-bias voltage by solving the Poisson equation.[28] At a sufficiently low voltage, the M value is unity because no impact ionization occurs due to the low electric field. As the reverse-bias voltage is gradually increased, the electric field strength and the space-charge region width increase. The impact ionization coefficients exhibit a rapid increase with increasing electric field (Fig. 5) and, as a result, the carrier multiplication factor M becomes significantly higher than unity. The junction breakdown is defined when the M value approaches infinity (in reality about 10,000) or the integral part in Eq. [2] approaches unity.[28] "The critical electric field strength" is defined as the maximum electric field at the breakdown. The reverse-bias voltage at which the M value approaches infinity is defined as "the theoretical breakdown voltage". This kind of calculation was repeated for different donor densities, by which the calculated data in Fig. 6 were acquired. In the figure, the breakdown voltages experimentally obtained for SiC(0001) and ($11\bar{2}0$) pn diodes are also plotted by red squares and blue triangles, respectively, which show very good agreement with the theoretical values, calculated by using the data of Fig. 5. Owing to the low impact ionization coefficient of electrons along ⟨0001⟩, the critical electric field strength along this direction is about 25% higher than that perpendicular to ⟨0001⟩. As a result, SiC(0001) pn junctions exhibit approximately 56% higher breakdown voltage than SiC($11\bar{2}0$) junctions with the same structure. Here the orientation dependences of the critical electric field and breakdown voltage are not as large as that of the ionization coefficients shown in Fig. 5. Although the α_n values are very low along ⟨0001⟩, the α_p values are much larger and the electric field dependence of α_p along ⟨0001⟩ is similar to that along ⟨$11\bar{2}0$⟩. In a semiconductor junction, the avalanche breakdown is mainly determined by a significant process of either hole-initiated or electron-initiated carrier multiplication. In SiC, the hole-initiated carrier multiplication is dominant along ⟨0001⟩ and does not greatly depend on the crystal orientation. On the other hand, the electron-initiated multiplication makes a minor contribution to avalanche breakdown along ⟨0001⟩. This is the reason why the orientation dependences of the breakdown voltage and critical electric field are relatively small.

From a technological point of view, the anisotropies in the low-field electron mobility and critical electric field of SiC give a positive influence on the performance of SiC(0001) power devices. As described in this subsection, the on-resistance of SiC(0001) power devices is mainly determined by the low-field mobility along ⟨0001⟩, which is about 20% higher than that perpendicular to ⟨0001⟩. On the other hand, the breakdown voltage of SiC (0001) devices is mainly governed by the critical electric field along ⟨0001⟩, which is about 25% higher than that perpendicular to ⟨0001⟩. Thus, SiC(0001) devices exhibit a lower on-resistance in the on-state and a

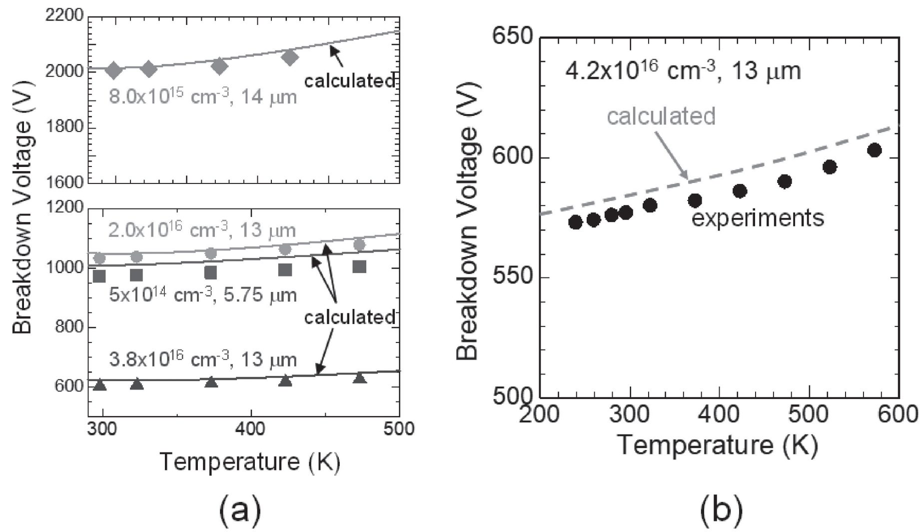

Fig. 7. Temperature dependences of the breakdown voltages for SiC(0001) pn diodes with various doping densities and thicknesses (indicated in the figure) in the temperature ranges of (a) 300–470 K, (b) 240–573 K. The experimental and calculated breakdown voltages are denoted by symbols and lines, respectively. (Reprinted from T. Kimoto *et al.*, J. Phys. D: Appl. Phys., vol. 51, 363001 (2018), with the permission of IOP Publishing.)

higher breakdown voltage in the off-state, compared with SiC devices fabricated on other crystal faces.

Figure 7 shows the temperature dependence of the breakdown voltage for SiC(0001) pn diodes with various doping densities and thicknesses, where the experimental values are plotted by symbols. The breakdown voltages calculated by using the impact ionization coefficients are shown by solid or dashed lines, indicating that the temperature dependence of the breakdown voltage can be predicted with high accuracy (error $<2\%$).

3.2. Zener breakdown. It is known that the dominant breakdown mechanism in heavily-doped pn junctions is electron tunneling through the bandgap (Zener breakdown).[28] In SiC, the bandgap is about three times larger than in Si, which suppresses the electron tunneling. However, the maximum electric field strength in SiC pn junctions can be about ten times higher, which should induce thinning of the potential barrier and enhance the tunneling. To clarify the occurrence of Zener breakdown in SiC, the author's group prepared mesa pn diodes with 12 different doping densities from 10^{16} to $10^{19}\,\mathrm{cm}^{-3}$ and investigated the leakage current in wide voltage and temperature ranges.[39] Here both the N-doped n-layer and Al-doped p-layer were epitaxially grown on a heavily N-doped n-type substrate by chemical vapor deposition at 1650 °C with a growth rate of about 8 µm/h. The acceptor density of the p-layer was fixed at $5 \times 10^{19}\,\mathrm{cm}^{-3}$, while the donor density of the n-layer was changed from 2×10^{16} to $1 \times 10^{19}\,\mathrm{cm}^{-3}$. Deep and vertical mesa structures were formed by reactive ion etching to define the junction area (2×10^{-4}–$8 \times 10^{-3}\,\mathrm{cm}^2$). The doping densities were determined by capacitance–voltage measurements and the depth profiles of N and Al atom densities were measured by secondary ion mass spectrometry (SIMS). These measurements confirmed that abrupt pn junctions were formed, which is consistent with the fact that very little dopant diffusion occurs even at 2000 °C in SiC.[8] Since abrupt pn junctions were formed, the electric field distribution near the junction as a function of the bias voltage was calculated by using the Poisson equation.

Figures 8(a) and 8(b) show the current density–reverse voltage characteristics and the current density–maximum electric field strength at the junction interface of several SiC pn diodes at room temperature, respectively. As shown in Fig. 8(a), when the doping density is in the 10^{16}–$10^{17}\,\mathrm{cm}^{-3}$ range, the leakage current density was below the detection limit until carrier multiplication by impact ionization takes place. However, a marked leakage current was observed for pn diodes with a doping density over $2 \times 10^{18}\,\mathrm{cm}^{-3}$. Since SiC has an indirect-transition band structure, the current density calculated by assuming a direct band-to-band tunneling model[40] was higher than the experimental values by several orders of magnitude (not shown). As shown in Fig. 8(c), electrons near the valence band top before

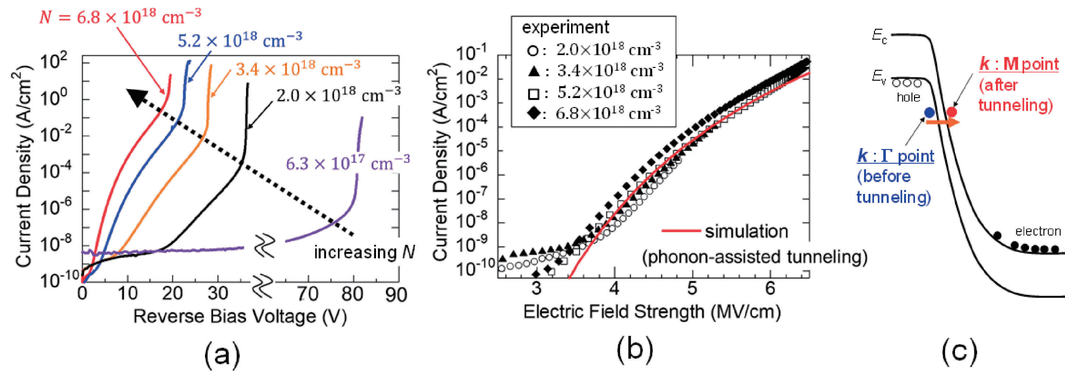

Fig. 8. (a) Current density–reverse voltage characteristics of several heavily-doped SiC pn diodes at room temperature. (b) Current density–maximum electric field strength at the junction interface. The reverse characteristics of all the heavily-doped pn diodes fall onto almost the same curve, and these characteristics can be well reproduced by the phonon-assisted tunneling model, as shown by the red curve. (c) Energy band diagram showing band-to-band tunneling.

tunneling are located at the Γ point whereas electrons should be located at the M point near the conduction band bottom after tunneling, indicating that phonons must be involved in this tunneling process. By using a phonon-assisted tunneling model[41] with appropriate phonon energies and density of states, the experimental characteristics for all the heavily-doped pn diodes could be well reproduced.[39]

When the data shown in Fig. 8(a) are replotted against the maximum electric field strength at the junction interface (Fig. 8(b)), the reverse characteristics of all the heavily-doped pn diodes fall onto almost the same curve, and these characteristics can be expressed by the phonon-assisted tunneling model mentioned above. Figure 8(b) indicates that the band-to-band tunneling current in SiC starts at about 4 MV/cm and it reaches 1 mA/cm^2 at approximately 5.7 MV/cm. Since a leakage current of 1 mA/cm^2 is a typical maximum leakage allowable in many applications, the Zener breakdown limit can be determined to be approximately 5.7 MV/cm in SiC. It is noted that the temperature dependence of the tunneling current is very small, suggesting that the phonon emission process is more important than the phonon absorption process. The temperature dependence over a wide range from 50 to 550 K can be modeled by taking account of the changes of the bandgap and the phonon distribution function (Bose–Einstein statistics).[39]

Thus, the ideal leakage current in SiC pn junctions caused by impact ionization and band-to-band tunneling can be accurately calculated by using the results described in this section. Any other components higher than the calculated values must originate from defect-associated generation currents including defect-assisted tunneling and surface leakage.

4. Progress and future challenges of SiC power MOSFETs

4.1. High-voltage, low-loss SiC power MOSFETs. SiC MOSFETs are suitable for high-voltage and low-loss power switches because of the potentially very low on-resistance, fast switching, and MOS gate structure.[8),42] Although high-performance vertical SiC power MOSFETs were demonstrated in the 1990s,[43)–46] the relatively high on-resistance of SiC power MOSFETs has been a critical issue to be resolved. Figure 9(a) shows the major resistance components inside a vertical power MOSFET, where the on-resistance is the sum of the substrate resistance, drift (n-layer) resistance, channel resistance, *etc.* In 600–1200 V class SiC MOSFETs, which are key devices in the volume market, the drift resistance (SiC limit) is so low ($<$1 mΩcm^2) that the other resistances can be the dominant components. In particular, reduction of the channel resistance has been the most important challenge in the history of SiC power MOSFET development.

In SiC power MOSFETs, SiO_2 is an almost exclusive choice as a gate dielectric material, because a sufficiently large potential barrier (desirably $>$2.5 eV) can be attained at both the conduction-band and valence-band sides.[8] However, the SiO_2/SiC interface has been extremely defective and the electron mobility in the MOS inversion channel ("channel mobility") has been as low as typically 10–40 cm^2/Vs in spite of the relatively high bulk

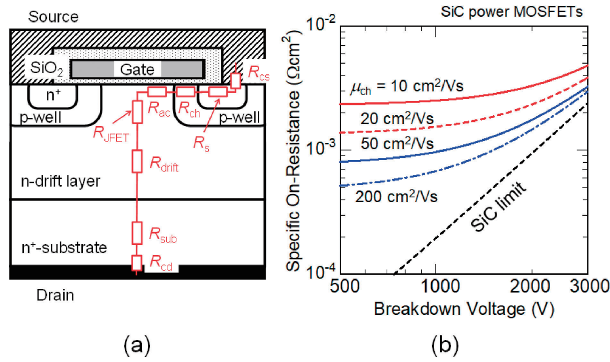

Fig. 9. (a) Major resistance components inside a vertical power MOSFET, where the on-resistance is the sum of the substrate resistance (R_{sub}), drift resistance (R_{drift}), channel resistance (R_{ch}), *etc.* (b) Specific on-resistance (on-resistance for a unit area) versus the breakdown voltage of SiC power MOSFETs, calculated by assuming several channel mobilities of 10, 20, 50, and 200 cm^2/Vs. Here the channel length and cell pitch were 0.5 µm and 8 µm, respectively. In 600–1200 V class SiC MOSFETs, the drift resistance is so low (<1 mΩcm^2) that the other resistances, especially the channel resistance, are dominant.

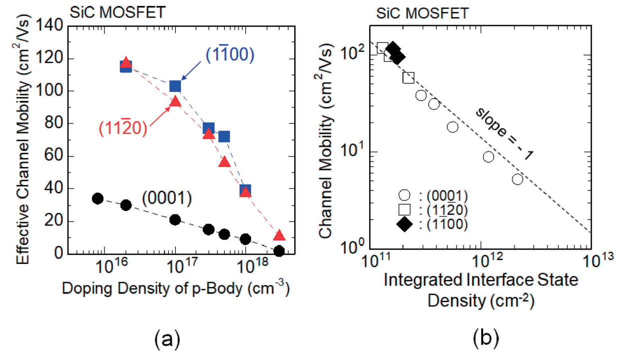

Fig. 10. (a) Channel mobility as a function of the doping density of the p-body for SiC(0001), (11$\bar{2}$0), and (1$\bar{1}$00) MOSFETs. Here the gate oxides with a thickness of about 40 nm were formed by dry oxidation at 1300 °C and subsequent interface nitridation with NO at 1250 °C. (b) Correlation between the channel mobility for n-channel SiC MOSFETs fabricated on lightly-doped p-body and the interface state density integrated from $E_c - 0.2$ eV to $E_c - 0.5$ eV (E_c: the conduction band bottom).

mobility (~1000 cm^2/Vs). Figure 9(b) shows the on-resistance for a unit area (specific on-resistance) versus the breakdown voltage of SiC power MOSFETs, for channel mobilities of 10, 20, 50, and 200 cm^2/Vs. Here the channel length and cell pitch were 0.5 µm and 8 µm, respectively. The resistance of the junction FET region was estimated by a two-dimensional device simulation. The substrate resistance was 0.18 mΩcm^2 (0.018 Ωcm × 100 µm). The gate-oxide field in the on-state was assumed to be 3.0 MV/cm. It is noted that the channel resistance is independent of the breakdown voltage, while the drift resistance exhibits a rapid increase with the breakdown voltage, as given by Eq. [1]. Therefore, the specific on-resistances of 1 kV-class SiC MOSFETs are mostly governed by the channel resistance. The channel resistance occupies about 69% and 58% of the total on-resistance for 600 V and 1,200 V devices, respectively, for the typical channel mobility of 20 cm^2/Vs. In other words, the on-resistance of 1 kV-class SiC power MOSFETs can be significantly reduced by enhancing the channel mobility.

In the 1990s, SiC(0001) MOSFETs exhibited very poor channel mobilities below 10 cm^2/Vs. Interface nitridation with a nitric oxide (NO) gas after oxide formation (typically thermal oxidation of SiC) was proposed[47),48)] and has been the standard process for the production and research of SiC(0001) power MOSFETs for the last 20 years. Post-oxidation annealing in NO greatly reduces the interface state density in SiO_2/SiC structures and the channel mobility can be improved from 5–8 to 20–40 cm^2/Vs on SiC(0001).[48)]

Another breakthrough in the mobility enhancement was the fabrication of MOSFETs on non-basal planes other than SiC(0001). Figure 10(a) plots the channel mobility (effective mobility) as a function of the doping density of the p-body for SiC(0001), (11$\bar{2}$0), and (1$\bar{1}$00) MOSFETs.[49)] Here the gate oxides with a thickness of about 40 nm were formed by dry oxidation at 1300 °C and subsequent interface nitridation with NO at 1250 °C. The MOSFETs with lightly-doped p-body fabricated on (11$\bar{2}$0) and (1$\bar{1}$00) faces (see Fig. 4(b)) exhibit high mobilities of 117 and 115 cm^2/Vs, respectively, which are about three times higher than that of the SiC(0001) MOSFET, while maintaining the high threshold voltage. It is noted that a high channel mobility on SiC(11$\bar{2}$0) was first achieved with a wet oxidation technique.[50)]

Here the channel mobility in SiC MOSFETs is briefly discussed. A similar surface orientation dependence of the channel mobility is observed in Si MOSFETs, and this dependence has been explained mainly by the anisotropy in the effective mass.[51)] However, it is difficult to explain the large difference in the channel mobility between SiC(0001) and SiC(11$\bar{2}$0) (or (1$\bar{1}$00)) MOSFETs simply by the effective mass anisotropy. Extensive studies have revealed that the density of interface states (electrically active defect levels at the oxide/semiconductor interface) in SiC MOS structures near the conduction

band bottom is higher than that in Si MOS structures by two or three orders of magnitude.[8] Since the total interface state density ($>10^{12}\,\mathrm{cm}^{-2}$) is of the same order as the sheet electron density in the inversion channel, the majority of electrons induced by the gate bias are trapped at the interface states and these electrons become immobile (electron trapping effect). This is the primary reason why the channel mobility in SiC MOSFETs is so low. The interface states located near the conduction band bottom are acceptor-like, meaning that these interface states are negatively charged after trapping electrons. This negative charge works as a strong Coulomb scattering center for electrons in the inversion channel. This is another important cause of the low channel mobility. Figure 10(b) plots the channel mobility of various SiC n-channel MOSFETs fabricated on lightly-doped p-body versus the interface state density integrated from $E_c - 0.2\,\mathrm{eV}$ to $E_c - 0.5\,\mathrm{eV}$ (E_c: the conduction band bottom), which was extracted from C–V analyses of MOS capacitors. The data for SiC MOSFETs fabricated on different crystal faces and the gate-oxide formation processes are plotted in the figure. This figure indicates that the channel mobility is almost inversely proportional to the interface state density irrespective of the crystal face. Therefore, it can be concluded that the high channel mobilities of SiC$(11\bar{2}0)$ and $(1\bar{1}00)$ MOSFETs originate from the relatively low interface state density on these faces, and the anisotropy in the effective mass plays a minor role. However, it has not yet been clarified why the interface state density can be reduced by using these non-basal planes. It is known that the fixed charge density is usually smaller than the density of trapped electrons in the on-state of SiC MOSFETs. To reveal the scattering mechanism of electrons in SiC MOS channels, the electron trapping effect, Coulomb scattering by the trapped electrons, and roughness scattering have been investigated.[52]

The high mobility on the non-basal planes has been a strong driver for developing vertical trench MOSFETs, the schematic structure of which is shown in Fig. 11(a). The bottom half of a trench MOSFET is basically the same as that of a planar MOSFET shown in Fig. 1(c), but relatively narrow (about 1 µm width) trenches are formed near the surface in a trench MOSFET. The trench surface is covered with an oxide film and the trench is filled with the gate material (typically polycrystalline Si). When a sufficiently large positive voltage is applied to the gate, a conduction channel is formed on the trench sidewalls of the p-body, enabling the current flow. The trench sidewalls in SiC trench MOSFETs can be either $(11\bar{2}0)$ or $(1\bar{1}00)$. A magnified illustration of the region near the trench structure (without the oxide and the gate metal for simplicity) is shown in Fig. 11(b). Here the base material is "off-axis" SiC(0001) wafers, the surface of which is tilted from the (0001) face toward $[11\bar{2}0]$ by a small off-angle (typically 4°), because a high density of surface atomic steps induced by the off-cut serves as a template for perfect polytype replication during SiC epitaxial growth.[15),53] Therefore, the high channel mobility on SiC$(1\bar{1}00)$ is beneficial for fabricating SiC trench MOSFETs, because SiC$(1\bar{1}00)$ is easily formed along the trench sidewalls on SiC(0001) wafers tilted toward $[11\bar{2}0]$, as shown in Fig. 11(b). It is not easy to form an exact $(11\bar{2}0)$ face along the trench sidewalls because of the wafer tilting toward $[11\bar{2}0]$.

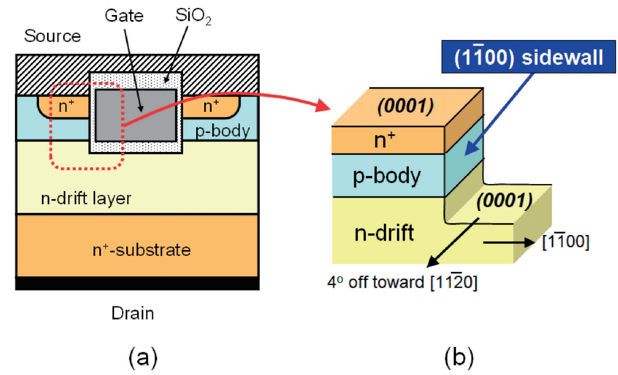

Fig. 11. (a) Schematic structure of a trench MOSFET. (b) Schematic illustration near the trench structure of a SiC trench MOSFET. The gate oxide and gate contact are omitted to clearly show the sidewall of the trench. SiC$(1\bar{1}00)$ is easily formed along the trench sidewall on a SiC(0001) wafer tilted toward $[11\bar{2}0]$.

Based on these results, the author demonstrated high-performance SiC trench MOSFETs in collaboration with Rohm. By using interface nitridation for gate oxides on the trench sidewalls and increasing the cell density, the on-resistance of SiC power MOSFETs could be reduced to $0.79\,\mathrm{m\Omega cm^2}$ for 630 V and $1.4\,\mathrm{m\Omega cm^2}$ for 1260 V devices,[54),55] which are about 80–200 times better than the Si unipolar limit. In more recent years, high-performance SiC power MOSFETs with breakdown voltage (V_B)–on-resistance (R_{on}) values of 1800 V–$2.0\,\mathrm{m\Omega cm^2}$,[56] 3800 V–$8.3\,\mathrm{m\Omega cm^2}$,[57] and 12000 V–$123\,\mathrm{m\Omega cm^2}$[58] have been reported. Furthermore, "super-junction" structures, which consist of multiple p- and n-pillars

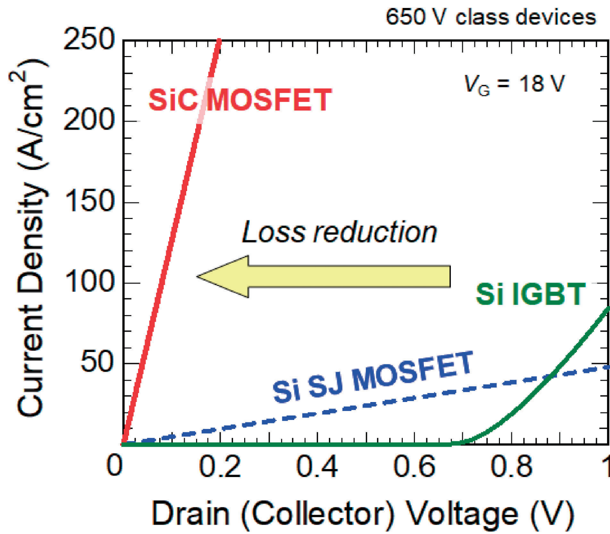

Fig. 12. On-state characteristics of SiC trench MOSFET, Si MOSFET, and Si IGBT at a gate voltage of 18 V, where the blocking voltage of all the devices is 650 V. The SiC trench MOSFET was developed by Rohm and the author's group. The Si MOSFET and IGBT are commercial devices. (Reproduced from Ref. 63.)

along the vertical direction, have successfully been formed with SiC, and very high performances of 1170 V–0.63 mΩcm^2,[59] and 7800 V–18 mΩcm^2,[60] have been demonstrated. The reliability issues of SiC power MOSFETs such as the threshold voltage instability,[61] degradation of body diodes,[62),63] and short-circuit ruggedness[64] have been extensively investigated in recent years.

Figure 12 compares the experimentally obtained on-state characteristics of several 650 V power switching devices.[63] Here the SiC trench MOSFET was developed by Rohm and my group.[55] The Si IGBT and MOSFET represent typical commercial devices. In the Si IGBT and MOSFET, the channel mobility is reasonably high, about 420–550 cm^2/Vs at a gate voltage of 18 V. However, the resistance of the thick n-layer (drift layer or voltage-blocking layer) governs the total on-resistance in Si power devices with a breakdown voltage higher than 600 V. Although Si IGBTs have been widely used in various applications,[65] a Si IGBT exhibits almost no current until the offset voltage of approximately 0.7 V is applied, owing to the built-in potential of the Si pn junction embedded at the collector side. Therefore, the on-state voltage drop of a Si IGBT is inherently higher than 0.8 V, which results in a certain on-state power loss even under partial-load conditions. Another drawback of Si IGBTs is the relatively slow switching speed and large switching loss due to minority carrier injection (bipolar operation). On the other hand, 650 V Si MOSFETs with a super-junction structure show fast switching because of the unipolar operation, and no offset voltage near the origin is observed,[66] as shown in Fig. 12. However, the on-resistance of a 650 V Si super-junction MOSFET is relatively high, leading to a higher voltage drop than a Si IGBT at a high current density. In contrast, SiC power MOSFETs can exhibit very low on-resistance without any offset voltage. Even though the channel mobility in SiC MOSFETs (about 10–20 cm^2/Vs on (0001) and about 40–70 cm^2/Vs on $(1\bar{1}00)$ or $(11\bar{2}0)$ with a relatively heavily-doped p-body) is much lower than that in Si MOSFETs, the resistance of the n-layer (drift resistance) is about 500 times lower than that in Si devices (Fig. 3), leading to a significantly lower on-resistance. The SiC power MOSFET shown in Fig. 12 can achieve a high current density of 200 A/cm^2 at a substantially lower drain voltage of about 0.16 V, compared with Si devices, which results in a much smaller on-state loss. In addition to the low on-state loss, fast switching can also be achieved with SiC MOSFETs.

4.2. Innovation for high-quality SiC MOS interface. Although high-performance SiC power MOSFETs have been developed, the on-resistance so far achieved is far from the ideal values especially in 600–1200 V class MOSFETs, due to the low electron mobility in the MOS channel (high channel resistance), as described in the last subsection. For a long time, thermal oxidation of SiC has been the standard method to form a gate oxide (SiO_2) for MOSFET fabrication. It is, however, not yet clear what happens with the host carbon atoms during oxidation of SiC. In the ideal case, carbon atoms are removed by making carbon monoxide (CO) as a byproduct, according to the reaction: $SiC + (3/2)O_2 \rightarrow SiO_2 + CO$. But it has been believed that some carbon atoms must remain near the SiO_2/SiC interface and those carbon atoms may be the main origin of interface defects. A "carbon-cluster model" has been proposed[67] and is supported by experimental results in a rather indirect manner. However, there exists no direct link between the "carbon clusters" and the interface defects energetically located near the conduction band bottom of SiC, which limit the electron mobility in the MOS channel. Despite extensive physical and chemical analyses of the SiO_2/SiC structures, no consensus on the origin of interface defects has been reached in the community.[63),68]

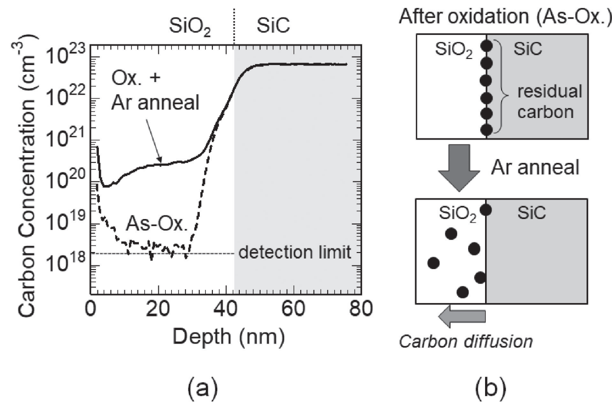

Fig. 13. (a) Depth profiles of carbon atom density in the SiO_2/SiC structures before and after Ar annealing at 1300 °C, measured by secondary ion mass spectrometry (SIMS).[69] (b) Schematic images explaining the SIMS results in (a). Excess carbon atoms may be present near the interface after oxidation, and they may be released and diffuse toward the surface by high-temperature Ar annealing.

The author's group performed depth analyses of carbon atom density in many different SiO_2/SiC structures annealed under various conditions and discovered important details of the behavior of carbon atoms in the system. Figure 13(a) shows the depth profiles of carbon atom density in the SiO_2/SiC structures, which were measured by SIMS.[69] Two SiC(0001) samples were simultaneously oxidized at 1300 °C for 30 min, which yielded a 42 nm-thick SiO_2 layer on the surface. After the oxidation, one sample was subjected to annealing in pure Ar at 1300 °C for 1 min. As shown in Fig. 13(a), the carbon atom density in the SiO_2 layer is below the detection limit (about $2 \times 10^{18}\,\mathrm{cm}^{-3}$) for the as-oxidized sample, but it significantly increased to the $10^{20}\,\mathrm{cm}^{-3}$ range after Ar annealing. The area density of carbon atoms obtained by integrating the carbon atom density inside the oxide is as high as $1\text{–}2 \times 10^{15}\,\mathrm{cm}^{-2}$, which is almost the same as the surface carbon atom density on SiC(0001). Here the source of carbon atoms, which cause severe carbon contamination in the oxide by Ar annealing, must be present in the SiC side or at the interface. It is known that the carbon interstitial density inside a SiC epilayer is extremely low ($<10^{11}\,\mathrm{cm}^{-3}$) because carbon interstitials diffuse out during the epitaxial growth.[8] Besides, a carbon atom substituting at a lattice site in SiC does not diffuse even at a very high temperature such as 1900 °C. Thus, the carbon source is most likely excess carbon atoms located very near the oxide/SiC interface. And the carbon atoms may be released and diffuse toward the surface by high-temperature Ar annealing. This speculation is schematically shown in Fig. 13(b). It is also of interest that the interface state density exhibited a marked decrease by this high-temperature Ar annealing (carbon reduction) after thermal oxidation, though the obtained interface defect density was not sufficiently low.[70]

In another approach, the author's group extracted the interface state density very close to the conduction band bottom ($E_c - (0.03\text{–}0.18)\,\mathrm{eV}$) through MOS-Hall effect measurements combined with an analysis of the quantum-confinement-induced energy levels inside the inversion layer. A significant difference between the measured Hall mobility and the effective channel mobility was observed due to the severe electron trapping effect. For example, the Hall mobility of a SiC(0001) MOSFET with a gate oxide annealed in NO fabricated on a lightly-doped p-body was 118–134 cm^2/Vs at room temperature, whereas the effective mobility determined from the MOSFET characteristics was as low as 36–41 cm^2/Vs, indicating that about 70% of electrons induced by the gate bias are trapped at the interface states. By using the Hall effect data (both the Hall mobility and the sheet electron density) and MOSFET characteristics, the energy distribution of interface state density was extracted. Here, the energy levels and wavefunctions of electrons inside the channel were calculated by solving the Poisson and Schrödinger equations self-consistently.[71] This analysis clarified that the interface state density distribution is uniquely determined irrespective of the p-body doping in a wide range ($10^{15}\text{–}10^{18}\,\mathrm{cm}^{-3}$), when the energy level of interface defects is defined with respect to the bottom edge of the two-dimensional density of states of SiC considering the quantum confinement effect, whereas the defect distribution exhibits a large and unreasonable variation when the energy level is defined with respect to the three-dimensional density of states. In other words, the energy distribution of the interface state density near E_c in SiC MOS structures seems to be shifted upward due to quantum confinement inside the channel potential. Since the defect states in the gate oxide must be free from quantum confinement because the defects are located outside the channel potential, this type of defects may be excluded as a major origin of interface states near E_c.[71] If a significant portion of "interface states" are located in the SiC bulk region very close to the interface, such a quantum confinement effect may be expected.

In the meantime, several first-principles calculations of defects near the SiO_2/SiC interface have revealed that a $(C\text{-}C)_C$ defect at the interface,[72] a $(C\text{-}C)_{Si}$ defect inside SiC,[73] a C-ring defect inside SiO_2,[74] and some other C-related defects have relatively low formation energy at a typical oxidation temperature (1200–1300 °C) and these defects create electrically active levels in the bandgap near E_c. Based on the SIMS results, the energy levels of interface defects, considering the quantum confinement effects, and the theoretical prediction mentioned above, it is presumed that thermal oxidation of SiC may inevitably induce generation of various C-related defects at and near the SiO_2/SiC interface. Therefore, the author's group has attempted to improve the SiC MOS interface by preventing oxidation of SiC.

Figure 14 shows the schematic process flows of gate oxide formation on SiC, where Fig. 14(a) is the conventional process and Figs. 14(b) and (c) illustrate the proposed processes to avoid thermal oxidation of SiC. In Fig. 14(b) (Process A), a polycrystalline Si thin film is deposited on SiC and this Si film is converted to SiO_2 by thermal oxidation.[75] Here the etching of the SiC surface with a hydrogen (H_2) gas at 1300 °C prior to the Si deposition is effective in removing a very thin (<10 nm) defective layer near the surface, which is created by sacrificial oxidation performed during the MOSFET fabrication. The temperature of Si oxidation for obtaining SiO_2 must be as low as possible (typically 750 °C), so that SiC is never oxidized while Si is completely converted to SiO_2. In Fig. 14(c) (Process B), a SiO_2 film is directly deposited on the SiC surface by chemical vapor deposition (CVD).[76] In either case, without H_2 etching of the SiC surface at 1300–1350 °C prior to thin film deposition (Si or SiO_2) as well as interface nitridation after oxide formation, the interface state density was even higher than that by the conventional process shown in Fig. 14(a).

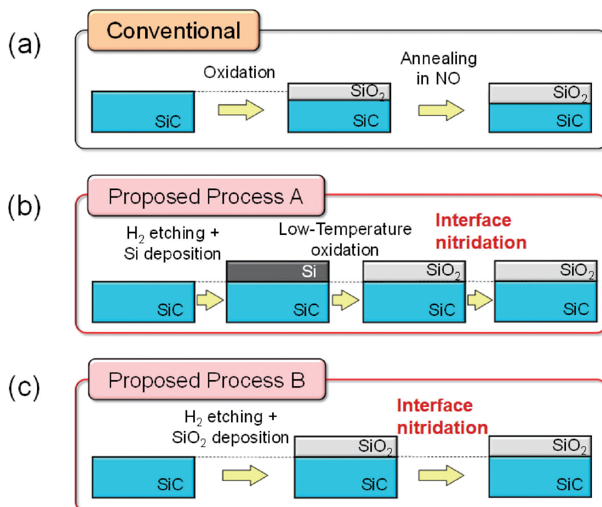

Fig. 14. Schematic process flows of gate oxide formation on SiC. (a) Conventional process. (b) and (c) illustrate the proposed processes that avoid thermal oxidation of SiC.

The energy distributions of the interface state density obtained for several SiO_2/SiC(0001) MOS structures are plotted in Fig. 15, where the results obtained by the proposed processes A and B are compared with the conventional ones. Here n-type MOS capacitors with an oxide thickness of about 30 nm were prepared and the interface state density was extracted by a high(1 MHz)–low(quasi-static) method. "As-Ox" and "Ox-NO" denote the results for the conventional processes, namely oxide formation by thermal oxidation without and with post-oxidation annealing in NO at 1250 °C, respectively. In Fig. 15(a), "H_2-Si-Ox-N_2" and "H_2-Si-Ox-NO" indicate the proposed processes shown in Fig. 14(b) with interface nitridation by N_2 and NO, respectively (Process A), where N_2 annealing was performed at 1400 °C for 45 min and NO annealing at 1250 °C for 70 min. The "H_2-Si-Ox-N_2" process resulted in a very low interface state density below $3 \times 10^{10}\,cm^{-2}eV^{-1}$ in the extracted energy range near the conduction band bottom (E_c). The interface state density obtained by the "H_2-Si-Ox-NO" process is higher than that by "H_2-Si-Ox-N_2", probably due to slight oxidation during the annealing step in NO. However, the interface state density is lower than that by the "Ox-NO" process which has been adopted for the production of SiC MOSFETs. On the other hand, "H_2-CVD-N_2" and "H_2-CVD-NO" in Fig. 15(b) denote the proposed processes shown in Fig. 14(c) with interface nitridation by N_2 and NO, respectively (Process B), where N_2 annealing was performed at 1450 °C for 45 min and NO annealing at 1250 °C for 70 min. By the proposed processes ("H_2-CVD-N_2" and "H_2-CVD-NO"), the interface state density can be reduced to a mid $10^{10}\,cm^{-2}eV^{-1}$ near E_c. In the conventional processes ("As-Ox" and "Ox-NO"), the interface state density exhibits a rapid increase toward E_c, which is the main cause for the very low channel mobility in n-channel SiC(0001) MOSFETs.[8] In contrast, no such sharp increase in the interface state density near E_c was observed and the distribution was rather flat in the measured energy range for the MOS structures formed by the proposed

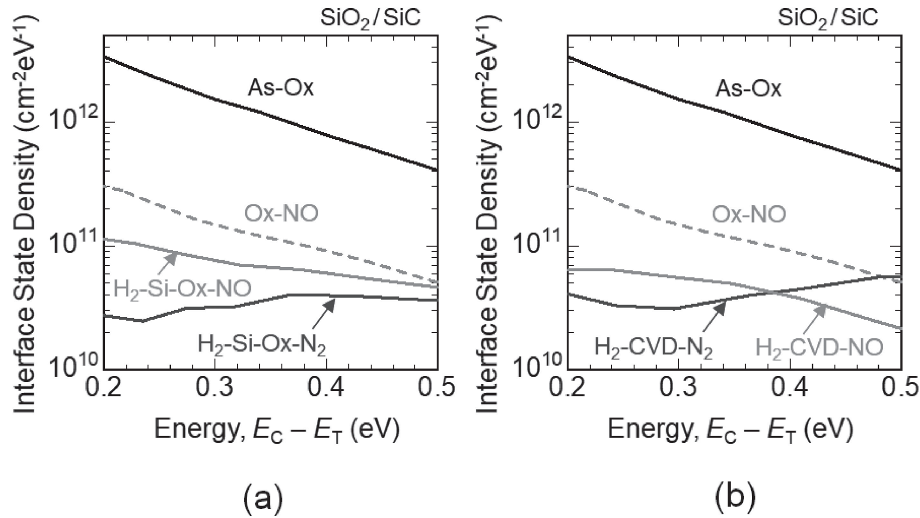

Fig. 15. Energy distributions of interface state density obtained for several SiO_2/SiC(0001) MOS structures, extracted by a high(1 MHz)–low(quasi-static) method on n-type MOS capacitors with an oxide thickness of about 30 nm. "As-Ox" and "Ox-NO" denote the results for the conventional processes, namely oxide formation by thermal oxidation without and with post-oxidation annealing in NO, respectively. (a) "H_2-Si-Ox-N_2" and "H_2-Si-Ox-NO" denote the proposed processes shown in Fig. 14(b) with interface nitridation by N_2 and NO, respectively (Process A). (b) "H_2-CVD-N_2" and "H_2-CVD-NO" indicate those for the proposed processes shown in Fig. 14(c) with interface nitridation by N_2 and NO, respectively (Process B).

processes ("H_2-Si-Ox-N_2", "H_2-CVD-N_2" and "H_2-CVD-NO"), implying that the defect nature may be different. Thus, exclusion of SiC oxidation is effective for reducing interface states, but it has not yet been clarified why the obtained energy distribution of the interface state density is different for different nitridation processes (annealing in N_2 or NO). Slight oxidation (about 0.5–1 nm) during the annealing in NO may affect the interface quality. Furthermore, the role of nitrogen atoms in interface state reduction is not clear at present. After nitridation, nitrogen atoms are accumulated at the interface, which can be monitored by SIMS. However, chemical information about Si-N or C-N bonding has not been acquired because the density is below the detection limit of common chemical/physical analyses. Further studies are required to reveal the mechanism of this defect reduction as well as the origin of interface states itself in SiC MOS structures.[63]

To investigate the impact of interface defect reduction on device characteristics, n-channel SiC(0001) MOSFETs were fabricated on p-type epitaxial layers with an acceptor density of 1–$3 \times 10^{15}\,cm^{-3}$. Figure 16 demonstrates the channel mobility (field-effect mobility) versus the gate voltage for SiC MOSFETs with gate oxides (thickness: about 30 nm) formed with four different processes, the two conventional ones ("As-Ox" and

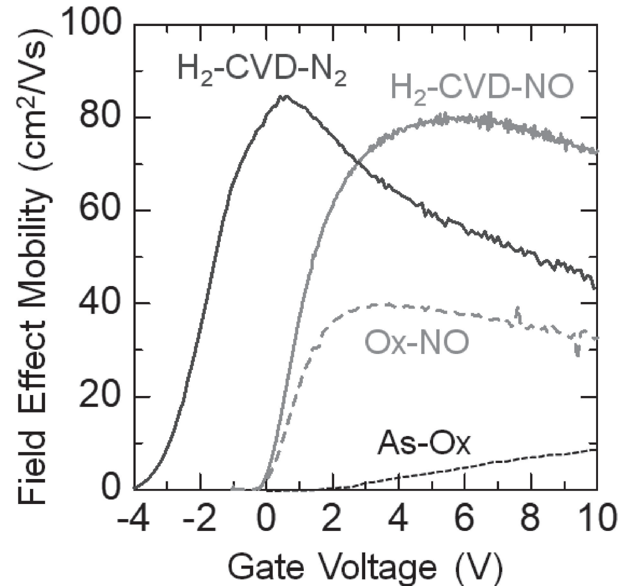

Fig. 16. Channel mobility (field-effect mobility) versus gate voltage for SiC(0001) MOSFETs with gate oxides formed with four different processes, two conventional ones ("As-Ox" and "Ox-NO") and two proposed ones ("H_2-CVD-N_2" and "H_2-CVD-NO"). (Reproduced from Ref. 77.)

"Ox-NO") and the two proposed ones ("H_2-CVD-N_2" and "H_2-CVD-NO").[77] The peak mobility for the "Ox-NO" MOSFET is $41\,cm^2/Vs$, which is typical

and has been unchanged for the last 20 years. Although the "H_2-CVD-N_2" MOSFET exhibited a high peak mobility of 85 cm^2/Vs, the threshold voltage was shifted in the negative direction, resulting in normally-on operation (a current flows at zero gate voltage). In power devices, normally-on operation is not desirable for fail-safe reasons. On the other hand, a similarly high peak mobility of 80 cm^2/Vs with normally-off operation (threshold voltage: 0.92 V) was achieved with the "H_2-CVD-NO" MOSFET. The high mobility in n-channel MOSFETs reflects the low interface state density near the conduction band bottom, which was attained by the proposed three-step process, (i) hydrogen etching to remove the surface defective layer, (ii) oxide formation without oxidation of SiC, and (iii) interface nitridation. It is noted that the results shown in Figs. 15 and 16 were obtained on SiC(0001). Since relatively high channel mobilities of 100–120 cm^2/Vs can be achieved on SiC($11\bar{2}0$) and ($1\bar{1}00$) even by the conventional process (dry oxidation followed by annealing in NO) as shown in Fig. 10, fabrication of SiC MOSFETs on these non-basal planes by using the proposed processes is currently in progress.

In Si MOSFETs, the channel mobility can be reproduced by a model, which considers phonon scattering, Coulomb scattering, and interface roughness scattering.[78] In SiC MOSFETs, however, electron trapping at the interface states and Coulomb scattering by trapped electrons are significant and the channel mobility cannot be analyzed simply by the Si-MOSFET model. To understand the carrier scattering in an inversion layer of a SiC MOSFET, further basic studies are required. Since the electron trapping effect must be much smaller for the proposed processes, MOS-Hall effect measurements will provide important insight into the carrier scattering in SiC MOSFETs. For example, Coulomb scattering by the fixed charges and roughness scattering may be clearly observed.

To fabricate high-performance and high-reliability MOSFETs requires sufficiently high dielectric breakdown characteristics of the gate oxide as well as stability of the threshold voltage against the high gate bias. The leakage current through the oxide formed by the proposed "H_2-CVD-NO" process was below the detection limit (10^{-9} A/cm^2) until 6 MV/cm and exhibited Fowler-Nordheim tunneling current with a barrier height of about 2.7 eV from 6 to 11 MV/cm. The breakdown electric field of the oxide was as high as 11.2 MV/cm. In addition, positive and negative bias stress (oxide field: ±4 MV/cm) on the "H_2-CVD-NO" MOSFET did not cause a threshold voltage shift ($\Delta V_{\mathrm{th}} < 0.05$ V). Thus, the proposed process offers a new approach to SiC MOSFET development and can be a key technology for the future. The fabrication of SiC MOSFETs using Process A ("H_2-Si-Ox-N_2" and "H_2-Si-Ox-NO") is under investigation.

5. Progress and future challenges of ultrahigh-voltage SiC bipolar devices

5.1. Potential of SiC bipolar devices and carrier lifetime enhancement. In power devices, unipolar devices such as MOSFETs and SBDs are desirable because unipolar devices exhibit fast and low-loss switching characteristics and their fabrication is easier. In unipolar devices, the resistance of the n-layer (drift layer or voltage blocking layer) is determined by the thickness and donor density, because only electrons supplied from intentionally doped donors contribute to the current. When the breakdown voltage is designed to exceed a certain value, however, the n-layer resistance (drift resistance) becomes unacceptably high, which is shown as the material limit in Fig. 3. In Si power devices, the n-layer resistance becomes very high (>50 m$\Omega$$cm^2$) when the breakdown voltage is higher than 600–800 V. For higher-voltage devices, minority carrier injection from a p-region to the thick n-layer is utilized (bipolar operation), which results in a significant reduction of the n-layer resistance, because both electrons and holes, the density of which is higher than the donor density, can contribute to the current. Therefore, bipolar devices such as IGBTs are used for high-voltage applications.

One inherent limitation of Si power devices is the ultrahigh-voltage blocking capability. When the breakdown voltage exceeds 10 kV, the required thickness and donor density of the n-layer become about 1.2 mm and 1×10^{13} cm^{-3}, respectively. Such wafers are difficult to produce and the required donor density is close to the intrinsic carrier density of Si at 120 °C. Fabrication of ultrahigh-voltage SiC devices is much easier compared with Si, owing to the about ten times higher critical electric field. For example, the thickness and donor density of the n-layer required for 10 kV SiC devices are about 80 µm and 8×10^{14} cm^{-3}, respectively. However, the resistance of this thick and lightly-doped n-layer becomes high for such ultrahigh-voltage unipolar devices even with SiC. Hence, SiC bipolar devices are attractive for 10 kV (or higher) applications.

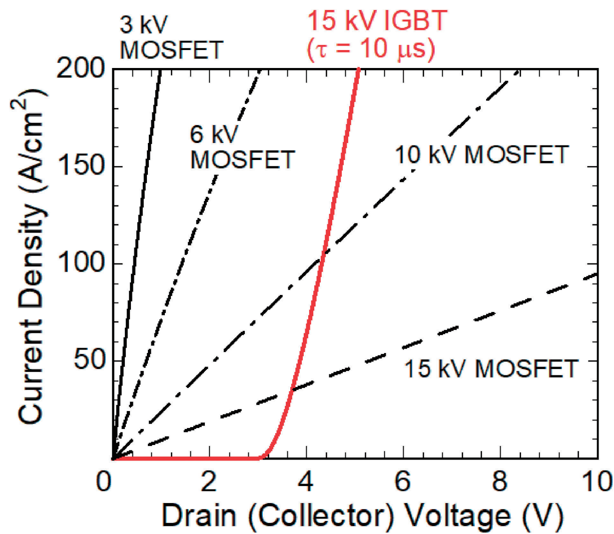

Fig. 17. On-state characteristics of SiC power MOSFETs with several different breakdown voltages plotted by black lines. The characteristic of a 15 kV SiC IGBT is shown by the red solid line, indicating the superior potential of ultrahigh-voltage SiC IGBTs. These characteristics were obtained by device simulation. The channel mobility was assumed to be 20 cm^2/Vs.

In Fig. 17, the simulated on-state characteristics of SiC power MOSFETs with several different breakdown voltages are plotted by black lines. The same assumptions for the channel (channel mobility = 20 cm^2/Vs), junction FET, and substrate resistances as those in Fig. 9 were used in calculating the on-state characteristics. Since the resistance of the voltage-blocking region (drift resistance) exhibits a rapid increase with increasing the breakdown voltage as shown in Fig. 3, the on-resistance becomes very high for a 15 kV MOSFET even with SiC. By utilizing minority-carrier injection (bipolar operation) with an IGBT structure (Fig. 1(d)), the resistance of the thick and lightly-doped n-layer (voltage-blocking region) can be greatly reduced, leading to a superior on-state characteristic, as plotted by the red solid line. Here the carrier lifetime in the n-layer was assumed to be 10 µs. Though a relatively large offset voltage of 3 V is observed due to the wide bandgap of SiC, the voltage drop at high current density of a 15 kV SiC IGBT is much smaller than that of a 15 kV SiC MOSFET.

In bipolar devices, the lifetime of injected carriers (carrier lifetime) is of crucial interest, because it determines both the on-state and switching characteristics. For high-performance ultrahigh-voltage devices, a long carrier lifetime is the key material requirement because it naturally leads to a longer diffusion length of minority carriers and thereby to an enhanced reduction of the resistance of the high-resistivity voltage-blocking region. In current Si bipolar-type power devices such as IGBTs, the carrier lifetime is kept very long to reduce the on-resistance, while the switching speed and loss can be minimized by optimizing the amount and depth profile of injected carriers, because the amount of injected carriers should govern both on-state and switching performances rather than the lifetime itself.[65] This concept can be applied to SiC bipolar devices.

Until 2008, SiC exhibited short carrier lifetimes, typically, below 1 µs in spite of its indirect-transition band structure. Figure 18(a) shows the inverse of the carrier lifetime versus carbon vacancy density obtained for very thick and lightly-doped SiC epitaxial layers.[37),63] The author's group identified that a carbon vacancy defect creates multiple deep levels called "$Z_{1/2}$ center" in the bandgap of SiC by combining deep level transient spectroscopy (DLTS) and photo-excited electron paramagnetic resonance (EPR) measurements on specially-prepared SiC samples.[79] As shown in Fig. 18(a), the inverse of the carrier lifetime is in proportion to the carbon vacancy density in a wide range, indicating that the carbon vacancy is the primary lifetime killer in SiC.[80] The author's group also experimentally determined the capture cross-sections of electrons and holes for the four levels of a carbon vacancy in SiC (E_c − 0.41, 0.46, 0.54, 0.58 eV) and constructed a carrier recombination model via the multiple levels by using the rate equations of electron and hole densities (Fig. 18(b)).[81] The red solid line in Fig. 18(a) denotes the relationship between the carrier lifetime and the carbon vacancy density calculated with the developed model. The calculated result shows very good agreement with the experimental data plotted by symbols. The large capture cross sections of holes (5–7×10^{-14} cm^2) for these four negatively-charged levels are mainly responsible for the significant carrier recombination via these defects.[81]

Since the carbon vacancy defects limit the carrier lifetime in SiC, the density must be reduced to a sufficient level to achieve a long carrier lifetime. It was discovered that carbon vacancy defects can be drastically reduced by either carbon ion implantation and subsequent annealing in Ar at 1500–1700 °C[82] or thermal oxidation at 1300–1500 °C.[83] In either case, it is understood that excess carbon atoms are introduced to a near-surface region of SiC and those carbon atoms diffuse toward a deeper region.

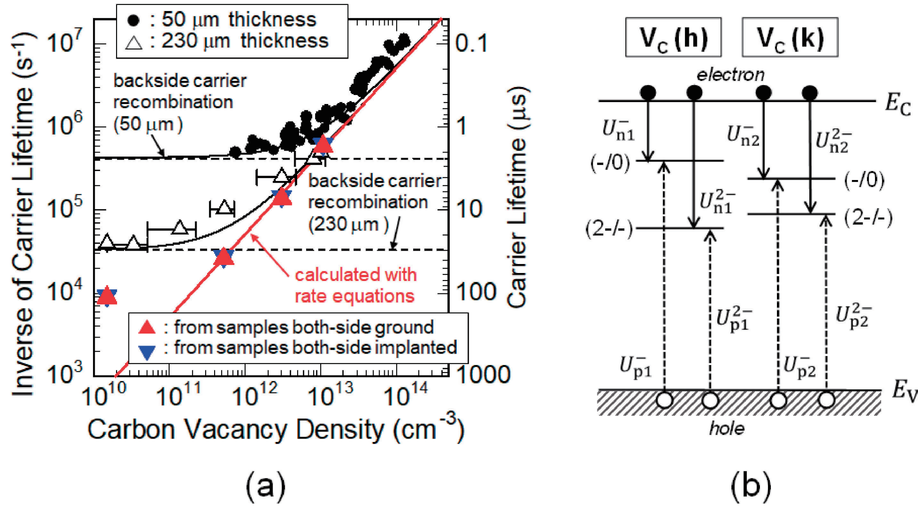

Fig. 18. (a) Inverse of carrier lifetime versus carbon vacancy density obtained for very thick and lightly-doped SiC epitaxial layers,[37),63)] where the symbols denote the experimental data and the red line is the calculated result. The closed circles and open triangles denote the carrier lifetimes obtained from about 50 µm- and 230 µm-thick lightly-doped n-type SiC epitaxial layers on n-type substrates, respectively. The red triangles and blue inverted triangles depict the carrier lifetimes extracted from the lifetime data for lightly-doped n-type free-standing epitaxial layers, where both sides (front and back sides) were ground and Ar-implanted, respectively. (Reproduced from Ref. 63.) (b) Carrier recombination model taking into account four levels associated with a carbon vacancy defect in SiC. The carbon vacancy at the hexagonal site (V_C(h)) and cubic site (V_C(k)) creates both the (−/0) and (2−/−) levels. Here U_{ni} and U_{pi} ($i = 1, 2$) denote the effective capture rate of electrons and holes, respectively, at the individual defect levels.

Although the source of excess carbon atoms during oxidation of SiC has not been fully clarified, it is presumed that excess carbon atoms are emitted from the oxidation front because carbon atoms are not necessary to form SiO_2 via oxidation of SiC. Since the depth profiles of the carbon vacancy and some other carbon-interstitial-related defects in oxidized SiC are very similar to those in SiC implanted with carbon ions and subsequent annealing as far as the process temperatures are the same, a very similar phenomenon must be taking place during the oxidation process and the carbon implantation process. Note that a carbon interstitial in SiC shows very large diffusion constant even at 1300–1400 °C, whereas a carbon vacancy is immobile even at 1800 °C. The diffusion of silicon interstitials and impurities is negligibly small at temperatures below 1800 °C. During the carbon diffusion, a carbon atom fills a carbon vacancy, resulting in annihilation of the carbon vacancy. It is noted that this is another indication that thermal oxidation of SiC induces generation of excess carbon atoms inside SiC, which was suggested in subsection 4.2.

Figure 19(a) shows the depth profiles of the carbon vacancy density in SiC (260 µm-thick epitaxial layer) after thermal oxidation at 1400 °C for several different periods.[37)] Here the depth profiles were acquired by repeating DLTS measurements and mechanical polishing. Figure 19(b) shows a possible schematic image of the diffusion of carbon interstitials and elimination of carbon vacancies during thermal oxidation of SiC. In the as-grown SiC epitaxial layer, the carbon vacancy density is $8 \times 10^{12}\,\mathrm{cm}^{-3}$ throughout the measured region. By prolonging the oxidation period, the carbon vacancy defects are almost removed from the surface to the deep region, and the thickness of the almost carbon-vacancy-free region reaches about 200 µm after oxidation for 72 h. The carbon vacancy density in the defect-eliminated region is below $2 \times 10^{10}\,\mathrm{cm}^{-3}$ (detection limit). The thickness of the defect-eliminated region is proportional to the square root of the oxidation period, implying that this defect elimination is limited by diffusion of some species, most likely carbon interstitials. Because the thickness of the voltage-blocking region required for fabrication of 10 and 20 kV SiC devices is about 80 and 160 µm, respectively, the 200 µm-thick SiC layer with an extremely low carbon vacancy density shown in Fig. 19(a) is promising for fabricating such ultrahigh-voltage devices. It is noted that the oxidation period for the defect elimination can be considerably shortened when the carbon vacancy density in an initial SiC crystal is low,[84)] which can be achieved by

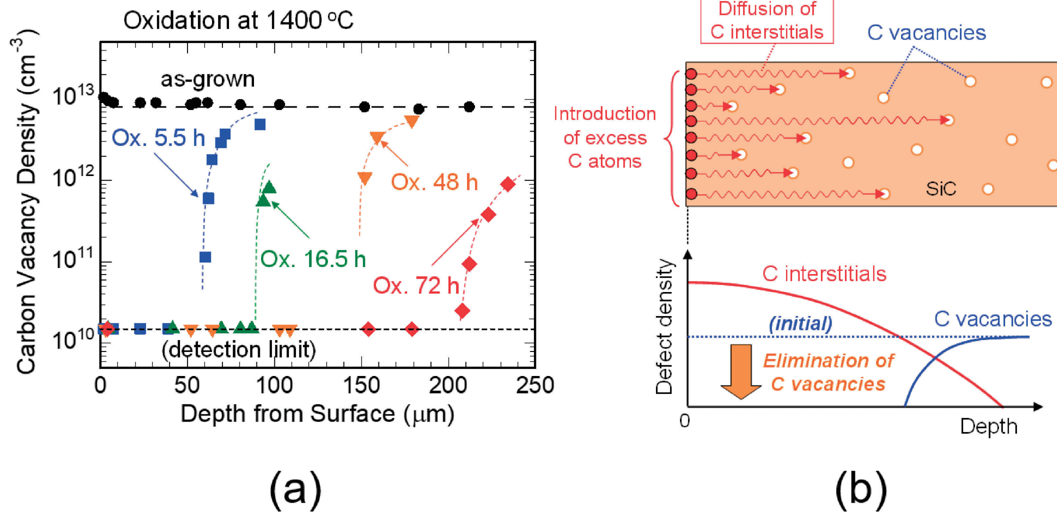

Fig. 19. (a) Depth profiles of the carbon vacancy density in SiC after thermal oxidation at 1400 °C for several different periods.[37] The depth profiles were acquired by repeating DLTS measurements and mechanical polishing. (b) Schematic image of carbon interstitial diffusion and carbon vacancy elimination during oxidation of SiC. (Reprinted from T. Kimoto *et al.*, J. Phys. D: Appl. Phys., vol. 51, 363001 (2018), with the permission of IOP Publishing.)

optimizing the growth condition.[8] It is noted that thermal oxidation is very effective for the elimination of carbon vacancy defects but it will induce generation of carbon-associated defects near the SiO_2/SiC interface, as described in 4.2. In real device fabrication, chemical etching such as high-temperature H_2 etching of the SiC surface after thermal oxidation can solve this latter problem while maintaining a very low carbon vacancy density.

The carrier lifetime can be indeed enhanced by eliminating carbon vacancy defects. Figure 20 depicts the decay curves of the excess carrier density measured at 293 K for about 230 μm-thick n-type SiC epitaxial layers doped to $1 \times 10^{14}\,cm^{-3}$ before and after carbon vacancy elimination by oxidation at 1400 °C for 72 h. The decay curves were acquired by microwave-detected photoconductance decay (μ-PCD) measurements. Here the excitation source was a pulsed YLF (yttrium lithium fluoride)-3HG laser with a wavelength of 349 nm. The decay of the electrical conductance (which is proportional to the excess carrier density) was monitored by the microwave reflectivity at a frequency of 26 GHz. A surface oxide formed by the oxidation was etched off with HF acid before the measurements. The carrier lifetime for the as-grown SiC (without oxidation) was 2.1 μs, whereas it increased to 48 μs after the carbon vacancy elimination, a more than 20-fold improvement. The major recombination path of excess carriers in such high-quality SiC with an extremely low carbon

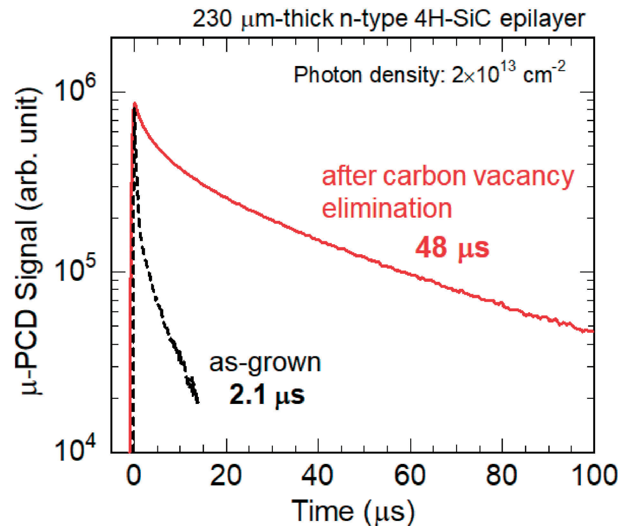

Fig. 20. Decay curves of the excess carrier density for about 230 μm-thick SiC epitaxial layers before and after carbon vacancy elimination by oxidation at 1400 °C for 72 h. The decay curves were acquired by microwave-detected photoconductance decay (μ-PCD) measurements. (Reprinted from T. Kimoto *et al.*, J. Phys. D: Appl. Phys., vol. 51, 363001 (2018), with the permission of IOP Publishing.)

vacancy density (*e.g.*, carbon vacancy density $<10^{11}\,cm^{-3}$ in Fig. 18(a)) is an open question.

5.2. Ultrahigh-voltage SiC devices. In addition to the carrier lifetime, an important challenge for fabricating ultrahigh-voltage (>10 kV)

SiC devices is epitaxial growth of a very thick (>100 µm) and high-purity (~10^{14} cm^{-3}) epitaxial layer as a voltage-blocking region. The author's group developed fast epitaxial growth of SiC using a custom-made chemical vapor deposition (CVD) system (horizontal "hot-wall" CVD reactor).[22),85)] The source gases were SiH_4 and C_3H_8 with a carrier gas of H_2 and the substrate temperature during the epitaxial growth was 1650 °C. The growth rate was increased from 10 to 48 µm/h while maintaining a flat surface and high purity (<5×10^{13} cm^{-3}).[85)] A key issue for fast SiC epitaxy is prevention of silicon-cluster formation in the gas phase during the CVD growth of SiC. To achieve this, the reactor pressure was reduced from 12–15 kPa to 4 kPa.

The enhancement of the carrier lifetime in SiC described in the previous subsection has resulted in a significant performance improvement of ultrahigh-voltage SiC bipolar devices.[86),87)] Figure 21 demonstrates the forward characteristics of 13 kV SiC pin diodes fabricated with and without enhancement of the carrier lifetime.[87)] Here a pn junction was epitaxially grown on a low-resistivity SiC(0001) substrate, and a mesa structure was formed for device isolation. The voltage-blocking region was a 98 µm-thick SiC epitaxial layer doped with nitrogen to 2×10^{14} cm^{-3}. For the carrier lifetime enhancement, thermal oxidation was performed at 1400 °C for 24 h. The forward characteristics were markedly improved by the lifetime enhancement. The differential on-resistance at 200 A/cm^2 could be reduced from 4.7 to 1.4 mΩcm^2, which is about 50 times better than the SiC unipolar limit shown in Fig. 3. Since the substrate resistance is 0.63 mΩcm^2, the resistance of the thick voltage-blocking region is estimated to be lower than 0.8 mΩcm^2.

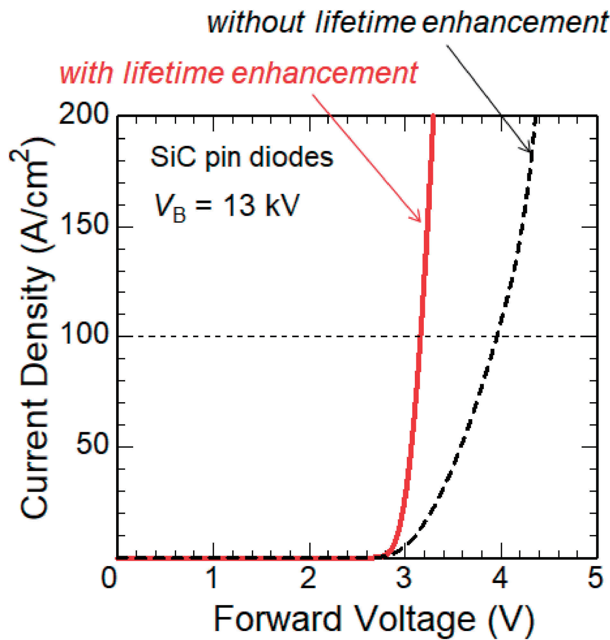

Fig. 21. Forward characteristics of 13 kV SiC pin diodes fabricated with and without enhancement of the carrier lifetime.[87)] The voltage-blocking region was a 98 µm-thick SiC epitaxial layer doped with nitrogen to 2×10^{14} cm^{-3}. Carrier lifetime enhancement was achieved by thermal oxidation at 1400 °C for 24 h.

By using thicker and high-purity voltage-blocking regions, extremely high-voltage (>20 kV) SiC devices have been demonstrated. Figure 22 depicts the current density–voltage characteristics of a fabricated SiC pin diode (area: 0.21 cm^2).[88)] A 268 µm-thick SiC epitaxial layer with a donor density of 1–2×10^{14} cm^{-3} was prepared. This thickness is about 10 times larger and the donor density is about 10 times lower than the typical values employed in fabricating 3 kV SiC power devices. After the lifetime enhancement by oxidation at 1400 °C for 72 h, a 2 µm-thick p-type anode doped with aluminum to 1×10^{19} cm^{-3} was epitaxially grown. In any high-voltage devices, electric field crowding along the device edge (periphery) must be minimized to achieve a nearly ideal breakdown voltage, which can be calculated using the impact ionization coefficients. To alleviate electric field crowding, the diode edge was terminated by combination of a sloped mesa and an advanced junction termination extension

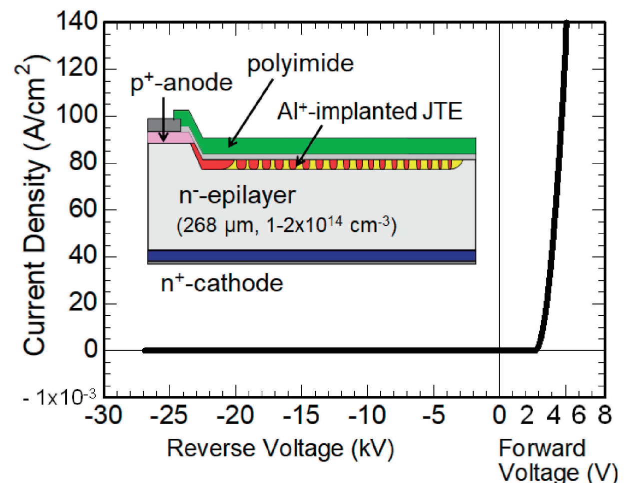

Fig. 22. Current density–voltage characteristics of a 27 kV SiC pin diode.[88)] A 268 µm-thick SiC epitaxial layer with a donor density of 1–2×10^{14} cm^{-3} was prepared for the voltage-blocking region. The inset shows the schematic structure of the pin diode.

(JTE).[88] In a desirable JTE structure, the acceptor density in the p-region formed along the device periphery is gradually decreased from the inner side to the outer edge. In conventional approaches, three-step ion implantation or a combination of ion implantation and plasma etching has been adopted to achieve such a gradual decrease in the acceptor density. In the original JTE shown in the inset of Fig. 22, the width of the p-rings formed by the second implantation is modulated by the mask design, to obtain an ideal acceptor density distribution along the horizonal direction. This original JTE structure was formed by two-step aluminum ion implantation. This structure offers a wide window for the optimum JTE dose and superior tolerance against fluctuations of the surface charge[88] compared with the conventional two (or three)-zone JTE.[89] As shown in Fig. 22, the fabricated diode exhibited an extremely high breakdown voltage over 27 kV, which was a limitation of the measurement setup. Since the maximum breakdown voltage of Si devices is 8–11 kV, SiC devices can break the Si limit by a factor of about 3. In spite of the very high breakdown voltage, a low differential on-resistance of 9.7 $m\Omega cm^2$ was achieved, thanks to the lifetime enhancement of the thick voltage-blocking region. These characteristics of 13 kV–1.4 $m\Omega cm^2$ and 27 kV–9.7 $m\Omega cm^2$ are the exceptionally high performance among any high-voltage semiconductor diodes. The temperature dependence of these characteristics has been discussed in the literature.[90]

A device simulation study revealed that the forward characteristics of these ultrahigh-voltage SiC diodes can be reproduced with a carrier lifetime of 4–6 µs in the voltage-blocking region,[88),91] which is much shorter than the values (30–48 µs) measured for lightly-doped SiC after lifetime enhancement described in the previous subsection. In forward-bias operation of pin diodes, the excess carrier density exceeds $5 \times 10^{16}\,cm^{-3}$ at a current density of 100–200 A/cm^2. Under this high-injection condition, band-to-band and Auger recombinations cannot be neglected.[91),92] Therefore, the carrier lifetime determined by the band-to-band and Auger recombinations can be an inherent limitation in the ultrahigh-voltage bipolar devices.

Regarding SiC ultrahigh-voltage (>20 kV) switching devices, bipolar junction transistors,[93] thyristors,[94] and IGBTs[95),96] have been reported. Each device has inherent merits and disadvantages. The author's group demonstrated an npn-type SiC bipolar junction transistor with a record performance.[93] After epitaxial growth of a 186 µm-thick n-type voltage-blocking layer on an n-type SiC(0001) substrate, a 0.35 µm-thick p-type base and a 1.2 µm-thick n-type emitter were continuously grown. The doping density was $2 \times 10^{14}\,cm^{-3}$ (nitrogen) for the voltage-blocking layer, $1 \times 10^{18}\,cm^{-3}$ (aluminum) for the base, and $2 \times 10^{19}\,cm^{-3}$ (nitrogen) for the emitter, respectively. The 100 µm-wide emitter fingers were defined by a 1.3 µm-deep etching. The edge of the collector junction was terminated with a sloped mesa and the original JTE. A very high breakdown voltage of over 23 kV was achieved, which is the highest recorded for a bipolar junction transistor. Since surface recombination near the emitter junction severely affects the current gain,[97] the surface was passivated with deposited SiO_2 annealed in NO. The current gain was improved from about 34 to 63 by this surface passivation. In SiC bipolar junction transistors, however, the on-resistance is almost identical to the unipolar resistance of the voltage-blocking region, and the on-resistance of the 23 kV SiC transistor is relatively high at 321 $m\Omega cm^2$.

The primary advantage of IGBTs compared with bipolar junction transistors and thyristors is the MOS gate structure.[98] The author and the National Institute of Advanced Industrial Science and Technology (AIST) group investigated both n-channel and p-channel SiC IGBTs and found that the performance of n-channel SiC IGBTs is much better than that of p-channel SiC IGBTs.[99] In n-channel IGBTs, a long carrier lifetime in the lightly-doped "n-type" voltage-blocking layer is required, whereas a long lifetime in the lightly-doped "p-type" layer is important in p-channel IGBTs. In SiC, the lifetime in the p-type material is considerably shorter than that in the n-type material even after the carbon vacancy elimination, the reason for which is still unclear.[100] Thus, the on-resistance of n-channel SiC IGBTs is always lower than that of p-channel SiC IGBTs. In the fabrication of n-channel SiC IGBTs, the bottom p-type collector region was formed by thick and heavily-doped epitaxial growth on an n-type SiC substrate and the subsequent removal of the substrate,[101] because heavily-doped (low-resistivity) p-type SiC wafers are not available. Although other fabrication processes for SiC IGBTs are similar to those of SiC power MOSFETs, the IGBT structure was carefully optimized through device simulations taking into account the injection of excess carriers at the collector junction and the carrier profile inside the very thick voltage-blocking region.[102] Figure 23 demonstrates (a) the on-state and (b) blocking

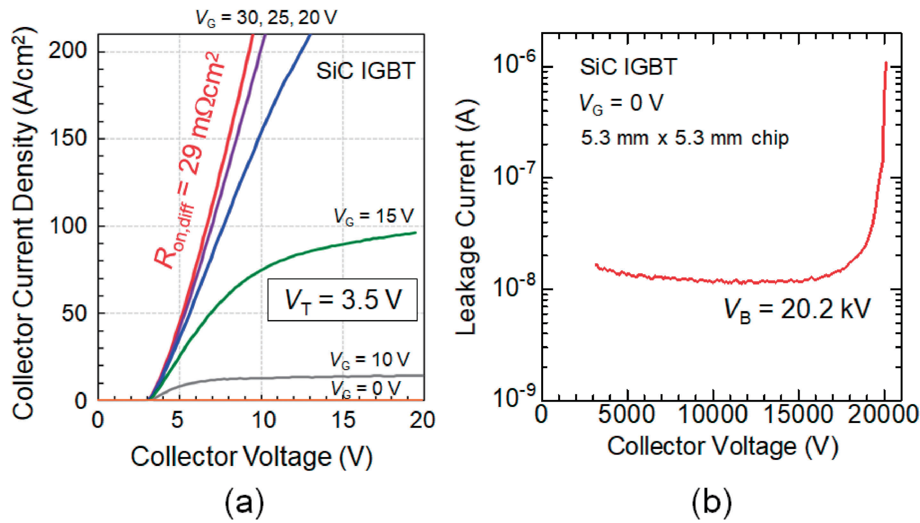

Fig. 23. (a) On-state and (b) blocking characteristics of a fabricated SiC n-channel IGBT.[63),96)] In this IGBT, the n-type voltage-blocking region was 220 µm thick and doped to $4 \times 10^{14}\,cm^{-3}$ (nitrogen), and the gate oxide thickness was 83 nm. (Reproduced from Ref. 63.)

characteristics of a fabricated n-channel SiC IGBT with a chip size of 5.3 mm × 5.3 mm.[63),96)] In this IGBT, the n-type voltage-blocking region was 220 µm thick and doped to $4 \times 10^{14}\,cm^{-3}$ (nitrogen), and the gate oxide thickness was 83 nm. A high current density of $100\,A/cm^2$ was attained at a collector voltage of 6.8 V (gate voltage: 30 V), and the differential on-resistance at $100\,A/cm^2$ was $29\,m\Omega cm^2$. This on-resistance is considerably lower than the unipolar resistance (about $310\,m\Omega cm^2$) of the lightly-doped voltage-blocking region, indicating the effect of minority carrier injection. In the blocking characteristics, the leakage current of the present IGBT was very low, 15 nA at 15 kV (gate voltage: 0 V), and a very high breakdown voltage of 20.2 kV was achieved. This performance (20.2 kV–$29\,m\Omega cm^2$) is one of the best among ultrahigh-voltage semiconductor transistors reported in the literature.[95),103)]

6. Applications of SiC power devices

Through rapid progress in SiC material and device technologies, SiC devices are now the most mature among wide bandgap semiconductor power devices, due to their high performance and reliability. Figure 24 schematically shows the major application ranges in terms of the device blocking voltage for Si, SiC, GaN, and Ga_2O_3 power switching devices (diodes are not shown). Regarding Si power devices, power MOSFETs are mainly adopted in the blocking voltage range below about 800 V, whereas IGBTs are used in the voltage range higher than 600 V.[28)] Si

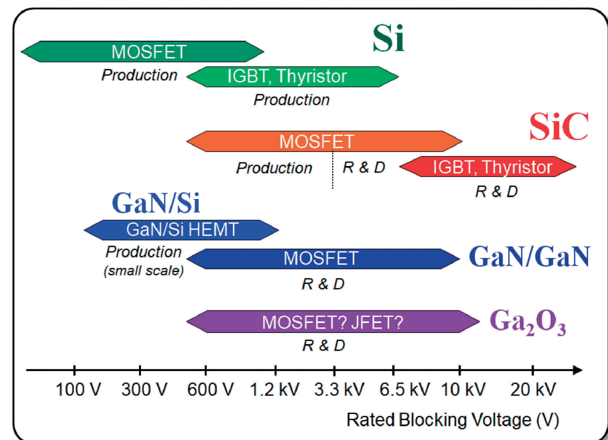

Fig. 24. Major application ranges in terms of the device blocking voltage for Si, SiC, GaN and Ga_2O_3 power switching devices.

thyristors are mostly employed in the very high-voltage range (>5 kV). It is expected that SiC power MOSFETs will replace Si devices in the blocking voltage range from 600 to 6500 V owing to their low on-resistance and fast switching. Below 500 V, however, it will be difficult for SiC devices to compete with Si, because Si power MOSFETs in this low voltage range show high performance and are quite often integrated with gate drive circuits and sensors. SiC IGBTs are promising in the very high blocking voltage range above 5–8 kV.

On the other hand, lateral GaN high-electron-mobility transistors (HEMTs) have been extensively

developed in the blocking voltage range from 300 to 900 V.[11),104)] The major features of lateral GaN HEMTs include very low on-resistance owing to high electron mobility and high sheet carrier density at the AlGaN/GaN interface and very fast switching characteristics owing to small parasitic capacitances originating from the lateral device structure. However, AlGaN/GaN HEMTs have certain limitations in high-voltage and high-current operation because of their lateral structure. Therefore, SiC power MOSFETs and AlGaN/GaN HEMTs possess individual advantages and will find the major applications in different fields. Roughly speaking, SiC power MOSFETs are used for high-voltage and high-current applications, while AlGaN/GaN HEMTs are used for relatively low-voltage and low-current (and fast switching) applications. Vertical GaN power devices fabricated on GaN wafers[105)] and vertical Ga_2O_3 power devices[14),106)] have been emerging, and they will compete with SiC devices in the blocking voltage range from 600 to 6500 V in the future.

The global market volume of power devices was about 18 billion U.S. dollars in 2019, and low-voltage (<300 V) and medium-voltage (300–1700 V) devices account for about 45% and 40% of the total volume, respectively.[107)] For sustainable development of the modern society, production of electric vehicles (EVs) is rapidly growing and the battery voltage of EVs is trending upwards. Furthermore, the growth of solar and wind power plants is also remarkable. Since 600–1200 V devices are key components in these applications, it is predicted that the market for 600–1200 V devices will increase more significantly than the total market for power devices. SiC and other wide bandgap semiconductor power devices are expected to outcompete Si counterparts in such applications. On the other hand, almost no ultrahigh-voltage (>10 kV) devices are being produced at present, because it is extremely difficult to fabricate them with Si. However, the development of advanced electric power infrastructure will require numerous 13–15 kV devices in the future, as these devices will be the cores for constructing solid-state (electronic) transformers and fault isolation systems used for future smart grid technologies.[108)]

The mass production of SiC SBDs[109)] and power MOSFETs[110),111)] started in 2001 and 2010, respectively. An initial application of 600 V SiC power devices was switching-mode power supplies for high-performance workstations and servers. Thanks to the low switching loss of SiC devices, the switching frequency can be increased by 50% or higher, by which smaller passive components (inductors and capacitors) can be used, leading to size reduction of power supplies with higher efficiency. Photovoltaic power conditioners are another major application of 600–1200 V SiC power MOSFETs, where the on-state loss is much reduced (20–75%) by using SiC, resulting in a higher conversion efficiency. Other applications include fast battery chargers, air conditioners, motor control for industrial robots, elevators, and induction heating systems, all of which show significant loss reduction by using SiC. SiC devices are also used for high-specification audio amplifiers. Honda and Tesla have announced the installation of SiC power devices into the main motor control of fuel cell vehicles in 2016 and electric vehicles in 2018, respectively. Toyota has adopted SiC power MOSFETs and SBDs in boost converters for a new model of fuel cell vehicles in 2020 and demonstrated a 70% reduction of power loss in the converters. Since 2014, 3.3 kV (partly 1.7 kV) SiC devices have been used in railcar systems mainly in Japan. In the Tokyo Metro, the JR Yamanote-line, and many others, the range of regenerative braking operation can be significantly expanded by using SiC devices, leading to about 30% power reduction in the train drive.[112)] Since July 2020, the new model "Shinkansen N700S" has been driven by 3.3 kV SiC power modules, which reduce the power loss, converter size, and railcar weight.[113)] In more recent years, the feasibility of SiC devices for very high-voltage power supplies has been investigated. Size reduction of very high-voltage (>100 kV) power supplies is in high demand for particle accelerators used in ion implantation, electron irradiation, and cancer treatments. Concerning the development and applications of SiC unipolar power devices, see review papers.[114)–116)]

Very high-voltage SiC bipolar devices (IGBTs, thyristors, pin diodes) are not currently being commercially manufactured. The epitaxial growth of very thick and lightly-doped voltage-blocking layers is not well established in the production level, even though very impressive results have been recently reported.[117)] Another concern with SiC bipolar devices is the long-term reliability issue caused by stacking fault expansion during forward biasing of a SiC pn junction.[118)] However, this degradation observed in SiC bipolar devices has been greatly reduced through dislocation engineering in SiC as well as adoption of unique device design.[63)] It is expected that production of very high-voltage SiC bipolar devices will start in the near future.

7. Conclusions

Several important achievements in SiC power devices and material mainly obtained by the author's group were reviewed. Regarding the breakdown phenomena in SiC devices, the impact ionization coefficients of electrons and holes were accurately determined, and their strong anisotropy was discussed taking into account the unique band structure of SiC. The leakage current in heavily-doped ($>2 \times 10^{18}\,\mathrm{cm}^{-3}$) SiC pn junctions can be well reproduced with a phonon-assisted band-to-band tunneling model. Recent progress and an explanation of the importance of channel mobility enhancement in SiC power MOSFETs were presented. Although the characteristics of SiC power MOSFETs (typically $1\,\mathrm{kV}$–$1\,\mathrm{m\Omega cm^2}$) significantly outperform Si power devices, the on-resistance is severely limited by the channel resistance. By excluding thermal oxidation of SiC combined with interface nitridation, a very low interface state density in the mid $10^{10}\,\mathrm{cm^{-2}eV^{-1}}$ was achieved, which gave a two-fold improvement of channel mobility (from 41 to over $80\,\mathrm{cm^2/Vs}$). Fundamental studies on the carrier lifetimes in SiC and ultrahigh-voltage bipolar devices were also presented. The density of carbon vacancy defects in SiC, a primary carrier-lifetime killer, has been reduced from $8 \times 10^{12}\,\mathrm{cm}^{-3}$ to $<2 \times 10^{10}\,\mathrm{cm}^{-3}$ (below the detection limit) over a 200 µm-thick epitaxial layer by the original technology (high-temperature oxidation). By carbon vacancy elimination, the carrier lifetime was markedly enhanced from about 2 µs to over 40 µs. By using fast epitaxial growth of high-purity SiC epitaxial layers, the carrier lifetime enhancement, and the original edge-termination structure, record performances of pin diodes ($13\,\mathrm{kV}$–$1.4\,\mathrm{m\Omega cm^2}$, $27\,\mathrm{kV}$–$9.7\,\mathrm{m\Omega cm^2}$) were achieved. A 23 kV SiC bipolar junction transistor and a 20 kV SiC n-channel IGBT were also demonstrated. In the last section, the current status of mass production, social implementation, and the impacts of SiC power devices were briefly described.

Since SiC device technology has made a rapid progress, not only power devices but also integrated circuits (ICs) are now considered as realistic targets for SiC. Basic studies on SiC-based ICs that can operate under harsh environments such as very high temperature and radiation exposure are now underway.[119)–121)]

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Profile

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