Digital Active Gate Drive System for Silicon Carbide Power MOSFETs

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Abstract

The recent development of silicon carbide (SiC) power devices has opened up a promising future for the field of power electronics. The utilization of their superior physical potential is the key to achieving improved performance of already-existing applications and also opening up new fields of application with an increased power density. On the other hand, SiC power devices still face challenges that need to be addressed before fulfilling their potential. Their fast switching speed induces large surge voltages and ringings, raising reliability issues related to electromagnetic interference. The peculiar considerations of SiC power devices, including the variation of the device characteristics and the long-term reliability, causes deviation from the ideal condition and lose the designed performance of power converters. Active gate drive (AGD) technique has gathered attention as one of the key techniques to overcome these issues and realize the fast and high-frequency switching operation of SiC power MOSFETs (metal-oxide-semiconductor field-effect transistors). However, the increasing complexity in the circuit design makes it hard to have an optimized operation without expert know-hows or considerable design efforts, indicating the limitation of the analog approach.

This dissertation develops the digital active gate drive system for SiC power MOSFETs. The transformation of gate drive design from analog adjustment to digital optimization realizes a versatile computer-aided handling of the switching behavior of SiC MOSFETs, eliminating the individual design process of gate drivers considering the device characteristics and other requirements. For the utilization of superior device characteristics of SiC MOSFETs, the AGD technique is introduced as its core. The contribution of this dissertation is summarized as follows.

Firstly, the hardware of the digital active gate driver (DAGD) is developed. Its fundamental concept is realized by applying the architecture and operation of the digital-to-analog converter into the gate drive circuit. The prototype of DAGD is designed, confirming the fundamental operation to shape the gate voltage waveform of SiC MOSFET using

a multi-bit gate signal sequence. It is experimentally shown that the transient switching behavior of the SiC MOSFET can be manipulated via the operating points corresponding to the designated gate voltage levels. It is also verified that the switching characteristics, evaluated by the amount of overshoots and switching loss, can be improved. Additionally, another hardware configuration of DAGD is designed using modular topology to achieve advanced features of controlling both the dynamic and the static behavior of the power devices during the switching operation. These hardwares of DAGD enable the individual adjustment of switching behavior for each SiC MOSFET via the gate voltage waveform.

Secondly, the software to optimize the operation of DAGD is developed. The development of DAGD hardware realizes a combinatorial optimization of the switching behavior of SiC MOSFETs. A metaheuristics-based optimization software is developed to obtain a set of optimum AGD patterns for a given power device and operating condition. The system is verified both in the simulation and in the experiment, successfully obtaining the set of optimum gate signal sequences, which clarifies the effectiveness of the designated AGD patterns on the switching characteristics. In addition to these initial optimization schemes, the deviation from the initial condition is also investigated. An updating scheme of the software is developed to maintain the performance of AGD in the presence of uncertain changes in the condition.

Thirdly, its advantage in the applications is discussed. It is demonstrated that the individual shaping of gate voltage waveform realizes a versatile switching operation regardless of the device characteristics or the operating conditions. The imbalance of current-sharing in the parallel operation of SiC MOSFETs can be mitigated by the adoption of unique AGD patterns, which considers the inherent difference in the device parameters or the circuit layout. Furthermore, the shift of device characteristics after the circuit implementation is also addressed, showing that the original performance of AGD is regained by the updating of the AGD pattern.

Finally, the developed digital active gate drive system, which consists of the core elements of the hardware and the software, is organized and visualized. It provides solutions to the challenges regarding the practical applications of SiC MOSFETs, clarifying the system requirements for particular issues addressed in the dissertation.

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Contents

Notations and acronyms

Notations

Notation	Usage	Meaning
$\mathbb{Z}$		Set of integer numbers
$\in$	$a \in A$	a is an element of A
$\bar{\cdot}$	$\overline{b}$	Negation of b (Boolean operator)
$\dfrac{\mathrm{d}}{\mathrm{d}t}$	$\dfrac{\mathrm{d}\boldsymbol{x}}{\mathrm{d}t}$	Time derivative of $\boldsymbol{x}$

Acronyms

Acronym	Meaning
AC	Alternate Current
ADC	Analog-Digital Converter
AGD	Active Gate Driver
DAC	Digital-Analog Converter
DAGD	Digital Active Gate Driver
DC	Direct Current
DSP	Digital Signal Processor
DUT	Device Under Test
FET	Field-Effect Transistor

FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
JFET	Junction Field-Effect Transistor
LDO	Low-drop-out
MMDAGD	Modular-Multilevel Digital Active Gate Driver
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SBD	Schottky Barrier Diode
Si	Silicon
SiC	Silicon Carbide
SoC	System-on-Chip

Symbols

Symbol	Meaning
V_{GS}	Gate-source voltage
V_{DS}	Drain-source voltage
I_{D}	Drain current
I_{G}	Gate current
V_{th}	Gate threshold voltage
V_{plateau}	Gate plateau voltage
R_{on}	Drain-source on-resistance

Chapter 1

Introduction

Power electronics constitutes an essential element of our modern society. Its applications range from low voltage to high voltage in a variety of fields where electric power is processed, such as power supplies for information devices, home appliances, motor drives for vehicles and trains, and converters for grid connections. The flourishing development of this field has been supported by the continuous advancement in the technology of power devices, which are semiconductor switching devices that enable the switched-mode operation of power conversion circuits [1, 2]. To this day, various kinds of silicon-based power devices have been developed and utilized, such as power metal-oxide-semiconductor field-effect transistors (MOSFETs), gate-turnoff thyristors, and insulated-gate bipolar transistors (IGBTs) [1, 3, 4]. Unlike logic semiconductor devices, power semiconductor devices require a larger amount of power and, depending on the device, a higher voltage level to operate themselves. These requirements necessitate the gate drive circuits, which interface the logic-level signal region and the power-processing region.

In recent years, the field of power electronics has witnessed a revolutionary change following the introduction of wide-bandgap (WBG) semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), into power devices [5–10]. They exhibit superior physical properties for power device application over silicon, represented by the lower on-resistance, higher breakdown electric field strength, faster switching speed, and higher thermal conductivity [7,8,11,12]. Table 1.1 shows the main physical properties of Si, SiC, and GaN for vertical power devices at room temperature [5, 11, 13, 14]. They can achieve higher efficiency by replacing the Si-based power devices in the existing power electronics applications. More importantly, these devices are expected to open up new fields of applications with an increased power density that Si-based power devices would not be able

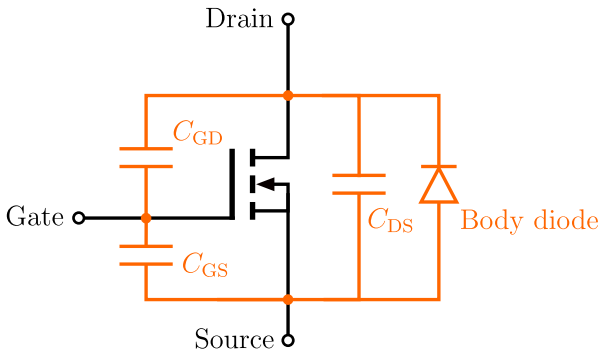
Table 1.1: Material properties of Si, 4H-SiC, and GaN at room temperature [5,11,13,14].

	Si	SiC	GaN
Bandgap [eV]	1.12	3.26	3.42
Breakdown electric field [MV/cm]	0.3	2.8	2.8–3.0
Electron saturation velocity [cm/s]	1×10^7	2.2×10^7	2.7×10^7
Thermal conductivity [W/cmK]	1.5	4.9	2.0

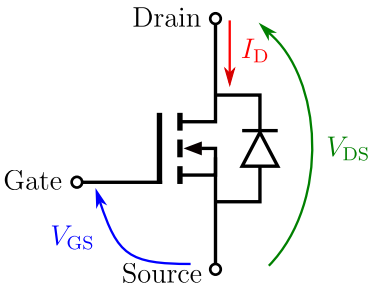
to achieve [7, 15]. Their installation to power electronics applications is rapidly ongoing, supported by the emerging and growing markets including electric vehicles, photovoltaic and wind power plants, and data center power supplies [7, 16].

On the other hand of the advantages, SiC power devices face peculiar challenges that need to be addressed before fulfilling their potential []. One of the major concerns is the increased level of overshoot and ringing caused by the fast and high-frequency switching [17]. They lose the reliability of the power device, increase the problems related to the electromagnetic interference (EMI), and can even cause fatal false-turn-on phenomenon [7, 18, 19]. The variation of device parameters is another challenge for SiC devices. These mismatched device parameters are particularly troublesome when SiC MOSFETs are connected in series or parallel, as they cause a serious imbalance of electrical and thermal stresses [7, 20, 21]. For the full utilization of the superior material potential of SiC power devices without compromising with the drawbacks, innovations are required in peripheral technologies along with the improvement of the power devices themselves. Particularly, the gate drivers are considered one of the most critical technologies as they directly control their switching behaviors [7, 18].

This dissertation investigates the digitization of the gate drive circuit for SiC MOSFETs. The transformation of gate drive design from analog adjustment to digital optimization realizes a versatile computer-aided handling of the switching behavior of SiC MOSFETs, eliminating the individual design process of gate drivers considering the device characteristics and other requirements. For the utilization of superior physical characteristics of SiC devices, the active gate drive (AGD) technique is introduced as the core [19,22]. The digital active gate drive system is developed consisting of three aspects: hardware, software, and applications. The rest of this chapter reviews the detailed background of this research. Section 1.1 reviews the fundamentals of gate drive circuits for power MOSFETs, addressing the challenges regarding the gate drive of SiC power MOSFETs. Section 1.2 reviews the AGDs in the literature from the aspects of configuration and optimization,



(a) Equivalent circuit considering internal capacitances and body diode.



(b) Definition of V_{GS}, V_{DS}, and I_D.

Figure 1.1: Schematic representation of MOSFET.

where the potential benefit of digitized gate drivers is discussed. Section 1.3 gives the overview of the thesis.

1.1 Operation of power MOSFETs

This section provides a fundamental understanding of the operation of power MOSFETs, as well as the basic roles and features of gate drivers. The peculiar considerations in the gate driving of SiC MOSFETs are addressed.

1.1.1 Gate driving of MOSFET

The MOSFET is a voltage-controlled unipolar switching device having three electrodes: gate (G), drain (D), and source (S). Figure 1.1 (a) shows the equivalent circuit of MOSFET. It has internal capacitances between each pair of electrodes, namely the gate-source capacitance (C_{GS}), the gate-drain capacitance (C_{GD}), and the drain-source capacitance (C_{DS}). Additionally, the body of the MOSFET forms a parasitic diode known as the body diode. Figure 1.1 (b) shows the definition of the voltages and currents that describe the operation of the MOSFET. The gate-source voltage (V_{GS}) is defined as the voltage between the gate and the source, and the drain-source voltage (V_{DS}) is defined as the voltage between the drain and the source. The drain current (I_D) is defined as the current that flows into the drain electrode.

The operation of MOSFET is governed by V_{GS}, as it sets the bias state of the MOS structure to control the formation of the channel (inversion layer) [1, 11]. The gate drive

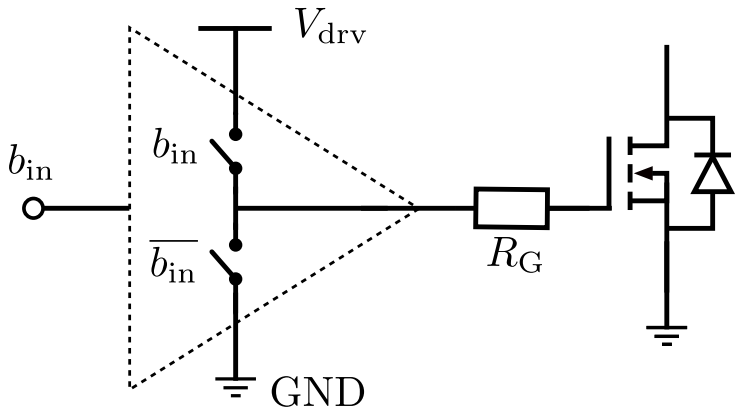


Figure 1.2: Basic configuration of gate drive circuit for power MOSFET. b_{in} denotes the input logic signal, V_{drv} denotes the positive DC voltage required to drive the MOSFET, and R_{G} denotes the external gate resistor.

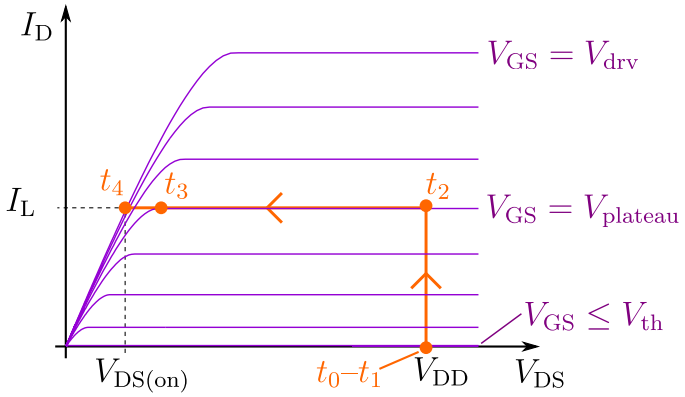
circuit, or simply the gate driver, is used to charge and discharge the gate capacitances to turn the MOSFET on and off. Figure 1.2 shows the most basic configuration of the gate driver for MOSFET. It has the push-pull switches to apply the positive driving voltage (V_{drv}) or the ground to V_{GS}, according to the input logic signal (b_{in}). An external gate resistor (R_{G}) is usually inserted between the push-pull stage and the gate of the MOSFET to adjust the time constant of the gate charging.

1.1.2 Switching operation of MOSFET

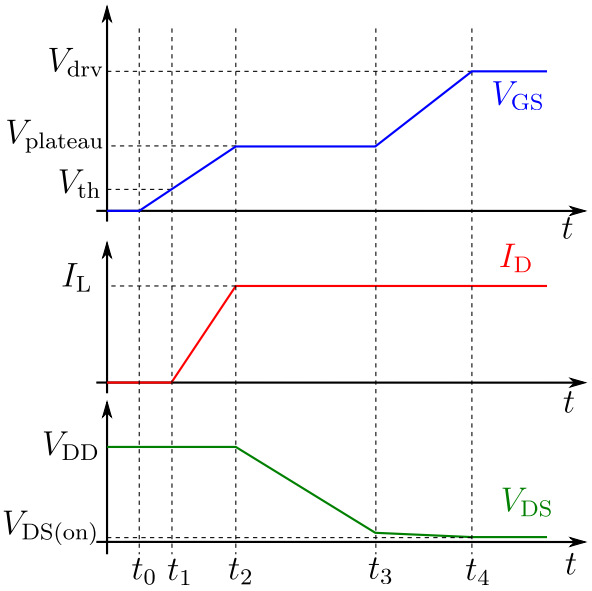
The transient switching behavior of the MOSFET is described [1,11,23,24]. We assume a MOSFET is applied to a switching test circuit with an inductive load, where the blocking voltage of V_{DD} [V] and the load current of I_{L} [A] are supplied. We also assume the *square-law characteristics* for I_{D}, which is not a numerically precise expression for SiC power MOSFETs but helps us to grasp the fundamental operation of MOSFETs [11].

Figure 1.3 shows the simplified waveforms of V_{GS}, V_{DS}, and I_{D} at the turn-on. The turn-on process begins at t_0 by applying a positive step-wise voltage between the gate and source terminals. At t_1, when V_{GS} exceeds a certain value, I_{D} begins to flow due to the formation of the channel. This V_{GS} level is called the threshold voltage (V_{th}). After t_1, the MOSFET is in the saturation region, where the rise of V_{GS} increases I_{D}, while V_{DS} is kept at the same value. A simplified expression of I_{D} during this period is given by Eq. (1.1).

$$I_{\mathrm{D}} \sim \mu_{\mathrm{N}}^{*} C_{\mathrm{OX}} \frac{W}{2L} (V_{\mathrm{GS}} - V_{\mathrm{th}})^2 \tag{1.1}$$



(a) Drain characteristics of MOSFET and transition of switching trajectory.



(b) Simplified switching waveforms of V_{GS}, V_{DS}, and I_D.

Figure 1.3: Simplified switching behavior of MOSFET at turn-on transient.

Here, C_{OX} denotes the capacitance per unit area of the oxide, W and L denote the width and length of the channel, respectively, and μ_N^* denotes the electron mobility of the inversion layer, all of which are parts of the device parameters of the MOSFET.

I_D reaches the load current I_L at t_2. After that, V_{DS} decreases while V_{GS} and I_D are kept almost at the same value. This is due to the Miller effect; almost all of the gate current flowing to the gate terminal is used to charge the gate-drain capacitance C_{GD} as V_{DS} decreases. The V_{GS} level at which this phenomenon occurs is called the gate plateau voltage ($V_{plateau}$), which is derived from Eq. (1.1) and given by Eq. (1.2).

$$V_{\text{plateau}} = V_{\text{th}} + \sqrt{\frac{2I_{\text{L}}L}{\mu_{\text{N}}^{*}C_{\text{OX}}W}} \tag{1.2}$$

At t_3, as V_{DS} equals $V_{\text{GS}} - V_{\text{th}}$, the MOSFET enters the quasi-linear region, and V_{GS} starts to increase again. Finally, V_{GS} reaches the driving voltage V_{drv} at t_4, which completes the turn-on procedure. The turn-off procedure is explained by following the transition in the opposite direction.

When the MOSFET is completely turned on, V_{DS} and I_{D} have a relationship expressed by Eq. (1.3), where R_{on} denotes the drain-source on-resistance.

$$I_{\text{L}} = \frac{1}{R_{\text{on}}} V_{\text{DS(on)}} \tag{1.3}$$

R_{on} is expressed as the sum of several resistances existing in the structure of power MOSFET, including the channel resistance, drift resistance, and substrate resistance. For the widely commercialized SiC MOSFETs with a blocking voltage of 1200 V or less, the channel resistance (R_{ch}) is the most dominant element of the total R_{on} [25]. The channel resistance is given by Eq. (1.4).

$$R_{\text{ch}} = \frac{L}{\mu_{\text{N}}^{*}C_{\text{OX}}W(V_{\text{GS}} - V_{\text{th}})} \tag{1.4}$$

1.1.3 Challenges regarding gate driving of SiC MOSFETs

SiC MOSFETs pose several considerations regarding its gate drive circuit. The realization of fast switching is of most importance to enjoy the superior physical potential of SiC MOSFET, enabling low switching loss and higher switching frequency operation. On the other hand, the large $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}i/\mathrm{dt}$ caused by the fast switching can couple with the non-ideal components in the circuit, such as stray inductance of the power loop and parasitic capacitances within the electronic components or arising from the circuit layout [17, 26, 27]. They result in large overshoots of V_{DS} or I_{D}, which can exceed the rated operation range and damage the SiC MOSFET itself or other components [8, 17, 28]. The large overshoot also contributes to the increased ringing, which adds to the EMI and raises reliability concerns, including the false-turn-on phenomenon [7, 18, 19, 29].

The simplest approach to limit the switching speed is the use of a large gate resistor (R_{G}). Figure 1.4 shows an example of the switching waveforms of a SiC MOSFET full-bridge circuit with different values of gate resistance, which confirms that a smaller

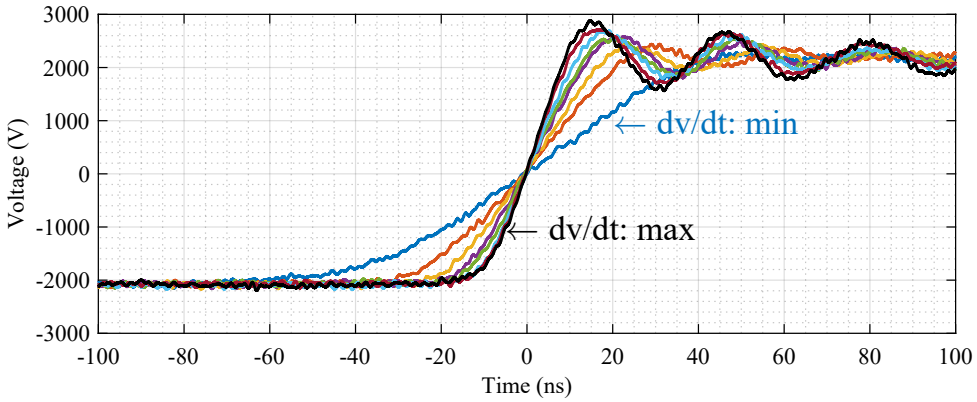


Figure 1.4: Example of output voltage waveforms of SiC MOSFET full-bridge with different values of R_G ranging from 5 Ω (dv/dt: maximum) to 40 Ω (dv/dt: minimum). © 2023 IEEE.

dv/dt with a smaller voltage overshoot is achieved by applying larger R_G [30]. However, the decreased switching speed, in turn, significantly increases the switching loss [28]. This trade-off needs to be carefully addressed in each design of power electronics application. Another conventional solution is the application of external circuits, such as passive snubber circuits or filtering circuits [31–33]. However, they inevitably increase the overall circuit volume and the total loss as a converter, which diminishes the advantage of WBG devices [32, 34].

Another peculiar challenge that SiC MOSFETs have been facing to date is the variation of device parameters [18, 35]. Figure 1.5 shows the measurement results of I_D–V_{GS} characteristics of eleven SiC MOSFETs of the same model number, which were picked up randomly from laboratory stock. The variation of V_{th} is present, as the value is distributed within the range of about 0.8 V. In addition to the inherent variations, the device parameters can change in the long run as a consequence of mechanical or electronic stress, partly depending on the operating conditions and gate bias conditions. While the detailed origin and dynamics of the cause of V_{th} instability are actively under research, literature does indicate that the defects and their trapped electrons in the oxide and the interface states at the oxide-semiconductor interface contribute to those variations [25, 36–38].

The variations in device parameters affect the switching operation of SiC MOSFETs. The shift of V_{th} itself moves the timing of switching operations, as can be understood from Fig. 1.3. It also affects some of the related device parameters, such as $V_{plateau}$ and R_{on}, as understood from Eq. (1.2) and Eq. (1.4), respectively. The mismatch of V_{th} and R_{on}

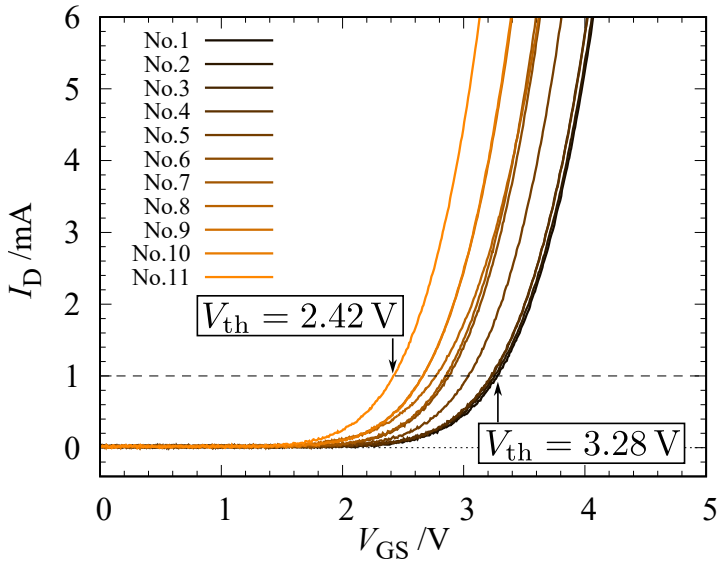


Figure 1.5: I_D–V_{GS} characteristics of several SiC MOSFETs of the same model measured at $V_{DS} = 10\,V$ and at room temperature. Measurement was done using a semiconductor curve tracer (custom-made product, IWATSU Electric Co, Ltd.). V_{th} is defined here as V_{GS} level at which I_D reaches 1.0 mA.

is particularly troublesome in applications where several SiC MOSFETs are connected in parallel or series as they cause a severe imbalance of current or voltage shared among the devices, leading to the breakdown or imbalanced electric stress on the power device itself and other peripheral components [20, 21, 39–41].

1.2 Active gate drive of SiC MOSFETs

To overcome the limitation in the basic configuration of gate drivers, improved configurations and features of gate drivers have been investigated for voltage-controlled power devices. They are, in general, called the active gate drivers (AGDs). This section discusses the basics of AGDs and reviews the related techniques presented in the literature, clarifying the advantages of digitization.

1.2.1 Overview of active gate drive

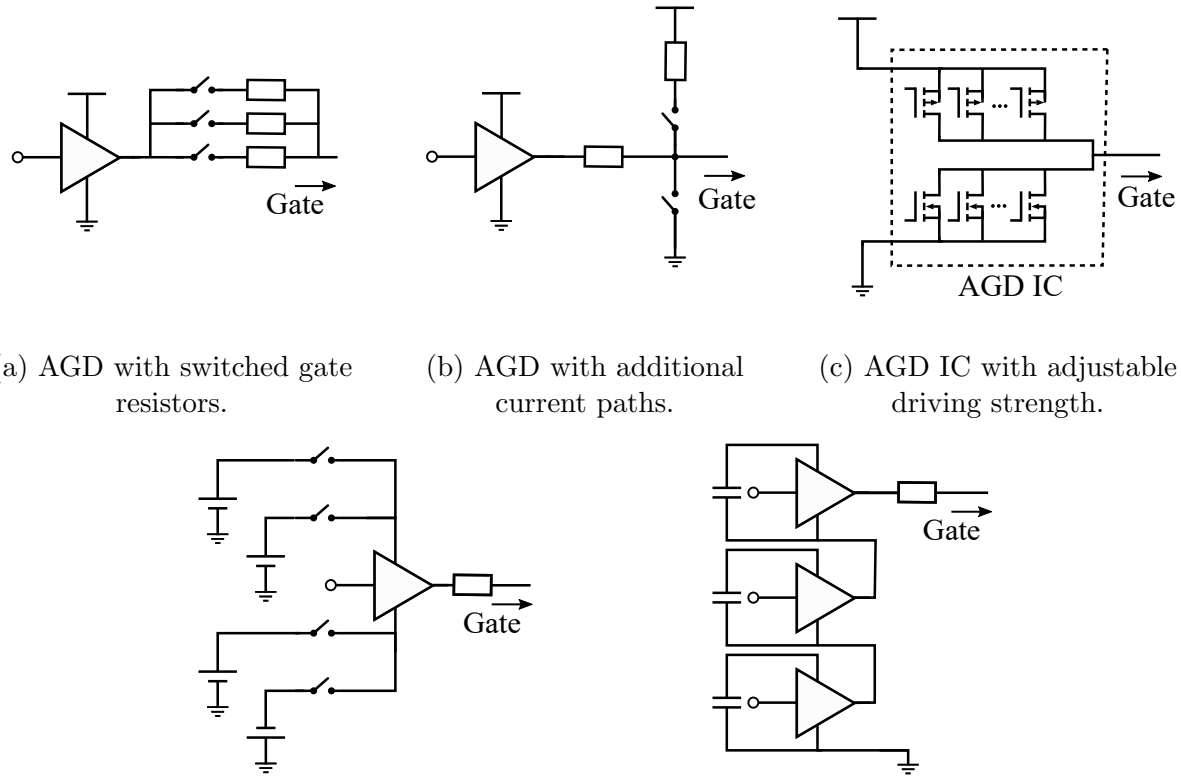
The fundamental objective of AGD is to control the transient switching behavior of the power devices. The limitation of the basic gate driver, as shown in 1.2, is that it can only

apply the binary state of either on or off to the power device. The dynamics of the switching transient between the two states is totally determined by the device characteristics of the power MOSFET and the passive components in the gate drive circuit. In AGD, on the other hand, several active mechanisms or components are added to the gate drive circuit to adjust the switching speed of the power devices actively during the switching transient [19, 22]. This idea had already been proposed in the 1990's to utilize Si IGBTs efficiently without using snubber circuits [31, 42–45]. Since the advent of WBG power devices, AGD has gained increasing attention as a promising technique to achieve better handling of their fast switching transient [19, 22, 32, 46, 47].

There exist several approaches to modifying the basic gate drive circuit to realize the AGD operation. The AGD topologies presented in the literature can be roughly classified into three types, namely the resistor-controlled AGDs [32, 47–49], the current-controlled AGDs [31, 42, 50–54], and the voltage-controlled AGDs [34, 45, 55–62]. Figure 1.6 shows some of the examples of the AGD topologies. The resistor-controlled AGDs are equipped with several gate resistors that are switched during the switching transient [32,47–49]. The current-controlled AGDs are realized by using additional current paths to boost the gate charge [31,42], by using inductive components [63], or by adjusting the driving strength of the switching devices inside the gate driver IC [50, 52, 53]. The voltage-controlled AGDs apply multiple voltage levels consecutively during the switching transient by using voltage amplifiers [55], by switching between multiple DC sources [56,64,65], or by using modular-multilevel configuration [34, 62]. They have demonstrated superior trade-offs between the overshoot of voltage or current and the switching loss compared to the conventional method, such as the use of large gate resistors and snubber circuits [32,33]. AGD has also shown promising potential for improved balancing of current or voltage across parallel-connected or series-connected SiC MOSFETs [59, 66–68].

1.2.2 Optimization and digitization

AGD requires additional signals to control the auxiliary switches inside the gate drive circuit. In the relatively slow switching of IGBTs, the real-time analog feedback of device voltage or current is employed for generating the signals for the auxiliary switches within the switching transient [42,45]. This approach becomes challenging as the switching speed gets faster, especially for WBG devices with tens of ns of switching time. For this reason, most AGDs employ several additional gate signals with different delays and widths to



(a) AGD with switched gate resistors.

(b) AGD with additional current paths.

(c) AGD IC with adjustable driving strength.

(d) AGD with multiple DC sources.

(e) AGD with modular-multilevel topology.

Figure 1.6: Examples of AGD topologies.

control those auxiliary switches individually [19,56]. One of the enabling factors for them is the availability of advanced digital controllers, such as digital signal processors (DSPs) and field-programmable gate arrays (FPGAs). The clock frequency of hundreds of MHz or more makes it possible to output multi-channel high-resolution gate signals to precisely adjust the switching behavior of the power devices within the short switching period.

The operation of AGDs must be designed properly to obtain the expected performance. Several approaches have been investigated in the literature for optimizing the parameters for shaping the AGD waveform, including the timing to operate the auxiliary switches and the values of the resistance, current, or voltage that are applied during the active operation. In the analog approach, those parameters are calculated by a model to describe the switching behavior of the power devices [32,56,69], which requires prior identification of the relevant device parameters. They are designed to be significantly effective in a particular condition and for a specific device. However, such an increased complexity in

the circuit design and parameter tuning require a considerable design effort with expert knowledge and experience. Besides, as the optimum operation is only guaranteed in the condition supposed in the design process, it is hard to adjust the operation flexibly, especially when the conditions can change. To have flexibility against potentially changing conditions, the reconfigurability and versatility of the AGD operation would be the key requirement for the AGD hardware. The digitization of the AGD is a promising way to achieve this, where its operation could be totally optimized by the signal adjustment using the software without adjusting the hardware itself [70, 71]. This means that the application-specific analog design, which relies on the know-how of the individuals and the time-consuming try-and-error process, can be replaced by general optimization methods utilizing the advanced resources of the digital controllers and processors. The hardware of digital AGD to realize the versatile gate driving of SiC MOSFETs needs to be investigated, as well as the software to fulfill their potential.

1.3 Outline of the dissertation

This dissertation develops the digital active gate drive system for SiC power MOSFETs. The core elements of the system, including the hardware and the software, are proposed and developed. Several experimental results confirm the advantages of the system in several applications where SiC MOSFETs face practical challenges. The hardware for the DAGD system is firstly developed in Chapter 2 to perform AGD operations using the concept of the digital-analog converter (DAC). After verifying its fundamental function, the software to optimize the DAGD sequence is constructed in Chapter 3, clarifying the system-level advantage of DAGD. Chapters 4 and 5 target the applicability of the DAGD system to deal with obstacles in the practical application of SiC MOSFETs. Chapter 4 investigates the application to parallel operation of SiC MOSFETs for improving the current-sharing performance. Modular-structure DAGD is developed as a new hardware to provide additional features. Chapter 5 discusses the necessity to re-adjust the pre-optimized AGD pattern during the operation of power converters in response to the uncertain changes in the condition, such as the aging of SiC MOSFETs. A software updating scheme is developed to maintain the performance of AGD against uncertain changes. Finally, Chapter 6 concludes the contributions and provides future directions. The rest of this section gives an overview of each chapter in this dissertation.

Chapter 2 develops the concept and hardware of DAGD. The DAC architecture is introduced to AGD for the digital shaping of V_{GS} waveform. The prototype of DAGD is designed and fabricated based on the configuration of the binary-weighted resistor DAC, which generates the gate-source voltage waveform of the MOSFET directly and flexibly by a multi-bit gate signal sequence. The operation of DAGD is investigated by focusing on the switching trajectory on the state space of the device, which is discretely controlled through successive transitions between operating points. Experimental and simulated results confirm that the proposed gate driver can effectively suppress and regulate the surge voltage and ringing during turn-off. Based on the confirmed operation, an improved configuration of DAGD is presented using GaN HEMT as the internal switching device.

Chapter 3 develops an optimization system for the DAGD operation. It is discussed that the increasing complexity in the circuit design of AGDs makes it hard to have an optimized operation without expert know-how or considerable design efforts. Taking the benefit of DAGD to adjust its operation using digital bit sequence, a digital-twin-compatible metaheuristic optimization system for AGD sequence is proposed. It offers a totally-digital control of switching characteristics of power devices through genetic-algorithm-based optimization. The optimization system is verified in simulation and experiment by successfully obtaining the optimum Pareto-front solutions in double-pulse switching tests. The optimization is also performed for several different operating conditions and for different SiC MOSFETs, where the trend of optimum gate signal sequences is analyzed.

Chapter 4 investigates the applicability of the DAGD system to the parallel operation of SiC MOSFETs. The issues faced in the parallel operation of SiC MOSFETs are reviewed to clarify the requirements for the DAGD system. An improved configuration of DAGD using modular topology is designed, which provides additional features of the DAGD hardware to coordinate both the dynamic and the static behavior of SiC MOSFETs. It is verified that the proposed gate driver can improve the current-sharing performance of parallel-connected SiC MOSFETs with mismatched device parameters.

Chapter 5 targets the effectiveness of AGD patterns against uncertainties that cause deviation from the initial condition. It is discussed that the performance of the pre-defined optimum AGD pattern, which is evaluated at the initial test condition, is vulnerable to uncertain changes in the device characteristics, including aging. A software-based updating scheme is presented to adjust the AGD pattern in response to unforeseen parametric

changes in an already-mounted power device. A metaheuristics-based search using a previously optimized population helps the fast convergence without knowledge of the factor causing the change. The scheme is experimentally verified using modular DAGD in a boost converter operation, where the shift of the device characteristics is simulated.

Chapter 6 summarises the contributions of this dissertation by combining the findings and achievements of this study into a DAGD system. The remaining challenges and future directions are discussed.

Chapter 2

Design of digital active gate driver

This chapter develops the concept of the digital active gate driver (DAGD) for SiC power MOSFETs. As described in Chapter 1.2, AGD is a technique to shape the gate-source voltage (V_{GS}) waveform of the MOSFET. The architecture of a digital-to-analog converter (DAC) is introduced into the gate drive circuit to overcome the aforementioned limitation of the basic gate driver. The transient V_{GS} waveform is shaped through the successive alteration of the voltage levels by a multi-bit gate signal sequence.

2.1 Conception of digital active gate driver

The concept of the digital active gate driver for SiC power MOSFETs is developed by introducing the DAC architecture into the gate drive circuit. A DAC converts the digital input signals, typically multi-bit, to the analog output signal. The resistor DAC consisting of push-pull switches and resistors, which is one of the most common configurations of DAC, is referenced for its similarity with the topology of gate drive circuits. The detailed design and operation are described in this section.

2.1.1 Circuit design

Figure 2.1 shows the configuration of n-bit digital active gate driver. It is designed according to the architecture of the binary-weighted resistor DAC [72]. The n single gate drive circuits are connected in parallel with the binary-weighted gate resistances of $2^k R\,[\Omega]$ ($k = 0, 1, ..., n-1$). When all the input signals b_0, b_1, ..., b_{n-1} are 1, V_{drv} is applied to V_{GS} to completely turn on the MOSFET. When they are all 0, V_{GS} is pulled down to the ground to turn off the MOSFET. No static current flows through the gate resistors at

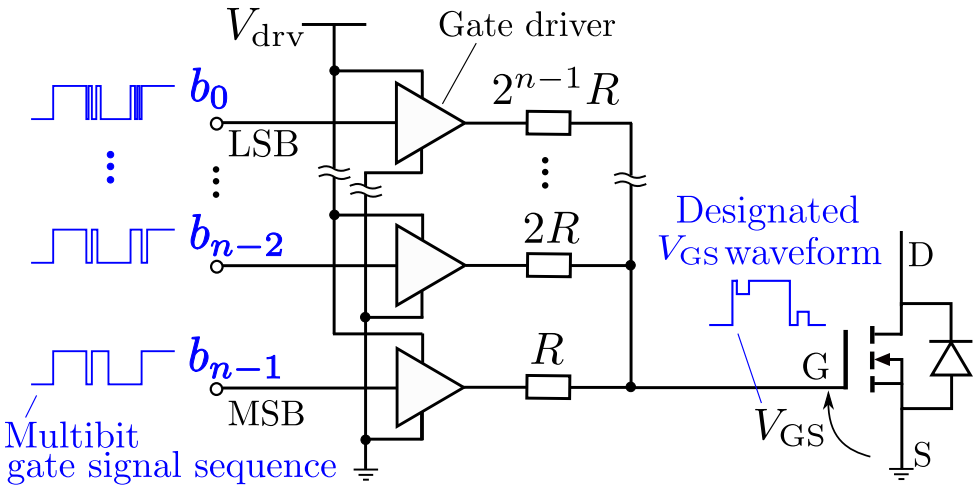


Figure 2.1: Configuration of n-bit digital active gate driver.

these two states. During the transient state of switching, on the other hand, the input signals are successively changed at the clock rate of the controller. They divide the gate input voltage (V_{drv}) by the switched gate resistors to set the value of V_{GS} as given by Eq. (2.1).

$$V_{\mathrm{GS}} = \frac{R_{\mathrm{off}}}{R_{\mathrm{on}} + R_{\mathrm{off}}} V_{\mathrm{drv}} = \frac{\sum_{j=0}^{n-1} b_j 2^j}{\sum_{j=0}^{n-1} 2^j} V_{\mathrm{drv}} \tag{2.1}$$

Here, R_{on} and R_{off} refer to the combined resistances of the gate resistors whose input signals are 1 and 0, respectively. It is also assumed that the gate drivers have no output resistances that affect the calculation of Eq. (2.1). The derivation of Eq. (2.1) is detailed in Appendix A. The desired V_{GS} waveform can be obtained by adjusting the sequence of the multi-bit gate signals.

The flexibility of the shaping depends on the number of bits and the clock rate of the gate signal. As a prototype, 4 bit is examined because of its less complexity in circuit implementation without loss of generality. The proposed driver can set V_{GS} at multiple voltage levels successively during each turn-on/off operation under the given resolution. This gains the flexibility of the gate-driving strategy and generality, which are set apart from the hardware configuration.

2.1.2 Strategies for shaping gate-source voltage waveforms

To investigate effective V_{GS} waveforms to suppress the surge voltage, an understanding of the detailed switching operation is required. An example of the switching waveforms

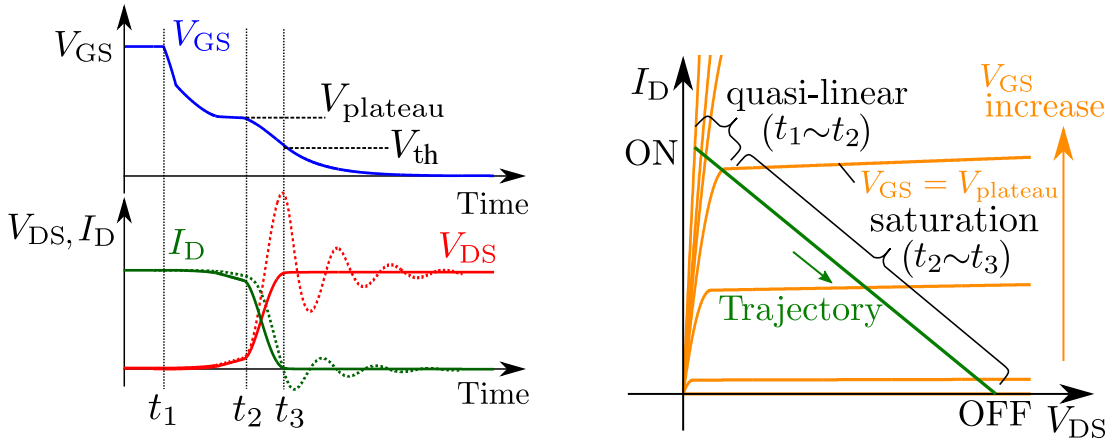
of the MOSFET during turn-off is shown in Fig. 2.2 (a) with solid lines, in which V_{DS} denotes the drain-source voltage and I_{D} the drain current. Here, an ideal resistive load is assumed. The switching trajectory is shown in Fig. 2.2 (b), along with the I_{D}–V_{DS} characteristics for several values of V_{GS}. The turn-off operation begins at t_1 when 0 V is applied to the gate terminal. Then, V_{GS} starts to decrease until it becomes flat at the gate plateau voltage (V_{plateau}). During this period, the MOSFET operates in its quasi-linear region. V_{GS} stays flat until t_2 owing to the Miller effect, where almost only the gate-drain internal capacitor is discharged. At t_2, the MOSFET enters its saturation region, and both I_{D} and V_{DS} start to change rapidly. At t_3, V_{GS} crosses the threshold voltage (V_{th}), and the MOSFET turns off.

In a real circuit, because of the presence of stray inductances, the fast turn-off of the device leads to large surge voltage and ringing, as shown in Fig. 2.2 (a) with dashed lines. They can be suppressed using the active gate drive, as it regulates the large $\mathrm{d}i/\mathrm{d}t$ of the drain current. If we set V_{GS} between V_{plateau} and V_{th} during t_2 and t_3, the switching becomes slow only during the period and the surge voltage is hopefully reduced. This is equivalent to setting operating points on the state space and thereby controlling the switching trajectory discretely, as illustrated in Fig. 2.3. It should be noted that the V_{GS}-shaping strategy depends on the load conditions because the load line is not simply a linear relationship in real applications.

2.1.3 Evaluation method for switching time

The switching time of the MOSFET used to be calculated from the V_{DS} waveform, and indicates how quickly the device can be turned on or off. However, when high-amplitude ringing appears, the output power of the MOSFET does not reach a stable state, making it difficult to specify the end of the switching operation clearly. Instead, the following index is introduced to estimate how long the device is in the transient state during the switching operation. The ON and OFF regions on the I_{D}–V_{DS} plane are used for this definition, which are given by Eq. (2.2).

$$\begin{cases} \text{OFF region} : \left(\dfrac{I_{\mathrm{D}}}{I_{\mathrm{D,on}}}\right)^2 + \left(\dfrac{V_{\mathrm{DS}}}{V_{\mathrm{DS,off}}} - 1\right)^2 \leq 0.2^2 \\ \text{ON region} : \left(\dfrac{I_{\mathrm{D}}}{I_{\mathrm{D,on}}} - 1\right)^2 + \left(\dfrac{V_{\mathrm{DS}}}{V_{\mathrm{DS,off}}}\right)^2 \leq 0.2^2 \end{cases} \tag{2.2}$$



(a) Transient waveforms of V_{GS}, V_{DS}, and I_D.

(b) Switching trajectory and I_D–V_{DS} curves for several values of V_{GS}.

Figure 2.2: Examples of switching waveforms of MOSFET during turn-off, assuming load is an ideal resistor.

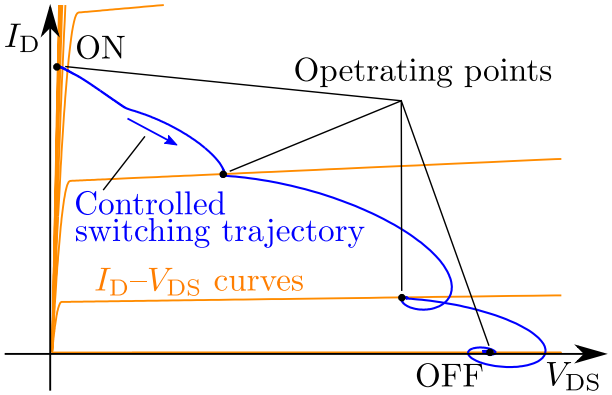


Figure 2.3: Conceptual diagram of switching trajectory control using discrete operating points.

Here, $I_{D,on}$ denotes the value of I_D when the MOSFET is on, and $V_{DS,off}$ that of V_{DS} when the MOSFET is off. We define $t_{tran,off}$ for turn-off and $t_{tran,on}$ for turn-on as the time between the transition from one region to another, until the trajectory converges in the region. With these definitions, as long as the ringing remains, the switching is regarded to be in a transient state and does not converge. This index is particularly relevant to high-frequency switching because the transient state accounts for a large proportion of a switching period.

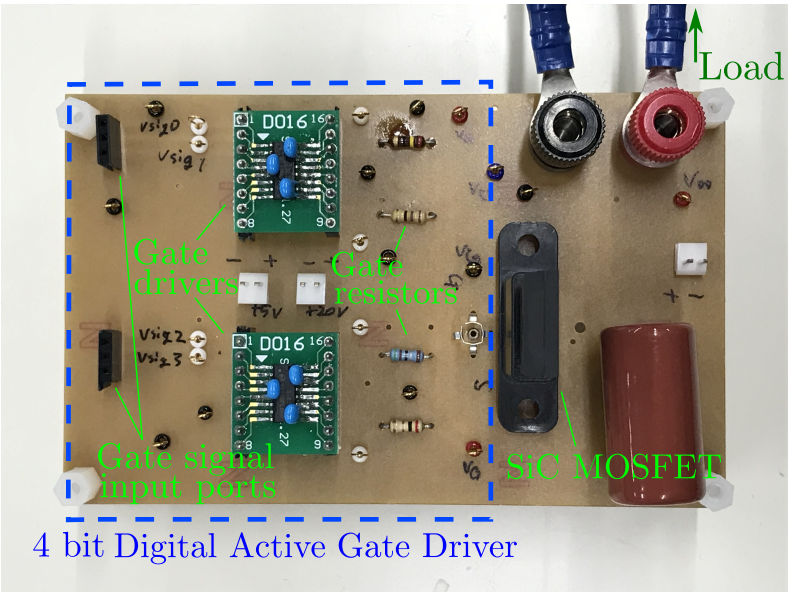


Figure 2.4: Photograph of fabricated circuit.

2.2 Experimental verification

In this section, the operation of the proposed gate driver is verified in the experiment. The prototype of the 4-bit DAGD is fabricated using discrete gate driver ICs. Various V_{GS} waveforms are tested for their effectiveness in suppressing the surge voltage during turn-off without sacrificing the switching time.

2.2.1 Fabrication of prototype DAGD

Figure 2.4 shows the photograph of the digital active gate driver fabricated on a PCB. The schematic diagram of the circuit, including the SiC MOSFET and the switching test circuit, is shown in Fig. 2.5. A commercial isolated gate driver (Si8235, Silicon Labs Inc.) is used as the switch for each bit. Gate resistors are selected considering the output resistances of this driver, which are 2.7 Ω for source operation and 1.0 Ω for sink operation [73]. The gate signals are programmed and generated by an FPGA (sbRIO-9607, National Instruments Corp.) at the clock of 40 MHz. SiC MOSFET (SCT2450KE, ROHM Co., Ltd.) is switched at 50 kHz and 33 V is supplied. The load is composed of a resistor of 33 Ω and wires, which have a large stray inductance that contributes to the large surge voltage during turn-off.

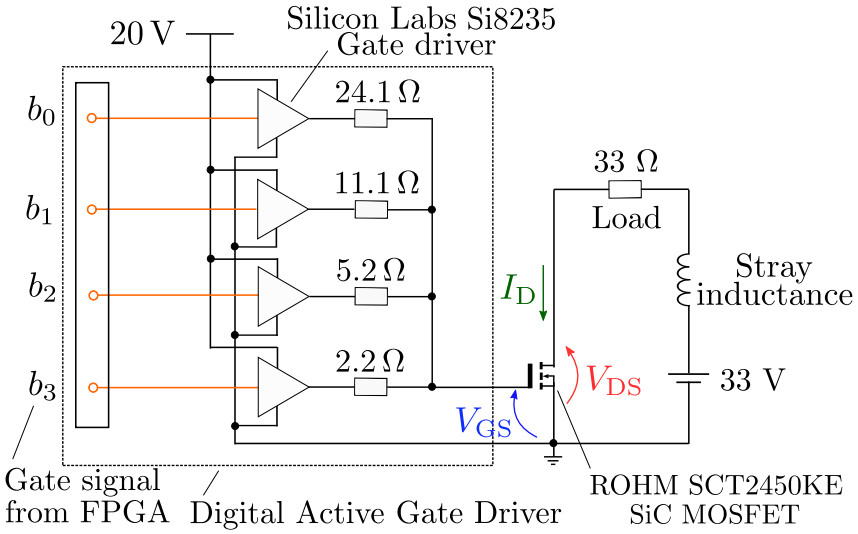


Figure 2.5: Schematic diagram of experimental circuit.

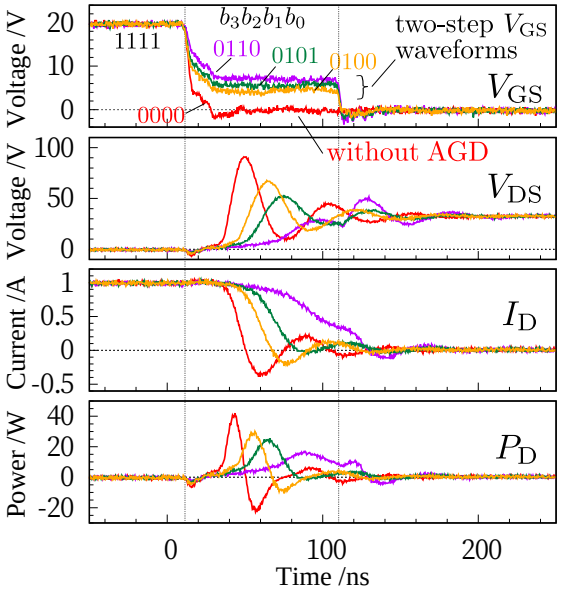


Figure 2.6: Switching waveforms without AGD and with simple two-step V_{GS} waveforms.

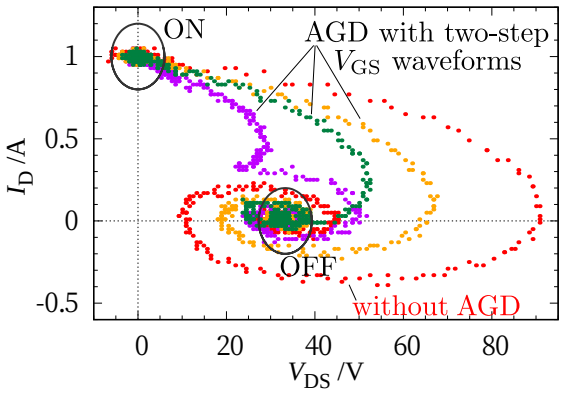


Figure 2.7: Switching trajectories without AGD and with simple two-step V_{GS} waveforms.

2.2.2 Manipulation of switching trajectory with active gate drive

Firstly, the MOSFET is switched without active gate drive (without AGD); the gate signal is changed from 1111 to 0000 during turn-off. The switching waveforms of V_{GS}, V_{DS}, I_D, and instantaneous power dissipation ($P_D = V_{DS} \times I_D$) are plotted in Fig. 2.6 with red lines. A large surge voltage and ringing are present, and the peak of V_{DS} is 90.8 V.

Secondly, to investigate the relationship between the value of V_{GS} and the switching waveform, an intermediate voltage level is inserted between on and off. The simple two-step V_{GS} waveforms as shown in Fig. 2.6 with purple/green/yellow lines are tested. Here, the three signals are selected out of the possible 15 levels because they showed the most remarkable change. The switching trajectories are also plotted on the phase plane in Fig. 2.7 using the same colors. The ON and OFF regions given by Eq. (2.2) are also shown with ellipses.

When the gate signal is 0100, the gate charge extraction is slowed down, and the surge voltage is suppressed. The switching trajectory moves toward the OFF operating point from the start. In the next case, the switching trajectory moves toward the outside of the OFF region during 0101 is input. This means that the designated V_{GS} is between $V_{plateau}$ and V_{th}. The switching is, therefore, not completed during the period until the gate signal turns 0000. This trend is observed more clearly in the last case, where the switching trajectory stays between the ON and OFF regions while 0110 is given, and then the rest of the switching continues when the gate signal turns 0000.

From these results, it is confirmed that the transient switching behavior of the SiC MOSFET is dynamically adjusted by the selection of V_{GS} level. The results also showed that the surge voltage can be suppressed by setting V_{GS} between $V_{plateau}$ and V_{th}.

2.2.3 Switching improvements with adjusted gate signal sequences

In the cases above, the gate charge extraction is slowed down, which results in the delay of V_{DS} and I_D to start switching. To discharge it quickly before switching begins, 0000 should be sent briefly as the first step of the turn-off procedure until V_{GS} reaches $V_{plateau}$. Also, after V_{DS} and I_D finish switching, the gate signal should quickly be changed to 0000 to complete the turn-off operation.

Considering these, the gate signal sequence is adjusted as listed in Table 2.1 through trial and error. The resulting waveforms are plotted in Fig. 2.8 and Fig. 2.9. Table 2.2 shows the peak of the surge voltage ($V_{DS,peak}$), calculated $t_{tran,off}$, and switching loss (P_{mos}) in each case, compared with those without active gate drive. Between AGD 1 and 2, the surge voltage is better suppressed in AGD 2, by about 50 V compared with that without AGD. The switching time is shorter in AGD 1, because in AGD 2 the trajectory stays longer outside the OFF region. The reason for these differences is that the designated value of V_{GS} in AGD 2 is slightly above V_{th}, as confirmed in Section 2.2.2, which leads

Table 2.1: Adjusted gate signal sequences during turn-off.

case	gate signal sequence (changed every 25 ns)
AGD 1	1111 → 0000 → 0100 → 0100 → 0000
AGD 2	1111 → 0000 → 0101 → 0101 → 0000
AGD 3	1111 → 0000 → 0101 → 0100 → 0000

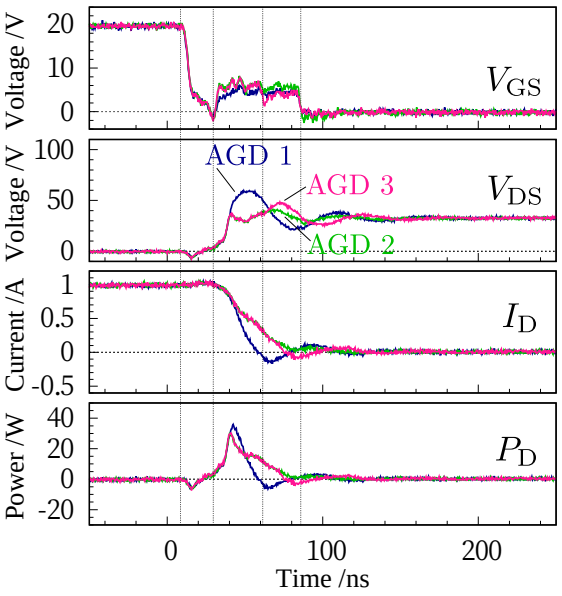


Figure 2.8: Switching waveforms in AGD 1, 2, and 3.

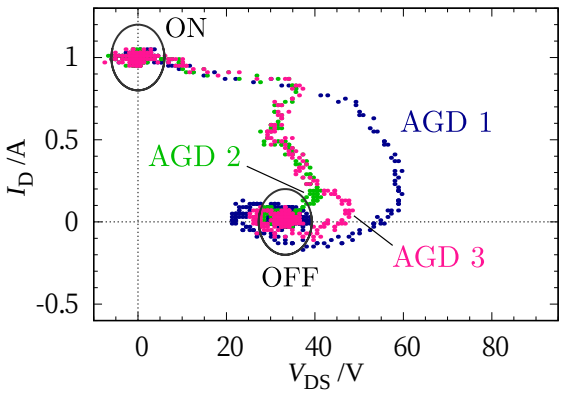


Figure 2.9: Switching trajectories in AGD 1, 2, and 3.

Table 2.2: Peak of surge voltage, switching time, and switching loss.

case	$V_{DS,peak}$ (V)	$t_{tran,off}$ (ns)	P_{mos} (μJ)
without AGD	90.8	115	0.21
AGD 1	59.6	61	0.43
AGD 2	41.2	73	0.64
AGD 3	48.4	88	0.60

to the slower switching speed during the active period. It is expected that by combining these two waveforms, as can be observed in AGD 3, a good balance between the V_{DS} peak and $t_{tran,off}$ can be achieved. In AGD 3, the switching trajectory first follows that of AGD 2, and then switches to that of AGD 1. However, although the surge voltage is well suppressed, the switching time is the longest among these three. This is partly attributed to the additional fluctuation in V_{GS}, followed by the additional oscillation in V_{DS} and I_D.

The turn-off switching loss in the MOSFET (P_{mos}) is calculated by integrating P_D.

Since the slopes of V_{DS} and I_{D} become gentle by active gate drive, the loss inevitably increases. The loss in the gate drive circuit also increases due to the configuration of the digital-to-analog converter. The efficiency of this driver for practical application needs to be investigated.

From these experimental results, the proposed gate driver and the strategy of shaping the V_{GS} waveform proved effective in suppressing the surge voltage and mitigating the turn-off transient. It is also confirmed that the adjustment of the gate signal sequence allows the application of various V_{GS} waveforms. This result characterizes the proposed driver because the operating principle of many reported active gate drivers, such as switched resistor ones, limits the outline of the V_{GS} waveform. The increase in the number of bits and the clock rate will facilitate the development of sophisticated strategies for adjusting its operation.

2.2.4 In-rated switching operation test of SiC MOSFET

The operation of DAGD has been confirmed so far in this section. However, as SiC MOSFETs are aimed at high-power applications, the proposed gate driver must also be tested in an operating condition processing higher power. Accordingly, the operating condition is set at 200 V and 4 A using the same circuit board. The transient switching waveforms and switching trajectories without and with AGD are shown in Figures 2.10 and 2.11, respectively.

As can be seen in Fig. 2.10, the switching waveforms without AGD exhibit sustained oscillation at the frequency of around 25 MHz. This frequency approximately corresponds to the resonant frequency of stray inductance and the output capacitance of the MOSFET, which are hundreds of nH and hundreds of pF, respectively. Meanwhile, with AGD, where the gate signal sequence is adjusted to $1111 \rightarrow 0000 \rightarrow 0101 \rightarrow 0101 \rightarrow 0000$ every 25 ns, oscillation does not occur and the surge voltage is suppressed. In Fig. 2.11, the trajectory without AGD first approaches the OFF operating point until the oscillation begins and the trajectory converges into a limit cycle outside the OFF region. With AGD, on the other hand, the trajectory smoothly moves toward the OFF operating point.

The circuit used here has large stray inductances on purpose, which led to the oscillation at a relatively low voltage. However, such a failure in circuit operation can happen with fewer stray inductances under much higher voltage conditions. These results indicate that the influence of stray inductances can be set aside by the active gate drive. In

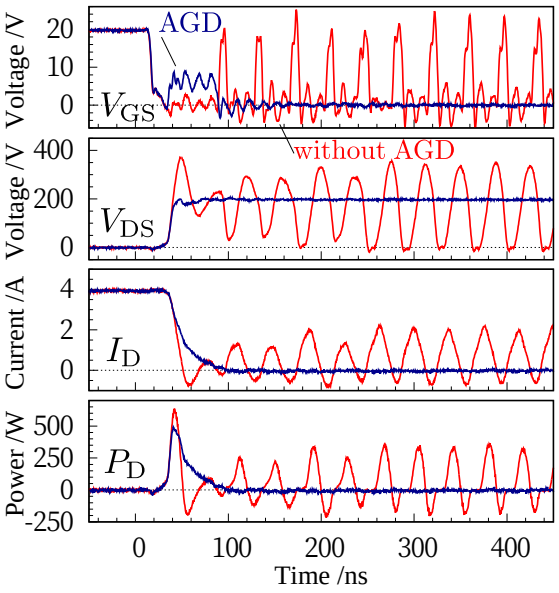


Figure 2.10: Switching waveforms without/with AGD under a higher-voltage condition.

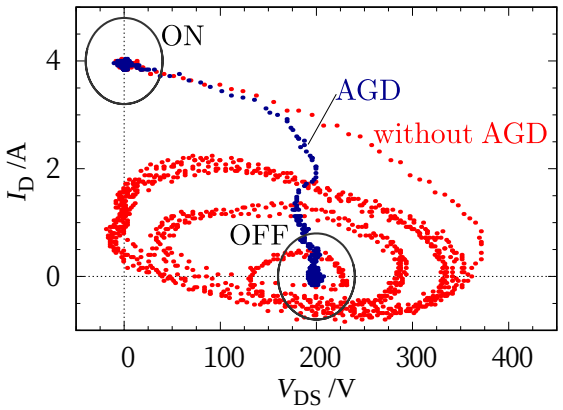


Figure 2.11: Switching trajectories without/with AGD under a higher-voltage condition.

other words, the active gate drive allows larger stray inductances, which will ease the restrictions in circuit design and operation, especially in highly integrated power circuits.

2.3 Additional verification in simulation

The verification of the experimental results is given by SPICE simulation using the SIMetrix software. The simulation settings are basically the same as those shown in Fig. 2.5, except for some differences as follows: the gate drivers are configured using ideal switches with the same output resistances as the Si8235; the characteristics of the SiC MOSFET is given by a model available on the manufacturer's website; the stray inductance in the main circuit is assumed to be 600 nH.

2.3.1 Support for experimental results

Switching waveforms without and with AGD are shown in Fig. 2.12. The gate signal sequences in AGD 1, 2, and 3 are the same as in the experiment, except that 0000 is designated for the first 50 ns. This is because the time at which V_{DS} and I_D start switching is delayed compared to that in the experiment. It is confirmed that the driving results without AGD, AGD 1, and AGD 2 approximately reproduce the experimental results.

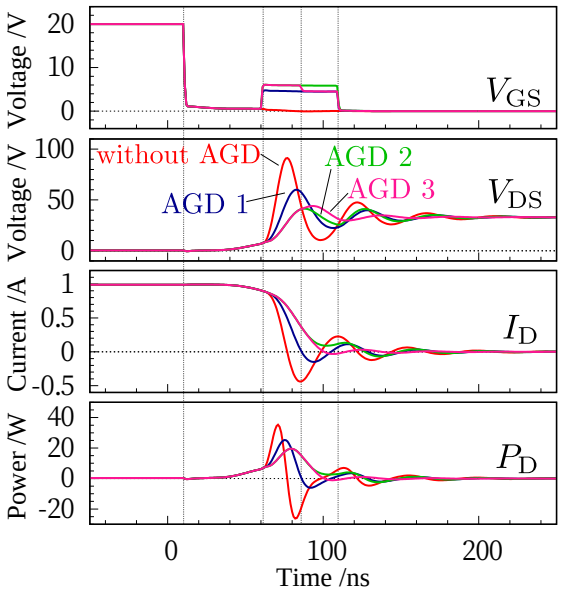


Figure 2.12: Simulated switching waveforms without/with AGD.

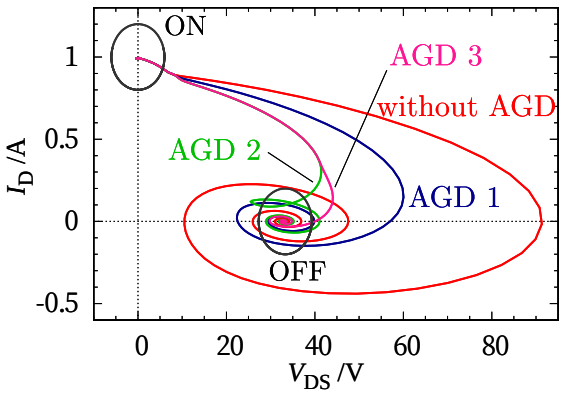


Figure 2.13: Simulated switching trajectories without/with AGD.

Table 2.3: Peak of surge voltage, switching time, and switching loss (simulation).

case	$V_{\mathrm{DS,peak}}$ (V)	$t_{\mathrm{tran,off}}$ (ns)	P_{mos} (μJ)
without AGD	91.3	88	0.23
AGD 1	60.0	55	0.46
AGD 2	41.5	71	0.63
AGD 3	44.1	41	0.57

However, as opposed to the experimental results, AGD 3 shows the shortest switching time and a well-suppressed surge voltage, as shown in Table 2.3, which is the result we expected to see in the experiment. This difference is explained by the switching trajectory, which transits smoothly from that of AGD 2 to that of AGD 1, thereby converging into the OFF region without additional oscillation.

2.3.2 Performance comparison with simple gate drivers

This section describes a comparison of gate drivers' performance between the proposed method and the conventional gate driver (CGD) with different values of gate resistances in simulation. The five cases as follows are compared; the first two cases, "without AGD" and "AGD 3", are picked up from Fig. 2.12 and Table 2.3, and the other three cases are obtained using CGD, where one gate driver is used and the gate resistance (R_{G}) is set at

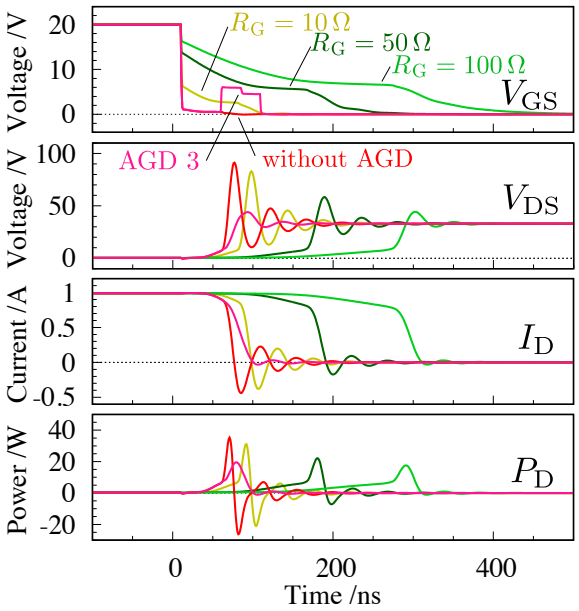


Figure 2.14: Simulated switching waveforms without AGD, with AGD 3, and with CGD ($R_G = 10/50/100\,\Omega$).

Table 2.4: Peak of surge voltage, switching time, and switching loss: comparison between the proposed gate driver and the conventional gate driver (CGD) with incremented gate resistances (simulation).

case	$V_{DS,peak}$ (V)	$t_{tran,off}$ (ns)	P_{mos} (μJ)
without AGD	91.3	88	0.23
AGD 3	44.1	41	0.57
CGD ($R_G = 10\,\Omega$)	83.0	76	0.32
CGD ($R_G = 50\,\Omega$)	58.4	77	0.64
CGD ($R_G = 100\,\Omega$)	44.3	83	0.98

10/50/100 Ω. Figure 2.14 shows the simulated switching waveforms, and Table 2.4 shows the peak of surge voltage, switching time, and switching loss in each case. From Table 2.4, when $R_G = 100\,\Omega$, the surge voltage is suppressed as low as in AGD 3. However, the switching loss and the switching time are almost doubled, and the switching is delayed compared to AGD 3. These results indicate that the proposed gate driver can achieve a better trade-off than the conventional gate drivers.

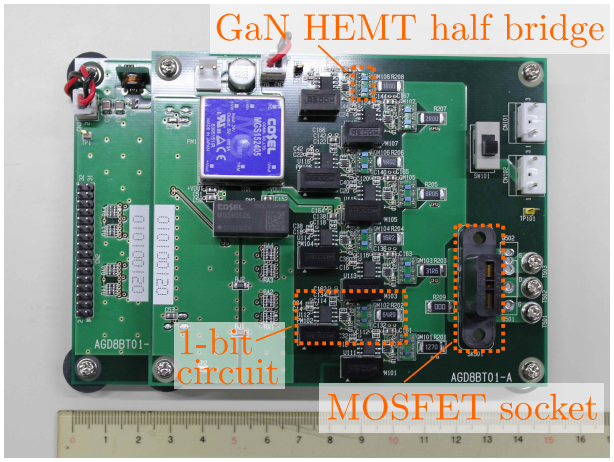
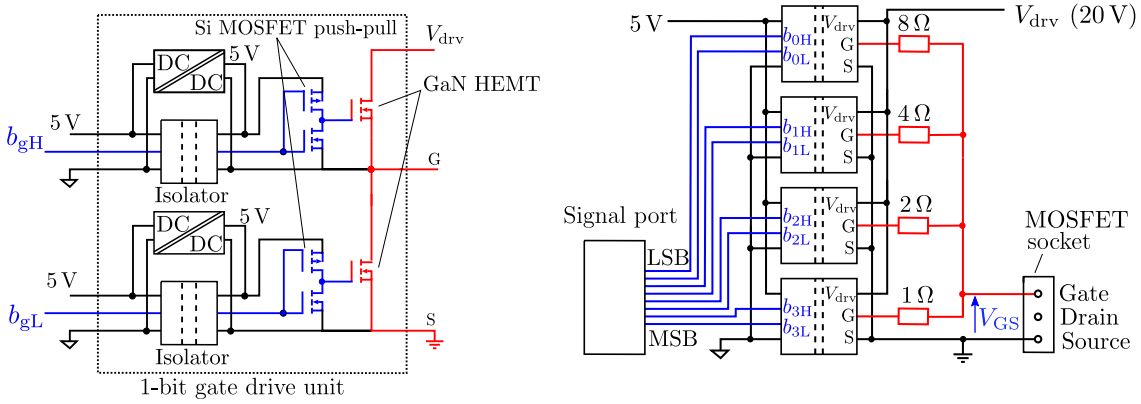


Figure 2.15: Photograph of GaN-HEMT-based 8-bit DAGD.



(a) 1-bit gate drive unit. (b) 4-bit configuration.

Figure 2.16: Schematic configuration of GaN-HEMT-based digital active gate driver.

2.4 GaN-HEMT-based DAGD

In this section, an updated DAGD configuration is presented, using GaN-HEMT as the switching device inside the gate driver. The fundamental concept and operation of DAGD have been verified so far in this chapter. However, the use of commercial gate driver ICs and a controller with a low clock-rate of 40 MHz limits the resolution of the resulting V_{GS} waveform. Switching frequency of an order of 100 MHz will be required for precise control of gate voltage and the rise/fall time should be as small as possible to realize a fast transition from one V_{GS} level to another. Therefore, GaN HEMT is adopted as the switching device inside the gate driver [74]. Figure 2.15 shows the fabricated GaN-HEMT-based DAGD, and Fig. 2.16 shows its schematic configuration. Four half-bridge

legs of GaN HEMTs (EPC2014C, Efficient Power Conversion) are integrated with gate resistances of 1, 2, 4, 8 Ω. Although 4-bit configuration is studied in this chapter, the fabricated DAGD board has additional four half-bridge legs with gate resistances of 16, 32, 64, 128 Ω, which can be utilized if 8-bit resolution is preferred.

2.5 Summary

In this chapter, the concept of the digital active gate driver for SiC MOSFETs is investigated via experiment and simulation. The use of binary-weighted resistor DAC configuration is found applicable as the mechanism to shape the gate voltage arbitrarily using multi-bit digital signals. A flexible gate-driving strategy is discussed using discrete operating points on the state space of the device given by the discrete V_{GS} values. This point of view gives the advantage of controlling the switching trajectory of the MOSFET by means of digital signals. The experimental results using the prototype of DAGD indicate that the switching behavior of the device drastically changes by the selection of gate signal sequence during the switching transient. It is confirmed that the surge voltage during turn-off is suppressed and the switching transient is shortened by adjusting the V_{GS} waveform based on the estimated device characteristics. These results are also verified in the SPICE simulation. Finally, an improved hardware of DAGD is designed using GaN HEMTs to achieve faster response of V_{GS} waveform. The investigation of the systematic benefit of the DAGD system is continued in the next chapter, utilizing the hardware developed in this chapter.

Chapter 3

Software-aided optimization of switching behavior

This chapter investigates a software-based optimization strategy for DAGD. With the developed DAGD, the analog phenomenon of power switching is now controlled by means of digital signal adjustment. This fundamentally transforms the nature of the approach to designing the function of the gate driver from hardware to software, making it a target of combinatorial optimization problems. To cultivate this aspect, suitable optimization software needs to be developed. The genetic algorithm (GA) [75], one of the best-known metaheuristics, is found preferable for optimizing DAGD's operation because of its binary nature. The optimization platform is developed using GA with an orientation toward establishing a digital-twin-compatible link, where the performance of an AGD sequence would be evaluated in simulation and then applied to the experiment. The detailed system configuration and its verification results are presented in this chapter.

3.1 Gate driving strategy for DAGD

In variable-voltage type AGDs, it is essential to consider the voltage-related characteristics of MOSFETs, such as the drain characteristics, gate threshold voltage (V_{th}), and Miller plateau voltage (V_{plateau}). The relationship between the V_{GS} level and the state of the MOSFET is discussed on the I_{D}–V_{DS} plane [11]. Figure 3.1 shows several I_{D}–V_{DS} curves of a MOSFET and a load curve for a pure inductive load. As shown in this figure, the transient behavior of the switching trajectory is strongly related to V_{GS} levels, especially V_{th} and V_{plateau}.

DAGD directly manipulates its trajectory by means of shaping the V_{GS} waveform.

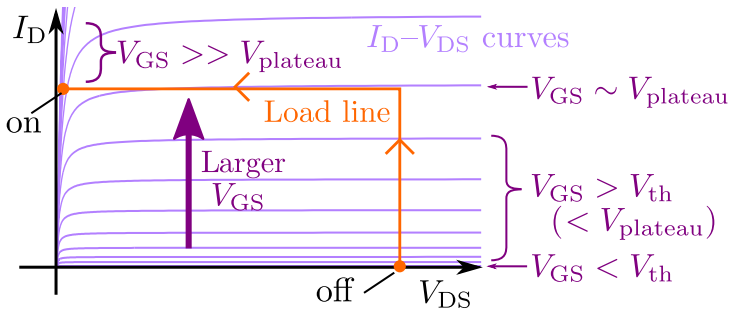


Figure 3.1: Example of I_D–V_{DS} (drain current vs drain-source voltage) curves of MOSFET and load curve. © 2023 IEEE.

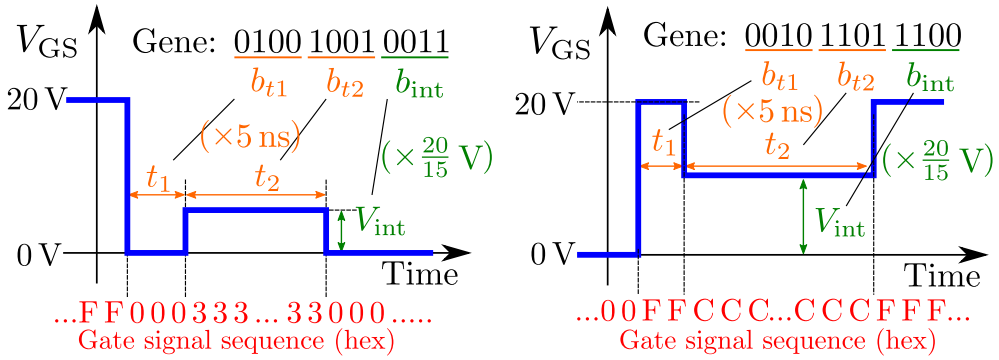
When V_{GS} is set to a certain value specified by a gate signal, it is equivalent to choosing an I_D–V_{DS} curve corresponding to the V_{GS} value. Therefore, selecting a gate signal during the switching transient is equivalent to setting a particular operating point, which is an intersection between the corresponding I_D–V_{DS} curve and the load curve.

3.2 Optimization of gate signal sequence using genetic algorithm

This section develops the optimization tool for DAGD using GA. In GA, the target of optimization is a population, which is a set of individuals with their own genes and fitness. The individuals with better fitness are searched by using genetic operators, namely the selection, crossover, and mutation, through the generations [76]. DAGD is a preferable application for GA because of the binary nature of its operating principle. While the gate signal sequence itself can be directly used as a gene, we convert it to a genotype to set a constraint on V_{GS} waveform, which will help clarify the relationship between the optimum patterns and the switching characteristics.

3.2.1 Genetic expression of V_{GS} waveform

Figure 3.2 shows the adopted V_{GS} waveform and the corresponding genotype. These types of V_{GS} waveform are called as the three-level waveform in some literature [45, 77]. At the beginning of the turn-off process, the gate is quickly discharged for the duration of t_1 until the transition of I_D begins. Then, V_{GS} is set to an intermediate voltage level V_{int} for the duration of t_2 to slow down the transition of I_D and V_{DS}. A similar strategy is applied to turn-on as shown in Fig. 3.2 (b). A 12-bit binary string is used as the gene to express



(a) Turn-off. (b) Turn-on.

Figure 3.2: Genotype and phenotype of gate signal sequences and corresponding V_{GS} waveforms. © 2023 IEEE.

these target V_{GS} waveforms, which is divided into three parts of 4-bit strings: b_{t1}, b_{t2}, and b_{int}. The first two parts designate the duration of t_1 and t_2 by multiplying them by 5 ns. b_{int}, which designates the voltage level V_{int}, is considered to be the most important part of the three, as it determines the operating point of the MOSFET. We can effectively analyze which voltage level and timing would improve the switching characteristics with this waveform. Hereafter, b_{int} is expressed using a hexadecimal number. The gene is encoded to a time-series gate signal sequence as shown in Fig. 3.2.

The performance of this AGD waveform strongly depends on the resolution of the input signals. Considering the response speed of the SiC MOSFETs, such as delay time and rise/fall times, are several ten nano-seconds or smaller, nano-second-order control is required. To realize such fine-tuning of V_{GS} waveform, the controller needs to be an FPGA with a clock frequency of several hundred MHz. In addition, a pulse width of less than 15 ns is found challenging considering the response of the switching devices and the signal isolators used inside DAGD. Therefore, we set a rule that t_1 and t_2 must be more than 10 ns, except for the case of 0 ns.

The following two values are used to evaluate the fitness of the genes. One is the amount of overshoot, which is the peak of V_{DS} at the turn-off and that of I_D at the turn-on. The other is the switching loss calculated by integrating $I_D \times V_{DS}$ for 200 ns from the start of turn-off/on. This duration is decided considering the convergence of ringings.

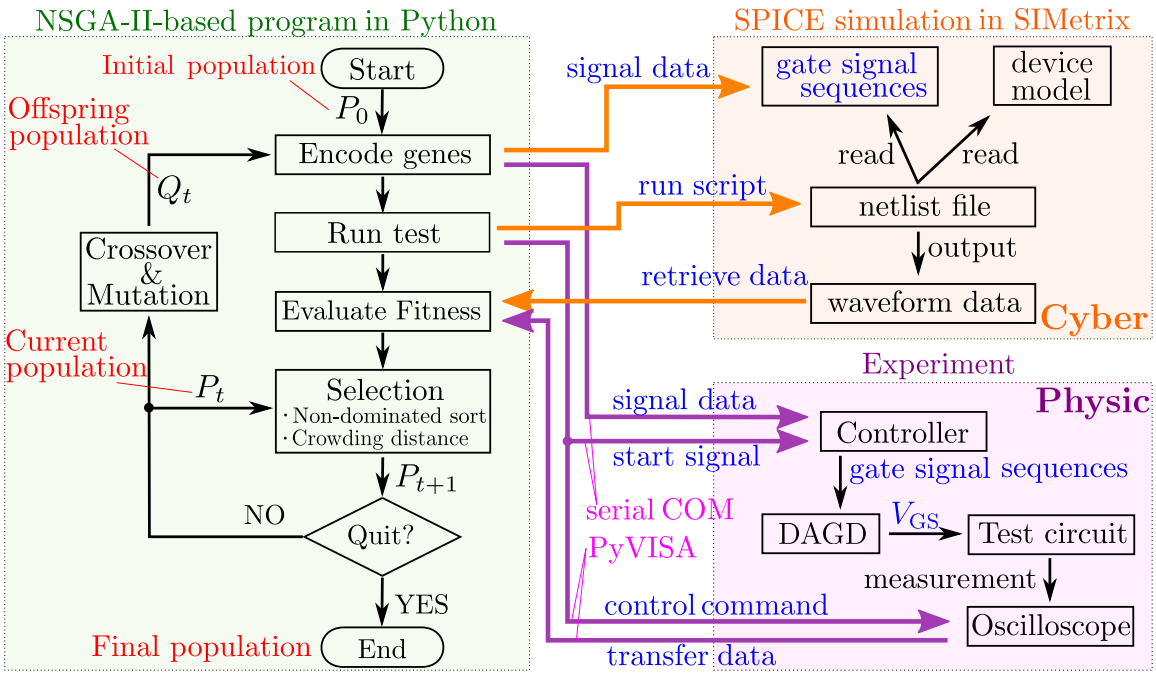


Figure 3.3: Flowchart of optimization process interfacing SPICE simulation (orange area) and experiment (purple area). Orange and purple arrows denotes the data or command transfer between the program in PC and simulation soft/experimental apparatus. © 2023 IEEE.

3.2.2 Optimization process using Python

The optimization algorithm is constructed based on the non-dominated sorting GA II (NSGA-II) [76], which is a well-known and widely-used multi-objective GA, using a Python framework called DEAP [78]. The flowchart of the optimization process is shown in Fig. 3.3. The left-hand part describes the Python program that runs on the user's PC, which has two interfaces for the SPICE simulation in SIMetrix software and experimental instruments. The gate signal data and commands are sent from left to right, and the waveform data is sent from right to left through respective means. This structure makes the optimization tool a digital-twin-compatible system, where the optimization algorithm developed using simulation can be directly applied to the experiment. It is also expected that the effective AGD sequence would be predicted using simulation. A switching test is supposed in this chapter, but a similar structure can be configured for other applications, such as converter operation. The detailed procedure is described in the following.

Firstly, an initial population consisting of 60 individuals with randomly selected genes is created. Their genes are then encoded into the time-series gate signal sequence data,

and the switching tests are performed for all genes. In the simulation, a SIMetrix script simulates the predefined netlist file containing the circuit information and device model references. It reads the gate signal sequence, saved as a text file, as the input signals of DAGD. The outcome of the simulation is saved as the output file, and the necessary data, such as device voltage and current waveforms, are read by the Python program. In the experiment, the Python program sends the signal sequence data and start command to the controller through serial communication. Then, the switching test is performed, and the device current and voltage waveforms are measured by an oscilloscope. The waveform data is transferred back to the Python program. No user interaction is needed as the oscilloscope is totally controlled by the program through PyVISA commands.

Based on the waveform data, the fitness of each gene is calculated. The selection is performed consequently using the non-domination rank, which is an index assigned to each solution from their fitness to classify how close it is to the Pareto-front [76]. Further details of the selection algorithm are described in Appendix B.

The second loop starts here by generating an offspring population of the same size from the current population by two-point crossover and one-bit flip mutation with probabilities of 0.9 and 0.1, respectively. Its individuals are encoded, tested, and evaluated in the same manner as described above. From the second loop, the selection is performed from the set of current (parent) and offspring populations. The search ends after going through this process for 15 loops, which we confirmed to be sufficient for the search to converge, and the final population is obtained.

This is a system that preliminary simulates or tests the gate signal sequences for the power device to obtain the Pareto-front solutions. One can select the solution that meets the requirements for switching characteristics after the hardware implementation. The key advantage of such a system is that the whole optimization is handled by software. The expert know-how or time-consuming try-and-error do not exist in the design procedure.

3.3 System verification in simulation and experiment

The proposed optimization system is applied to the standard double-pulse switching test with an inductive load. The optimization is performed in the simulation and in the experiment, respectively.

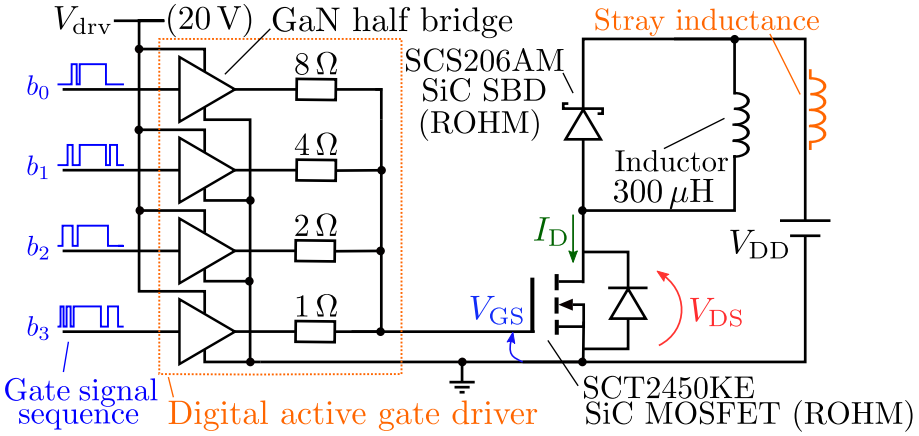


Figure 3.4: Schematic diagram of GaN-HEMT-based 4-bit DAGD and double-pulse test circuit. © 2023 IEEE.

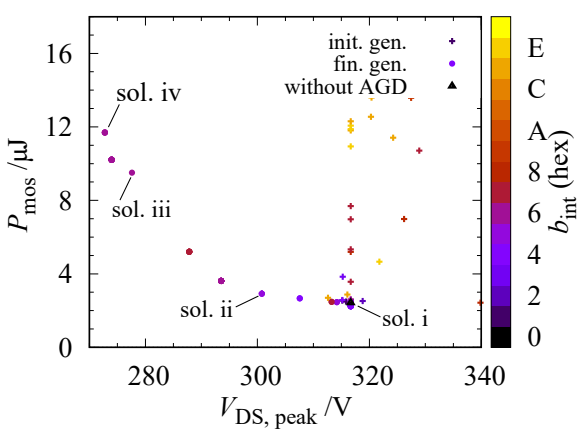
3.3.1 Test circuit and simulation setup

Figure 3.4 shows the schematic diagram of the test circuit. In the simulation, it is represented as a netlist file with stray inductances assumed at each terminal of the power devices and the wire from V_{DD}, which are 5 nH and 60 nH, respectively. We adopt a physically-based simulation model for SiC MOSFET based on its surface potential [79]. It can reproduce the accurate I_D–V_{DS} characteristics even in the high-power region, which helps the analysis of the AGD strategy based on I_D–V_{DS} curves. Device models for the other parts are adopted from the manufacturer's database. The operating condition is set at 240 V and 4 A, which is the same as in the experiment.

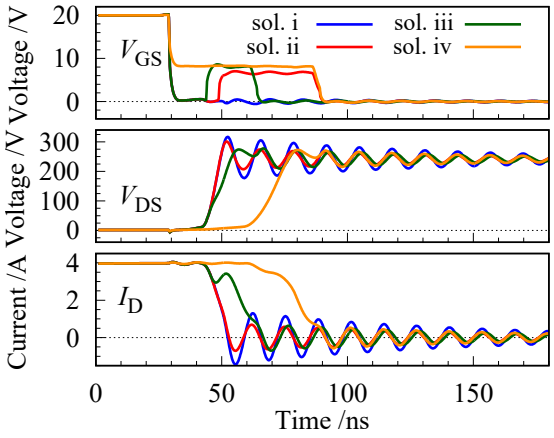
3.3.2 Simulation results

Figure 3.5 shows the results of optimization at turn-off, and Figure 3.5 (a) shows the fitness map of the solutions in the initial and final generation population. The color bar on the right-hand side denotes which value of b_{int} is selected for each solution. The fitness without AGD, which corresponds to a solution with a gene "0000_0000_0000", is also shown for comparison. This figure confirms that the Pareto-front solutions are successfully obtained by the optimization.

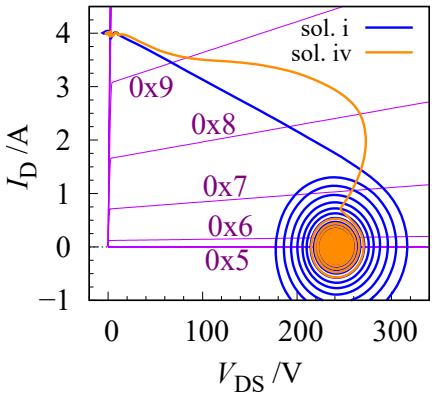
We choose some of the solutions in the Pareto-front to analyze their transient behavior. Figure 3.5 (b) shows the transient switching waveforms of the selected four solutions. Table 3.1 shows the representative trade-off relationship between $V_{DS,peak}$ and transition times of V_{DS} and I_D between their 10 % and 90 % of the rated value. In sol. iii and iv,



(a) Fitness map of initial and final generation solutions.



(b) Switching waveforms of V_{GS}, V_{DS}, and I_D for solutions i, ii, iii, and iv.



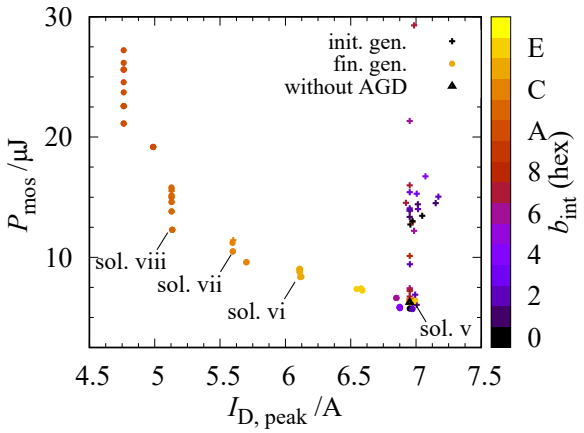
(c) Switching trajectories of solution i and iv.

Figure 3.5: Optimization results at turn-off in simulation. © 2023 IEEE.

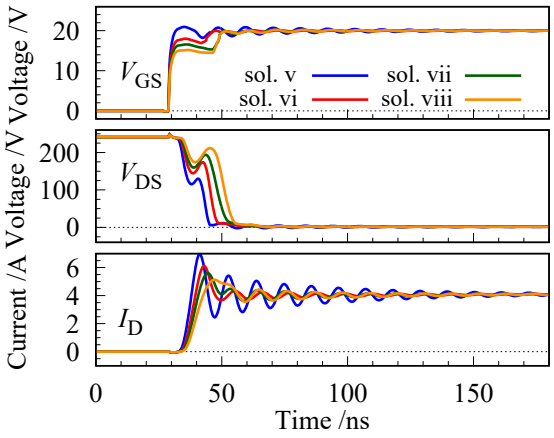
Table 3.1: Trade-off between overshoot and transition time of V_{DS} and I_D for selected solutions at turn-off. © 2023 IEEE.

turn-off solutions	sol.i	sol.ii	sol.iii	sol.iv
$V_{DS,peak}$ (V)	317	301	278	273
V_{DS} fall time (ns)	5.4	5.4	9.0	13.2
I_D rise time (ns)	7.2	7.4	20.8	23.6

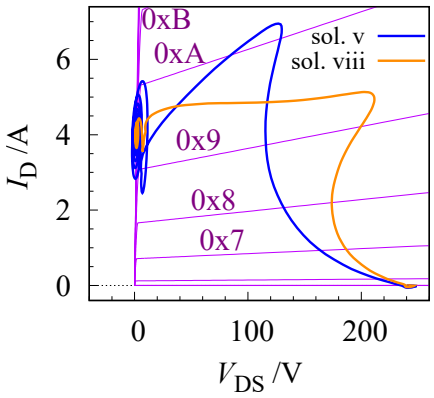
b_{int} = 0x6 is selected and $V_{DS,peak}$ is well-suppressed, while the transition time is longer and so do the switching loss. In sol. iv, the discharge of the gate is slowed from the start by setting t_1 at 0 ns, which further increases the switching loss. In sol. ii, a smaller value of b_{int} = 0x5 is selected, which increases the overshoot but decreases the transition time and the loss. Figure 3.5 (c) shows the switching trajectories of sol. i and iv. Here, we



(a) Fitness map of initial and final generation solutions .



(b) Switching waveforms of V_{GS}, V_{DS}, and I_D for solutions v, vi, vii, and viii.



(c) Switching trajectories of solution v and viii.

Figure 3.6: Optimization results at turn-on in simulation. © 2023 IEEE.

Table 3.2: Trade-off between overshoot and transition time of V_{DS} and I_D for selected solutions at turn-on. © 2023 IEEE.

turn-on solutions	sol.v	sol.vi	sol.vii	sol.viii
$I_{D,peak}$ (V)	6.97	6.11	5.60	5.13
V_{DS} rise time (ns)	10.8	14.0	16.6	21.6
I_D fall time (ns)	3.2	4.0	4.6	5.4

checked the possible 15 V_{GS} levels corresponding to the 4-bit gate signal, and drew the I_D–V_{DS} curves at these V_{GS} values. From this figure, it is understood that b_{int} = 0x6 corresponds to a V_{GS} level right above V_{th}, whose operating point is also slightly above the off state. The trajectory approaches this operating point during the duration of t_2, thereby suppressing the surge voltage, and then converges into the off state.

Figure 3.6 shows the optimization results at turn-on. From Fig. 3.6 (a), the Pareto-front is successfully obtained at turn-on as well. We can clearly recognize the sets of solutions with the same value of b_{int}, which gets larger as $I_{\mathrm{D,peak}}$ increases. This trade-off relationship is also confirmed in Table 3.2. The selected b_{int} is 0xA for the solutions around $I_{\mathrm{D}} = 4.75$A and 0xB for those around $I_{\mathrm{D}} = 5.2$A. From Fig. 3.6, it is understood that these bits designate the V_{GS} levels just above V_{plateau}. In sol. viii, the trajectory first moves toward the operating point on the I_{D}–V_{DS} curve corresponding to b_{int} =0xB, suppressing the overshoot of I_{D}. This result indicates that V_{int} must be above V_{plateau} to suppress the surge current at turn-on, and the overshoot increases as V_{int} becomes higher than V_{plateau}.

3.3.3 Experimental setup

We now apply the GA-based optimization system for DAGD to the experiment, utilizing the bottom-right part in Fig. 3.3. Figure 3.7 shows the photograph of experimental setup. The experimental apparatus comprises a PC, a controller (Zynq UltraScale+ MPSoCs, Xilinx Inc.), GaN-based DAGD, double-pulse test circuit, an oscilloscope (MDO4014-3, Tektronix Inc.) with probes, and power supplies. The 4-bit gate signal is generated inside FPGA by replacing the falling/rising edge of PWM signal with the turn-off/turn-on signal sequence given for each bit, as illustrated in Fig. 3.8. The Python program in the user PC communicates with the controller and the oscilloscope as described in Fig. 3.3. The waveforms of V_{GS}, V_{DS}, and I_{D} are measured by the oscilloscope and transferred to the PC for the calculation of the fitness.

3.3.4 Experimental results

Figure 3.9 shows the optimization results at turn-off. It can be observed that the algorithm generally works as expected in the experiment. Due to the inevitable measurement errors and the resulting loss calculation errors, the Pareto-front solutions are spread compared to simulation results. For this reason, the fitness of the solution without AGD may be located above the Pareto-front. The selected values of b_{int} are typically 0x6 for the solutions with smaller surge voltage, yielding a very similar result to the simulation. Also, the transient switching waveforms and trajectories in Fig. 3.9 (b) and (c) are similar to the simulation results. It is understood that the surge voltage is suppressed by the same physics as observed in the simulation. Table 3.3 compares the calculated switching

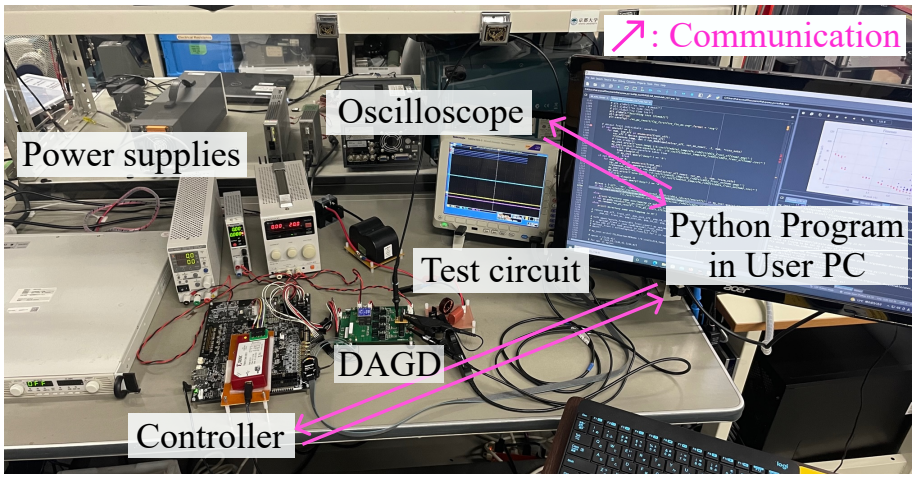


Figure 3.7: Photograph of laboratory experiment setup. © 2023 IEEE.

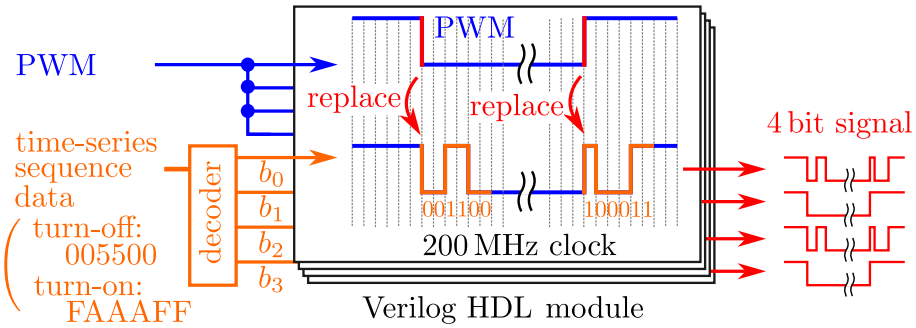
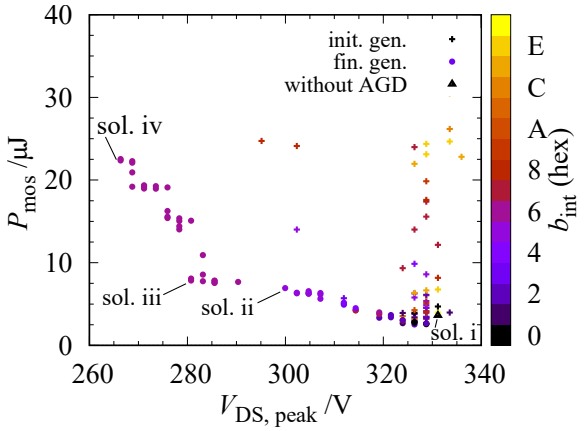


Figure 3.8: 4-bit gate signal generation inside FPGA. © 2023 IEEE.

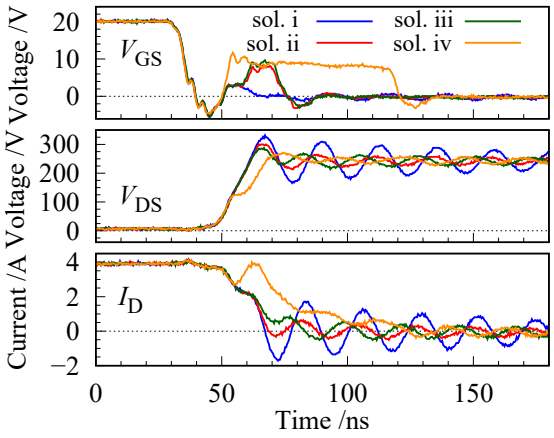
transition times among the selected solutions, which also indicates the same trade-off relationship is established as in simulation.

Figure 3.10 shows the optimization results at turn-on. The sets of solutions with the same value of b_{int} are obtained, and b_{int} =0xB is selected for solutions with the least $I_{\mathrm{D,peak}}$. From Fig. 3.10 (b), a fluctuation of V_{GS} is encountered, making it hard to read what voltage level is actually designated. Nonetheless, from Fig. 3.10 (c), it is understood that sol. viii designated the operating point right above V_{plateau}, as observed in simulation.

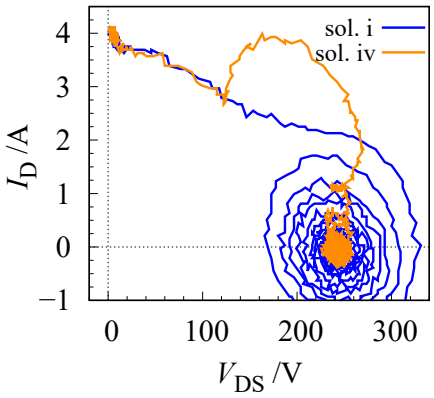
These results confirm that the proposed optimization system works similarly both in the simulation and experiments, verifying its digital-twin compatibility. The selected bits are quite similar but slightly different from the simulation results in both cases. In particular, the variables t_1 and t_2 do not match in simulation and experiment. This is partly because the gate dynamic characteristics are hard to reproduce accurately in the device model, and also partly because it is susceptible to change due to many influences,



(a) Fitness map of initial and final generation solutions.



(b) Switching waveforms of V_{GS}, V_{DS}, and I_D for solutions i, ii, iii, and iv.



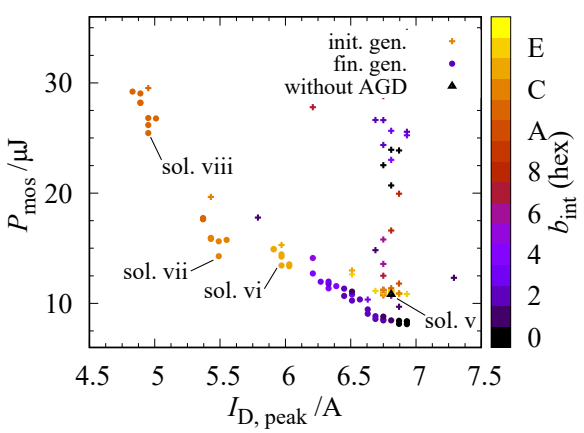
(c) Switching trajectories of solution i and iv.

Figure 3.9: Optimization results at turn-off in experiment. © 2023 IEEE.

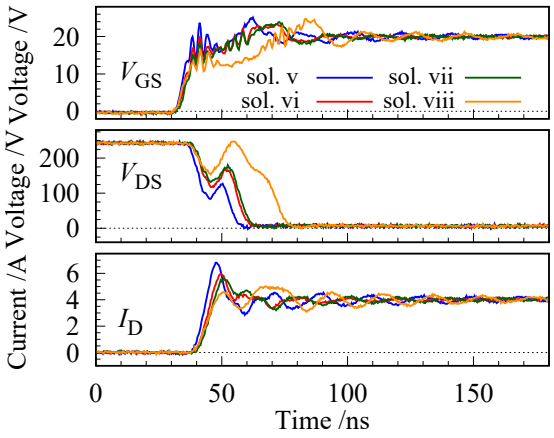
Table 3.3: Trade-off between overshoot and transition time for selected solutions at turn-off in experiment. © 2023 IEEE.

turn-off solutions	sol.i	sol.ii	sol.iii	sol.iv
$V_{DS,peak}$ (V)	331	300	281	269
V_{DS} fall time (ns)	11.6	11.2	17.6	18.0
I_D rise time (ns)	16.0	34.8	49.2	54.0

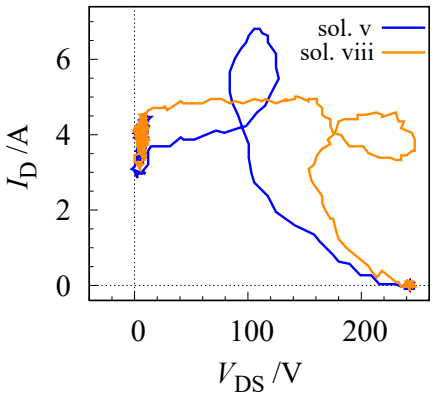
such as parameter variation among devices and temperature, as well as external circuitry configuration. For these reasons, it is not yet possible to use the predicted signal sequences directly in the experiment. The help of local-search-based algorithms can be integrated to realize a link between them.



(a) Fitness map of initial and final generation solutions.



(b) Switching waveforms of V_{GS}, V_{DS}, and I_D for solutions v, vi, vii, and viii.



(c) Switching trajectories of solution v and viii.

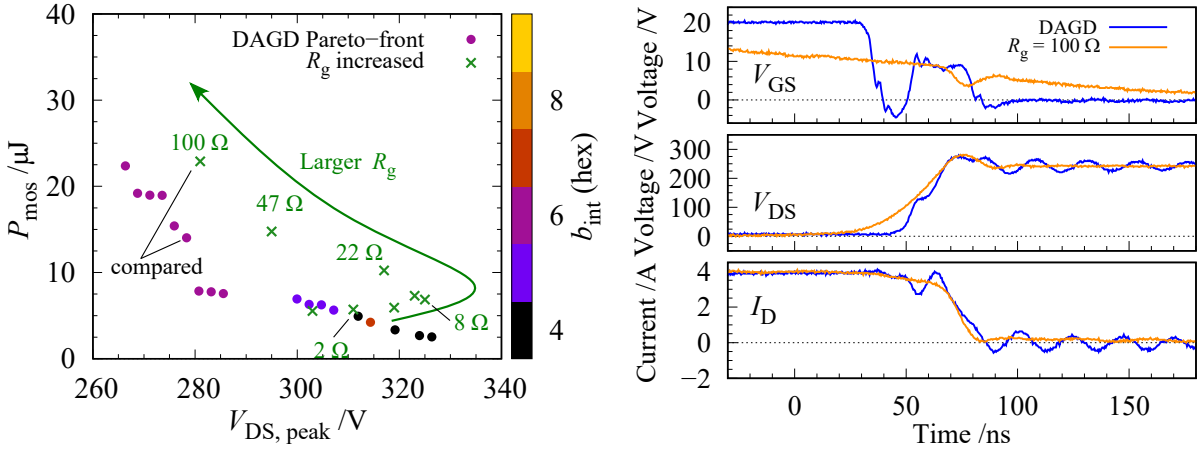
Figure 3.10: Optimization results at turn-on in experiment. © 2023 IEEE.

Table 3.4: Trade-off between overshoot and transition time for selected solutions at turn-on in experiment. © 2023 IEEE.

turn-on solutions	sol.v	sol.vi	sol.vii	sol.viii
$I_{D,peak}$ (V)	6.85	5.97	5.43	4.95
V_{DS} rise time (ns)	11.0	20.2	22.8	44.8
I_D fall time (ns)	3.4	5.2	5.2	6.8

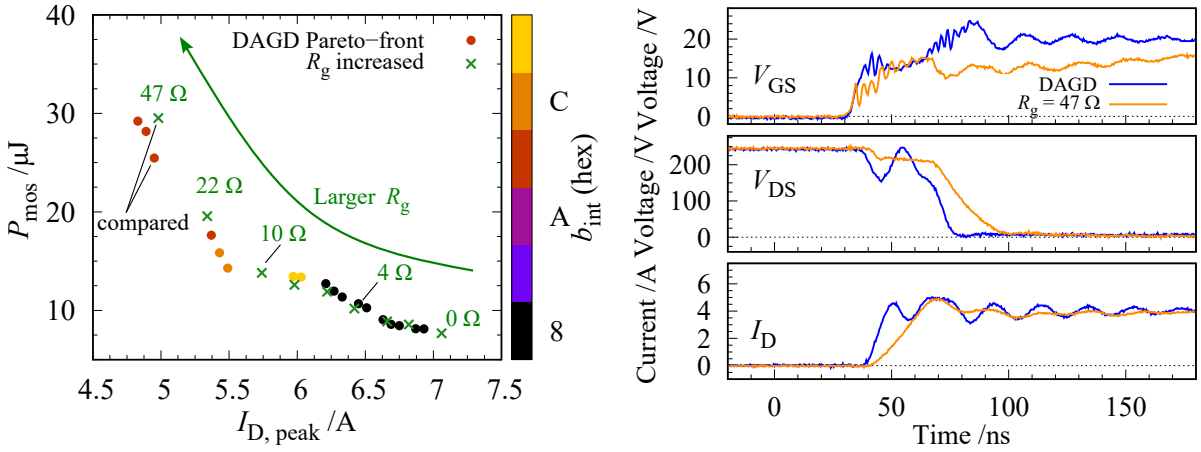
3.3.5 Comparison with simple gate-driving

Figures 3.11 and 3.12 show the comparison of switching characteristics between Pareto-front solutions achieved by DAGD (Figs. 3.9 and 3.10) and simple gate driving with different values of gate resistors. As can be clearly seen, DAGD solutions achieve better trade-offs compared to simple gate driving. We selected two solutions with similar



(a) Fitness map. (b) Switching waveforms.

Figure 3.11: Comparison of switching characteristics at turn-off between DAGD (Pareto-front solutions) and standard gate driving with large R_G.



(a) Fitness map. (b) Switching waveforms.

Figure 3.12: Comparison of switching characteristics at turn-on between DAGD (Pareto-front solutions) and standard gate driving with large R_G.

amounts of overshoots, as shown in the figure, and compared the transient waveform in Fig. 3.11 (b) and Fig. 3.12 (b). From Fig. 3.11 (b), it is found that the maximum di/dt is the same between the two solutions, yielding the same voltage overshoot, but the transition of drain voltage is quicker with DAGD, resulting in less switching loss. At turn-on, although it is not as drastic as in turn-off, DGAD solutions show a similar trend. Moreover, as can be confirmed in transient waveforms, the switching delay is much smaller in DAGD solutions because a fast switching speed is applied at the beginning of the transient.

3.4 Optimization in other operating conditions and for different SiC MOSFETs

So far in this chapter, the digital-twin-compatible optimization is verified for a single operating condition and a single device. This section provides some additional experimental results in different operating conditions and using different SiC MOSFETs to ensure the versatility of the proposed optimization tool and also to clarify the influence of these alterations on the optimum AGD sequence. The obtained solutions are analyzed from the viewpoint of device parameters.

3.4.1 Results in different operating conditions

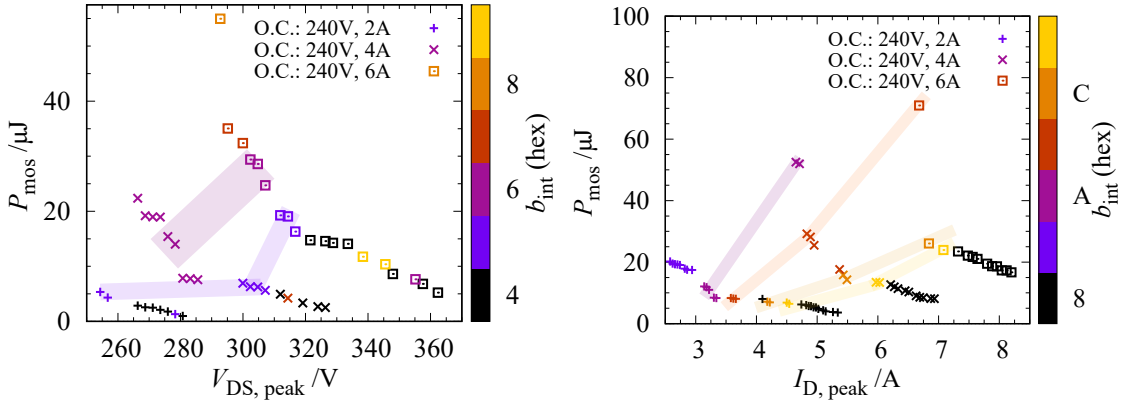
The optimization is performed for different operating conditions (O.C.). Firstly, different I_{D} of 2 A, 4 A and 6 A are applied whereas V_{DS} is kept at 240 V. This assumes an application that deal with variable load operation. Figure 3.13 (a) and (b) show the Pareto-front solutions at turn-off and turn-on, respectively. It is confirmed that the optimization works in all of these conditions. From Fig. 3.13 (b), it is found that the selected b_{int} becomes larger as the operating current increases. This trend corresponds to the observation in Section 3.3 that the effective value of b_{int} at turn-on is strongly tied with V_{plateau}, which becomes larger as I_{D} increases as understood from Eq. (1.2).

Secondly, three V_{DS} values of 120 V, 240 V, and 400,V are applied with the same operating current of 4 A. Figure 3.14 (a) and (b) show the optimization results. The Pareto-front solutions are obtained in all the conditions. In Fig. 3.14 (b), almost the same b_{int} is selected for all V_{DS} conditions, which is a clearly different trend compared to Fig. 3.13 (b). This can be attributed to the device physics that the V_{plateau} does not drastically change with the increase of V_{DS}.

3.4.2 Results for different device

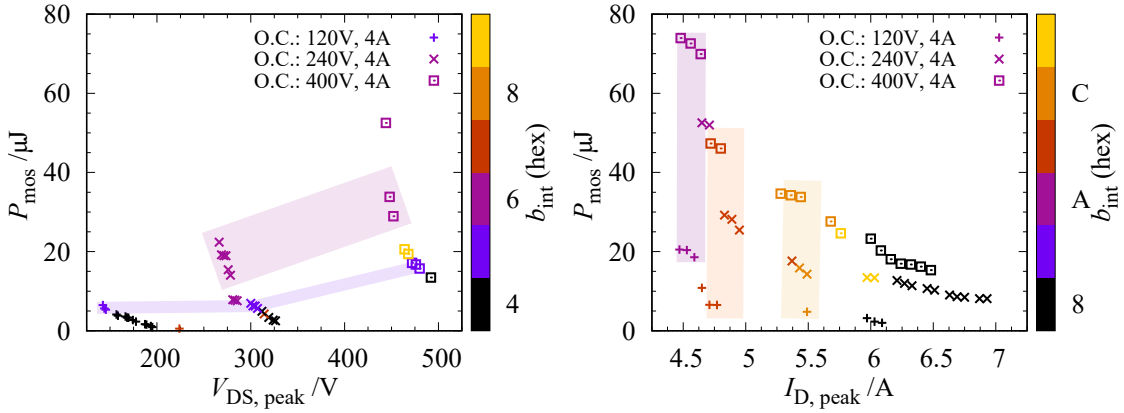
Lastly, the optimization is performed for several different devices at the operating condition of 240 V and 4 A. The results are compared from the viewpoint of differences in device parameters.

We compare the four randomly selected devices of the same model number (SCT2450KE, ROHM Co., Ltd.) to investigate the variation in V_{plateau}. Figure 3.15 shows the map of the optimized solutions for the four devices. There appear overlaps of the solutions at dif-



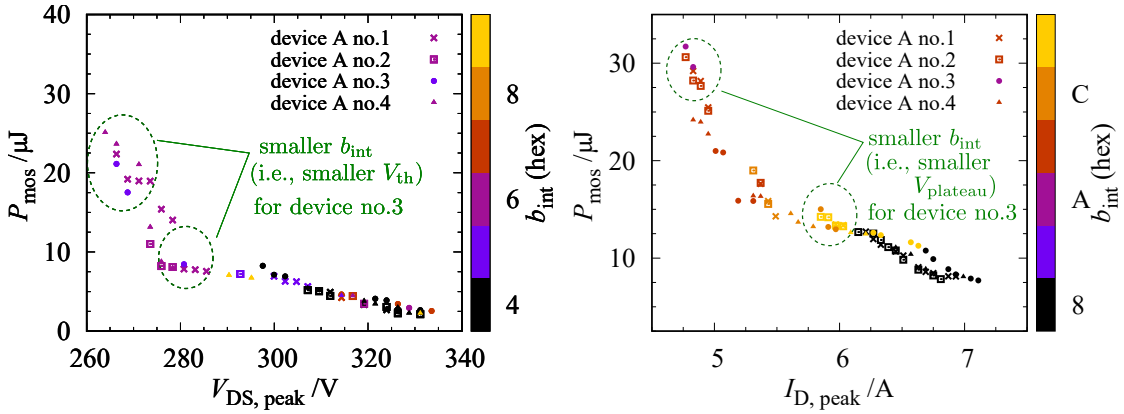
(a) Pareto-front solutions at turn-off. (b) Pareto-front solutions at turn-on.

Figure 3.13: Optimization results under variable-current conditions. © 2023 IEEE.



(a) Pareto-front solutions at turn-off. (b) Pareto-front solutions at turn-on.

Figure 3.14: Optimization results under variable-voltage conditions. © 2023 IEEE.

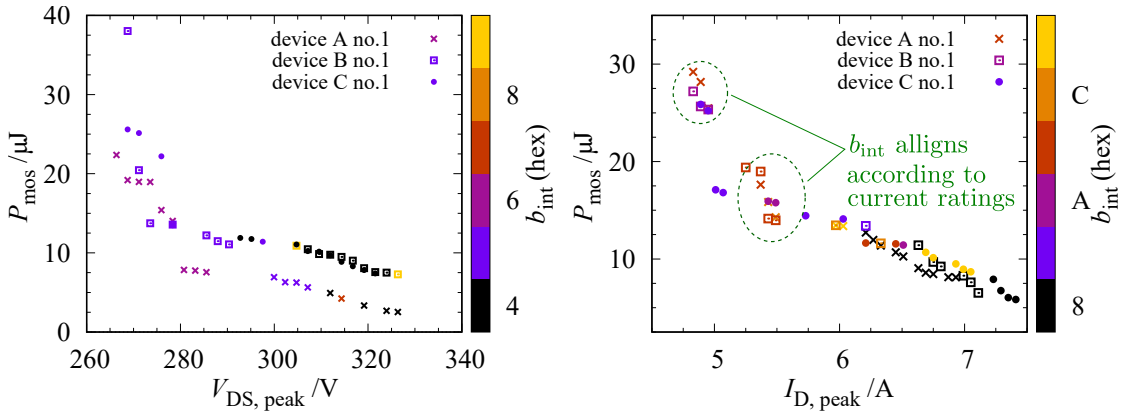


(a) Pareto-front solutions at turn-off. (b) Pareto-front solutions at turn-on.

Figure 3.15: Optimization results for SiC MOSFETs of the same model.

Table 3.5: Selected devices and their parameters extracted from the datasheets.

Device	Model	Ratings	V_{th}	R_{on}
device A	SCT2450KE	1200 V, 10 A	2.8 V (Typ.)	450 mΩ
device B	SCT2160KE	1200 V, 16 A	2.8 V (Typ.)	160 mΩ
device C	SCT2080KE	1200 V, 40 A	2.8 V (Typ.)	80 mΩ



(a) Pareto-front solutions at turn-off. (b) Pareto-front solutions at turn-on.

Figure 3.16: Optimization results for SiC MOSFETs with different current ratings.

ferent colors. From the solutions circled around $I_{\mathrm{D,peak}} = 4.8\,\mathrm{A}$ and around $I_{\mathrm{D,peak}} = 6\,\mathrm{A}$, it is found that the device no. 3 clearly shows lower-bit solutions. It implies that V_{plateau} of device no.3 is relatively lower than the other three, so that the V_{th} is smaller.

Next, we investigate the three models of SiC MOSFET of the same series with different current ratings. The selected devices are listed in Table 3.5. It is expected that V_{plateau} for the same operating condition becomes smaller as the current rating increases. The optimized solutions for these devices are shown in Fig. 3.16. The solutions around $I_{\mathrm{D,peak}} = 5\,\mathrm{A}$ and $I_{\mathrm{D,peak}} = 5.5\,\mathrm{A}$ show that a smaller b_{int} is selected for the device with a larger current rating. This does indicate the difference in V_{plateau} among these devices.

These results confirm that the proposed optimization approach is applicable regardless of the target device and also that the optimum solutions reflect the differences in the device parameters.

3.5 Summary

This chapter developed the GA-based optimization software for the DAGD system. The V_{GS} waveform of SiC MOSFETs was transformed into the target of the combinatorial

optimization problem. A digital-twin-compatible optimization system was configured, which interfaces both the simulation software and the experimental instruments. The system was verified both in the simulation and in the experiment. The optimized solutions were analyzed in relation to the I_{D}–V_{DS} curves of the device, which clearly described the effectiveness of the designated V_{GS} level on the switching characteristics. The orientation toward developing a digital-twin platform utilizing the physically associated simulation opens up the possibility for a conceptually new approach for adjusting the AGD operation, which is never feasible with analog technique. Additionally, the optimization was also performed for several different operating conditions and for different devices, verifying the flexibility to be applied to other applications without changing the hardware itself. The analysis of the obtained solutions indicated that the optimum solutions reflect the differences in the device parameters.

The developed software in this chapter aimed at obtaining Pareto-front solutions of the given power device in the initial condition, from which the user can choose the one that fits the application. The function of the software needs to be added or changed depending on the target of optimization. Chapter 5 investigates additional features to be added to the software, targeting the deviation from the initial condition of optimization.

Chapter 4

Application to parallel connection of SiC MOSFETs

The parallel connection of SiC MOSFETs is an important technique to process large currents in the power converter [80]. However, the mismatch of the device parameters and even the parasitic inductance among the parallel-connected power devices will lead to a disastrous imbalance of current-sharing performance [20, 21]. It can destroy the device immediately in extreme cases or, if not immediately, can also damage the device and the package in the long run, which will accelerate the imbalanced aging among the parallel-connected devices. It is expected that AGD will compensate for the mismatches instead, easing the restrictions on the design of circuit layouts and the selection of the devices [68, 81].

In this chapter, the applicability of DAGD for parallel operation of SiC MOSFETs is investigated. A new hardware configuration of DAGD is introduced using modular topology, which provides additional benefits compared to the prototype using resistor voltage division, which was presented in Chapter 2. The fabricated gate driver is applied to the switching test of parallel-connected SiC MOSFETs. The effectivity is investigated under the presence of mismatches of the device characteristics or the circuit layout.

4.1 Design of modular multi-level digital active gate driver

The configuration of DAGD proposed in Chapter 2 was taken directly from the configuration of binary-weighted resistor DAC, which consists of several switches connected in parallel. However, the voltage division using resistors generates a non-negligible loss in

the gate driver, making it inadequate for practical application. It also lacks the ability to control the gate voltage while the MOSFET is on, which would be beneficial in the parallel operation of SiC MOSFETs to balance the static current sharing. As another approach to achieving the binary-weighted multi-level topology, the series connection of binary-weighted voltage is investigated. Modular topology, as also seen in modular multi-level converters [82], is employed. The proposed configuration provides additional features to the DAGD system particularly suitable for paralleling of SiC MOSFETs. We call it the modular-multilevel DAGD (MMDAGD), the details of which are explained in the rest of this section.

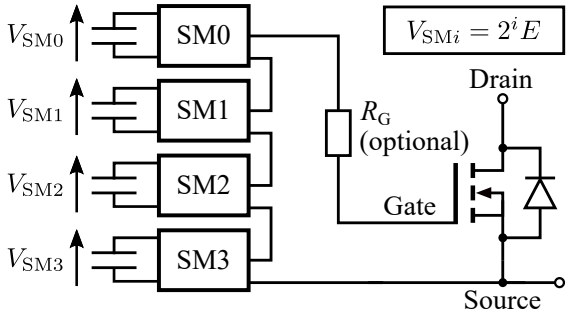
4.1.1 Concept and operation

Figure 4.1 (a) shows the overall schematic configuration of 4-bit MMDAGD. It consists of four submodules (SMi, $i \in \{0, 1, 2, 3\}$), which mainly consist of a half-bridge circuit with a submodule capacitor (C_{SM}). A binary-weighted submodule voltage of $V_{\mathrm{SM}i} = 2^i E\,[\mathrm{V}]$ is stored in each submodule capacitor. The output of SMi is shorted when the input signal (b_i) is 0, and is connected to $C_{\mathrm{SM}i}$ when b_i is 1. Hence, the output voltage of MMDAGD, or V_{GS}, is expressed as the sum of the output voltages of submodules as given by (4.1).

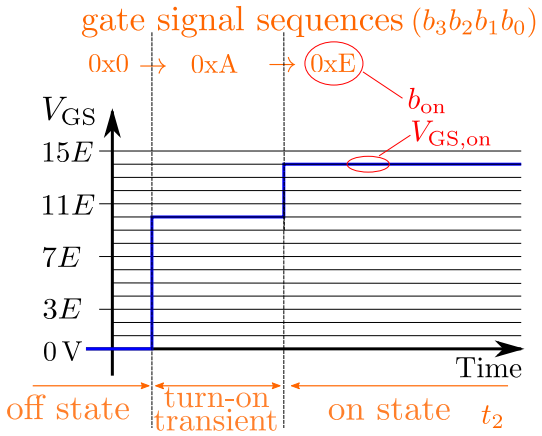
$$V_{\mathrm{GS}} = \sum_{i=0}^{3} b_i V_{\mathrm{SM}i} = \sum_{i=0}^{3} 2^i b_i E \tag{4.1}$$

V_{GS} waveform is shaped by switching these submodules successively during the switching transient. Figure 4.1 (b) shows an example of turn-on V_{GS} waveform generated by 4-bit MMDAGD, and Fig. 4.1 (c) describes the transition of submodules. Note that the gate signal is expressed as $b_3b_2b_1b_0$ and in hexadecimal numbers, where b_3 is MSB (SM3) and b_0 is LSB (SM0). During the off state, the gate signal is 0, which means that all the submodules are off. When the gate signal turns 0xA (1010), SM1 and SM3 are turned on, which gives the total voltage of $10E$ at the output. Lastly, the gate signal is changed to 0xE, yielding $14E$ at V_{GS}. In this manner, the time-series sequence of gate signals is converted into the 15-level V_{GS} waveform by piling up the binary-weighted voltages of the selected submodules. The successive modulation of V_{GS} is possible as is so with resistor DAGD proposed in Chapter 2. The time constant of these transitions can be adjusted by the external gate resistor R_{G}.

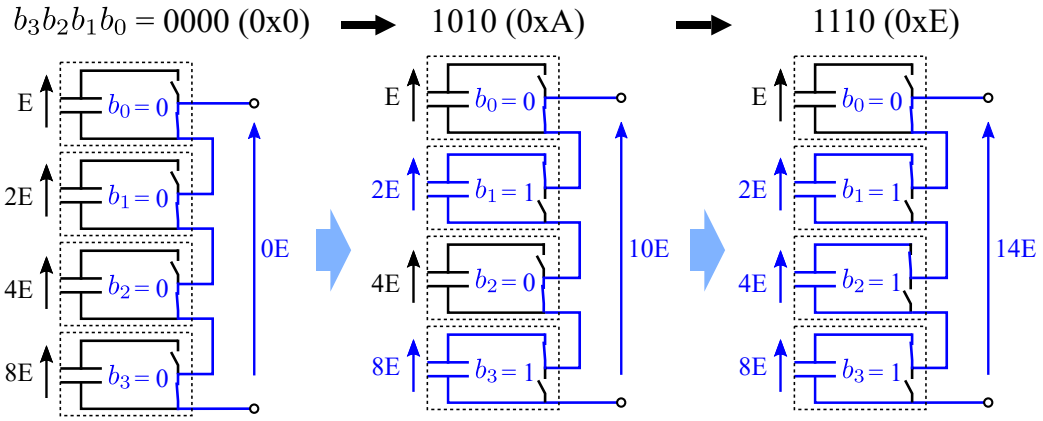
Another important feature of MMDAGD is that it can control $V_{\mathrm{GS,on}}$, which is a V_{GS} level applied during the MOSFET is in on-state, by changing the gate signal given during



(a) Configuration of 4-bit MMDAGD. Submodules with binary-weighted voltage capacitor are connected in series to provide 15 level gate-source voltage levels.



(b) Example of active V_{GS} waveform using MMDAGD at turn-on. Four-bit gate signal sequences are expressed in hexadecimal numbers (e.g., 0xE = 1110).



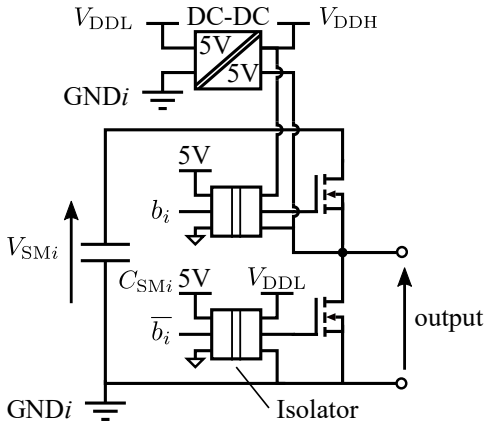
(c) Example of transition of submodules during turn-on.

Figure 4.1: Concept and operation of 4-bit MMDAGD. © 2023 IEEE.

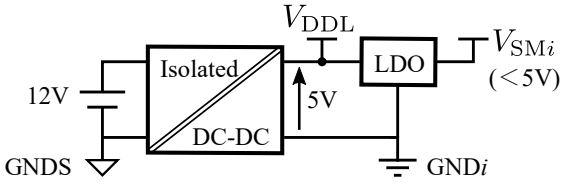
the period (b_{on}) as shown in Fig. 4.1 (b). It is known that on-resistance (R_{on}) of SiC MOSFETs can be controlled by $V_{GS,on}$, as can also be understood from Eq. (1.4). If several devices with different values of R_{on} are connected in parallel, the static-current distribution can be balanced by adjusting b_{on}.

4.1.2 Submodule configuration

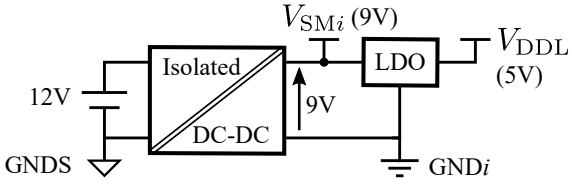
Figure 4.2 (a) shows the schematic configuration of a submodule (SMi), where GNDi indicates the reference ground of the submodule. Its output stage is composed of a half-bridge circuit of n-type Si MOSFETs. They are driven by the input signal b_i, which is transferred



(a) Configuration of output stage.



(b) V_{SMi} and V_{DDL} generation ($V_{\mathrm{SM}i} < 5\,\mathrm{V}$).



(c) V_{SMi} and V_{DDL} generation ($V_{\mathrm{SM}i} = 9\,\mathrm{V}$).

Figure 4.2: Schematic configuration of submodules (SMi) © 2023 IEEE.

through digital isolators with 5 V output. The output of the low-side isolator is powered by V_{DDL}, which is referenced from GNDi, while that of high-side isolators is powered by V_{DDH}, which is generated from V_{DDL} using another 5 V-to-5 V type isolated DC-DC converter. The deadtime between the high-side and low-side signals are determined to be 5 ns, which is generated externally.

The half-bridge circuit is connected to the submodule capacitor C_{SMi} with V_{SMi} generation circuit. As each submodule needs to be floating from others considering the operating principle, each $V_{\mathrm{SM}i}$ is supplied using an isolated DC-DC converter. In the prototype configuration shown in this paper, the submodule voltages are set as $V_{\mathrm{SM0}} = 1.25\,\mathrm{V}$, $V_{\mathrm{SM1}} = 2.25\,\mathrm{V}$, $V_{\mathrm{SM2}} = 4.5\,\mathrm{V}$, and $V_{\mathrm{SM3}} = 9.0\,\mathrm{V}$, respectively, which gives the maximum V_{GS} value of 17 V. For SM0, SM1, and SM2, V_{SMi} is generated using 5 V output DC-DC converter, which is then regulated using a low-drop-out (LDO) regulator, as shown in Fig. 4.2 (b). The 5 V is also supplied as V_{DDL}. For SM3, V_{SM3} is taken directly from the 9 V-output of the DC-DC converter as shown in Fig. 4.2 (c). An LDO regulator is also utilized to obtain V_{DDL}.

It should be noted that V_{SM} can be as small as 1 V or less to achieve precise adjustment of V_{GS}. In such a case, the use of p+n type complementary MOSFETs with shared gate signal is not beneficial; the gate signal line cannot be shared because, assuming the gate signal swing is from 0 to 5 V, the gate-source voltage of the p-type MOSFET would swing between -1 and 4 V, which is not sufficient for its operation. It is also not possible to use commercial gate driver ICs as submodules because the under-voltage lock-out feature

prevents the operation at low values of $V_{\mathrm{SM}i}$. These are the reasons to use n-type dual MOSFETs as the half-bridge with two isolated gate signals.

4.1.3 Comparison with resistor DAGD and other existing topologies

So far, we have developed two hardware topologies to achieve the DAGD operation, namely the resistor DAGD proposed in Chapter 2 and MMDAGD proposed in this chapter. The resistor DAGD is configured with parallel-connected n-bit gate drive circuits, which operate using a single DC power supply, as shown in 2.1. However, the generation of digitized voltage through resistor division generates non-negligible loss at the gate drive circuit, greatly losing its practicality and potential to be integrated. On the other hand, MMDAGD is designed by a series connection of n-bit gate drive circuits (submodules). Although each submodule requires a floating DC power supply, which adds to the circuit complexity, there is no resistive component used for the generation of digitized voltage, significantly reducing the loss in its operation. It also has the additional feature of adjusting $V_{\mathrm{GS,on}}$. Considering these differences, MMDAGD is considered an upgraded realization of DAGD hardware, particularly in terms of functionality.

Similar ideas of configuring a gate driver through the series connection of submodules are also found in [62, 83]. The major difference between MMDAGD and the modular AGDs proposed in the literature [62, 83] is that every submodule has a different value of submodule voltage. This feature enables the DAC-like operation featuring readily available 15 V_{GS} levels, adding to the flexibility of the V_{GS} shaping. The expansion of the configuration is also possible by re-configuring the submodule voltages or adding another. Particularly, adding a negative-bias submodule will be useful for applications in need of cross-talk suppression [84, 85].

4.1.4 Fabricated MMDAGD

Figure 4.3 shows the prototype of 4-bit MMDAGD, which is designed using discrete components and fabricated on a four-layer PCB. As recognized in Fig. 4.3, the half-bridge MOSFETs and submodule capacitors are placed compactly, while signal isolators and DC-DC converters take up much of the space of the PCB surface. It is expected that most of the components will be integrated into a chip eventually.

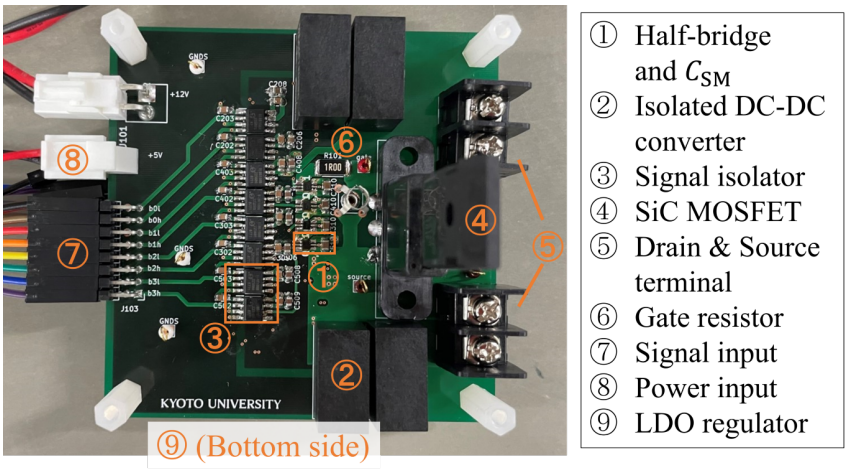


Figure 4.3: Photograph of prototype MMDAGD. © 2023 IEEE.

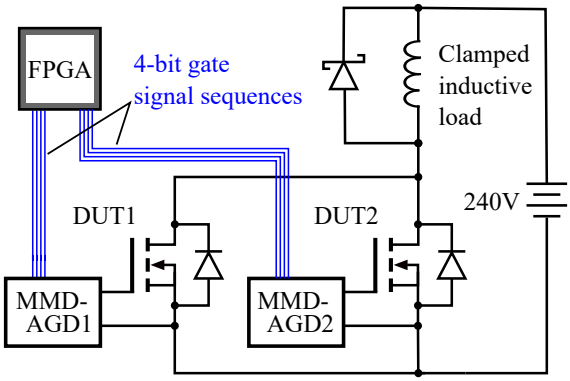


Figure 4.4: Schematic diagram of double-pulse switching test circuit with two parallel-connected SiC MOSFETs. © 2023 IEEE.

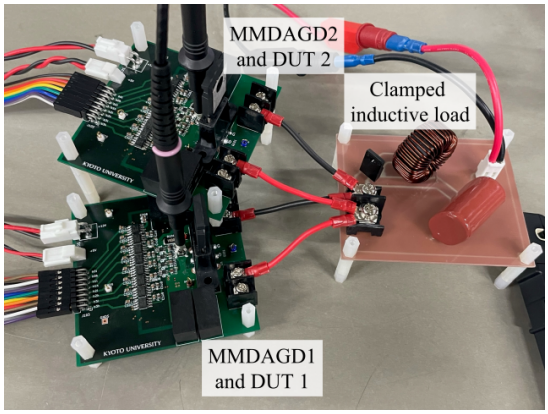


Figure 4.5: Photograph of the test circuit. © 2023 IEEE.

4.2 Current-balancing of parallel-connected SiC MOSFETs

The operation and effectiveness of MMDAGD are experimentally verified in the current balancing of parallel-connected SiC MOSFETs, focusing on the switching behavior at the turn-on. Figure 4.4 shows the schematic diagram of the test circuit, and Fig. 4.5 shows the photograph of the test setup. A standard double-pulse switching testing circuit is adopted with a clamped inductive load consisting of a SiC Schottky-barrier diode (SCS206AM, ROHM Co., Ltd.) and an inductor of 300 μH. Two SiC MOSFETs (device-under-test: DUT) are connected in parallel (DUT1 and DUT2), each of which is driven

by MMDAGD. The gate signal sequences for each MMDAGD are generated by an FPGA (Zynq UltraScale+ MPSoCs, Xilinx Inc.), whose clock rate of the output signals is set at 200 MHz. The operating condition is set at 240 V and 6 A, which is split to 3 A for each DUT in an ideal operation. The difference in wire length between DUT1 and DUT2 is as minimized as possible to exclude the influence of layout difference on the switching behavior of the two DUTs. The drain current (I_D) and V_{GS} of the two DUTs are measured using current probes and voltage probes (TCP0020 and TPP0200, Tektronix Inc.), and the waveform is acquired in an oscilloscope (MDO4104, Tektronix Inc.).

4.2.1 Selection of DUTs with parameter variations

We selected three DUTs based on the measurements of I_D–V_{GS} characteristics using a curve tracer (custom-made, IWATSU Electric Co., Ltd.). Figure 4.6 shows the measured I_D–V_{GS} curves and V_{th} of the three DUTs. Devices A and B have almost the same characteristics with $V_{th} \sim 3.25$ V, while device C has clearly different characteristics with $V_{th} \sim 2.66$ V. Such differences in the device characteristics are often found in commercial SiC power MOSFETs due to the process variation [35]. We prepare two cases, one with matched devices and one with mismatched; devices A and B are adopted as DUT1 and DUT2 in case 1, while devices A and C are adopted in case 2.

The influence of these differences on the parallel operation is first investigated. Fig. 4.7 shows the turn-on switching waveforms in each case without AGD operation, where the gate signal is changed from 0000 to 1111. From Fig. 4.7 (a), it is found that I_D is equally balanced both dynamically and statically in parallel operation of matched devices. On the other hand, in Fig. 4.7 (b), DUT2 turns on faster than DUT1, leading to the dynamic imbalance. It is also shown that the static current is not shared equally due to the difference in R_{on}, as the device C with smaller V_{th} takes larger current.

4.2.2 Balancing current-sharing using AGD

We now activate the AGD operation to improve the current-sharing performance and also to suppress the overshoot of I_D. The AGD sequences are searched manually via try-and-error.

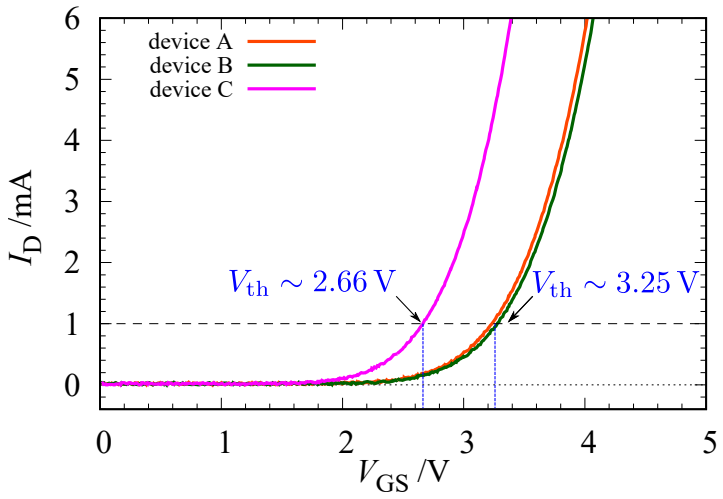
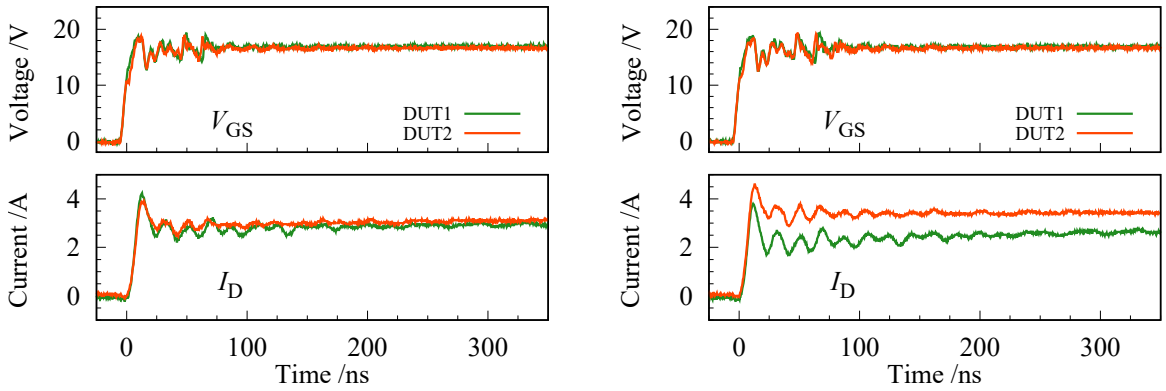


Figure 4.6: I_D–V_{GS} characteristics and V_{th} (at $I_D = 1\,\mathrm{mA}$) of selected DUTs measured at $V_{DS} = 10\,\mathrm{V}$.



(a) case 1 (DUT1: device A, DUT2: device B). (b) case 2 (DUT1: device A, DUT2: device C).

Figure 4.7: Turn-on switching waveforms without AGD. The gate signals are changed as 0x0 → 0xF. © 2023 IEEE.

Parallel connection of matched devices

Firstly, the AGD is applied to case 1. Figure 4.8 show the switching waveforms of two DUTs, which are driven using the same AGD sequence (AGD i). The switching waveforms without AGD are also shown for reference. The I_D waveforms of two devices are consistent under the AGD operation and the overshoot is decreased. Therefore, for parallel operation of matched devices, the overshoot can be suppressed by adopting the same AGD sequence without interfering with the originally balanced current-sharing.

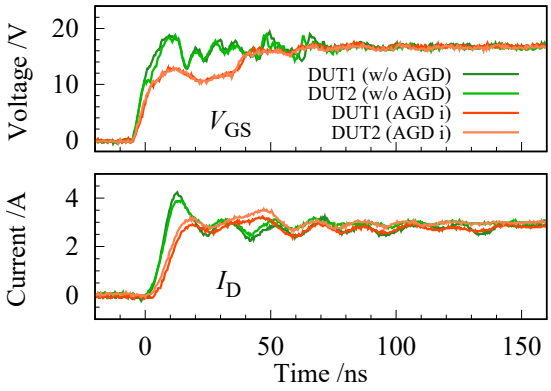
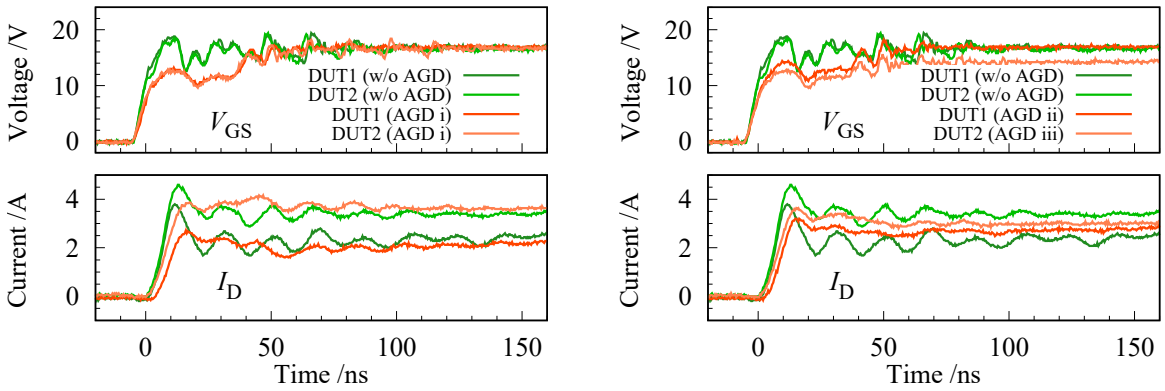


Figure 4.8: Turn-on switching waveforms in case 1 with AGD and without AGD. AGD i: 0x0 → 0xA (40 ns) → 0xF. © 2023 IEEE.



(a) Same AGD sequence is applied. AGD i: 0x0 → 0xA (40 ns) → 0xF.

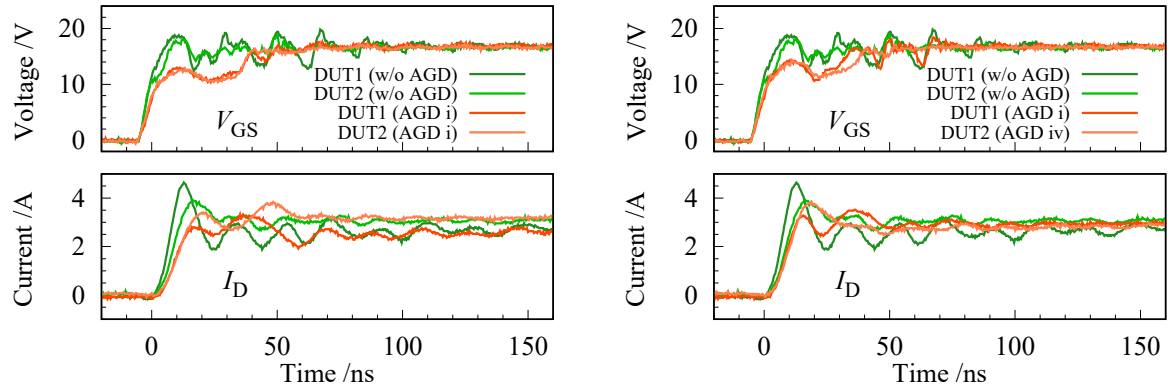
(b) Individually-adjusted AGD sequence is applied. AGD ii: 0x0 → 0xB (40 ns) → 0xF. AGD iii: 0x0 → 0xA (40 ns) → 0xD.

Figure 4.9: Turn-on switching waveforms in case 2 with AGD (orange) and without AGD (green). © 2023 IEEE.

Parallel connection of mismatched devices

Secondly, the AGD is applied to case 2. Figure 4.9 (a) shows the switching waveforms when the same AGD sequence (AGD i) is applied to both devices. Although the overshoot is suppressed slightly, the dynamic and static imbalance still remains. Consequently, the AGD sequence needs to be adjusted individually to mitigate these differences. As DUT2 takes a larger current in both durations, it is expected that the relative increment of dynamic and static gate voltage levels for DUT1 would help mitigate the imbalance.

Figure 4.9 (b) shows the switching waveforms using adjusted AGD sequences, which



(a) Same AGD sequence is applied. AGD i: 0x0 → 0xA (40 ns) → 0xF.

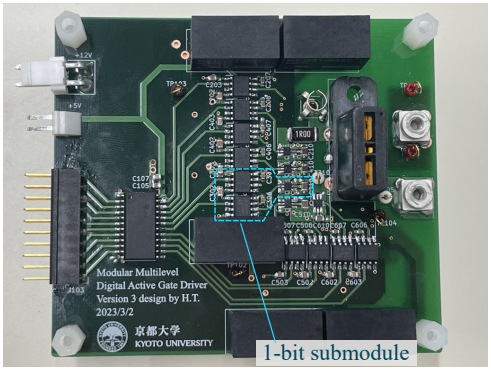
(b) Individually-adjusted AGD sequence is applied. AGD i: 0x0 → 0xA (40 ns) → 0xF. AGD iv: 0x0 → 0xA (35 ns) → 0xF.

Figure 4.10: Turn-on switching waveforms in case 1 with different wire lengths. © 2023 IEEE.

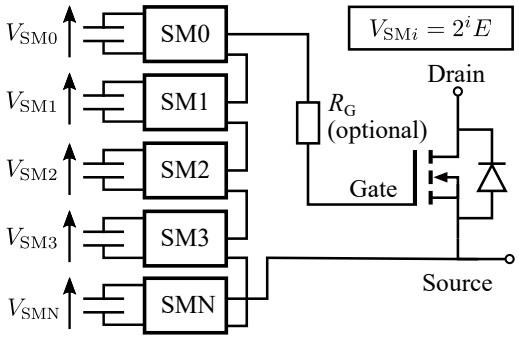
have 1-bit difference during the transient state 2-bit difference during the steady state. It is confirmed now that the current-sharing performance is improved both dynamically and statically, with the static current difference decreased from 1 A to 0.2 A.

4.2.3 Parallel connection with mismatched layout

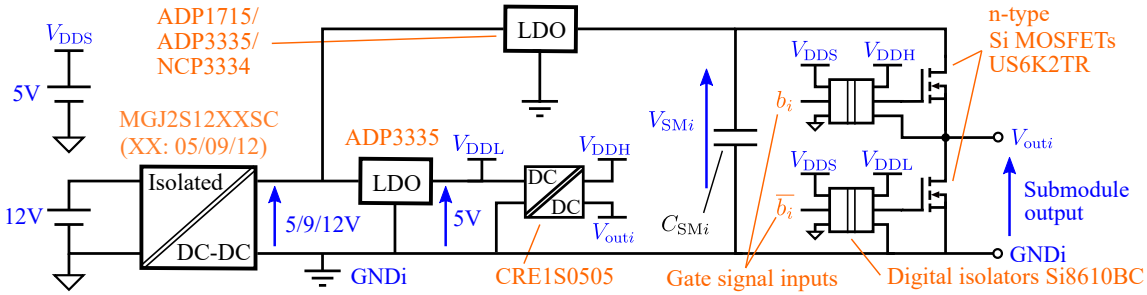
Additionally, we investigate a scenario with an mismatched layout. The pair of case 1 is adopted, but the length of both wires between the DUT2 and the test circuit is changed. Figure 4.10 shows the switching waveforms of the DUTs in different wire length for DUT2. It is confirmed that as the imbalance appears as the differences in wire length increases, which is attributed to the mismatched inductance in the power loop. Figure 4.10 (a) shows the switching waveform without AGD and with AGD i, which was effective in case 1 (Fig. 4.8). The I_D waveforms now do not overlap each other without AGD, and the application of the same AGD sequence does not help the imbalance to decrease. Accordingly, the AGD sequence is individually adjusted as shown in Fig. 4.10 (b), and the current-sharing performance is improved. These results confirmed that the MMDAGD can also be applied to improve the current-sharing in the presence of mismatched circuit layout, which will ease the restriction in the placement of parallel-connected power devices.



(a) Photograph of MMDAGD board (front side view).



(b) Simplified diagram ($E = 1.25\,\mathrm{V}$, $V_{SMN} = 2.5\,\mathrm{V}$).



(c) Detailed schematic configuration of i-th submodule (SMi). Different sets of DC-DC converters and LDOs are used depending on V_{SMi}. Additionally to the schematic, a signal buffer (SN74ABT827DW, Texas Instruments) is used at the input port of gate signals.

Figure 4.11: Schematic configuration of 4-bit MMDAGD with a negative module.

4.3 Improved configuration of MMDAGD

This section provides the improved design of MMDAGD. Figure 4.11 shows the photograph and schematic configuration of the improved design. Besides the layout improvements to minimize the gate current path and the board area, some additional functions have been adopted.

Firstly, an accurate binary weighting of submodule voltages is achieved by the adoption of the same circuit topology for every submodule. The submodule voltages are set at 1.25 V, 2.5 V, 5.0 V, and 10.0 V, which gives the maximum V_{GS} level of 18.75 V. Different pairs of the DC-DC converter and the LDO regulator are used depending on the submodule voltage, as shown in Fig. 4.11 (c).

Secondly, an additional submodule to generate negative gate voltage is connected

inversely in series with the 4-bit modules. The negative gate voltage of $-2.5\,\mathrm{V}$ can be additionally generated only for a partial period of the whole switching event to prevent the self-turn-on of the power device. This feature would be particularly beneficial in applications where the risk of cross-talk phenomenon should be avoided, such as in the bridge configuration.

4.4 Summary

This section experimentally verified the applicability of the DAGD system to the parallel operation of SiC MOSFETs, targeting the imbalance in current-sharing among the devices. An upgraded circuit configuration of DAGD hardware to achieve DAC operation was designed using modular topology, providing additional functions to control both the dynamic and the static behavior of the switching operation. MMDAGD was applied to the balancing of current-sharing in parallel-connected SiC MOSFETs. The prototype of 4-bit MMDAGD was fabricated using discrete components, and its operation was confirmed. It was verified that MMDAGD can simultaneously balance the device current, both dynamically and statically, while suppressing the current overshoots. The experiment was performed in several different scenarios where the difference in the device characteristics or the circuit layout inherently exists. It was shown that the imbalance can be mitigated by adopting a unique V_{GS} waveform for each device. Lastly, based on the confirmed operation, an improved circuit configuration of MMDAGD was designed for use in the following chapter.

The imbalances targeted in this chapter are attributed mainly to the inherent variations of the device parameters. On the other hand, they may also appear *a posteriori* due to the aging of the device. Detecting these changes and adjusting the AGD operation would be essential techniques to fulfill the potential of AGDs. This aspect is further investigated in Chapter 5.

Chapter 5

Update of AGD pattern against uncertainties

So far in this dissertation, the effectiveness of DAGD in a fixed initial condition has been verified, as an optimization in a given condition was performed in Chapter 3, and the inherent variation of the device parameters in parallel operation was targeted in Chapter 4. However, the performance of the pre-defined optimum AGD pattern is vulnerable to uncertainties that cause deviation from the initial condition. We particularly put the focus on the uncertain changes in device characteristics that appear after the circuit implementation. It is known that after prolonged or highly stressed use, the device parameters could shift and change its performance [38, 86]. To maintain the performance of AGD under these changes, its operation needs to be adjusted at some point during the operation. This is impossible for analog AGDs as their operation is fixed by the hardware design, but can be realized by digital AGDs by re-shaping the AGD pattern. Such an updating scheme of optimum AGD pattern would be a beneficial function of software for the DAGD system.

This chapter develops an updating scheme of the optimum AGD pattern by taking a metaheuristics approach to search for the best-effort solution without knowing the factor that caused the changes. The developed scheme is verified experimentally in a boost converter operation, where the change of the device characteristics is simulated.

5.1 Target of optimization

The updating scheme is investigated by applying DAGD to a boost converter, which is one of the standard configurations of the switched-mode DC-DC converters [87]. MMDAGD

proposed in Chapter 4 is applied to drive the SiC MOSFET installed in the converter. An updating scheme of the optimum AGD pattern is developed as a function of the software for the DAGD system. While there exist other factors that cause the deviation from the initial condition, such as the load current or the device temperature, this section particularly targets the long-term shift of device parameters, which is one of the major concerns for SiC MOSFETs [88–90]. As proven in the previous chapters, the distinctive advantage of the DAGD system is that it can implement a metaheuristics approach to adjust the AGD operation after the circuit implementation. This advantage is beneficial for dealing with the shift of device parameters as they are hard to model and also hard to measure during the operation of power converters. For simplicity, we assume a step-wise parametric shift of the device characteristics.

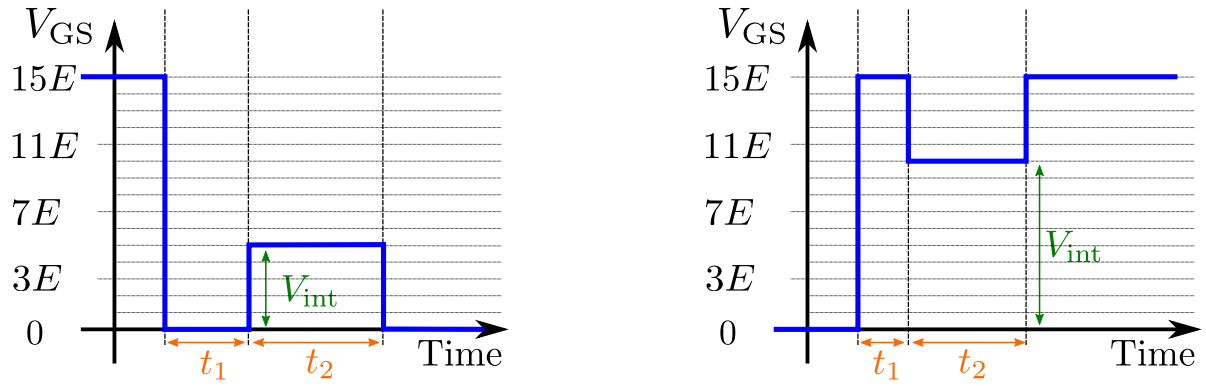
5.1.1 Requirement for the software

While the multi-purpose optimization to obtain the Pareto-front AGD patterns has been performed in Chapter 3 and also in several publications [61, 70, 71, 91], the cost function needs to be single-purpose to perform the automatic selection of optimum AGD pattern without the user's interaction. Additionally, a proper cost function needs to be set to select the optimum solution considering several aspects of switching behavior. When using several indices to evaluate the switching characteristics, there exists a set of Pareto-front solutions as confirmed in Chapter 3. To maintain the AGD performance under the shift of device parameters, it is expected that the cost function chooses the suitable solution out of the Pareto-front solutions considering, regardless of its shape.

5.1.2 Parameters for shaping gate voltage waveform

The AGD pattern is expressed using a vector so that it can be handled by the optimization algorithm. Figure 5.1 shows the target V_{GS} waveform, which is expressed using a vector $\boldsymbol{v} = (a, b, c)$. Here, the parameters a, b, and c are integers that determine the waveform parameters according to Eq. (5.1).

$$\begin{cases} V_{\mathrm{int}} = a \times 1.25\,[\mathrm{V}] & \mathrm{a} \in \{0,\ 1,\ 2,\ ...,\ 14{,}15\} \\ t_1 = b \times 2.5\,[\mathrm{ns}] & \mathrm{b} \in \{0,\ 1,\ 2,\ ...,\ 14{,}30\} \\ t_2 = c \times 10\,[\mathrm{ns}] & \mathrm{c} \in \{0,\ 1,\ 2,\ ...,\ 14{,}30\} \end{cases} \tag{5.1}$$



(a) Turn-off. (b) Turn-on.

Figure 5.1: AGD patterns using three parameters.

5.2 Updating scheme of AGD pattern using ABC algorithm

Several approaches could be taken for metaheuristics swarm intelligence or population-based optimization problems [92]. The genetic algorithm (GA) was used in Chapter 3 for its high efficiency in searching the solution space to obtain the Pareto-front solutions. However, GA is not suitable for the purpose of this chapter because it inevitably tries numerous unsuccessful solutions spreading across the entire solution space, which may frequently degrade the performance of the power converter during the search process. Assuming that the new optimum solution in the changed condition is not far from the initial optimum solution, the local-search-based algorithm is preferred. We apply the Artificial Bee Colony (ABC) algorithm for the search of the optimum AGD pattern, which has been developed inspired by the bees' collective behavior to search for a better food source [93]. It holds several candidates for the optimum solution while performing local searches around them. This is the preferred behavior of optimization for the purpose of this chapter. It also has applicability to time-varying problems [94], which has similarities with the updating problem of the AGD pattern. The essential parts of the algorithm are briefly described in this section, while more details can be found in [93].

5.2.1 Main body of the algorithm

The main body of the ABC algorithm is constructed based on [93] and modified to add the updating scheme. Figure 5.2 shows the flowchart of the updating scheme, whose objective

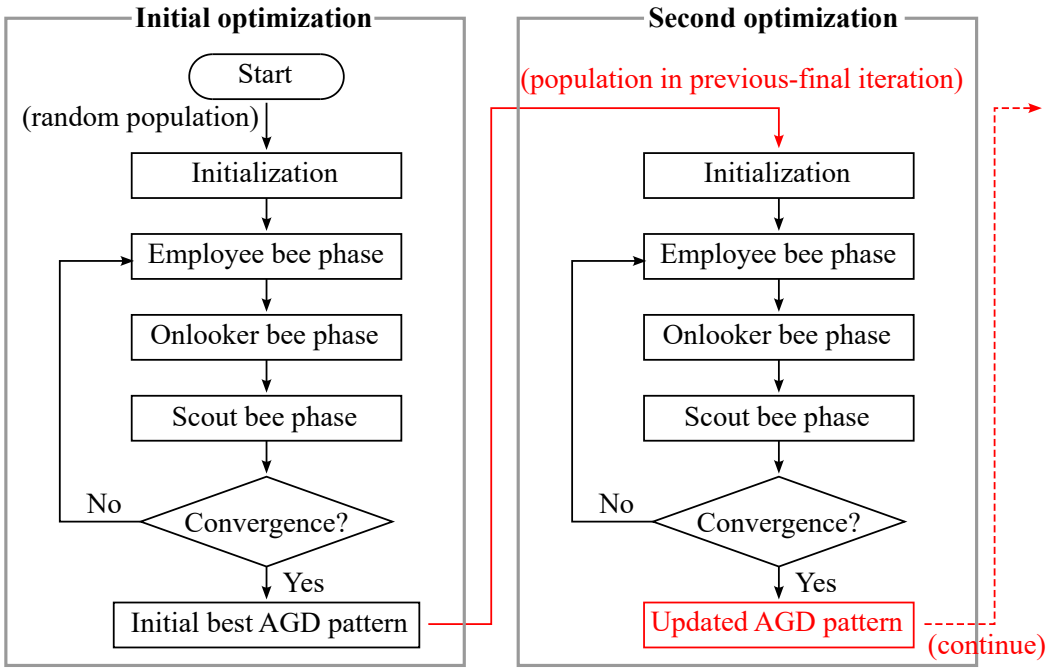


Figure 5.2: Flowchart of ABC-algorithm-based optimization and updating scheme for MMDAGD in continuous operation.

is to maximize the fitness of the bees. An initial population of N vectors is generated randomly at the beginning, and the fitness f_i $(i = 1, 2, ..., N)$ of each vector is evaluated. The following three stages are the main searching operations of the ABC algorithm.

The first one is the employee bee phase, where a local search is performed for every bee in the population. Each bee selects a neighborhood solution based on its memorized vector $(\boldsymbol{v}_i)$ and evaluates its fitness. A candidate neighborhood vector of the i-th bee $(\boldsymbol{v}_i{}')$ is given by Eq. (5.2).

$$\boldsymbol{v}_i{}' = \mathrm{round}\big(\boldsymbol{v}_i + \phi(\boldsymbol{v}_i - \boldsymbol{v}_k)\big) \tag{5.2}$$

Here, $k \in [1, N]$ is a random integer except i, $\phi \in [-1, 1]$ is a random number, and round$(\cdot)$ is a function to round off each component of the vector. The memorized vector is updated if the fitness of the new vector is better than the memorized one.

The second stage is the onlooker bee phase, which is also repeated for the same number as the previous phase. In this phase, one of the vectors in the population is selected by roulette wheel selection based on their probability p_i, which is calculated by its fitness as given by Eq. (5.3).

$$p_i = \frac{f_i}{\Sigma_{n=1}^{N} f_n} \tag{5.3}$$

A neighborhood solution of the selected vector is searched and evaluated in the same manner as in the employee bee phase. This way, the neighborhood of vectors with higher fitness is intensively searched in this stage.

The third stage is the scout bee phase. If the fitness of a bee has not been updated for five iterations, it turns a scout bee with a randomly generated vector, and its fitness is evaluated.

The convergence is judged by whether the best fitness is not updated for more than 5 consecutive iterations or if the number of iterations exceeds the limit of 15. The optimization in the initial condition ends at this point, and the best bee vector is used as the initial best AGD pattern.

The second optimization is initiated deliberately or automatically by detecting the change in fitness or any other unforeseen event. This time, the bee vectors that belong to the population in the last iteration of the previous optimization are reused as the initial population instead of randomly generated vectors. This would help the quick convergence because those vectors would be a set of semi-optimum vectors in the previous condition, supposing that the optimum vector in the next condition is not far from that in the last condition. Again, the three phases of the ABC algorithm are repeated, and the best vector is updated for the changed condition. The maximum iteration of the second optimization is set at five, meaning that no scout bee phase is used. The best bee after the second optimization is used as the updated AGD pattern.

As it inevitably takes some time for the optimization process, a sudden change of conditions or a shift of conditions with a long enough time constant is supposed to be the target of the updating scheme, such as the long-term degradation of the power device. For fast-changing conditions that are known in advance or predicted precisely, including alternating load current, there exists another strategy in the literature such as the use of a look-up table to choose the right pattern for the given operating current [54].

5.2.2 Cost function for evaluating AGD performance

A cost function evaluates the AGD performance, or the fitness, based on the switching characteristics, such as the overshoot of drain voltage (V_{DSpeak}) or drain current (I_{Dpeak}) and the switching loss, which can be substituted with the converter loss in case of DC-DC converters in the steady-state. The following two indices of normalized overshoot $\tilde{x}$ and normalized converter loss $\tilde{y}$ are used for its calculation, which are represented

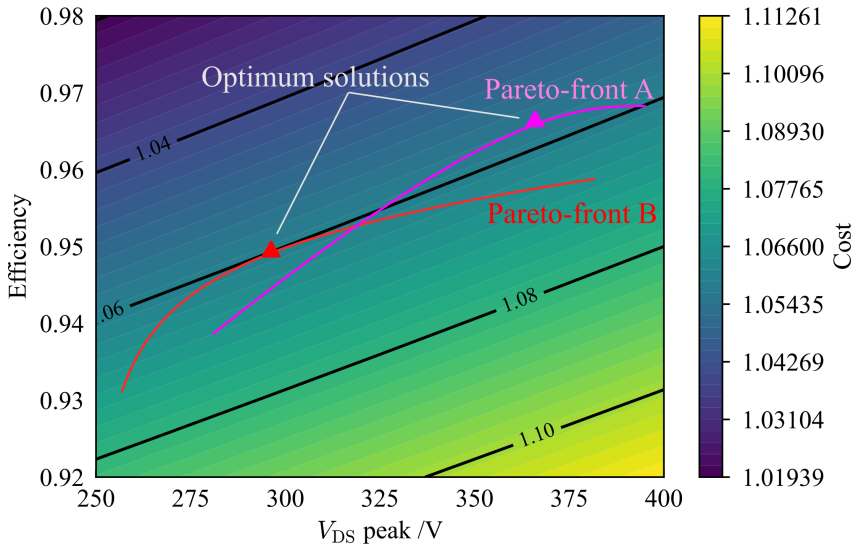
as $\tilde{x} = V_{\mathrm{DSpeak}}/V_{\mathrm{DSnom}}$ for turn-off and $\tilde{x} = I_{\mathrm{Dpeak}}/I_{\mathrm{Dnom}}$ for turn-on, and $\tilde{y} = 1/\eta$. Here, V_{DSnom} and I_{Dnom} represent the nominal operating condition of V_{DS} and I_{D} for the MOSFET, and η represents the efficiency of the converter.

Single-purpose optimization function of simple addition has been adopted in the literature, using two or three indices such as normalized switching loss, overshoot of voltage/current, di/dt or dv/dt, and ringing, with weighting coefficients [34, 48, 54, 56]. Figure 5.3 (a) shows an example of a heat map of a cost function with a simple addition of $\tilde{x}$ and $\tilde{y}$. The selection of the weighting coefficients, namely the gradient of the cost function surface, is critical to obtain the ideal AGD operation, which is defined as the tangent point between the Pareto-front solutions and the surface. However, without the knowledge of the shape of the Pareto-front, this cost function has a limited ability to guide the optimum solution to a particular region, such as below some level of overshoot, which would be beneficial from the designer's point of view. It is also not clear whether the coefficients need to be changed in response to the change in the operating conditions, which may end up selecting extreme solutions depending on the shape of the Pareto-front curve.

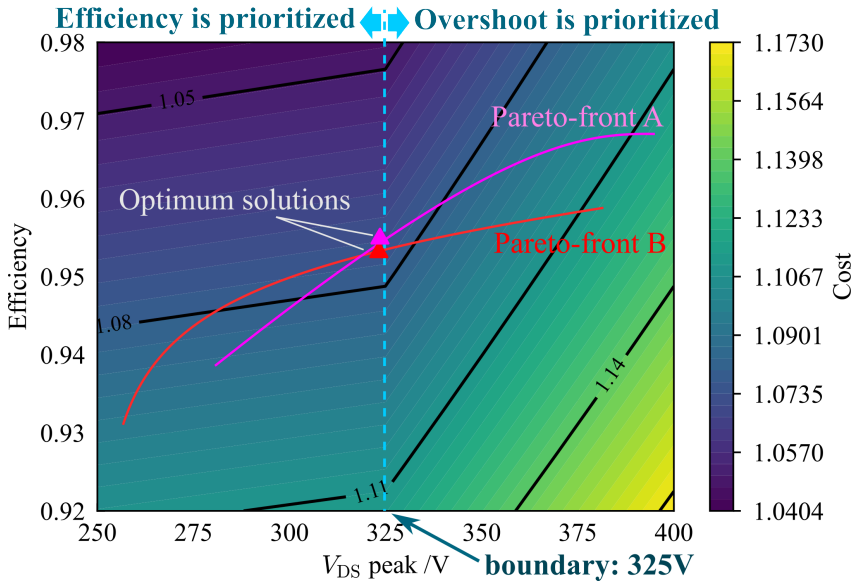
As an improvement, we introduce a pice-wise linear cost function that explicitly sets a boundary for the overshoot, as given by Eq. (5.4).

$$C(\tilde{x}, \tilde{y}) = \begin{cases} \alpha_1 \tilde{x} + \tilde{y} & \tilde{x} < \tilde{x}_{\mathrm{bound}} \\ \alpha_2 \tilde{x} + \tilde{y} + (\alpha_1 - \alpha_2)\tilde{x}_{\mathrm{bound}} & \tilde{x} \geq \tilde{x}_{\mathrm{bound}} \end{cases} \tag{5.4}$$

Here, the normalized variable $\tilde{x}_{\mathrm{bound}}$ denotes the user-configurable boundary for the overshoot, which is given by $\tilde{x}_{\mathrm{bound}} = V_{\mathrm{DSbound}}/V_{\mathrm{DSnom}}$ for turn-off and $\tilde{x}_{\mathrm{bound}} = I_{\mathrm{Dbound}}/I_{\mathrm{Dnom}}$ for turn-on. The parameters α_1 and α_2 denote the weighting coefficient used under and above the boundary. By setting α_1 a small value and α_2 a large value, the suppression of overshoot is prioritized above the boundary, while the reduction of loss is prioritized under the boundary. Figure 5.3 (b) shows an example of a heat map of the proposed cost function. It is indicated that the proposed cost function can selectively define the desired device characteristics to be achieved by the optimum AGD pattern regardless of the shape of the Pareto-front solutions. The weighting coefficients of $\alpha_1 = 0.02$ and $\alpha_1 = 0.2$ are used in the following experiment. As $C(\tilde{x}, \tilde{y})$ given by Eq. (5.4) is larger than 0 and takes a value of around 1, its reciprocal is used as the fitness f_i.



(a) Simple cost function: $C(\tilde{x}, \tilde{y}) = 0.05\tilde{x} + 0.95\tilde{y}$.



(b) Cost function $C(\tilde{x}, \tilde{y})$ given by Eq. (5.4), where $\alpha_1 = 0.02,\ \alpha_1 = 0.2,\ x_{\text{bound}} = 325\,\text{V}$.

Figure 5.3: Heat maps of cost functions for evaluating AGD performance (at turn-off operation).

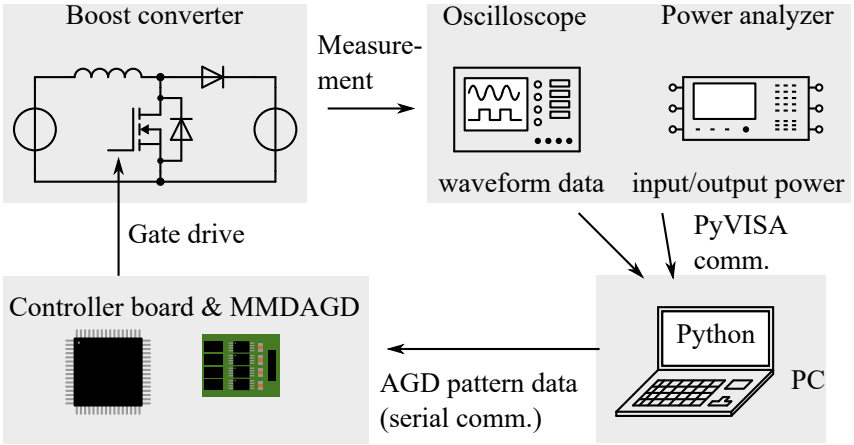


Figure 5.4: Illustration of optimization process in the experiment.

5.2.3 Implementation of the scheme

The proposed scheme is implemented using laboratory experimental apparatus. The main algorithm runs on Python on the user's PC, which interacts with the controller and the measurement instruments. The core part of the Python program is obtained and modified from an open-source Python source code for ABC algorithm, which is available online [95].

Figure 5.4 illustrates the flow of the optimization process. We assume the power converter is operating in a steady state. The PC sends a new AGD pattern to the controller through serial communication, which is then applied to MMDAGD installed in the converter to change the switching behavior of the SiC MOSFET. Measurements are done with an oscilloscope and a power analyzer after a waiting of several seconds for the measured value to stabilize. The data of the switching waveform and input/output power of the converter are transferred to the PC through PyVISA communication, where the cost of the applied AGD pattern is calculated. These procedures are repeated for each searching operation shown in Fig. 5.2.

5.3 Experimental verification of updating scheme

This section provides the experimental verification of the proposed scheme. MMDAGD is installed in a boost converter operated in the continuous-current mode, and the updating scheme is employed during its operation. After obtaining the initial best solution, the condition is forcibly changed to trigger the second optimization to update the best AGD pattern.

5.3.1 Experimental setup

Figure 5.5 shows the schematic configuration of the boost converter, whose operating condition is summarised in Table 5.1. The fabricated circuit is shown in Fig. 5.6. A SiC MOSFET (SCT3120AL, ROHM Co., Ltd.) is selected as the device-under-test (DUT) and is driven by a MMDAGD. A SiC Schottky barrier diode (SCS310AH, ROHM Co., Ltd.) is used as the rectifier. They are cooled using heat sinks and DC fans to keep the surface temperature of the SiC MOSFET package stable at around 60 °C during the operation. An electric load (LN-300C, KEISOKU GIKEN Co., Ltd.) and high-power wire-wound resistors (TE1000B Series, TE connectivity) configure the variable-resistance load R_{out} set at 100 Ω. These settings give the nominal switching condition for the DUT as $V_{\mathrm{DSnom}} = 250\,\mathrm{V}$ and $I_{\mathrm{Dnom}} = 6.25\,\mathrm{A}$, which are used in the calculation of cost function.

The switching waveforms are measured using an oscilloscope (MDO4104-3, Tektronix Inc.) and probes: V_{GS} is measured with a 1 GHz passive prove (TPP1000, Tektronix Inc.), V_{DS} with a 200 MHz high-voltage differential probe (THDP0200, Tektronix Inc.), and I_{D} and I_{L} with 50 MHz AC/DC current probes (TCP0020, Tektronix Inc.). A power analyzer (WL1806E, Yokogawa Electric Corp.) measures I_{in}, V_{in}, I_{out} and V_{out} to calculate the input and output power of the converter.

5.3.2 Initial optimization

Firstly, the initial optimization is performed using a randomly-created initial population. The boundary parameters for the overshoots used in Eq. (5.4) are set at $V_{\mathrm{DSbound}} = 320\,\mathrm{V}$ and $I_{\mathrm{Dbound}} = 8.5\,\mathrm{A}$. During the optimization process of either turn-off or turn-on, the other one is always done without AGD so that the condition for the optimization does not change.

Figure 5.7 shows the optimization results at turn-off. Figure 5.7 (a) shows the distribution of the 20 solutions in the last iteration with their costs indicated by the color bar. It is confirmed the overshoot of V_{DS} is suppressed below the boundary of 320 V when using the best AGD pattern, while the efficiency has dropped by about 0.5 % compared to the most efficient case but with the largest overshoot (without AGD). Figure 5.7 (b) shows the switching waveforms of V_{GS}, V_{DS}, and I_{D} using the best AGD pattern compared to those without AGD. The designated switching pattern for the best AGD is also shown as a reference. An intermediate voltage level of 6.25 V is set during V_{DS} rises to suppress

Table 5.1: Operating conditions of boost converter.

I_{in}	V_{in}	I_{out}	V_{out}	Duty	f_{SW}
6.25 A	100 V	2.5 A	250 V	60 %	250 kHz

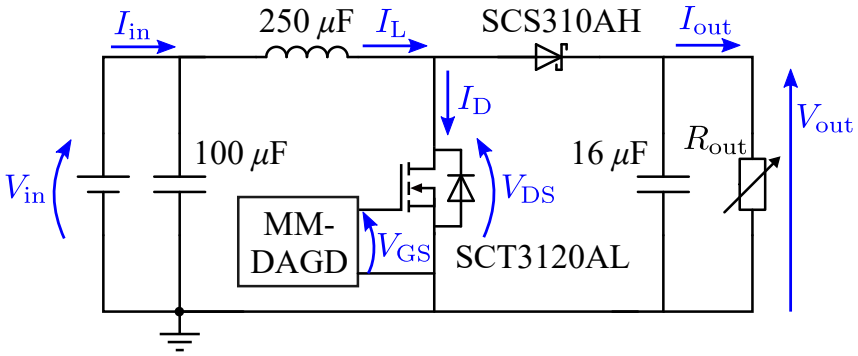


Figure 5.5: Schematic configuration of boost converter. MMDAGD is installed to drive the main SiC MOSFET.

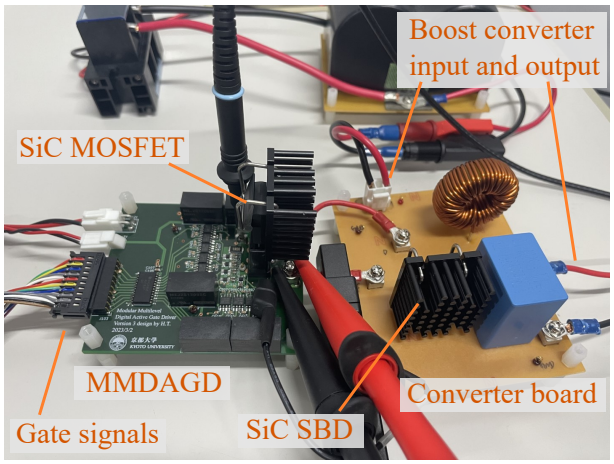
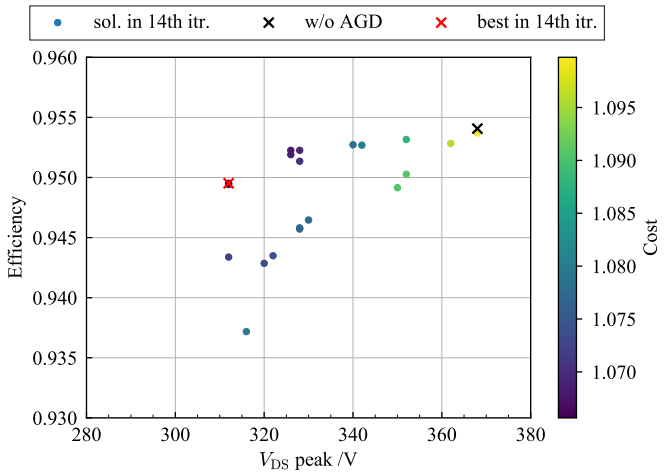


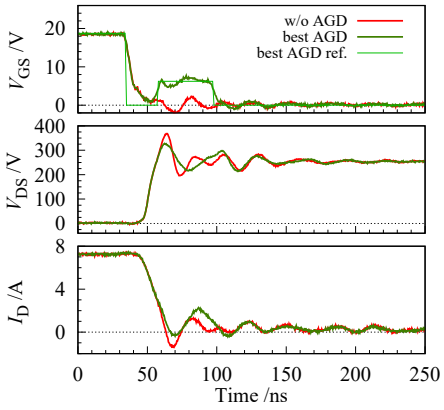
Figure 5.6: Photograph of boost converter with MMDAGD.

the overshoot.

Figure 5.8 (a) shows the optimization results at turn-on. The best AGD pattern achieves the overshoot of I_D below 8.5 A at an efficiency drop of around 0.5 %. The proposed cost function with switched weighting coefficients successfully selected the most efficient solution under the boundary of overshoot despite the Pareto-front solutions forming an almost linear distribution. Figure 5.8 (b) shows the switching waveforms using the

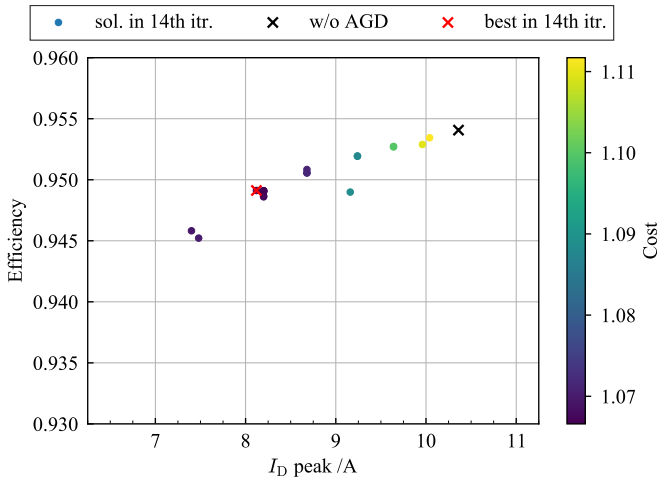


(a) Switching characteristics and costs of solutions in final iteration.

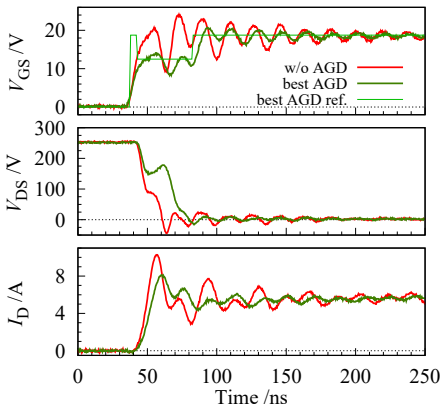


(b) Switching waveforms of V_{GS}, V_{DS}, and I_D without AGD and with the best AGD pattern.

Figure 5.7: Results of initial optimization at turn-off ($V_{DSbound} = 320\,V$).



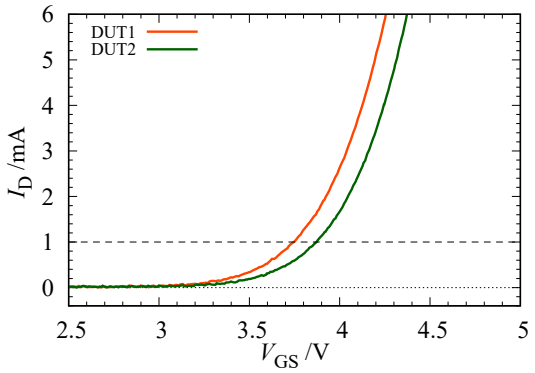
(a) Switching characteristics and costs of solutions in final iteration.



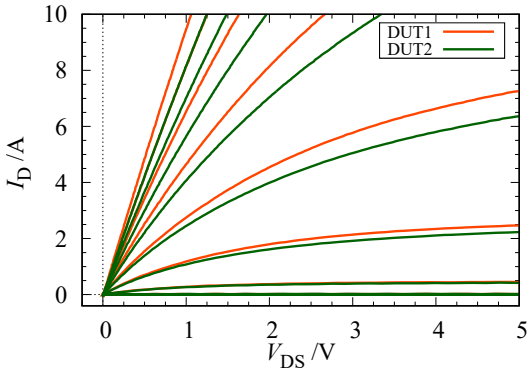
(b) Switching waveforms of V_{GS}, V_{DS}, and I_D without AGD and with the best AGD pattern.

Figure 5.8: Results of initial optimization at turn-on ($I_{Dbound} = 8.5\,A$).

best AGD pattern, where an intermediate voltage level of 12.5 V suppresses the overshoot of I_D.



(a) I_D–V_{GS} characteristics at $V_{DS} = 10\,\mathrm{V}$.



(b) I_D–V_{DS} characteristics at $V_{GS} = 1, 3, ..., 17, 19\,\mathrm{V}$.

Figure 5.9: Measured device characteristics of the two DUTs.

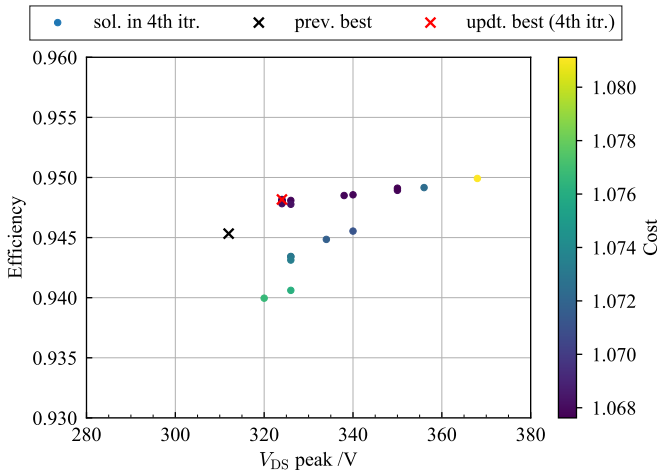
5.3.3 Updating of optimum AGD pattern

Next, the device characteristics are deliberately changed to perform the update of the optimum AGD pattern. Due to the difficulty of performing suitable aging of the same device, we simulated the change by replacing the DUT with another device of the same model but with different device parameters. Figure 5.9 shows the device characteristics of the original DUT (DUT1) and replacing DUT (DUT2), which are measured using a semiconductor curve tracer (custom-made, IWATSU Electric Co., Ltd.). DUT2 has larger V_{th} compared to DUT1, and the I_D–V_{DS} curves are shifted as that of DUT1 at $V_{DS} = 17\,\mathrm{V}$ almost overlaps with that of DUT2 at $V_{DS} = 19\,\mathrm{V}$.

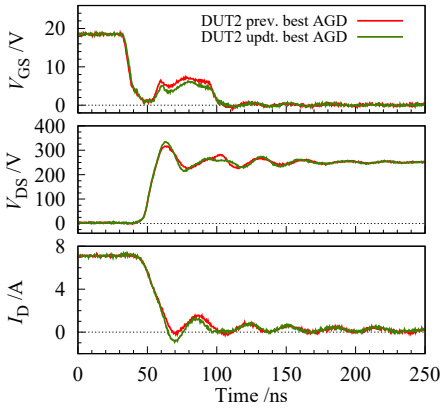
The second optimization is performed at the same boundary condition. The best AGD patterns and other solutions in the final iteration shown in Fig. 5.7 and Fig. 5.8 are utilized as the new initial population. We stopped the operation of the boost converter, swapped the DUTs, restarted the boost converter operation again using the previous best AGD pattern, and waited for a long enough time for the converter operation to stabilize. Then, the second optimization process was initiated, starting from the turn-off optimization.

Figure 5.10 shows the results at turn-off. In Fig. 5.10 (a), the switching performance using the previous-best AGD pattern is shown with a black cross, which is still lower than the boundary, but the efficiency is reduced due to the shift of the device characteristics. The updated optimum AGD pattern after five iterations, shown with a red cross, successfully improved the efficiency while complying with the boundary constraint.

Figure 5.11 shows the optimization results at turn-on. Figure 5.11 (a) indicates that

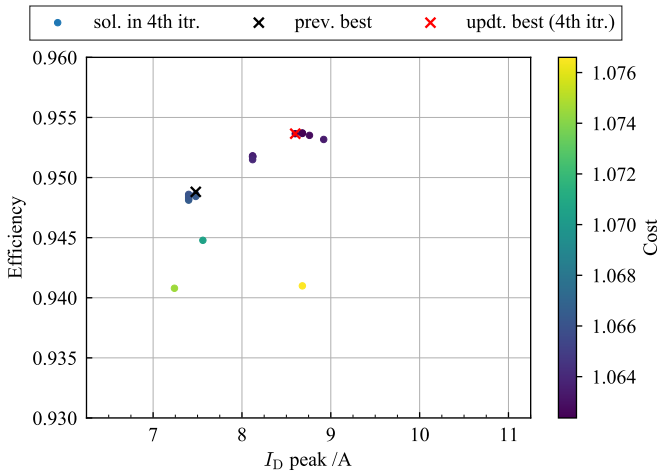


(a) Switching characteristics and costs of solutions in final iteration.

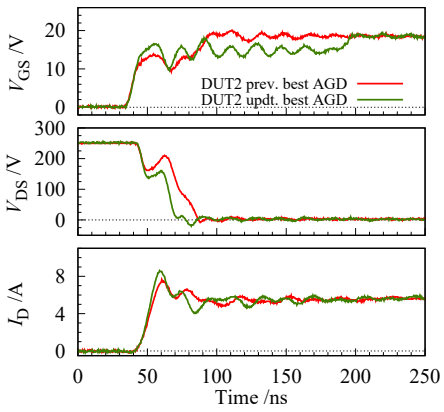


(b) Switching waveforms of V_{GS}, V_{DS}, and I_D with previous-best and updated AGD patterns.

Figure 5.10: Results of second optimization at turn-off after the DUT is replaced.



(a) Switching characteristics and costs of solutions in final iteration.



(b) Switching waveforms of V_{GS}, V_{DS}, and I_D with previous-best and updated AGD patterns.

Figure 5.11: Results of second optimization at turn-on after the DUT is replaced.

the previous best solution suppresses the overshoot of I_D excessively that the efficiency is largely sacrificed. This corresponds to the shift of I_D–V_{DS} curves; DUT2 has a lower saturation current compared to DUT1 at the same V_{GS} level, meaning that it has more impact on the limitation of drain current and, thus, on the overshoot suppression. These changes are also confirmed in the switching waveforms as shown in Fig. 5.11 (b). On

the other hand, the updated optimum AGD pattern achieves the overshoot near the boundary and an efficiency of 0.7 % higher than the previous best solution. The updated AGD pattern selects a higher V_{GS} level during the turn-on transient to compensate for the shift in device characteristics essentially.

These results indicated the importance of choosing the appropriate AGD pattern for the power device, even for the same model number. The proposed scheme for the AGD pattern worked as expected to update the old solution with the new one, maintaining the performance of AGD during the operation of the power converter. The results add to the particular advantage of the DAGD system that can heuristically compensate for unforeseen deviations from the initial condition without actually modeling or measuring the changes.

5.4 Summary

This chapter investigated the updating scheme of the optimum AGD pattern for DAGD to maintain its performance in the presence of unforeseen changes. The ABC algorithm was adopted as the main body of the scheme to utilize its high efficiency in the heuristic local search. A modified cost function is introduced to set a boundary for the amount of permitted overshoot. The proposed scheme is applied to a boost converter in a continuous operation. The parametric shift of device characteristics is simulated by replacing the DUT with a device of the same model number with a parametric variation. It was verified that the previous-optimum AGD pattern is not optimum anymore under the simulated change and that the proposed scheme successfully updated it within a small number of iterations. The proposed scheme further cultivated the advantage of the DAGD system to modify their optimum pattern during the continuous operation of power converters in response to the deviation from the initial condition. This aspect will be an important element of software for the DAGD system for the further development of aging-aware and variation-aware gate driving of SiC power MOSFETs.

Chapter 6

Conclusions and future directions

This dissertation aimed at developing a digital active gate drive system for SiC power MOSFETs. The core elements of the system, the hardware and the software, have been developed. Its advantages have been clarified in several applications where SiC MOSFETs face particular challenges in practical application. The developed system is visualized as shown in Fig. 6.1. This chapter summarizes the contributions from each chapter.

6.1 Summary of contribution

Chapter 1 introduced the research background and the aim of this thesis. The basic understanding of SiC power MOSFETs and its challenges were introduced, followed by a brief review of AGD techniques in the literature. The orientation toward the digitization of the AGD technique was discussed.

Chapter 2 investigated the concept of the digital active gate driver for SiC MOSFETs by developing the hardware. The prototype of DAGD is designed based on the architecture of the binary-weighted resistor DAC. The fundamental concept of DAGD to shape the V_{GS} waveform using a multi-bit gate signal sequence was confirmed. Experimental results showed that the transient switching behavior of the SiC MOSFET can be controlled via the operating points corresponding to the designated V_{GS} levels. It was also verified that the surge voltage can be suppressed by the adjustment of the gate signal sequence. Based on the confirmed operation, an improved configuration of DAGD using GaN HEMTs was designed.

Chapter 3 investigated the software for DAGD to optimize the switching characteristics of SiC MOSFETs. GA was adopted as the optimization algorithm, taking V_{GS}

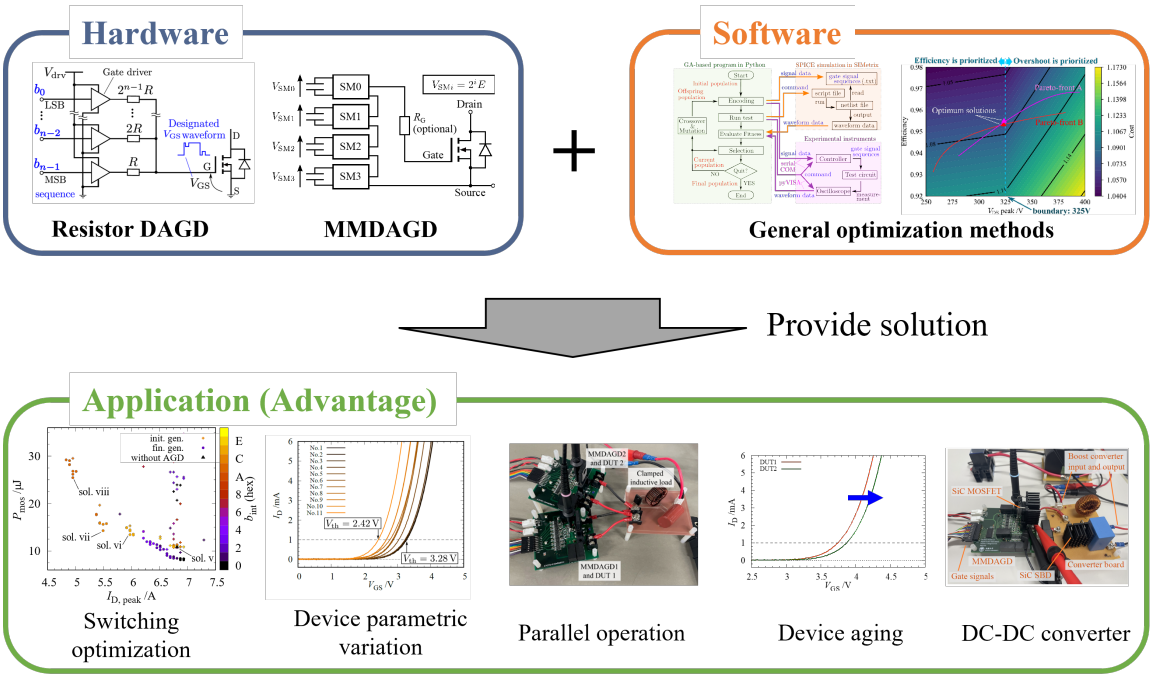


Figure 6.1: Visualization of developed digital active gate drive system.

waveform as the target of the combinatorial optimization problem. A Python-based optimization tool was developed, which has the digital-twin compatibility to interface both the simulation software and the experimental apparatus. The system was verified both in the simulation and in the experiment, successfully obtaining the set of optimum gate signal sequences. The optimized solutions were analyzed in relation to the I_{D}–V_{DS} curves of the device, which clearly described the effectiveness of the designated V_{GS} level on the switching characteristics. The optimization was also performed for several different operating conditions and for different devices, which indicated that the optimum solutions reflect the differences in the device parameters.

Chapter 4 aimed at the application of DAGD system into the parallel operation of SiC MOSFETs. MMDAGD was designed as a new hardware for DAGD system to provide additional functions to control both the dynamic and the static behavior of the switching operation. MMDAGD is applied to the balancing of current-sharing in parallel-connected SiC MOSFETs. The experiment was performed in several different scenarios where the inherent difference in the device characteristics or the circuit layout exists. It was verified that the dynamic and static current-sharing performance was improved by the adoption of individually-adjusted V_{GS} waveforms.

Chapter 5 investigated the performance of DAGD system in the presence of unforeseen changes. An updating scheme of the AGD pattern was developed to maintain its performance by adopting the ABC algorithm as the main body of the scheme. A suitable cost function is introduced to define the optimum switching behavior to be achieved by AGD. The proposed scheme was verified in a boost converter, where the shift of device parameters of SiC MOSFET is simulated. It was confirmed that the previous-optimum AGD pattern is not optimum anymore under the simulated change, and that the proposed scheme successfully updated it to regain the performance.

6.2 Future directions

In addition to the fundamental feature of DAGD system provided in this thesis, there still remains room for improvements and additional investigations to add to its practicality and utility. This section discusses several future directions that the author would like to point out.

The first direction is the expansion in the application of the DAGD system. The parallel operation of multiple SiC MOSFETs would be one of the future work to Chapter 4. It is obvious that the difficulty of achieving current-balancing is increased as more number of devices are concerned. A software function to perform computational optimization of multiple-paralleled SiC MOSFETs would be an advantageous application of DAGD. The applicability of DAGD in DC-DC converter was verified in Chapter 5. Application to more advanced topology with a higher degree of freedom, such as full-bridge configuration as seen in the motor drive applications and even the multi-level converters operating more number of power devices, would be one of the future challenges to show the practicality of the DAGD system.

Secondly, it can be pointed out that the studies in this dissertation were carried out in rather ideal environments, where the conditions other than the topic of the investigation were kept the same. In Chapters 2, 3, and 4 the switching operation was carried out in the switching test circuit where the condition for each switching operation was kept exactly the same, and in Chapter 5, the boost converter was operated at a steady state with a stable DC source and a constant load. These environments do not reflect the actual environment where the SiC power devices are applied, as more and more uncertainties would be present. The metaheuristics optimization scheme presented in Chapter 5 can be

utilized for a stepwise change that is hard to measure, such as the long-term parametric shift of the device characteristics. On the other hand, there exist parameters that are rather easily acquired, such as the load current with the use of current sensors. As the dependence of AGD pattern on the load current was clarified in Chapter 3, this adjustment may be done with a simple feedback control. The classification and development of software functions against the targeted phenomena will be required to design the DAGD system for practical applications.

Lastly, the utilization of the digital-twin structure needs to be worked on. In Chapter 3, the use of the AGD pattern obtained in simulation into the real power device was addressed. Inversely, it would be beneficial if the results obtained from the real power device could be utilized to adjust the simulation model. For example, the results of Chapter 5 indicated that the parametric shift of the device characteristics can be obtained as the change in the optimum AGD pattern. It could potentially be utilized to diagnose the condition of the power devices if we could adjust the parameters of the device model to match the change observed in the real power device. This orientation would be one of the keys to realizing a complete digital-twin system for SiC MOSFETs that enhances the better handling of their switching behavior.

Appendix A

Derivation of Equation (2.1)

This chapter derives Eq. (2.1) in Section 2.1. $R_{\rm on}$ and $R_{\rm off}$ used in Eq. (2.1) are given by Eq. (A.1) and Eq. (A.2), respectively.

$$R_{\rm on} = \left(\sum_{j=0}^{n-1} \frac{b_j}{2^{n-1-j}R} \right)^{-1} \tag{A.1}$$

$$R_{\rm off} = \left(\sum_{j=0}^{n-1} \frac{\overline{b_j}}{2^{n-1-j}R} \right)^{-1} \tag{A.2}$$

Using these expressions, Eq. (2.1) is derived as Eq. (A.3).

$$\begin{aligned}
V_{\rm GS} &= \frac{R_{\rm off}}{R_{\rm on}+R_{\rm off}} V_{\rm drv} \\
&= \frac{\left(\sum_{j=0}^{n-1} \frac{\overline{b_j}}{2^{n-1-j}R} \right)^{-1}}{\left(\sum_{j=0}^{n-1} \frac{b_j}{2^{n-1-j}R} \right)^{-1} + \left(\sum_{j=0}^{n-1} \frac{\overline{b_j}}{2^{n-1-j}R} \right)^{-1}} V_{\rm drv} \\
&= \frac{\left(\sum_{j=0}^{n-1} \overline{b_j} 2^j \right)^{-1}}{\left(\sum_{j=0}^{n-1} b_j 2^j \right)^{-1} + \left(\sum_{j=0}^{n-1} \overline{b_j} 2^j \right)^{-1}} V_{\rm drv} \\
&= \frac{\sum_{j=0}^{n-1} b_j 2^j}{\sum_{j=0}^{n-1} \overline{b_j} 2^j + \sum_{j=0}^{n-1} b_j 2^j} V_{\rm drv} \\
&= \frac{\sum_{j=0}^{n-1} b_j 2^j}{\sum_{j=0}^{n-1} 2^j} V_{\rm drv}
\end{aligned} \tag{A.3}$$

Appendix B

Selection procedure of generic algorithm

This chapter gives an additional description of the selection algorithm used in the optimization system developed in Chapter 3. The selection procedure of NSGA-II [76] utilizes two indices, namely the non-domination rank and the crowding distance, to sort the population based on their fitness. A solution being non-dominated refers to a state where there is no solution whose at least one of the fitness values is better (smaller) than those of the solution. The solutions in $\mathcal{F}_0$ (rank 0) are non-dominated by any other solutions, while those in $\mathcal{F}_k$ (rank k) are non-dominated if ignoring the solutions belonging to all the fronts with lower ranks, as shown in Fig. B.1. The crowding distance of a solution is calculated by taking the sum of the side length of a cuboid composed between the two neighboring solutions of the same front, as also shown in Fig. B.1 [76]. This distance is used to select a set of well-spread individuals in the lastly-added front $\mathcal{F}_i$ so that the total size of the next generation population P_{t+1} is kept at N.

The selection procedure performed in the flowchart shown in Fig. 3.3 is given by Algorithm B.1. Here, P_t denotes the population of t-th generation, Q_t denotes its offspring, $\mathcal{F} = \{\mathcal{F}_0, \mathcal{F}_1, ...\}$ denotes a group of fronts classified by their non-domination rank, and N is the size of the population. With this algorithm, the next generation individuals are selected from the closest to the Pareto-front, with descending order in crowding distance. Further details can also be found in [76, 78].

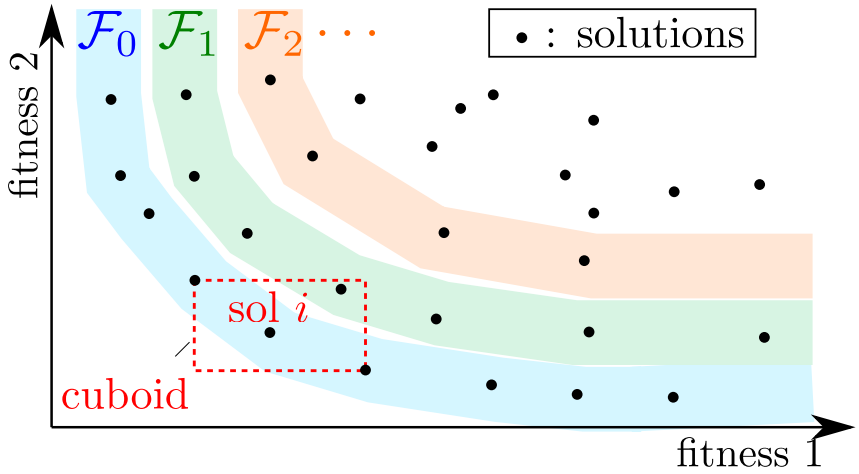


Figure B.1: Illustrations of solutions sorted by non-domination rank and example of cuboid for sol. i in $\mathcal{F}_0$. © 2023 IEEE.

Algorithm B.1 Selection procedure of NSGA-II.

$R_t = P_t \cup Q_t$
$\mathcal{F} = \mathsf{fast\text{-}non\text{-}dominated\text{-}sort}(R_t)$
$P_{t+1} = \emptyset$ and $i = 0$
while $|P_{t+1}| + |\mathcal{F}_i| < N$ do
    $\mathsf{assign\text{-}crowding\text{-}distance}(\mathcal{F}_i)$
    $P_{t+1} = P_{t+1} \cup \mathcal{F}_i$
    $i = i + 1$
$\mathsf{sort}(\mathcal{F}_i)$ # according to crowding distance
$P_{t+1} = P_{t+1} \cup \mathcal{F}_i[0 : (N - |P_{t+1}|)]$

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