Novel Rectenna Design Methods for Wireless Power Transfer Systems

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Abstract

This thesis presents the novel design methods for high-efficiency rectennas and second harmonic reradiation rectennas for wireless power transfer systems. The rectifying diode's theoretical rectification efficiency limits a rectenna's maximum rectification efficiency. Therefore, achieving a high-efficiency rectenna requires minimizing losses in the diode's surrounding circuitry and maximizing the diode's theoretical rectification efficiency. In this study, two methods are proposed to reduce the losses in the diode's surrounding circuitry: (1) a design method for single shunt rectifier circuits that achieve matching with the output filter, and (2) a design method for directly connecting the receiving antenna and the rectifying circuit. Additionally, by applying method (2), a rectenna that reradiates the second harmonic was developed. This thesis mainly describes three research outcomes that we conducted.

First, we propose a new structure for the single-shunt rectifier circuit, which can reduce circuit loss and achieve higher efficiency than conventional structures. The proposed structure can match the impedance of measurement equipment (or the receiving antenna) without conventional matching circuits, such as stubs and tapers. In the proposed structure, rectification and impedance matching are achieved simultaneously by placing a feeding point on the $\lambda/4$ line of the output filter. Circuit simulations compared the conventional and proposed structures' RF–dc conversion efficiency and circuit loss. The results indicated that the proposed structure has lower circuit loss and higher RF–dc conversion efficiency than the conventional structure. We fabricated the proposed rectifier circuit using a GaAs Schottky barrier diode. Both simulation and measurement results demonstrated that the proposed structure of the single-shunt rectifier circuit can rectify and match impedance. The fabricated rectifier circuit achieved a maximum RF–dc conversion efficiency of 91.0%, setting a world record for 920-MHz band rectifier circuits.

Second, we introduce a novel single-diode rectenna that enhances RF–dc conversion efficiency through harmonic control of the antenna impedance. We employ source-pull simulations encompassing the fundamental frequency and its harmonics to achieve a highly efficient rectenna. The results of these simulations delineate the source-impedance ranges required for enhanced efficiency at each harmonic. Based on the source-pull simulation results, we designed two inverted-F antennas with input impedances within and outside these identified source impedance ranges. Experimental results show that the proposed rectenna achieves a maximum RF–dc conversion efficiency of 75.9% at the fundamental frequency of 920 MHz, an input power of 10.8 dBm, and a load resistance of 1 kΩ. This efficiency is higher than the comparative rectenna without harmonic control of the antenna impedance. We demonstrate that the proposed rectenna achieves high efficiency through the direct connection of the antenna and the single diode, along with harmonic control of the antenna impedance.

Finally, we propose a rectennas design method that provides high RF–dc conversion effi-

ciency and enhanced second harmonic reradiation levels by employing source-pull simulation with harmonics. Reusing harmonics generated by a rectenna is advantageous in retrodirective systems because harmonic reradiation can serve as a battery-less pilot signal. In this retrodirective system, it is essential for the rectenna to effectively reradiate harmonics while maintaining high RF–dc conversion efficiency. The proposed design method enables a rectenna to facilitate second harmonic reradiation without additional filters. Source-pull simulation was conducted on a single-series rectifier circuit, revealing the correlation between RF–dc conversion efficiency and second harmonic reradiation levels, with specific source impedance values at each harmonic. An inverted-F antenna with a short-circuit stub on the back side was designed based on the source-pull simulation results. The designed rectenna achieves an RF–dc conversion efficiency of 60.6% and a second harmonic reradiation level of 0.17 dBm at a frequency of 920 MHz, with an input power of 10.0 dBm and a load resistance of 1.0 kΩ. This design performs significantly better than previous designs regarding harmonic reradiation level while maintaining high RF–dc conversion efficiency.

Our proposed novel structure of the single-shunt rectifier circuit can reduce the matching loss, resulting in higher efficiency. Our proposed novel single-series rectenna can achieve higher efficiency, and its design method using source-pull simulation with harmonics helps develop a highly efficient rectenna. Additionally, our developed novel single-series rectenna, which reradiates the second harmonic, can be used in retrodirective systems, utilizing the second harmonic as the pilot signal. Therefore, by applying the outcomes of this thesis, we can expect to design highly efficient rectennas that optimize diode efficiency and develop highly efficient retrodirective systems.

Contents

Chapter 1

General introduction

This thesis presents the novel design methods for high-efficiency rectennas (receiving antennas and rectifier circuits) and second harmonic reradiation rectennas for wireless power transfer (WPT) systems. Proposed methods contribute to the development of high-efficiency rectennas. This chapter begins with a historical overview of WPT, underscoring the importance of rectenna research. This chapter then delves into previous studies on rectennas, presenting the research objectives and the issues it aims to resolve.

1.1 History of wireless power transfer

In 1864, Maxwell's groundbreaking prediction about electromagnetic waves laid the foundation for communication and WPT. He postulated that electromagnetic waves transmit energy through a medium, a principle further elucidated in Maxwell's equations [1]. Twenty-four years later, Hertz's experiments with dipole and loop antennas confirmed Maxwell's predictions. These experiments demonstrated electromagnetic waves' radiative and propagative properties, setting the stage for modern wireless communication and WPT [2]. Inspired by Hertz's experiments, Tesla invented the Tesla coil in 1904. He conducted low-frequency power transmission experiments using the Tesla coil. Tesla envisioned a grand plan for transmitting power across the entire globe [3]. However, his experiments failed due to the low operating frequency and the resulting low power density at the receivers [4]. In 1926, Yagi and Uda, the inventors of the Yagi-Uda antenna, conducted WPT experiments. In these experiments, a frequency of 68 MHz was used, and it was reported that a dc output of 200 mW was achieved at a distance of 1.5 m from a transmitter RF output ranging from 2 W to 3 W [5].

In 1964, W. C. Brown successfully conducted the world's first microwave power transmission (MPT) experiment. He supplied power to a helicopter using a microwave beam, achieving a successful flight [4]. Furthermore, he conducted an MPT experiment to measure the transmission efficiency from the transmitter to the receiver (dc–dc). In this experiment, a 1 kW-class magnetron and a Gaussian beam horn antenna were used at the transmitter, and a rectenna array consisting of dipole antennas and a single shunt rectifier circuit was used at the receiver. The experiment measured an output dc power of 500 W at the receiver from an input dc power of 1 kW at the transmitter [6]. This overall transmission efficiency of 50% remains the world record to this day [7]. His experiments have made significant contributions to the development of MPT up to the present. Inspired by the success of Brown's MPT experiment, P.E. Glaser conceived the concept of a space solar power system (SSPS) [8]. SSPS is a system that transmits the power generated by solar panels deployed in space to Earth using microwaves. SSPS represents MPT's most important ultimate goal. Research and development of terrestrial WPT systems have been actively conducted as a step towards realizing SSPS.

1.2 Recent activities in the field of microwave power transmission

From the 1980s to the 2000s, the research team at Kyoto University in Japan actively conducted MPT experiments on the ground. The team at Kyoto University collaborated with Kobe University and Mitsubishi Electric, among others, to conduct MPT experiments on flying objects and between ground locations [9–11]. MPT experiments involving flying objects and ground stations were conducted in Japan and various countries worldwide [10]. This global accumulation of MPT experiments has spurred the revitalization of the MPT industry in the 2020s, with various MPT products being introduced in recent years.

In particular, several startup companies in the United States have launched MPT products. Companies such as Ossia [12], Powercast [13], and Energous [14] have announced MPT systems, including transmission and receiving units. Ossia has developed a multipath retrodirective method for indoor and in-vehicle applications, utilizing reflective waves from walls. The retrodirective method is a beam control technique used in communications. In this method, a pilot signal emitted from the receiver is captured by the transmission array antenna, which then radiates the complex conjugate of this signal, focusing the radio waves back to the receiver. This technique allows for safer MPT as it can transmit power around obstacles due to its system characteristics. Consequently, various research and development efforts are underway using retrodirective MPT.

Moreover, the MPT industry in Japan is also experiencing a surge. In 2022, Japanese government has established new domestic radio regulation (RR) for far-field WPT across three frequency bands: 920 MHz, 2.45 GHz, and 5.8 GHz [15, 16]. The new domestic RR led to various Japanese companies and startups entering the MPT industry. Notably, the 920 MHz band is the only one under the new regulations that can be used in areas where people are present, making it one of the first to be implemented in society. For example, Panasonic [17] and AETERLINK [18] have announced transmitters and receivers operating in the 920 MHz band. Additionally, to achieve higher energy density, considerations are underway to use the 20 GHz band or a higher frequency [10]. These activities reflect the active global research and development in MPT in industry and academia.

1.3 General challenges of MPT systems

The power flow applied to the entire MPT system is illustrated in Fig. 1.1. Among these, the transmission efficiency is determined by geometric conditions such as the antenna size relative to the operating frequency wavelength and the transmission distance. In other words, increasing the frequency improves transmission efficiency under the same antenna size and transmission distance conditions. However, increasing the frequency also increases the circuit losses in both the transmitter and the receiver. Therefore, to achieve high efficiency in MPT, it is crucial to enhance the efficiency of circuits containing nonlinear elements, such as the RF amplifier in the transmitter and the rectifier circuit in the receiver. In particular, in the field of energy harvesting, it is essential to broaden the bandwidth and improve the efficiency under low power conditions of rectennas to reutilize the surplus power of communication waves. Here, the focus is on the rectenna, the theme of this research, and previous studies on improving the efficiency of rectennas are discussed.

1.4 Previous studies and challenges of rectennas

1.4.1 Theoretical calculations of the diode's efficiency

The diode efficiency limits the maximum rectification efficiency of a rectenna. Various studies have been conducted on the theoretical calculation of diode efficiency. In 1992, Tae-Whan and K. Chang introduced closed-form equations for the equivalent circuit of a diode for the fundamental wave and direct current, calculating the theoretical rectification efficiency of the diode [19]. Furthermore, J. O. McSpadden and K. Chang et al. extended this theoretical calculation method to account for variations in input power [20]. These theoretical calculation methods can represent the impact of the diode's turn-on voltage and breakdown voltage on efficiency and the efficiency degradation due to the cutoff frequency. However, these theoretical methods ignore harmonics and only sometimes match the measurement results of rectifier circuits.

In 2014, S. Hemour et al. proposed a theoretical efficiency calculation method for diodes at low power [21]. They introduced this method to investigate the rectification performance of spin diodes using magnetic tunnel junctions. Similar to the method by Kai Chang et al., their method applies closed-form equations around the equivalent circuit of the diode. How-

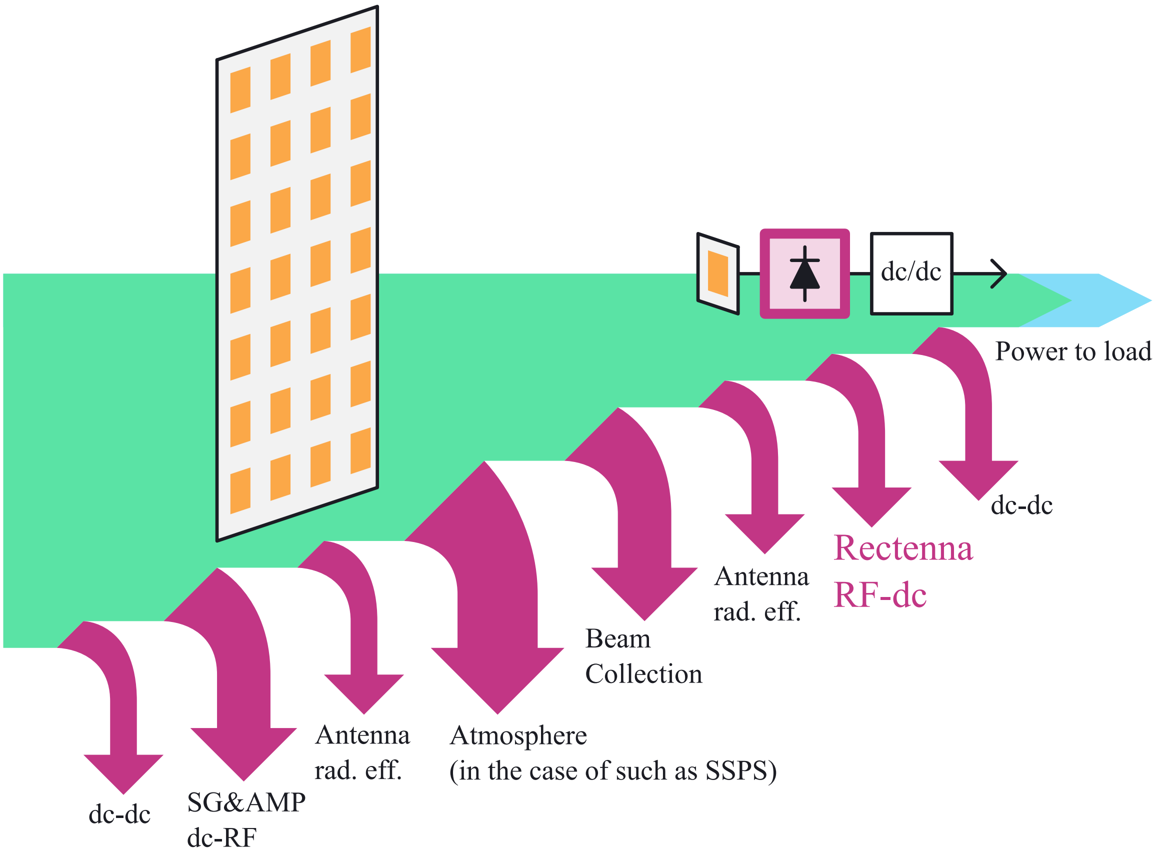


Figure 1.1: Power flow of general MPT systems.

ever, their proposed theoretical calculation method represents the harmonics arising from the nonlinear current-voltage characteristics of the diode using a first-order modified Bessel series. By introducing this series representation, their method accounts for the harmonics generated in the diode.

Furthermore, in 2020, S. Hemour et al. improved their proposed calculation method to accommodate high power levels [22]. Because their method considers harmonics, the theoretical calculation results for rectification efficiency closely match the measurement results of rectennas. Additionally, they expressed the rectification efficiency of the rectifier circuit as the product of the efficiencies of each block, illustrated in Fig. 1.2.

As described above, various theoretical efficiency calculation methods have been proposed. Here, using the block representation of the rectifier circuit efficiency shown in Fig. 1.2, the research on rectennas can be broadly classified into two categories. The first category is the research on diode elements aimed at improving $\eta_{\rm d}$ and $\eta_{\rm p}$ in Fig. 1.2. The second category is the research on rectenna circuit designs and configurations to improve $\eta_{\rm m}$ and $\eta_{\rm dct}$ in Fig. 1.2.

We discuss each of the efficiencies in Fig. 1.2. Fig. 1.3 shows a simplified equivalent circuit of the rectenna in the case of a single diode and a schematic diagram representing the compo-

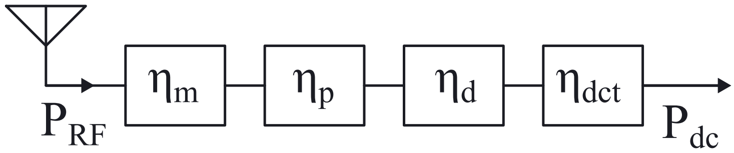


Figure 1.2: Block diagram of the rectenna's efficiency. η_m represents the matching efficiency, η_p represents the efficiency associated with parastic losses, η_d is the diode's power conversion efficiency(core conversion), η_dct is the efficiency of dc power transfer from the diode to the dc load. The rectifier circuit's total RF–dc conversion efficiency is $\eta_0 = P_{dc}/P_{RF}$. [21]

nents of each efficiency. As shown in Fig. 1.3, efficiency η_d is due to the diode's voltage-current (V-I) characteristic. In a steady state, as shown in Fig. 1.3b, a reverse dc bias and a fundamental input wave are applied between the anode and cathode of the diode. The voltage waveform across the diode is clipped due to the nonlinearity of the V-I characteristic of the diode. Efficiency η_d decreases at low input power due to the forward voltage threshold and at high input power due to the breakdown voltage. Therefore, a high breakdown voltage and a low forward voltage threshold are required to improve efficiency η_d. Efficiency η_p, shown in Fig. 1.3c, is influenced by the diode's series resistance component R_s and junction capacitance C_j (including package parasitic reactance). These components act as a low-pass filter. As the frequency increases, less voltage is applied to R_j, decreasing efficiency η_p. Thus, low series resistance R_s and junction capacitance C_j are essential to improve efficiency η_p. Efficiency η_dct, illustrated in Fig. 1.3d, is the dc power transfer function due to matching the power supply and load resistance when the diode is viewed as a dc power source. Improving efficiency η_dct involves selecting the optimal load resistance under operating conditions. An maximum power point tracking (MPPT) system consistently follows the optimal load using a dc–dc converter connected to the rear of the rectenna. Efficiency η_m, shown in Fig. 1.3e, represents the matching efficiency when aligning the impedance of the diode-side circuit with the antenna. Designing the rectifier circuit and the antenna to be matched to $50\,\Omega$ is common. The matching circuit should consist of low-loss elements, providing impedance matching with as short paths as possible to improve efficiency η_m. Furthermore, Fig. 1.2 assumes zero loss due to harmonics generated by the diode. In other words, as shown in Fig. 1.3f, when the diode is viewed as a power source that generates each harmonic, open ends, short-circuit ends, and reactive terminations must be provided for each harmonic so that the power loss due to that power source is zero. This change in circuit behavior for these harmonics is called harmonic controlling.

Summarizing the discussion of rectenna efficiency shown in Fig. 1.2, the efficiencies related to the diode element are represented by η_p and η_d, while the efficiencies that can be improved through rectenna design include η_m, η_dct, and losses due to harmonics. In other words, in rectenna design, the efficiency cannot exceed η_p, η_d, and η_dct, which are determined by the rectifying diode used. Therefore, it is crucial for designers to first obtain the theoretical maximum efficiency of the rectifying diode under the operating conditions defined by the frequency, input power, and load resistance. The rectenna should then be designed to maximize this efficiency. The method for calculating the theoretical maximum efficiency η_{p}, η_{d}, and η_{dct} is detailed in Appendix A.

1.4.2 Development of diode elements for MPT

We discuss previous studies on diode elements for rectennas. The study of diodes for rectennas focuses on improving η_{p} and η_{d}. To improve η_{p}, it is essential to lower R_{s} and C_{j}, which means that the diode's cutoff frequency is high, allowing for fast switching. To improve η_{d}, high breakdown voltage and low forward voltage are required. Higher output power is also needed for higher-power WPTs, so the diode must have a higher withstand voltage. Schottky barrier diodes are used for rectenna diodes from the viewpoint of high-speed switching. The semiconductors in Schottky barrier diodes include Si, GaAs, and GaN. In particular, GaN and GaAs diodes have been extensively studied in recent years due to their faster operation and higher breakdown voltage [23, 24]. However, because GaN and GaAs diodes are expensive, Si diodes are commonly used in commercial applications. Therefore, Si Schottky barrier diodes are often used in research and development.

1.4.3 Previous studies of several types of rectenna

Examples of previous research on rectenna circuit designs and configurations are described. Among the rectification efficiencies shown in Fig. 1.2, η_{p}, η_{d}, and η_{dct} are determined by theoretical calculations once the rectifying diode, its operating frequency, input power, and load are selected. However, theoretical calculations assume that power consumption due to harmonics is zero in the surrounding circuits through harmonic controlling. Therefore, in designing high-efficiency rectennas, it is crucial to minimize matching losses (η_{m}), power losses due to diode harmonics, and losses in the circuits surrounding the diodes. Various antenna shapes can be considered, but rectifier circuits can be broadly classified into two categories. The rectifier circuit methods can be divided into those using a single diode and those using multiple diodes. Fig. 1.4 shows circuit diagrams of several rectenna types.

The most familiar method using multiple diodes is the full-bridge rectifier circuit. Due to its configuration, it is well-suited for use with dipole antennas employing parallel lines. Previous research has reported high-efficiency rectennas directly connecting a dipole antenna with harmonic stubs to a full-bridge rectifier circuit [25]. However, there are disadvantages, such as requiring at least four diodes and crossover wiring on the load resistance side. Another method using multiple diodes is the charge pump. Compared to the full-bridge rectifier, the charge pump requires only two diodes, which is half the number. Additionally, the output voltage can theoretically reach a maximum equal to the breakdown voltage of the diodes. Due to this characteristic, it is often used when high voltage is needed at low power.

The single-shunt rectifier circuit is the most commonly used method in single-diode configurations. W. C. Brown first proposed the single shunt. This circuit utilizes the distributed parameter transmission line theory of high-frequency circuits. The $\lambda/4$ line and capacitor of the output filter reflect odd-order harmonics at the open end and even-order harmonics at the short-circuited end. The circuit achieves a theoretically 100% efficient full-wave rectification waveform through this harmonic controlling. Due to the utilization of high-frequency circuit characteristics, full-wave rectification is possible with just one diode, making it commonly used in MPT [26]. Another single-diode method is the single-series rectifier circuit. As shown in Fig. 1.4, this circuit is similar to the single shunt, but the diode's connection method and the arrangement of L and C are swapped. This circuit configuration also theoretically achieves 100% rectification efficiency through harmonic controlling. In 2013, T. Ohira derived the maximum rectification efficiencies of these various rectifier circuit configurations through theoretical calculations and compiled the results [27].

Rectifier circuits have various configurations, but achieving high efficiency in high-frequency bands requires effective harmonic controlling. The research group at Kyoto University proposed using an class-F load for the output filter of the single shunt. They noted that the harmonic controlling of high-frequency amplifiers and rectifier circuits is identical except for the fundamental frequency components. They introduced an class-F load by changing the capacitor of the output filter to a combination of $\lambda/4$ open stubs for the fundamental and harmonic frequencies. This single shunt with an class-F load achieved high efficiency in the microwave band [28, 29]. This circuit configuration using open stubs has since been adopted in various studies on microwave rectennas.

Class-R loads have also been proposed as an advanced harmonic controlling method [30]. Both class-F and class-R loads aim to eliminate power loss due to harmonics. While class-F loads reflect harmonics at open and short ends, class-R loads employ reactive termination for harmonics. Reactive termination turns harmonics into reactive power, thus eliminating power consumption by harmonics. High rectification efficiency has also been reported for single shunts using R-class loads. Previous research has proposed harmonic controlling methods for class-F and class-R loads, such as adjusting the transmission line length beneath the diode. class-F loads have been applied to single shunts and high-efficiency charge pumps [29]. Harmonic control using stubs has also been implemented and reported for full-bridge rectennas [25].

As described above, many harmonic controlling and impedance matching design methods in rectenna design have been reported. However, the specific circuit configurations and shapes are left to the designers' skills. In other words, there needs to be a systematic compilation of designing the surrounding circuits to utilize diode efficiency fully.

1.5 Objectives and outline of this thesis

The primary objective of this thesis is to summarize the high-efficiency design methods for single-diode rectennas. Additionally, as an application of the proposed high-efficiency rectenna design in WPT systems, the secondary objective of this study is the development of a rectenna for a harmonic retro-directive system. Regarding the primary objective, this study summarizes two approaches: A. impedance matching to a standard impedance such as $50\,\Omega$, and B. direct connection of the antenna designed with a non-$50\,\Omega$ impedance to the rectifier circuit. For approach A, this study proposes a circuit configuration and design method for impedance matching using the output filter of a single shunt rectifier circuit. This study proposes a single-series rectenna and its design method for approach B, which performs harmonic controlling using the antenna. Regarding the secondary objective, the study proposes a harmonic reradiation single series rectenna and its design method, applying the design method from approach B.This study focuses on designing the rectennas in the 920 MHz band, which is permissible for use in areas with human presence under Japanese new domestic RR.

This dissertation is structured as follows:

- **Chapter 2: Design method of a single-shunt rectifier circuit with impedance matching at the output filter**

  Chapter 2 presents a design example of a rectenna using a single-shunt rectifier circuit with $50\,\Omega$ impedance matching. We propose a new circuit configuration for the single-shunt rectifier circuit. The output filter performs impedance matching and harmonic suppression in the proposed configuration. The circuit simulation confirms that the proposed structure reduces matching losses. Additionally, we compare the measurement results of the rectifier circuit with those from previous research examples.

- **Chapter 3: Design method of a rectenna directly connecting the antenna and the rectifier circuit**

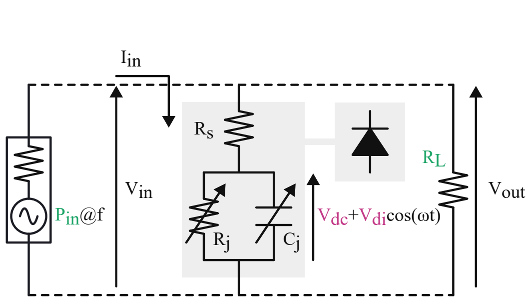
  In Chapter 3, we design a single series rectenna as an example of a rectenna design without $50\,\Omega$ impedance matching. We propose a rectenna circuit configuration that performs harmonic controlling with the antenna in a single-diode rectenna. Furthermore, we introduce harmonic source-pull simulation as a new design method for the proposed rectenna. We compare the characteristics of single-diode rectennas, specifically the single-shunt and single-series rectennas. The ideal circuit simulation confirms that full-wave rectification with a theoretical efficiency of 100% is possible using the proposed single-series rectenna structure. We fabricate both the proposed rectenna and a comparison rectenna and demonstrate through performance comparison that the proposed rectenna achieves higher rectification efficiency.

- **Chapter4: Development of a second harmonic reradiating rectenna for retrodirective systems using harmonics**

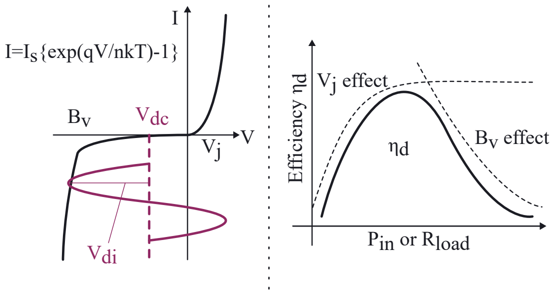
  In Chapter 4, we develop a rectenna for a WPT system using a retrodirective approach that reutilizes the second harmonic. We design a high-efficiency rectenna capable of re-radiating the second harmonic using the harmonic source-pull simulation method introduced in Chapter 3. Using harmonic source-pull simulation, we elucidate the trade-off relationship between the rectification efficiency of the rectenna and the reradiation level of the second harmonic. By comparing the simulation and measurement results of the proposed rectenna with those of conventional rectennas, we confirm an improvement in the second harmonic reradiation level of the proposed rectenna. Furthermore, by comparing previous research examples, we confirm that the proposed rectenna successfully achieves high second harmonic reradiation levels and high rectification efficiency.

- **Chapter 5: Concluding remarks**

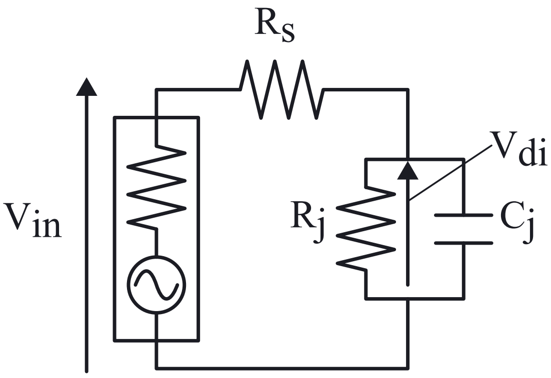
  This chapter summarizes the results obtained in each chapter and describes our research contributions to the field of WPT.



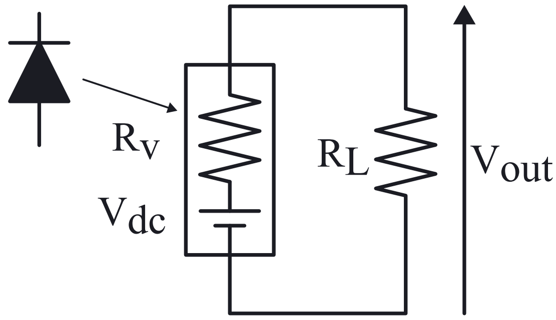
(a) Equivalent circuit of a single-shunt rectenna



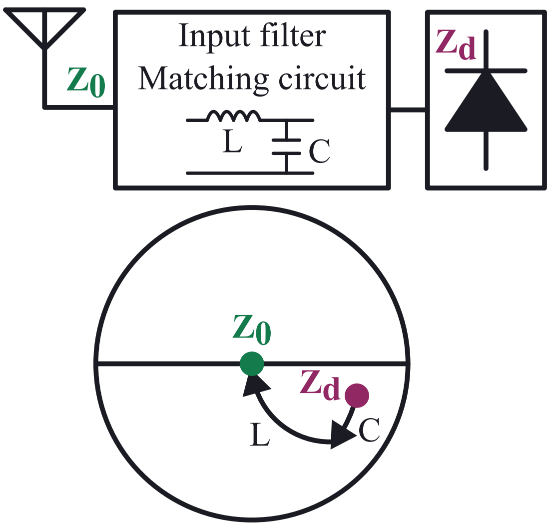
(b) Diode's V-I characteristics (η_d)



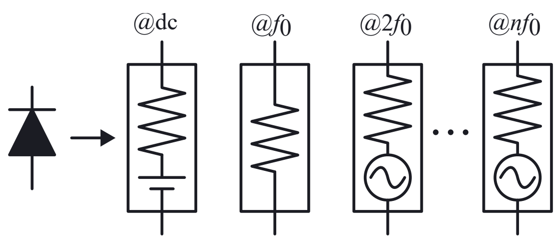
(c) Equivalent circuit of a closed loop at the fundamental frequency of the rectenna (η_p)



(d) Equivalent circuit of a closed loop in dc of the rectenna (η_{dct})

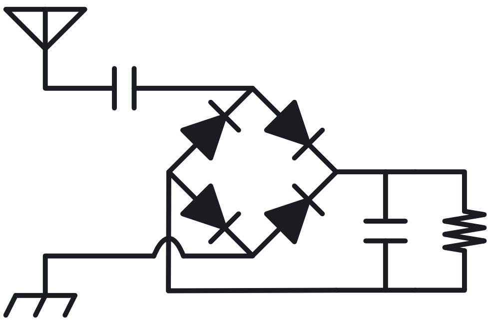


(e) Matching path between the rectifier's and the antenna's input impedances on the Smith chart (η_m)

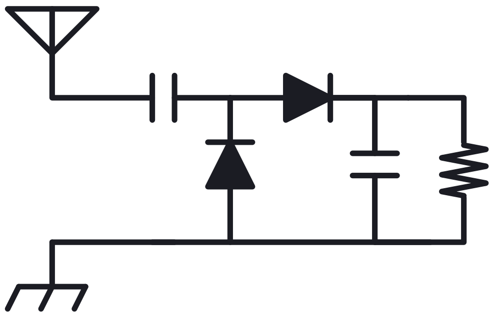


(f) Representation of the diode as a power source or load at each harmonic

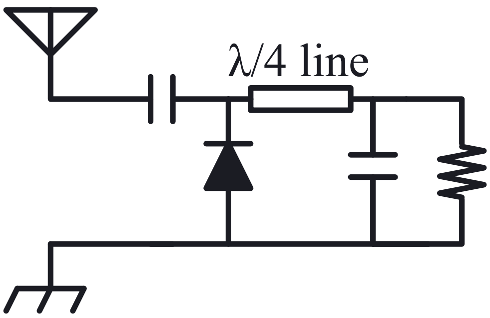
Figure 1.3: Equivalent circuit of a rectenna and a diode, and the components of each rectenna's efficiency.



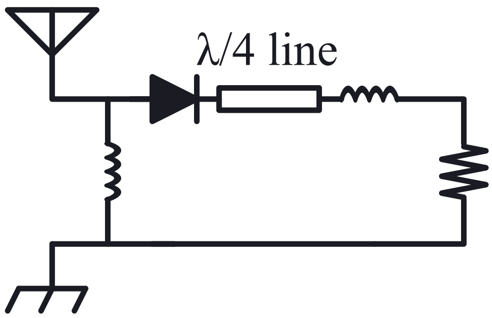
(a) Full-bridge rectenna



(b) Charge pump rectenna



(c) Single-shunt rectenna



(d) Single-series rectenna

Figure 1.4: Circuit diagrams of several rectenna types.

Chapter 2

Design method of a single-shunt rectifier circuit with impedance matching at the output filter

2.1 Introduction

This chapter presents a novel single-shunt rectifier circuit where the output filter performs impedance matching and harmonic controlling. Matching a standard impedance such as 50 Ω is commonly performed in high-frequency circuit design. The advantages of 50 Ω matching include the ability to design each system component separately and the ease of circuit evaluation in experiments. However, matching to a standard impedance like 50 Ω involves matching losses due to the matching circuit. To address this issue, we propose a circuit configuration for the single shunt rectifier that can further reduce the matching losses associated with impedance matching. This chapter explains the principles of this circuit configuration and details the proposed circuit's design method. Additionally, this chapter discusses the motivation for focusing on the design of 1 W-class rectifier circuits in the 920 MHz band. The proposed circuit configuration principles and detailed design method are explained.

Previous studies on 920-MHz band rectifier circuits have primarily focused on low-power applications such as radio-frequency energy harvesting (RFEH) and RFID [31–43]. In these low-power WPT systems, extracting the device drive voltage with low input power is a critical challenge. As a result, rectifier circuits using multiple diodes, including charge pumps that extract relatively high voltage with low input power, have been extensively studied. However, these rectifier circuits, while effective, require two or more diodes, which increases diode loss and design complexity. Consequently, the efficiency of standard low-power 920-MHz band rectifier circuits is generally less than 90% [44]. This underscores the importance of our focus on the design of 1 W-class rectifier circuits in the 920 MHz band, a significant advancement in the field. Several watt-class and 920-MHz band WPT systems will be in high demand. Thus, increasing the rectifier circuit's power and efficiency is essential. The diode and the circuit scheme determine a rectifier circuit's maximum RF–dc conversion efficiency. Previous studies have extensively discussed the maximum efficiency of rectifying diodes and circuit schemes [19,27,45–47]. Based on these considerations, achieving higher efficiency in the rectifier circuit necessitates reducing circuit losses around the rectifying diode as much as possible in the actual design.

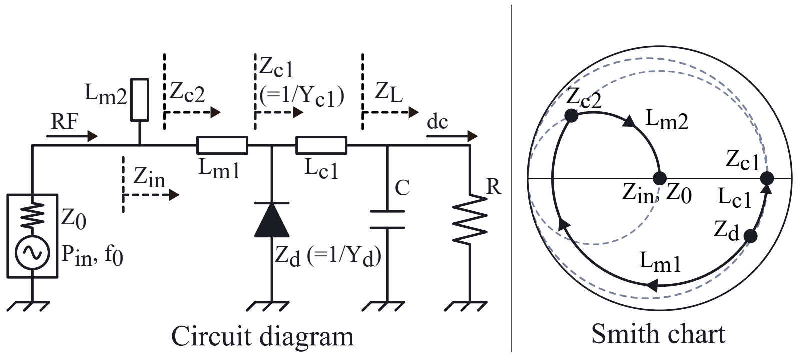
This study proposes a new structure for single-shunt rectifier circuits that can achieve higher efficiency. We have focused on improving the efficiency of rectifier circuits in the 1 W input power class to meet the demand for several watt-class WPT systems. Previous studies have investigated circuit structures to enhance the efficiency of single-shunt rectifier circuits. The previous study [48] discussed the relationship between the line lengths above and below the diode and the RF–dc conversion efficiency. However, this study [48] did not perform impedance matching of the input and reference impedance. Another study [49] addressed second-order harmonic controlling and compensation of the imaginary part of the impedance using the transmission line below the diode to achieve higher efficiency. Nevertheless, this study [49] employed a taper to match the rectifier circuit's input impedance with the reference impedance. In contrast, the proposed structure eliminates the need for standard matching circuits, such as stubs and tapers. The proposed structure can perform full-wave rectification and impedance matching by placing a feeding point on the output filter's $\lambda/4$ transmission line. This approach reduces the extra circuit loss caused by standard matching circuits, achieving high RF–dc conversion efficiency.

In this chapter, we first describe the novel structure of the single-shunt rectifier circuit proposed in this study and compare it to its conventional structure. We outline the design approach and simulation settings for the proposed rectifier circuit. Next, we explain the measurement approach for the rectifier circuit. Then, we present the simulation and measurement results, comparing the proposed rectifier circuit's RF–dc conversion efficiency with other 920-MHz band rectifiers. Finally, we conclude this chapter and suggest directions for future studies.

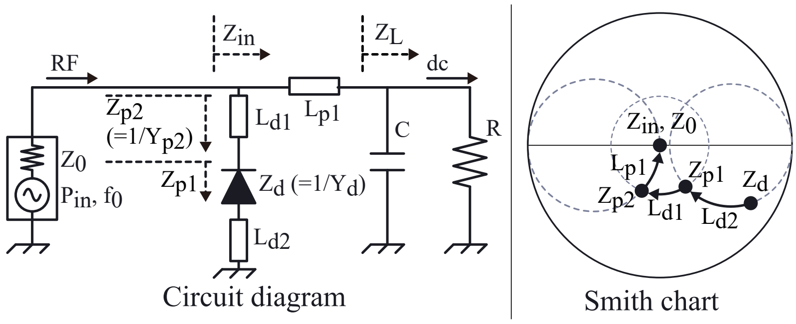
2.2 Comparison and applicable conditions of the proposed structures

2.2.1 Comparison of impedance matching of the conventional and proposed structures

This subsection explains the differences in impedance matching between the conventional and proposed structures. Fig. 2.1 shows the circuit diagrams and the impedance matching path on the Smith chart for both the conventional and proposed single-shunt rectifier circuit structures.



(a) Conventional structure.



(b) Proposed structure.

Figure 2.1: Circuit diagrams and impedance matching on smith chart of the conventional and proposed structure of single-shunt rectifier circuit.

The conventional structure (Fig. 2.1a) comprises a matching circuit (or low-pass filter), a rectifying diode, and an output filter. The input impedance Z_{L} of a parallel circuit consisting of a capacitor and a load resistor is given by the following equation:

$$Z_{\mathrm{L}} = \frac{R}{1+\mathrm{j}\omega RC}, \tag{2.1}$$

where ω, R, and C represent the angular frequency, load resistance, and capacitance, respectively. Assuming that the angular frequency ω is sufficiently large, the parallel circuit of R and C behaves like a short circuit. The output filter presents an open circuit for odd-order harmonics and a short circuit for even-order harmonics generated by the diode. This harmonic treatment by the output filter allows full-wave rectification [26, 50]. The diode impedance is defined as $Z_{\mathrm{d}} = R_{\mathrm{d}} - \mathrm{jX_d}$. We consider the transmission lines lossless and assume the characteristic impedance of the transmission line and matching target to be Z_0.

For the conventional structure shown in Fig. 2.1a, impedance matching to Z_0 can be explained as follows. Adjusting the line length of the $\lambda/4$ transmission line L_{c1} compensates for the imaginary component of the diode input admittance Y_{d}. Assuming that the angular frequency ω is sufficiently large in Eq. (2.1), the $\lambda/4$ transmission line L_{c1} in the output filter can be considered a short stub. The input admittance Y_{c1} of a parallel circuit consisting of a diode and a short stub (output filter) is given by the following equation:

$$Y_{c1} = \frac{R_d}{R_d^2 + X_d^2} + j\left(\frac{X_d}{R_d^2 + X_d^2} - \frac{1}{Z_0 \tan(\beta l_{c1})}\right), \tag{2.2}$$

where β and l_{c1} represent the phase constant and the length of the transmission line L_{c1}, respectively. If the imaginary part of the input admittance Y_{c1} is zero, the line length l_{c1} is given by:

$$l_{c1} = \frac{1}{\beta} \arctan\left(\frac{R_d^2 + X_d^2}{Z_0 X_d}\right). \tag{2.3}$$

When the line length l_{c1} satisfies Eq. (2.3), the input impedance Z_{c1} can be derived from Eq. (2.2) as:

$$Z_{c1} = \frac{R_d^2 + X_d^2}{R_d}. \tag{2.4}$$

Single-stub shunt tuning matches this input impedance Z_{c1} to Z_0 using the transmission line L_{m1} and the open stub L_{m2} [51].

We developed the proposed structure by considering the impedance of the $\lambda/4$ transmission line in the conventional structure's output filter. The right end of the $\lambda/4$ transmission line, which is connected to a smoothing capacitor, becomes a short circuit to the fundamental wave ($Z = 0$). Conversely, the left end of the $\lambda/4$ transmission line becomes an open circuit ($Z = \infty$). In other words, impedance matching between the rectifier and the measurement system (or the receiving antenna) can be achieved by setting the input point of RF power on the $\lambda/4$ transmission line.

For the proposed structure shown in Fig. 2.1b, the impedance matching to Z_0 can be explained as follows. The proposed structure does not use conventional matching circuits like stubs and tapers. Instead, it uses the transmission lines above and below the diode and the output filter for matching. The shorted transmission line L_{d2} compensates for the imaginary component of the diode input impedance Z_d. The input impedance Z_{p1} of the series circuit consisting of the diode and the shorted transmission line L_{d2} is given by the following equation:

$$Z_{p1} = R_d + j(Z_0 \tan(\beta l_{d2}) - X_d), \tag{2.5}$$

where l_{d2} is the length of the transmission line L_{d2}. If we set the line length l_{d2} to $\lambda/8$, as per the bandstop circuit proposed in the previous study [49], the input impedance Z_{p1} is given by the following equation:

$$Z_{p1} = R_d + j(Z_0 - X_d). \tag{2.6}$$

Then, the input impedance Z_{p1} is adjusted on the SWR circle by the transmission line L_{d1}. The following equation expresses the input impedance Z_{p2}:

$$Z_{p2} = Z_0 \frac{Z_{p1} + jZ_0 \tan(\beta l_{d1})}{Z_0 + jZ_{p1} \tan(\beta l_{d1})}, \tag{2.7}$$

where l_{d1} is the length of the transmission line L_{d1}. The transmission line L_{d1} moves the input impedance Z_{p1} to the first intersection of the SWR circle and the normalized admittance $1 + jx$ circle on the admittance chart. The line length l_{d1} is given by:

$$l_{\mathrm{d1}} = \frac{1}{\beta} \arctan\left(\frac{Z_0 X_{\mathrm{d2}} + \sqrt{R_{\mathrm{d}} Z_0 \left(R_{\mathrm{d2}}^2 + X_{\mathrm{d2}}^2\right)}}{Z_0 R_{\mathrm{d2}}}\right), \tag{2.8}$$

where $R_{\mathrm{d2}} = R_{\mathrm{d}} - Z_0$ and $X_{\mathrm{d2}} = Z_0 \tan \beta l_{\mathrm{d2}} - X_{\mathrm{d}}$. Substituting Eq. (2.8) into Eq. (2.7), the input admittance Y_{p2} (equal to $1/Z_{\mathrm{p2}}$) is given by the following equation:

$$Y_{\mathrm{p2}} = \frac{1}{Z_0}\left(1 + \mathrm{j}\frac{\sqrt{Z_0 R_{\mathrm{d}} \left(R_{\mathrm{d2}}^2 + X_{\mathrm{d2}}^2\right)}}{Z_0 R_{\mathrm{d}}}\right). \tag{2.9}$$

The input admittance Y_{p2} given in Eq. (2.9) is matched to the impedance Z_0 by single-stub shunt tuning using the transmission line L_{p1} [51]. Here, the combined length of the proposed structure's transmission lines L_{d1} and L_{p1} corresponds to the length of the conventional structure's transmission line L_{c1}.

The conventional and proposed structures match the diode input impedance Z_{d} to the reference impedance Z_0. However, as shown in Fig. 2.1, the paths on the Smith chart differ. The proposed structure can adjust the impedance on the Smith chart to a lower level than the conventional structure, enabling impedance matching with the reference impedance Z_0. The proposed structure reduces the matching circuit's loss by reducing the path length on the Smith chart for matching. Consequently, the proposed structure can achieve higher RF–dc conversion efficiency than the conventional structure by reducing the loss in the matching circuit.

2.2.2 Applicable conditions of the proposed structure

We discuss the conditions under which the diode's input impedance Z_{d} can achieve impedance matching to the reference impedance in the proposed structure. The proposed structure compensates for the imaginary component of Z_{d} using the shorted transmission line L_{d2}. Single-stub shunt tuning with L_{d1} and L_{p1} then performs the impedance matching, as shown in Fig. 2.1. We consider the scenario where the input impedance Z_{p1} lies within the circle of normalized admittance $1 + \mathrm{j}x$ on the admittance chart. In this case, the combined lengths of L_{d1} and L_{p1} must be longer than $\lambda/4$ to match Z_{p1} to Z_0. Therefore, the diode impedance Z_{d} must satisfy the following equation:

$$\frac{R_{\mathrm{d}}}{R_{\mathrm{d}}^2 + \left(Z_0 \tan\left(\beta l_{\mathrm{d2}}\right) - X_{\mathrm{d}}\right)^2} < \frac{1}{Z_0}. \tag{2.10}$$

If the line length l_{d2} of the shorted transmission line is $\lambda/8$, the condition for the diode impedance Z_d becomes:

$$\frac{R_d}{R_d^2 + (Z_0 - X_d)^2} < \frac{1}{Z_0}. \tag{2.11}$$

Full-wave rectification and impedance matching are still possible with the proposed structure, even if the diode impedance Z_d does not satisfy Eq. (2.10) or Eq. (2.11). However, in this scenario, the impedance matching path of the proposed structure is longer, resulting in higher circuit loss than the conventional structure.

2.3 Design method of the rectifier circuit

We explain the approach and conditions for designing and simulating the proposed 920-MHz band single-shunt rectifier circuit. The rectifier circuit was designed using the following steps:

1. Select the rectifying diode and dielectric substrate.
2. Use the theoretical calculation proposed by [20] to determine the diode efficiency and optimum load resistance.
3. Adjust the rectifier circuit's parameters by executing optimization with circuit simulation.
4. Perform electromagnetic (EM) simulation for the rectifier circuit.
5. Simulate the rectifier circuit using the EM simulation results.

The rectifier circuit's parameters were adjusted to achieve maximum RF–dc conversion efficiency by iteratively repeating steps 3 to 5.

We designed the rectifier circuit using a rectifying diode, microstrip lines, and radial open stubs. We used NPC-H220A as the dielectric substrate, which has a metal thickness of 18 μm, a dielectric thickness of 0.8 mm, a dielectric constant of 2.16, and a dissipation factor of 0.0005. The width of the microstrip lines was set to 2.46 mm, resulting in a characteristic impedance (Z_0) of 50 Ω at 920 MHz. The rectifying diode used was a GaAs Schottky barrier diode, which is non-commercial. Fig. 2.2 and Table 2.1 show the equivalent circuit and parameters of the rectifying diode. The diode's packaged model is SC-79. We employed the Advanced Design System (ADS) from Keysight Technologies for the circuit and EM simulations.

2.3.1 Theoretical calculation of the diode efficiency and the optimum load

We employed the theoretical calculation method and equivalent circuit proposed in [20] to obtain the optimum load, diode input impedance, and maximum diode efficiency. We used the

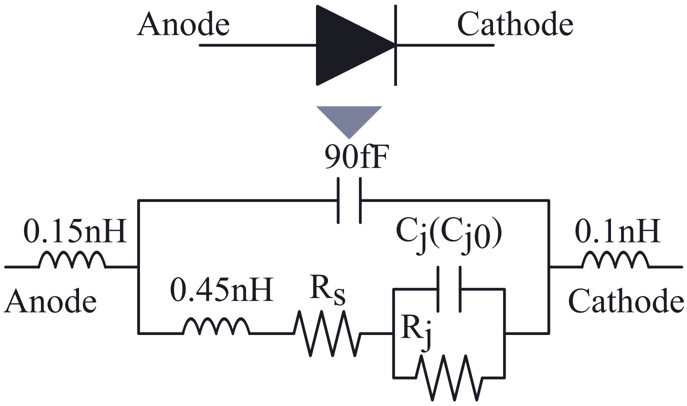


Figure 2.2: Equivalent circuit model of the GaAs Schottky barrier diode.

Table 2.1: SPICE parameters of the diode.

Parameters	Value
Breakdown voltage B_V (V)	70
Junction potential V_j (V)	1.0
Series resistance R_S (Ω)	1.6
Saturation current I_S (μA)	8.4
Junction capacitance C_{j0} (pF)	3.0
Breakdown current I_{BV} (μA)	9.1
Emission coefficient N	1.75
Grading coefficient M	0.5

diode parameters shown in Table 2.1. The output voltage V_{out}, built-in V_{bi}, and junction capacitance C_j were set to $V_{out} = 30\,\mathrm{V}$, $V_{bi} = 0\,\mathrm{V}$, and $C_j = 3.0\,\mathrm{pF}$, respectively. The load resistance R_{load} was varied from $1\,\Omega$ to $10000\,\Omega$ in steps of $1\,\Omega$. We calculated the phase θ_{ON} corresponding to the moment when the diode turns ON using the following equation [20]:

$$\tan\theta_{ON} - \theta_{ON} = \frac{\pi R_S}{R_{load}\left(1 + \frac{V_{bi}}{V_{out}}\right)}. \tag{2.12}$$

We solved Eq. (2.12) using the Newton method with an initial value of $\theta_{ON} = \pi$. Using the θ_{ON} obtained from Eq. (2.12), we calculated the diode input impedance Z_d according to [20]:

$$\begin{aligned} Z_d = & \frac{\pi R_S}{\cos\theta_{ON}\left(\frac{\theta_{ON}}{\cos\theta_{ON}} - \sin\theta_{ON}\right)} \\ & + \frac{\pi R_S}{\mathrm{j}\omega R_S C_j\left(\frac{\pi-\theta_{ON}}{\cos\theta_{ON}} + \sin\theta_{ON}\right)}. \end{aligned} \tag{2.13}$$

At the optimum load resistance R_{load} of $217\,\Omega$, we found the diode input impedance Z_d and maximum diode efficiency of $21.1 - \mathrm{j}43.3\,\Omega$ and 88.5%, respectively. Therefore, this rectifying

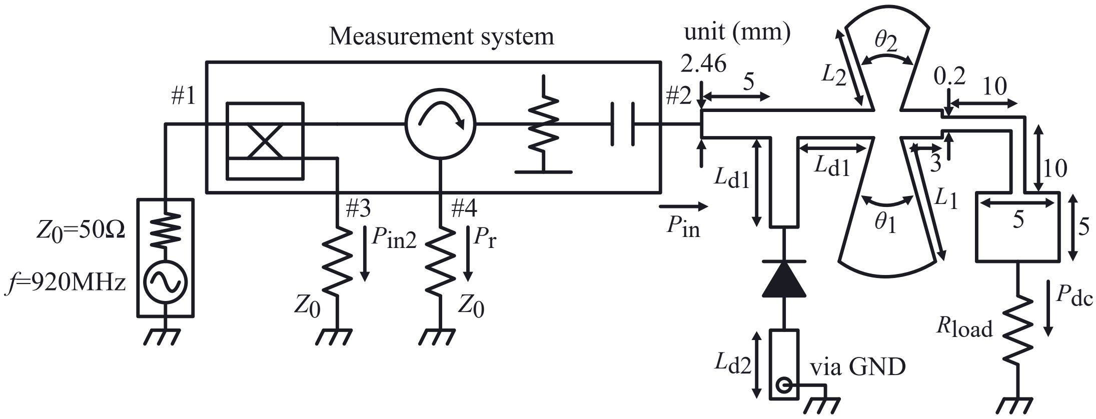


Figure 2.3: Configuration of the rectifier circuit on Advanced Design System (ADS).

diode satisfies Eq. (2.10) if $Z_0 = 50\,\Omega$ and $l_{d2} = 0\,\text{mm}$. This theoretical calculation method focuses only on the fundamental frequency [20]. Thus, we used the obtained optimum load resistance and maximum efficiency as indices for the circuit design.

2.3.2 Circuit simulation

Fig. 2.3 illustrates the configuration of the rectifier circuit in ADS. The S-parameters of the measurement system's components (directional coupler, circulator, attenuator, and dc block) were included in the circuit simulation to reduce the error between simulation and measurement. We used an offset to align the input power to the rectifier circuit with the power at port 3 in the measurement experiments, ensuring that the power at ports 3 and 2 were equal. In the simulation, the power at port 2 was obtained by multiplying the power at port 3 by the offset value, mirroring the measurement experiments. In this study, the output filter used a class-F load configuration. Instead of a smoothing capacitor, radial open stubs were used in the output filter with lengths of $\lambda/4$ for the fundamental frequency (L_1) and the second harmonic (L_2). Radial open stubs were chosen because they handle harmonics more accurately than smoothing capacitors. Additionally, the lambda/4 radial open stub L_1 effectively short-circuits at 920 MHz. We employed the harmonic balance method for circuit simulation and optimization, considering up to the 10th harmonics. The input power P_{in}, load resistance R_{load}, lengths of the microstrip lines L_{d1}, L_{d2}, L_{p1}, and the angles of the radial open stubs θ_1 and θ_2 were optimized to maximize RF–dc conversion efficiency. The initial values of R_{load} and P_{in} were set based on theoretical calculations. After optimization, EM simulations were performed on the rectifier circuit. The performance of the rectifier circuit was then examined using the harmonic balance method based on the results of the EM simulations.

2.4 Measurement method

Fig. 2.4 shows the configuration of the measurement system used in this study. The signal generator (Agilent, E4421B) generates the fundamental wave, amplified by 40 dB using the amplifier (R&K, A1000-15-R). The amplified power is then delivered to the rectifier circuit through a directional coupler (Pasternack, PE2200-30), circulator (Ditom, D3C0710N), attenuator (Nihon Koshuha Co., FA-N-09K03), and dc block (Pasternack, PE8211). The rectifier circuit's input power is measured using power sensor A (Agilent, 8481A) and a power meter (Agilent, E4419B) via the directional coupler. The reflected power from the rectifier circuit is measured using power sensor B (Agilent, 8481B) and the power meter via the circulator. Calibration is performed at port 2 of the measurement system to measure the input power to the rectifier circuit accurately. During calibration, power sensors A and B are connected to ports 3 and 2, respectively, and port 4 is terminated with 50 Ω. RF power is input to port 1, and an offset is applied to the value measured by power sensor A to match the value measured by power sensor B. The dc voltage V_{out} and current I_{out} at the load are measured using digital multimeter A (Agilent, 34401A) and digital multimeter B (Keysight, 34465A). For more precise measurements, a -3 dB attenuator is inserted in front of the rectifier circuit's input port to suppress the reflection of harmonics by the measurement system. The output dc power P_{out} is computed using the following equation:

$$P_{\mathrm{out}} = V_{\mathrm{out}} I_{\mathrm{out}}. \tag{2.14}$$

The RF–dc conversion efficiency η is calculated using the following equation:

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \times 100\% = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{x P_{\mathrm{in}2}} \times 100\%, \tag{2.15}$$

where x is the offset value applied during calibration. This measurement's offset value x was 26.9 dB.

2.5 Simulation and measurement results

2.5.1 Comparison of the performance of the conventional and proposed structures

Using circuit simulation, we compared the RF–dc conversion efficiency η and circuit loss α of the conventional and proposed structures. Fig. 2.5 shows the circuit diagram in ADS used for this comparison. To calculate the circuit loss α, we analyzed the power at both ends of each transmission line and extracted the fundamental wave component of the analyzed power. The circuit loss α was computed by taking the difference in the power of the fundamental wave components at both ends of each transmission line. The following equation defines the circuit

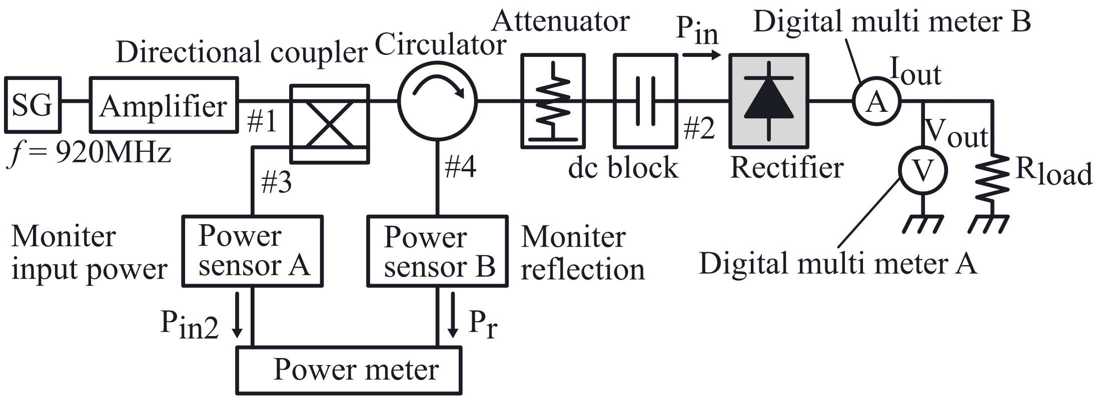


Figure 2.4: Measurement system of the rectifier circuit in this study. The attenuator with -3 dB was inserted in front of the input port of the rectifier circuit for more accurate measurements.

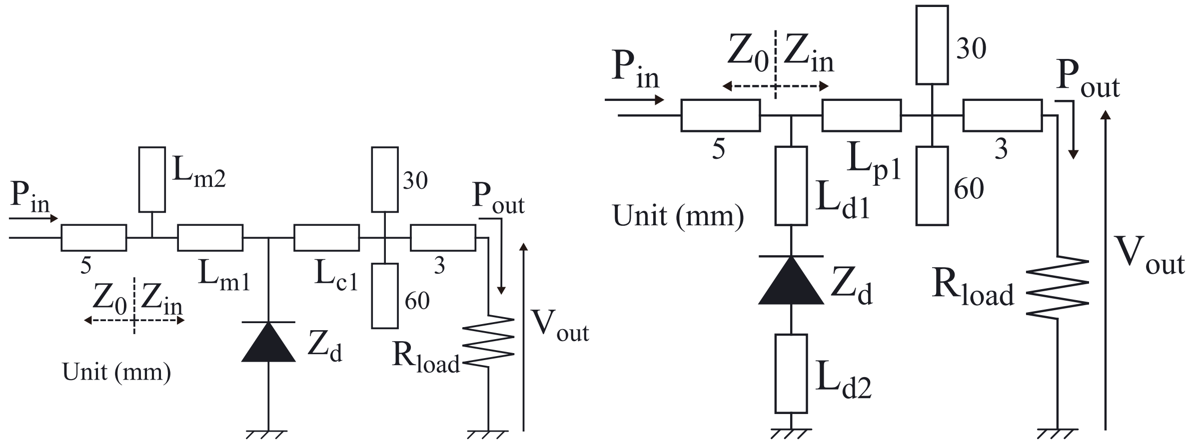
Table 2.2: Parameters of the conventional rectifier circuit.

R_{load} (Ω)	L_{m1} (mm)	L_{m2} (mm)	L_{c1} (mm)	V_{out} (V)	η (%)	α (%)
200	80.5	32.8	41.7	13.3	88.03	2.53
400	80.7	41.4	41.9	18.6	86.84	4.45
600	77.5	44.5	43.3	22.6	85.10	6.13
800	76.2	46.3	43.6	25.8	83.52	7.83
1000	75.5	47.7	43.6	28.6	81.76	9.49

loss α:

$$\alpha = \frac{1}{P_{\mathrm{in}}} \sum_{n=1}^{m} \left(P_{l,n} - P_{r,n}\right) \times 100\%, \tag{2.16}$$

where n is a natural number, m is the number of lines in the circuit, and $P_{l,n}$ and $P_{r,n}$ are the power of the fundamental wave components at the left and right ends of the n-th line, respectively. Additionally, open stubs were used instead of radial stubs to reduce the number of parameters to be optimized. At 920 MHz, an open stub with a line length of 60 mm effectively short-circuits the load resistance. To compare the circuit loss α based on the impedance matching approach, we fixed the parameters other than L_{m1}, L_{m2}, θ, and L_{c1} of the conventional structure and L_{d1}, L_{d2}, and L_{p1} of the proposed structure. Furthermore, we fixed the input power P_{in} at 1.0 W and varied R_{load} from 200 Ω to 1000 Ω in 200 Ω steps. We optimized L_{m1}, L_{m2}, and L_{c1} of the conventional structure and L_{d1}, L_{d2}, and L_{p1} of the proposed structure to maximize the RF–dc conversion efficiency at each load resistance. Table 2.2 and Table 2.3 show the optimized parameters at each load resistance. The comparison in Table 2.2 and Table 2.3 indicates that the proposed structure minimizes circuit loss and achieves higher RF–dc conversion efficiency than the conventional structure.



(a) Conventional structure. (b) Proposed structure.

Figure 2.5: Circuit diagrams of the conventional and proposed structure of single-shunt rectifier circuit.

Table 2.3: Parameters of the proposed rectifier circuit.

R_{load} (Ω)	L_{m1} (mm)	L_{m2} (mm)	L_{c1} (mm)	V_{out} (V)	η (%)	α (%)
200	14.1	31.0	38.2	13.5	90.53	0.94
400	10.3	42.2	52.1	18.8	88.76	1.30
600	11.0	45.6	50.6	20.9	87.45	1.67
800	10.6	47.4	48.7	26.4	86.91	2.05
1000	10.0	48.4	48.3	29.4	86.48	2.40

2.5.2 Comparison of the impedance-matching paths of the conventional and proposed structures

We compared the impedance matching paths of the conventional and proposed structures at the fundamental frequency using ADS, as shown in Fig. 2.5. To ensure a fair comparison, the dc operating point of the diode was fixed by applying a reverse voltage using an external dc power supply. We applied reverse voltages of 13.3 V and 13.5 V to the diodes in the conventional and proposed circuits, respectively. The input power P_{in} and load resistance R_{load} were fixed at 1.0 W and 200 Ω, respectively, for both circuits. The impedance matching paths were analyzed by varying the length of each transmission line while applying the reverse voltage to the diode. In the conventional structure shown in Fig. 2.5a, the line lengths L_{p1}, L_{d1}, and L_{d2} varied from 60 mm to 38.2 mm, 0.1 mm to 14.1 mm, and 0.1 mm to 31 mm, respectively, in 0.1 mm steps. Similarly, in the proposed structure shown in Fig. 2.5b, the line lengths L_{p1}, L_{d1}, and L_{d2} were varied in the same ranges. Fig. 2.6 shows the simulation results of the impedance-matching

Table 2.4: Parameters of the rectifier circuit after the optimization.

Parameters	Value	Parameters	Value
L_{d1}	23.1 mm	L_{d2}	29.7 mm
L_{p1}	25.8 mm	L_1	43.3 mm
L_2	28.8 mm	θ_1	16 °
θ_2	10 °	P_{in}	2.48 W
R_{load}	260 Ω	η	92.4%

paths for both structures. The impedance-matching paths correspond to the paths described in Section 2.2. There is a slight difference between the impedance matching paths shown in Fig. 2.1 and Fig. 2.6 due to changes in the diode input impedance caused by varying the line lengths. In this circuit simulation, the voltage waveform at the diode changes when the transmission lines L_{d2}, L_{p1}, L_{c1}, and L_{m2} are varied while maintaining a constant reverse voltage. This change affects the diode conduction angle θ_{ON}, altering the diode input impedance Z_d. Consequently, varying the line lengths also changes the diode input impedance, leading to differences in the impedance matching paths between Fig. 2.1 and Fig. 2.6. Additionally, Fig. 2.6 shows that the proposed structure has a shorter impedance-matching path and can perform impedance matching through a lower impedance than the conventional structure. This shorter path results in less circuit loss during impedance matching, giving the proposed structure an advantage over the conventional structure.

2.5.3 Simulation and measurement results of the proposed rectifier circuit

We fabricated the rectifier circuit using the proposed structure. Table 2.4 displays the values of each parameter illustrated in Fig. 2.3 after optimization and EM simulation. At an input power $P_{in} = 2.48\,\mathrm{W}$ and load resistance $R_{load} = 260\,\Omega$, the maximum RF–dc conversion efficiency is 92.4% in the simulation. Fig. 2.7 shows a photograph of the fabricated rectifier circuit in this study. Its size is smaller than $0.25\lambda \times 0.5\lambda$ ($\lambda = 326\,\mathrm{mm}$), with dimensions of 63 mm × 100 mm. In the simulation, the optimum load was 260 Ω; however, in the measurement, it was 292 Ω. We fixed the frequency and load resistance R_{load} at 920 MHz and 292 Ω and swept the input power P_{in} to simulate and measure the RF–dc conversion efficiency and reflection. Fig. 2.8a shows the results from theoretical calculations, simulations, and measurements of the RF–dc conversion efficiency and reflection as functions of power characteristics at $R_{load} = 292\,\Omega$. The theoretical calculation results shown in Fig. 2.8 were derived using the calculation method presented in Appendix A. The change in RF–dc conversion efficiency and reflection with varying input power P_{in} showed good agreement between simulation and measurement. The measurement experiments yielded a maximum RF–dc conversion efficiency of 91.0% and a reflection of 0.598%, with an input power $P_{in} = 1.79\,\mathrm{W}$ and load resistance $R_{load} = 292\,\Omega$. Fig. 2.8a

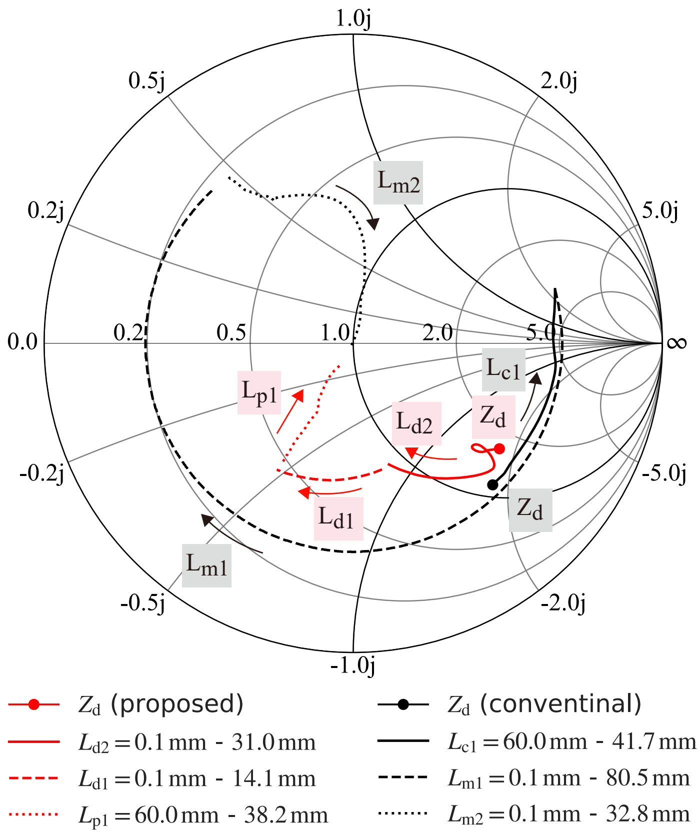


Figure 2.6: Impedance matching paths of the conventional and proposed structures. We set $P_{\text{in}} = 1.0\,\text{W}$, $R_{\text{load}} = 200\,\Omega$ in the circuit simulation shown in Figure2.5. We applied the reverse voltage of 13.3 V and 13.5 V to the diode of the conventional and proposed circuits, respectively, using an external dc power supply. The line lengths L_{c1},L_{m1}, L_{m2}, L_{p1},L_{d1}, and L_{d2} were varied from 60 mm to 41.7 mm, from 0.1 mm to 80.5 mm, from 0.1 mm to 32.8 mm, from 60 mm to 38.2 mm, from 0.1 mm to 14.1 mm, and from 0.1 mm to 31 mm in 0.1 mm steps, respectively.

demonstrates that the proposed structure can simultaneously achieve impedance matching and full-wave rectification at the fundamental frequency. Fig. 2.8b illustrates the results from the theoretical calculations, simulations and measurements of the RF–dc conversion efficiency and reflection as functions of load characteristics at $P_{\text{in}} = 1.0\,\text{W}$. Fig. 2.8b shows that the proposed rectifier circuit can perform impedance matching around the optimum load in the measurement. The maximum measured efficiency of 91.0% is 4.3 percentage points lower than the theoretical efficiency of 95.3% under the same input power and load conditions. This 4.3-point reduction in efficiency is likely due to matching losses, harmonic losses, and insertion losses in the circuits. In other words, the proposed circuit effectively achieves harmonic controlling necessary for full-wave rectification while sufficiently suppressing matching losses. From Fig. 2.8, it can be observed that the theoretical efficiency exhibits a broader bandwidth in both power and load

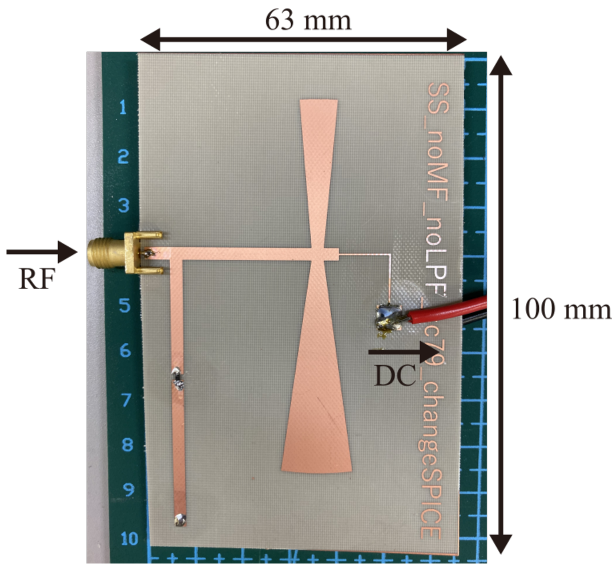
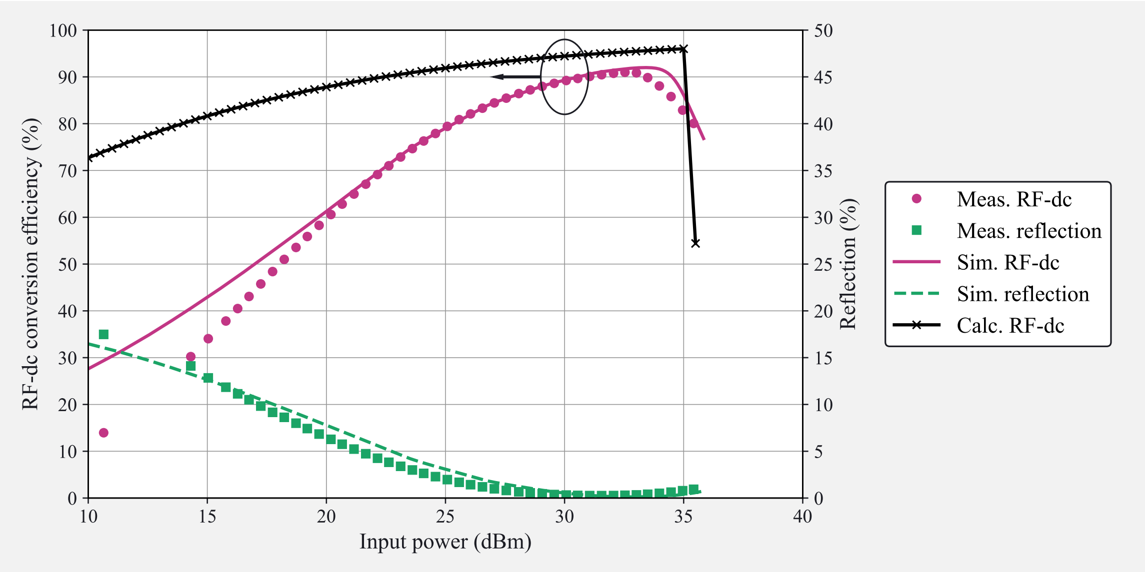


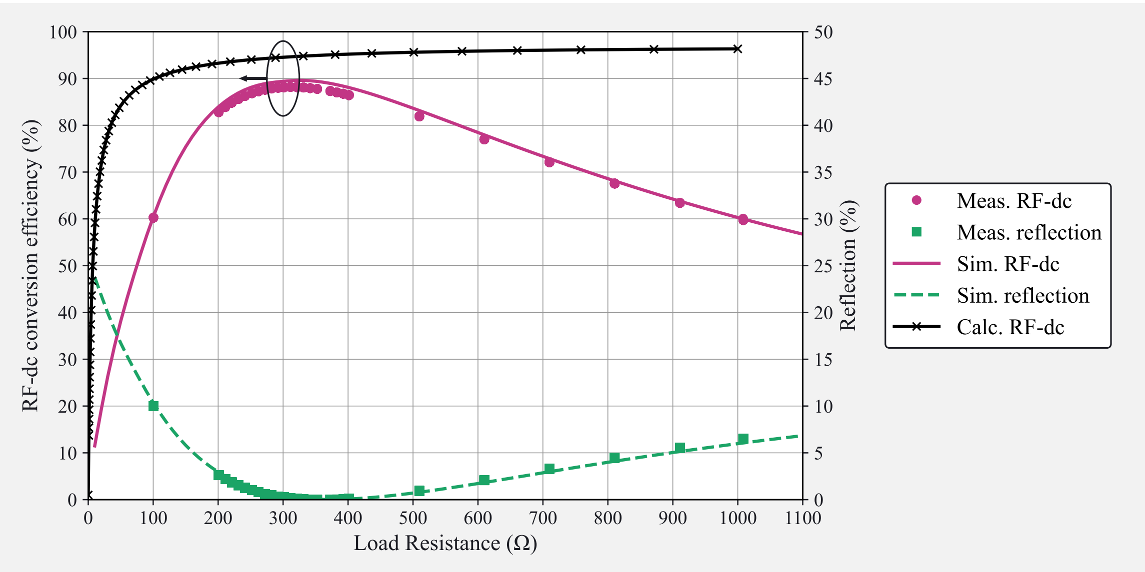
Figure 2.7: Photograph of the fabricated single-shunt rectifier circuit.

characteristics compared to the measured and simulated results. This is because the designed rectifying circuit is tuned to perform impedance matching and harmonic processing under specific input power and load conditions. As shown in Fig. 2.8, the rectifying circuit designed in this study achieves the highest efficiency near an input power of 31.5 dBm and a load resistance of 292 Ω, with impedance matching occurring around these operating conditions, resulting in low reflection.

We compared the performance of the developed rectifier circuit with other 920-MHz band rectifier circuits. For comparison, we selected a single-shunt rectifier circuit and another type of rectifier circuit with an efficiency of 70% or higher. Table 2.5 shows the results of this performance comparison. Since diodes operate near their threshold voltage, achieving higher efficiency at lower input power ranges is more challenging. Consequently, rectifier circuits with lower input power generally exhibit lower efficiency, as shown in Table 2.5. However, this study obtained high efficiency by driving the diode with an applied voltage significantly higher than its threshold voltage. Compared to a rectifier circuit driven by a similarly high applied voltage [52], the developed rectifier circuit achieves higher efficiency because the proposed structure reduces circuit loss. The maximum RF–dc conversion efficiency of the rectifier circuit developed in this study was 91.0%, a world record for 920-MHz band rectifier circuits.



(a) Power characteristics at $R_{\mathrm{load}} = 292\,\Omega$.



(b) Load characteristics at $P_{\mathrm{in}} = 1.0\,\mathrm{W}$.

Figure 2.8: Results from theoretical calculations, simulations, and measurements of the RF–dc conversion efficiency and reflection as functions of (a) power characteristics and (b) load characteristics.

2.6 Conclusions

This chapter developed a 920-MHz band single-shunt rectifier circuit for the WPT system. To achieve high efficiency, we proposed a novel structure that does not use standard matching circuits such as stubs and tapers. In the proposed structure, the transmission lines above and below the diode and the output filter can simultaneously perform impedance matching and rectification at the fundamental frequency. Using circuit simulation, we compared the circuit loss and RF–dc conversion efficiency of the conventional and proposed structures. The simulation results demonstrate that the proposed structure has lower circuit loss and higher efficiency than the conventional structure. We fabricated and measured the proposed rectifier circuit, and the results showed that it can simultaneously perform impedance matching and rectification at the fundamental frequency. Furthermore, we compared the performance of the rectifier circuit developed in this study with other 920-MHz band rectifier circuits. The rectifier circuit developed in this study achieved a maximum RF–dc conversion efficiency of 91.0%, setting a world record for 920-MHz band rectifier circuits. The proposed structure is designed explicitly for single-shunt rectifier circuits and contributes to high efficiency by leveraging their structural features. This high-efficiency design approach for single-shunt rectifier circuits can also be applied to other frequency bands. In the future, we plan to apply the proposed rectifier circuit to the 920-MHz band WPT system.

Table 2.5: Performance comparison of rectifier circuits with input power of 10 dBm or more and around 920 MHz bands.

References	Frequency (MHz)	Circuit type	Input power (dBm)	Efficiency (%)
[53]	900	Single-shunt	17.0	69.9
[47]	900	Single-shunt	13.4	80.4
[42]	900	Charge pump	10.0	80.0
[43]	920	Charge pump	15.0	78
[54]	900	Amplifier & rectifier	16.0	88.0
[52]	850	Amplifier & rectifier	39.0	81.0
This work	920	Single-shunt	32.5	91.0

Chapter 3

Design method of a single-diode rectenna directly connecting the antenna and the rectifier circuit

3.1 Introduction

In Chapter 2, we introduced a novel single-shunt rectifier circuit that achieves higher efficiency with reduced matching losses when matching to a standard 50 Ω impedance. Matching circuits inherently include matching losses. Therefore, achieving zero matching loss in rectennas by directly matching the antenna input impedance with the diode input impedance, rather than matching to a standard impedance, is a better design approach for high efficiency. This chapter proposes a single-series rectenna that directly connects the antenna to the rectifying circuit and discusses a new design method using harmonic source-pull simulations.

Fig. 3.1 illustrates the distinctions between the single-shunt and single-series rectenna circuit diagrams. W.C. Brown introduced a single-shunt rectenna with a half-wave dipole antenna and a parallel-connected rectifying diode, classified as a type I rectenna in Fig. 3.1 [55]. His single-shunt rectifier circuit utilizes the properties of a distributed circuit to control the harmonics generated by the diode. Notably, the dc-pass filter, consisting of a quarter-wavelength line and a smoothing capacitor, acts as an open circuit for the odd harmonics and a short circuit for the even harmonics generated by the diode. This harmonic control enables full-wave rectification using a single diode [26]. Brown achieved an RF–dc conversion efficiency of 90% with a 2.45 GHz-band single-shunt rectenna [55].

Several researchers have focused on the similarities between harmonic control in the dc-pass filter of a single-shunt rectenna and that of a class-F load in a high-frequency amplifier [28, 47, 56–58]. Numerous studies have documented using single-shunt rectifier circuits employing a class-F load. However, due to its frequency characteristics, the capacitor in the dc-pass filter fails to provide adequate short-circuit terminations at higher harmonics. In the class-F

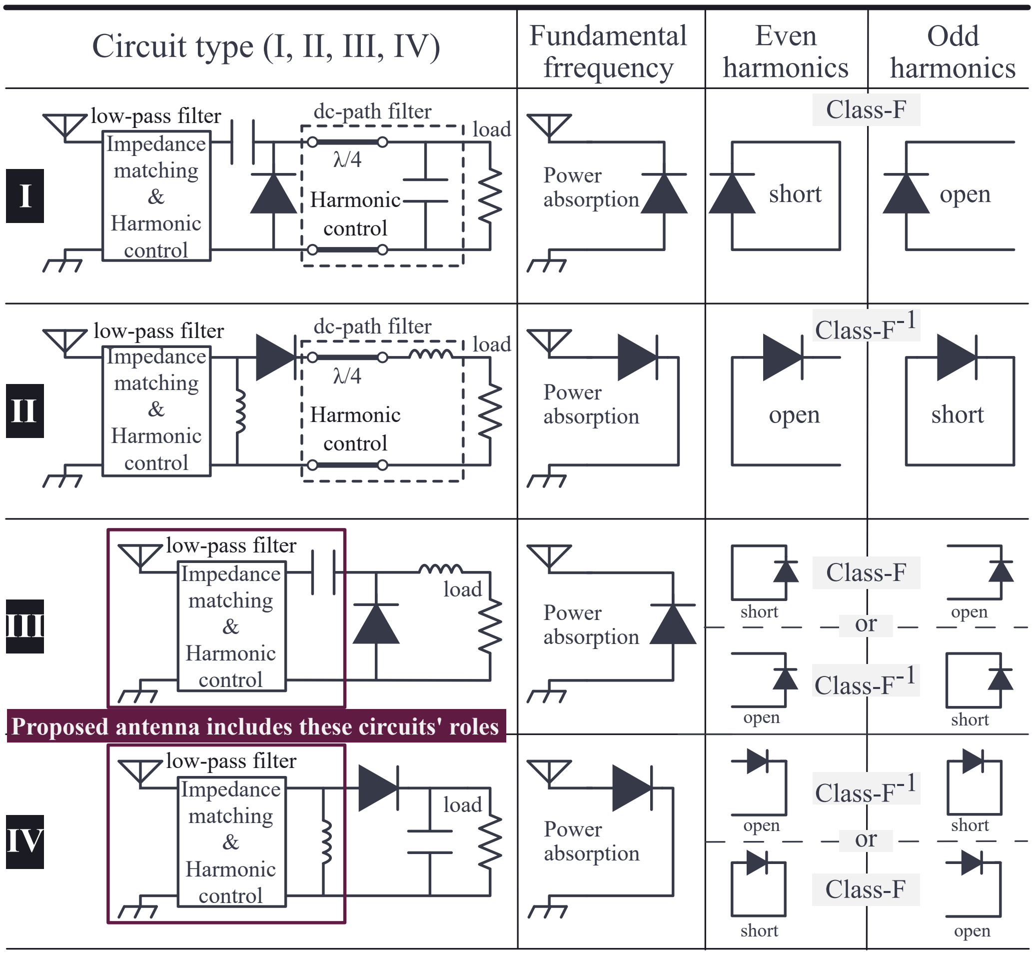


Figure 3.1: Comparison of the differences between single-shunt and single-series rectennas and the configuration of the proposed single-series rectenna.

load configuration, shown as type I in Fig. 3.1, the capacitor is replaced with parallel-connected open stubs that function as quarter-wavelength resonators for the fundamental frequency and harmonics. These open stubs fine-tune the short-circuit terminations at the fundamental frequency and each harmonic, resulting in a more efficient rectifier circuit than a capacitor. Previous studies have reported single-shunt rectifier circuits using a class-F load, achieving an efficiency of 90% at the 2.45 GHz band [28]. This thesis also reported the single-shunt rectifier circuit using a class-F load with an RF–dc conversion efficiency of 91% at the 920 MHz band, as shown in Chapter 2. Therefore, harmonic control is essential for achieving full-wave rectification and high efficiency with a single diode, as demonstrated in single-shunt rectennas.

Diode efficiency limits a rectenna's maximum RF–dc conversion efficiency [20]. Therefore, it is crucial to determine the maximum efficiency of the diode under operational conditions and minimize circuit losses in peripheral components. Designing a rectenna with a simple configuration is essential. In the standard design of a single-diode rectenna, as shown in Fig. 3.1, the dc-pass filter, the low-pass filter, or both are responsible for harmonic control. Concurrently, the low-pass filter matches the impedance between the receiving antenna and the rectifier circuit. The operating conditions of the rectifying diode vary depending on the input power and load resistance. Typically, the low-pass filter is optimized for a specific diode operating condition. Therefore, consolidating harmonic control and impedance matching into a single component is crucial to minimize circuit losses. A previous study [59] introduced a highly efficient rectenna featuring a direct connection between a half-wave dipole antenna and a full-bridge rectifier circuit without the low-pass filter. Harmonic control was achieved using short stubs connected to the antenna, resulting in an impressive RF–dc conversion efficiency of 92.8% [59]. However, the full-bridge rectenna features a cross-connection at the dc-pass filter, complicating the configuration for a single-layered rectenna. A single-diode rectenna is needed that eliminates the need for cross-connections at the dc-pass filter and simplifies the configuration by avoiding additional circuits to achieve higher RF–dc conversion efficiency.

This study introduces a novel single-diode rectenna, shown as type IV in Fig. 3.1, which enhances RF–dc conversion efficiency by using harmonic control of the receiving antenna impedance. This study focuses on developing a single-series rectenna equipped with an antenna capable of controlling harmonics. Specifically, the roles of the low-pass filter and an inductor for the dc short circuit are integrated into the receiving antenna. This configuration minimizes losses in additional circuits and improves RF–dc conversion efficiency. Notable distinctions between our proposed rectenna and a single-shunt rectenna that utilizes a Class-F load include simplifying the dc-pass filter through harmonic control at the antenna. Additionally, our rectenna differs from the full-bridge rectenna presented in [59] in that it achieves full-wave rectification using only a single diode. We incorporate source-pull simulations in designing our rectenna. Source/load-pull techniques are commonly used in high-frequency amplifier design [60–62]. They also apply to rectenna design, which involves non-linear elements similar to those in high-frequency amplifiers. Although previous research extensively covers rectenna design using load-pull methods [54, 63–66], designs employing source-pull techniques are less common. Moreover, previous investigations into the use of source-pull methods for rectenna design have focused solely on the fundamental frequency [67–71]. A previous study [72] utilized multi-harmonic active source-pull in the MHz band for rectifier design, but the rectifier in [72] is transistor-based, not diode-based. Consequently, this study employs source-pull simulations encompassing the fundamental frequency and the harmonics in designing a diode-based single-series rectenna.

3.2 Principle of the proposed rectenna

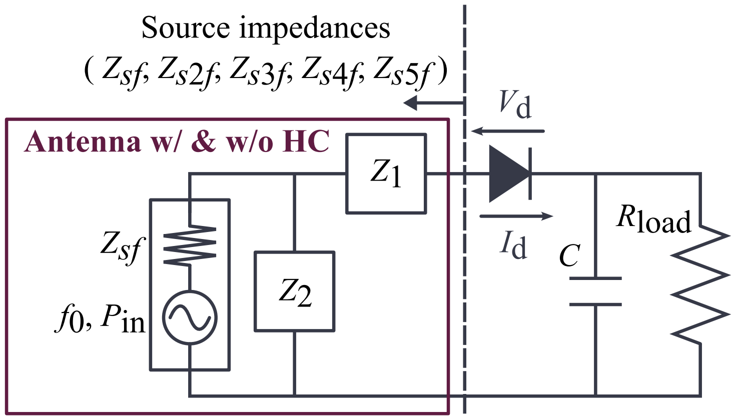
3.2.1 Feature comparison of single-diode rectennas

Theoretically, a single-shunt rectenna that utilizes a quarter-wavelength line and a capacitor can attain 100% RF–dc conversion efficiency. Conversely, the dc-pass filter of the type II single-series rectenna shown in Fig. 3.1, which employs a quarter-wavelength line and an inductor, creates an open circuit at even harmonics and a short circuit at odd harmonics. This harmonic control enables the diode to operate in inverted-F (Class-F^{-1}) mode [73, 74], resulting in an ideal RF–dc conversion efficiency of 100%. In contrast, when harmonic control is concentrated in the low-pass filter, as shown in type III and type IV configurations in Fig. 3.1, both Class-F and Class-F^{-1} operations become applicable for single-shunt and single-series rectenna configurations.

In a single-shunt rectenna, the dc-pass filter must be an open circuit at the fundamental frequency to ensure that the input power is directed solely to the diode and does not flow to the load. Consequently, if the low-pass filter controls the harmonics in a single-shunt rectenna, the dc-pass filter requires an inductor connected in series, as shown in type III in Fig. 3.1. In contrast, in a single-series rectenna, the dc-pass filter must be a short circuit at the fundamental frequency to ensure that the input power is directed solely to the diode and does not flow to the load, as shown in type IV in Fig. 3.1. Therefore, if the low-pass filter controls the harmonics in the single-series rectenna, the dc-pass filter requires a capacitor connected in parallel. Capacitors generally have lower losses than inductors, as indicated by their higher non-loaded quality factor Q. A type III single-shunt rectenna can omit the series-connected capacitor on the rectenna's input side when an open-ended antenna, such as a patch antenna, is utilized. Likewise, a type IV single-series rectenna can omit the parallel-connected inductor on the rectenna's input side when a short-ended antenna, like an inverted-F antenna, is employed. Consequently, a single-series rectenna that relies solely on a capacitor is more likely to reduce circuit losses than a single-shunt rectenna, which requires an inductor. This feature of the single-series rectenna is advantageous for rectenna design. This study focused on and designed the single-series rectenna based on these advantages. Furthermore, this study proposes a new single-series rectenna that integrates the roles of the low-pass filter and shunt inductor into the receiving antenna, performing harmonic control at the receiving antenna.

3.2.2 Ideal circuit simulation of the single-series rectenna

The previous study [27] established the theoretical efficiency of a single-series rectifier circuit at 81.1%. However, this study [27] did not incorporate harmonic control. In this subsection, we use circuit simulations employing ideal components and circuits to demonstrate that when



	DC	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$
Z_1	0 Ω	0 Ω	Z_{s2f}	Z_{s3f}	Z_{s4f}	Z_{s5f}
Z_2	0 Ω	10^{21}Ω	0 Ω	0 Ω	0 Ω	0 Ω

Figure 3.2: Circuit diagram for a comparative analysis of two cases: with and without harmonic control at the antenna. The resistances 0 Ω and 10^{21} Ω represent a short circuit and an open circuit, respectively.

the antenna (functioning as the power supply) controls the harmonics, the RF–dc conversion efficiency of the single-series rectenna can reach 100%. Additionally, as part of the ideal circuit simulation, we conducted a comparative analysis of two cases: with and without harmonic control at the antenna (the power supply).

Fig. 3.2 shows the circuit diagram for a simulation using the Advanced Design System (ADS) from Keysight Technologies. We used the harmonic balance method, with the maximum order set to the fifth harmonic. The fundamental frequency, denoted by f_0, was 920 MHz. The input power was 10.0 dBm, and the load resistance was 11 kΩ. In this simulation, we utilized an ideal diode represented within the circuit using the following equation:

$$I_\mathrm{d} = \begin{cases} 0 & (V_\mathrm{d} < 0), \\ \frac{V_\mathrm{d}}{R_\mathrm{d}} & (V_\mathrm{d} \geq 0), \end{cases} \tag{3.1}$$

whereI_d represents the current through the diode, V_d represents the voltage, and $R_\mathrm{d} = 0.5\,\mathrm{m}\Omega$ represents the on-resistance of the diode. We used a 1 nF capacitor as an output-smoothing capacitor. The power supply impedance Z_{sf} and impedances Z_1 and Z_2 determined the source impedances at the fundamental frequency and harmonics. We configured the source impedances at each harmonic Z_{snf} using the magnitude M_n and phase D_n of the reflection coefficients S_{snf},

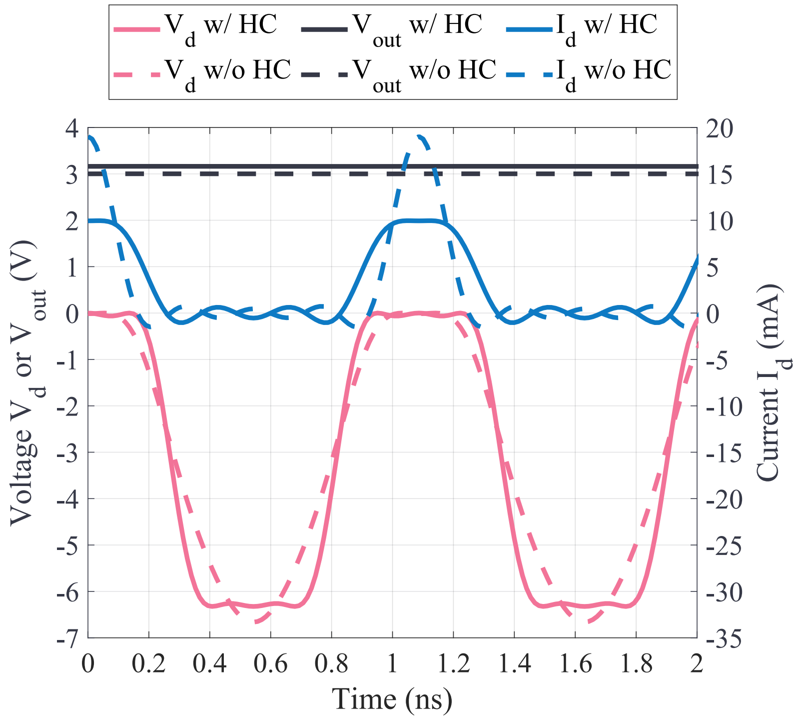


Figure 3.3: Voltage (red) and current waveforms (blue) at the diode and the output dc voltage (black) with and without harmonic control (HC) in the ideal circuit simulation.

as defined by the following equations:

$$Z_{snf} = Z_0 \frac{1+S_{snf}}{1-S_{snf}} \quad (n = 1, 2, \ldots, 5), \tag{3.2}$$

$$S_{snf} = M_n \exp\left(\mathrm{j}D_n \frac{\pi}{180^\circ}\right) \quad (n = 1, 2, \ldots, 5), \tag{3.3}$$

where n represents the harmonic order, and Z_0 represents a reference impedance of $50\,\Omega$. We configured the source impedances to create short circuits at the even harmonics and open circuits at the odd harmonics, enabling Class-F operation of the diode. Equations (3.2) and (3.3) indicate that Z_{snf} diverges when$M_n = 1$. Consequently, we cannot use $M_n = 1$ due to simulation errors. We therefore used $M_n = 0.9999$ and $D_n = 0^\circ$ to represent an open circuit, while we represented a short circuit by $M_n = 0.9999$ and $D_n = 180^\circ$. In cases where harmonic control was not employed, we set the source impedances at each harmonic to $50\,\Omega$ ($M_n = 0$ and $D_n = 0^\circ$ when $n \neq 1$), but not for the fundamental frequency. In both cases, we optimized the source impedance at the fundamental frequency on the real axis to achieve impedance matching for the rectifier circuit.

Fig. 3.3 shows the voltage and current waveforms at the diode, as observed in the simulation. Table 3.1 displays the harmonic power at the diode with or without harmonic control in the

Table 3.1: Harmonic power at the diode with or without harmonic control (HC) in the ideal circuit simulation.

Num. of harmonic	w/ HC (mW)	w/o HC (mW)
dc	10.0	9.01
f_0	10.0	10.0
$2f_0$	1.00×10^{-5}	5.91×10^{-1}
$3f_0$	3.90×10^{-4}	3.14×10^{-1}
$4f_0$	1.50×10^{-7}	8.80×10^{-2}
$5f_0$	3.00×10^{-5}	2.74×10^{-5}

simulation, rounded to three significant digits. The simulations yield a 100% RF–dc conversion efficiency when harmonic control is applied and a 90.1% efficiency when it is not. These waveforms exhibit square-wave double voltage and half-wave double current patterns with harmonic control, consistent with Class-F operation theory. The simulations indicate that the RF–dc conversion efficiency for a single-series rectenna reaches 100% with harmonic control, an increase of 9.9% compared to the case without harmonic control. The RF–dc conversion efficiency of the rectenna is associated with the theoretical efficiency, taking into account losses from the diode and circuits.

3.3 Rectenna design method

3.3.1 Rectifier design using the source-pull simulation with harmonics

Fig. 3.4 shows a circuit diagram of the source-pull simulation for the single-series rectifier circuit. We used R5775-K from Panasonic as the dielectric substrate, with the following specifications: dielectric constant = 3.62, tangential constant = 0.0046, substrate thickness = 0.75 mm, and metal thickness = 18 μm. The line width was 1.62 mm, providing a reference impedance of Ω. The rectifying diode employed was the SMS7621 from Skyworks. Fig. 3.5 and Table 3.2 show the equivalent circuit and the SPICE parameters of the diode before and after adjustment, respectively. The SPICE parameters in the datasheet are tailored for small-signal applications such as detector circuits and mixers. Consequently, when these SPICE parameters are used for rectenna design, discrepancies can arise between simulation outcomes and experimental results, particularly under high power inputs within the diode's tolerance range. To address this, we measured the voltage-current characteristics of the diode and adjusted the SPICE parameters, except for C_{j0}, based on these measurements, as detailed in Table 3.2. The parameter C_{j0} was fine-tuned through the empirical evaluation of several rectifier circuits utilizing the same diode, ensuring alignment between simulation and experimental results. We used the GJM1552C1H430JB01 capacitor from Murata, with a capacitance of 43 pF. The dc-pass filter

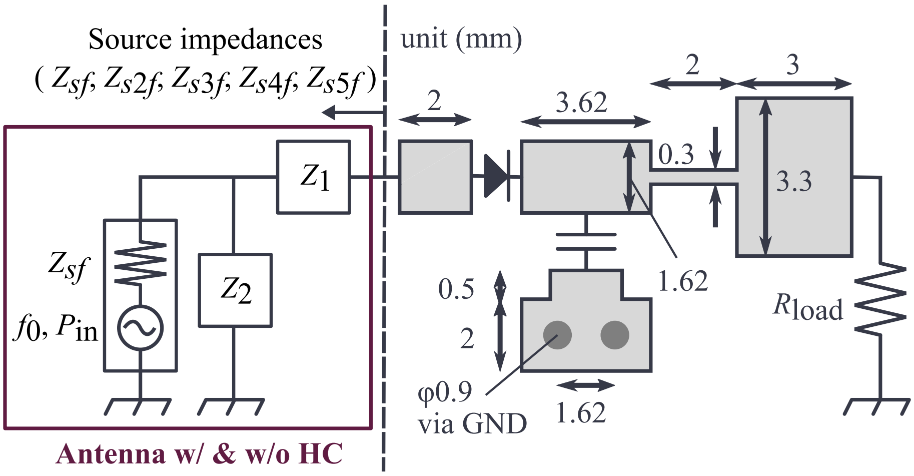


Figure 3.4: Circuit diagram of the source-pull simulation for the single-series rectifier circuit.

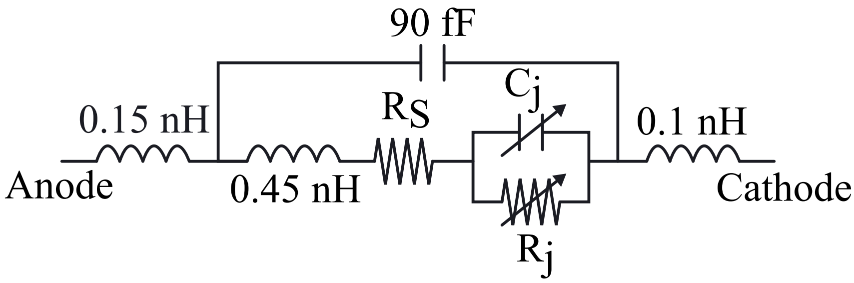
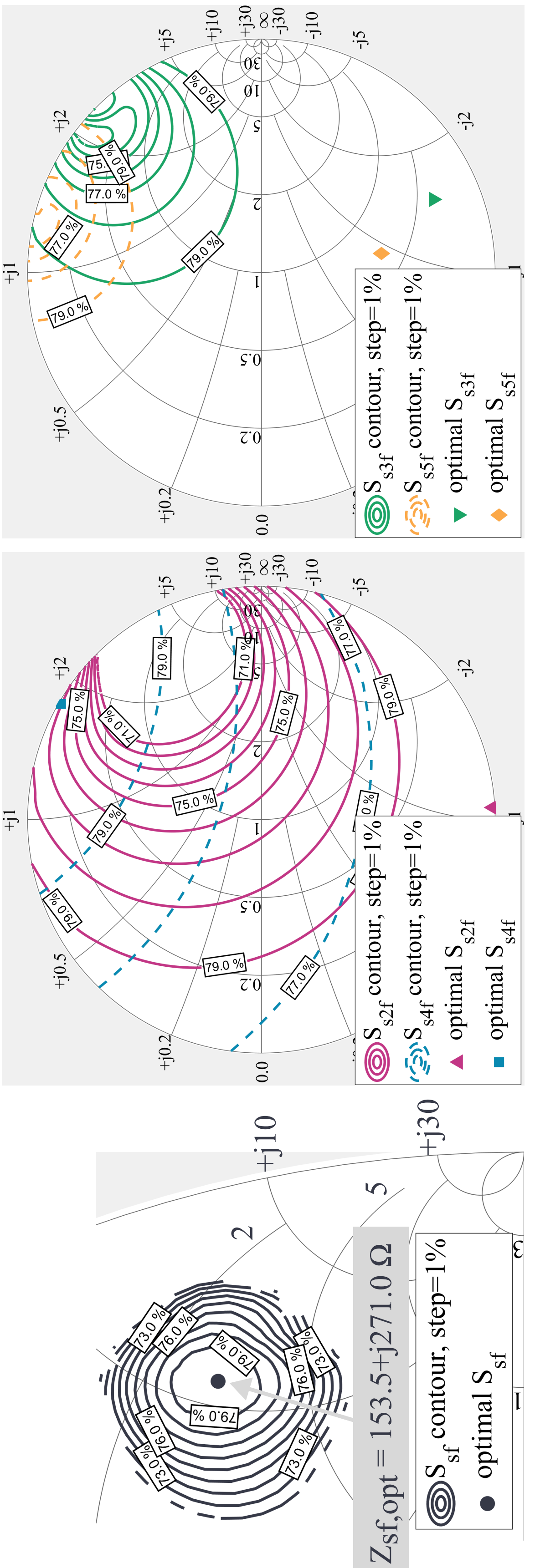


Figure 3.5: Equivalent circuit of the diode (SMS7621). The package model is SC-79.

is a simple circuit consisting of a capacitor connected in parallel, allowing dc power to pass to the load while blocking the fundamental frequency and harmonics. We swept the source impedances during the simulation while keeping the input power and load resistance fixed at 10.0 dBm and 1 kΩ, respectively. These source impedances were determined using equations (3.2) and (3.3). Each harmonic impedance was varied in steps of 0.01 for the magnitude M_n of the reflection coefficient, ranging from 0.01 to 0.99, and in 11° steps for the phase D_n of the reflection coefficient, ranging from 0° to 360°. Before conducting the source-pull simulation, we optimized the source impedance at each harmonic to maximize efficiency. Then, we swept the source impedance at each harmonic. The source impedances for orders not involved in the source-pull simulation sweep were fixed to the values obtained from optimization.

Table 3.2: SPICE parameters of the diode (SMS7621) before and after adjustment.

	Parameter	Value	Parameter	Value
before adjustment (from datasheet)	I_s	0.4 nA	R_s	12 Ω
	N	1.05	C_j0	0.1 pF
	V_j	0.51 V	M	0.35
	B_v	3 V	I_bv	10 μA
after adjustment	I_s	2 μA	R_s	9.6 Ω
	N	1.7	C_j0	0.15 pF
	V_j	0.3 V	M	0.35
	B_v	8.4 V	I_bv	0.8 mA



(a) At the fundamental frequency.

(b) At the second and fourth harmonics.

(c) At the third and fifth harmonics.

Figure 3.6: Source-pull simulation results for the proposed single-series rectenna at an input power of 10.0 dBm, resulting in a dc output voltage of 2.84 V. (a) Contours at the fundamental frequency in the upper right of the Smith chart. (b) Contours at the second and fourth harmonics. (c) Copontours at the third and fifth harmonics.

Fig. 3.6 shows the results of the source-pull simulation, with specific figures for the fundamental frequency (Fig. 3.6a), the second and fourth harmonics (Fig. 3.6b), and the third and fifth harmonics (Fig. 3.6c). In Fig. 3.6, each plot represents the optimal source impedance at which maximum efficiency is achieved in the simulation. The maximum RF–dc conversion efficiency is 80.4%, resulting in an output dc voltage of 2.84 V. Based on the source-pull simulation results, we established target source impedances for each harmonic within the range where the RF–dc conversion efficiency reaches 79.0% or higher. Fig. 3.6a shows a close-up of the upper right corner of the Smith chart; in this figure, the optimal fundamental source impedance is $153.5 + j271.0\,\Omega$. This result indicates that the fundamental source impedance becomes high when a dc output voltage of several volts is extracted at a low input power of 10.0 dBm. The input impedance of the rectifier circuit is the conjugate value of the source impedance. Consequently, Fig. 3.6a indicates that the input impedance of the rectifier circuit at the fundamental frequency is capacitive; this occurs because of parasitic capacitances, including the capacitances of both the diode junction and the package. Additionally, Fig. 3.6 shows that the target range for the fundamental source impedance is narrower than that for other harmonic source impedances. The contour results for the fundamental frequency demonstrate that the RF–dc conversion efficiency changes rapidly with variations in the fundamental source impedance. The source impedances for even harmonics are the second-most critical parameters for the RF–dc conversion efficiency. The second-harmonic source impedance is located in the lower-left corner of the Smith chart, and the fourth-harmonic source impedance is found in the upper right corner, where efficiencies of 79.0% or higher can be achieved. In contrast, the source impedances for odd harmonics are less sensitive to the RF–dc conversion efficiency than the fundamental and even harmonics. The RF–dc conversion efficiency becomes 79.0% or higher over a wide range in the lower left portion of the Smith chart for both the third and the fifth harmonics. The range of variation of the RF–dc conversion efficiency due to fluctuations of the source impedance is most significant for the fundamental wave, and this variation tends to decrease as the harmonic order increases. Lower-order harmonics substantially influence the RF–dc conversion efficiency because they possess higher energy [75]. In other words, when designing the receiving antenna, it is crucial to maintain the input impedance within the target range for the fundamental frequency.

3.3.2 Antenna design

Based on the results of the source-pull simulation shown in Fig. 3.6, we designed the receiving antenna. In a single-series rectenna, a short circuit on the anode side of the diode is required at dc to apply a reverse dc voltage to the diode. We adopted an inverted-F antenna with a short stub to satisfy this requirement. Fig. 3.7 shows the designed inverted-F antenna, which we simulated using the T-solver of CST (Dassault Systèmes) for antenna design. The substrate used for the

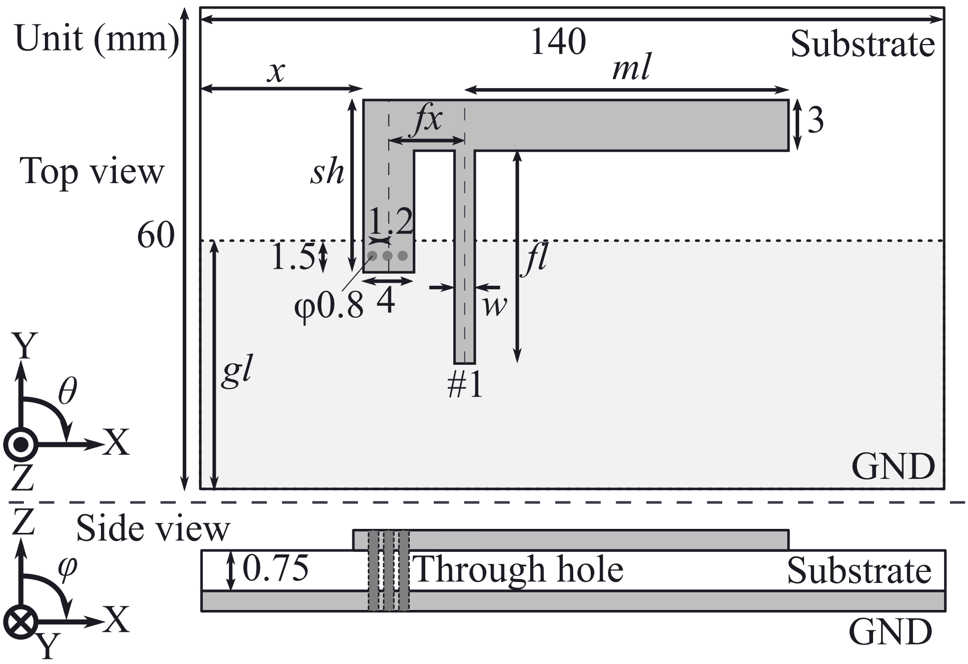


Figure 3.7: Circuit diagram of the designed inverted-F antenna.

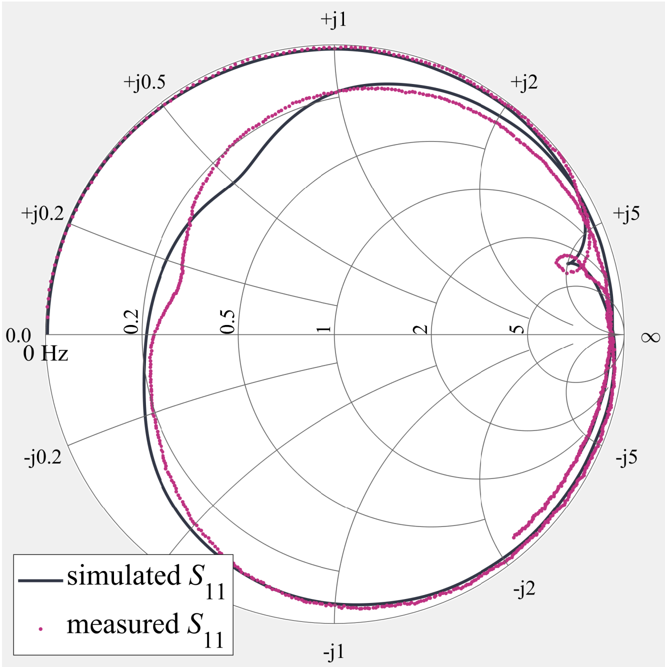
antenna was R5775-K. To analyze the antenna, we connected a waveguide port toward the positive Y-axis at port #1, as shown in Fig. 3.7. We designed two receiving antennas using the inverted-F antenna geometry, as shown in Fig. 3.7: one for the proposed rectenna and another for the comparative rectenna. The dimensions indicated in Fig. 3.7 are the design parameters of the antennas. The proposed rectenna was designed so that the antenna input impedance at all harmonics falls within the target source impedance range for an RF–dc conversion efficiency of 79% or higher. The comparative rectenna was designed so only the antenna input impedance at the fundamental frequency falls within the target range. To confirm that harmonic control of the antenna impedance is efficacious in improving the RF–dc conversion efficiency in addition to fundamental impedance matching, we compared the performance of the rectenna with harmonic control (proposed circuit) and the rectenna without harmonic control (comparative circuit).

Table 3.3 shows the adjusted design parameters of the inverted-F antenna with and without harmonic control. Fig. 3.8 shows the frequency characteristics of the input impedance of the designed inverted-F antennas with and without harmonic control. The simulated and measured input impedance of the designed antennas at each harmonic are shown in Fig. 3.9, along with the target impedance range. Specifically, Fig. 3.9a, Fig. 3.9b, and Fig. 3.9c demonstrate that, in both the simulations and the measurements, the antenna with harmonic control achieves input impedance values at each harmonic that fall within the target source-impedance range (i.e., an RF–dc conversion efficiency of 79.0% or higher). Conversely, the input impedance of the

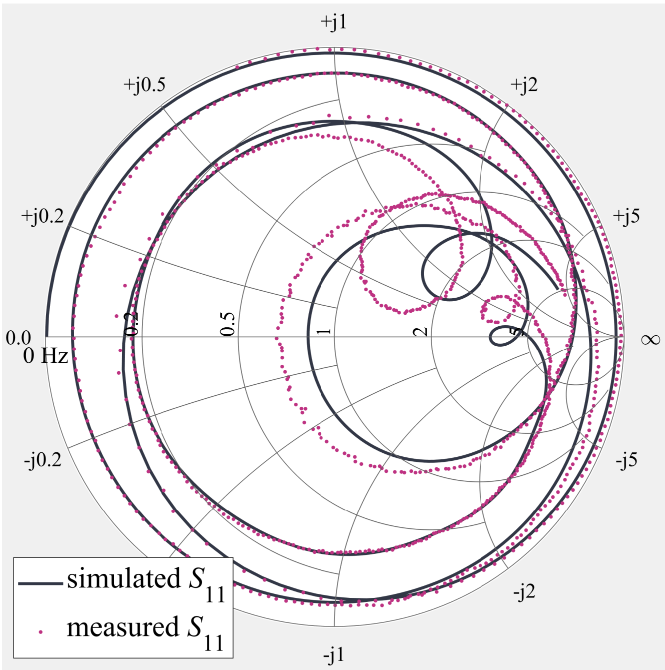
Table 3.3: Adjusted parameters of the designed inverted-F antenna with and without harmonic control (HC).

	Parameter	Value (mm)	Parameter	Value (mm)
with HC	gl	35	fl	32.5
	ml	53.5	sh	18
	fx	3.5	w	0.3
	x	30.5		
without HC	gl	48	fl	41.5
	ml	62	sh	10
	fx	39	w	0.5
	x	18.5		

antenna without harmonic control falls within the target source impedance range only at the fundamental and fifth harmonics. For the second, third, and fourth harmonics, the input impedance of the antenna without harmonic control is outside the target source impedance range. Simulation results show that the radiation efficiencies of the antennas with and without harmonic control at 920 MHz were 89.2% and 84.3%, respectively. The maximum gains of the theta component on the XY plane were 1.64 dBi at$\theta = -7°$ and 2.48 dBi at $\theta = -8°$, respectively.

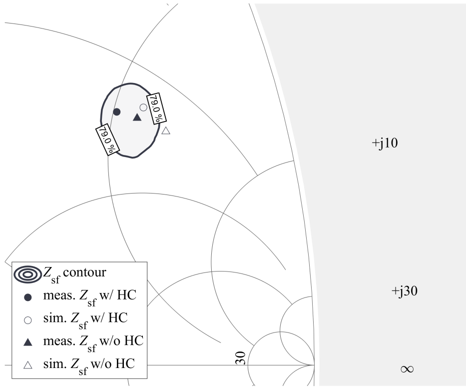


(a)

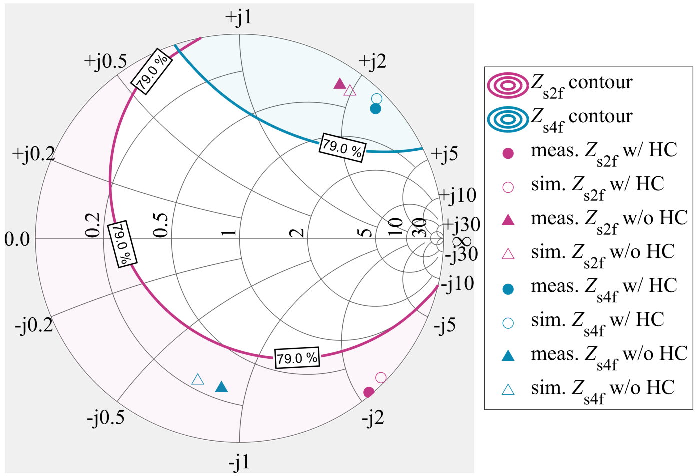


(b)

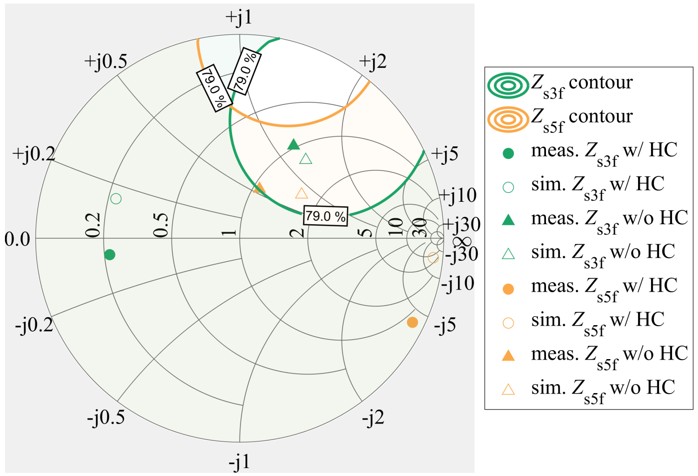
Figure 3.8: Simulated and measured input impedance of the inverted-F antenna with and without harmonic control from 0 Hz to 5 GHz. (a) The antenna with harmonic control. (b) The antenna without harmonic control.



(a) At the fundamental frequency.



(b) At the second and fourth harmonics.



(c) At the third and fifth harmonics.

Figure 3.9: Simulated and measured input impedances of the designed inverted-F antenna with and without harmonic control (HC) and the target source impedances at each harmonic. (a) Results at the fundamental frequency. (b) Results at the second and fourth harmonics. (c) Results at the third and fifth harmonics.

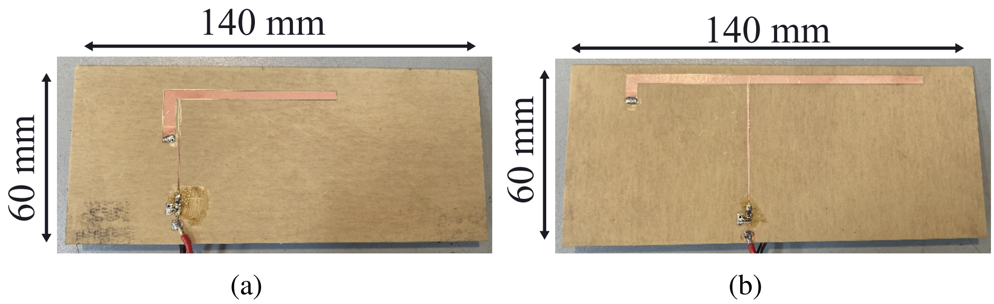


Figure 3.10: Photos of the fabricated rectennas, (a) with harmonic control, (b) without harmonic control.

3.4 Rectenna measurement

3.4.1 Input power and load resisitance characteristics

Fig. 3.10 shows the fabricated rectennas with and without harmonic control. We measured the input power and load resistance characteristics of these rectennas. Fig. 3.11 and Fig. 3.12 show a photo and an outline of the measurement system of the rectenna in an anechoic chamber, respectively. In this measurement setup, we positioned the rectennas at an angle θ to obtain the peak output dc power. To estimate the actual input power to the rectifier circuit P_{in}, we measured the output power of the designed inverted-F antenna both with and without harmonic control using the system shown in Fig. 3.12. Before conducting the rectenna measurement, the received power of the antenna was measured at the same angle as the rectenna measurement using power sensor B. We used a three-stub tuner (MS-N-811, NIHON KOUSHUHA) and an SMA cable to match the impedance between the designed inverted-F antenna and the system reference impedance of $50\,\Omega$. The insertion loss of the three-stub tuner and the SMA cable used in the received power measurement, as shown in Fig. 3.12, was measured. Finally, the input power to the rectifier circuit P_{in} was determined by deducting the insertion loss of the three-stub tuner and cable from the received power.

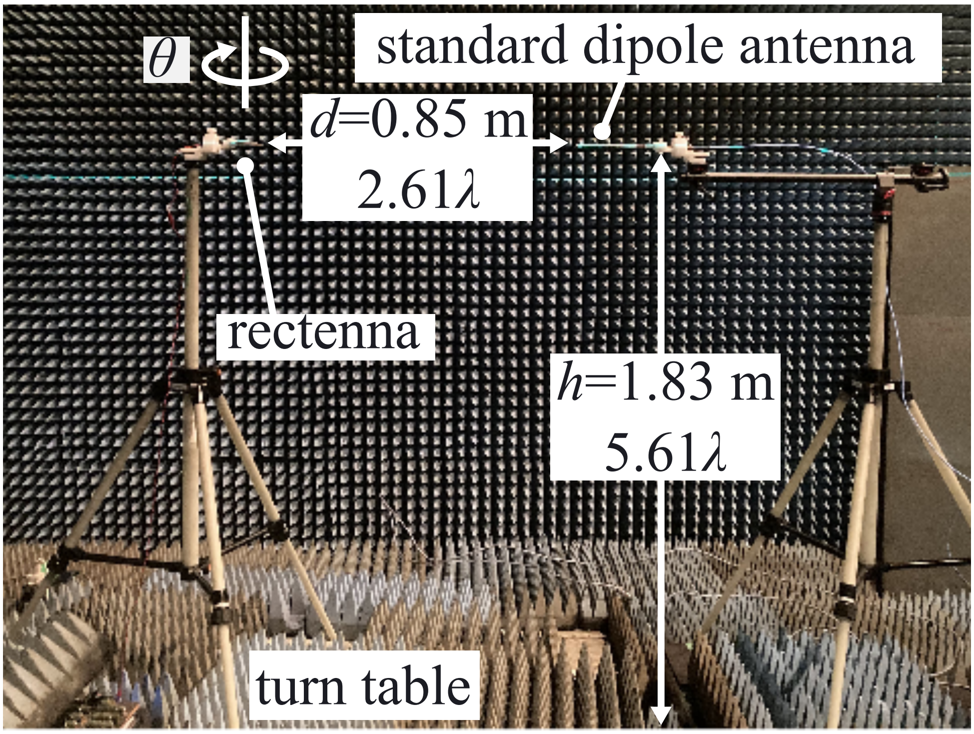


Figure 3.11: Photo of the rectenna measurement system.

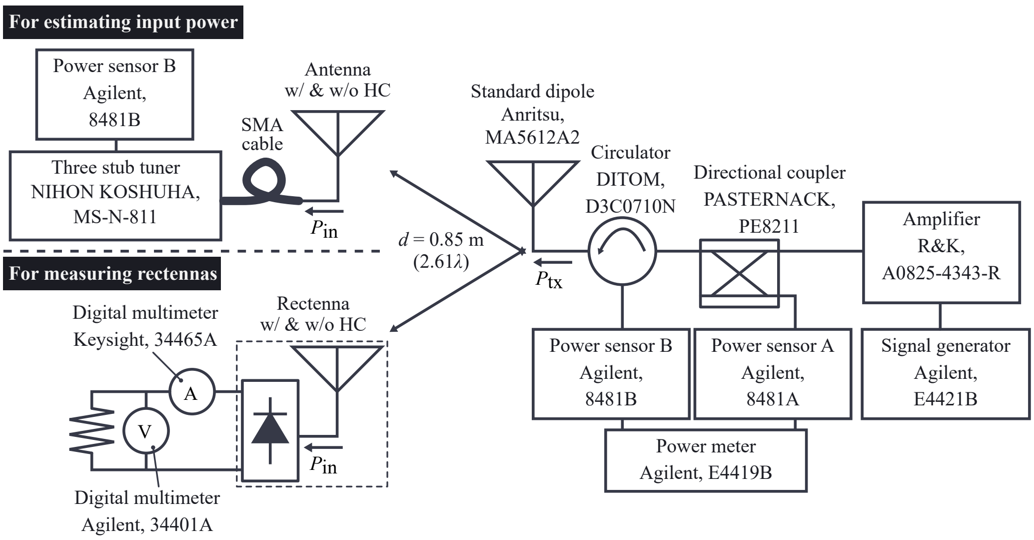
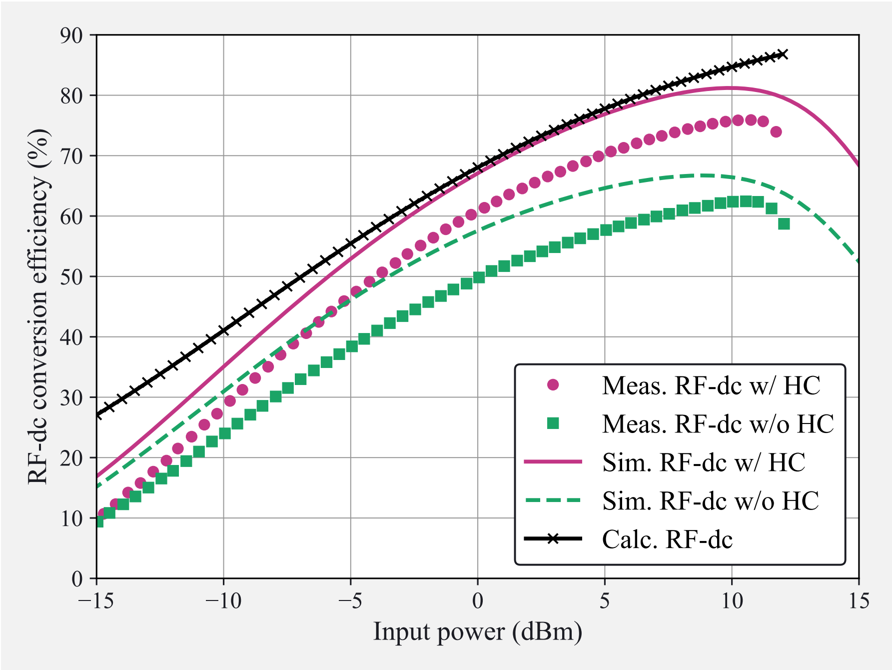
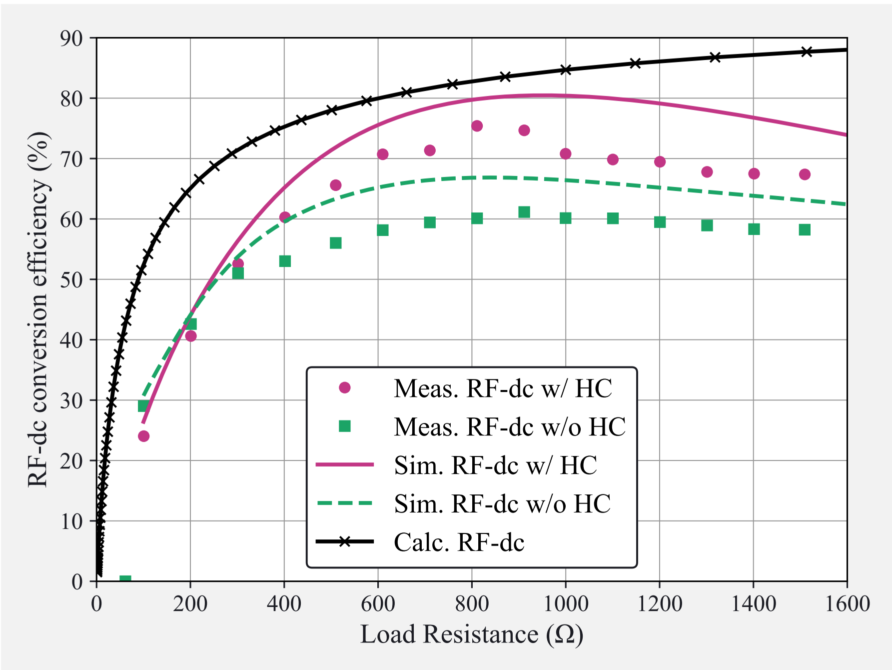


Figure 3.12: Outline of the rectenna measurement system.



(a)



(b)

Figure 3.13: Simulated and measured RF–dc conversion efficiency of the designed rectennas with and without harmonic control. (a) The RF–dc conversion efficiency vs. the input power at the load resistance of 1 kΩ. (b) The RF–dc conversion efficiency vs. the load resistance at the input power of 10.0 dBm.

Fig. 3.13 shows the theoretical, simulated, and measured RF–dc conversion efficiencies of the designed rectennas. The maximum measured RF–dc conversion efficiency of the rectenna with harmonic control reached 75.9% at an input power of 10.8 dBm and load resistance of 1 kΩ. In contrast, the rectenna without harmonic control achieved a maximum efficiency of 62.4% at an input power of 10.6dBm and load resistance of 1 kΩ. Both simulated and measured results demonstrate that the proposed rectenna with harmonic control of the antenna impedance has higher RF–dc conversion efficiency than the comparative rectenna without harmonic control. These comparative results confirm that the harmonic control of the antenna impedance effectively enhances RF–dc conversion efficiency. We compare the simulated and theoretical rectification efficiency results of the rectenna with harmonic control shown in Fig. 3.13. Across the range of input power and load resistance depicted in Fig. 3.13, the simulated efficiency closely aligns with the theoretical efficiency calculations. For an input power of 3 dBm in Fig. 3.13a, the rectification efficiency is 73.5% in the simulation and 74.2% in the theoretical calculation, with a difference of 0.7%. Similarly, in Fig. 3.13b, at a load resistance of 800 Ω, the rectification efficiency is 79.7% in the simulation and 83.0% in the theoretical calculation, with a difference of 3.3%. These results indicate that the proposed rectenna effectively reduces insertion of a matching circuit and harmonic losses by directly connecting the antenna with harmonic control, thereby maximizing the theoretical efficiency of the diode. In the measurement results of the rectenna with harmonic control shown in Fig. 3.13, the rectification efficiency is lower than that observed in the simulation. This discrepancy is likely due to errors arising from the diode SPICE parameters or manufacturing inaccuracies. Therefore, we consider that through re-tuning and redesign, the measured performance can be brought closer to that demonstrated in the simulation. Indeed, as shown in Fig. 2.8, which presents the measurement results of the rectification circuit discussed in Chapter 2, several rounds of redesign successfully achieved a close match between the simulation and measurement results. Table 3.4 compares the performance of rectennas operating in the 920 MHz band, demonstrating that the proposed rectenna achieves superior efficiency with a single diode compared to previous studies.

Table 3.4: Performance comparison of the rectennas around 920 MHz band.

References	Rectenna or Rectifier only	Rectifier type	Number of diodes	Efficiency(%) at P_{in}(dBm)
[76]	Rectifier only	Single-shunt	1	66.0 at 9.0
[47]	Rectifier only	Single-shunt	1	80.4 at 13.4
[77]	Rectenna	Charge-pump	2	71.0 at 0.0
[78]	Rectenna	Charge-pump	2	71.0 at 15.0
[79]	Rectenna	Charge-pump	2	81.0 at 11.0
[80]	Rectenna	Charge-pump	2	83.0 at -4.0
This work	Rectenna	Single-series	1	75.9 at 10.8

3.4.2 Angular characteristics

The radiation patterns of the proposed rectenna were evaluated on the XY and YZ planes using a far-field measurement system in an anechoic chamber. Additionally, the angular characteristics of the output dc power of the proposed rectenna were measured in another anechoic chamber. During the angular characteristics measurements, the transmission power P_{tx} was set to 35 dBm, and a load resistance of 1 kΩ was employed. The turntable shown in Fig. 3.11 facilitated the angular measurements. Fig. 3.14 shows both simulated and experimental results related to the designed inverted-F antenna's radiation patterns and the proposed rectenna's angular characteristics. The radiation pattern results have been normalized to their peak values. The peak output dc power of the rectenna with harmonic control was higher in the XY plane than in the YZ plane. The peak output dc power and angle of the rectenna with harmonic control were 8.05 dBm and 5° on the XY plane, respectively.

3.5 Conclusions

This chapter demonstrated that a novel single-diode rectenna can improve RF–dc conversion efficiency through harmonic control of the antenna impedance. We employed source-pull simulations encompassing the fundamental frequency and harmonics to achieve a highly efficient rectenna. Based on the source-pull simulation results, we designed the inverted-F antenna. Subsequently, we performed experimental measurements using the fabricated rectennas. Our findings indicate that the maximum RF–dc conversion efficiency for the designed rectenna reached 75.9% at an input power of 10.8 dBm and a load resistance of 1 kΩ. These measurements and comparisons to the comparative rectenna and previous studies underscore the achievement of full-wave rectification and high efficiency in the proposed single-series rectenna, where harmonic control is executed at the receiving antenna.

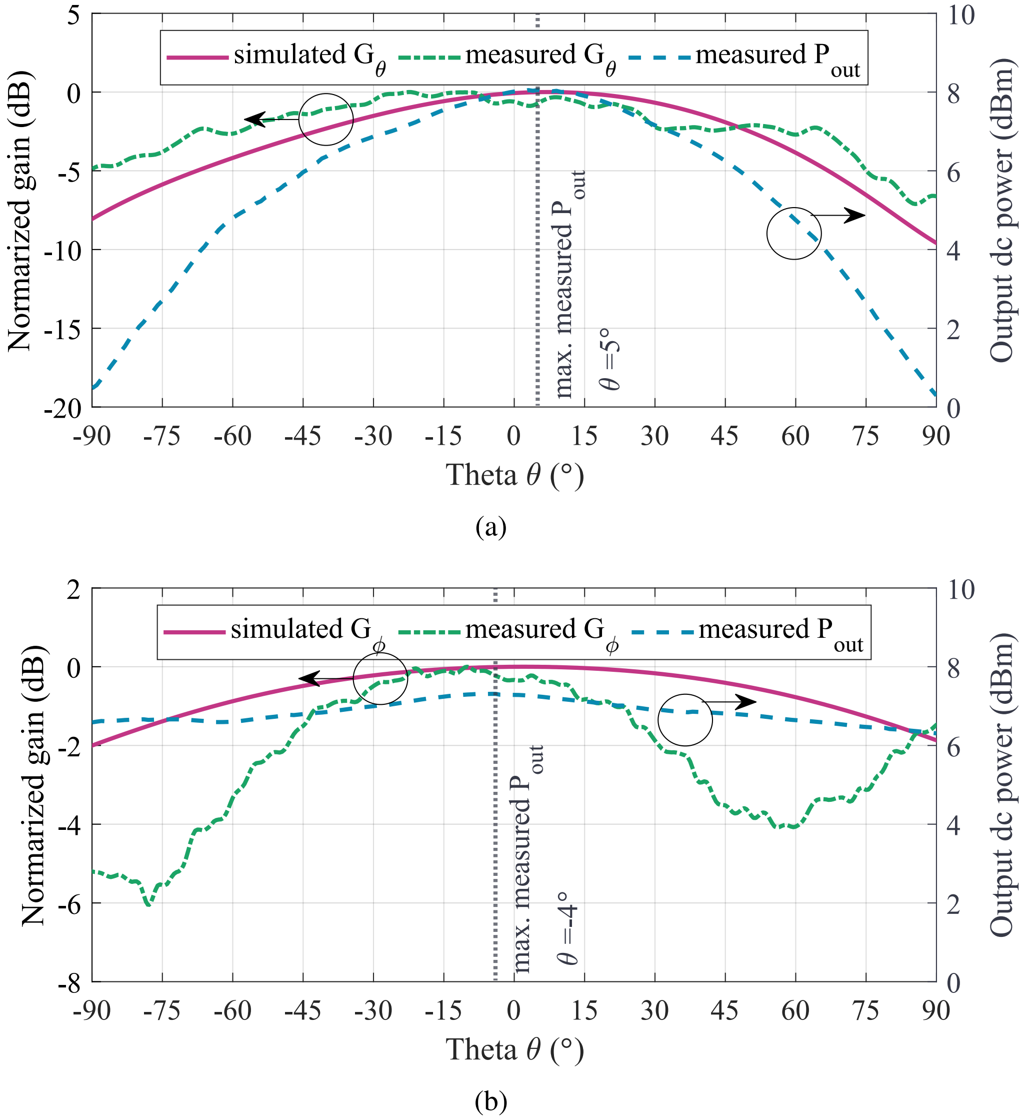


Figure 3.14: Simulattion and measurement results of the normalized gain of the designed antenna and the angular characteristics of the output dc power of the designed rectenna. (a) Results on the XY plane. (b) Results on the YZ plane.

Chapter 4

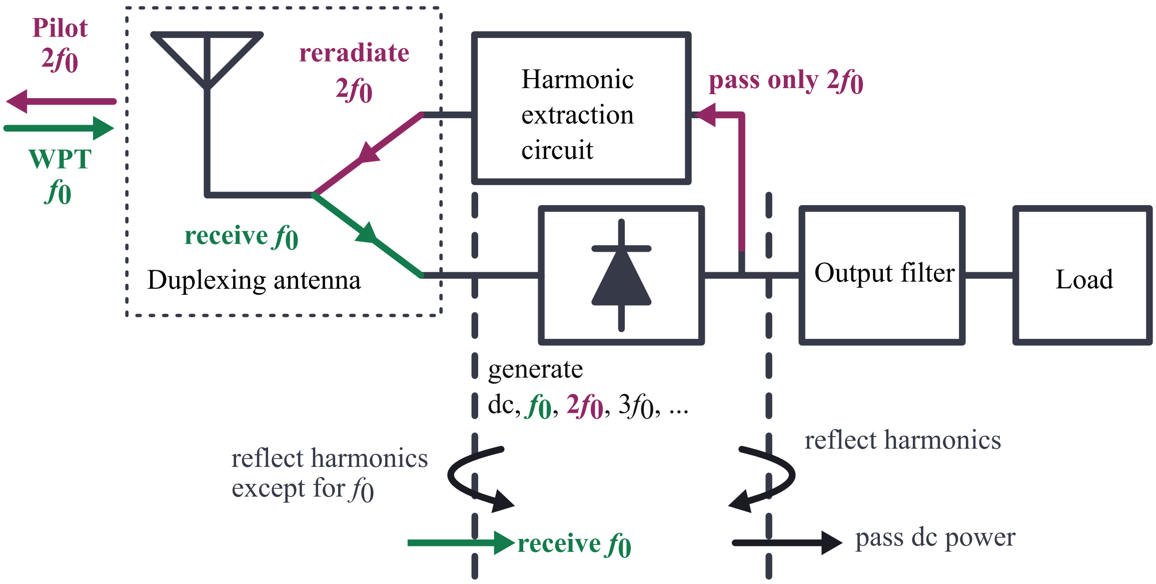
Development of a second harmonic reradiating rectenna for harmonic retrodirective systems

4.1 Introduction

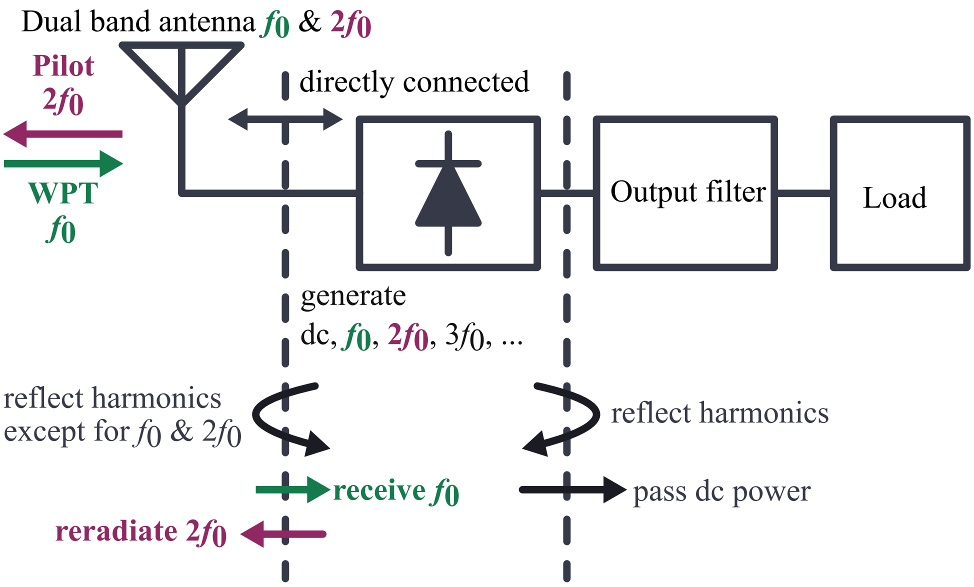
In Chapter 3, the harmonic source-pull simulation is introduced for rectenna design. This chapter explains the application of rectenna design using harmonic source-pull simulation to develop a rectenna capable of reradiating second harmonics.

The rapid growth of the Internet of Things (IoT) and wearable devices has created the challenge of battery charging and replacement [81]. Far-field radiative wireless power transfer (WPT) addresses these power supply issues [82]. In far-field radiative WPT, electromagnetic waves emitted by a transmitting array antenna are captured and converted into dc power by a rectenna, which combines a receiving antenna and a rectifier circuit. Rectennas are considered alternatives to batteries or supplementary power sources. The benefits of far-field radiative WPT include the ability to power multiple and mobile devices wirelessly and the potential for simultaneous wireless information and power transfer [83].

Target tracking is crucial for far-field radiative WPT systems used for mobile devices. A retrodirective beam control system is a target-tracking method in the wireless communications industry. This system performs beam control by taking the phase conjugate of a pilot signal transmitted from the receiving device. As a result, the peak power density of the beam decreases in the absence of the pilot signal. Due to its inherent safety, this system is also applied to far-field radiative WPT [10, 84]. However, this system requires a pilot signal from the receiving device, making it challenging to obtain this signal from a non-charged device.



(a) Previous rectenna [75]



(b) Proposed rectenna

Figure 4.1: Circuit diagram and the signal flow of a rectenna reradiating the second harmonic (a) proposed in [75] and (b) proposed in this study.

During the rectification process in rectifying diodes, harmonics are unintentionally generated [51]. Several studies have focused on harmonic retrodirective systems that reuse these harmonics as pilot signals [75, 85–88]. The power level of harmonics generated by rectifying diodes is higher for lower orders [75]. Therefore, these retrodirective systems mainly consider reusing the second and third harmonics. When the second harmonic is used as a pilot signal, its pure power level is higher than that of the third harmonic. Therefore, reusing the second harmonic implies the possibility of achieving higher levels of the pilot signal that the transmitter can receive.

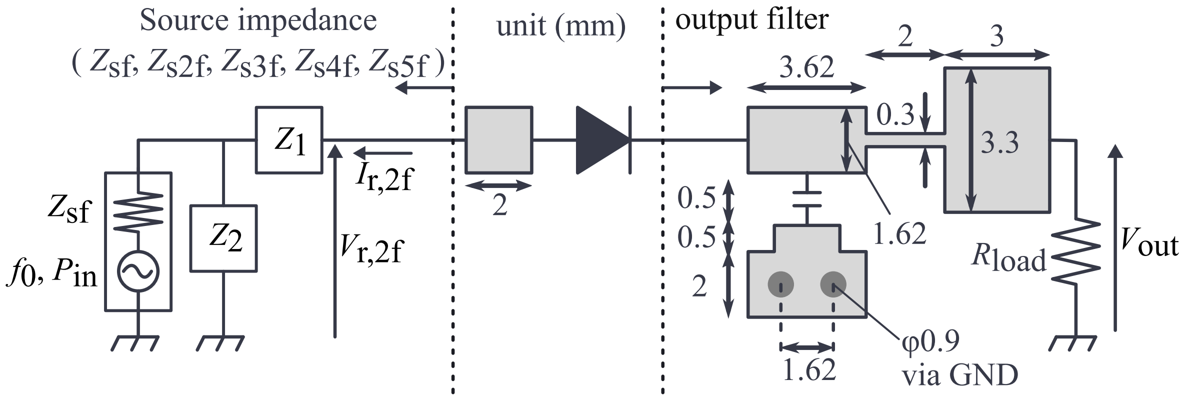
The previous study [75] proposed a duplexing dipole antenna to reradiate the second harmonic from the rectenna, as shown in Fig. 4.1a. A filter was integrated with the output filter of the charge pump rectifier circuit, allowing for the efficient extraction of the second harmonic. This design provided higher RF–dc conversion efficiency and harmonic reradiation levels than existing models. However, the trade-off between RF–dc conversion efficiency and the second harmonic level in the rectenna was not explicitly addressed. Moreover, the rectenna proposed in [75] requires an additional filter and a coupler for second harmonic extraction. Due to the insertion losses caused by these additional components, the harmonic reradiation level decreases. Therefore, a more detailed understanding of the maximum harmonic reradiation level, its efficiency trade-off, and an efficient rectenna design method is required.

This study proposes a rectennas design method that provides high RF–dc conversion efficiency and enhanced second harmonic reradiation levels by employing source-pull simulation with harmonics. Source-pull techniques, commonly used in high-frequency amplifier design [60–62], have also been adapted for rectenna design [67, 89–92]. This study aimed to design a rectenna with an objective function in a source-pull simulation encompassing both RF–dc conversion efficiency and second harmonic reradiation levels. The receiving antenna was designed to match the target impedance obtained from the source-pull simulation. The designed antenna was directly connected to a rectifier circuit, as shown in Fig. 4.1b. This method facilitates direct second harmonic extraction and reradiation from the antenna, eliminating the need for additional filters. This paper outlines the proposed design method and discusses the trade-off between RF–dc conversion efficiency and second harmonic reradiation levels using source impedance contour plots on a Smith chart.

4.2 Rectenna design

4.2.1 Rectifier design method using the source-pull simulation

We explain the difference between the conventional rectenna, which only enhances RF–dc conversion efficiency, and the proposed rectenna, which enhances the second harmonic reradiation level while maintaining high RF–dc conversion efficiency. The input and output filters flanking



	dc	f_0	$2f_0$	$3f_0$	$4f_0$	$5f_0$
Z_1	0 Ω	0 Ω	Z_{s2f}	Z_{s3f}	Z_{s4f}	Z_{s5f}
Z_2	0 Ω	10^{21}Ω	0 Ω	0 Ω	0 Ω	0 Ω

0 Ω : short
10^{21}Ω : open

Figure 4.2: Circuit diagram of the source-pull simulation with harmonics conducted in this study. 0 Ω and 10^{21} Ω represent short and open circuits, respectively. f_0 is the fundamental frequency, and Z_{snf} is the source impedance at the n-th harmonics.

the diode in a conventional rectenna reflect harmonics. This reflection enhances RF–dc conversion efficiency by confining harmonic power within the diode, thereby preventing losses. In the proposed rectenna, shown in Fig. 4.1b, the output filter reflects harmonics similarly to the conventional rectenna. However, the proposed rectenna directly connects the receiving antenna to the rectifier circuit without an input filter. Unlike the conventional rectenna's input filter, the antenna in the proposed rectenna does not reflect the second harmonic but reflects the other harmonics. The diode can be represented as a current source generating the second harmonic [93]. The proposed antenna is designed to match the impedance of the current source and the antenna at the second harmonic, allowing the antenna to reradiate the second harmonic. This rectenna design enables the reuse of the second harmonic for reradiation instead of rectification while minimizing the decrease in RF–dc conversion efficiency due to harmonic losses, except for the second harmonic.

Fig. 4.2 shows the circuit diagram of the source-pull simulation for the rectifier circuit. The circuit type is a single-series rectifier circuit. The dielectric substrate is R5775K from Panasonic, characterized by a dielectric constant of 3.62, a tangential constant of 0.0046, a substrate thickness of 0.75 mm, and a metal thickness of 18 μm. The characteristic impedance of the microstrip line was set to 50 Ω, and the reference line width was set to 1.62 mm. The rectifying diode was the SMS7621 from Skyworks, with its equivalent circuit and SPICE parameters shown in Fig. 3.5 and Table 3.2 in Chapter 3. We used the Advanced Design System (ADS) from

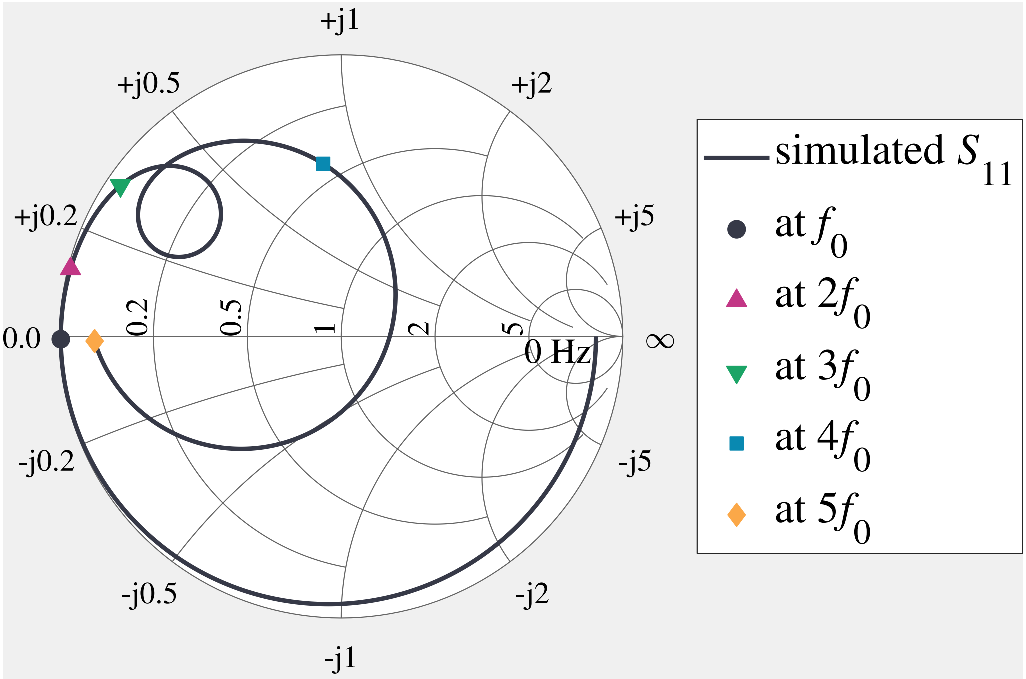


Figure 4.3: Simulated reflection coefficient of the output filter from 0 Hz to 4.6 GHz.

Keysight Technologies for the circuit simulation, employing the harmonic balance method to analyze the rectifier circuit. The fundamental frequency was set at 920 MHz, and the maximum order for harmonic balance was fixed at the fifth order.

Source/load pull is an analysis technique that sweeps the source and load impedances, the input impedances of each harmonic of the input/output circuit across the diode. Therefore, the frequency response of the input impedance of the output filter (load impedance) affects the source-pull simulation results. Since the proposed rectenna reradiates the second harmonic directly from the antenna, the source pull, which determines the input impedance of the antenna, is essential. Consequently, this study's output filter was first designed, and the source-pull simulation was performed with the load impedance fixed. The output filter, shown in Fig. 4.2, consists of a simple circuit with a capacitor (GJM1552C1H430JB01, Murata; capacitance: 43 pF) connected in parallel with the load. The output filter was analyzed using EM simulation in ADS. Fig. 4.3 shows the simulated reflection coefficient of the output filter. The results indicate that the output filter provides a short circuit at the fundamental frequency and the second, third, and fifth harmonics. The source-pull simulation was performed using this designed output filter.

Fig. 4.2 shows the circuits representing impedances Z_1 and Z_2 connected to the power supply circuit for the source-pull simulation. The circuits Z_1 and Z_2 were assigned individual impedances for each harmonic. The circuit Z_1, connected in series to the power supply, provided the source impedance for the second to fifth harmonics. The circuit Z_2, connected in parallel on the power supply side, provided a short circuit for higher-order harmonics beyond the second harmonic. To independently provide a source impedance at the fundamental frequency, Z_1 was short-circuited, Z_2 was open-circuited, and the power supply provided the source impedance at the fundamental frequency. In a single-series rectenna, it is necessary to short-circuit the anode side of the diode to apply a dc reverse bias, and hence, Z_1 and Z_2 provided the short circuit at dc. An open circuit was set at $10^{21}\,\Omega$, and a short circuit was set at $0\,\Omega$. The source impedance Z_{snf} at each harmonic was set using equations Eq. (3.2) and Eq. (3.3) as in Chapter 3. The RF–dc conversion efficiency η was calculated as the ratio of the input RF power P_{in} to the output dc power $P_{\mathrm{out,dc}}$ using the following formula:

$$\eta = \frac{P_{\mathrm{out,dc}}}{P_{\mathrm{in}}} \times 100\% = \frac{V_{\mathrm{out}}^2}{P_{\mathrm{in}} R_{\mathrm{load}}} \times 100\%, \tag{4.1}$$

where V_{out} and R_{load} represent the output dc voltage and load resistance, respectively. Furthermore, we defined the second harmonic reradiation level from the rectenna as the power level of the second harmonic reflected the power supply side using the following formula:

$$P_{\mathrm{2nd}} = \frac{1}{2}\Re\left(I_{\mathrm{r,2f}} V_{\mathrm{r,2f}}\right), \tag{4.2}$$

where $I_{\mathrm{r,2f}}$ and $V_{\mathrm{r,2f}}$ represent the reflected second harmonic current and voltage at the power supply, respectively.

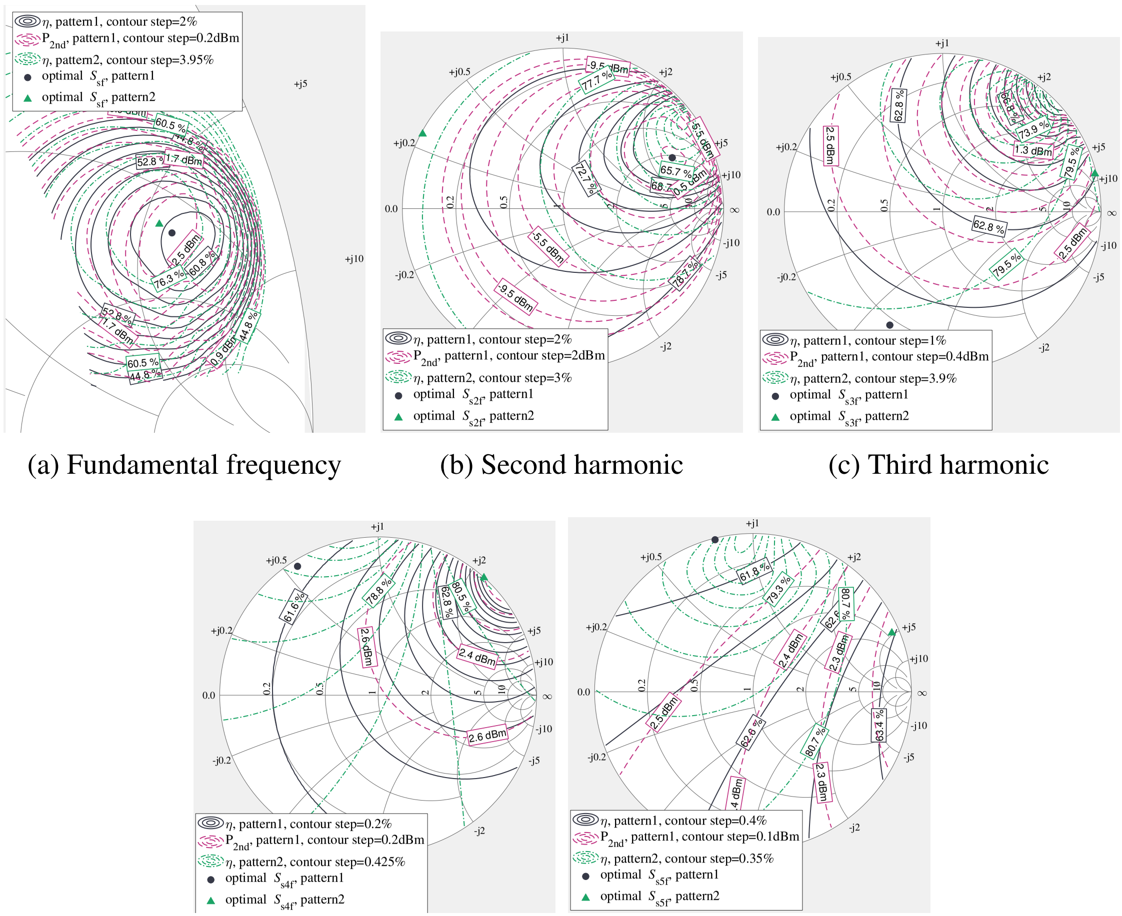
The source-pull simulation was conducted in the following two steps:

1. Optimization of each harmonic source impedance.
2. Sweeping each harmonic source impedance individually.

In step 1, the optimization variables were the magnitude M_n and phase D_n of each harmonic source impedance as explained in Eq. (3.3). We fixed the input power at 10 dBm and the load resistance at 1.0 kΩ during the optimization. The optimization target function was set in two patterns:

- Pattern 1: Both the RF–dc conversion efficiency and the second harmonic level were set as the optimization target functions. This setting is for this study.
- Pattern 2: Only the RF–dc conversion efficiency was set as the optimization target function. This setting compares with Pattern 1 to confirm the trade-off between RF–dc conversion efficiency and the second harmonic reradiation level.

The optimization variables were randomly swept in both patterns to maximize the target functions. In step 2, each harmonic source impedance was individually swept. The source impedances for harmonics other than the one being swept were fixed to the values obtained in step 1. The harmonic source impedances were swept by varying the reflection coefficient magnitude M_n from 0.01 to 0.99 in steps of 0.005 and the reflection coefficient phase D_n from 0° to 360° in 1° increments. Equations Eq. (3.2) and Eq. (3.3) show that $Z_{sn\mathrm{f}}$ diverges when $M_n = 1$. Therefore, we avoided assigning $D_n = 1$.



(a) Fundamental frequency (b) Second harmonic (c) Third harmonic

(d) Fourth harmonic (e) Fifth harmonic

Figure 4.4: Source-pull simulation results for each harmonic. The fundamental frequency, input power, and load resistance are 920 MHz, 10 dBm, and 1.0 kΩ, respectively. The black solid and red dashed contours represent the RF–dc conversion efficiency and the second harmonic reradiation level of pattern 1, respectively. The green contour represents the RF–dc conversion efficiency of pattern 2. The markers represent the optimal source impedance achieved through optimization.

Fig. 4.4 shows the source-pull simulation results for each harmonic's RF–dc conversion efficiency and the second harmonic level. The contours represent the RF–dc conversion efficiency of patterns 1 and 2 and the second harmonic level of pattern 1. Each point indicates the optimal source impedance achieved through optimization for patterns 1 and 2. The highest RF–dc conversion efficiency and second harmonic level of pattern 1 were 61.5% and 2.67 dBm, respectively, while the highest RF–dc conversion efficiency of pattern 2 was 81.0%.

Fig. 4.4a is an enlarged view of the upper right part of the Smith chart. In pattern 1, the range for achieving high RF–dc conversion efficiency coincides with the range for a high second harmonic level. The source impedance at the fundamental frequency is the complex conjugate of the input impedance of the diode at the fundamental frequency. FFig. 4.4a indicates that the input impedances of the diode at the fundamental frequency in patterns 1 and 2 are not significantly different. Furthermore, the sensitivity of the RF–dc conversion efficiency and the second harmonic level to the fundamental source impedance are more significant than that observed for the other harmonics. Therefore, adjusting the fundamental input impedance is paramount to the antenna design.

Fig. 4.4b shows that the ranges yielding an efficiency of 78.7% or higher differ from those obtaining a high second harmonic level of 0.5 dBm or higher in pattern 1, unlike the results obtained at the fundamental frequency. The range with a high RF–dc conversion efficiency for pattern 1 is located in the lower right part of the Smith chart, where the reflection coefficient magnitude is close to 1. Meanwhile, the range for a high second harmonic level in pattern 1 is located in the upper right part, where the reflection coefficient magnitude is approximately 0.5. The contours of pattern 1 demonstrate the trade-off relationship between the second harmonic reradiation level and the RF–dc conversion efficiency. Reradiating the second harmonic without reflecting it to the diode side disturbs the rectification waveform and reduces the RF–dc conversion efficiency. The trade-off between the RF–dc conversion efficiency and the second harmonic level shown in Fig. 4.4b is consistent with this phenomenon. Compared to pattern 1, the range corresponding to a high RF–dc conversion efficiency in pattern 2 is located in the left part of the Smith chart, where the reflection coefficient magnitude is close to 1. A high RF–dc conversion efficiency is obtained by reflecting the second harmonic back to the diode side in both patterns. The reflection coefficient phases required to achieve high RF–dc conversion efficiency for patterns 1 and 2 differ due to the differences in the fixed source impedances at the other harmonics.

Fig. 4.4c shows that the third source impedance for obtaining a high second harmonic level in pattern 1 is located on the lower left side of the Smith chart. Similar to the second harmonic results, there is a trade-off relationship between the RF–dc conversion efficiency and the second harmonic level for the third harmonic. The reflection coefficient magnitudes required to achieve high RF–dc conversion efficiency in patterns 1 and 2 are near 1. Meanwhile, the reflection coefficient phases required to obtain high RF–dc conversion efficiency in patterns 1 and 2 differ.

Fig. 4.4d and Fig. 4.4e show that the variations in RF–dc conversion efficiency and second harmonic level due to changes in the fourth and fifth-harmonic source impedances were 2.6 points and 0.8 dB, and 1.6 points and 0.3 dB in pattern 1, respectively. These results indicate greater design flexibility for the fourth- and fifth-harmonic source impedances than lower-order harmonics.

Fig. 4.4 shows that the rectenna design's lower-order harmonic impedance is more critical. Consequently, we set the design targets for the antenna input impedance (source impedance) only for the fundamental, second, and third harmonics. The design targets for these harmonics were set to achieve an RF–dc conversion efficiency of 60.8% or higher and a second harmonic level of 1.7 dBm or higher.

4.2.2 Antenna design

We designed a receiving antenna based on the source-pull simulation results. Fig. 4.5 shows a schematic of the designed antenna. In a single-series rectenna, it is necessary to short-circuit the anode side of the diode at dc. To meet this requirement, we used an inverted-F antenna with a short-circuited point as the primary form of the receiving antenna. CST T-solver was used for the antenna design. The dielectric substrate was the same R5775K used in the rectifier circuit. The analysis was conducted by connecting a waveguide port to position #1 in Fig. 4.5, with a positive direction along the Y-axis. The angles θ and ϕ shown in Fig. 4.5 are measured from the positive direction of the Y-axis to the positive directions of the X and Z axes, respectively.

The source-pull simulation results show that the antenna input impedance at the fundamental frequency is dominant. Initially, we adjusted the primary inverted-F antenna parameters without a back stub. The design target for the fundamental input impedance is to achieve high impedance. For this purpose, we adjusted the distance x between the short-circuited point and the feed point, as well as the feed line width w of the inverted-F antenna without a back stub. Fig. 4.6a shows the input impedance of the inverted-F antenna without the back stub (length x, 2.8 mm and width w, 0.5 mm). These adjustments yielded a high fundamental input impedance, but the second harmonic input impedance was also high, exceeding the target range. The short-circuit stub was inserted on the back side of the substrate, as shown in Fig. 4.6b. This short stub adjusts the second harmonic source impedance to a reflection coefficient of 0.5. The insertion position x_2 of the back stub was adjusted to tune the second harmonic source impedance with the feed line position fixed. Fig. 4.6b shows the changes in the antenna input impedance when the insertion position x_2 is varied. It demonstrates that adding the back stub minimally affected the input impedance at the fundamental frequency. Furthermore, increasing the insertion position x_2 of the back stub brings the second harmonic input impedance closer to the absolute value of the reflection coefficient of 0.5. Finally, the feed line length l was adjusted to rotate the

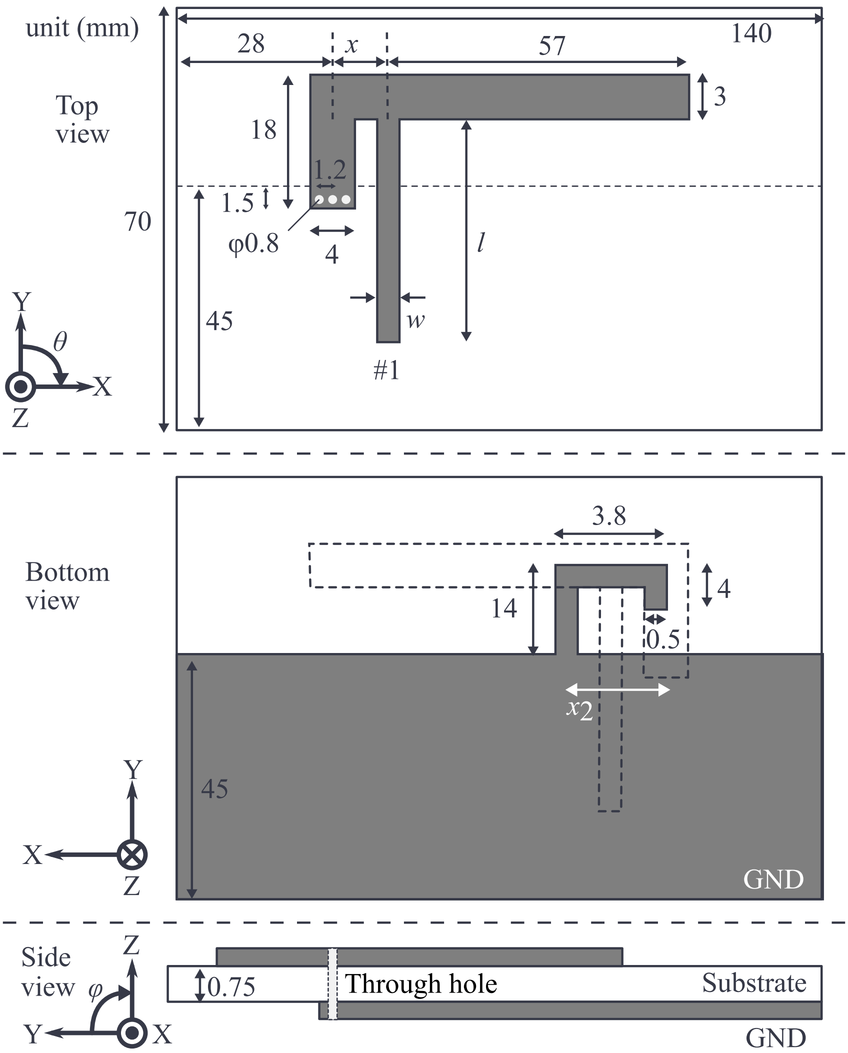
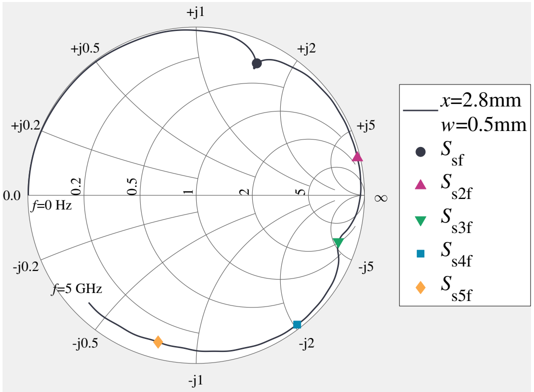
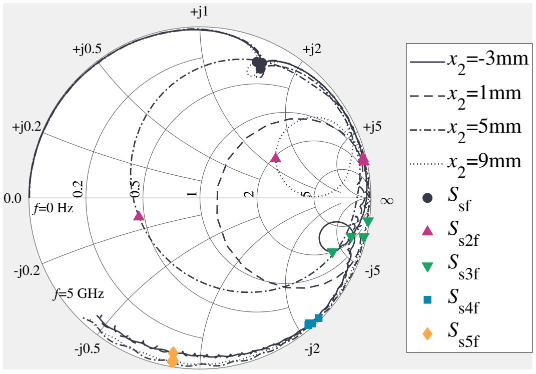


Figure 4.5: Schematic of the designed antenna. The primary form of the antenna is an inverted-F antenna. The label #1 is the input port directly connected to the rectifier circuit.

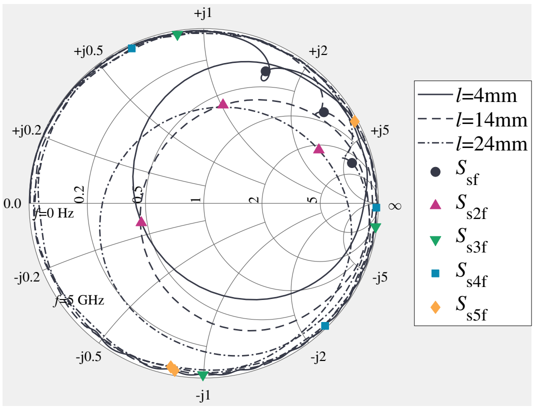
input impedance of the fundamental and the second harmonic around the center of the Smith chart. Figure 4.6c shows the changes in input impedance when the line length l is varied; the longer the feed line length l, the more the input impedance rotates. At a line length l of 24 mm, the input impedance for the fundamental and second harmonics falls within the design target range. Based on the antenna analysis results, we set the feed line width www to 0.5 mm, the distance x between the feed point and the short-circuit point to 2.8 mm, the position of the back short-circuit stub x_2 to 5 mm, and the feed line length l to 24 mm.



(a) Results without a back stub



(b) Results of sweeping x_2



(c) Results of sweeping l

Figure 4.6: Simulated antenna input impedance of the designed antenna from 0 Hz to 5 GHz as the variables x, w, x_2, and l are adjusted. (a) Results corresponding to $x = 2.8$ mm and $w = 0.5$ mm without a back stub. (b) Results corresponding to x_2 varied from -3 mm to 9 mm, with $x = 2.8$ mm, $w = 0.5$ mm, and $l = 4$ mm. (c) Results corresponding to l varied from 4 mm to 24 mm, with $x = 2.8$ mm, $w = 0.5$ mm, and $x_2 = 5$ mm.

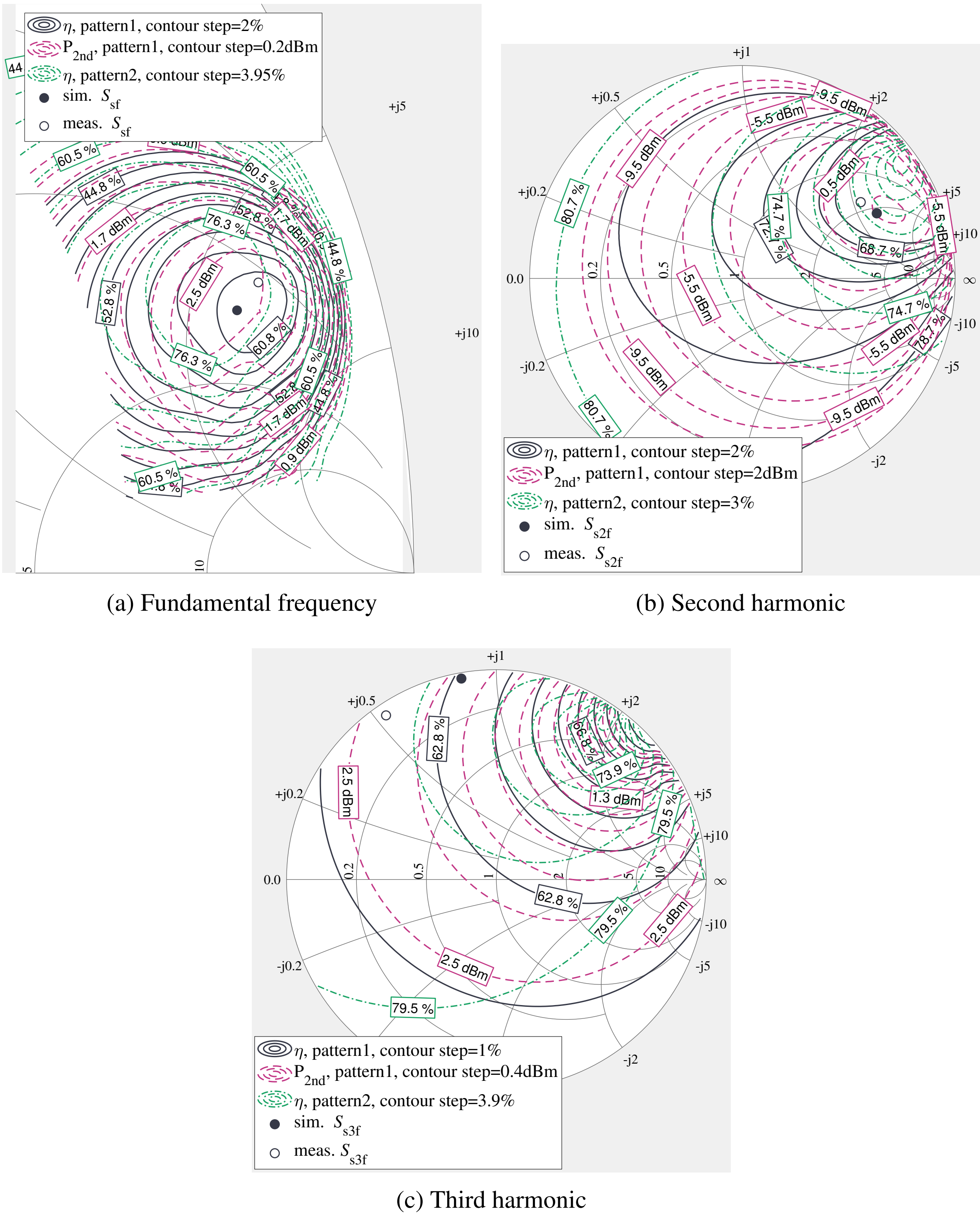
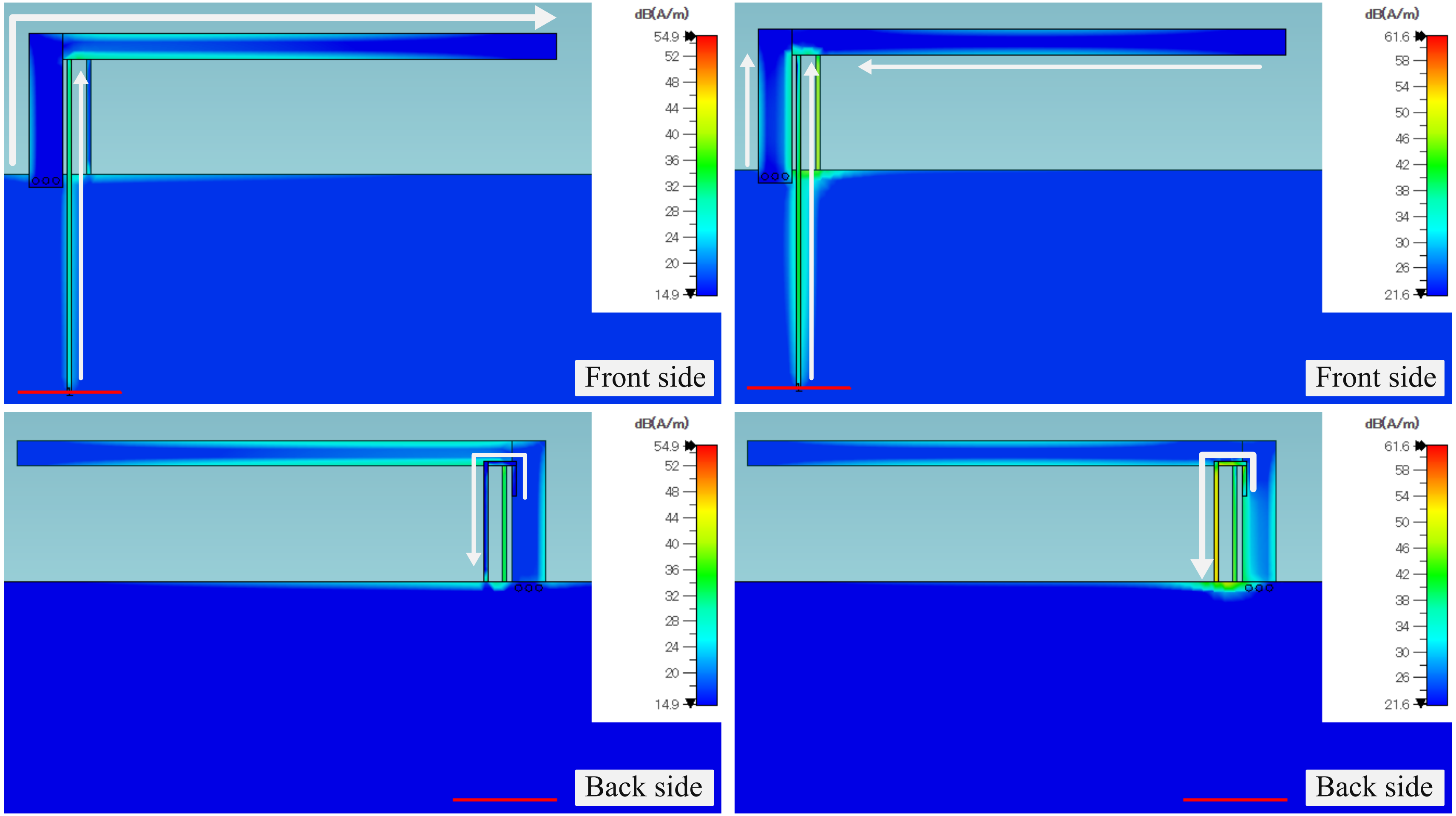


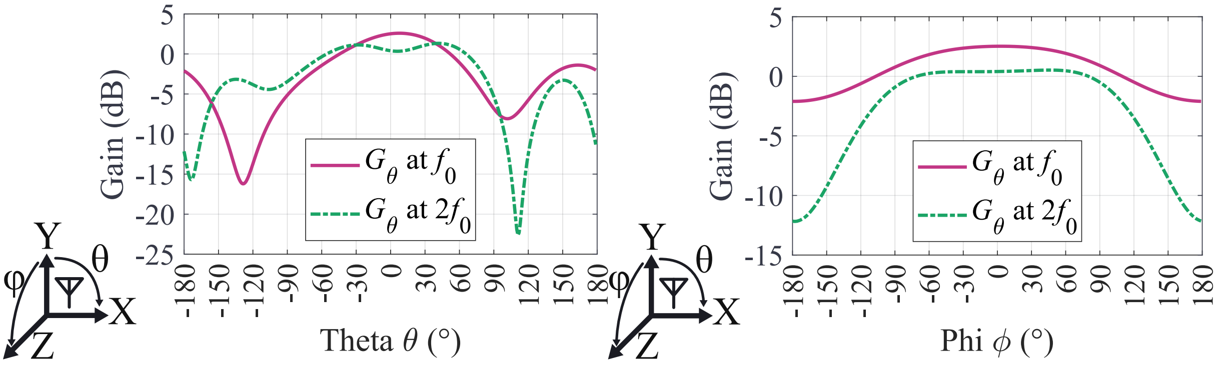
Figure 4.7: Measurement and simulation results of the reflection coefficient of the designed antenna. The target impedance is the range in which the efficiency and second harmonic level exceed 60.8% and 1.7 dBm, respectively. The black and white dots are the simulation and measurement results, which are within the target impedance ranges. The results obtained for (a) the fundamental frequency, (b) the second harmonic, and (c) the third harmonic.



(a) Fundamental frequency

(b) Second harmonic

Figure 4.8: Simulation results of the surface current distribution at (a) the fundamental frequency and (b) the second harmonic. The arrows represent the direction of the current.



(a) XY plane (b) YZ plane

Figure 4.9: Simulated radiation pattern of the designed antenna at the fundamental frequency and the second harmonic on (a) the XY plane and (b) the YZ plane.

Fig. 4.7 shows the simulation and measurement results of the designed antenna's reflection coefficient. The measurement results also show that the input impedances for the fundamental and second harmonics are within the target range.

Fig. 4.8 and Fig. 4.9 show the simulated surface current distributions and radiation patterns at the fundamental frequency and the second harmonic, respectively. At the fundamental frequency, the current flows mainly through the stub on the front side, as shown in Fig. 4.8a, so the antenna acts as a typical inverted-F antenna. Thus, the radiation pattern on the XY plane becomes unidirectional, as shown inFig. 4.9a. At the second harmonic, the current flows in the back stub as well, with the current in the back stub and the current in the short-circuit stub on the front side being in opposite phases, as shown in Fig. 4.8b. These opposing phases neutralize the radiation from both sides. Consequently, the current on the open stub on the front side dictates the primary radiation pattern, rendering the radiation pattern on the XY plane at the second harmonic predominantly unidirectional, as shown in Fig. 4.9a.

The simulated radiation efficiencies of the designed antenna for the fundamental frequency and the second harmonic were 87.6% and 73.6%, respectively. The simulated front gain on the XY plane for the fundamental frequency was 2.35 dBi, while that for $\theta = 90°$ on the XY plane for the second harmonic was -3.82 dBi.

4.3 Experimental demonstrations

4.3.1 Measurement setup

Fig. 4.10 shows photographs of the designed single-series rectenna. Fig. 4.11 and Fig. 4.12 show a photograph and block diagram of the system used to measure the rectenna performance.

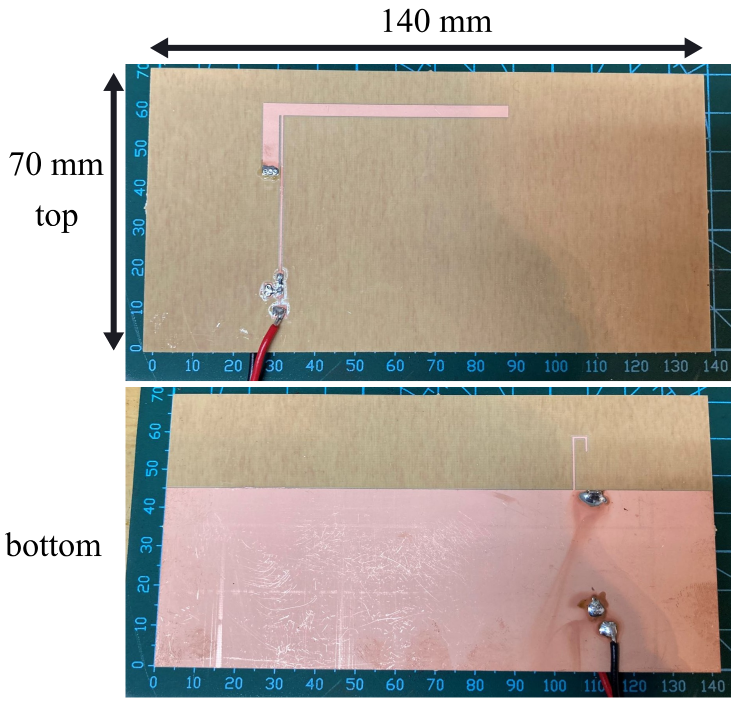


Figure 4.10: Photographs of the designed rectenna.

Measurements were performed in an anechoic chamber at the Microwave Energy Transmission Laboratory (METLAB) at Kyoto University. A standard dipole antenna for the 900 MHz band (Anritsu, MA5612A2) was used as the fundamental transmission antenna, and a standard dipole antenna for the 1.8 GHz band (Anritsu, MA5612B2) was used as the second harmonic receiving antenna. The rectenna and two standard dipole antennas were installed 0.75 m above the ground, as shown in Fig. 4.11. The fundamental transmission dipole antenna and the rectenna were installed facing each other and separated by a distance of 0.8 m. The second harmonic receiving dipole antenna was installed at a distance of 1.0 m with $\theta = 90^\circ$ on the XY plane of the rectenna. The power input to the rectenna P_{in} was calculated using the Friis transmission formula, as shown here:

$$P_{\mathrm{in}} = P_{\mathrm{tx,f}} G_{\mathrm{tx,f}} G_{\mathrm{rx,f}} \left(\frac{\lambda_f}{4\pi d_1} \right)^2, \tag{4.3}$$

where $P_{\mathrm{tx,f}}$, $G_{\mathrm{tx,f}}$, $G_{\mathrm{rx,f}}$, λ_{f}, and d_1 represent the transmission power, gain of the standard dipole antenna for the fundamental frequency, front gain of the rectenna at the fundamental frequency, free-space wavelength at the fundamental frequency, and the distance between the rectenna and the dipole for the fundamental frequency, respectively. The level of the second harmonic reradiated from the rectenna P_{2nd} was calculated using the Friis transmission formula as follows:

$$P_{\mathrm{2nd}} = \frac{P_{\mathrm{rx,2f}}}{G_{\mathrm{tx,2f}} G_{\mathrm{rx,2f}}} \left(\frac{4\pi d_2}{\lambda_{2f}} \right)^2, \tag{4.4}$$

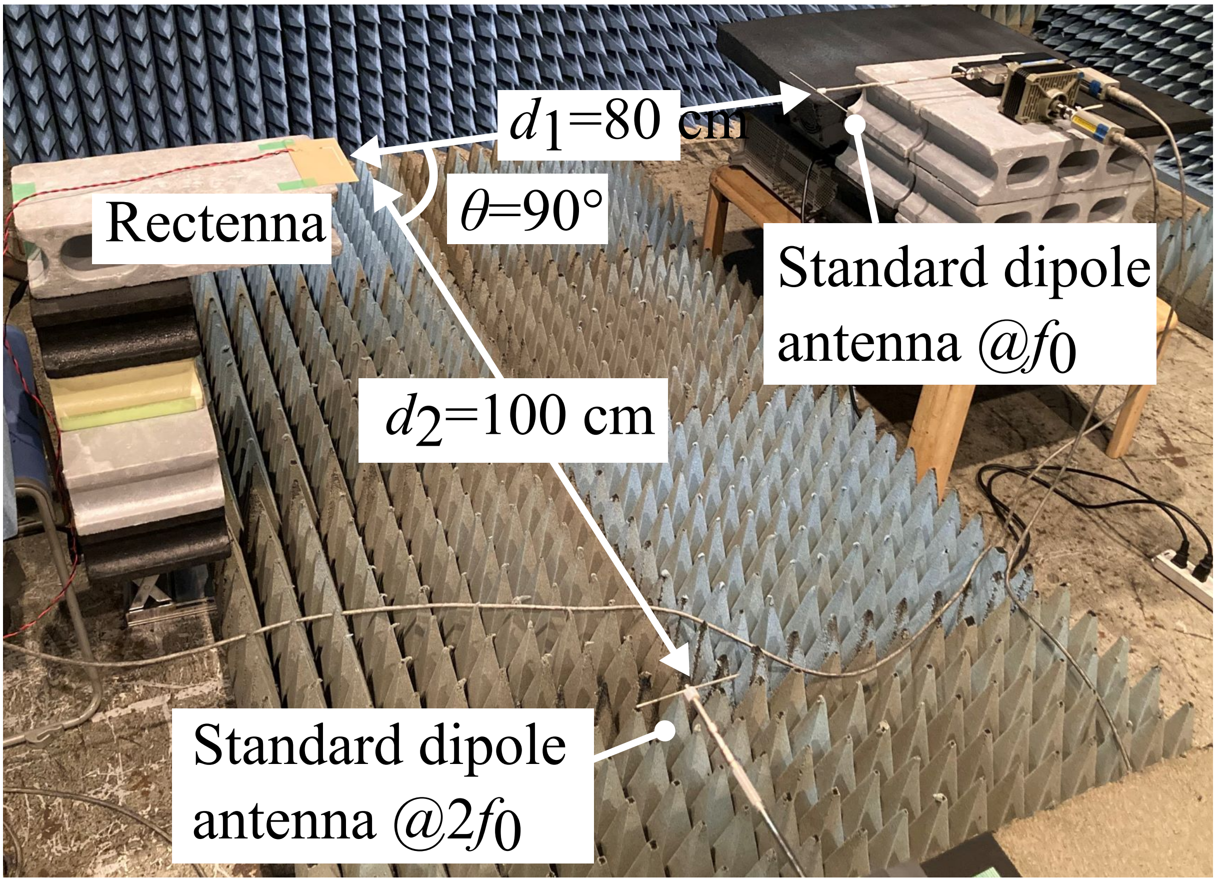


Figure 4.11: Measurement setup for the rectenna.

where $P_{\mathrm{rx,2f}}$, $G_{\mathrm{tx,2f}}$, $G_{\mathrm{rx,2f}}$, λ_{2f}, and d_2 represent the power received by the standard dipole antenna for the second harmonic, the gain of the rectenna at $\theta = 90°$ on the XY plane at the second harmonic, gain of the standard dipole antenna for the second harmonic, free-space wavelength at the second harmonic, and the distance between the rectenna and the dipole for the second harmonic, respectively. Calibrated values were used to gain the standard dipole antennas, and simulation values were used to gain the rectenna. The gains of the standard dipole antennas for the fundamental frequency and second harmonic are $G_{\mathrm{tx,f}} = 1.8\,\mathrm{dBi}$ and $G_{\mathrm{rx,2f}} = 3.01\,\mathrm{dBi}$, respectively.

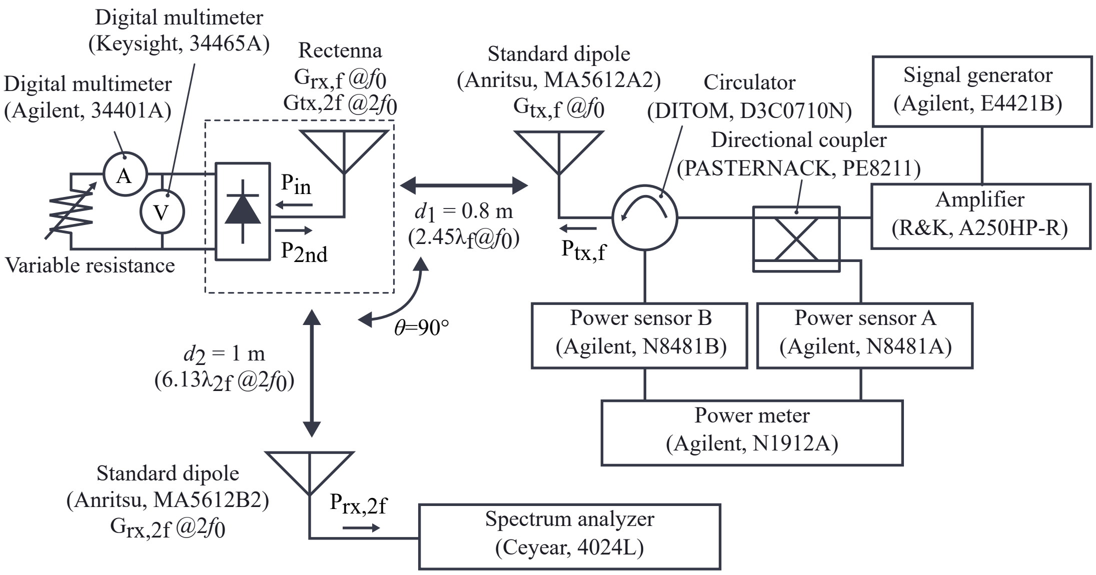
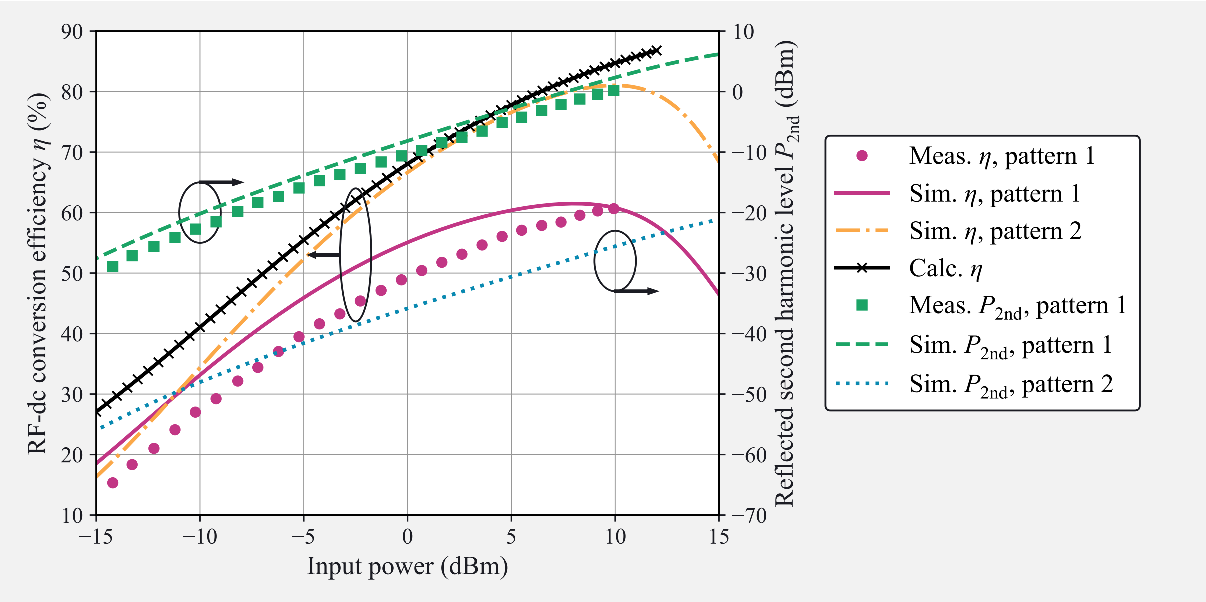


Figure 4.12: Block diagram of the measurement system.

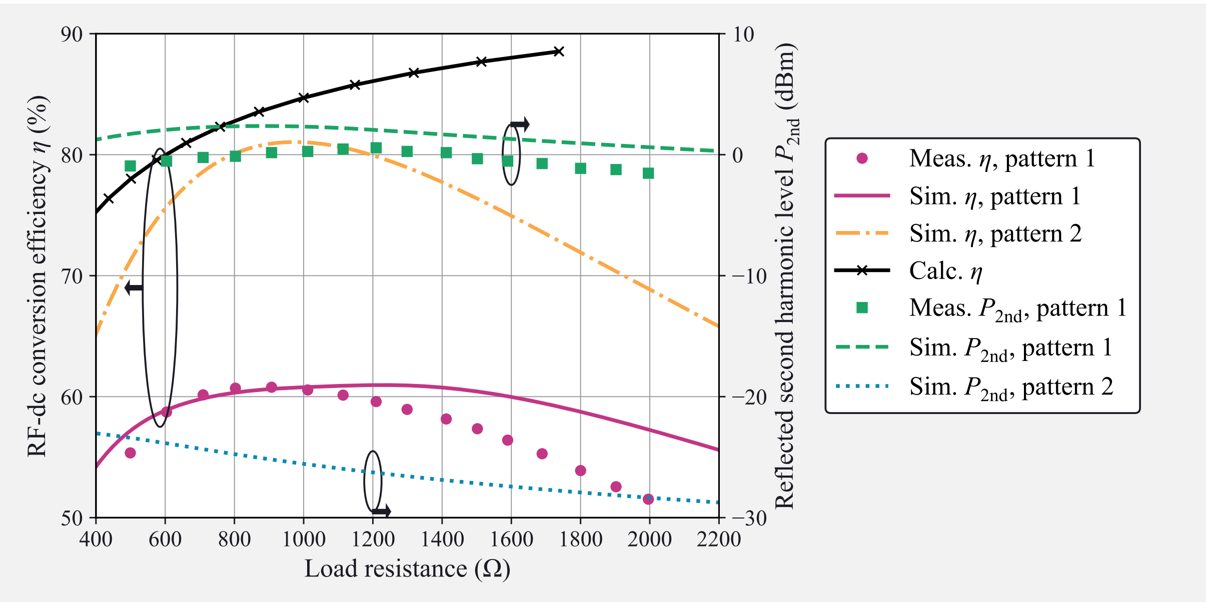
4.3.2 Measurement and simulation results

Fig. 4.13 shows the theoretical, simulation and measurement results of the RF–dc conversion efficiency and the second harmonic reradiation level of the designed rectenna (pattern 1). It also shows the simulation results of the rectenna optimized only for maximizing RF–dc conversion efficiency (pattern 2). The measurement results indicate that the maximum RF–dc conversion efficiency of pattern 1 was 60.8% at a load resistance of 907 Ω and an input power of 10.0 dBm. The maximum second harmonic level of pattern 1 was 0.57 dBm at a load resistance of 1209 Ω and an input power of 10.0 dBm. At the design parameters of an input power of 10.0 dBm and a load resistance of 1.0 kΩ, the RF–dc conversion efficiency was 60.6%, and the second harmonic level was 0.17 dBm in pattern 1.

Fig. 4.13 shows that the second harmonic level increases monotonically with increasing input power in both patterns. However, the variation in the second harmonic level due to load changes is less pronounced than in both patterns' RF–dc conversion efficiency. The results of load variation indicate that the RF–dc conversion efficiency in pattern 1 increases up to a load of 1.0 kΩ. Beyond 1.0 kΩ, the variation decreases with increasing resistance due to the effect of the diode's breakdown voltage. Fig. 4.13 shows that the second harmonic level of the rectenna in pattern 1 is up to 29.6 dB higher than that of the rectenna in pattern 2. Because of the reradiation of the second harmonic power, the RF–dc conversion efficiency of the rectenna in pattern 1 is up to 22.5 points less than that of the rectenna in pattern 2.



(a) Input power sweep



(b) Load resistance sweep

Figure 4.13: Measurement and simulation results of the performance of the rectenna. Pattern 1 shows the case in which the RF–dc conversion efficiency and the second harmonic level are optimization target functions. Pattern 2 shows the case in which only the RF–dc conversion efficiency is the optimization target function. Results obtained by sweeping (a) the input power with a load resistance of 1.0 kΩ and (b) the load resistance with an input power of 10.0 dBm.

Furthermore, as shown in Fig. 4.13, the measured efficiency of the proposed rectenna in pattern 1 is more than 20% lower than that of pattern 2 and the theoretical efficiency calculation. This decrease in efficiency is attributed to the reradiation of the second harmonic. In other words, the proposed rectenna in pattern 1 effectively connects a radiative load when the diode is viewed as a power source for the second harmonic. In the process of theoretical efficiency calculation, the diode's surrounding circuitry is assumed to result in zero power loss from each harmonic. Consequently, when the diode is considered as a power source for the second harmonic, the ideal load would be an open or short circuit. Therefore, connecting a load under these conditions leads to a decrease in efficiency, as suggested by the theoretical efficiency calculation process. Thus, the lower efficiency of pattern 1 compared to pattern 2, as observed in both simulation and measurement results in Fig. 4.13, can also be explained by the theoretical efficiency calculation process of the diode.

Table 4.1 compares the simulated power balance of the rectennas in patterns 1 and 2 at an input power of 10 dBm and a load resistance of 1.0 kΩ. The proposed rectenna (pattern 1) extracts the second harmonic, leading to an 18.5% increase in the second harmonic level compared to the conventional rectenna (pattern 2). The diode loss of the proposed rectenna is only 1% higher than that of the conventional rectenna. In other words, the proposed rectenna can divert part of the power that could be converted to dc power to second harmonic reradiation with little change in overall power utilization efficiency.

Table 4.2 summarizes the comparison of the performances of the harmonic reradiation rectenna with other antennas reported in previous studies for frequencies around the 900 MHz band. This table shows that the proposed rectenna has the highest harmonic reradiation level among all the compared rectennas. The proposed rectenna directly connects the antenna and rectifier circuit, simplifying the rectifier circuit configuration. Therefore, as shown in Table 4.2, the rectifier circuit mounting area is the most minor compared to previous studies due to the

Table 4.1: Comparison of the power balance of the rectennas in patterns 1 and 2

Pattern	Parameters	%
Pattern 1 (proposed design)	RF–dc	61.5
	P_{2nd}/P_{in}	18.6
	diode loss	19.9
Pattern 2 (conventional design)	RF–dc	81.0
	P_{2nd}/P_{in}	0.1
	diode loss	18.9

input filter's removal. Fig. 4.4 and Table 4.2 demonstrate the feasibility of designing a rectenna that surpasses the previous study [75] in both RF–dc conversion efficiency and second harmonic levels, contingent on the design targets.

4.4 Conclusions

This chapter proposed a rectenna design method using source-pull simulation with harmonics to achieve high RF–dc conversion efficiency and second harmonic reradiation levels. The results of the source-pull simulation show a trade-off relationship between the RF–dc conversion efficiency and the second harmonic reradiation levels. The designed rectenna has an RF–dc conversion efficiency of 60.6% and a second harmonic reradiation level of 0.17 dBm at a frequency of 920 MHz, an input power of 10.0 dBm, and a load resistance of 1.0 kΩ. Compared to previous 920 MHz band rectenna designs, the rectenna designed in this study had the highest second harmonic reradiation level while maintaining a high RF–dc conversion efficiency. The proposed method is a practical approach to designing a highly efficient rectenna that enhances harmonic reradiation levels.

Table 4.2: Performance comparison of the rectennas reradiating second harmonic around the 900 MHz band

Reference	[78]	[87]	[75]	This study
Frequency (GHz)	0.915	0.915	0.915	0.92
Order of the reradiated harmonic	second	second	second	second
RF–dc conversion efficiency(%) at 10 dBm	25*	30	65	60.6
Harmonic power level (dBm) measured at 10 dBm	-12*	-33	-6	0.17
Maximum RF–dc conversion efficiency(%)	58*	30	71	60.8
Maximum harmonic level (dBm) at input power (dBm)	-12 at 10*	-33 at 10	-1 at 17	0.57 at 10.0
Mounting area of the rectifier circuit	$0.035\lambda \times 0.104\lambda$	N.A.	$0.076\lambda \times 0.122\lambda$	$0.017\lambda \times 0.035\lambda$

* graphically estimated

Chapter 5

Concluding Remarks

5.1 Summary of this thesis

In wireless power transmission systems, high-efficiency rectennas are essential. The rectifying diode's theoretical rectification efficiency limits a rectenna's efficiency. The design methods to maximize the diode's rectification efficiency are left to the individual skills of each designer. This study summarizes high-efficiency design methods for single-diode rectennas. This thesis proposes new circuit configurations and design methods for two high-efficiency rectenna designs: one that matches a 50 Ω impedance and another designed for a non-50 Ω impedance and demonstrates their practical application. The proposed high-efficiency rectenna design methods were successfully applied to WPT systems, leading to the development of rectennas for harmonic retro-directive systems. This practical application underscores our research's relevance and potential impact in real-world scenarios. The summaries of each chapter are presented below.

In Chapter 1, we first have discussed the history of wireless power transmission and recent research developments. Next, we have reviewed previous studies on rectennas and identified the challenge of summarizing high-efficiency rectenna design methods that rely on something other than designers' skills. Finally, we have presented this study's research objectives and outlined the structure of this dissertation.

In Chapter 2, we proposed a novel single-shunt rectifier circuit that performs impedance matching using an output filter and summarized its design method. Using impedance matching theory based on transmission lines, we described the differences in impedance matching paths between conventional circuits and the proposed circuit. Additionally, we presented the fundamental wave input impedance conditions for diodes applicable to the proposed circuit. Through simulations, we compared the rectification efficiency and circuit losses of the conventional and proposed circuits, demonstrating that the proposed circuit exhibited lower losses and higher efficiency under various load conditions. The proposed circuit was designed for the 920 MHz band, and both simulations and experimental measurements showed that the proposed circuit could achieve full-wave rectification and impedance matching simultaneously. The designed 920 MHz single shunt rectifier circuit achieved a world-record rectification efficiency of 91% for the 920 MHz band.

In Chapter 3, we proposed a novel single-series rectenna that performs harmonic controlling using the antenna. Additionally, we introduced a new rectenna design method using source-pull simulations that include harmonics. Ideal circuit simulations demonstrated that the proposed rectenna configuration could achieve 100% full-wave rectification efficiency. By applying harmonic source-pull simulations to the rectifying circuit, we identified the source impedance for each harmonic, which corresponds to the input impedance requirements of the antenna, necessary for achieving high efficiency. Based on the harmonic source-pull simulation results, we designed an inverted-F antenna and developed a rectenna by directly connecting the antenna to the rectifying circuit. We compared the rectification efficiency of the proposed rectenna with that of a conventional rectenna, which does not perform harmonic controlling using the antenna, through simulations and experimental measurements. The results showed that the proposed rectenna achieved higher rectification efficiency. Compared to previous research examples of 920 MHz band rectennas, the developed rectenna achieved the highest rectification efficiency with a single diode.

In Chapter 4, we applied the rectenna design method using the harmonic source-pull simulation presented in Chapter 3 to develop a harmonic reradiation rectenna. The harmonic source-pull simulation clarified the trade-off relationship between rectification efficiency and second harmonic reradiation level on a Smith chart. Based on the harmonic source-pull simulation results, we designed an inverted-F antenna with a stub for the second harmonic. Simulations and experimental measurements demonstrated that the developed rectenna achieved a higher second harmonic reradiation level than conventional rectennas optimized solely for rectification efficiency. The developed rectenna showed the highest second harmonic reradiation level among previously reported 920 MHz band rectennas. Additionally, the proposed rectenna could use a portion of the rectified dc power for second harmonic reradiation without compromising the overall power conversion efficiency of the diode.

In conclusion, the single-diode rectenna design methods proposed in this dissertation enable achieving high efficiency in rectennas for wireless power transmission systems. The proposed single-shunt rectenna circuit configuration, which performs impedance matching with the output filter, can reduce matching losses and realize more efficient rectennas. The rectenna design method using harmonic source-pull simulations reveals the required antenna input impedance, allowing for the reverse design of antennas based on these impedances to achieve higher efficiency rectennas. Furthermore, the proposed rectenna design method using harmonic source-pull simulations can also be applied to harmonic reradiation rectennas. It is useful for realizing rectennas that reradiate harmonics without compromising the diode's power conversion efficiency.

5.2 Thesis contribution

The two design methods presented in Chapter 2 and Chapter 3 of this study apply to rectennas' design in microwave and millimeter-wave bands other than the 920 MHz band. The rectenna design method proposed in Chapter 3, which uses harmonic source-pull simulations, involves reverse engineering the antenna or low-pass filter to achieve the required source impedance. This design method can be applied to any frequency, rectifying diode, and rectifying circuit configuration. The reverse engineering approach allows for flexibility in designing the antenna and low-pass filter while the achievable maximum rectification efficiency is uniquely determined. Therefore, using the proposed method, it is expected that any designer, under any conditions, can achieve a rectification efficiency close to the maximum possible. This method will improve rectification efficiency in future rectenna research and development and ultimately enhance the overall efficiency of wireless power transmission systems. The design method for harmonic reradiation rectennas proposed in Chapter 4 clarifies the trade-off relationship between rectification efficiency and harmonic level. Using this method means that developers of rectennas for harmonic retro-directive systems can set achievable targets for rectification efficiency and harmonic levels. Thus, the development example presented in Chapter 4 is expected to advance the research and development of harmonic retro-directive systems. The proposed design method using harmonic source-pull simulations can also be applied to mixers and amplifiers, which use nonlinear elements similar to rectifying circuits. Therefore, this dissertation is expected to contribute to wireless power transmission and the future field of communications.

Appendix A

Theoretical calculation of the diode's efficiency

Chapter 1 discusses previous studies on theoretical efficiency calculations of diodes. In this appendix, we discuss the theoretical efficiency η_d of rectifier diodes and the transfer efficiency η_p due to junction capacitance, as illustrated in Chapter 1.

A.1 The derivation of diode's theoretical efficiency

Fig. A.1 illustrates a single-shunt rectifier circuit's equivalent circuit, focusing on the fundamental wave and dc power paths. In the figure, the blue lines indicate the transmission path of the fundamental wave power, while the red lines show the transmission path of the dc power. The equivalent circuit of the diode also includes the package reactance. However, the effects of package reactance can be mitigated by adjusting the matching circuits and output filters surrounding the diode. Additionally, the matching circuits and output filters are considered ideal circuits, and their losses are not considered in the theoretical calculations. This paper demonstrates the efficiency calculation process using the single-shunt rectifier circuit shown in Fig. A.1. However, the same results can be obtained by solving using the single-series rectifier circuit. Here, the following equation represents the nonlinear V-I characteristics of the diode.

$$I_d = I_s \left(\exp \frac{V_d}{V_{bi}} - 1 \right), \tag{A.1}$$

Here, I_d, V_d, I_s, and V_bi represent the diode current, voltage, reverse saturation current, and built-in voltage, respectively. The built-in voltage V_bi is expressed as $\frac{nkT}{q}$, where q is the elementary charge, k is the Boltzmann constant, T is the temperature, and n is the diode's emission coefficient. The following equations express the dc and fundamental wave voltage applied to the nonlinear characteristic part of the diode, as shown in the figure.

$$V_d = -V_{dc} - V_{di} \cos \omega t. \tag{A.2}$$

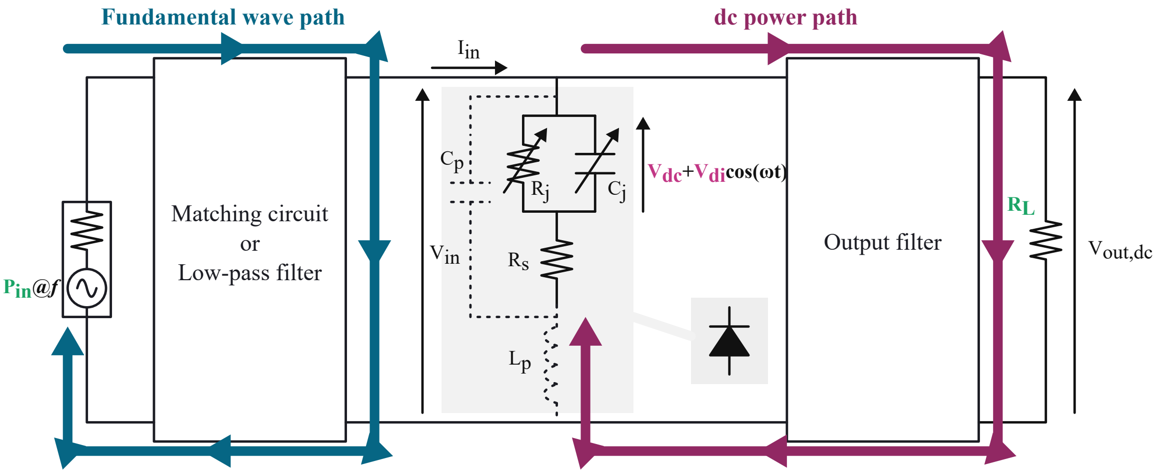


Figure A.1: Equivalent circuit of a single-shunt rectifier circuit.

Equation (A.2) can be expanded as follows by substituting equation (A.1) into equation (A.1) and using the first-kind modified Bessel function [94].

$$I_d = I_s\left[\exp\left(-\frac{V_{dc}}{V_{bi}}\right) \times \left(B_0\left(-\frac{V_{di}}{V_{bi}}\right) + 2\sum_{i=1}^{\infty} B_i\left(-\frac{V_{di}}{V_{bi}}\right)\cos(i\omega t)\right) - 1\right], \tag{A.3}$$

Here, B_i represents the first kind of modified Bessel function. Equation Eq. (A.3) provides the following equation for expressing the fundamental wave current resulting from the diode's V-I characteristics.

$$I_{d,f} = 2I_s \exp\left(-\frac{V_{dc}}{V_{bi}}\right) B_1\left(-\frac{V_{di}}{V_{bi}}\right)\cos(\omega t). \tag{A.4}$$

On the other hand, the C-V characteristics of the diode are expressed by the following equation.

$$C_j = C_{j0}\left(1 - \frac{V_d}{V_j}\right)^{-m}, \tag{A.5}$$

Here, $C_{\mathrm{j}0}$, V_j, and M represent the zero-biased junction capacitance, junction potential, and junction coefficient of the diode, respectively. The following equation expresses the charge Q_j stored in the junction capacitance.

$$Q_j = \int C_j dV = C_{j0}V_j \frac{\left(1 - \frac{V}{V_j}\right)^{1-M}}{M-1} \tag{A.6}$$

The current I_cj generated by the junction capacitance C_j is expressed by the following equation.

$$I_{Cj} = \frac{dQ}{dt} = C_{j0}V_{di}\omega\left(1 + \frac{V_{dc}}{V_j} + \frac{V_{di}}{V_j}\cos\omega t\right)^{-M} \sin\omega t \tag{A.7}$$

Here, t represents time. In Equation (A.7), let u be defined as $\frac{V_{di}}{V_j}\cos(\omega t)$.

$$u \triangleq \frac{V_{di}}{V_j}\cos\omega t \tag{A.8}$$

We obtain the following equation by performing a Taylor expansion of equation (A.7) up to the third order in terms of u.

$$\begin{aligned}\left(1+\frac{V_{dc}}{V_j}+\frac{V_{di}}{V_j}\cos\omega t\right)^{-M} &= \left(1+\frac{V_{dc}}{V_j}+u\right)^{-M} \\ &\approx \left(1+\frac{V_{dc}}{V_j}\right)^{-M} - M\left(1+\frac{V_{dc}}{V_j}\right)^{-M-1} u \\ &+ \frac{M(M+1)}{2}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-2} u^2 \\ &- \frac{M(M+1)(M+2)}{6}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-3} u^3\end{aligned} \tag{A.9}$$

We obtain the following equations by organizing equation (A.9) according to the fundamental wave, second harmonic, and third harmonic.

$$\begin{aligned}I_{cj} =& C_{j0}V_{di}\omega\left[\left(1+\frac{V_{dc}}{V_j}\right)^{-M}\sin\omega t\right. \\ &-\frac{1}{2}M\left(1+\frac{V_{dc}}{V_j}\right)^{-M-1}\left(\frac{V_{di}}{V_j}\right)\sin 2\omega t \\ &+\frac{M(M+1)}{8}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-2}\left(\frac{V_{di}}{V_j}\right)^2\sin\omega t \\ &+\frac{M(M+1)}{8}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-2}\left(\frac{V_{di}}{V_j}\right)^2\sin 3\omega t \\ &-\frac{M(M+1)(M+2)}{12}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-3}\left(\frac{V_{di}}{V_j}\right)^3\sin 2\omega t \\ &\left.-\frac{M(M+1)(M+2)}{48}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-3}\left(\frac{V_{di}}{V_j}\right)^3\sin 4\omega t\right]\end{aligned} \tag{A.10}$$

Equation (A.10) can express the fundamental wave current resulting from the diode's C-V characteristics.

$$I_{cj,f} = \omega C_{j0}V_{di}\left[\left(1+\frac{V_{dc}}{V_j}\right)^{-M}+\frac{M(M+1)}{8}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-2}\left(\frac{V_{di}}{V_j}\right)^2\right]. \tag{A.11}$$

From equations (A.4) and (A.11), the total fundamental wave current $I_{\mathrm{t,f}}$ resulting from the nonlinear characteristics of the diode is expressed by the following equation.

$$I_{t,f} = I_{d,f} + \mathrm{j}I_{cj,f}. \tag{A.12}$$

Here, note that the current $I_{\mathrm{cj,f}}$ due to the C-V characteristics leads the current $I_{\mathrm{d,f}}$ due to the I-V characteristics by 90° in phase. The input current I_{in} to the diode is in the opposite direction of the total current given by equation (A.12). Therefore, the following equation expresses the input current I_{in} to the diode.

$$I_{in} = -I_{d,t} = -\left(I_{d,f} + \mathrm{j}I_{cj,f}\right). \tag{A.13}$$

On the other hand, the input voltage V_{in} applied to the diode is expressed by the following equation.

$$V_{in} = V_{di} + R_s I_{in}. \tag{A.14}$$

From equations (A.13) and (A.14), the input fundamental wave power of the diode is expressed by the following equation.

$$\begin{aligned} P_{in} &= \frac{1}{2}\Re(V_{in}I_{in}^{*}) \\ &= -V_{di}I_s \exp\left(-\frac{V_{dc}}{V_{bi}}\right)B_1\left(\frac{V_{di}}{V_{bi}}\right) + \frac{1}{2}R_s\left[\left(2I_s\exp\left(-\frac{V_{dc}}{V_{bi}}\right)B_1\left(\frac{V_{di}}{V_{bi}}\right)\right)^2\right. \\ &\left.+\left(\omega C_{j0}V_{di}\left[\left(1+\frac{V_{dc}}{V_j}\right)^{-M} + \frac{M(M+1)}{8}\left(1+\frac{V_{dc}}{V_j}\right)^{-M-2}\left(\frac{V_{di}}{V_j}\right)^2\right]\right)^2\right]. \end{aligned} \tag{A.15}$$

Next, we focus on the dc power path shown in the figure. From equation (A.3), the dc current $I_{\mathrm{d,dc}}$ resulting from the diode is expressed by the following equation.

$$I_{d,dc} = I_s\left(B_0\left(-\frac{V_{di}}{V_{bi}}\right)\exp\left(-\frac{V_{dc}}{V_{bi}}\right) - 1\right) \tag{A.16}$$

The following equation expresses the voltage relationship in the closed circuit from the diode to the load resistor.

$$(R_L + R_s)I_sB_0\left(-\frac{V_{di}}{V_{bi}}\right)\exp\left(-\frac{V_{dc}}{V_{bi}}\right) - V_{dc} - (R_L + R_s)I_s = 0. \tag{A.17}$$

Here, R_{L} is the load resistor of the rectifier circuit. In equations (A.15) and (A.17), the two unknown variables are V_{dc} and V_{di}. In other words, by determining the input power, load resistance, operating frequency, and rectifier diode (SPICE parameters), we can solve the simultaneous equations of equations (A.15) and (A.17). By solving the simultaneous equations, the unknown variables V_{dc} and V_{di} can be obtained. The obtained V_{dc} can be used to calculate the output power $P_{\mathrm{out,dc}}$ using the following equation.

$$P_{out,dc} = \frac{R_L V_{dc}^2}{(R_s + R_L)^2} \tag{A.18}$$

Here, the following equation expresses the efficiency η_{d} of the rectifier diode.

$$\eta_d = \frac{R_L V_{dc}^2}{P_{in}\left(R_s + R_L\right)^2} \times 100\%. \tag{A.19}$$

Next, we consider the transfer function due to the junction capacitance of the rectifier diode. The equivalent circuit of the diode can be treated as a low-pass filter consisting of R_{s}, R_{j}, and C_{j}. When the diode is modeled as a low-pass filter, the following equation expresses the transfer function relating the input power at the diode terminals to the input power into the V-I characteristics [95].

$$\eta_p = \frac{1}{\left(1 + \left(\omega C_{j,dc}\right)^2 R_s R_{j,dc}\right)^2} \tag{A.20}$$

Since rectification by the diode is performed through the V-I characteristics, the voltage V_{d} applied to R_{j} is essential. In other words, Equation (A.20) implies that the input power is not effectively transferred to the nonlinear V-I characteristic part at higher frequencies, resulting in a decrease in rectification efficiency. From equations (A.19) and (A.20), the overall efficiency η_{diode} of the rectifier diode is expressed by the following equation.

$$\eta_{diode} = \eta_d \eta_p = \frac{R_L V_{dc}^2}{P_{in}\left(R_s + R_L\right)^2} \frac{1}{\left(1 + \left(\omega C_{j,dc}\right)^2 R_s R_{j,dc}\right)^2} \times 100\% \tag{A.21}$$

A.2 Method of calculation by program

This section explains the program-based method for solving the simultaneous equations of equations (A.15) and (A.17) using a program. Solving equation (A.17) for V_{dc} yields the following equation.

$$V_{dc} = -I_s\left(R_L + R_s\right) + V_{bi} W_0\left(\frac{I_s}{V_{bi}}\left(R_L + R_s\right)\exp\left(I_s \frac{R_L + R_s}{V_{bi}}\right) B_0\left(\frac{V_{di}}{V_{bi}}\right)\right) \tag{A.22}$$

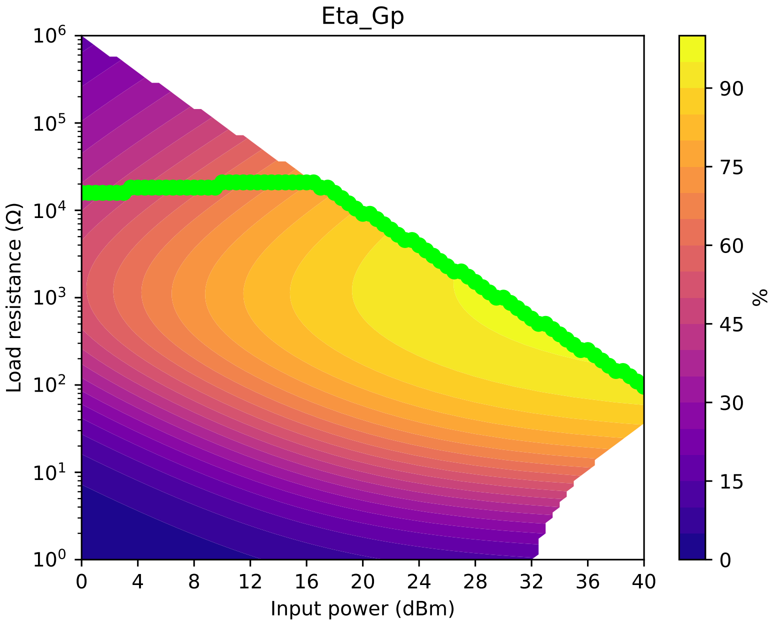
Here, W denotes the Lambert W function. W_0 denotes the principal branch of the Lambert W function, taking the positive value of the two possible solutions. The derivation from equation (A.15) to equation (A.22) was performed using the SymPy library in Python. Substitute equation (A.22) into equation (A.17) and solve for V_{di}. Here, the equation for V_{di} obtained by substituting Equation (A.17) into Equation (A.22) is difficult to solve algebraically. Therefore, in this study, the solution for V_{di} was obtained using the bisection method. The bisection method was implemented using the ”brentq” function from the SciPy library in Python. Since V_{di} is always a positive number, the initial lower bound for the bisection method was set to 0, and the following equation gave the initial upper bound.

$$V_{di,upper} = \sqrt{\frac{P_{in}}{R_L}}\left(R_L + R_s\right) \tag{A.23}$$

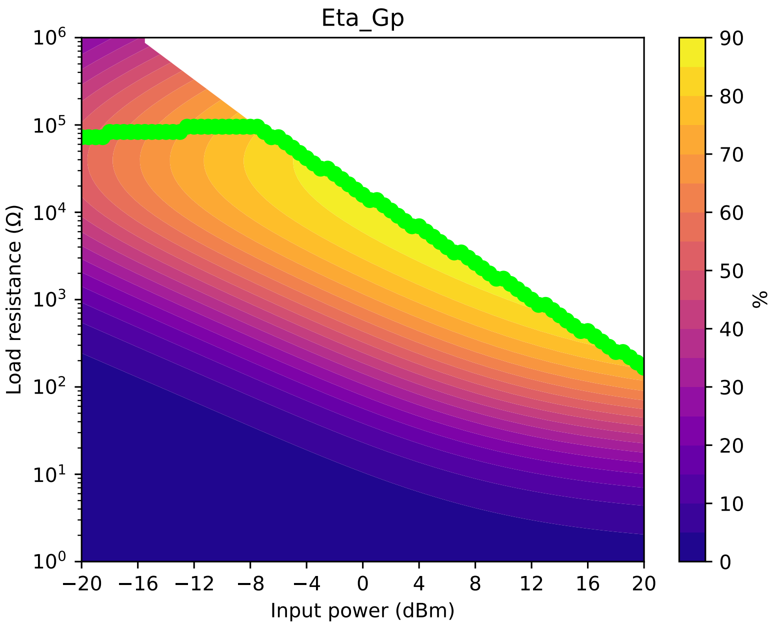
Equation (A.23) shows the relationship that the power generated by V_{di} must always be less than or equal to the input power. By setting the input power P_{in}, load resistance R_{L}, frequency f, and diode as described above, and solving the simultaneous equations of equations (A.15) and (A.17), V_{dc} and V_{di} can be obtained to calculate the rectification efficiency of the diode.

A.3 Results of theoretical efficiency calculations

The theoretical rectification efficiency at a frequency of 920 MHz was calculated for the GaAs Schottky barrier diode used in Chapter 2 and the SMS7621 diode used in Chapters 3 and 4. The figures show V_{dc}, V_{di}, and rectification efficiency η_{diode} for the GaAs Schottky barrier diode and the SMS7621 diode. The contour plots in the figures illustrate the diodes' theoretical rectification efficiency, and the green plots indicate the optimal load conditions at each input power level. The white-shaded areas in the figures represent regions where the instantaneous voltage V_{d} of the diode exceeds the breakdown voltage B_{v} or where the instantaneous current $I_{\mathrm{t,f}}$ exceeds the maximum forward current of the diode. The figures show that the diode's theoretical rectification efficiency increases with higher input power, and the optimal load conditions vary for each power level. Note that the results shown in the figures do not include matching losses from the matching circuit or circuit losses from harmonic controlling. The fundamental wave input impedance of the diode varies according to the optimal load conditions at each power level. Chapters 2, 3, and 4 of this paper use these theoretical rectification efficiency calculation results to compare with simulation and measurement results.



(a) Results of GaAs Schottky barrier diode



(b) Results of SMS7621

Figure A.2: Calculation results of the diode's theoretical efficiency. Theoretical efficiency of (a) GaAs Schottky barrier diode and (b) SMS7621. The points indicate the optimal load for each input power.

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Publication list

Journal papers

1. K. Kawai, N. Shinohara, and T. Mitani, ”Novel Structure of Single-Shunt Rectifier Circuit with Impedance Matching at Output Filter.” IEICE Transactions on Electronics, no. 2, vol. 106, pp. 50-58, 2023. (Chapter 2)

2. K. Kawai, N. Shinohara, and T. Mitani, ”Efficiency Enhancement of a Single-Diode Rectenna Using Harmonic Control of the Antenna Impedance,” IEICE Transactions on Electronics, Microwave and Millimeter-Wave Technologies, accepted (Early Access). (Chapter 3)

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6. N. Takabayashi, T. Toyonaga, K. Suzuki, K. Kawai, Y. Tanaka and N. Shinohara, ”Initial Developments of Image-Recognition-Aided Microwave Power Transmission System for Smartphone Charging,” 2022 Wireless Power Week (WPW), Bordeaux, France, 2022, pp. 553-557.

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9. N. Shinohara, B. Yang and K. Kawai, ”Far-Field Beam Wireless Power Transfer with Combination of Beam Forming and Optical Target Detection,” 2024 18th European Conference on Antennas and Propagation (EuCAP), Glasgow, United Kingdom, 2024, pp. 1-4.

Other presentations in international conference

1. K. Kawai, N. Shinohara and T. Mitani, ”Design of Rectenna for Microwave Wireless Power Transfer System Using Third Harmonic Reradiation,” 3rd Thailand-Japan Microwave Student Workshop, Nov., 2022.

Awards

1. IEEE MTT-S Kansai Chapter 13th Kansai Microwave Meeting for Young Engineers, Distinguished Service Award, 2020.10.31.

2. IEEE MTT-S Kansai Chapter, Best Poster Award, 2022.12.26.

3. Kyoto Revengers (N. Takabayashi, K. Kawai, T. Toyonaga, and K. Suzuki), Top 10 1st Stage Proposal Award, for “Smartphone MPT”, Inaugural IEEE Global Student Wireless Power Competition 2022.

4. Best Video Presentation Award in IEEE Global Student Design Competition 2023, for ”Microwave Power Transmission System for Smartphone”, IEEE Wireless Power Technology Conference and Expo 2023 (WPTCE2023), 2023.6.4-8.

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