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論文題目	A study on heavy ion-induced single event effects for radiation-tolerant FPGA development （耐放射線性 FPGA に向けた重粒子誘起シングルイベント効果の研究）		

（論文内容の要旨）

Thanks to the continued miniaturization of transistors and improvements in manufacturing processes, the processing power once required for supercomputers is now available in our smartphones. With semiconductors literally everywhere, their reliability as a social infrastructure is becoming more important than ever before in history. Regardless of where semiconductors are used on Earth or in space, they are exposed to radiation that deposits charges on them, called single event effects (SEEs) or soft errors. As transistors shrink and operate at lower voltages, the sensitivity of memory cells, such as static random access memories (SRAMs) and flip-flops (FFs), to radiation generally increases. Additionally the transition from planar to three-dimensional (3D) transistor structures makes them more complex and challenging. Therefore, research on SEEs and their characterization is essential to understand them and make them more reliable.

This dissertation focuses on SEEs and soft errors on field-programmable gate arrays (FPGAs), which are mainly composed of programmable logics (PLs) and SRAMs. FPGAs are a type of integrated circuits (ICs), and thanks to their reconfigurable feature, high parallel processing capabilities, and short turnaround time, they are widely used in the terrestrial applications including artificial intelligence (AI) accelerators, even in the satellite system.

Configuration RAMs (CRAMs) store the interconnection of PLs and their logic to provide a given functionality. Single event upsets (SEUs) in the CRAMs cause the functional interrupt or malfunction of the FPGAs. Embedded SRAMs are called as block RAMs (BRAMs), and are arranged in a highly dense grid, and store the data in the FPGAs. SRAMs are always subject to single bit upsets (SBUs) and multiple cell upsets (MCUs), which are key fingerprints describing their complex charge collection mechanisms with neighboring cells. By examining CRAMs and BRAMs in FPGAs and their phenomena under radiation, the reliability of FPGAs is discussed in this dissertation.

The studies in this dissertation address the SEUs in CRAMs and single event transients (SETs) in PLs, as well as charge collection mechanisms of SBUs and MCUs in SRAMs which will be used for BRAMs. First, an SEU tolerance of the atom switch (AS) FPGA, which is one of the non-volatile technologies, is investigated revealing its immunity of state change under heavy ion irradiation. This is followed by an investigation of SETs in the peripheral circuits using pulsed laser irradiation.

Then, SBUs and MCUs in SRAMs are explored with heavy ion irradiation under different data patterns and applied voltages to reveal the unique charge collection mechanisms on 3D transistors by analyzing the fail bit maps according to the independent events and conducting simulations. A unique voltage dependence of SRAMs is then discussed, which is contrary to the predictions of the model proposed in the literature. Based on the above results and findings, the SEU cross-section (XS) model of bulk SRAM is proposed and verified.

This dissertation provides interesting and insightful findings through studies based on various heavy ion and pulsed laser irradiation experiments and simulations: ASs, which are used for CRAMs for AS-based FPGA, can withstand against heavy ion up to 68.9 MeV·cm^2/mg, which is enough high SEE tolerance for space application. SBUs and MCUs and its voltage dependence have been examined in detail, revealing the characteristic charge collection mechanisms in FinFET SRAMs. The XS-LET-V_{DD} curve model for bulk planar and FinFET SRAMs has been proposed for predicting XSs of BRAMs in FPGAs.

This dissertation contributes to the understanding and ensuring the reliability of FPGAs, as well as demonstrating the prospective applications of the proposed model for predicting proton and neutron XSs, which are crucially important for both terrestrial and space applications.