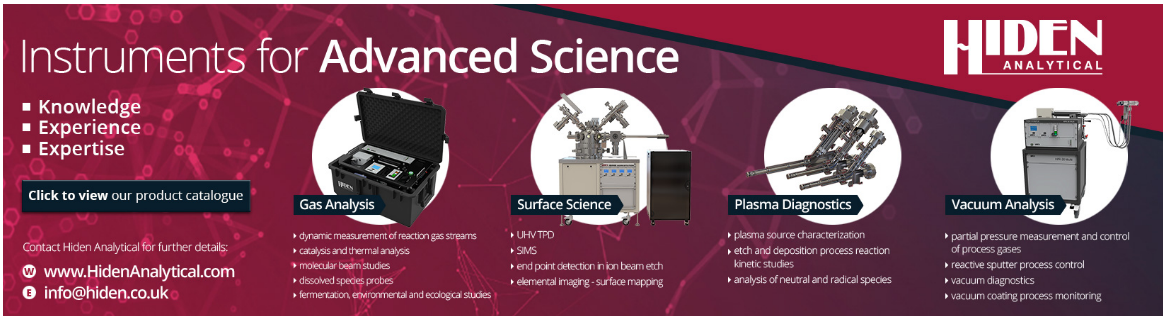
Journal of Applied Physics

RESEARCH ARTICLE | APRIL 02 2025

Analysis of trap-assisted tunneling current at non-alloyed contacts formed on heavily ion-implanted n-type SiC

Masahiro Hara ; Hajime Tanaka ; Mitsuaki Kaneko ; Tsunenobu Kimoto

J. Appl. Phys. 137, 135704 (2025)
https://doi.org/10.1063/5.0258366



Journal of Applied Physics | ARTICLE | pubs.aip.org/aip/jap

Analysis of trap-assisted tunneling current at non-alloyed contacts formed on heavily ion-implanted n-type SiC

Cite as: J. Appl. Phys. **137**, 135704 (2025); doi: 10.1063/5.0258366
Submitted: 16 January 2025 · Accepted: 18 March 2025 ·
Published Online: 2 April 2025

View Online Export Citation CrossMark

Masahiro Hara,[1,a)] Hajime Tanaka,[1,2] Mitsuaki Kaneko,[1] and Tsunenobu Kimoto[1]

AFFILIATIONS

[1]Department of Electronic Science and Engineering, Kyoto University, Nishikyo, Kyoto 615-8510, Japan
[2]Division of Electrical, Electronic and Infocommunications Engineering, Osaka University, Suita, Osaka 565-0871, Japan

[a)]**Author to whom correspondence should be addressed:** hara@semicon.kuee.kyoto-u.ac.jp

ABSTRACT

Numerical calculation of trap-assisted tunneling (TAT) current was performed and trap levels that dominantly contribute to the TAT current at non-alloyed contacts formed on phosphorus ion-implanted n-type SiC were speculated. Based on a careful discussion focusing on the impact of the energy level of traps on the tunneling probability and tunneling current, it was found that the energy level contributing to the TAT current was sensitively varied depending on the applied voltage. It turned out that a trap located at the half energy of the Schottky barrier height from the conduction band edge mainly contributed to the enhanced TAT current under a reverse bias, while shallower traps were responsible for the forward TAT current.

I. INTRODUCTION

Thanks to the high critical electric field (~2.5 MV/cm), silicon carbide (SiC) has become an attractive alternative to silicon (Si) in high-voltage power device applications.[1–4] SiC Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) have already been put into real power conversion systems, achieving a significant loss reduction.[5–7] SiC is also regarded as a promising semiconductor material for high-temperature electronics because of its wide bandgap (3.26 eV),[8,9] and operation of transistors and logic circuits at an elevated temperature (>300 °C) has been demonstrated.[10–13]

Ion implantation is a key technology for fabricating these electronic devices. The ion implantation process for SiC has been developed, and wide-range control of the doping density has been achieved for n- and p-type SiC by nitrogen (N), phosphorus (P), and aluminum (Al) ion implantation.[14–17] Besides, electrical properties in ion-implanted regions, including carrier density, mobility, and resistivity, have been intensively studied.[18–21] On the other hand, fundamental properties at electrodes formed on ion-implanted SiC, such as barrier height and carrier transport mechanism, have less been focused on so far.[22,23] Understanding the contact properties of metal/heavily ion-implanted SiC structures is particularly important for ohmic contacts, which are often formed on ion-implanted region with a very high doping density ($>10^{19}$ cm^{-3}).

We have worked on characterization of the barrier height and carrier transport at non-sintered metal/heavily doped SiC interfaces (i.e., heavily doped SiC Schottky interfaces) as an important first step toward improving the ohmic contact formation process, while thermal treatment is usually required for obtaining low-resistance and stable ohmic contacts on SiC.[24–26] In the case of Schottky contacts on heavily doped SiC epitaxial layers, current–voltage (I–V) characteristics are well described by direct tunneling (DT), including both the thermionic field emission (TFE) and field emission (FE).[27–29] When contacts are formed on ion-implanted SiC, on the other hand, the current density at the interface is found to be larger by several orders of magnitude than that at contacts on epitaxially grown SiC with almost identical doping density.[23,30] Capacitance–voltage measurements on vertical SBD structures fabricated with P^+-implanted SiC revealed that the barrier height at the metal/ion-implanted SiC interface was almost the same as that at an interface on epitaxial SiC, and both values were close to the ideal barrier height expected from the difference in the work function of the electrode and SiC.[23] Since it is known that high-energy ion bombardment generates various kinds of defect levels in the bandgap,[31–34] the enhanced current is plausibly explained by the contribution of trap-assisted tunneling (TAT) through implantation-induced deep levels.[23,35]

The enhanced current by TAT at metal/ion-implanted SiC contacts is advantageous for ohmic contact formation. Indeed, without high-temperature sintering ($\sim$1000 °C), which is the standard process for ohmic contact formation on SiC,[24–26] we demonstrated a very low contact resistivity (ρ_c) of $10^{-6}\,\Omega\,\mathrm{cm}^2$ for magnesium (Mg) and titanium (Ti) electrodes formed on heavily P^+-implanted n-type SiC ($3-7\times10^{19}\,\mathrm{cm}^{-3}$).[35] Although how TAT contributes to the carrier transport at metal/ion-implanted SiC interfaces was discussed based on the doping density dependence of ρ_c,[35] a quantitative analysis of the TAT current at metal/SiC contacts has not been achieved. Toward gaining a deeper understanding of the TAT phenomenon and precisely modeling a ρ_c at SiC ohmic contacts, the interface carrier transport should be further investigated by combining the calculation and experiment. In the present study, numerical calculation of TAT current is performed assuming various energy levels of traps, and it is speculated which trap dominantly contributes to the enhanced tunneling current at contacts formed on heavily P^+-implanted SiC.

II. CALCULATION

Figure 1 depicts a schematic band diagram of TAT through a Schottky barrier under a reverse bias. When carriers pass through a defect level (position: x_T), the tunneling path is divided into two shorter ones, leading to an enhanced tunneling probability. The calculation of tunneling probability is based on the Wentzel–Kramers–Brillouin (WKB) approximation,[36]

$$P(E) = \exp\left[-\frac{2\sqrt{2m^*}}{\hbar}\int_{x_\mathrm{in}}^{x_\mathrm{out}}\sqrt{U(x)-E}\,\mathrm{d}x\right], \tag{1}$$

where $\hbar$ is the Dirac constant, m^* is the tunneling effective mass, $U(x)$ is the energy potential in the space charge region, E is the energy of a carrier along the tunneling direction, and x_in and x_out are the positions of an incident and a transmitted carrier, respectively. The typical values of x_in and x_out are in sub-nanometer and several-nanometer orders, respectively, while these values strongly depend on the energy of an electron and applied voltage. As for TAT, previous studies[37–39] derived an expression for the tunneling probability $[P_\mathrm{TAT}(E)]$ by considering the equilibrium condition of the carrier capture/emission via tunneling as follows:

$$P_\mathrm{TAT}(E) = N_\mathrm{T}\sigma_\mathrm{T}\frac{P_1(E)P_2(E)}{P_1(E)+P_2(E)}, \tag{2}$$

where N_T is the trap density (area density) and σ_T is the capture cross section of the trap for tunneling carriers. $P_1(E)$ and $P_2(E)$ are the probabilities of tunneling from the metal to the trap level ($x_0 \to x_\mathrm{T}$) and from the trap level to the semiconductor ($x_\mathrm{T} \to x_1$), respectively, as illustrated in Fig. 1. Note that the factor $N_\mathrm{T}\sigma_\mathrm{T}$ can be interpreted as an indicator of how easily the tunneling carrier encounters a trap. Using $P_\mathrm{TAT}(E)$, the TAT current is calculated as

$$J_\mathrm{TAT} = \frac{A^*T}{k_\mathrm{B}}\int P_\mathrm{TAT}(E)\ln\left[\frac{\exp\{-(E-E_\mathrm{Fm})/k_\mathrm{B}T\}+1}{\exp\{-(E-E_\mathrm{Fs})/k_\mathrm{B}T\}+1}\right]\mathrm{d}E, \tag{3}$$

where A^* is the effective Richardson constant ($151\,\mathrm{A/cm^2\,K^2}$ for n-type SiC[35]), T is the absolute temperature, k_B is the Boltzmann constant, and E_Fm and E_Fs are the Fermi levels in the metal and the semiconductor, respectively. The above formulas are for tunneling from the metal to the semiconductor, while the tunneling current in the opposite direction can be calculated by flipping E_Fm and E_Fs in Eq. (3). Regarding tunneling probability for forward bias conditions, $P_1(E)$ and $P_2(E)$ are defined for tunneling from the semiconductor to the trap ($x_1 \to x_\mathrm{T}$) and from the trap level to the metal ($x_\mathrm{T} \to x_0$), respectively.

In this study, the TAT current was calculated by varying the energy level of the trap (E_T), which is directly linked with x_T. In Eq. (1), the electron effective mass along the c-axis at the conduction band edge ($0.33m_0$[40]) was chosen as m^* to compare the calculated I–V curves with experimental results for metal/P^+-implanted SiC(0001) Schottky contacts. $U(x)$ was defined by considering image force potential,[41] expressed as

$$U(x) = \frac{e^2N_\mathrm{D}}{2\varepsilon_\mathrm{s}}x^2 - \frac{e^2N_\mathrm{D}w}{\varepsilon_\mathrm{s}}x - \frac{e^2}{16\pi\varepsilon_\mathrm{s}x}, \tag{4}$$

where e is the elementary charge, N_D is the net donor density, ε_s is the dielectric constant of SiC ($10.32\varepsilon_0$ along the c-axis[17]), and w is the depletion layer width. The value of N_D was assumed to be $5\times10^{18}\,\mathrm{cm}^{-3}$, and the zero-field barrier height (ϕ_B0), without

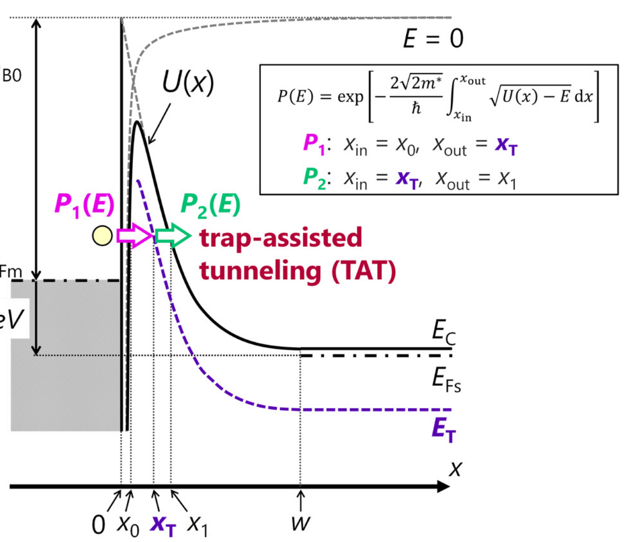


FIG. 1. Energy band diagram of an n-type SiC Schottky structure for numerical calculation of TAT current.

including the image force effect,[42] was set to be 1.0 eV, which corresponds to the typical barrier height at the Ti/n-type SiC interface.[35,42,43] Since N_T and σ_T are unknown parameters, some assumptions are required in the calculation. Regarding N_T (unit: cm^{-2}), the volume density of the trap was assumed to be a hundredth of N_D (i.e., $5 \times 10^{16}\,cm^{-3}$),[34] and it was also assumed that these traps are uniformly distributed in the ion-implanted region. Considering the process condition in our experiment,[23] the implantation depth of 600 nm was used, and N_T was calculated as $3 \times 10^{12}\,cm^{-2}$. Since the capture cross section of defects, σ_T, for the interaction with tunneling carriers might differ from that with carriers inside the conduction band, this parameter is unknown in the analysis of TAT current. Thus, in this study, σ_T of $1 \times 10^{-13}\,cm^2$ was assumed, resulting in the $N_T\sigma_T$ value of 0.3. Note that varying the value of σ_T directly leads to a change in the TAT current, that is, the calculated TAT current becomes ten or hundred times smaller when using $\sigma_T = 1 \times 10^{-14}$ or $1 \times 10^{-15}\,cm^2$, respectively. Based on the above calculation conditions, TAT current was numerically calculated with various E_T values from $E_C - E_T = 0.1$ to 0.9 eV, where E_C is the conduction band minimum.

III. RESULTS

Figure 2 shows the (a) band diagram near the metal/SiC interface, (b) tunneling probability, and (c) tunneling current, which were calculated under the forward bias of $V = +0.1$ V. In Fig. 2, the case of TAT through a trap with $E_C - E_T = 0.3$ eV is displayed as an example, and the calculated data for DT[28,35] are also plotted for comparison. As shown in Fig. 2(b), $P_{TAT}(E)$ is several orders of magnitude higher than the DT probability $[P_{DT}(E)]$ at a given energy. Note that the maximum value of the tunneling probability for TAT does not reach unity because the shortest tunneling distance, which depends on the energy level of a trap, never becomes 0 (i.e., $x_{in} \neq x_{out}$). Since a larger number of electrons exist at a lower energy, the increased tunneling probability for TAT in a low energy range directly leads to the enhanced tunneling current and a lower value of E_{peak}, which is defined as an energy where electron tunneling most frequently occurs,[28,35] as shown in Fig. 2(c). Two components of the TAT probability, $P_1(E)$ and $P_2(E)$, are also plotted in Fig. 2(b). It is found that the total TAT probability is close to the smaller one of $P_1(E)$ or $P_2(E)$, that is, tunneling through a longer path basically determines the total TAT current. Thus, it is expected that the TAT current is most enhanced when the tunneling path is divided into almost halves, that is, the relationship of $P_1(E) \simeq P_2(E)$ is satisfied. Since the energy level of a trap directly determines the position where the tunneling path is divided, the trap level that carriers pass through during tunneling has a strong impact on the TAT current.

Figure 3 shows the (a) forward and (b) reverse I–V characteristics at n-type SiC Schottky contacts with $\phi_{B0} = 1.0$ eV calculated based on the TAT model assuming various E_T. The gray dashed lines represent the calculated DT current. It is found that the calculated I–V characteristics for TAT are very different depending on which trap level is passed through. Under a forward bias, the TAT current is larger than the DT current in a wide voltage range when passing through relatively shallow levels ($E_C - E_T = 0.2-0.3$ eV). TAT through a trap with $E_C - E_T = 0.4$ eV offers the largest current in a low voltage range ($V \lesssim +0.1$ V), and a deeper trap with $E_C - E_T > 0.4$ eV leads to a smaller TAT current and a narrower voltage range where the tunneling current is enhanced. It was confirmed that the calculated TAT current with the energy

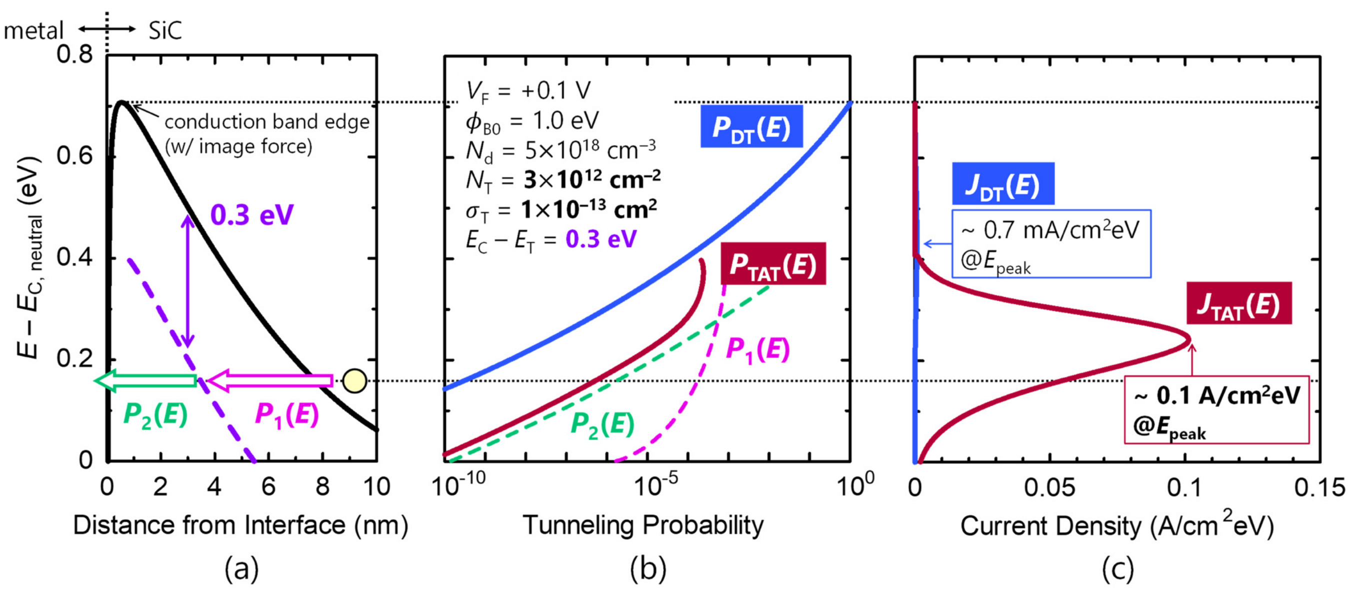


FIG. 2. (a) Band diagram, (b) tunneling probability, and (c) tunneling current as a function of electron energy calculated based on the DT and TAT models. $E_{C,\,neutral}$ indicates the conduction band edge in the neutral region in SiC (i.e., outside the depletion region).

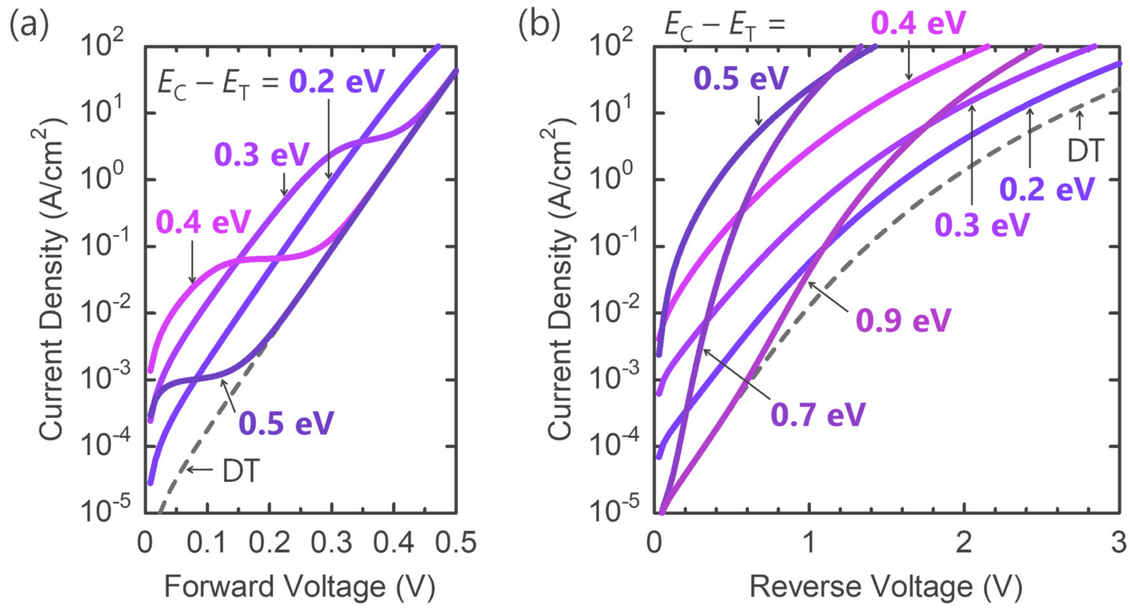


FIG. 3. TAT current in an n-type SiC Schottky structure calculated under (a) forward and (b) reverse bias conditions assuming various trap levels.

level of $E_C - E_T \geq 0.6\,\text{eV}$ was almost identical with the DT current. In the reverse characteristics, the TAT current becomes larger in an entire voltage range with the contribution of deeper traps for $E_C - E_T \leq 0.5\,\text{eV}$, while the TAT current in a lower voltage range ($-1\,\text{V} < V < 0\,\text{V}$) turns to decrease for a deeper energy level ($E_C - E_T > 0.5\,\text{eV}$). Note that the calculated TAT current is comparable with the DT current when assuming traps with $E_C - E_T \geq 1.0\,\text{eV}$. It is noteworthy that the TAT current through $E_C - E_T = 0.4$ or $0.5\,\text{eV}$ under a very small forward or reverse bias is several orders of magnitude larger than the DT current, which directly leads to a low contact resistivity of SiC ohmic contacts. Then, we tried to clarify the voltage-dependent changes in the trap level that dominantly contributes to the enhanced tunneling current based on the E_T dependence of $P_{TAT}(E)$ under each bias condition.

Figure 4(a) shows the calculated DT and TAT currents in a forward-biased n-type SiC Schottky structure. The calculated band diagram, tunneling probability, and tunneling current as a function of the energy are extracted for two applied voltage conditions of $V = +0.05\,\text{V}$ and $+0.25\,\text{V}$, and are shown in Figs. 4(b) and 4(c), respectively. Under a very low forward bias of $V = +0.05\,\text{V}$, a defect with the energy level of $E_C - E_T = 0.4\,\text{eV}$ gives the highest tunneling probability in a lower energy range among various trap levels, resulting from an almost identical tunneling distance for the two paths divided. Although the trap level of $E_C - E_T = 0.4\,\text{eV}$ enhances the tunneling probability in a limited energy range compared with $E_C - E_T = 0.3\,\text{eV}$, the highest probability for TAT with $E_C - E_T = 0.4\,\text{eV}$ at a lower energy, where more electrons exist, effectively increases the tunneling current, as seen in Fig. 4(b). On the other hand, the dominant trap level is changed at an increased applied voltage of $V = +0.25\,\text{V}$. In this situation, the dividing position for deeper traps ($E_C - E_T \geq 0.4\,\text{eV}$) shifts toward the interface side, leading to the relationship of $P_1(E) \ll P_2(E)$ and reduced value of $P_{TAT}(E)$. Note that a "hump" found in the forward I–V curves with deep traps ($E_C - E_T \geq 0.4\,\text{eV}$) can also be explained by the shift of the dividing position and is not due to a barrier inhomogeneity. Accordingly, a higher TAT probability resulting from $P_1(E) \simeq P_2(E)$ and a larger tunneling current are obtained with a relatively shallow trap level ($E_C - E_T = 0.3\,\text{eV}$), as shown in Fig. 4(c). As a result, under a forward bias, it is found that the dominant trap level is sensitively varied depending on the applied voltage condition: Traps with the energy level of $E_C - E_T = 0.4\,\text{eV}$ contribute to the enhanced tunneling current at a very low voltage, while a shallower trap ($E_C - E_T = 0.3\,\text{eV}$) turns to be responsible at a higher forward voltage.

Figure 5(a) plots the reverse I–V characteristics at an n-type SiC Schottky contact calculated based on the TAT and DT models, and Figs. 5(b) and 5(c) show the energy band diagram, tunneling probability, and tunneling current under a low reverse bias voltage ($V = -0.30\,\text{V}$) and a higher reverse bias ($V = -1.0\,\text{V}$), respectively. As found in Figs. 5(b) and 5(c), a larger tunneling current is obtained when the tunneling probability at the energy near E_{Fm} (indicated by a chain line in the figure) is higher. In contrast to the forward bias conditions, the dividing position for the tunneling path is not much changed depending on the applied voltage, and a trap with the energy level of $E_C - E_T = 0.5\,\text{eV}$ provides the highest tunneling probability and largest tunneling current under the two applied voltage conditions. The TAT current becomes smaller when assuming deeper traps with $E_C - E_T > 0.5\,\text{eV}$ due to the unbalance between $P_1(E)$ and $P_2(E)$ near E_{Fm}. As a result, almost

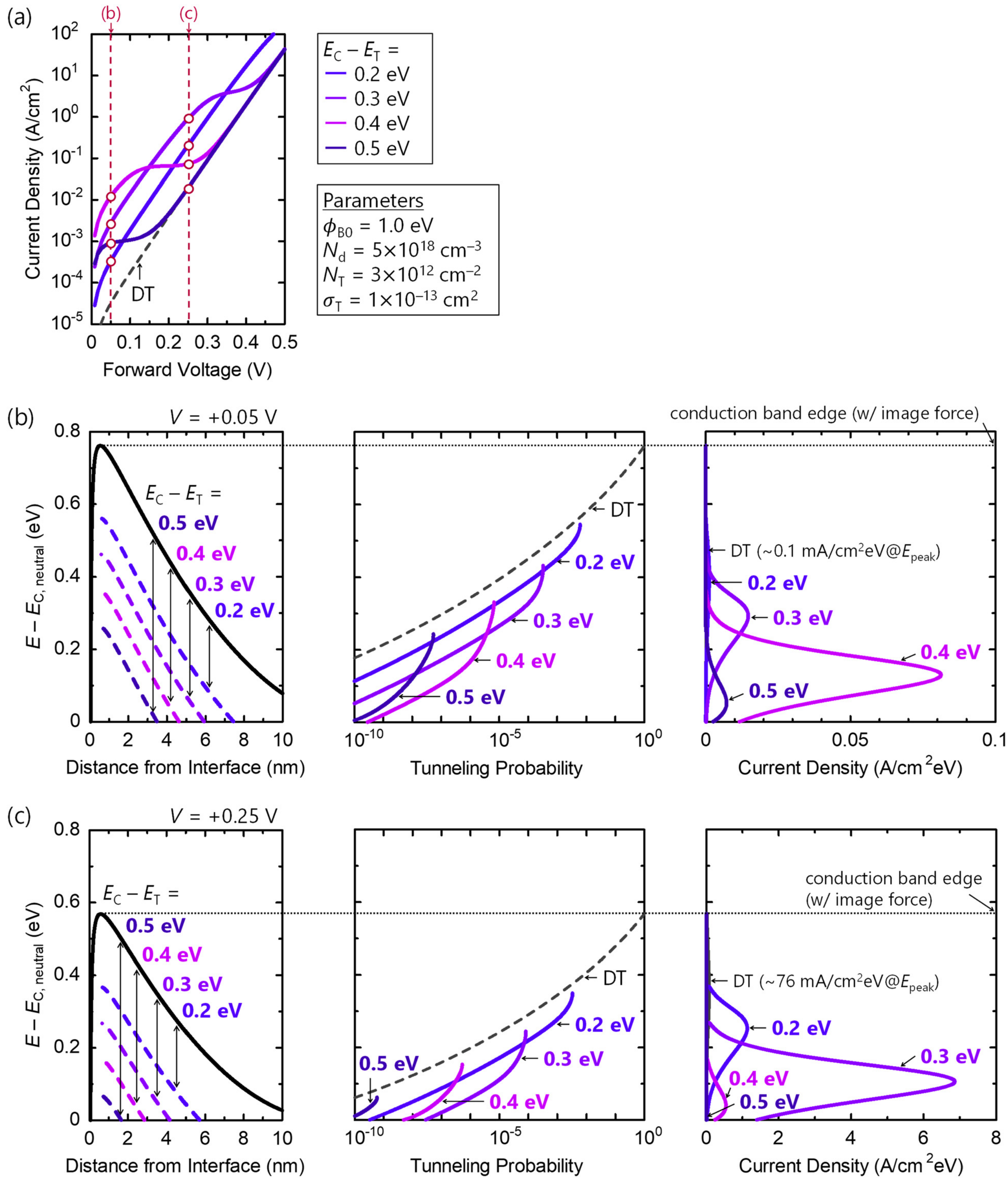


FIG. 4. (a) Forward *I–V* characteristics at an n-type SiC Schottky contact calculated based on the TAT model. Band diagram, tunneling probability and tunneling current as a function of electron energy at (b) a low voltage ($V = +0.05$ V) and (c) a higher voltage ($V = +0.25$ V). $E_{C,\text{ neutral}}$ is the conduction band edge in the neutral region in SiC.

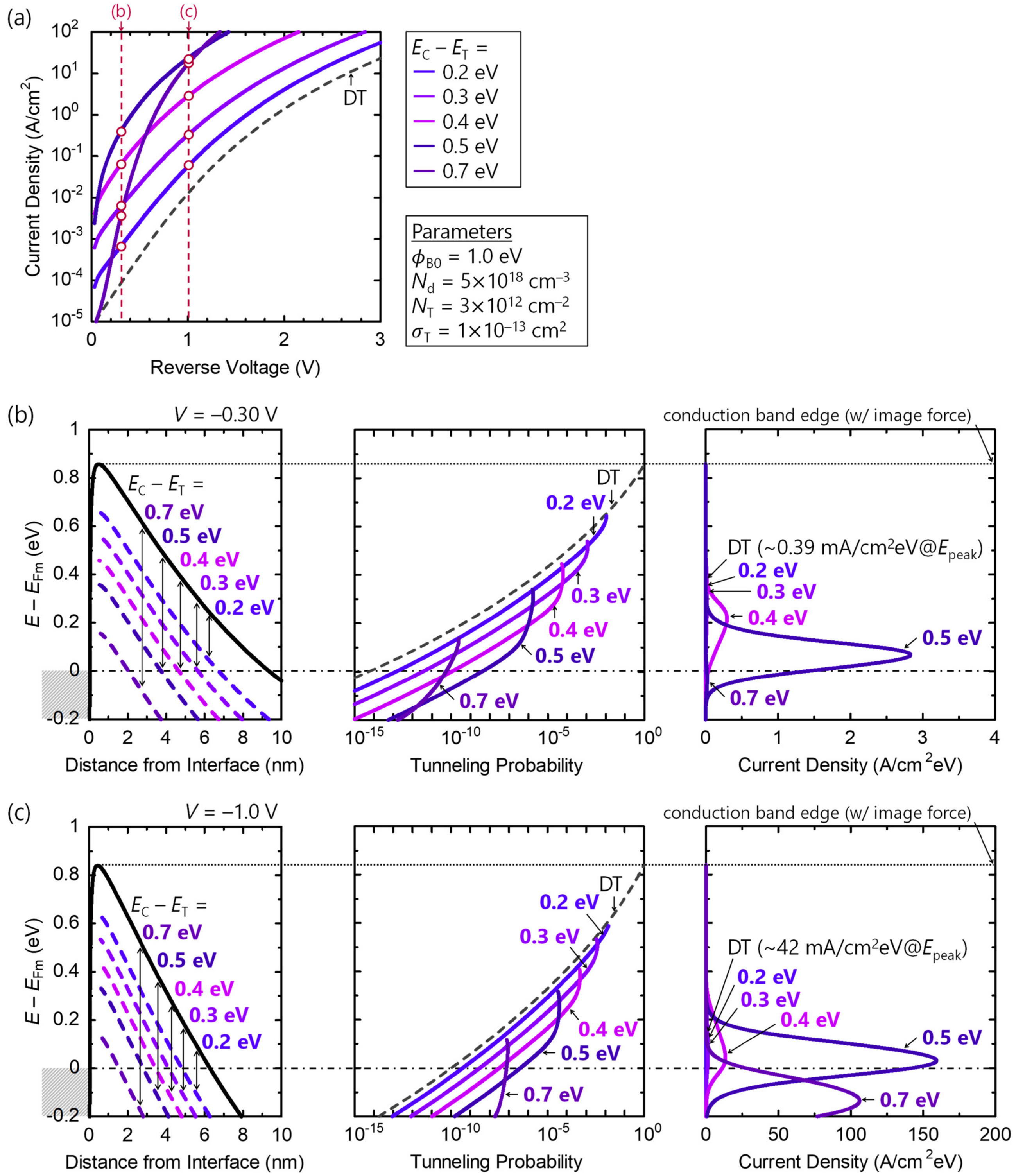


FIG. 5. (a) Reverse I–V characteristics at an n-type SiC Schottky contact calculated based on the TAT model. Band diagram, tunneling probability, and tunneling current as a function of electron energy at (b) a low voltage ($V = -0.30$ V) and (c) a higher voltage ($V = -1.0$ V). E_{Fm} is the Fermi level in the metal.

TABLE I. Major traps in P$^+$-implanted SiC and their energy levels, capture cross sections, and densities reported based on DLTS measurement.[34] The trap density is the value obtained after performing thermal oxidation (1150 °C, 2 h) for two times.

Label	Dose (cm^{-2})	Impurity density (cm^{-3})	Energy level (eV)	Capture cross section (cm^2)	Trap density (cm^{-3})
IN2 (ID_8)	8.0×10^{13}	1×10^{18}	0.30	10^{-18}	$<2 \times 10^{15}$
IN3 ($Z_{1/2}$)	5.6×10^{10}	7×10^{14}	0.63	10^{-14}	2×10^{14}
IN6	8.0×10^{13}	1×10^{18}	1.0	10^{-15}	$<7 \times 10^{15}$
IN8	8.0×10^{13}	1×10^{18}	1.2	10^{-15}	$<4 \times 10^{15}$
IN9 ($EH_{6/7}$)	5.6×10^{10}	7×10^{14}	1.5	10^{-14}	2×10^{14}

in the entire voltage range calculated, a trap level with $E_C - E_T = 0.5$ eV, which is half of the Schottky barrier height ($\phi_{B0} = 1.0$ eV), is the dominant trap level contributing to the enhanced tunneling current under a reverse bias condition.

IV. DISCUSSION

Based on the numerical calculation presented above, trap levels that may significantly enhance the TAT current at metal/heavily P$^+$-implanted n-type SiC interfaces with $\phi_{B0} = 1.0$ eV are presumed to be $E_C - E_T = 0.3-0.5$ eV, depending on the applied voltage condition. These trap levels are compared with implantation-induced defects reported for P$^+$-implanted SiC based on deep-level transient spectroscopy (DLTS) measurements,[34] which are listed in Table I with the implantation dose and the impurity density. Considering only the energy level of traps, IN2 (ID_8) and IN3 ($Z_{1/2}$) centers, whose energy levels are $E_C - E_T$ = 0.30 and 0.63 eV, respectively, are expected as responsible traps for enhancing the TAT current among the reported deep levels. On the other hand, focusing on the other trap parameters, especially the capture cross section, the numerical calculation in this study assumed a much higher value of σ_T than the reported values, even if this parameter for the interaction with tunneling carriers might differ from that with carriers inside the conduction band, as mentioned above.

Figure 6 shows the experimental $I-V$ characteristics of the Ti/n-type SiC vertical SBDs fabricated using P$^+$-implanted SiC ($N_D = 5 \times 10^{18}$ cm^{-3}).[35] The values of the series resistance (R_s) were extracted from the experimental forward and reverse $I-V$ curves as 33 and 95 mΩcm^2, respectively, and the voltage drop due to R_s was considered when plotting the calculated $I-V$ curves. Since a hump is not found in the experimental forward $I-V$ curves, it is expected that the dominant trap level continuously changes depending on the applied voltage, and traps with $E_C - E_T = 0.3$ and 0.4 eV would be mainly responsible for the enhanced tunneling current. On the other hand, the calculated TAT current through these traps is still much smaller than the experimental forward $I-V$ curves, especially at a low voltage, as seen in Fig. 6. Although the calculation of the TAT current with $E_C - E_T = 0.5$ eV seems to reasonably reproduce the experimental reverse $I-V$ characteristics, the validity of the trap parameters used in the calculation cannot be ensured at the present stage. Therefore, it is the next subject of study to reveal the reason for the large tunneling current in Schottky structures formed on heavily ion-implanted SiC. Elucidation of the defect properties in ion-implanted SiC with a very high doping concentration is an important future challenge. While the maximum doping density for DLTS-based characterization of deep levels was limited up to 1×10^{18} cm^{-3} in literature,[33,34] it is expected that more heavily ion-implanted SiC contains more various kinds and larger numbers of point defects. While a uniform distribution of implantation-induced traps was assumed in the calculation, the trap density near the surface of SiC could be higher than a deeper region, which could lead to a larger TAT current. Thus, this assumption should be carefully considered based on the experimental validation. Besides, the presence of extended defects (e.g., stacking faults) is also expected in heavily ion-implanted SiC, which form quantum wells at the band edge and possibly contribute to the TAT current. These defects should be identified based on careful electrical measurements (e.g., DLTS) and structural analyses [e.g., transmission electron microscopy (TEM)], and the numerical calculation should be improved with updated defect parameters in the future.

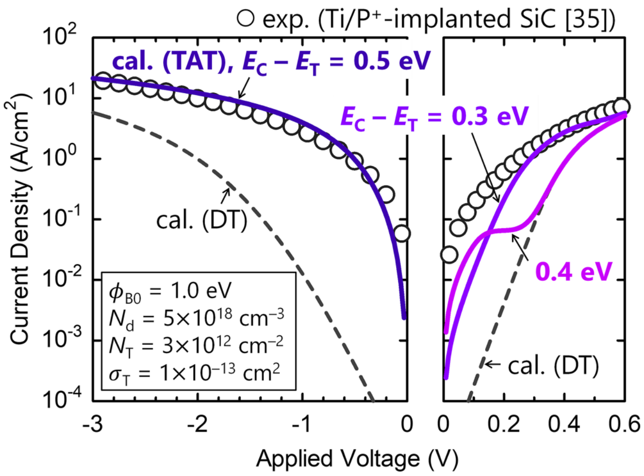


FIG. 6. Experimental $I-V$ characteristics at a Ti Schottky contact formed on P$^+$-implanted n-type SiC (symbols)[35] and calculated DT and TAT currents (dashed and solid lines, respectively). Voltage drop due to a series resistance is considered in plotting the calculated $I-V$ curves.

V. CONCLUSION

In this study, the energy level of a trap that dominantly contributes to the enhanced tunneling current at metal/heavily P^+-implanted SiC interfaces was studied through the numerical calculation of the TAT current. In the case of the barrier height and donor density of 1.0 eV and $5 \times 10^{18}\,\mathrm{cm}^{-3}$, respectively, the applied voltage-dependent changes in the dominant deep levels were discussed based on the tunneling probability and tunneling current as a function of the electron energy. It was found that a relatively deep level of $E_C - E_T = 0.4\,\mathrm{eV}$ mainly contributes to the increased TAT current under a small forward bias ($V \lesssim +0.1\,\mathrm{V}$), while the contribution of shallower defect levels ($E_C - E_T = 0.3\,\mathrm{eV}$) becomes dominant at a higher forward voltage. As for reverse I–V characteristics, a trap with the energy level of $E_C - E_T = 0.5\,\mathrm{eV}$, which is the half of the barrier height, is responsible for the enhanced TAT current in an entire voltage range. The insight regarding how the TAT current is influenced by the energy level of traps is beneficial for deeper understanding of the carrier transport phenomena at metal/heavily doped SiC and for designing low-resistance ohmic contacts on SiC.

ACKNOWLEDGMENTS

This work was supported in part by a Kakenhi Grand-in-Aid (Nos. 21J22891, 22KJ1709, and 21H05003) from the Japan Society for the Promotion of Science (JSPS) and the Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) Program of the Japan Science and Technology Agency (JST).

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Masahiro Hara: Conceptualization (equal); Data curation (lead); Formal analysis (lead); Funding acquisition (equal); Investigation (lead); Validation (equal); Visualization (lead); Writing – original draft (lead). **Hajime Tanaka:** Formal analysis (supporting); Funding acquisition (equal); Investigation (supporting); Project administration (supporting); Supervision (supporting); Validation (equal); Visualization (supporting); Writing – review & editing (equal). **Mitsuaki Kaneko:** Funding acquisition (equal); Investigation (supporting); Project administration (supporting); Resources (equal); Supervision (supporting); Validation (equal); Visualization (supporting); Writing – review & editing (equal). **Tsunenobu Kimoto:** Conceptualization (equal); Funding acquisition (lead); Investigation (supporting); Project administration (lead); Resources (equal); Supervision (lead); Validation (equal); Visualization (supporting); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] B. J. Baliga, IEEE Electron Device Lett. **10**, 455 (1989).
[2] T. Kimoto, Jpn. J. Appl. Phys. **54**, 040103 (2015).
[3] J. A. Cooper and D. T. Morisette, IEEE Electron Device Lett. **41**, 892 (2020).
[4] T. Kimoto, Proc. Jpn. Acad. Ser. B **98**, 161 (2022).
[5] K. Hamada, S. Hino, N. Miura, H. Watanabe, S. Nakata, E. Suekawa, Y. Ebiike, M. Imaizumi, I. Umezaki, and S. Yamakawa, Jpn. J. Appl. Phys. **54**, 04DP07 (2015).
[6] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, IEEE Trans. Ind. Electron. **64**, 8193 (2017).
[7] T. Kimoto and H. Watanabe, Appl. Phys. Express **13**, 120101 (2020).
[8] J. B. Casady and R. W. Johnson, Solid State Electron. **39**, 1409 (1996).
[9] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, Proc. IEEE **90**, 1065 (2002).
[10] J.-Y. Lee, S. Singh, and J. A. Cooper, IEEE Trans. Electron Devices **55**, 1946 (2008).
[11] P. G. Neudeck, S. L. Garverick, D. J. Spry, L.-Y. Chen, G. M. Beheim, M. J. Krasowski, and M. Mehregany, Phys. Status Solidi A **206**, 2329 (2009).
[12] L. Lanni, R. Ghandi, B. G. Malm, C.-M. Zetterling, and M. Östling, IEEE Trans. Electron Devices **59**, 1076 (2012).
[13] M. Kaneko, M. Nakajima, Q. Jin, and T. Kimoto, IEEE Electron Device Lett. **43**, 997 (2022).
[14] M. A. Capano, R. Santhakumar, R. Venugopal, M. R. Melloch, and J. A. Cooper, J. Electron. Mater. **29**, 210 (2000).
[15] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, J. Appl. Phys. **96**, 224 (2004).
[16] Y. Negoro, T. Kimoto, H. Matsunami, F. Schmid, and G. Pensl, J. Appl. Phys. **96**, 4916 (2004).
[17] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications* (John Wiley & Sons, 2014), pp. 1–538.
[18] M. Laube, F. Schmid, G. Pensl, G. Wagner, M. Linnarsson, and M. Maier, J. Appl. Phys. **92**, 549 (2002).
[19] J. Senzaki, K. Fukuda, and K. Arai, J. Appl. Phys. **94**, 2942 (2003).
[20] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensi, J. Heindl, H. P. Strunk, and M. Maier, Phys. Status Solidi A **162**, 277 (1997).
[21] J. M. Bluet, J. Pernot, J. Camassel, S. Contreras, J. L. Robert, J. F. Michaud, and T. Billon, J. Appl. Phys. **88**, 1971 (2000).
[22] M. Vivona, G. Greco, M. Spera, P. Fiorenza, F. Giannazzo, A. La Magna, and F. Roccaforte, J. Phys. D: Appl. Phys. **54**, 445107 (2021).
[23] M. Hara, M. Kaneko, and T. Kimoto, Appl. Phys. Express **16**, 021003 (2023).
[24] L. M. Porter and R. F. Davis, Mater. Sci. Eng. B **34**, 83 (1995).
[25] J. Crofton, L. M. Porter, and J. R. Williams, Phys. Status Solidi B **202**, 581 (1997).
[26] F. Roccaforte, F. La Via, and V. Raineri, Int. J. High Speed Electron. Syst. **15**, 781 (2005).
[27] M. Hara, S. Asada, T. Maeda, and T. Kimoto, Appl. Phys. Express **13**, 041001 (2020).
[28] M. Hara, H. Tanaka, M. Kaneko, and T. Kimoto, Appl. Phys. Lett. **120**, 172103 (2022).
[29] T. Kitawaki, M. Hara, H. Tanaka, M. Kaneko, and T. Kimoto, Appl. Phys. Express **16**, 031005 (2023).
[30] K. Kuwahara, T. Kitawaki, M. Hara, M. Kaneko, and T. Kimoto, Jpn. J. Appl. Phys. **63**, 050903 (2024).
[31] T. Dalibor, G. Pensl, H. Matsunami, T. Kimoto, W. J. Choyke, A. Schöner, and N. Nordell, Phys. Status Solidi A **162**, 199 (1997).
[32] M. L. David, G. Alfieri, E. M. Monakhov, A. Hallén, C. Blanchard, B. G. Svensson, and J. F. Barbot, J. Appl. Phys. **95**, 4728 (2004).
[33] K. Kawahara, G. Alfieri, and T. Kimoto, J. Appl. Phys. **106**, 013719 (2009).

[34]K. Kawahara, J. Suda, G. Pensl, and T. Kimoto, J. Appl. Phys. **108**, 033706 (2010).
[35]M. Hara, T. Kitawaki, H. Tanaka, M. Kaneko, and T. Kimoto, Mater. Sci. Semicond. Process. **171**, 108023 (2024).
[36]W. A. Harrison, Phys. Rev. **123**, 85 (1961).
[37]G. H. Parker and C. A. Mead, Appl. Phys. Lett. **14**, 21 (1969).
[38]J. C. Penley, Phys. Rev. **128**, 596 (1962).
[39]J. W. Gadzuk, J. Appl. Phys. **41**, 286 (1970).
[40]D. Volm, B. K. Meyer, D. M. Hofmann, W. M. Chen, N. T. Son, C. Persson, U. Lindefelt, O. Kordina, E. Sörman, A. O. Konstantinov, B. Monemar, and E. Janzén, Phys. Rev. B **53**, 15409 (1996).
[41]S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices*, 4th ed. (John Wiley & Sons, 2021).
[42]M. Hara, M. Kaneko, and T. Kimoto, Jpn. J. Appl. Phys. **60**, SBBD14 (2021).
[43]A. Itoh and H. Matsunami, Phys. Status Solidi A **162**, 389 (1997).