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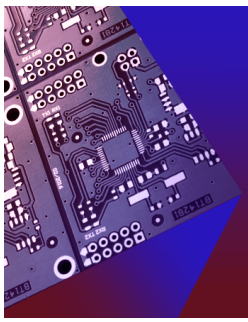

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# First-order SPICE modeling of SiC p- and n-channel side-gate JFETs toward high-temperature complementary JFET ICs

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## AFFILIATIONS

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## ABSTRACT

A device model of silicon carbide (SiC) p- and n-channel junction field-effect transistors (JFETs) applicable in a high-temperature range was constructed, and the validity of the model was evaluated in Simulation Program with Integrated Circuit Emphasis (SPICE) simulations. The constructed device model well reproduced the electrical characteristics of the JFETs fabricated in our previous study over a wide temperature range from room temperature to 573 K. Furthermore, the static and dynamic characteristics of a SiC complementary JFET inverter were simulated with the constructed device model, and the temperature dependence of the logic threshold voltage showed good agreement, where the differences between the measurements and calculations were as small as 0.05 V.





## I. INTRODUCTION

Silicon carbide (SiC) has been studied as one of the most promising materials for low-loss power device applications owing to its unique physical properties, such as a high critical electric field and wide bandgap.[1,2] SiC Schottky barrier diodes and SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) have been commercially available since the 2010s.[3] SiC is also promising for the application of integrated circuits (ICs) operating under high-temperature environments, such as automotive, space exploration, and deep-well drilling.[4–6] Most commercially available ICs consist of silicon (Si) complementary metal–oxide–semiconductor (CMOS) devices, which cannot operate above 473 K due to the physical limit of Si. Then, Si CMOS on silicon-on-insulator (SOI) has been proposed, and operation at up to 573 K has been confirmed.[7] On the other hand, SiC devices can operate in the temperature range in which Si devices cannot operate (>573 K) since the intrinsic carrier density of SiC is much lower than that of Si. Furthermore, doping concentrations in the p- and n-type regions of SiC can be controlled over a wide range ($10^{14}$–$10^{19}$ $cm^{-3}$) relatively easily by ion implantation,[2] which is exceptional as a wide bandgap semiconductor material.

Several transistors are considered to be suitable for configuring ICs operational at high temperatures. High-temperature operations of SiC MOSFETs,[8,9] bipolar junction transistors,[10–13] and junction field-effect transistors (JFETs)[14,15] have been reported. Among them, JFETs are expected to be more reliable than the other devices since the JFETs have stable threshold voltages over a wide temperature range and no gate oxide. Neudeck *et al.* reported that highly functional logic gates and memories were configured by SiC (depletion-mode) n-JFETs and resistors (JFET-R), and their operation at 773 K was demonstrated.[15] One of the disadvantages of the JFET-R circuit, however, is its high static power consumption since the current continues to flow through the resistor and n-JFET even without an input signal.

A complementary JFET (CJFET) circuit can be assembled with p- and n-JFETs in the same manner as CMOS circuits. We have demonstrated normal transistor operations at up to 673 K of SiC p- and n-channel JFETs fabricated by ion implantation into a high-purity semi-insulating (HPSI) SiC substrate.[16,17] Moreover,

operations of SiC CJFET logic gates were demonstrated from room temperature to 623 K.[18]

For the fabrication of SiC CJFET logic gates and memories, device models of SiC p- and n-JFETs that predict their electrical characteristics from room temperature to high temperature are required to design a circuit and perform simulations. In prior works, a first-order Simulation Program with Integrated Circuit Emphasis (SPICE) modeling for SiC n-JFETs operating at high temperatures was reported.[19–21] In their model, parameter fitting was performed based on n-channel MOSFET, which is not practical for calculating n-JFETs with different structural parameters. The SPICE model using gradual channel approximation and abrupt depletion approximation for JFETs was originally proposed for Si JFETs.[22–24] While there exist some reports on SiC n-JFET physics-based device models,[25,26] they are supposed to be applied to n-JFETs for power device applications, where operation at high temperature (>473 K) is not considered. Moreover, a SiC p-JFET device model has not been reported.

In this study, device models of SiC p- and n-JFETs are developed for the circuit design of SiC CJFET. The electrical characteristics of SiC p- and n-JFETs were calculated based on Makris's model in Ref. 27, considering incomplete ionization of dopants. Note that equations are derived in a procedure different from the prior model.[27] The current–voltage characteristics of SiC p- and n-JFETs were calculated with the developed device model and compared with the experimental data. The temperature dependence of the subthreshold slopes showed good agreement with the measured ones at up to 573 K. In addition, the characteristics of a SiC CJFET inverter were simulated, and the results agreed well with the experimental ones within a wide temperature range.

## II. MODEL EQUATIONS OF SIC p- AND n-JFETS

Figure 1 shows a schematic diagram of p- and n-JFETs fabricated in our previous study. The JFETs have side-gate structures where two gates are horizontally placed beside the channel. Figure 2 shows the schematic top and cross-sectional views of a side-gate n-JFET. $N_{D,ch}$, $N_{A,G}$, $L_n$, $W_n$, and $a_n$ are the donor concentration in the channel region, the acceptor concentration in the gate region, the channel length, the channel width, and the channel thickness of an n-JFET, respectively. Then, the device structure is the same as that considered in Ref. 27, and we constructed the device model based on the literature. The energy band diagrams at $x = x'$ and $y = 0$ are depicted in Figs. 3(a) and 3(b), respectively. The Poisson equation

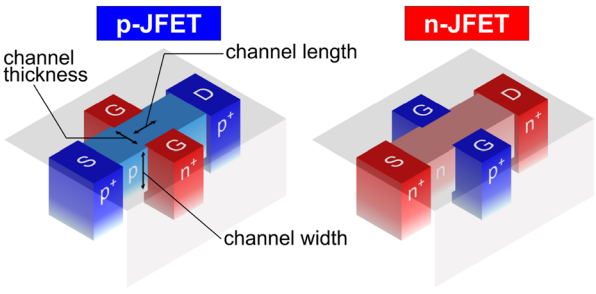


**FIG. 1.** Schematic structures of SiC side-gate p- and n-JFETs.[17]

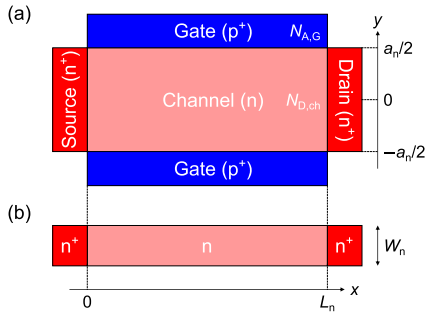


**FIG. 2.** Schematic (a) top and (b) side views of a side-gate n-JFET.

in the $y$-direction at $x = x'$ under gradual channel approximation is given by the following equation:[28]

$$\frac{d^2\psi_n(y)}{dy^2} = -\frac{q}{\varepsilon}[N_{D,ch} - n_{ch}(y)] = -\frac{q}{\varepsilon}\left\{N_{D,ch} - n_i \exp\left[\frac{E_{Fn}(x') - E_i(y)}{k_B T}\right]\right\} = -\frac{q}{\varepsilon}\left\{N_{D,ch} - n_i \exp\left[\frac{\psi_n(y) - V_n(x')}{U_T}\right]\right\}. \quad (1)$$

Here, $\psi_n(y), q, \varepsilon, n_{ch}(y), n_i, E_{Fn}(x'), E_i(y), k_B, T, V_n(x')$, and $U_T$ are the electrostatic potential in the channel region, the elementary charge, the permittivity in the semiconductor, the electron density in the channel region, the intrinsic carrier concentration, the quasi-Fermi level, the intrinsic Fermi level, the Boltzmann's constant, temperature, the potential difference between $x = 0$ and $x = x'$, and the thermal voltage, respectively. Using the finite difference

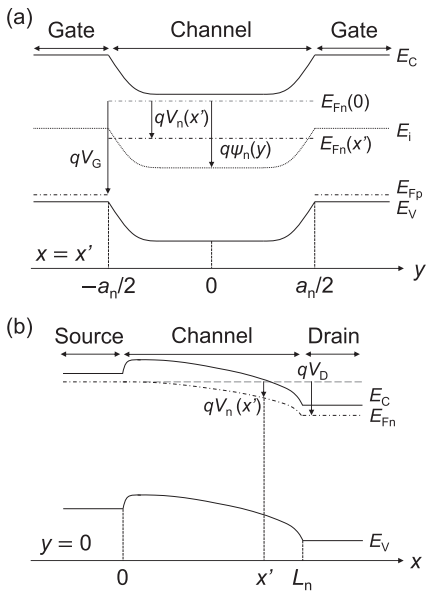


**FIG. 3.** Energy band diagram of a side-gate n-JFET along (a) the $y$-axis at $x = x'$ and (b) the $x$-axis at $y = 0$.

method, the second order differential of $\psi_n(y)$ can be approximated as[28]

$$\left.\frac{d^2\psi_n(y)}{dy^2}\right|_{y=0} = \frac{\frac{\psi_n(-a_n/2)-\psi_n(0)}{a_n/2} - \frac{\psi_n(0)-\psi_n(a_n/2)}{a_n/2}}{a_n/2} = \frac{8(\psi_{s,n}-\psi_{0,n})}{a_n^2}, \quad (2)$$

where $\psi_{s,n} = \psi_n(\pm a/2)$ and $\psi_{0,n} = \psi_n(0)$. Thus, setting $y = 0$ in Eq. (1), the relationship between $\psi_{s,n}$ and $\psi_{0,n}$ is given by

$$\psi_{s,n} - \psi_{0,n} = \frac{qa_n^2}{8\varepsilon}\left\{n_i \exp\left[\frac{\psi_{0,n} - V_n(x')}{U_T}\right] - N_{D,ch}\right\}. \quad (3)$$

The mobile charge (areal) density, which corresponds to the electrons in the channel region contributing to the drain current, can be expressed as the following equation:[27,28]

$$Q_{m,n} = -qN_{D,ch}\left[a_n - 2\sqrt{\frac{2\varepsilon(\psi_{0,n}-\psi_{s,n})}{qN_{D,ch}}}\right] = \sqrt{b_n(\psi_{0,n}-\psi_{s,n})} - Q_{f,n}, \quad (4)$$

where $b_n = 8qN_{D,ch}\varepsilon$ and $Q_{f,n} = qN_{D,ch}a_n$ (the donor charge density in the channel region). Although the above equation is the same as that mobile charge density obtained assuming that the channel region consists of a fully depleted (band bending) region and a (flatband) region with a charge-neutral condition, Eq. (4) has been derived in a different procedure. Equation (4) is obtained by substituting Eq. (6) into Eq. (9) in Ref. 27. These equations are obtained (in the literature) assuming that the accumulation term can be omitted and the pinch-off voltage is much larger than the thermal voltage. Here, the first term in Eq. (4) ($\sqrt{b_n(\psi_{0,n}-\psi_{s,n})}$) coincides with the space charge of the two depletion layers in the channel region under depletion approximation, whereas depletion approximation is not assumed in the derivation. Using $b_n$ and $Q_{f,n}$, Eq. (3) is rewritten as

$$\psi_{s,n} - \psi_{0,n} = \frac{Q_{f,n}^2}{b_n}\left\{\frac{n_i}{N_{D,ch}}\exp\left[\frac{\psi_{0,n} - V_n(x')}{U_T}\right] - 1\right\}. \quad (5)$$

Then, the relationship between $Q_{m,n}$ and $V_n(x')$ is given by

$$V_G - V_n(x') - V_{bi,n} = \psi_{s,n} + U_T \ln\left(\frac{n_i}{N_{D,ch}}\right) - V_n(x') = -\frac{(Q_{m,n}+Q_{f,n})^2}{b_n} + U_T \ln\left[-\frac{Q_{m,n}(2Q_{f,n}+Q_{m,n})}{Q_{f,n}^2}\right]. \quad (6)$$

Here, $V_{bi,n}$ is defined as $V_{bi,n} = U_T \ln(N_{D,ch}N_{A,G}/n_i^2)$ and the following equations:

$$q\psi_{s,n} = E_i(\pm a_n/2) - E_{Fn}(0) = qV_G - k_B T \ln\left(\frac{N_{A,G}}{n_i}\right), \quad (7)$$

$$Q_{m,n}(2Q_{f,n}+Q_{m,n}) = (Q_{m,n}+Q_{f,n})^2 - Q_{f,n}^2 = b_n(\psi_{0,n}-\psi_{s,n}) - Q_{f,n}^2 = -\frac{Q_{f,n}^2 n_i}{N_{D,ch}}\exp\left[\frac{\psi_{0,n} - V_n(x')}{U_T}\right] \quad (8)$$

are considered.

In the previous model,[27] the dopant in the channel region was assumed to be fully ionized. In SiC, however, the ionization energy of dopants (nitrogen or phosphorus for n-type doping and aluminum for p-type doping) is not small, and incomplete ionization should be considered, especially for p-JFETs. Then, the drain current equation (in an n-JFET) used in Ref. 27 is corrected as follows:

$$I_{D,n} = -\mu_e W_n \eta_n Q_{m,n}\frac{dV_n(x)}{dx}, \quad (9)$$

where $\mu_e$ and $\eta_n$ are the electron mobility and the ionization ratio of the donors in the channel, respectively. Although the ionization ratio can depend on the position inside the channel according to the difference between static and quasi-Fermi potential, we assume that the ionization ratio is constant over the entire channel region for simplicity in this study. It should be noted that incomplete ionization affects potential distribution and changes the threshold voltage of JFETs, which is not implemented for the sake of simplicity in this study. $dV_n(x)/dx$ is obtained by replacing $x'$ by $x$ in Eq. (6) and differentiating both sides of Eq. (6) by $x$,

$$\frac{dV_n(x)}{dx} = \left[\frac{2(Q_{m,n}+Q_{f,n})}{b_n} - \frac{U_T(Q_{m,n}+Q_{f,n})}{Q_{m,n}(2Q_{f,n}+Q_{m,n})}\right]\frac{dQ_{m,n}}{dx}. \quad (10)$$

Integrating both sides of Eq. (9) from $x = 0$ (source) to $x = L_n$ (drain), the following equation is obtained:

$$\int_0^{L_n} I_{D,n}dx = -\mu_e W_n \eta_n \int_0^{L_n} Q_{m,n}\frac{dV_n(x)}{dx}dx. \quad (11)$$

Then, considering that the drain current is independent of $x$, the left-hand side of Eq. (11) is expressed as $\int_0^{L_n} I_{D,n}dx = I_{D,n}L_n$. Therefore, the drain current is obtained as

$$I_{D,n} = -\mu_e \frac{W_n}{L_n}\eta_n\left[f_n\left(Q_{m,n}^D\right) - f_n\left(Q_{m,n}^S\right)\right], \quad (12)$$

where $Q_{m,n}^S$ and $Q_{m,n}^D$ are the mobile charge density at $x = 0$ (source) and $x = L_n$ (drain), respectively, and $f_n(Q_{m,n})$ is defined as

$$f_n(Q_{m,n}) = \frac{2}{3b_n}Q_{m,n}^3 + \frac{Q_{f,n}}{b_n}Q_{m,n}^2 - 2U_T\left[Q_{m,n} - Q_{f,n}\ln(2Q_{f,n}+Q_{m,n})\right]. \quad (13)$$

In the same way as an n-JFET, the drain current in a p-JFET $I_{D,p}$ can be derived as the following equations:

$$I_{D,p} = -\mu_h \frac{W_p}{L_p}\eta_p\left[f_p\left(Q_{m,p}^D\right) - f_p\left(Q_{m,p}^S\right)\right], \quad (14)$$

$$f_p(Q_{m,p}) = \frac{2}{3b_p}Q_{m,p}^3 - \frac{Q_{f,p}}{b_p}Q_{m,p}^2 - 2U_T\left[Q_{m,p} + Q_{f,p}\ln(2Q_{f,p}-Q_{m,p})\right], \quad (15)$$

where $\mu_h$ and $\eta_p$ are the hole mobility and the ionization ratio of the acceptors in the channel, respectively. $b_p$ and $Q_{f,p}$ are defined as $b_p = 8qN_{A,ch}\varepsilon$ and $Q_{f,p} = qN_{A,ch}a_p$. $Q_{m,p}$ is expressed as

$$Q_{m,p} = Q_{f,p} - \sqrt{b_p(\psi_{s,p} - \psi_{0,p})}. \quad (16)$$

In the present model, parasitic resistances and capacitances are not modeled. For calculating dynamic characteristics in circuits with JFET loads, such parasitic resistances and capacitances are required, the modeling of which is our future study.

$\eta_n = n_{ch}/N_{D,ch}$ and $\eta_p = p_{ch}/N_{A,ch}$ are calculated by solving the neutrality equations,[29]

$$n_{ch} = \frac{N_{D,ch}/2}{1 + \frac{g_D n_{ch}}{N_C}\exp\left(\frac{\Delta E_{D,h}}{k_B T}\right)} + \frac{N_{D,ch}/2}{1 + \frac{g_D n_{ch}}{N_C}\exp\left(\frac{\Delta E_{D,k}}{k_B T}\right)}, \quad (17)$$

$$p_{ch} = \frac{N_{A,ch}/2}{1 + \frac{g_A p_{ch}}{N_V}\exp\left(\frac{\Delta E_{A,h}}{k_B T}\right)} + \frac{N_{A,ch}/2}{1 + \frac{g_A p_{ch}}{N_V}\exp\left(\frac{\Delta E_{A,k}}{k_B T}\right)}. \quad (18)$$

Here, $p_{ch}$, $g_D$ ($g_A$), $N_C$ ($N_V$), and $\Delta E_{D,i}$ ($\Delta E_{A,i}$) are the hole density in the channel region of a p-JFET, the degeneracy factor of the donor (acceptor), the effective density of states in the conduction band (valence band), and the ionization energy of the donor (acceptor) at $i$-site ($i$ = h, k), respectively. $g_D$ and $g_A$ were substituted by 2 and 4, respectively. $\Delta E_{D,i}$ and $\Delta E_{A,i}$ become smaller with increasing the doping concentration and are expressed as the following equations:[30]

$$\Delta E_{D,i} = \Delta E_{D,i0} - \alpha(N_{D,ch})^{1/3}, \quad (19)$$

$$\Delta E_{A,i} = \Delta E_{A,i0} - \alpha(N_{A,ch})^{1/3}, \quad (20)$$

where $\Delta E_{D,i0}$ ($\Delta E_{A,i0}$) is the ionization energy of the donor (acceptor) in the lightly doped SiC, and $\Delta E_{D,h0}$, $\Delta E_{D,k0}$, $\Delta E_{A,h0}$, and $\Delta E_{A,k0}$ are set to 60, 120, 198, and 201 meV, respectively.[3] $\alpha$ is a parameter and is set to $4 \times 10^{-8}$ eV cm.[3] $\mu_e$ and $\mu_h$ expressions reported in Refs. 31 and 32 are adopted in our device model, which are expressed as the following equations:

$$\mu_e = +\frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_d}{N_{ref}}\right)^{0.76}}, \quad (21)$$

$$\mu_h = \frac{95\ \text{cm}^2/\text{Vs} \times \left(\frac{T}{300\ \text{K}}\right)^{-2.1}}{1 + \left(\frac{T}{300\ \text{K}}\right)^{-1.5}\left(\frac{N_A}{1\times10^{19}\ \text{cm}^{-3}}\right)^{0.7}}. \quad (22)$$

Here, $\mu_{min} = 40 \times \left(\frac{T}{300\ \text{K}}\right)^{-0.5}$ cm$^2$/Vs, $\mu_{max} = 950 \times \left(\frac{T}{300\ \text{K}}\right)^{-2.4}$ cm$^2$/Vs, and $N_{ref} = 2 \times 10^{17} \times \frac{T}{300\ \text{K}}$ cm$^{-3}$. Short-channel effects are not considered in this model. When comparing the experimental and calculated characteristics, we chose JFETs with long channel devices where short-channel effects do not occur.[33] All circuit simulations were conducted in SmartSpice by Silvaco.[34] Note that source or drain parasitic resistances were not considered in the simulation.

## III. RESULTS AND DISCUSSION

### A. Current–voltage characteristics of SiC p- and n-JFETs

Figures 4 and 5 depict $I_D^{1/2}$–$V_G$ curves on a linear scale and $I_D$–$V_G$ characteristics on a semi-log scale of SiC p- and n-JFETs at $|V_D|$ = 2 V from 300 to 573 K, respectively. The solid lines and symbols denote the calculated results with our device model and

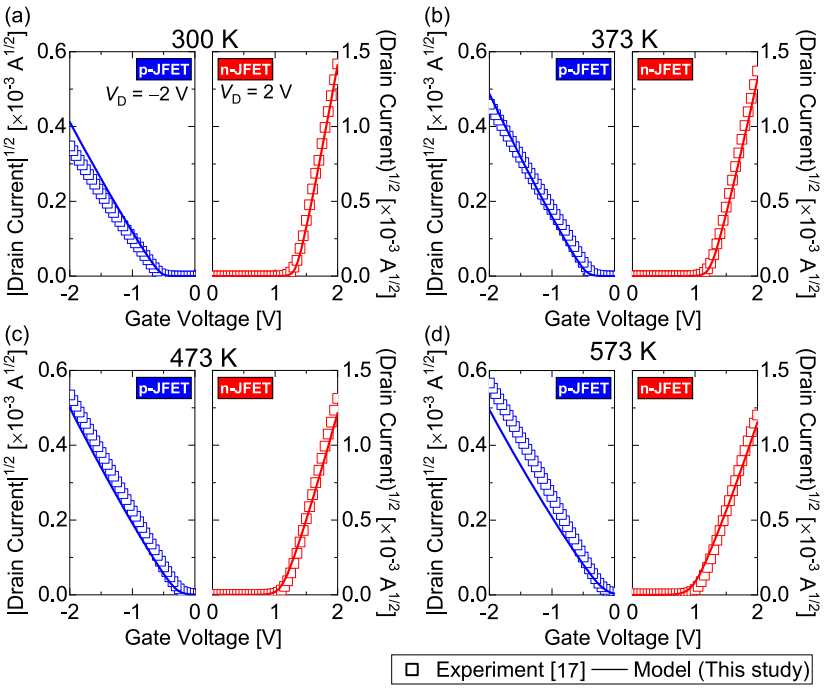


**FIG. 4.** (a)–(d) $I_D^{1/2}$–$V_G$ curves of SiC p- and n-JFETs at $|V_D|$ = 2 V from 300 to 573 K. Open square symbols and solid lines represent the experimental[17] and simulated results, respectively.

**TABLE I.** Major parameters used in simulations of the characteristics of SiC p- and n-JFETs extracted by fitting to the experimental results.

| p-JFET | | n-JFET | |
|---|---|---|---|
| Parameter | Value | Parameter | Value |
| $N_{A,ch}$ | $5 \times 10^{16}$ cm$^{-3}$ | $N_{D,ch}$ | $5 \times 10^{16}$ cm$^{-3}$ |
| $N_{D,G}$ | $5 \times 10^{19}$ cm$^{-3}$ | $N_{A,G}$ | $5 \times 10^{19}$ cm$^{-3}$ |
| $W_p/L_p$ | 0.3 $\mu$m/3.3 $\mu$m | $W_n/L_n$ | 0.6 $\mu$m/3.3 $\mu$m |
| $a_p$ | 460 nm | $a_n$ | 374 nm |

the measurement results of the JFETs fabricated in our previous study.[17] The major parameters in the calculations are shown in Table I. The doping concentrations are the same as those of the designed values, and the channel length, width, and thickness are the fitting parameters. The fitting parameters were fitted as temperature independent. The extracted values are slightly different from the designed ones due to the lateral straggling of the implanted atoms.[35,36] The device model constructed in this study well reproduced the electrical characteristics of the fabricated devices within all the measurement temperature ranges.

Figure 6 shows the temperature dependence of $V_{th}$ from 300 to 573 K. Closed circle and open square symbols represent the calculated data by the model constructed in this study and the measured data,[17] respectively. Those results agreed well from 300 to 573 K, and the differences between the measured and calculated results by our model were less than 0.05 V.

An analytical model (not our device model) describes the drain current of SiC p- and n-JFETs in the saturation region ($I_{Dp}, I_{Dn}$) by the following equations:[38]

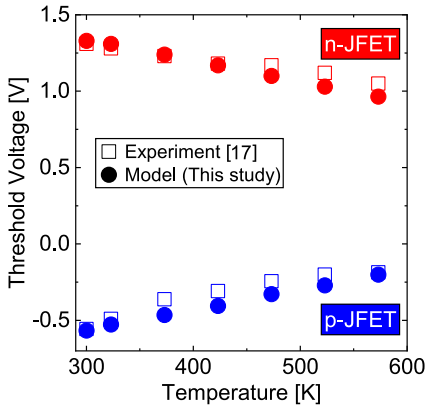


**FIG. 6.** Temperature dependence of threshold voltage $V_{th}$ in SiC p- and n-JFETs from 300 to 573 K. Open square and closed circle symbols correspond to the experimental[17] and simulated data, respectively.

$$I_{D,n} = \frac{\beta_n}{2}(V_{G,n} - V_{th,n})^2, \tag{23}$$

$$\beta_n = \frac{4\varepsilon W_n \mu_e n_{ch}}{L_n a_n N_{D,ch}}, \tag{24}$$

$$I_{D,p} = \frac{\beta_p}{2}(V_{G,p} - V_{th,p})^2, \tag{25}$$

$$\beta_n = \frac{4\varepsilon W_p \mu_h p_{ch}}{L_p a_p N_{A,ch}}, \tag{26}$$

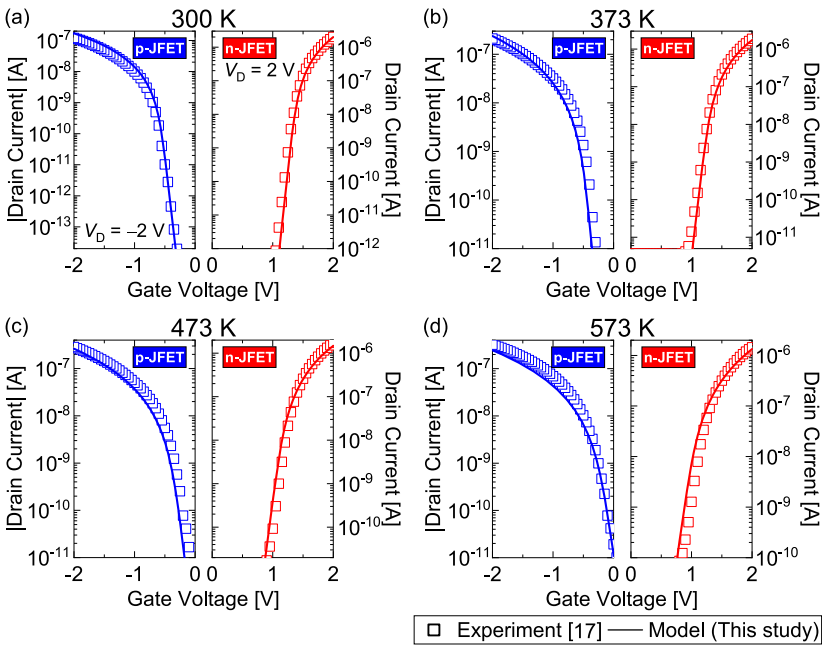


**FIG. 5.** (a)–(d) $I_D$–$V_G$ characteristics of SiC p- and n-JFETs at $|V_D| = 2$ V from 300 to 573 K on a semi-log scale. Open square symbols and solid lines denote the experimental[17] and simulated results, respectively.[37]

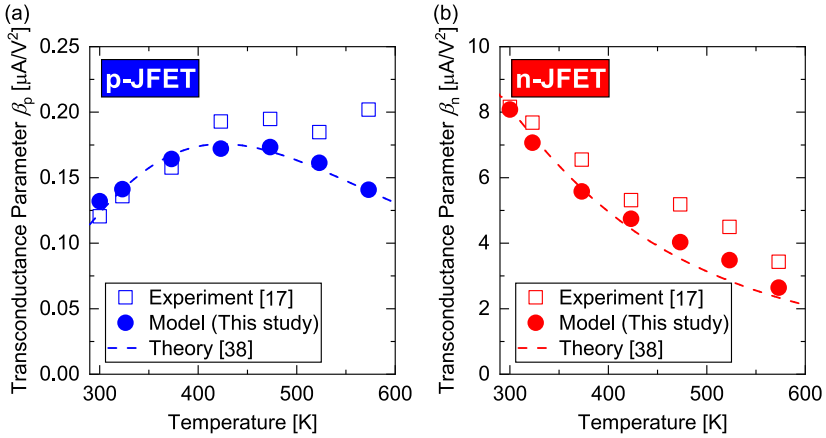


**FIG. 7.** (a) and (b) Temperature dependence of transconductance parameter $\beta$ in SiC p- and n-JFETs from 300 to 573 K. Open square and closed circle symbols correspond to the experimental[17] and simulated data, respectively. Dashed lines denote the theoretical $\beta$ predicted by the temperature dependence of the carrier mobility and the carrier concentration.[38]

where $\beta_n$ ($\beta_p$), $V_{th,n}$ ($V_{th,p}$), $p_G$ ($n_G$) are the transconductance parameter, the threshold voltage, and the hole (electron) concentration in the gate of an n-JFET (a p-JFET), respectively.

The temperature dependence of the transconductance parameters was obtained from the slope of the $I_D^{1/2}$–$V_G$ characteristics. Figure 7 depicts the temperature dependence of $\beta_n$ and $\beta_p$. Closed circle symbols, open square symbols, and dashed lines denote the simulated values by the developed device model, the experimental values,[17] and the theoretical estimations by Eqs. (24) and (26), respectively. Since the transconductance parameters cannot be expressed in analytical equations from the model provided in this study, $\beta_n$ and $\beta_p$ are extracted in the same way as obtained from the experimental curves. $\beta_n$ decreased with elevating the temperature due to the decrease in $\mu_e$. On the other hand, $\beta_p$ increased from room temperature to 473 K owing to the increase in $p_{ch}$ caused by the enhanced ionization of Al acceptors and decreased above 473 K due to the decrease in $\mu_h$. $\beta_p$ for the simulated and fabricated p-JFETs gradually deviates with elevating the temperature from 423 K. The current flowing through not only the channel region but also the undoped region in the HPSI SiC substrate, in which the resistivity becomes lower with elevating the temperature,[39] may cause the differences in $\beta_p$ at higher temperatures. Owing to the $\beta_p$ difference, the output characteristics of the fabricated p-JFETs show a slight deviation from those calculated by the model (not shown). Model refining is required, especially for p-JFET, to achieve further accurate simulation.

Figure 8 depicts the temperature dependence of the subthreshold swing ($SS$) extracted from $I_D$–$V_G$ characteristics. The closed circle and open square symbols denote the calculated and measured data,[17] respectively. The dashed lines indicate the theoretical limit of $SS$ in a JFET.[40] Although the measured $SS$ was slightly larger than the calculated and theoretical limits, the differences between the calculated and measured results were smaller than 15%.

## B. Static and dynamic characteristics of a SiC complementary JFET inverter

Figure 9 depicts a schematic structure of the SiC CJFET inverter assembled with side-gate JFETs fabricated in our previous study and a circuit diagram of a CJFET inverter. $V_{in}$, $V_{out}$, and $V_{dd}$ are the input voltage, the output voltage, and the supply voltage, respectively. The parameters used to calculate the characteristics of the

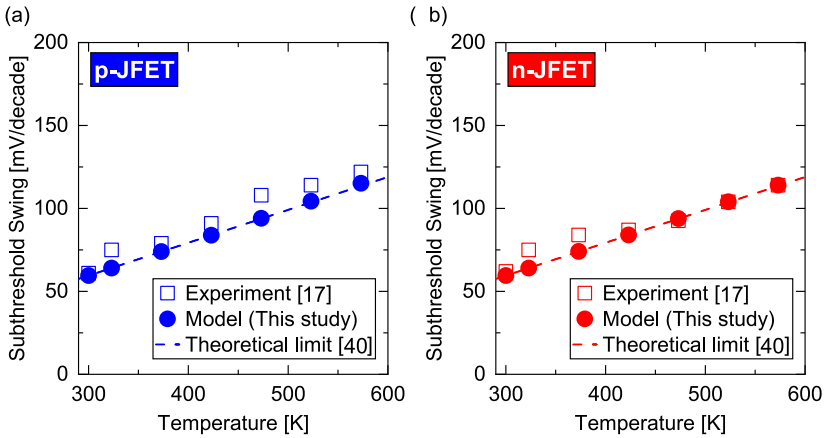


**FIG. 8.** (a) and (b) Temperature dependence of subthreshold swing $SS$ in SiC p- and n-JFETs from 300 to 573 K. Open square and closed circle symbols represent the experimental[17] and simulated data, respectively. Dashed lines correspond to the theoretical limit of $SS$.[40]

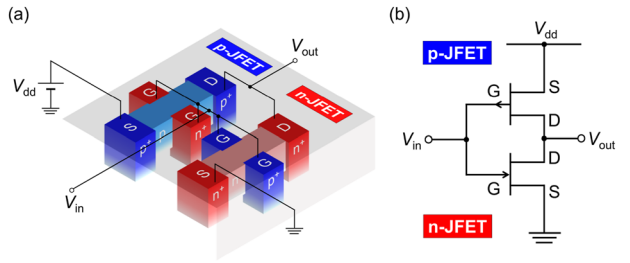


**FIG. 9.** (a) A schematic structure of the SiC CJFET inverter fabricated in our previous study and (b) a circuit diagram of a CJFET inverter.

**TABLE II.** Major parameters used in simulations of the characteristics of a SiC CJFET inverter.

| p-JFET | | n-JFET | |
|---|---|---|---|
| Parameter | Value | Parameter | Value |
| $N_{A,ch}$ | $5 \times 10^{16}$ cm$^{-3}$ | $N_{D,ch}$ | $5 \times 10^{16}$ cm$^{-3}$ |
| $N_{D,G}$ | $5 \times 10^{19}$ cm$^{-3}$ | $N_{A,G}$ | $5 \times 10^{19}$ cm$^{-3}$ |
| $W_p/L_p$ | 0.43 $\mu$m/4.0 $\mu$m | $W_n/L_n$ | 0.56 $\mu$m/4.0 $\mu$m |
| $a_p$ | 434 nm | $a_n$ | 430 nm |

CJFET inverter fabricated on an HPSI SiC substrate are shown in Table II, and $V_{dd}$ was set to 1.4 V.

The voltage transfer characteristics (VTCs) of a SiC CJFET inverter in a temperature range from 300 to 573 K are shown in Fig. 10. Solid lines and symbols with dashed lines represent the simulated and experimental results,[18] respectively. The SPICE simulations with the device model constructed in this study well reproduce the characteristics of the fabricated SiC CJFET inverter over a wide temperature range. At temperatures of 473 and 573 K, transition regions of the experimental VTC are slightly wider than the simulated VTC. The wider transition region may be due to the non-ideal leakage current mentioned in Sec. III A.

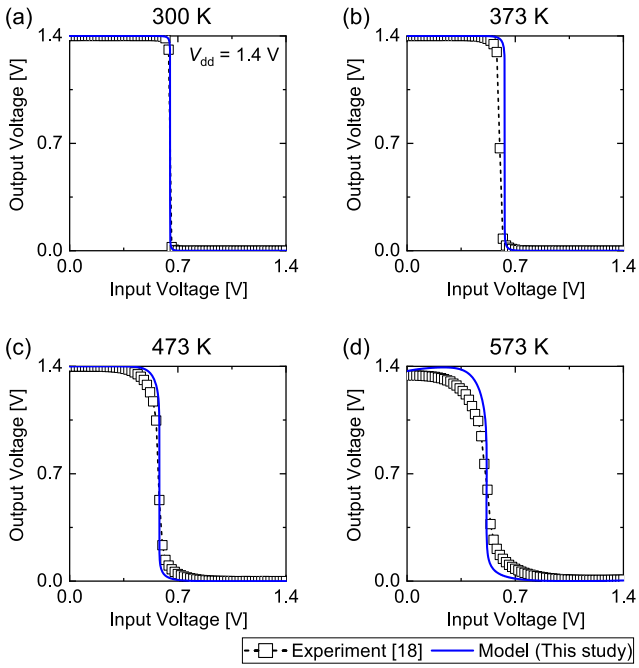


**FIG. 10.** (a)–(d) Voltage transfer characteristics of the SiC CJFET inverter at $V_{dd}$ = 1.4 V from 300 to 573 K. Open square symbols with dashed lines and solid lines represent the experimental[18] and simulated results, respectively.[37]

The logic threshold voltages ($V_{lth}$) and noise margins are extracted from the VTCs shown in Fig. 10. In this study, $V_{lth}$ was defined as $V_{in}$ at the maximum of $|dV_{out}/dV_{in}|$. The temperature dependence of $V_{lth}$ extracted from the VTCs is shown in Fig. 11. Open square and closed circle symbols correspond to the experimental[18] and simulated data, respectively. The simulated $V_{lth}$ agreed well with the experimental $V_{lth}$, and the differences between the simulated and experimental values are at most 0.05 V.

The low and high noise margins ($NM_L$ and $NM_H$) were defined by the following equations:

$$NM_L = V_{IL} - V_{OL}, \tag{27}$$

$$NM_H = V_{OH} - V_{IH}, \tag{28}$$

where $V_{IL}$ and $V_{OH}$ are defined as $V_{in}$ and $V_{out}$ at $dV_{out}/dV_{in} = -1$ within a transition region in the VTCs from the high level of $V_{out}$ to $V_{lth}$, and $V_{IH}$ and $V_{OL}$ are defined as $V_{in}$ and $V_{out}$ at $dV_{out}/dV_{in} = -1$ within a transition region in the VTCs from $V_{lth}$ to the low level of $V_{out}$. The temperature dependences of the $NM_L$ and $NM_H$ obtained from the VTCs are shown in Fig. 12. Closed circle and open square symbols are the simulated and experimental results,[18] respectively. The simulated $NM_L$ decreased and the simulated $NM_H$ increased with elevating the temperature, while both $NM_L$ and $NM_H$ of the fabricated SiC CJFET inverter decreased. The slight deviation is caused by the wider transition regions in the experimental VTCs, which is due to the non-ideal leakage current in the fabricated CJFET inverter. In the simulated results, the transition region is narrow, and an $NM_H$ increase is observed due to the $V_{lth}$ shift at higher temperatures.

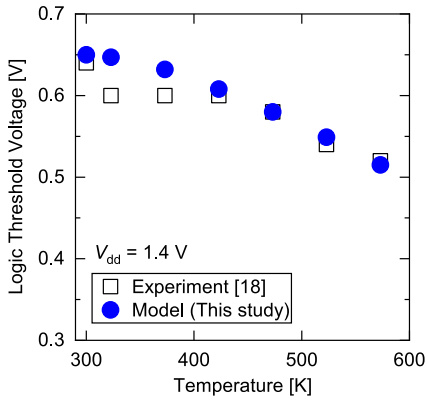


**FIG. 11.** Temperature dependence of the logic threshold voltages in a SiC CJFET inverter at $V_{dd}$ = 1.4 V from 300 to 573 K. Open square and closed circle symbols correspond to the experimental[18] and simulated data, respectively.

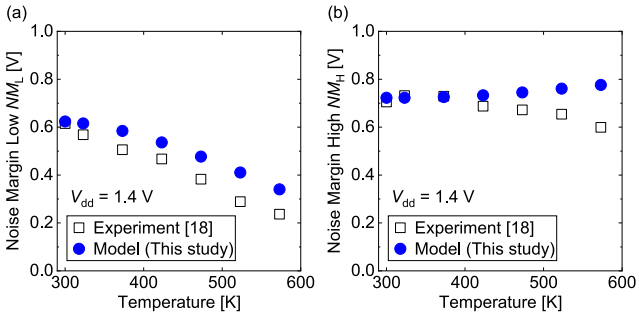


**FIG. 12.** (a) and (b) Temperature dependence of the noise margins in a SiC CJFET inverter at $V_{dd}$ = 1.4 V from 300 to 573 K. Open square and closed circle symbols correspond to the experimental[18] and simulated data, respectively.

Figure 13 presents the dynamic characteristics of a SiC CJFET inverter in a temperature range of 300–573 K. Dashed and solid lines denote the simulated and experimental results, respectively. A voltage follower circuit assembled with an op-amp (LT1793, Linear Technology) was connected to the output of the probe station due to the high output impedance of the fabricated SiC CJFET inverter.[18] Then, the load capacitance of 40 pF was connected to the output terminal of a SiC CJFET inverter in the SPICE simulations. As shown in Fig. 13, the simulations with our model well reproduced the output signals of the CJFET inverter fabricated in our previous study at up to 573 K. The rise and fall times ($t_r$, $t_f$) of the output signals were obtained as a time interval from 0% or 100% to 50%. The temperature dependences of $t_r$ and $t_f$ are shown in Fig. 14. $t_r$ and $t_f$ are inversely proportional to $I_{D,p}$ and $I_{D,n}$, respectively. With elevating temperature, $t_r$ decreases due to the increase in $I_{D,p}$. On the other hand, $t_f$ increases at higher temperatures, which is attributed to the decrease in $I_{D,n}$. As shown in Fig. 14, the simulated and experimental data were close at 300–573 K. These results indicate that the characteristics of the fabricated CJFET circuits can be predicted with our device model within a wide temperature range. It should be noted that the $t_r$ and $t_f$ are small, and the maximum operational

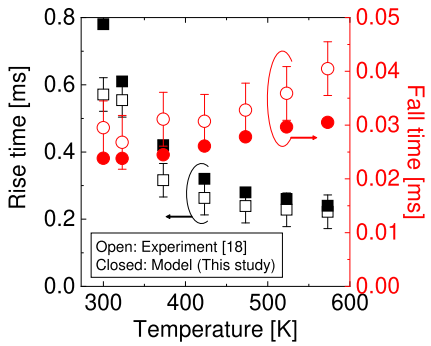


**FIG. 14.** Temperature dependences of rise and fall times in a SiC CJFET inverter at $V_{dd}$ = 1.4 V. Open and closed symbols represent the experimental[18] and simulated results, respectively.

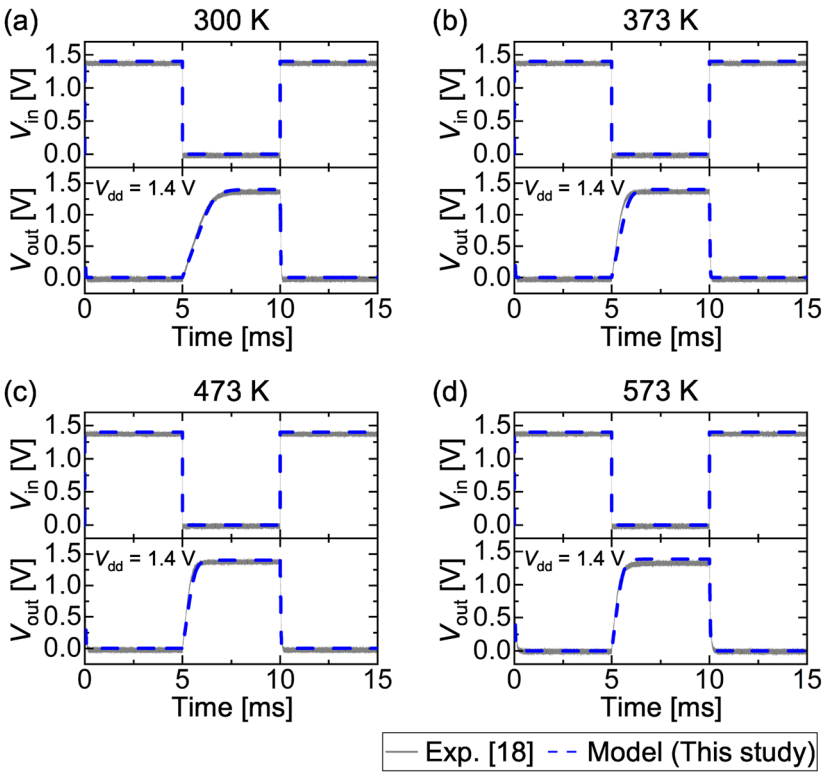


**FIG. 13.** (a)–(d) Dynamic characteristics of a SiC CJFET inverter at up to 573 K. Solid lines and dashed lines represent the experimental[18] and simulated results, respectively.

frequency is as low as a few kHz, which is attributed to the small transconductance of the fabricated JFET.[18]

The simulated results at elevated temperatures showed a slight difference from the experimental results. It is expected that the deviation can be minimized when the non-ideal leakage current is prevented. Since the non-ideal leakage current is likely due to the lower resistivity of the HPSI SiC substrate at high temperatures, the fabrication of SiC CJFET in a p- and n-well structure on an epitaxial layer like Si CMOS circuits (electrical isolation by p-n junctions) may be effective to reduce the leakage current, and the constructed device models are expected to show better agreement with the experimental results.

In this study, we have proposed a device model for SPICE simulations. As discussed in this paper, the proposed model successfully reproduces the experimental results for both single JFET and CJFET inverter circuit operations, demonstrating its applicability to logic circuit design. However, for analog circuit applications, a more precise model is required, which will be addressed in our future work.

## IV. CONCLUSION

The authors constructed a device model of SiC side-gate p- and n-JFETs and calculated the electrical characteristics of the SiC JFETs with the device model. The calculated and experimental results of $I_D$–$V_G$ characteristics agreed well over a wide temperature range from 300 to 573 K. The temperature dependences of the calculated *SS* well reproduced the experimental *SS* extracted from the $I_D$–$V_G$ characteristics. The results implied that the developed device model of both SiC p- and n-JFETs is valid at up to 573 K. The static characteristics of the SiC CJFET inverter were also calculated with the device model constructed in this study. The simulated $V_{lth}$ showed good agreement with the experimental results within the wide temperature range. The authors believe that the device model presented in this study is promising for the SiC CJFET circuit design and will lead to further development of the SiC CJFET circuits.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

**Noriyuki Maeda**: Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Visualization (lead); Writing – original draft (lead). **Mitsuaki Kaneko**: Conceptualization (lead); Funding acquisition (supporting); Project administration (lead); Resources (supporting); Supervision (lead); Validation (lead); Writing – original draft (supporting); Writing – review & editing (lead). **Hajime Tanaka**: Validation (equal); Writing – review & editing (lead). **Tsunenobu Kimoto**: Funding acquisition (lead); Project administration (supporting); Resources (lead); Supervision (equal); Writing – review & editing (supporting).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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