

1330 V, $67 \text{ m}\Omega \cdot \text{cm}^2$ 4H-SiC(0001) RESURF MOSFET

Tsunenobu Kimoto, Hiroaki Kawano, and Jun Suda

Abstract—Design and fabrication of 4H-SiC(0001) lateral MOSFETs with a two-zone reduced surface field structure have been investigated. The dose dependencies of experimental breakdown voltage show good agreement with simulation. Through the optimization of implant dose, high-temperature (1700 °C) annealing after ion implantation, and reduction of channel length, a breakdown voltage of 1330 V and a low on-resistance of $67 \text{ m}\Omega \cdot \text{cm}^2$ have been obtained. The figure-of-merit (V_B^2/R_{on}) of the present device reaches $26 \text{ MW}/\text{cm}^2$, being the best performance among lateral MOSFETs reported. The temperature dependence of static characteristics is also presented.

Index Terms—Power device, power MOSFET, reduced surface field (RESURF), silicon carbide (SiC).

OWING to the high critical electric field, silicon carbide (SiC) is a promising wide bandgap semiconductor for high-voltage power device applications [1]. Recent improvement in channel mobility of MOS interface has resulted in demonstration of vertical SiC MOSFETs which significantly outperform the Si counterparts [2]–[6]. Although lateral SiC power MOSFETs are more suited for future power IC applications, the performance of lateral SiC MOSFETs has still suffered from high on-resistance and relatively low breakdown voltage, compared to vertical SiC MOSFETs [7]–[10]. In this letter, simulation and fabrication of high-voltage SiC reduced surface field (RESURF) MOSFETs are investigated, leading to a record performance. The temperature dependence of static characteristics is also discussed.

Fig. 1 illustrates the schematic structure of a RESURF MOSFET fabricated in this letter. The structure is basically the same as the “two-zone” RESURF MOSFET [7]. Both the RESURF and lightly doped drain (LDD) regions were $10 \mu\text{m}$ long and $0.6 \mu\text{m}$ deep. RESURF MOSFETs were fabricated on $10 \mu\text{m}$ -thick p-type 8° off axis 4H-SiC(0001) epilayers doped to $7 \times 10^{15} \text{ cm}^{-3}$. The RESURF/LDD regions were formed by N^+ implantation at room temperature, while high-dose ($4 \times 10^{15} \text{ cm}^{-2}$) P^+ implantation at 300°C was employed to form source/drain. The p^+ -contact region was formed by Al^+ implantation. Post-implantation annealing was performed at 1700°C for 20 min in Ar with a carbon cap to suppress surface roughening [11]. After RCA cleaning, 70 nm -thick gate oxides were formed by direct oxidation in N_2O at 1300°C [12], [13]. The contact metal was Ti/Al annealed at 600°C for

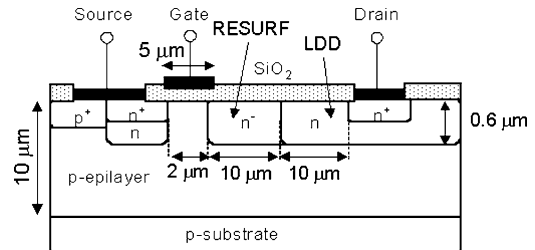


Fig. 1. Schematic structure of a SiC RESURF MOSFET fabricated in this letter.

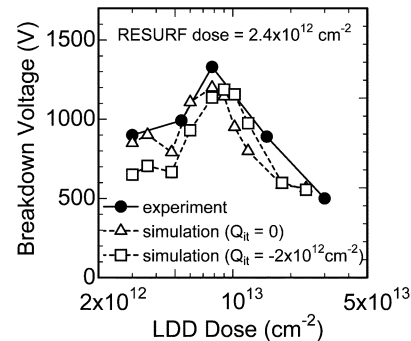


Fig. 2. LDD-dose dependencies of experimental and simulated breakdown voltages of 4H-SiC MOSFETs with a fixed RESURF dose of $2.4 \times 10^{12} \text{ cm}^{-2}$. The influence of MOS-interface charge ($Q_{\text{it}} = -2 \times 10^{12} \text{ cm}^{-2}$) is also simulated.

source/drain and Al for gate. The typical channel length and width were $2 \mu\text{m}$ and $200 \mu\text{m}$, respectively.

The RESURF and LDD doses were optimized to reduce the electric field crowding at the drain edge and in the gate oxide by using device simulation (ISE-DESSIS). The breakdown of devices (avalanche in SiC) was defined when the impact-ionization integral along an electric-force line reaches unity. The maximum electric field of oxide at the gate edge was also monitored.

Fig. 2 plots the LDD-dose dependencies of experimental and simulated breakdown voltages of 4H-SiC MOSFETs with a fixed RESURF dose of $2.4 \times 10^{12} \text{ cm}^{-2}$. The influence of MOS-interface charge is also simulated. The effective negative charge ($Q_{\text{it}} = -2 \times 10^{12} \text{ cm}^{-2}$) was assumed because of electron trapping at the oxide/n-type SiC interface. The simulated breakdown voltage is sensitive to the LDD dose, showing a maximum at a LDD dose of about $8 \times 10^{12} \text{ cm}^{-2}$. At this LDD dose, the fabricated MOSFET exhibited a maximum breakdown voltage as shown in Fig. 2. In the simulation, the avalanching point is located at the drain edge in the case of a low LDD dose, and at the RESURF/LDD interface for a high LDD dose. In the same manner, the RESURF-dose dependence of breakdown voltage was investigated. When the RESURF

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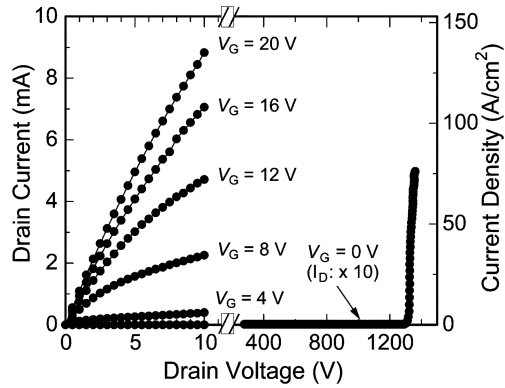


Fig. 3. Output characteristics of a fabricated 4H-SiC(0001) MOSFET with a RESURF dose of $2.4 \times 10^{12} \text{ cm}^{-2}$ and a LDD dose of $7.8 \times 10^{12} \text{ cm}^{-2}$.

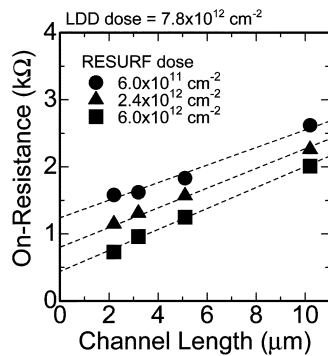


Fig. 4. Channel length dependence of on-resistance for 4H-SiC(0001) RESURF MOSFETs with various RESURF doses.

dose is too low, electric field crowding at the drain edge takes place, while oxide breakdown occurs when the RESURF dose is too high. The experimental breakdown voltage showed rather good agreement with simulated values.

Fig. 3 shows the output characteristics of a fabricated 4H-SiC MOSFET with a RESURF dose of $2.4 \times 10^{12} \text{ cm}^{-2}$ and a LDD dose of $7.8 \times 10^{12} \text{ cm}^{-2}$. The device exhibited a high breakdown voltage of 1330 V, and an on-resistance of $67 \text{ m}\Omega\text{cm}^2$ at an oxide field of 3.0 MV/cm . In the calculation of specific on-resistance, an active area of $6.4 \times 10^{-5} \text{ cm}^2$, including drain and source ($5 \mu\text{m}$ -long each), was assumed. The threshold voltage determined from the drain current—gate voltage characteristics in the linear region ($V_D = 0.1 \text{ V}$) was 2.6 V . The channel mobility was estimated to be $24 \text{ cm}^2/\text{Vs}$ from non-RESURF MOSFETs processed on the same substrate. The leakage current at zero-gate bias was very low, $8 \times 10^{-7} \text{ A/cm}^2$ at 1 kV . Stable and reversible breakdown was observed up to a relatively high avalanche current.

RESURF MOSFETs with different channel lengths were characterized to analyze the contribution of MOS-channel resistance. In general, the on-resistance of a MOSFET (R_{on}) at negligible drain voltage can be expressed by the following equation:

$$R_{\text{on}} = \frac{Ld_{\text{ox}}}{\{\mu_{\text{ch}}W\varepsilon_{\text{ox}}(V_G - V_T)\}} + R_{\text{drift}} + R_c \quad (1)$$

where the L is the channel length W the channel width, μ_{ch} the channel mobility, d_{ox} the oxide thickness, ε_{ox} the dielectric constant of gate oxide, V_G the gate voltage, V_T the threshold voltage, R_{drift} the resistance of drift region (RESURF and LDD

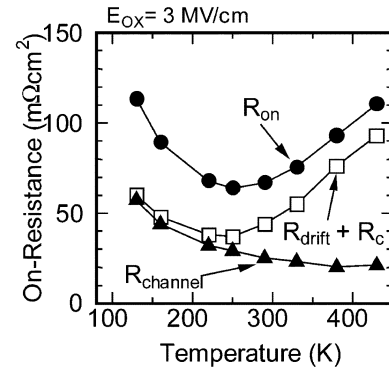


Fig. 5. Temperature dependence of total on-resistance and its components for the 4H-SiC(0001) RESURF MOSFET shown in Fig. 4.

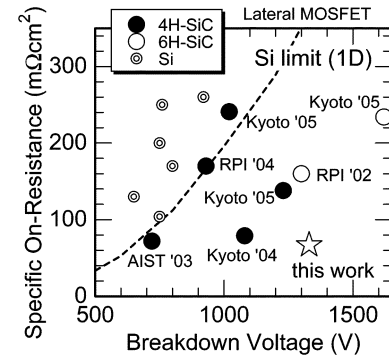


Fig. 6. On-resistance versus breakdown voltage for major lateral SiC MOSFETs reported in literature and this work, together with major lateral Si MOSFETs.

regions), and R_c the resistance of n^+ -contact regions including contact resistance. Fig. 4 represents the channel length dependence of on-resistance for 4H-SiC RESURF MOSFETs with various RESURF doses. In Fig. 4, the LDD dose was fixed, while the RESURF dose and channel length were varied. From the slope of the plots, the effective channel mobility could be estimated to be $20\text{--}25 \text{ cm}^2/\text{Vs}$. From the intercept at the ordinate, the sum of R_{drift} and R_c was determined to be 1240 , 770 , and 480Ω for a RESURF dose of $6.0 \times 10^{11} \text{ cm}^{-2}$, $2.4 \times 10^{12} \text{ cm}^{-2}$, and $6.0 \times 10^{12} \text{ cm}^{-2}$, respectively. These values are dominated by the resistance of RESURF region, because the RESURF dose is lower than the LDD dose. Since the contact resistance cannot be neglected (about $15\text{--}18\%$) in the present device, further reduction of on-resistance may be achieved by optimizing the annealing process of ohmic contacts.

The temperature dependencies of *measured* on-resistance and its components are shown in Fig. 5. The MOS-channel resistance showed significant decrease with increasing temperature, because electron trapping at the interface states is less pronounced at elevated temperature. The drift-region resistance becomes high at low temperature because of carrier freezing, and at high temperature due to decrease in bulk mobility. As a result, the total on-resistance of RESURF MOSFET showed a minimum at about room temperature.

Fig. 6 plots the on-resistance versus breakdown voltage for major lateral SiC MOSFETs reported in literature and this work, together with lateral Si MOSFETs. A classical limit of Si unipolar devices without super-junction structures is also shown by a dotted curve. The characteristics of the present

device (1330 V, 67 m $\Omega \cdot \text{cm}^2$) yielded a high figure-of-merit (V_B^2/R_{on}) of 26 MW/cm², being the best performance among lateral MOSFETs reported (3–10 MW/cm²) [7]–[10]. The optimization of LDD dose, high-temperature (1700 °C) annealing after ion implantation, and reduction of channel length were key issues to improve the performance.

In summary, the dose optimization and fabrication of 4H-SiC(0001) lateral MOSFETs with a two-zone RESURF structure have been investigated. The dose dependencies of experimental breakdown voltage showed good agreement with simulation. A breakdown voltage of 1330 V and a low on-resistance of 67 m $\Omega \cdot \text{cm}^2$ have been obtained. In this particular device, the contribution of MOS-channel resistance to the total on-resistance was approximately 40%.

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