Preliminary Experiments on Saturated DC Reactor Type Fault Current Limiter

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***Abstract*—Preliminary experiments have been performed on our proposed saturated DC reactor type superconducting fault current limiter (SFCL). The proposed SFCL is similar to a DC reactor type but an additional control winding is used. The DC bias current in the control winding saturates the core. The B–H curve of a magnetic circuit shows that low inductance value can be achieved in saturated region and high value in unsaturated region. The inductance of the saturated reactor depends on type of magnetic material, core size, number of turns and biasing conditions. The advantage of this type of SFCL over the existing DC reactor type is that, it shows low inductance value at normal operation and high value during fault time. On the other hand, the present DC reactor type SFCL shows a fixed value of inductance both in normal and fault time. In our experiment, we observed the inductance behavior of the saturated reactor by changing the control current. In order to make the work simple and convenient we have chosen a ferrite core. The experimental results are presented in this paper.**

***Index Terms*—Bridge type, fault current limiter, saturated dc reactor.**

I. Introduction

MANY CIRCUITS and topologies about superconducting fault current limiter (SFCL) are available today and some of them are well known as non-S/N transition type; for example [1]–[5] etc. A new DC reactor type superconducting fault current limiter (SFCL) has been proposed in a paper [6]. We described the details of the circuit and performed some simulation test of that type. Now we have carried out some preliminary experiments using copper wire instead of superconducting wire to check the principle of operation. However, superconductor can be used in the both coils to reduce volume and loss. Here a brief description is given about the circuit and its operational principle.

II. Circuit Description and Principle of Operation

The schematic diagram of the proposed SFCL is shown in Fig. 1. This type of SFCL is similar to the bridge type SFCL [2], [7] but a saturable DC iron-core reactor is used instead of air-core reactor. The saturable reactor consists of two windings; the main winding and a control winding. They are connected in such way so that the flux produced by both winding oppose each other. The main winding carries rectified line current and circulating current and the control winding carries DC bias current from an isolated source. In normal operation, feeding high DC bias current in the control winding the reactor is brought to saturation condition.

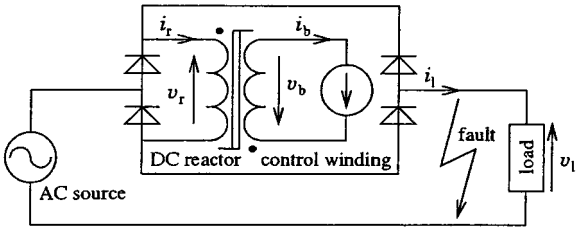

Fig. 1. Circuit diagram of proposed SFCL where i_r: reactor current, i_b: bias current, i_l: load current.

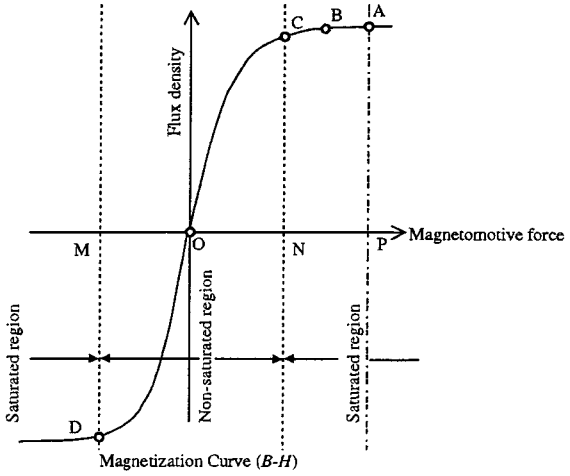

Fig. 2. Principle of operation of the proposed SFCL.

The inductance value depends on the saturation or nonsaturation condition of the core; a higher value in nonsaturated condition and a lower value in saturated condition. When the short circuit fault occurs, the source voltage appears across the inductor and inductor current starts increasing. So, depending on the reactor's condition the fault current rises at different rate; rapidly rises in saturated mode and slowly rises in nonsaturated mode of the reactor.

The ideal magnetizing B–H curve of a iron core is shown in Fig. 2. In the diagram, the curve COD represents unsaturated portion of the magnetizing curve. The width of this unsaturated region is MN in the horizontal direction. The DC bias current i_b in the control winding set the operating point at A in saturation region when no current flowing in the main coil (DC reactor). As the control winding and the reactor winding flux are opposing each other, it is possible to bring the operating point toward the

Manuscript received September 24, 2001. This work was supported in part by Kansai Electric Power Company Ltd.

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Publisher Item Identifier S 1051-8223(02)03844-7.

TABLE I
SPECIFICATION OF THE DC REACTOR

Core type	TDK PC30/T68-13.5-44
Main coil turns	75
Control coil turns	100
Main coil wire size	0.95 mm^2
Control coil wire size	0.196 mm^2
Main coil resistance	0.3 Ω
Control coil resistance	0.9 Ω
Inner diameter	44 mm
Outer diameter	70 mm
Cross sectional area	1.62 cm^2
Maximum flux density	510 mT
Non-saturated inductance	42 mH
Saturated inductance	0.2 mH

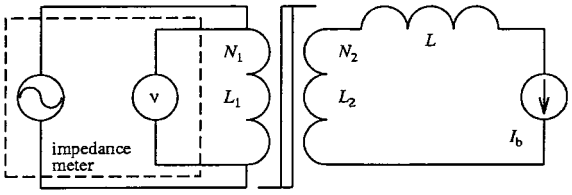

Fig. 3. Instrument setup in measuring inductance.

nonsaturated region by increasing the reactor current i_r. In this case the operating point moves to the PO direction through the path ABCO.

In normal operation, the reactor coil carries normal line current. The combined effect of reactor current i_r and bias current i_b keeps the operating point at B in the saturation region. The reactor shows low inductance in this region which is required in normal condition. When fault occurs, the fault current brings the core to the unsaturation region moving the operating point through the BCOD path. The high inductance value in BOCD path limits the fault current. As the fault current continues to increase, after certain interval the operating point shifts beyond the boundary of MD line and the core again goes to the saturation region. Therefore, the unsaturated width MN is the current limiting region and it is used to limit the fault current. In the saturation region beyond the MD line and the fault current again increases rapidly as it is also a low inductance region. This region can be used to determine the maximum current limiting capacity of the SFCL.

III. PREPARED SATURATED DC REACTOR

To carry out a simplest possible experiment we have chosen a readily available ferrite core instead of a iron core to make the DC reactor. The specification of DC reactor is described in Table I.

A troidal ferrite core is used in the DC reactor. The main coil that carries rectified load current has 75 turns and the control coil that is fed by the DC bias current contains 100 turns. The inductance measuring instrument setup is shown in Fig. 3. We observed the relationship between the inductance of main coil L_1 and the control (biasing) current I_b. A high value of known inductor ($L = 13.4$ H) is connected in series with the control circuit in order to reduce the measurement error. This inductor is a special kind of superconductor magnet of type SMU80511Q10.

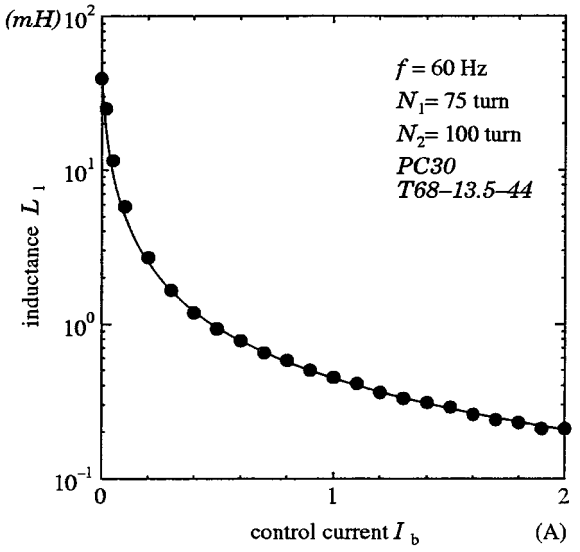

Fig. 4. Inductance at different control current.

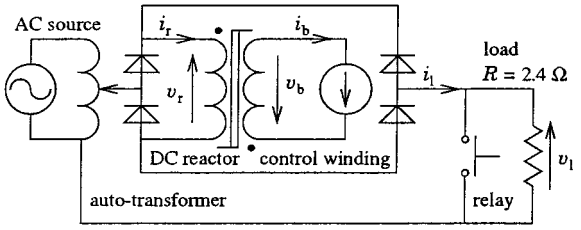

Fig. 5. Experimental setup diagram.

The reactor inductance was monitored at every 0.1 A step increment of the control current. The measured inductance L_1 is plotted in Fig. 4 by varying the control current I_b. The value was measured by impedance meter (HIOKI 3530 LCR Hi TESTER) up to 2 ampere of control current where its value is approximately 0.2 mH. On the other hand, at zero control current the nonsaturated inductance value was measured 42 mH. By using a curve fitting technique we found a relationship between reactor inductance L_1 and its control current I_b as follows:

$$L_1 = \left\{ \frac{0.446}{(I_b/\mathrm{A} + 0.018)^{1.136}} + 6.6 \times 10^{-3} \right\} \text{ mH}. \quad (1)$$

In the equation L_1 represents the reactor inductance measured from the main winding side and the I_b represents the DC control current in ampere. Using this equation we determined the inductance of the reactor while performing different tests at various control current.

IV. EXPERIMENT SETUP

The experimental circuit is shown in Fig. 5. Input voltage is taken from a autotransformer and a separate DC current source is connected to the control winding for supplying DC bias current. The model FCL is connected in series with a resistive type load and set the load value to 2.4 Ω. For making a fault, an electromagnetic relay is used instead of solid-state relay. This is because the solid state relay has some forward voltage drop. So, making a short-circuit test using that relay is not suitable in our small scale test arrangements. The relay is connected across the

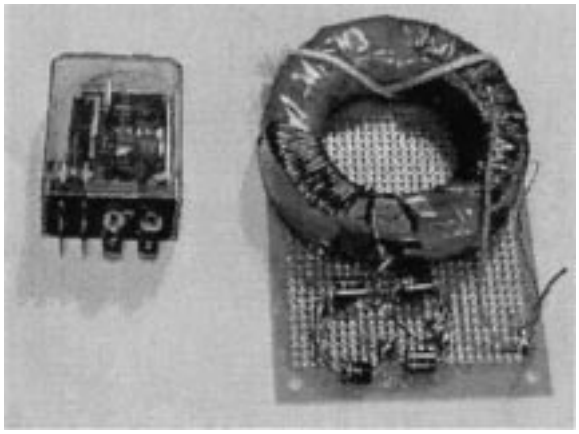

Fig. 6. Photograph of FCL using ferrite core and electromagnetic switch.

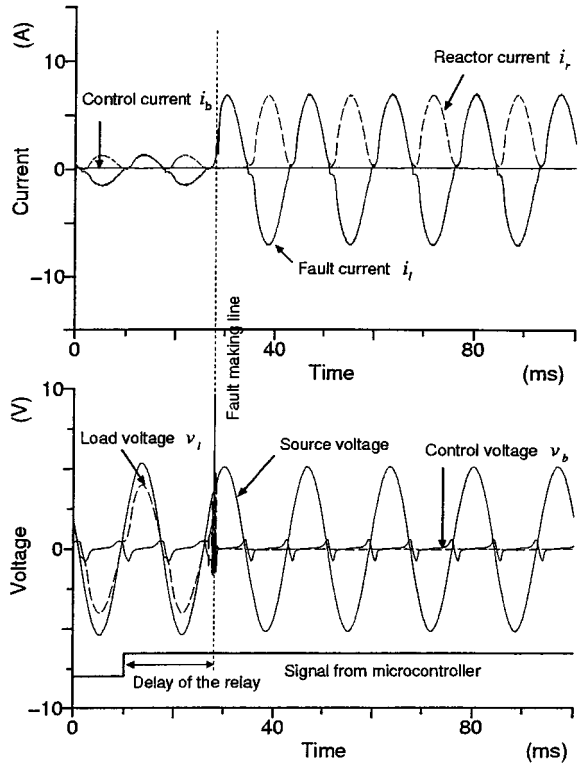

Fig. 7. Test results without using DC bias current in control coil. There is no clear indication of limiting fault current in the current waveforms.

load terminal to make an artificial fault. It is controlled using programmable signals from a micro-controller. Electromagnetic relay can not response instantly, so, certain time delay occurs between getting the signal and closing the contact of the relay. The photograph of the fabricated saturable DC reactor using ferrite core with Schottky diode (3WGJ) bridge and the electromagnetic relay used in this experiment is shown in Fig. 6. The control current is set to a suitable value (here it is 1.5 A) to maintain the operating point in saturation region. We monitored load current $i_{\rm l}$, load voltage $v_{\rm l}$, source voltage $v_{\rm s}$, reactor current $i_{\rm r}$, reactor voltage $v_{\rm r}$, control current $i_{\rm b}$ and control voltage $v_{\rm b}$ during short-circuit tests.

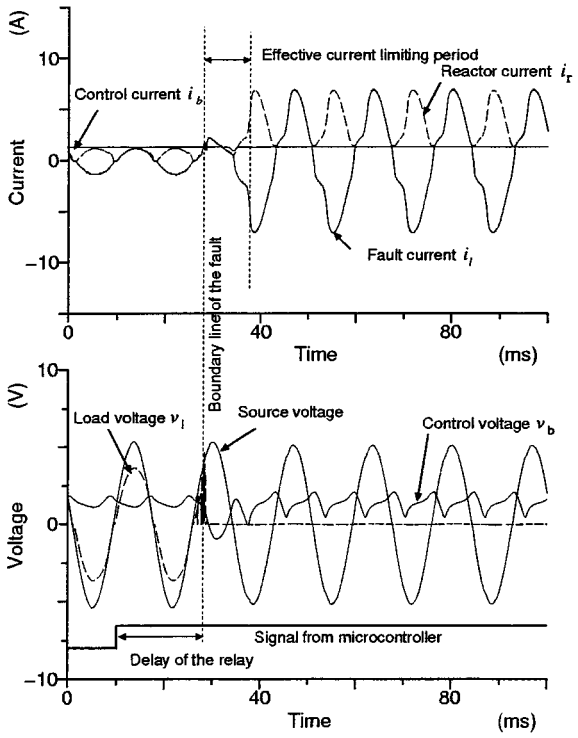

Fig. 8. Test results at 1.5 A DC bias current in control coil. Clear current limiting period is seen in the fault current waveform.

V. Experiment Results and Discussion

We carried out some experiments with this FCL and discussed the results below. Some tests are performed at different bias current $i_{\rm b}$ in the control coil to observe the limiting performance and only few of them are shown here. During test the source voltage and load current are selected as $V_{\rm s} = 3.5$ V and $I_{\rm l} = 1.5$ A respectively. The fault current with and without connecting FCL is also observed.

In Fig. 7 the output waveforms are obtained without using any control current ($I_{\rm b} = 0$ A). The upper curves represent the current waveforms of load, main coil and control coil and the lower curves represent the voltage waveforms of source, load and control coil. The fault making control signal from micro-controller is shown below of the voltage waveforms. In electromagnetic relay, some time difference occurs between getting signal and making contact. This delay of the relay is clearly shown in the control signal. If we see at the instant of fault making time we found no effective current limiting condition on the current waveforms. This is because the main coil that carries rectified load current can easily make the core saturated at the absence of control current (operating point moves outside the MD line in Fig. 2). At saturated condition the inductance value of the coil shows less than 0.3 mH. This small inductance has small effect on the fault current. So, we could not see any clear current limiting mode at this condition. On the other hand, in Fig. 8 when control current $I_{\rm b} = 1.5$ A is fed in the control winding we observed a different situation. A clear current limiting period occurs on the current waveforms after the fault. In this case, at normal operation the control current keeps the reactor in saturated condition (operating point is at B in Fig. 2). This is happened because the ampere-turn in control winding is higher than

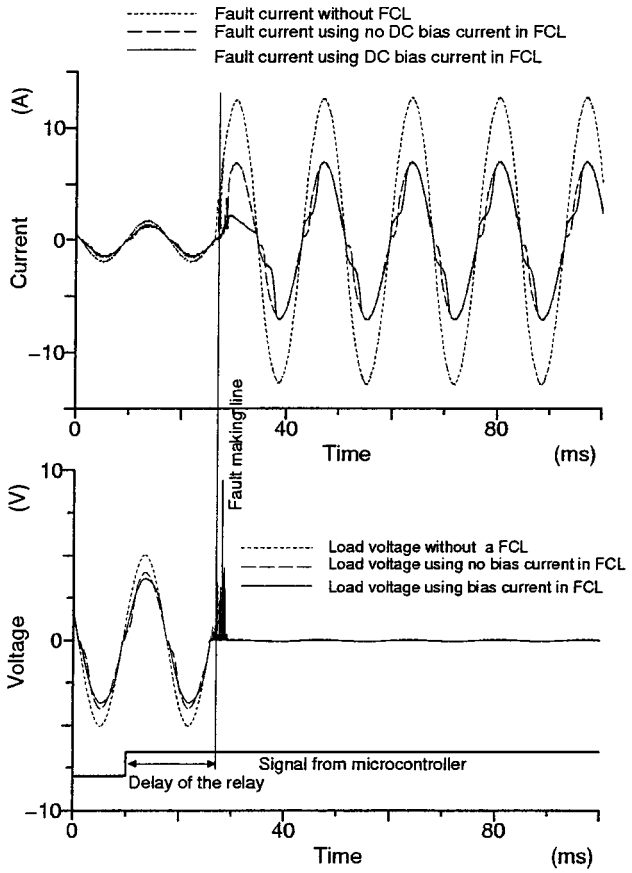

Fig. 9. Test results with/without using FCL. The upper curves represent the fault current waveforms and the lower curves represent the load voltage waveforms. These tests are performed at different conditions but with same fault reference signal.

that of the main winding. At the time of fault, the higher fault current overcome the value of control winding ampere-turn and brings the reactor in nonsaturated condition. In the waveform it is shown that the FCL limits the fault current for 10 ms.

In Fig. 9 both current and voltage waveforms are shown at different biasing conditions of the control coil during fault time. We have shown two tests results with FCL (using control current and without using control current) and one test results without connecting FCL taking the same fault event signal. In the waveforms the solid line of the upper plot limits the fault current for 10 ms at 1.5 A DC control current. Without using DC control current the system does not limit current like that. Without connecting the FCL to the system, the fault current goes to higher values compared to other two. In the plot, the dotted curve represent that waveform. Under such condition, only the system impedance can limit the fault current. In the lower part of the figure, all curves represents the voltage waveforms of the three different tests. Fault is made by short-circuiting the load terminal, so after fault, the load terminal voltage goes to zero that is clearly shown in the figure. When FCL is not connected to the circuit the load voltage amplitude shows a higher value compared to the amplitudes of other two waveforms. The reason is, the FCL itself has some impedance. This impedance is connected in series to the load and some voltage drop occurs across it.

VI. Conclusion

The preliminary experiments of saturated DC reactor type FCL were performed and the output results have been observed. The effect of the control current on limiting of the fault current has been clearly observed which was the main objective of this experiment. Although the experiment was carried out using a small ferrite core at very low voltage and current which is far beyond the capacity of a practical FCL, it was confirmed that the system worked in current limiting mode based on the principle. More research and developing efforts are required to build and test higher capacity FCL of this type in order to find out the feasibility for practical use.

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