Title

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Kyoto University
Effects of Wet Oxidation/Anneal on Interface Properties of Thermally Oxidized SiO₂/SiC MOS System and MOSFET’s

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Abstract—Effects of wet atmosphere during oxidation and anneal on thermally oxidized p-type and n-type MOS interface properties were systematically investigated for both 4H- and 6H-SiC. Deep interface states and fixed oxide charges were mainly discussed. The wet atmosphere was effective to reduce a negative flatband shift caused by deep donor-type interface states in p-type SiC MOS capacitors. Negative fixed charges, however, appeared near the interface during wet reoxidation anneal. In n-type SiC MOS capacitors, the flatband shift indicated a positive value when using wet atmosphere. The relation between interface properties and characteristics of n-channel planar 6H-SiC metal-oxide-semiconductor field effect transistors (MOSFET’s) was also investigated. There was little relation between the interface properties of p-type MOS capacitors and the channel mobility of MOSFET’s. The threshold voltage of MOSFET’s processed by wet reoxidation anneal was higher than that of without reoxidation anneal. A clear relation between the threshold voltage and the channel mobility was observed in MOSFET’s fabricated on the same substrate.

Index Terms—Deep interface states, fixed oxide charges, interface, MOS, MOSFET’s, reoxidation anneal, silicon carbide, wet oxidation.

I. INTRODUCTION

SI LICON CARBIDE (SiC) is a promising semiconductor for high-power, high-temperature, and high-frequency devices because of its superior properties such as wide bandgap, high breakdown field, high saturation electron drift velocity, and high thermal conductivity. For the aspect of device processes, SiC has an advantage of both n- and p-type conduction in a wide range by either in situ doping [1], [2] or selective ion implantation [3], [4]. One of the most important advantages of SiC over other wide bandgap semiconductors is that SiC can be thermally oxidized to form high-quality SiO₂ like Si : metal-oxide-semiconductor field effect transistors (MOSFET’s) can be made on SiC.

Nowadays, SiC MOSFET’s have been intensively investigated by many groups [5]–[8]. However, their excellent characteristics expected from SiC properties have not been achieved yet, mainly due to inferior SiO₂/SiC interface properties. While rather good characteristics are obtained on the SiO₂/n-SiC interface [9], [10], the SiO₂/p-SiC interface has a large amount of fixed charges and large interface state density [11], [12]. In recent years, wet oxidation [13] or wet reoxidation anneal [14] at low temperatures was reported to reduce the interface state density of p-type MOS capacitors. They did little discuss, however, on the effects of oxidation or anneal ambient on deep states and fixed charges near the interface. In addition, there have been few reports on the effects of oxidation or anneal ambient on SiO₂/n-SiC interface properties.

In this paper, we report systematic investigation on the effects of wet oxidation and reoxidation anneal in wet O₂ at low temperatures on the interface properties (deep interface states and fixed charges) of SiO₂/p-SiC and SiO₂/n-SiC, for both 4H and 6H polytypes. We also investigated on the relation between the interface properties and characteristics of n-channel planar 6H-SiC MOSFET’s.

II. EXPERIMENTS

MOS capacitors were fabricated on homo-epilayers grown on a (0001) Si-face of both 4H- and 6H-SiC. B-doped p-epilayers and N-doped n-epilayers were grown on highly doped p-type and n-type substrates, respectively. The epilayer thickness was 4 μm. The impurity concentrations of epilayers evaluated from Schottky characteristics were 2 × 10¹⁶ cm⁻³ for p-type and 2 × 10¹⁵ cm⁻³ for n-type. In this experiment, B-doped epilayers were used for p-type samples because the controllability of low doping level for B-doped epilayers is better than Al-doped epilayers in our CVD system. However, there is no essential difference in SiO₂/SiC interface properties between B-doped and Al-doped samples according to previous reports [15], [16].

Before thermal oxidation, the samples were cleaned by RCA cleaning followed by 0.5% HF dip. Thermal oxidation was carried out at 1150 °C in dry O₂ for 3 h or in wet O₂ (bubbling O₂ through deionized water at 95 °C) for 2 h followed by post-oxidation anneal at 1150 °C in Ar for 30 min. The oxide thicknesses determined from accumulation in high-frequency capacitance–voltage (C–V) curve were 350–400 Å for dry oxidation and 300–350 Å for wet oxidation. For some samples, reoxidation anneal [14] was carried out at 950 °C for 3 h in wet O₂ after Ar anneal, and in cooling off in Ar ambient, the
ramp rate was 3 °C/min. The samples were pulled out at room temperature. As a gate electrode, Al was evaporated through a metal mask to form circular (300, 500 μm in diameter) patterns. After forming the gate electrode, post-metallization anneal (PMA) was performed in a forming gas (N₂ : H₂ = 9 : 1) at 400 °C for 30 min.

N-channel planar MOSFET’s were fabricated on p-type 6H-SiC epilayers using a non self-aligned process. The source and drain regions were formed using multiple N⁺ ion implantations with a total dose of 5 × 10¹⁴ cm⁻². Post-implantation anneal was carried out at 1500 °C for 30 min in Ar. The gate oxidation was carried out in the same manner as the fabrication of MOS capacitors above mentioned. The channel length (L) was either 10 or 30 μm, and the channel width (W) was 200 μm. Ohmic contacts for source and drain regions were Al without an alloy process. After forming the Al gate electrode, PMA was performed.

The SiO₂/SiC interface properties were characterized by high-frequency C–V measurements of MOS capacitors at room temperature under the dark condition and after light illumination at deep depletion. The high-frequency C–V characteristics were measured with a probing frequency of 100 kHz and a bias sweep rate of 0.1 V/s. The total deep interface states and fixed charges were estimated from a ledge feature caused by deep interface states and a flatband voltage shift. The SiO₂/SiC interface properties were also characterized by MOSFET parameters such as the channel mobility and threshold voltage at room temperature.

III. RESULTS AND DISCUSSION

A. SiO₂/p-SiC Interface Properties

Fig. 1 shows typical high-frequency C–V curves under the dark condition for p-type 4H-SiC MOS capacitors fabricated by different oxidation processes. The measured curves show deep depletion because of the extremely low intrinsic carrier concentration due to the wide bandgap. Although a large negative flatband shift (ΔV₅₀) was observed for the dry oxidation samples, wet oxidation can reduce ΔV₅₀. Furthermore, the wet reoxidation anneal can reduce ΔV₅₀ to less than −1.0 V. The reoxidation anneal was also useful even after dry oxidation to reduce ΔV₅₀ to the same value as after wet oxidation. This indicates that the interface properties of MOS capacitors processed by wet reoxidation anneal at a low temperature do not depend on the oxidation gas.

The large negative ΔV₅₀ in p-type MOS capacitors is mainly caused by holes trapped at deep donor-type interface states, and not by fixed charges [17]. If negative fixed charges exist near the interface, however, the flatband shift can be reduced. Deep interface states and fixed charges were tried to be separated for MOS capacitors processed by wet oxidation and wet reoxidation anneal as well as a dry-oxidized MOS capacitor using high-frequency C–V characteristics after light illumination.

Fig. 2 shows a high-frequency C–V curve for a dry-oxidized p-type 4H-SiC MOS capacitor measured after light illumination at deep depletion. A tungsten lamp with a power of 120 W was used as the light source for illumination. The MOS capacitor was illuminated for more than 1 min to form an inversion layer at a bias of 10 V. After the illumination was turned off, the bias was swept in the sequence of A→B→C→D→E→F. When the inversion layer is formed by the illumination, the deep interface states capturing holes start to capture electrons and change the charge state to neutral, since the deep interface states are donor-type. At point C, the C–V curve shows a so-called “interface state ledge” [18] that appears when the deep states exist at the interface. At point D, holes accumulate near the interface and all deep interface states capture these holes. Once holes are captured at the deep interface states, they can not be thermally emitted to the valence band at room temperature. So, in the region of D→E→F, the charge state of the deep interface states is positive. The voltage shift between the region of B→C and that of E→F is caused by the difference of the charge states of the deep interface states. From this voltage shift (ΔV₁₀), the total deep interface state density per unit area (N₁₀) is obtained by

\[
N_{₁₀} = \frac{C_{ᵥ_{ds}} |ΔV_{₁₀}|}{q},
\]
Fig. 3. High-frequency $C-V$ curve of wet-oxidized p-type 4H-SiC MOS capacitor measured after light illumination.

Here, $C_{ox}$ is the capacitance of the gate oxide and $q$ the electronic charge. Fig. 2 indicates a $\Delta V_{fb}$ of $-13.5$ V, and the total deep interface state density $N_{is}$ is estimated to be $6.0 \times 10^{12}$ cm$^{-2}$ by (1). The flatband shift from the theoretical curve is caused by both holes trapped at the deep interface states and fixed charges. The subtraction of $\Delta V_{fb}$ gives the voltage shift caused by only the fixed charges. Then the fixed charge density is given by

$$Q_{fc} = \frac{C_{ox}(\Delta V_{fb} - \Delta V_{fb}^{theory})}{q},$$

In this dry-oxidized sample, the flatband shift was $\Delta V_{fb} = -16.0$ V. From these results, the fixed charge density $Q_{fc}$ was estimated to be $1.1 \times 10^{12}$ cm$^{-2}$ by (2). $Q_{fc}$ may include not only fixed charges but also other charges such as mobile ions and charged border traps besides deep interface states.

The small $\Delta V_{fb}$ of a wet-oxidized MOS capacitor in Fig. 1 could be realized by increase of negative fixed charges. Fig. 3 shows a high-frequency $C-V$ curve of a wet-oxidized p-type 4H-SiC MOS capacitor. The point C indicating an "interface state ledge" is located near the negative side of the theoretical curve. If negative fixed charges exist near the interface, the ledge can be located at the positive side of the theoretical curve. Therefore, the increase of negative fixed charges was negligible or a few during the wet oxidation with a large reduction of $N_{is}$. In this sample, $\Delta V_{fb}$ of $-4.2$ V and $\Delta V_{ds}$ of $-3.2$ V lead to $N_{is}$ of $1.9 \times 10^{12}$ cm$^{-2}$ and the significant reduction of $N_{is}$ contributes to the decrease of the negative large $\Delta V_{fb}$, while the small reduction of $Q_{fc}$ observed in the wet-oxidized sample compared with the dry-oxidized sample also contributes. The variation of fixed charges among samples might be caused by impurity contamination during Al evaporation. The same measurements were performed for p-type 6H-SiC using both dry- and wet-oxidized samples, and the results were similar to those of 4H-SiC.

Fig. 4 shows high-frequency $C-V$ curves after light illumination for p-type MOS capacitors processed by wet oxidation with wet reoxidation anneal. The results for the sample processed by dry oxidation with wet reoxidation anneal were similar. A ledge (point C) was observed for 4H-SiC as in Fig. 4(a), which is located at the positive bias compared with the theoretical curve. This results indicate the appearance of negative charges near/at the interface by wet reoxidation anneal. From the flatband shift and the hysteresis of the ledge feature, the negative fixed charges and total deep state density were estimated to be $-1.4 \times 10^{12}$ cm$^{-2}$ and $2.0 \times 10^{12}$ cm$^{-2}$, respectively. Deep acceptor-type interface states appear, and in this case, negative fixed charges are caused by both “real” negative fixed charges and electrons captured at the deep acceptor-type interface states. Thus, the small flatband shift in wet reoxidation annealed 4H-SiC is considered to be caused by cancel out of both positive charges by trapped holes and the negative charges, though it is difficult to separate these two effects.

For wet reoxidation annealed p-type 6H-SiC, the ledge feature is not clear compared with 4H-SiC as in Fig. 4(a), but, it is actually observed at a bias of $-1$ V as in Fig. 4(b). So, there might exist negative charges near/at the interface of p-type 6H-SiC.

The interface properties of p-type MOS capacitors for 4H- and 6H-SiC fabricated by dry/wet oxidation and with/without wet reoxidation anneal at a low temperature are summarized in Table I. As mentioned above, the wet oxidation is effective to improve the interface properties of p-type MOS capacitors. The improvement of interface properties by wet oxidation may be attributed to the elimination of unwanted carbon compounds. Thus, the investigation of carbon at the interface is necessary to clarify the effect of wet oxidation. Another effect of wet oxidation might be the passivation of dangling bonds at the interface by hydrogen. The wet reoxidation anneal at a low temperature (950 °C) can reduce the flatband shift. However, negative fixed charges appear in the oxide near the interface. The origin of negative fixed charges might be OH$^-$, which can not diffuse out from the interface at 950 °C, but it is not fully understood yet.

### Table I

<table>
<thead>
<tr>
<th>Oxidation / Anneal</th>
<th>$\Delta V_{fb}$ (V)</th>
<th>$Q_{eff}$ ($\times 10^{11}$ cm$^{-2}$)</th>
<th>$N_{is}$ ($\times 10^{11}$ cm$^{-2}$)</th>
<th>$Q_{fc}$ ($\times 10^{11}$ cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>dry/Ar</td>
<td>-16.0</td>
<td>71</td>
<td>60</td>
<td>11</td>
</tr>
<tr>
<td>wet/Ar</td>
<td>-4.2</td>
<td>25</td>
<td>19</td>
<td>6</td>
</tr>
<tr>
<td>dry/wet re-ox.</td>
<td>-1.1</td>
<td>6</td>
<td>18</td>
<td>-12</td>
</tr>
<tr>
<td>wet/wet re-ox.</td>
<td>-1.0</td>
<td>7</td>
<td>20</td>
<td>-13</td>
</tr>
</tbody>
</table>

(a) p-4H MOS

<table>
<thead>
<tr>
<th>Oxidation / Anneal</th>
<th>$\Delta V_{fb}$ (V)</th>
<th>$Q_{eff}$ ($\times 10^{11}$ cm$^{-2}$)</th>
<th>$N_{is}$ ($\times 10^{11}$ cm$^{-2}$)</th>
<th>$Q_{fc}$ ($\times 10^{11}$ cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>dry/Ar</td>
<td>-15.1</td>
<td>72</td>
<td>55</td>
<td>17</td>
</tr>
<tr>
<td>wet/Ar</td>
<td>-2.9</td>
<td>18</td>
<td>14</td>
<td>4</td>
</tr>
<tr>
<td>dry/wet re-ox.</td>
<td>-0.6</td>
<td>6</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>wet/wet re-ox.</td>
<td>-0.7</td>
<td>6</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

(b) p-6H MOS

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**B. SiO$_2$/n-SiC Interface Properties**

Fig. 5 shows typical high-frequency $C-V$ curves of n-type 4H-SiC MOS capacitors under the dark condition. The wet-oxidized sample has more positive flatband shift than the
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Fig. 4. High-frequency $C-V$ curve of wet reoxidation annealed p-type MOS capacitors measured after light illumination: (a) 4H-SiC MOS and (b) 6H-SiC MOS.

Fig. 5. High-frequency $C-V$ curves of n-type 4H-SiC MOS capacitors under the dark condition.

Fig. 6. High-frequency $C-V$ curve of dry-oxidized n-type 4H-SiC MOS capacitor after light illumination.

dry-oxidized sample. Still more, the flatband shift of the wet reoxidation annealed sample is more positive than that of samples without wet reoxidation anneal. When wet reoxidation anneal is done, the flatband shift takes almost the same value regardless of the oxidation ambient. The tendency is similar to that of p-type MOS capacitors.

Figs. 6 and 7 show high-frequency $C-V$ curves after light illumination for n-type 4H-SiC MOS capacitors processed by dry and wet oxidation, respectively. For the dry-oxidized n-type sample, the ledge feature can not be seen as in Fig. 6, which means that there are few deep states at the SiO$_2$/SiC interface. So, the flatband shift to the negative side for the dry-oxidized sample is mainly caused by real positive fixed charges. For the wet-oxidized n-type sample, on the other hand, the ledge feature can be seen at a bias of about $-4$ V as in Fig. 7, which means that deep acceptor-type interface states are formed by wet oxidation. It is difficult, however, to evaluate the deep interface states quantitatively because of dull ledge shape. Thus, only the flatband shift and effective fixed charges of both 4H- and 6H-SiC n-type MOS capacitors are given in Table II. These deep acceptor-type interface states capture electrons, and then, the charge state becomes negative. They may become one of the causes of the small positive flatband shift as in Fig. 5. Another cause of the positive flatband shift is negative fixed charges. For wet-oxidized p-type MOS capacitors, the reduction of positive fixed charges of mid-$10^{14}$ cm$^{-2}$ was obtained as in Fig. 3. If this reduction is caused by the increase of negative fixed charges, it is possible to increase negative fixed charges in n-type MOS capacitors by wet oxidation. Similar measurements were done for wet reoxidation annealed n-type samples, and the ledge feature could also be seen (not shown). Thus, the positive flatband shift shown in Fig. 5 is caused by both deep acceptor-type interface states and negative fixed charges. The same measurements were performed for n-type 6H-SiC processed by dry/wet oxidation and with/without wet reoxidation anneal, and the results were similar to those of 4H-SiC.

C. Relation Between Interface Properties and Characteristics of n-channel 6H-SiC MOSFET’s

To investigate the relation between interface properties and characteristics of MOSFET’s, 6H-SiC MOSFET’s were fabricated using dry/wet oxidation and with/without wet reoxidation anneal. After all processes for fabrication of MOSFET’s were done, the interface properties of MOS capacitors on the same chip of MOSFET’s were confirmed to be the same as mentioned in Section III-A. The bias of both source and substrate was zero in the measurement of current–voltage characteristics.
Typical drain current ($I_D$)-voltage ($V_D$) characteristics of 6H-SiC MOSFET’s for different gate voltage ($V_G$)’s are shown in Fig. 8, which have good saturation and enhancement-mode characteristics. Other MOSFET’s also showed good characteristics similar to Fig. 8. The channel mobility ($\mu_c$) was determined from the linear region at low drain voltage in Fig. 8. Fig. 9 shows the channel mobility as a function of ($V_G - V_T$), where $V_T$ is the threshold voltage. A maximum $\mu_c$ of 53.0 cm$^2$/Vs was obtained for dry-oxidized and wet reoxidation annealed 6H-SiC MOSFET’s, which is the best data at present in our experiments.

Fig. 10 shows typical $I_{DSS/2}-V_G$ characteristics of n-channel 6H-SiC MOSFET’s. In the case of the existence of fixed oxide charges, the threshold voltage is given by

$$V_T = V_{T(\text{theory})} - \frac{Q_{\text{fix}}}{C_{\text{ox}}}.$$  

Here, $V_{T(\text{theory})}$ is the theoretical threshold voltage, and $Q_{\text{fix}}$ the net fixed charge density, which means the sum of both positive and negative fixed charges. The MOSFET parameters such as $\mu_c$ and $V_T$ as well as $Q_{\text{fix}}$ for various interface properties are summarized in Table III: average of some (15–20) samples arbitrarily selected from one chip. From Table III, the followings are notified. First, the large negative flatband shift in MOS capacitors mainly caused by deep donor-type interface states has no relation with the threshold voltage of MOSFET’s, because deep donor-type interface states can capture electrons in the inversion layer to be neutral. Second, deep donor-type interface states do not affect the channel mobility, which can be explained in the same reason above mentioned. Third, the threshold voltage of wet reoxidation annealed MOSFET’s was higher than that of without reoxidation anneal. This indicates that negative charges appear near the interface by wet reoxidation anneal, that are the same results of the appearance of negative charges in MOS capacitors described in Section III-A.
The relation between the interface properties and characteristics of n-channel planar 6H-SiC MOSFET’s were also investigated. The large negative flatband shift caused by deep donor-type interface states has no relation with the threshold voltage and the channel mobility of MOSFET’s. On the contrary, there was a clear relation between the threshold voltage and the channel mobility in MOSFET’s fabricated on the same substrate. The threshold voltage of wet reoxidation annealed MOSFET’s was higher than that of without reoxidation anneal due to the negative fixed charges near the interface.

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REFERENCES


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Tsunenobu Kimoto, for photograph and biography, see this issue, p. 477.

Hiroyuki Matsunami (M’84) for a photograph and biography, see this issue, p. 477.