Design and Fabrication of RESURF MOSFETs on 4H-SiC(0001), $(11\bar{2}0)$, and 6H-SiC(0001)

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***Abstract*—Design and fabrication of lateral SiC reduced surface field (RESURF) MOSFETs have been investigated. The doping concentration (dose) of the RESURF and lightly doped drain regions has been optimized to reduce the electric field crowding at the drain edge or in the gate oxide by using device simulation. The optimum oxidation condition depends on the polytype: N_2O oxidation at 1300 °C seems to be suitable for 4H-SiC, and dry O_2 oxidation at 1250 °C for 6H-SiC. The average inversion-channel mobility is 22, 78, and 68 cm^2/Vs for 4H-SiC(0001), $(11\bar{2}0)$, and 6H-SiC(0001) MOSFETs, respectively. RESURF MOSFETs have been fabricated on 10-μm-thick p-type 4H-SiC(0001), $(11\bar{2}0)$, and 6H-SiC(0001) epilayers with an acceptor concentration of 1×10^{16} cm^{-3}. A 6H-SiC(0001) RESURF MOSFET with a 3-μm channel length exhibits a high breakdown voltage of 1620 V and an on-resistance of 234 $m\Omega \cdot cm^2$. A 4H–SiC$(11\bar{2}0)$ RESURF MOSFET shows the characteristics of 1230 V–138 $m\Omega \cdot cm^2$.**

***Index Terms*—Power device, power MOSFET, reduced surface field (RESURF), silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) has attracted increasing attention as a promising wide bandgap semiconductor projected for high-power devices [1], owing to its high electric breakdown field, high thermal conductivity, and reasonable maturity of crystals. Through recent progress in SiC device technology, high-voltage (300–1200 V) Schottky-barrier diodes have been commercially available [2]. In order to enjoy the full benefits of SiC-based power electronic systems such as high-voltage, low-loss, and high switching speed, SiC power switches are strongly required. In particular, SiC power metal-oxide-semiconductor field effect transistors (MOSFETs) have been recognized as an ideal power switch for a variety of voltage ranges, at least below 3 kV. Several groups have demonstrated vertical SiC power MOSFETs, which outperform the Si counterparts [3]–[7]. On the other hand, lateral SiC power MOSFETs are promising for high-voltage power integrated circuit (IC) applications in the future. Although several high-voltage lateral SiC MOSFETs have been reported [8]–[10], both the on-resistance and breakdown voltage have not reached the level achieved in vertical SiC MOSFETs.

In this paper, the design issues and fabrication of lateral SiC reduced surface field (RESURF) MOSFETs are investigated. MOSFETs have been processed on 4H-SiC(0001), 4H-SiC$(11\bar{2}0)$, and 6H-SiC(0001) substrates. An improvement of effective channel mobility has been also tried by high-temperature oxidation in O_2 or N_2O. High breakdown voltages (1020–1620 V) are realized in fabricated devices.

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TABLE I
AVERAGE EFFECTIVE MOBILITY (cm^2/Vs) FOR 4H-SiC(0001), $(11\bar{2}0)$, AND 6H-SiC(0001) MOSFETs. THE ACCEPTOR CONCENTRATION OF P-TYPE EPILAYERS IS ABOUT 1×10^{16} cm^{-3}

Substrate	Oxidation condition			
	wet O_2, 1150°C	dry O_2, 1250°C	dry O_2, 1300°C	N_2O, 1300°C
4H-SiC(0001)	8.2	4.1	3.9	22
4H-SiC$(11\bar{2}0)$	22	2.0	0.11	78
6H-SiC(0001)	36	68	37	39

II. Increase of Effective Channel Mobility by High-Temperature Oxidation

The performance of SiC power MOSFETs is generally limited by a high channel resistance, or a low effective channel mobility. Okuno *et al.* reported that the interface state density for 4H-SiC(0001) MOS structures is reduced by increasing the oxidation temperature to 1250 °C [11]. On the other hand, post-oxidation annealing or direct oxidation in NO has been recognized as an effective process to improve the quality of 4H-SiC(0001) MOS interface [12]. More recently, the usage of N_2O has been proposed for safety reason [13]. As another approach, the authors' group has found that 4H-SiC$(11\bar{2}0)$ exhibits superior MOS characteristics, especially processed by wet oxidation [14]. In this paper, planar n-channel MOSFETs were fabricated on 4H-SiC(0001), 4H-SiC$(11\bar{2}0)$, and 6H-SiC(0001) with gate oxides grown by either dry O_2 or N_2O at high temperature in order to improve the channel mobility.

P-type epilayers with an acceptor concentration of $1–2 \times 10^{16}$ cm^{-3} were used [15], [16]. Source and drain regions were formed by P^+ ion implantation at 300 °C followed by annealing in pure Ar at 1600 °C for 30 min. The total implant dose was 3×10^{15} cm^{-2}. Then, 50–70-nm-thick gate oxides were grown. Oxidation was performed in dry O_2 (10% diluted in N_2) or N_2O (also 10% diluted in N_2) at 1250–1300 °C. Al was used as gate and ohmic contacts. The typical channel length and width were 30 and 200 μm, respectively.

Table I summarizes the average effective channel mobility obtained for planar inversion-type MOSFETs fabricated on 4H-SiC(0001), $(11\bar{2}0)$, and 6H-SiC(0001) epilayers. Typ-

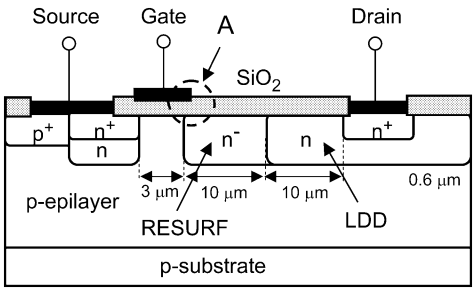

Fig. 1. Schematic structure of an SiC RESURF MOSFET simulated and fabricated in this paper. Both RESURF and LDD regions are 10 μm long and 0.6 μm deep. The p-type epilayer is 10 μm thick, doped to 1×10^{16} cm^{-3}. The typical thickness of gate oxide and channel length are 100 nm and 3 μm, respectively.

ical mobilities obtained by conventional wet O_2 oxidation at 1150 °C are also shown for comparison. Dry O_2 oxidation at 1250 °C resulted in a high channel mobility of 68 cm^2/Vs for 6H-SiC(0001) MOSFET, but further increase in oxidation temperature caused a decrease in mobility. In the case of 4H-SiC, dry O_2 oxidation at high temperature did not bring the improvement of channel mobility for both (0001) and $(11\bar{2}0)$. Instead, direct oxidation by N_2O at 1300 °C is very effective to enhance the mobility of 4H-SiC MOSFETs. A very high mobility close to 80 cm^2/Vs was attained for 4H-SiC$(11\bar{2}0)$ MOSFETs by N_2O oxidation. This mobility improvement can be correlated to the reduction of interface state density near the conduction band edge. The detailed investigation on the MOS interface properties and analysis on the interface structure will be described in a subsequent publication.

III. Structure Optimization of SiC RESURF MOSFETs

Fig. 1 illustrates a schematic structure of SiC RESURF MOSFET simulated and fabricated in this paper. Since it is not easy to satisfy both high avalanching voltage in SiC and low electric field strength in the gate oxide with a simple RESURF structure [17], the lightly doped drain (LDD) region is introduced near the n^+ drain. This is basically the same structure as "two-zone" RESURF reported by Banerjee *et al.* [18].

In this paper, both RESURF and LDD regions are 10 μm long and 0.6 μm deep. The p-type epilayers are 10 μm thick, doped to 1×10^{16} cm^{-3}. The thickness of the gate oxide was 100 nm. The channel length was fixed at 3 μm. The doping concentration (dose) of the RESURF and LDD regions were optimized by using device simulation (ISE-TCAD) to reduce the electric field crowding at the drain edge and in the gate oxide. In the simulation, material properties such as mobility and breakdown field were assumed as those of 4H-SiC(0001), and anisotropy was neglected. Since the properties of SiC depend on polytype as well as crystal orientation, the optimum dose for 4H-SiC$(11\bar{2}0)$ and 6H-SiC(0001) may be different.

Fig. 2 shows the equipotential lines for RESURF MOSFETs (a) without LDD (single RESURF zone) and (b) with properly designed LDD (two RESURF zones) at a high drain voltage of 600 V. The RESURF dose is 3.6×10^{12} cm^{-2} in this particular case. For the MOSFET without LDD, severe electric field crowding takes place at the drain edge as indicated by a dotted circle in Fig. 2(a). By introducing LDD with a 7.8×10^{12} cm^{-2} dose, the equipotential lines are more uniformly distributed in

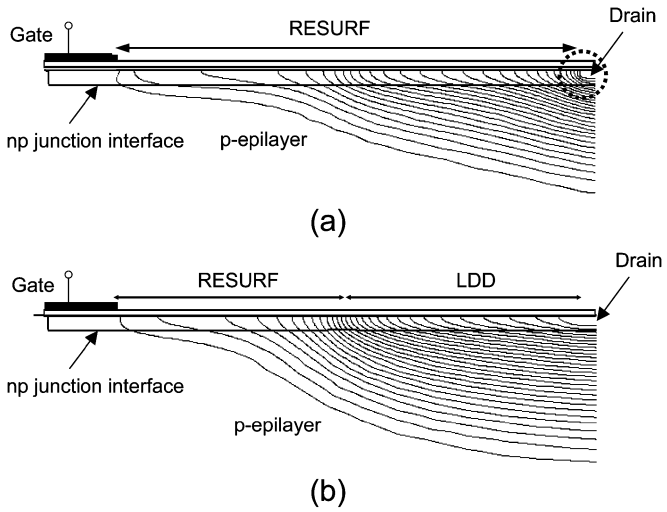

Fig. 2. Equipotential lines for RESURF MOSFETs (a) without LDD (single RESURF zone) and (b) with properly designed LDD (two RESURF zones) at a high drain voltage of 600 V. The RESURF dose is 3.6×10^{12} cm^{-2} in this particular case. The LDD dose shown in (b) is 7.8×10^{12} cm^{-2}. The step for equipotential lines is 20 V.

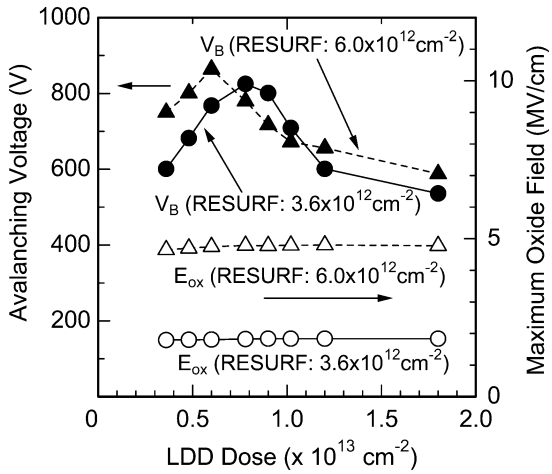

Fig. 3. LDD dose dependencies of avalanching voltage and maximum oxide field at the gate edge (point A in Fig. 1).

both RESURF and LDD regions as shown in Fig. 2(b). The breakdown voltage simulated for MOSFETs with LDD was typically 50–80% higher than that for MOSFETs without LDD.

Fig. 3 depicts the LDD dose dependencies of the avalanching voltage (inside SiC) and the maximum oxide field at the gate edge (point A in Fig. 1) for MOSFETs with a fixed RESURF dose of 3.6×10^{12} cm^{-2} or 6.0×10^{12} cm^{-2}. The avalanching voltage was defined when the impact ionization integral along an electric-force line reaches unity [19]. When the LDD dose is varied, the avalanching voltage exhibits a peak while the oxide field is almost constant. The maximum oxide field only depends on the RESURF dose (a higher RESURF dose leads to an increased oxide field). Thus, the optimum LDD dose can be easily determined for a given RESURF dose, typically in the range from 5×10^{12} cm^{-2} to 9×10^{12} cm^{-2}. Electric field crowding occurs at the drain edge when the LDD dose is too low, and does at the RESURF/LDD interface when the LDD dose is too high.

The RESURF dose dependencies of the avalanching voltage and the oxide field are plotted in Fig. 4, where the influences of

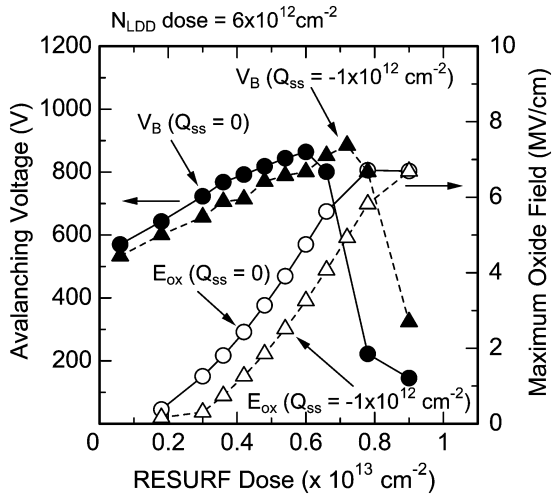

Fig. 4. RESURF dose dependencies of avalanching voltage and maximum oxide field. The influences of MOS-interface charge $(Q_{\rm ss})$ is also presented.

MOS-interface charge $(Q_{\rm ss})$ is also presented. Negative charge was assumed because of electron trapping at the interface. In this simulation, the LDD dose was fixed at 6×10^{12} cm^{-2}. To keep the oxide field below 3 MV/cm for long-term reliability, the RESURF dose should not exceed 5×10^{12} cm^{-2} in the case of an ideal MOS interface $(Q_{\rm ss}=0)$. The optimum RESURF dose shifts toward a higher value with increasing the interface charge, because the negative interface charge enhances the depletion of the RESURF region. In fact, a negative interface charge of 1×10^{12} cm^{-2} actually causes the shift of both plots toward the high RESURF dose side by 1×10^{12} cm^{-2}. When the RESURF dose is low, the electric field strength shows a sharp peak at the RESURF/LDD interface in an electric field analysis. On the other hand, if the RESURF dose is increased too much, the RESURF region fails to be depleted, leading to an abrupt drop of avalanching voltage. The oxide field increases with the RESURF dose, because the voltage drop inside the RESURF region is reduced and the potential at the gate edge of RESURF region is increased for a high RESURF dose.

IV. Fabrication of RESURF MOSFETs

RESURF MOSFETs were fabricated on 10 μm-thick p-type 4H-SiC(0001), $(11\bar{2}0)$, and 6H-SiC(0001) epilayers doped to 1.2×10^{16} cm^{-3} [15], [16]. The RESURF and LDD regions were formed by N^+ implantation with a dose of 4.0×10^{12} and 8.7×10^{12} cm^{-2}, respectively. High-dose P^+ implantation at 300 °C was employed to form the source/drain regions. Post-implantation annealing was performed at 1600 °C in Ar for 20 min. About 2-μm-thick SiO_2 films deposited by plasma chemical vapor deposition (CVD) were used as an implantation mask. In order to reduce the channel resistance, the gate oxides for 6H-SiC(0001) MOSFETs were formed by dry O_2 oxidation at 1250 °C, and the oxides for 4H-SiC(0001) and $(11\bar{2}0)$ MOSFETs by N_2O oxidation at 1300 °C, as described in Section III. The typical channel length and width were 3 μm and 200 μm, respectively. Al was used as gate and ohmic contacts. Ohmic characteristics can be obtained with Al metal when it is deposited on highly-doped n^+-SiC.

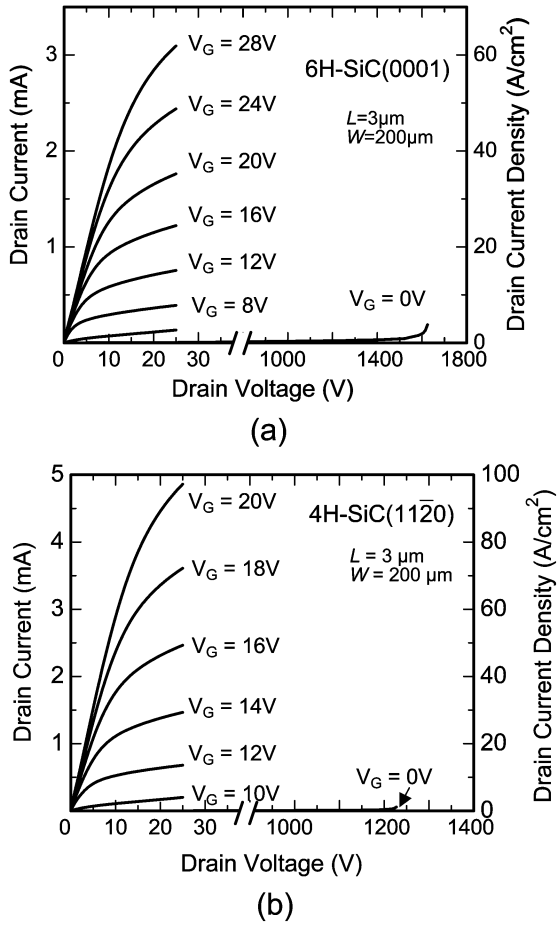

Fig. 5. Output characteristics of (a) 6H-SiC (0001) and (b) 4H-SiC$(11\bar{2}0)$ RESURF MOSFETs fabricated in this paper.

Fig. 5 represents the output characteristics of (a) 6H-SiC(0001) and (b) 4H-SiC$(11\bar{2}0)$ RESURF MOSFETs fabricated in this paper, where normal on-state operation and high-voltage blocking performance are observed. The threshold voltage was 1.0 V for 6H-SiC(0001) and 6.1 V for 4H-SiC$(11\bar{2}0)$ RESURF MOSFET, respectively. The 6H-SiC MOSFET exhibited a high breakdown voltage of 1620 V, while the breakdown voltage for 4H-SiC(0001) and $(11\bar{2}0)$ MOSFETs were 1020 (not shown) and 1230 V, respectively. The higher breakdown voltage for the 6H-SiC device may be partly attributed to the higher breakdown field along the $\langle0001\rangle$ direction of 6H polytype [20]. However, it is also known that the negative charge at the MOS interface of 6H-SiC is lower than that of 4H-SiC. As indicated in Figs. 3 and 4, the interface charge significantly influences the optimum RESURF/LDD doses and thereby the breakdown voltage of MOSFET. To clarify this effect, both 4H- and 6H-SiC RESURF MOSFETs fabricated with various RESURF/LDD doses should be compared. The absolute values of breakdown voltage experimentally obtained were higher than simulated values by 20% in the case of 4H-SiC devices. The reason for this difference might be ascribed to the reduced electric field crowding due to differences in experimental and simulated doping profiles caused by channeling effects in ion implantation and/or lateral diffusion of impurities during annealing. Since the breakdown

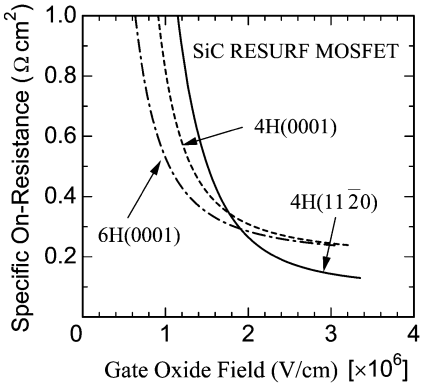

Fig. 6. Specific on-resistances for various SiC RESURF MOSFETs as a function of electric field in gate oxide.

was reversible for all the devices fabricated, the breakdown seems to be limited not by oxide failure but by avalanche inside SiC, probably near the drain edge.

Fig. 6 shows the specific on-resistances for various SiC RESURF MOSFETs as a function of electric field in the gate oxide. Here, the electric field in the oxide was defined simply as the gate voltage divided by the oxide thickness $(V_g/d_{\rm ox})$, because this field is reached in the oxide above the gate-source overlapping region. The on-resistance at an oxide field of 3.0 MV/cm was 234 m$\Omega \cdot$ cm^2 for 6H-SiC(0001), 241 m$\Omega \cdot$ cm^2 for 4H-SiC(0001), and 138 m$\Omega \cdot$ cm^2 for 4H-SiC$(11\bar{2}0)$ RESURF MOSFETs. These characteristics are one of the best performances reported for lateral SiC MOSFETs [21]–[23]. Furthermore, the on-resistances for 6H-SiC(0001) and 4H-SiC$(11\bar{2}0)$ MOSFETs are lower than the classical "Si limit." However, the on-resistances are far from the level expected from the material potential. A rough estimation of the resistance components by using test elements indicates that the channel resistance governs about 40%, 65%, and 45% of total resistances for 6H-SiC(0001), 4H-SiC(0001), and 4H-SiC$(11\bar{2}0)$ MOSFETs, respectively. It also turns out that the contact resistance cannot be neglected in these devices: Contribution to the total on-resistance is about 10%–20%. Further improvements of the MOS interface and/or shortening the channel length will lead to a decreased on-resistance.

Fig. 7 shows the temperature dependence of the specific on-resistance for 4H-SiC(0001), 4H-SiC$(11\bar{2}0)$, and 6H-SiC(0001) RESURF MOSFETs fabricated in this paper. The on-resistance is taken at an oxide field of 3.0 MV/cm. The on-resistances for 4H-SiC$(11\bar{2}0)$ and 6H-SiC(0001) RESURF MOSFETs increase at elevated temperature, because both channel and bulk resistances increase due to enhanced phonon scattering. However, the on-resistance for the 4H-SiC(0001) MOSFET decreases from room temperature to 100 °C, because the channel resistance, the dominant component, is decreased owing to reduced electron trapping. Above 100 °C, phonon scattering becomes more dominant, and the on-resistance turned to increase with increasing temperature. The breakdown voltage exhibited a positive temperature coefficient for all of the measured MOSFETs. For example, the breakdown voltage increased from 1620 V at 20 °C to 1740 V at 150 °C, indicating that the breakdown is governed by an avalanche phenomenon

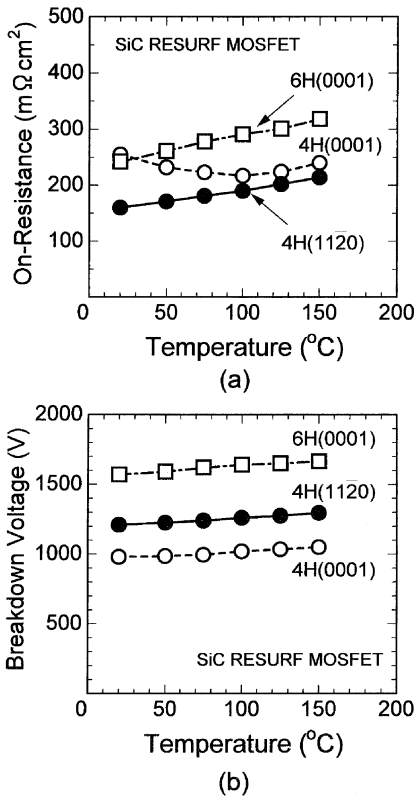

Fig. 7. Temperature dependence of (a) specific on-resistance and (b) breakdown voltage for 4H-SiC(0001), 4H-SiC$(11\bar{2}0)$, and 6H-SiC(0001) RESURF MOSFETs fabricated in this paper. The on-resistance is taken at an oxide field of 3.0 MV/cm.

in SiC, and not by oxide breakdown. The breakdown voltages of 4H-SiC MOSFETs at 150 °C were also about 6–9% higher than those at room temperature. Although this phenomenon can be interpreted by avalanche breakdown, the reduced negative charge at the MOS interface at elevated temperature might cause the change of electric field distribution, and may also contribute to the increased breakdown voltage.

V. Conclusion

Structure optimization and fabrication of RESURF MOSFETs on 4H-SiC(0001), 4H-SiC$(11\bar{2}0)$, and 6H-SiC(0001) have been investigated. By utilizing N_2O oxidation at 1300 °C, the effective channel mobility was improved to 22 and 78 cm^2/Vs for 4H-SiC(0001) and $(11\bar{2}0)$, respectively. Dry O_2 oxidation at 1250 °C resulted in an effective channel mobility of 68 cm^2/Vs for 6H-SiC. The optimum doping concentrations (doses) of the RESURF and LDD regions to reduce the electric field crowding at the drain edge or in the gate oxide were estimated by using device simulation. RESURF MOSFETs were fabricated on 10 μm-thick p-type 4H-SiC(0001), $(11\bar{2}0)$, and 6H-SiC(0001) epilayers doped to 1×10^{16} cm^{-3}. A 6H-SiC(0001) RESURF MOSFET with a 3-μm channel length exhibited a high breakdown voltage of 1620 V and an on-resistance of 234 m$\Omega \cdot$ cm^2. A 4H-SiC$(11\bar{2}0)$ RESURF MOSFET showed the characteristics of 1230 V–138 m$\Omega \cdot$cm^2, which is better than that of 4H-SiC(0001) MOSFET, owing to the higher channel mobility in the 4H-SiC$(11\bar{2}0)$ device.

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