Experimental and Theoretical Investigations on Short-Channel Effects in 4H-SiC MOSFETs

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***Abstract*—In this paper, a fundamental investigation on short-channel effects (SCEs) in 4H-SiC MOSFETs is given. Planar MOSFETs with various channel lengths have been fabricated on p-type 4H-SiC (0001), $(000\bar{1})$ and $(11\bar{2}0)$ faces. In the fabricated MOSFETs, SCEs such as punchthrough behavior, decrease of threshold voltage, deterioration of subthreshold characteristics, and saturation of transconductance occur by reducing channel length. The critical channel lengths below which SCEs occur are analyzed as a function of p-body doping and oxide thickness by using device simulation. The critical channel lengths obtained from the device simulation is in good agreement with the empirical relationship for Si MOSFETs. The critical channel lengths in the fabricated SiC MOSFETs are slightly longer than simulation results. The dependence of crystal face orientations on SCEs is hardly observed. Impacts of interface charge on the appearance of SCEs are discussed.**

***Index Terms*—Device simulation, MOSFET, short-channel effect (SCE), silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) has attracted increasing attention as a wide bandgap semiconductor which has high breakdown field, high thermal conductivity, and high saturation electron drift velocity [1]. Since high-voltage SiC Schottky barrier diodes have been released as real products [2], SiC MOSFETs have been regarded as a promising candidate for low-loss and fast power devices in advanced electronic systems [3]. Among many SiC polytypes, 4H-SiC is the suitable polytype for power devices because of its high bulk mobility and its small anisotropy.

Although 4H-SiC MOSFETs have a great potential for high-voltage power electronic application, the performance of fabricated 4H-SiC MOSFETs had been far from that theoretically expected, because of its low inversion channel mobility and high specific on-resistances. In recent years, however, several successful investigations to increase channel mobility have been reported. For example, oxidation or re-oxidation in NO or N_2O ambience is an attractive process to improve inversion channel mobility [4]–[6]. The "nitridation" process has resulted in the development of high-voltage SiC power MOSFETs with reasonably low on-resistance [7]–[9]. Another method to increase channel mobility is the usage of 4H-SiC $(000\bar{1})$ or $(11\bar{2}0)$ face to fabricate MOSFETs [10], [11]. More recently, a low specific on-resistance below $10\ \mathrm{m\Omega \cdot cm^2}$ has been realized by reducing the channel length to 0.5 μm by using a self-aligned implantation process [12]. SiC lateral MOSFETs with a submicrometer channel length is also very attractive as high-frequency power transistors, which can favorably compete with Si LDMOSFET [13]. The reduction of channel length is effective to gain high switching speed of SiC integrated circuits (ICs) in the future. Thus, the reduction of channel length is of great importance to realize high-performance SiC MOSFETs, in addition to the increase of channel mobility.

In Si MOSFETs, the reduction of channel length may cause short-channel effects (SCEs) [14]. SCEs adversely affect MOSFET performance: For example, punchthrough behavior, decrease of threshold voltage, deterioration of subthreshold characteristics, and saturation of transconductance occur in short-channel MOSFETs. Thus, SCEs should be suppressed. Although the occurrence of SCEs is expected in SiC MOSFETs, very few investigations on SCEs have been reported [15]. While fundamental characteristics of SiC MOSFETs have been investigated [16], the understanding on SCEs in SiC MOSFETs is lacking.

In this paper, the authors have fabricated 4H-SiC MOSFETs with various channel lengths and SCEs have been investigated. A submicrometer channel could be successfully formed by optimizing the fabrication process. Two-dimensional device simulation was also used to analyze SCEs. The experimental and simulated critical channel lengths, below which SCEs occur, are compared with the empirical relationship for Si MOSFETs [17].

II. Device Fabrication

Planar MOSFETs were fabricated on p-type off-axis 4H-SiC (0001) and $(000\bar{1})$ and on-axis $(11\bar{2}0)$ epilayers. The thickness of epilayers was 5 or 10 μm. The acceptor concentration of p-body (N_A) determined from the capacitance–voltage $(C$–$V)$ measurements was about $1 \times 10^{16}\ \mathrm{cm^{-3}}$ or $1 \times 10^{17}\ \mathrm{cm^{-3}}$. The source/drain regions were formed by high-dose P^+ implantation. About 2-μm-thick SiO_2 deposited by plasma-enhanced chemical vapor deposition was employed as an implantation mask. The SiO_2 mask was patterned by reactive ion etching with a CF_4–H_2 chemistry. Multiple P^+ implantation was carried out at 300 °C to form a 0.2-μm-deep box profile of P atoms with implant doses of $2.8 \times 10^{15}\ \mathrm{cm^{-2}}$, $1.2 \times 10^{15}\ \mathrm{cm^{-2}}$, $6.0 \times 10^{14}\ \mathrm{cm^{-2}}$, and $4.0 \times 10^{14}\ \mathrm{cm^{-2}}$ at 110, 60, 30, and 10 keV, respectively. After ion implantation, high-temperature annealing was performed at 1600 °C for 10 min with a graphite cap to suppress surface roughening [18]. After the RCA cleaning, thermal oxidation was carried out in dry N_2O (10% diluted in N_2) ambience at 1300 °C, followed by post-oxidation-annealing in a N_2 ambience at 1300 °C for 30 min [6], [19]. The gate-oxide

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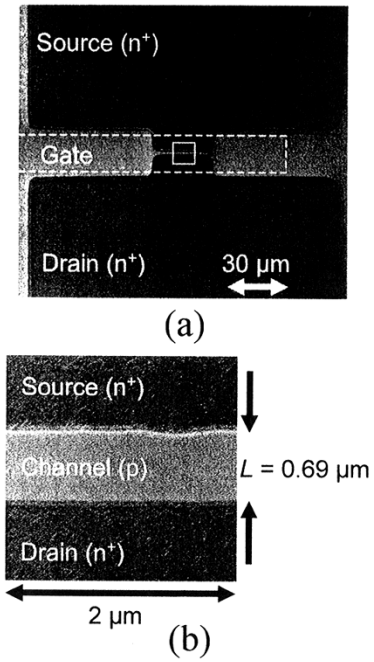

Fig. 1. (a) SEM images of overall view of a fabricated 4H-SiC MOSFET and (b) submicrometer channel region after post-implantation annealing. The dark area is the n^+-region and the bright area the p-region.

TABLE I
AVERAGE EFFECTIVE MOBILITY OF FABRICATED 4H-SIC MOSFETS

	effective channel mobility [cm^2/Vs]		
p-body doping [cm^{-3}]	(0001)	$(000\bar{1})$	$(11\bar{2}0)$
10^{16}	21	28	71
10^{17}	11	19	53

thickness (d) was about 70 nm and gate metal was Al. The channel length (L) and width (W) of MOSFETs are 0.2–15 and 30–150 μm, respectively. As the first fundamental investigation, only the channel length and p-body doping concentration were varied without any vertical scaling of the device in this study.

Fig. 1 shows a typical scanning electron microscopy (SEM) image (plan view) of (a) the overall view of MOSFET and (b) the channel region after post-implantation annealing. In Fig. 1, the dark and bright areas correspond to n^+- and p-regions, respectively. The dashed line in Fig. 1(a) means the region where gate electrode is formed after thermal oxidation. Fig. 1(b) exhibits the magnified view of channel region in Fig. 1(a), the area enclosed with white line. A submicrometer channel (p-region) can be successfully formed. In this study, the channel length for each MOSFET was not defined from a mask pattern but directly measured by SEM as shown in Fig. 1(b).

III. RESULTS AND DISCUSSION

A. Basic MOSFET Performance

Average effective channel mobilities (μ_{eff}) obtained from the fabricated MOSFETs are listed in Table I. The $(11\bar{2}0)$ and $(000\bar{1})$ MOSFETs exhibited higher channel mobility than the (0001) MOSFETs. The lightly doped MOSFET on $(11\bar{2}0)$ face showed a high effective channel mobility of 71 $cm^2/V \cdot s$. Although the increase of acceptor concentration led to the decrease of channel mobility for each face, the $(11\bar{2}0)$ MOSFETs exhibited a mobility of 53 $cm^2/V \cdot s$ even for the p-body doping of 10^{17} cm^{-3}. The relatively high channel mobility for $(11\bar{2}0)$ and $(000\bar{1})$ MOSFETs can be attributed to the lower interface state density near the conduction band edge. The detailed analysis on the MOS interface are described elsewhere [20].

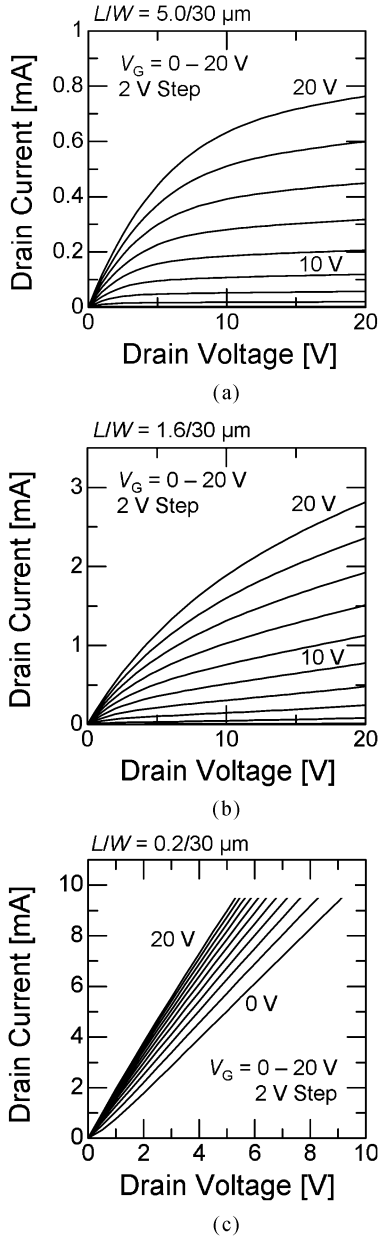

Fig. 2. Drain characteristics of lightly doped $(N_A = 9 \times 10^{15}\ cm^{-3})$ 4H-SiC MOSFETs on the (0001) face: (a) $L = 5.0$ μm, (b) $L = 1.6$ μm, (c) $L = 0.2$ μm. Non-saturation characteristics due to punchthrough are observed in MOSFET with the submicrometer channel length.

B. Observation of SCEs

Fig. 2 shows the drain current (I_D)-drain voltage (V_D) characteristics of MOSFETs on lightly doped $(N_A = 9 \times 10^{15}\ cm^{-3})$ (0001) epilayers with three different channel lengths: (a) $L = 5.0$, (b) $L = 1.6$, and (c) $L = 0.2$ μm, respectively. The gate voltage is varied from 0 to 20 V. The long-channel $(L = 5.0\ \mu m)$ MOSFET exhibited saturation characteristics [Fig. 2(a)], while nonsaturation characteristics

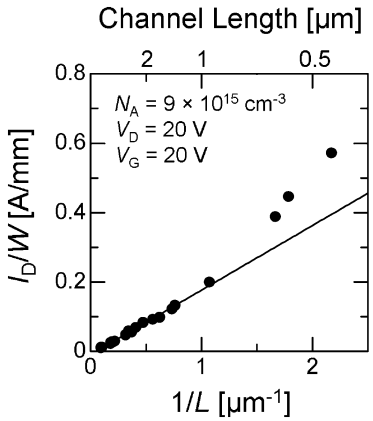

Fig. 3. Relationship between the drain current (I_D) and the inverse of channel length $(1/L)$ in the 4H-SiC (0001) MOSFETs. The reduction of channel length causes the increase of drain current. The drain current in short-channel MOSFETs is higher than expected values.

due to drain-induced barrier lowering (DIBL) are observed in Fig. 2(b) $(L = 1.6\ \mu\text{m})$ [21]. The shortest channel MOSFET, with a channel length of 0.2 μm, exhibits ohmic-like drain current at zero gate bias, indicating a punchthrough behavior due to SCEs [Fig. 2(c)]. Punchthrough behavior was observed only in lightly doped MOSFETs with submicrometer channel lengths but not in highly doped MOSFETs. Similar results were obtained for 4H-SiC $(000\bar{1})$ and $(11\bar{2}0)$ MOSFETs.

Fig. 3 shows the relationship between channel length and drain current of MOSFETs on lightly doped epilayers. Drain current at fixed bias voltage is inversely proportional to channel length for long-channel MOSFETs. As the channel length is reduced, however, the relationship between drain current and the inverse of channel length deviates from the proportionality.

In this paper, the threshold voltage was defined from the drain current (I_D)-gate voltage (V_G) plot in the linear region and the $\sqrt{I_D}$-V_G plot in the saturation region as shown in Fig. 4(a) and (b), respectively. Fig. 4 shows the gate characteristics of lightly doped MOSFETs fabricated on the (0001) face, where the drain current is normalized by channel length (L) and width (W). Note that the difference in threshold voltage determined from the linear region and the saturation region is small for MOSFETs with relatively long channel. In the linear region [Fig. 4(a)], the threshold voltage is slightly decreased by reducing the channel length. The drain current of 0.6 μm-channel MOSFET is saturated because of series resistance effect. The threshold voltage in the saturation region is shifted toward the negative direction by the reduction of channel length, and the 0.6 μm-channel MOSFET cannot shut off the drain current due to punchthrough behavior.

The drain/voltage dependence of threshold voltage in the (0001) MOSFET with the p-body acceptor concentration of 9×10^{15} cm^{-3} is shown in Fig. 5. The threshold voltage decreased when the drain voltage was increased. The decrease in threshold voltage is pronounced for MOSFETs with short channel length, which is mainly caused by DIBL [21]. The highly doped MOSFETs hardly exhibited such decrease in threshold voltage (not shown).

The channel length dependencies of threshold voltage (V_T) at drain voltages of (a) 0.1 V and (b) 20 V for 4H-SiC (0001)

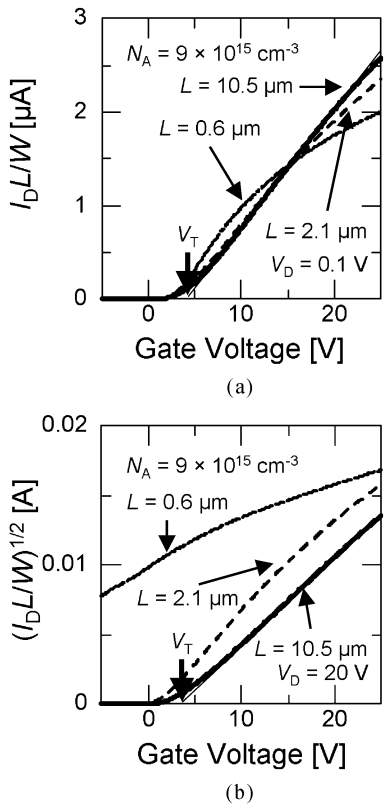

Fig. 4. (a) Gate voltage dependence of drain current and (b) $\sqrt{I_D}$ in lightly doped 4H-SiC (0001) MOSFETs. Threshold voltage in the linear and saturation region is defined from the plots (a) and (b), respectively.

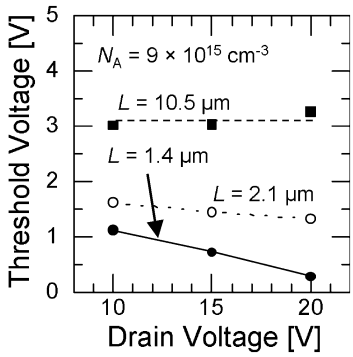

Fig. 5. Drain voltage dependence of threshold voltage in the lightly doped $(N_A = 9 \times 10^{15}\ \text{cm}^{-3})$ MOSFETs on the 4H-SiC (0001) face. The threshold voltage is decreased with increasing drain voltage and/or reducing channel length.

MOSFETs are shown in Fig. 6. At the low drain voltage of 0.1 V [Fig. 6(a)], the lightly doped MOSFETs exhibit gradual decrease in threshold voltage with shortening the channel length, and the threshold voltage decreases below 0 V in the shortest channel MOSFET. For highly doped MOSFETs, the decrease of threshold voltage was not observed. At the high drain voltage of 20 V [Fig. 6(b)], the decrease of threshold voltage occurs not only in lightly doped MOSFETs but in highly doped MOSFETs, though the decrease itself is smaller. Thus, the decrease of threshold voltage becomes more pronounced in the lightly doped devices when drain voltage becomes higher, being in good agreement with characteristics of Si MOSFETs [14], [21].

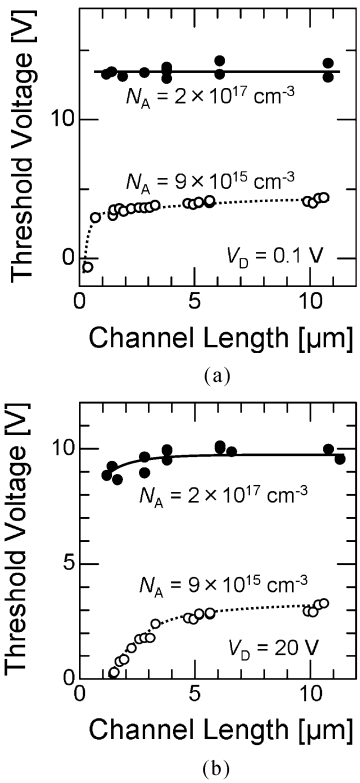

Fig. 6. Relationship between the threshold voltage and the channel length. (a) $V_D = 0.1$ V. (b) $V_D = 20$ V. Closed and open circles represent characteristics of highly doped and lightly doped MOSFETs on the (0001) face, respectively.

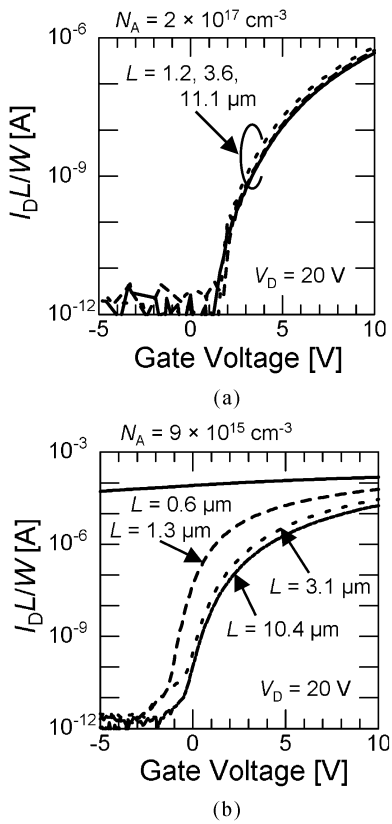

Fig. 7. Subthreshold characteristics of 4H-SiC (0001) MOSFETs fabricated on (a) highly doped and (b) lightly doped epilayers. The drain current is normalized by the channel length and width. The lightly doped MOSFET with a submicrometer channel length cannot be turned off.

The subthreshold characteristics (log I_D–V_G characteristics) of (a) highly doped and (b) lightly doped (0001) MOSFETs are shown in Fig. 7, in which drain current is normalized by channel length and width. In this measurement, the drain voltage was fixed at 20 V, where SCEs are pronounced. For highly doped MOSFETs, the subthreshold characteristics are not deteriorated even for a channel length of 1.2 μm [Fig. 7(a)]. However, for lightly doped MOSFETs, the subthreshold characteristics are deteriorated with the reduction of channel length [Fig. 7(b)]. When channel length is reduced from 10.4 to 3.1 or 1.3 μm, the subthreshold characteristics slightly shifted toward the negative gate voltage direction, which is consistent with a slight decrease of threshold voltage, as shown in Fig. 6, while the change of subthreshold slope is not significant. In the 0.6-μm-channel MOSFET, the significant drain current flowed even at the negative gate bias, due to punchthrough behavior.

Fig. 8 shows the relationship between the transconductance (g_m) and the channel length in (0001) MOSFETs, where the transconductance was determined at a drain voltage of 20 V and a gate voltage of 20 V. The transconductance is inversely proportional to the channel length for long-channel MOSFETs. For short-channel $(L \leq 2\ \mu\text{m})$ MOSFETs fabricated on lightly doped epilayers, however, the transconductance is smaller than that extrapolated from the characteristics of long-channel MOSFETs. On the other hand, for highly doped MOSFETs, the transconductance is proportional to the inverse of channel length within the investigated range of channel length.

As described above, SCEs are most pronounced at high drain voltage in the lightly doped MOSFETs. The depletion layer

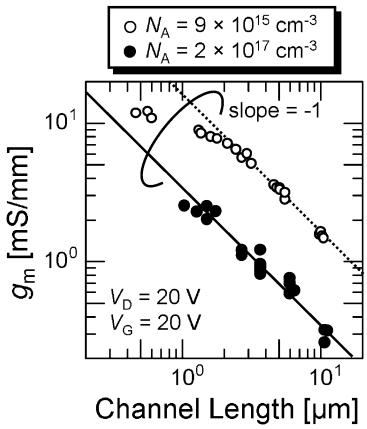

Fig. 8. Relationship between the transconductance and the channel length in 4H-SiC (0001) MOSFETs. For the lightly doped MOSFETs, the saturation of transconductance is observed.

from the drain region is more extended at higher drain voltage, resulting in the occurrence of SCEs. The extension of depletion region is more significant in lightly doped devices, which promotes the occurrence of SCEs. Quantitative analyses are described Section III-C. To investigate the dependencies of crystal face orientation, the authors fabricated MOSFETs on (0001), $(000\bar{1})$, and $(11\bar{2}0)$ faces. However, MOSFETs on each face showed similar phenomena when the channel length was reduced, and the crystal face dependencies were hardly observed.

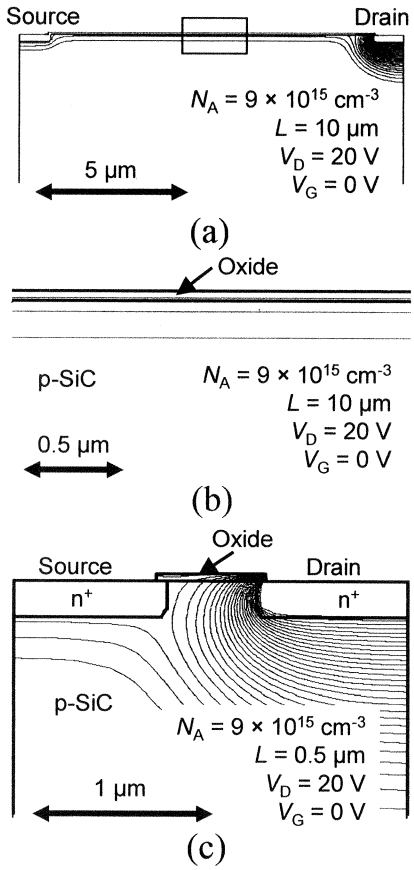

Fig. 9. (a), (b) Contour lines of electric potential inside the channel region in simulated 4H-SiC MOSFETs with the channel length of 10 μm and (c) 0.5 μm. The acceptor concentration of p-body is 9×10^{15} cm^{-3}. In the MOSFET with a channel length of 0.5 μm, the electric potential shows 2-D distribution.

C. Device Simulation

The phenomena which occurred in short-channel SiC MOSFET were simulated by using two-dimensional (2-D) device simulator (ISE-DESSIS). In the device simulation, the acceptor concentration of p-body, oxide thickness, and channel length were varied and the junction depth was about 0.2 μm. An ideal MOS interface was assumed in the simulation. SCEs such as the decrease of threshold voltage and the deterioration of subthreshold characteristics were also observed in the simulated MOSFETs.

Typical electric potential distributions simulated for SiC MOSFETs are shown in Fig. 9. The simulated MOSFETs have the acceptor concentration of 9×10^{15} cm^{-3} and gate oxide thickness of 55 nm. The channel length was varied from 0.5 to 10 μm. This structure is similar to that of fabricated MOSFETs. Fig. 9(a) and (b) exhibits the contour lines of electric potential for a long-channel ($L = 10\,\mu$m) MOSFET, and Fig. 9(c) the contour lines for a short-channel ($L = 0.5\,\mu$m) MOSFET. Fig. 9(b) exhibits the magnification of channel region marked by the rectangle in Fig. 9(a). Although the contour lines inside the channel region in the long-channel MOSFET show one-dimensional distribution as shown in Fig. 9(b), the electric potential distribution becomes 2-D in the short-channel MOSFETs [Fig. 9(c)]. The reduction of channel length makes the influence of depletion layer from the drain region significant, and the potential inside the channel region is decreased, which causes SCEs.

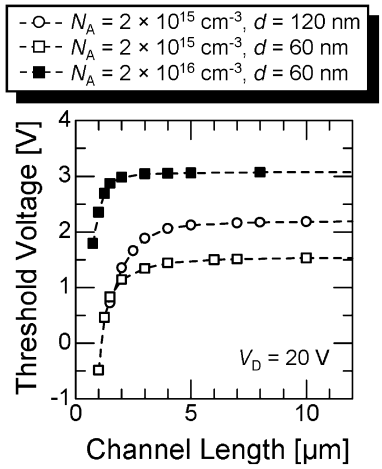

Fig. 10. Relationship between the threshold voltage and the channel length in simulated MOSFETs. Decrease of threshold voltage is more pronounced when the p-body doping is lower and/or the oxide thickness is thicker.

Fig. 10 shows the channel length dependence of threshold voltage obtained by device simulation. In the simulation, the threshold voltage was determined in the same manner as experiments. In Fig. 10, the open circles mean the results for MOSFETs with an acceptor concentration of 2×10^{15} cm^{-3} and a gate oxide thickness of 120 nm, the open squares the MOSFETs with an acceptor concentration of 2×10^{15} cm^{-3} and a gate oxide thickness of 60 nm, and the closed squares the MOSFETs with an acceptor concentration of 2×10^{16} cm^{-3} and a gate oxide thickness of 60 nm. In the simulation, the decrease of threshold voltage takes place steeply at a shorter channel length, when the MOSFETs have higher p-body doping and/or thinner oxide thickness, in agreement with experimental results.

In Fig. 11, the relationship between threshold voltage and channel length in the simulated MOSFETs is compared with that in the fabricated MOSFETs. The acceptor concentration and gate oxide thickness for simulated MOSFETs are 2×10^{17} cm^{-3} and 70 nm [Fig. 11(a)] and 9×10^{15} cm^{-3} and 55 nm [Fig. 11(b)], respectively. This structure is similar to that of fabricated MOSFETs in both cases. The open and closed circles denote the simulated and experimental results, respectively. In the long channel region, the experimental threshold voltages [about 10 V in (a) and 3 V in (b)] are higher than the simulated values [about 9 V in (a) and 2 V in (b)] because of negative effective fixed charge at the SiC/SiO_2 (MOS) interface. In n-channel 4H-SiC MOSFETs, negative effective fixed charge exists at the MOS interface because electrons induced by gate voltage are trapped at a high density of interface states [19], [22]. The influence of effective fixed charge on SCEs is discussed Section III-D. In the short channel region, the threshold voltage of fabricated MOSFETs decreased gradually at a longer channel length than that of the simulated devices. The reason for decrease in experimental threshold voltage at relatively long channel length is not clear at present. However, the acceptor concentration in SiC near the MOS interface in the fabricated MOSFETs may be lower than the value determined by *I–V* measurements on as-grown epilayers. After thermal oxidation, the nitrogen atoms are accumulated in SiC near the MOS interface [23]. The increase of nitrogen concentration

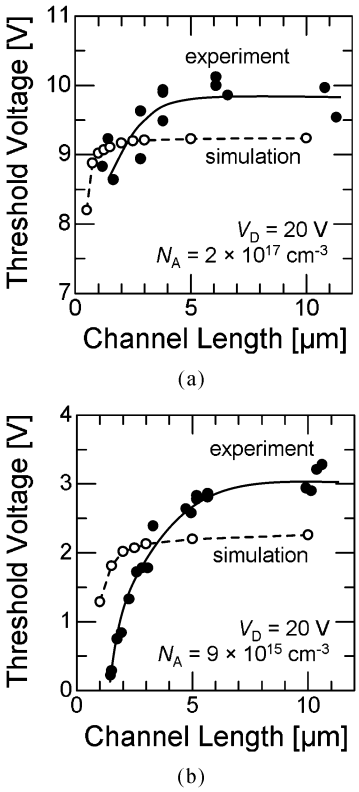

Fig. 11. Channel length dependence of threshold voltage for simulated and fabricated 4H-SiC MOSFETs with (a) high acceptor concentration and (b) low acceptor concentration. Decrease of threshold voltage takes place at a shorter channel length in simulated MOSFETs than in fabricated MOSFETs.

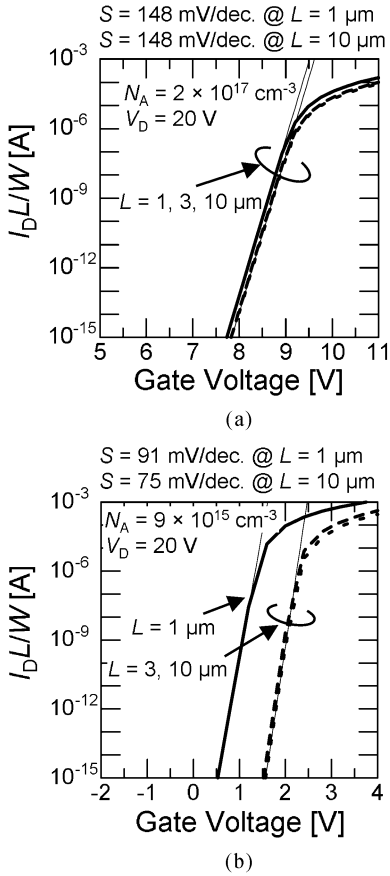

Fig. 12. Subthreshold characteristics of 4H-SiC MOSFETs obtained by device simulation. The drain current is normalized by the channel length and width. The simulated devices have (a) acceptor concentration of 2×10^{17} cm^{-3} and oxide thickness of 70 nm and (b) acceptor concentration of 9×10^{15} cm^{-3} and oxide thickness of 55 nm. Deterioration of subthreshold characteristics occurs only in lightly doped MOSFETs.

naturally leads to the decrease of acceptor concentration near the MOS interface. Another reason may be related to the junction depth in the fabricated MOSFETs. The junction depth (0.2 μm) in the fabricated MOSFETs was simulated by transport of ions in matter calculation. However, the real junction depth becomes lager, due to small channeling effects during implantation and slight diffusion near the tail region [24]. Both the decrease of acceptor concentration and the increase of junction depth enhance the extension of depletion layer, and lower the potential inside channel region. This suggests that SCEs occur more easily in the fabricated MOSFETs, compared with the simulated MOSFETs. Although the channel length was determined from SEM images of SiC surface, the distance between the source and drain region may be shorter in the buried region because of the larger straggle of high-energy P^+ implantation. This may also enhance the SCEs in the fabricated devices.

Fig. 12 shows the subthreshold characteristics in the simulated devices with a (a) highly doped and (b) lightly doped p-body. In the figure, the drain current is normalized by channel length and width. In the simulation of highly doped MOSFETs, the subthreshold characteristics are not deteriorated when the channel length is reduced to 1.0 μm [Fig. 12(a)], in agreement with experimental results [Fig. 7(a)]. The subthreshold slope (S) of the MOSFET with high p-body doping and channel length of 10 μm is 148 mV/dec. When the channel length is reduced to 1.0 μm, the subthreshold slope is not changed (148 mV/dec). For the lightly doped MOSFETs [Fig. 12(b)], the negative shift of subthreshold characteristics due to the decrease of threshold voltage is observed, and the subthreshold slope is increased from 75 to 91 mV/dec when channel length is reduced from 10.0 to 1.0 μm. It should be noted, however, that the subthreshold swings (slopes) for simulated MOSFETs are much lower than experimental values, due to a high density of interface states in real MOSFETs.

D. Critical Channel Length

In Si MOSFETs, the boundary between long-channel and short-channel MOSFETs is described as [17]

$$L_{\rm crit} = 0.4\gamma^{1/3}. \tag{1}$$

Here, the $L_{\rm crit}$ means the critical channel length below which SCEs occur, and γ is given by

$$\gamma = r_j d(W_S + W_D)^2 \tag{2}$$

where r_j is the junction depth in μm, d the oxide thickness in Å, and W_S and W_D the source and drain depletion width in μm, respectively. In [17], Si short-channel MOSFETs are defined based upon two criteria. The first criterion is based on the channel length dependence of drain current. The MOSFET which exhibits a 10% (or more) deviation (increase) in drain current from the linear dependence upon the inverse of channel

length is regarded as a short-channel device. The second criterion is related to the dependence of the subthreshold current on drain voltage [25], [26]. Long-channel devices do not exhibit the drain-voltage dependence of drain current in the subthreshold region when the drain voltage is larger than $3kT/q$. The MOSFET, drain current of which increases with increasing drain voltage in the subthreshold region, is defined as a short-channel device.

Characteristics of SiC MOSFETs with various structures including channel length were simulated, and the critical channel length was estimated. In the simulation, the short-channel SiC MOSFETs were defined based upon the same criterion as Si MOSFETs, which is the dependence of subthreshold current on drain voltage. From this analysis, the boundary can be described as

$$L_{\rm crit} = 0.44\gamma^{1/3}. \tag{3}$$

This simulation result in SiC MOSFETs is in very good agreement with the empirical relationship for Si MOSFETs. Considering SiC and Si MOSFETs with the same structure, the potential inside channel region should be mainly influenced by the extension of depletion layer from the drain region, and not by the bandgap itself. The extension of depletion region in SiC and Si MOSFETs is almost the same at given bias, because the smaller dielectric constant of SiC is almost cancelled by a larger built-in voltage. Therefore, the critical channel lengths of simulated SiC MOSFETs are almost the same as those of Si MOSFETs.

The authors tried to determine the critical channel length in the fabricated SiC MOSFETs according to the same criteria as in Si MOSFETs described above (increase of drain current). However, it was difficult to define the short-channel MOSFETs in this manner, due to fluctuation of drain current observed for the fabricated MOSFETs with similar structures. Therefore, a new criterion related to the decrease of threshold voltage has been employed in this paper.

The drain current of a MOSFET can be described as

$$I_D = \frac{\mu W C_{\rm OX}}{L}(V_G - V_T)V_D \tag{4}$$

in the linear region and

$$I_{\rm Dsat} = \frac{\mu W C_{\rm OX}}{L}\frac{(V_G - V_T)^2}{2} \tag{5}$$

in the saturation region [14], where $C_{\rm OX}$ is the oxide capacitance per unit area. When the threshold voltage (V_T) is reduced to $V_T - \Delta V_T$, the increase of drain current in the linear and saturation regions (ΔI_D and $\Delta I_{\rm Dsat}$, respectively) can be expressed by

$$\Delta I_D = \frac{\mu W C_{\rm OX}}{L} V_D \Delta V_T \tag{6}$$

and

$$\Delta I_{\rm Dsat} \simeq \frac{\mu W C_{\rm OX}}{L}(V_G - V_T)\Delta V_T. \tag{7}$$

Here, the term $\Delta {I_D}^2$ was neglected. Thus, the increase of drain current is proportional to the decrease of threshold voltage. The relative increase normalized by the drain current is given by the following:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta V_T}{V_G - V_T} \propto \Delta V_T \tag{8}$$

in the linear region and

$$\frac{\Delta I_{\rm Dsat}}{I_{\rm Dsat}} = \frac{2\Delta V_T}{V_G - V_T} \propto 2\Delta V_T \tag{9}$$

in the saturation region. The $\Delta I_D/I_D$ and $\Delta I_{\rm Dsat}/I_{\rm Dsat}$ are proportional to ΔV_T and $2\Delta V_T$, respectively. Therefore, in this study, short-channel MOSFETs are defined as the devices, threshold voltage of which is lower than that of sufficiently long-channel MOSFETs by 1.0 V in the linear region and 0.5 V in the saturation region.

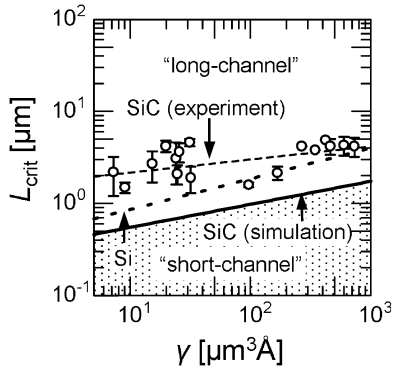

Fig. 13. Critical channel length versus γ relationship. Open circles with error bars and dashed line represent experimental results and their least-square fit, respectively. The solid line means the relationship simulated for SiC MOSFETs. The dotted line shows the empirical relationship for Si MOSFETs.

Fig. 13 shows the critical channel length versus γ for various MOSFETs. The open circles with error bars and dashed line mean the critical channel lengths for the fabricated SiC MOSFETs and their least-square fitting, respectively. The solid line represents the simulated critical channel length of SiC MOSFETs determined by the ΔV_T definition described above. The dotted line shows the empirical relationship for Si MOSFETs, which is described as "$L_{\rm crit} = 0.4\gamma^{1/3}$." In the fabricated MOSFETs, the relationship between $L_{\rm crit}$ and γ can be described as (shown by the dashed line)

$$L_{\rm crit} = 1.56\gamma^{1/7}. \tag{10}$$

On the other hand, the relationship for simulated SiC MOSFETs is described as

$$L_{\rm crit} = 0.31\gamma^{1/4}. \tag{11}$$

Although the critical channel lengths of fabricated SiC MOSFETs show a trend similar to the simulation results, the absolute values of experimental critical channel length are longer than those theoretically expected. As discussed in the last subsection, the acceptor concentration in SiC near the MOS interface may be lower and the junction depth may be larger in the fabricated MOSFETs. This leads to the increase of "γ" and thereby to the increase of critical channel length. In addition to these factors,

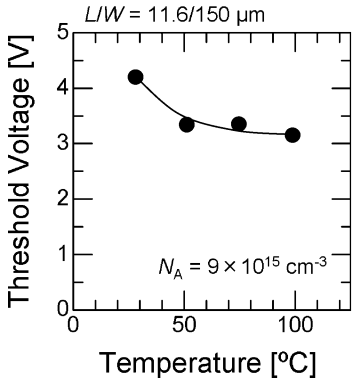

Fig. 14. Temperature dependence of threshold voltage for a lightly doped 4H-SiC (0001) MOSFET. The threshold voltage decreased with elevating temperature.

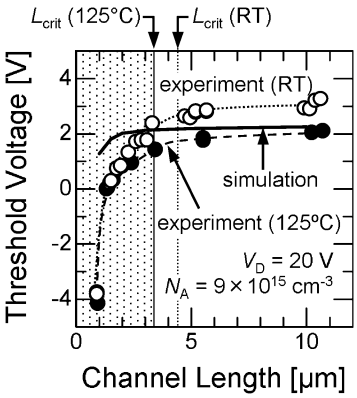

Fig. 15. Channel length dependence of threshold voltage at room temperature and 125 °C in 4H-SiC (0001) MOSFETs with low p-body doping. The simulated relationship is also plotted by the solid curve. At a high temperature, the decrease of threshold voltage occurred more steeply at shorter channel length than at room temperature.

the effective fixed charge at the SiO_2/SiC interface may influence on SCEs, as described below.

As shown in Fig. 11, the experimental threshold voltage gradually decreases from a relatively long-channel length region when reducing the channel length, while the simulated threshold voltage shows a steep decrease near the critical channel length. Thus, the critical channel lengths of fabricated MOSFETs may be overestimated due to the gradual decrease of threshold voltage in the relatively long-channel region. This gradual decrease of threshold voltage may be caused by the effective fixed charge at the MOS interface. To investigate the influence of effective fixed charge on SCEs, MOSFET characteristics at high temperature were analyzed. Fig. 14 shows the temperature dependence of threshold voltage for 4H-SiC (0001) MOSFETs fabricated in this study. The threshold voltage decreased with elevating temperature, meaning the decrease of negative effective fixed charge, due to the enhanced electron emission from interface states. Fig. 15 exhibits the relationship between threshold voltage and channel length in the fabricated 4H-SiC (0001) MOSFETs at room temperature (RT) and high temperature (125 °C). The simulated result is also shown by a solid curve. At the high temperature, the gradual decrease of threshold voltage is suppressed, and the relationship between threshold voltage and channel length approaches the result obtained by device simulation. As a result, the critical channel lengths at high temperature become shorter than those at room temperature. Therefore, the effective fixed charge at the MOS interface has impacts on the appearance of SCEs. Detailed analyses on this issue are now under investigation.

IV. Conclusion

4H-SiC MOSFETs with various channel lengths have been fabricated to investigate SCEs. In the lightly doped MOSFETs, the SCEs occurred even at a relatively long channel of 3–5 μm, while it was hard to observe the SCEs in highly doped MOSFETs with a 1 μm-long channel.

The critical channel lengths, below which SCEs occur, were analyzed. The boundary between short-channel devices and long-channel devices can be described as "$L_{\rm crit} = 1.56\gamma^{1/7}$" for the fabricated MOSFETs and "$L_{\rm crit} = 0.31\gamma^{1/4}$" for the simulated MOSFETs. The difference in critical channel length for Si and 4H-SiC MOSFETs is not very large, because the occurrence of SCEs is mainly affected by the depletion layer extended from the drain, and not by the bandgap or breakdown field. The effective fixed charge at the SiC MOS interface apparently enhances the SCEs, and this tendency is less-pronounced at elevated temperature because the effective fixed charge caused by electron trapping decreases. The crystal face dependence was hardly observed.

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