

4H-SiC Lateral Double RESURF MOSFETs With Low ON Resistance

Masato Noborio, *Student Member, IEEE*, Jun Suda, and Tsunenobu Kimoto, *Senior Member, IEEE*

Abstract—Designing and fabrication of 4H-SiC (0001) lateral MOSFETs with a double reduced surface field (RESURF) structure have been investigated to reduce ON resistance. In order to achieve high breakdown voltage, a two-zone RESURF structure was also employed in addition to the double RESURF structure. The simulated double RESURF MOSFETs with optimum doses exhibit slightly higher breakdown voltage and lower drift resistance than the simulated single RESURF MOSFETs. The double RESURF structure is attractive to suppress oxide breakdown at gate edge. After the device simulation for dose optimization, the 4H-SiC two-zone double RESURF MOSFETs have been fabricated by using a self-aligned process. The fabricated MOSFET has demonstrated a high breakdown voltage of 1380 V and a low ON resistance of $66 \text{ m}\Omega \cdot \text{cm}^2$ (including a drift resistance of $24 \text{ m}\Omega \cdot \text{cm}^2$). The drift resistance of the fabricated double RESURF MOSFETs is only 50% or even lower than that of the single RESURF MOSFETs.

Index Terms—Breakdown voltage, device simulation, MOSFET, ON resistance, reduced surface field (RESURF), silicon carbide (SiC).

I. INTRODUCTION

SILICON CARBIDE (SiC) has attracted increasing attention as a wide-bandgap semiconductor for advanced high-power devices [1]. Among many SiC polytypes, 4H-SiC has been recognized as the suitable polytype for power devices due to its high bulk mobility and its small anisotropy. Increasing maturity of material quality is another advantage of 4H-SiC.

A number of vertical high-voltage SiC MOSFETs, which significantly outperform the theoretical limit of Si unipolar devices, have already been demonstrated as discrete devices [2]–[6]. On the other hand, only a limited number of reports on SiC lateral power MOSFETs, which show great promise for high-voltage power ICs in the next generation [7], have been published. The reduced surface field (RESURF) structure is attracted to attain high breakdown voltage in the lateral MOSFETs [8]. However, the ON resistance of SiC RESURF MOSFETs has still been high due to its high channel resistance [9]–[14]. In recent years, several successful developments of SiC MOS technology to increase the channel mobility have been reported. For example, “nitridation” process is effective to

enhance channel mobility [15]–[17], and the usage of 4H-SiC (000 $\bar{1}$) or (11 $\bar{2}$ 0) face is another attractive approach to fabricate high-channel mobility SiC MOSFETs [18], [19]. In our previous work [20], high breakdown voltage over 1 kV and low ON resistance below $100 \text{ m}\Omega \cdot \text{cm}^2$ have been realized in 4H-SiC two-zone RESURF MOSFETs with N_2O -grown gate oxides. The ratio of drift resistance to the total ON resistance for this device was about 50%. Thus, the reduction of drift resistance has become important even in SiC MOSFETs for further improvement of the device performance.

In this paper, the authors have designed and fabricated high-voltage SiC lateral MOSFETs with a double RESURF structure to reduce the drift resistance. By employing a two-zone RESURF structure in addition to the double RESURF structure, both high breakdown voltage and low ON resistance could be realized.

II. DEVICE STRUCTURE AND CONCEPT

Fig. 1(a) shows the structure of a two-zone double RESURF MOSFET simulated and fabricated in this paper. The double RESURF structure has a thin p-layer (top-p region) placed on the top of the RESURF region [21]. Since the double RESURF region is depleted not only from the bottom p-epilayer/RESURF junction but also from the RESURF/top-p junction, a higher RESURF dose can be employed than the normal RESURF MOSFETs, leading to a lower ON resistance, the concept of which is similar to “superjunction” devices [22]. In order to achieve high breakdown voltage, it is important to reduce the electric field strength at both the gate and drain edges. To achieve this, the RESURF region is divided into two regions: a low-dose RESURF1 region close to the gate edge and a high-dose RESURF2 region close to the drain region [10], as shown in Fig. 1(a).

The authors fabricated two types of RESURF MOSFETs; the drift length (L_{Drift}), which is the sum of RESURF1 and RESURF2 length, was different. The RESURF1 and RESURF2 lengths were $5 \mu\text{m}$ each (total drift length: $10 \mu\text{m}$) or $10 \mu\text{m}$ each (total drift length: $20 \mu\text{m}$). The depths of RESURF and top-p regions were 0.6 and $0.1 \mu\text{m}$, respectively. The gate overlapping length was $5 \mu\text{m}$, and the distance between top-p region and MOS channel region on the surface was about $1 \mu\text{m}$.

Fig. 1(b) shows the structure of a test element group (TEG) device fabricated in this paper. The TEG devices have a similar structure to RESURF MOSFETs, except for channel region. The channel length of TEG device was $0 \mu\text{m}$, which means that the source region is shorted to the RESURF1 region. Thus, in TEG devices, the channel resistance can be neglected, and the

Manuscript received August 2, 2006; revised January 4, 2007. This work was supported in part by Grant-in-Aid for Research Fellow of Japan Society for the Promotion of Science, by a Grant-in-Aid for Scientific Research (No. 18206032), and by the 21st century COE Program (No. 14213201) from the Ministry of Education, Culture, Sports, and Technology, Japan. The review of this paper was arranged by Editor M. A. Shibib.

The authors are with the Department of Electronic Science and Engineering, Kyoto University, Kyoto 615-8510, Japan (e-mail: noborio@semicon.kuee.kyoto-u.ac.jp).

Digital Object Identifier 10.1109/TED.2007.894249

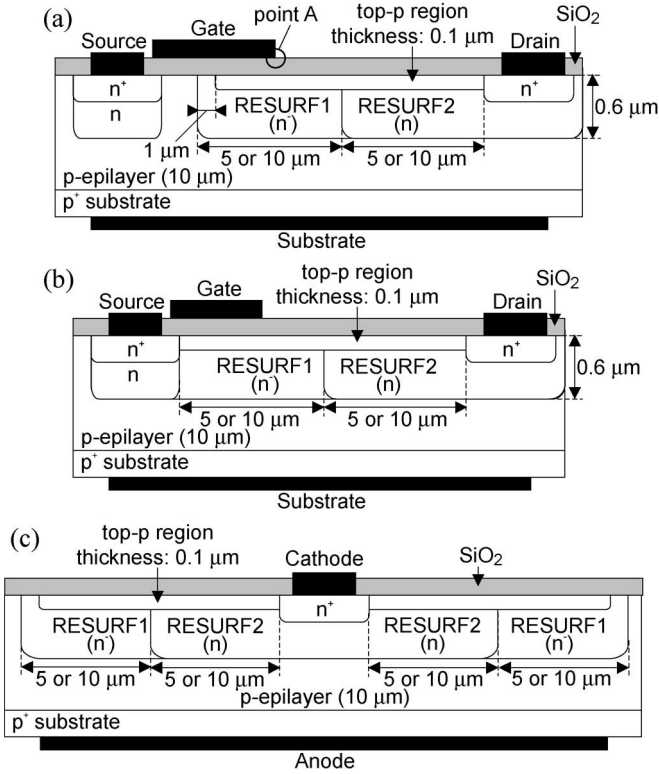


Fig. 1. Schematic structure of (a) SiC two-zone double RESURF MOSFET, (b) TEG device, and (c) RESURF diode.

dominant resistance component is the drift resistance. The drift resistance of RESURF MOSFETs was estimated from that of TEG devices with the same RESURF1, RESURF2, and top-p doses as fabricated RESURF MOSFETs in this paper.

Fig. 1(c) shows the structure of a RESURF diode fabricated in this paper. The structure of RESURF diodes is similar to that of fabricated RESURF MOSFETs but without source region and gate electrode. Thus, breakdown voltage of RESURF diodes corresponds to that of RESURF MOSFETs when the breakdown takes place in SiC (not in the gate oxide).

III. DEVICE SIMULATION FOR STRUCTURE OPTIMIZATION

In order to achieve both low ON resistance and high breakdown voltage, the RESURF and top-p doses for SiC double RESURF MOSFETs have been optimized by using a 2-D device simulator (ISE-DESSIS). In the simulation, the structure of two-zone double RESURF MOSFETs with a long drift length of 20 μm (RESURF1 and RESURF2 lengths are 10 μm each) shown in Fig. 1(a) was employed, and the RESURF1, RESURF2, and top-p doses (D_{RES1} , D_{RES2} , and D_{TP} , respectively) were varied. The acceptor concentration of a 10- μm -thick p-epilayer was fixed at $7.5 \times 10^{15} \text{ cm}^{-3}$, and a channel length of 3 μm and a gate oxide thickness of 70 nm were used. The breakdown of devices was defined when the maximum electric field in SiC exceeds 3 MV/cm or that in SiO₂ becomes higher than 10 MV/cm.

Fig. 2(a) shows the RESURF2 dose (D_{RES2}) dependence of breakdown voltage (V_B) at a fixed *net* RESURF1 dose

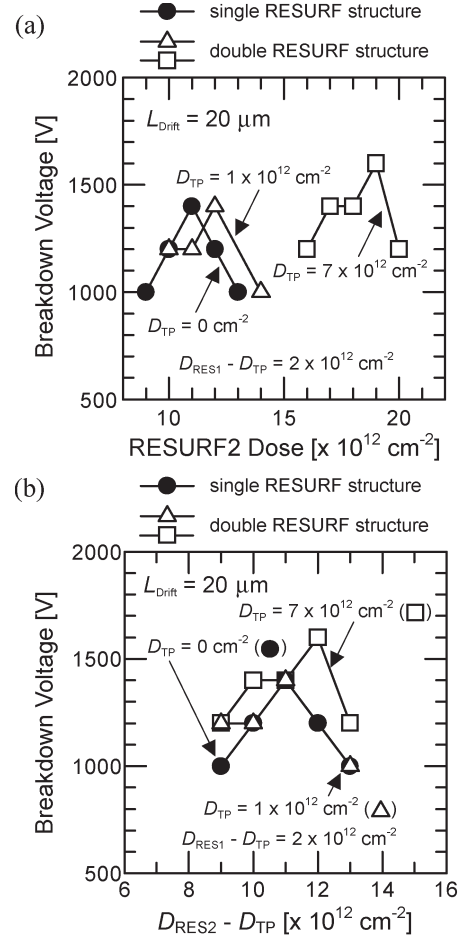


Fig. 2. (a) RESURF2 dose (D_{RES2}) and (b) *net* RESURF2 dose ($D_{\text{RES2}} - D_{\text{TP}}$) dependences of the breakdown voltage simulated for 4H-SiC RESURF MOSFETs with a drift length of 20 μm . Closed circles denote the breakdown voltage of SiC two-zone single RESURF MOSFETs, and open symbols denote that of SiC two-zone double RESURF MOSFETs. In both cases, the *net* RESURF1 dose ($D_{\text{RES1}} - D_{\text{TP}}$) is fixed at $2 \times 10^{12} \text{ cm}^{-2}$.

($D_{\text{RES1}} - D_{\text{TP}}$) of $2 \times 10^{12} \text{ cm}^{-2}$. The closed circles denote the breakdown voltage of SiC two-zone single RESURF MOSFETs (without double RESURF structure), the open triangles denote that of SiC two-zone double RESURF MOSFETs with a top-p dose of $1 \times 10^{12} \text{ cm}^{-2}$, and the open boxes denote that of SiC two-zone double RESURF MOSFETs with a top-p dose of $7 \times 10^{12} \text{ cm}^{-2}$. From Fig. 2(a), the simulated RESURF MOSFETs show a peak breakdown voltage at a certain RESURF2 dose. Fig. 2(b) shows the relationship between *net* RESURF2 dose ($D_{\text{RES2}} - D_{\text{TP}}$) and breakdown voltage. From this figure, breakdown voltage over 1.2 kV is predicted at a *net* RESURF2 dose ($D_{\text{RES2}} - D_{\text{TP}}$) of 10–12 $\times 10^{12} \text{ cm}^{-2}$ regardless of the top-p dose. The breakdown voltage also depends on the *net* RESURF1 dose (not shown). The simulated breakdown voltage was mainly determined not by the individual doses but by the *net* RESURF1 and *net* RESURF2 doses ($D_{\text{RES1}} - D_{\text{TP}}$ and $D_{\text{RES2}} - D_{\text{TP}}$, respectively). This result indicates that the ON resistance can be reduced by increasing the RESURF1, RESURF2, and top-p doses while keeping high breakdown voltage, as far as both the *net* RESURF1 and *net* RESURF2 doses are kept at the optimum values.

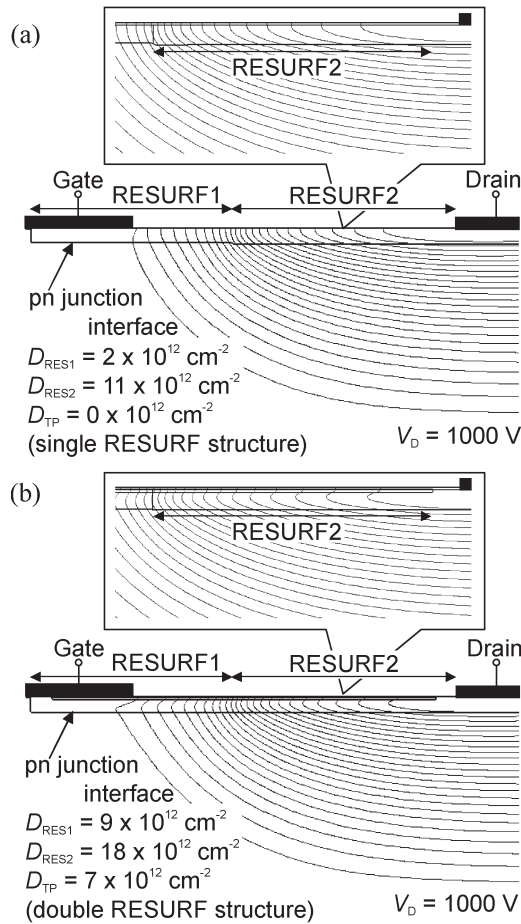


Fig. 3. Equipotential lines for 4H-SiC (a) single RESURF MOSFET and (b) double RESURF MOSFET. A drain voltage of 1000 V is applied. The step for equipotential lines is 40 V. The magnified plots of RESURF2 region in both MOSFETs are also shown. Although the individual doses are different, the *net* RESURF1 and *net* RESURF2 doses are the same, which are 2×10^{12} and 11×10^{12} cm^{-2} , respectively.

Fig. 3 exhibits the equipotential lines for single RESURF MOSFET [Fig. 3(a)] and double RESURF MOSFET [Fig. 3(b)] at a drain voltage of 1000 V with zero-gate bias, and Fig. 4 shows the electric field distribution in the RESURF region near the SiO_2/SiC interface for single and double RESURF MOSFETs. Fig. 3 includes the magnified plots of RESURF2 region in both MOSFETs. In Figs. 3 and 4, the single RESURF MOSFET has a RESURF1 dose of 2×10^{12} cm^{-2} and a RESURF2 dose of 11×10^{12} cm^{-2} . In the case of double RESURF MOSFET, a RESURF1 dose of 9×10^{12} cm^{-2} , a RESURF2 dose of 18×10^{12} cm^{-2} , and a top-p dose of 7×10^{12} cm^{-2} are employed. Although the RESURF1 and RESURF2 doses of double RESURF MOSFET are much higher than those of the single RESURF MOSFET, difference in electric potential distribution is very small between single and double RESURF MOSFETs (Fig. 3). This result originates from that the *net* RESURF1 and *net* RESURF2 doses are the same, 2×10^{12} cm^{-2} ($D_{\text{RES1}} - D_{\text{TP}}$) and 11×10^{12} cm^{-2} ($D_{\text{RES2}} - D_{\text{TP}}$), respectively, for these MOSFETs. Since the “net space charge” is the same for these devices due to charge compensation, the equipotential lines for the double RESURF MOSFET are similar to those for the single RESURF

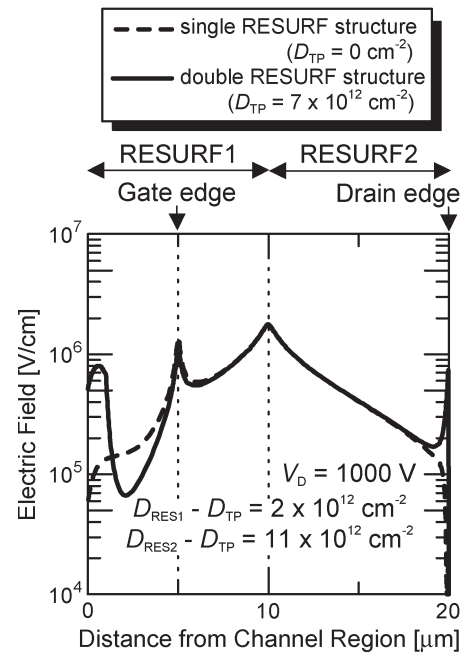


Fig. 4. Electric field distribution in the RESURF region near the SiO_2/SiC interface from the edge of channel to the drain for single and double RESURF MOSFETs. A drain voltage of 1000 V is applied. The *net* RESURF1 and *net* RESURF2 doses are fixed at 2×10^{12} and 11×10^{12} cm^{-2} , respectively. The top-p dose (D_{TP}) for single RESURF MOSFET is 0 cm^{-2} and that for double RESURF MOSFET is 7×10^{12} cm^{-2} .

MOSFET. In Fig. 4, the electric field near the channel region (about $1 \mu\text{m}$ from the channel region) of the double RESURF MOSFET is higher than that of single RESURF MOSFET. The reason why the high electric field is obtained near the channel region in the double RESURF MOSFET is that the relatively high electric potential region, compared with single RESURF MOSFET, is extended from the drain region due to its high RESURF doses. In the most of the region, the electric field distribution for the double RESURF MOSFET is comparable with that for the single RESURF MOSFET in spite of high RESURF doses. The top-p region suppresses the increase of electric field at the SiO_2/SiC interface.

As previously mentioned, it is interesting to note that the double RESURF structure is also effective in suppressing the oxide breakdown in addition to reduction of drift resistance. The top-p region in the double RESURF structure protects the gate oxide from high electric field in the blocking state because the electric potential at the MOS interface is reduced by the existence of top-p/RESURF junction. The relationship between gate oxide field at the gate edge [point A in Fig. 1(a)] and top-p dose is shown in Fig. 5. In this figure, the *net* RESURF1 and *net* RESURF2 doses are fixed at 2×10^{12} cm^{-2} and 11×10^{12} cm^{-2} , respectively. Closed circle denotes the single RESURF MOSFET ($D_{\text{TP}} = 0 \text{ cm}^{-2}$), and open circles denote the double RESURF MOSFETs ($D_{\text{TP}} > 0 \text{ cm}^{-2}$). A drain voltage of 1000 V is applied with zero-gate bias. As shown in Fig. 5, the gate oxide field at the gate edge is remarkably decreased by increasing the top-p dose.

From the simulation, the optimum *net* RESURF1 and *net* RESURF2 doses for 4H-SiC two-zone double RESURF MOSFETs with a drift length of $20 \mu\text{m}$ could be estimated to

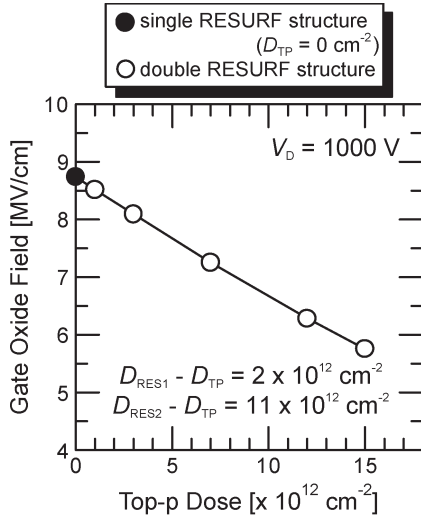


Fig. 5. Top-p dose dependence of gate oxide field at gate edge [point A in Fig. 1(a)]. Closed circle denotes the single RESURF MOSFET, and open circles denote the double RESURF MOSFETs. The *net* RESURF1 and *net* RESURF2 doses are fixed at 2×10^{12} and 11×10^{12} cm^{-2} , respectively. A drain voltage of 1000 V is applied with zero-gate bias.

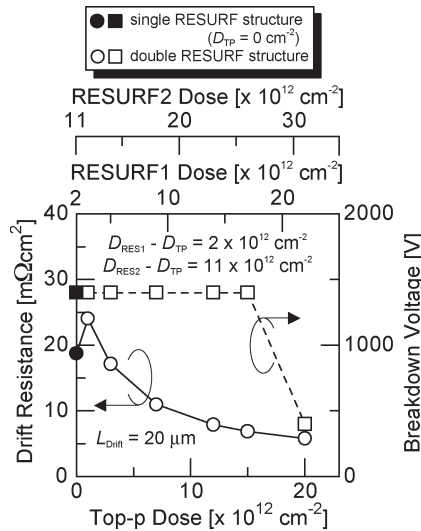


Fig. 6. Top-p dose dependence of drift resistance and breakdown voltage for the simulated 4H-SiC RESURF MOSFETs with a drift length of $20 \mu\text{m}$. Open and closed circles represent the drift resistance, and the open and closed boxes represent the breakdown voltage. Closed symbols denote the characteristics of single RESURF MOSFETs, and open symbols denote those of double RESURF MOSFETs. The *net* RESURF1 and *net* RESURF2 doses are fixed at 2×10^{12} and 11×10^{12} cm^{-2} , respectively. The RESURF1 and RESURF2 doses, to keep the optimum *net* doses, are indicated at the top of the plot.

be 2×10^{12} cm^{-2} and 10 – 12×10^{12} cm^{-2} , respectively. Fig. 6 shows the top-p dose dependence of breakdown voltage and drift resistance simulated for RESURF MOSFETs with a drift length of $20 \mu\text{m}$. The simulated MOSFETs shown in Fig. 6 have an optimum *net* RESURF1 dose of 2×10^{12} cm^{-2} and an optimum *net* RESURF2 dose of 11×10^{12} cm^{-2} . The RESURF1 and RESURF2 doses to keep the optimum *net* doses are also shown in the upper axis of Fig. 6. From Fig. 6, the advantage of double RESURF structure over single RESURF structure becomes clear. The drift resistance can be reduced to lower than $10 \text{ m}\Omega \cdot \text{cm}^2$ by increasing the RESURF1, RESURF2,

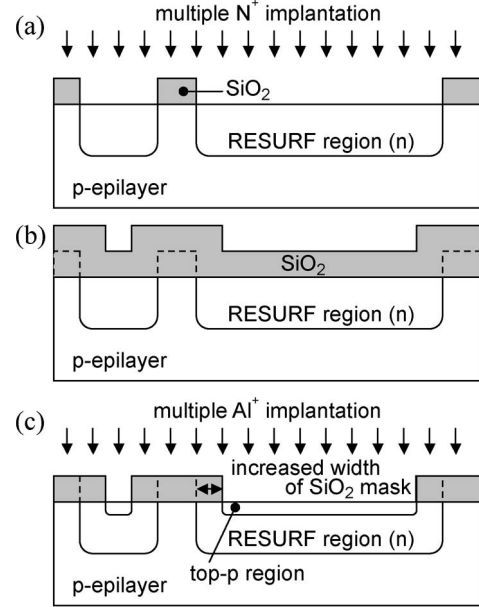


Fig. 7. Schematic flow of a self-aligned process employed in this paper. After (a) multiple N^+ implantation, (b) SiO_2 was deposited by PECVD. Then, (c) SiO_2 film was etched by RIE, and multiple Al^+ implantation was carried out through SiO_2 mask with increased width to form the top-p region.

and top-p doses (D_{RES1} , D_{RES2} , and D_{TP}) while keeping the same *net* RESURF1 ($D_{\text{RES1}} - D_{\text{TP}}$) and *net* RESURF2 ($D_{\text{RES2}} - D_{\text{TP}}$) doses. The authors have, however, found that breakdown voltage is decreased when the top-p dose is too high. For example, when the RESURF1, RESURF2, and top-p doses are 22×10^{12} cm^{-2} , 31×10^{12} cm^{-2} , and 20×10^{12} cm^{-2} (*net* RESURF1 and *net* RESURF2 doses are “optimum,” 2×10^{12} cm^{-2} and 11×10^{12} cm^{-2}), respectively, the breakdown voltage is reduced to about 500 V because electric field crowding takes place at top-p/drain and/or top-p/RESURF junction. In the simulation, MOSFETs with the optimum *net* RESURF1 and *net* RESURF2 doses exhibit high breakdown voltage over 1.2 kV when the top-p dose is kept below 15×10^{12} cm^{-2} .

IV. DEVICE FABRICATION

Double RESURF MOSFETs, TEG devices, and RESURF diodes were fabricated on $10\text{-}\mu\text{m}$ -thick p-type 4H-SiC (0001) epilayers with an acceptor concentration of 7×10^{15} cm^{-3} . The top-p region of double RESURF MOSFETs was formed by a self-aligned process shown in Fig. 7. The self-aligned process begins with the deposition of about $1.5\text{-}\mu\text{m}$ -thick SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). The deposited SiO_2 was patterned by reactive ion etching (RIE) with a $\text{CF}_4\text{-H}_2$ chemistry. Multiple N^+ implantation was carried out at room temperature (RT) to form a $0.6\text{-}\mu\text{m}$ -deep RESURF1 region [Fig. 7(a)]. The total implant dose of N^+ (RESURF1 dose: D_{RES1}) was varied in the range from 2×10^{12} to 10×10^{12} cm^{-2} . After the multiple N^+ implantation, about $1.5\text{-}\mu\text{m}$ -thick SiO_2 was deposited by PECVD without removal of the initial SiO_2 mask [Fig. 7(b)]. Then, the whole area of SiO_2 film was etched by RIE to expose the SiC surface. The SiO_2 mask with an increased width (about $1 \mu\text{m}$ on each side) can be employed as a mask for subsequent top-p implantation without

additional lithographic process. The top-p region was formed by multiple Al⁺ implantation at RT [Fig. 7(c)]. The total implant dose of Al⁺ (top-p dose: D_{TP}) was varied in the range from 3×10^{12} to 7×10^{12} cm⁻². By using the self-aligned process, the risk that the channel region connects to the top-p region can be eliminated. The RESURF2 region was also formed by multiple N⁺ implantation at RT, with a box profile of the same junction depth as the RESURF1 region by using a renewed SiO₂ mask. The total implant dose of N⁺ (RESURF2 dose: D_{RES2}) was varied in the range from 9×10^{12} to 18×10^{12} cm⁻². High-dose (5×10^{15} cm⁻²) P⁺ implantation at 300 °C was employed to form the source/drain regions. After these ion implantations, high-temperature annealing was performed at 1700 °C for 20 min with a carbon cap to suppress surface roughening [23]. Nearly all of the implanted N and Al atoms are activated (activation ratio > 95%) through the present annealing procedure [24], [25]. After RCA cleaning, thermal oxidation was carried out in dry N₂O (10% diluted in N₂) ambience at 1300 °C [17], [26], followed by postoxidation annealing in a N₂ ambience at 1300 °C for 30 min. The gate oxide thickness (d) was about 74 nm. Al was used as the gate metal and the contact metal for the source/drain region, and Ti/Al was evaporated on the backside for the substrate contact. All contacts except the gate metal were annealed at 600 °C for 10 min. The typical channel length (L) and width (W) of RESURF MOSFETs were 1–5 and 200 μm, respectively. In the TEG device, the channel length was 0 μm and the width was 200 μm. Two types of RESURF MOSFETs which have a total drift length (L_{Drift}) of 10 or 20 μm have been fabricated.

It is not clear how much the distance between top-p and channel regions affects the device performance. However, the qualitative explanation is described as follows. When the distance is too long (e.g., > 5 μm), the device may exhibit low breakdown voltage because the top-p region cannot protect the gate oxide, as discussed previously. On the other hand, when the distance is too short (e.g., < 0.2 μm), the resistance of JFET located at the region between the channel and top-p regions may become high. The quantitative influence on device characteristics, for example, breakdown voltage and ON resistance, is currently under investigation.

The gate characteristic of test MOSFET without RESURF region processed on the same wafer is shown in Fig. 8. The channel length and width of the test MOSFET are 50 and 200 μm, respectively. Fig. 8 also shows the relationship between the channel mobility and the gate voltage. The effective channel mobility is approximately 17 cm²/V · s, and the threshold voltage was estimated to be 7.4 V from the gate characteristics.

V. EXPERIMENTAL RESULTS AND DISCUSSION

The relationship between the drift resistance (R_{Drift}) and the RESURF1 dose in the fabricated MOSFETs with a long drift length of 20 μm is shown in Fig. 9. The drift resistance was estimated by the TEG devices with the same doses as RESURF MOSFETs. In Fig. 9, the *net* RESURF1 and *net* RESURF2 doses were fixed at 2×10^{12} and 9×10^{12} cm⁻², respectively, and the RESURF1, RESURF2, and top-p doses were changed. For example, when the RESURF1 dose (D_{RES1})

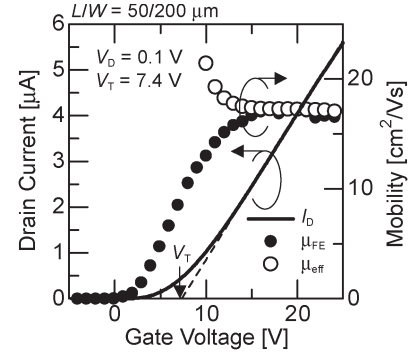


Fig. 8. Gate characteristics of test MOSFET without RESURF region, processed on the same wafer, in the linear region. The channel length and width are 50 and 200 μm, respectively. The relationship between mobility and gate voltage is also shown. Solid line denotes the drain current, and closed and open circles mean the field effect mobility (μ_{FE}) and effective channel mobility (μ_{eff}), respectively.

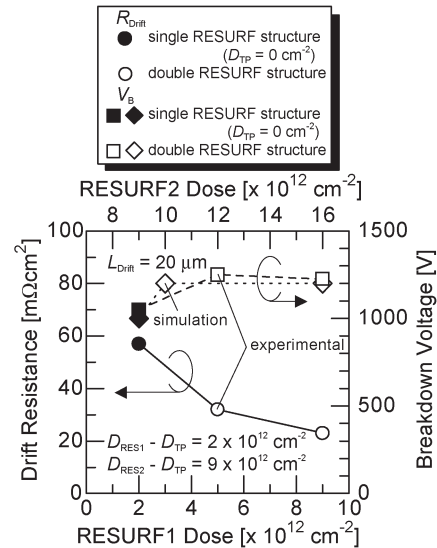


Fig. 9. RESURF1 dose dependence of drift resistance and breakdown voltage for the fabricated 4H-SiC RESURF MOSFETs with a drift length of 20 μm. The breakdown voltage experimentally obtained was compared with the simulated results. Open and closed circles represent the drift resistance, open and closed boxes represent the breakdown voltage experimentally obtained, and open and closed rhombuses represent the simulated breakdown voltage. Closed symbols denote the characteristics of single RESURF MOSFETs, and open symbols denote those of double RESURF MOSFETs.

was increased, the top-p dose (D_{TP}) was also increased to keep the fixed *net* RESURF1 dose ($D_{RES1} - D_{TP}$). The RESURF1 dose dependence of the breakdown voltage (V_B) obtained from the fabricated and simulated RESURF MOSFETs is also shown in Fig. 9. Although the drift resistance in the single RESURF MOSFET (closed circle in Fig. 9) was 57 mΩ · cm², the drift resistance was as low as 23 mΩ · cm² by employing the double RESURF structure with the highest doses. The fabricated two-zone RESURF MOSFETs with double RESURF structure exhibited higher breakdown voltage than that with single RESURF structure (open boxes versus closed box in Fig. 9). The breakdown voltages of single and double RESURF MOSFETs were 1050 and over 1200 V, respectively. In the double RESURF MOSFETs, high electric potential region is easily extended from the drain region when high drain voltage is

TABLE I
BREAKDOWN VOLTAGE OF RESURF MOSFETs AND
RESURF DIODES WITH A LONG DRIFT LENGTH OF
20 μm ($V_{B,FET}$ AND $V_{B,D}$, RESPECTIVELY)

structure	D_{RES1} [cm^{-2}]	D_{RES2} [cm^{-2}]	D_{TP} [cm^{-2}]	$V_{B,FET}$ [V]	$V_{B,D}$ [V]
two-zone RESURF	2×10^{12}	9×10^{12} 11×10^{12}	0	1060 1190	1070 1180
two-zone double RESURF	5×10^{12} 9×10^{12}	12×10^{12} 16×10^{12} 18×10^{12}	3×10^{12} 7×10^{12}	1280 1050 1260 1380	1200 1140 1380 1330

TABLE II
BREAKDOWN VOLTAGE OF RESURF MOSFETs AND
RESURF DIODES WITH A SHORT DRIFT LENGTH
OF 10 μm ($V_{B,FET}$ AND $V_{B,D}$, RESPECTIVELY)

structure	D_{RES1} [cm^{-2}]	D_{RES2} [cm^{-2}]	D_{TP} [cm^{-2}]	$V_{B,FET}$ [V]	$V_{B,D}$ [V]
two-zone RESURF	2×10^{12}	9×10^{12} 11×10^{12}	0	780 920	830 970
two-zone double RESURF	5×10^{12} 9×10^{12}	12×10^{12} 16×10^{12} 18×10^{12}	3×10^{12} 7×10^{12}	700 710 760 760	1040 1010 1160 1230

applied because the RESURF1 and RESURF2 doses are higher than that of the single RESURF MOSFET, and the change in electric potential near the drain edge becomes gradual. Thus, the electric field crowding at the drain edge is relaxed, and the breakdown voltage is increased. The breakdown voltage experimentally obtained was consistent with the value expected by device simulation. In the case of RESURF MOSFETs with a short drift length of 10 μm , the drift resistance was reduced from 26 to 10 $\text{m}\Omega \cdot \text{cm}^2$ by employing double RESURF structure, and the breakdown voltage was about 700 V (not shown).

The authors have also fabricated RESURF diodes shown in Fig. 1(c). The breakdown voltage obtained from fabricated RESURF MOSFETs and diodes ($V_{B,FET}$ and $V_{B,D}$, respectively) is summarized in Tables I and II. Tables I and II show the results of devices with long and short drift lengths, respectively. From Table I, the breakdown voltage of RESURF MOSFETs with a long drift length of 20 μm is similar to that of the RESURF diodes because the breakdown occurred in SiC (not in the gate oxide). On the other hand, in the case of short drift length, RESURF MOSFETs exhibit lower breakdown voltage than RESURF diodes. This result arises from that breakdown which took place in the gate oxide (not in SiC). The breakdown voltage of RESURF MOSFETs with short drift length may be

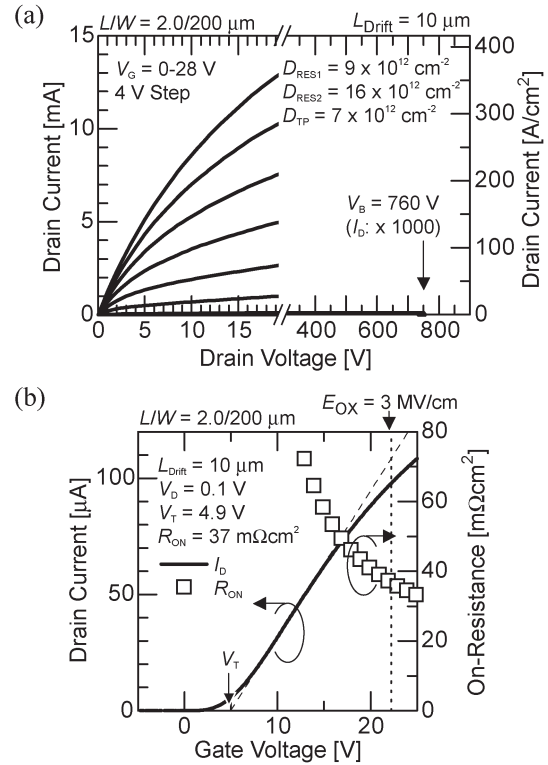


Fig. 10. (a) Output and (b) gate characteristics of a fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a short drift length of 10 μm . The device with short drift length exhibits a breakdown voltage of 760 V and an ON resistance of 37 $\text{m}\Omega \cdot \text{cm}^2$ at an oxide field of 3 MV/cm.

improved by optimizing the device structure, for example, gate overlapping length and individual doses.

Figs. 10 and 11 show the output and gate characteristics of the fabricated SiC two-zone double RESURF MOSFETs with a short drift length of 10 μm and a long drift length of 20 μm , respectively. The channel length is about 2 μm . In Fig. 10, the MOSFET with short drift length has a RESURF1 dose of $9 \times 10^{12} \text{ cm}^{-2}$, a RESURF2 dose of $16 \times 10^{12} \text{ cm}^{-2}$, and a top-dose of $7 \times 10^{12} \text{ cm}^{-2}$. In the case of RESURF MOSFET with the short drift length [Fig. 10(a)], a breakdown voltage of 760 V was obtained, and the breakdown occurred at the gate oxide. The relationship between the gate voltage and the ON resistance is also shown in Fig. 10(b). In the ON state [Fig. 10(b)], the MOSFET exhibits an ON resistance of 37 $\text{m}\Omega \cdot \text{cm}^2$ at an oxide field (E_{OX}) of 3 MV/cm. From the characteristics of TEG devices, the drift resistance and channel resistance were estimated to be 10 and 26 $\text{m}\Omega \cdot \text{cm}^2$, respectively. The contact resistance was obtained as about 1 $\text{m}\Omega \cdot \text{cm}^2$ from a TLM test structure. In the calculation of specific ON resistance, drain and source pads (3- μm long each) were included. From Fig. 10(b), the threshold voltage determined from the gate characteristics is 4.9 V, which is lower than that of a test MOSFET shown in Fig. 8 (7.4 V). This decrease in threshold voltage can be attributed to the short-channel effects [27], because the p-body (epilayer) is lightly doped. The present two-zone double RESURF MOSFET with short drift length exhibits the lowest ON resistance in any 600-V class lateral MOSFETs ever reported.

On the other hand, in the two-zone double RESURF MOSFET with a long drift length of 20 μm (Fig. 11), which has

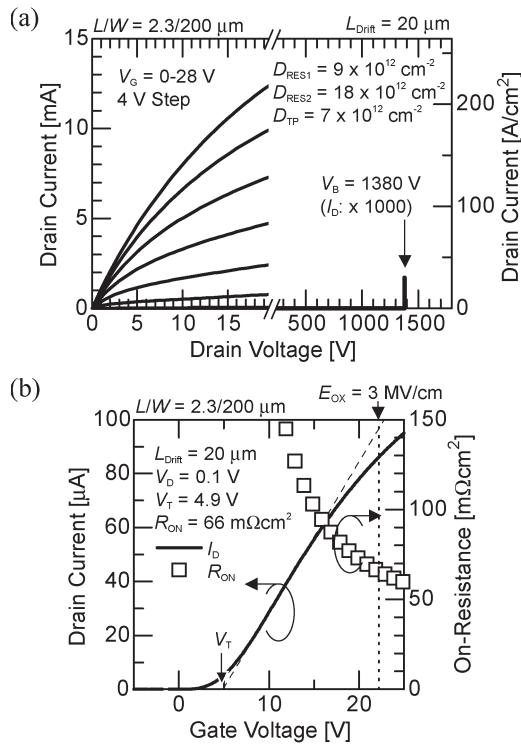


Fig. 11. (a) Output and (b) gate characteristics of a fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a long drift length of 20 μm . The device with long drift length exhibits a high breakdown voltage of 1380 V and a low ON resistance of 66 $\text{m}\Omega \cdot \text{cm}^2$ at an oxide field of 3 MV/cm.

a RESURF1 dose of $9 \times 10^{12} \text{ cm}^{-2}$, a RESURF2 dose of $18 \times 10^{12} \text{ cm}^{-2}$, and a top-p dose of $7 \times 10^{12} \text{ cm}^{-2}$, breakdown of this MOSFET took place not in the gate oxide but in SiC when a high drain voltage of 1380 V was applied. From Fig. 11(b), the MOSFET with the long drift length exhibited a threshold voltage of 4.9 V and a specific ON resistance of 66 $\text{m}\Omega \cdot \text{cm}^2$ (including a drift, channel, and contact resistances of 24, 41, and 1 $\text{m}\Omega \cdot \text{cm}^2$, respectively) at an oxide field of 3 MV/cm. The highest figure-of-merit (V_B^2/R_{ON}) of 29 MW/cm^2 among any SiC lateral MOSFETs [7], [9]–[14], [20] and Si lateral superjunction MOSFETs [28] could be realized by employing a two-zone double RESURF structure.

VI. CONCLUSION

The authors have simulated and fabricated 4H-SiC two-zone double RESURF MOSFETs for the first time. From the device simulation, the breakdown voltage in double RESURF MOSFETs is mainly determined by the *net* RESURF1 and *net* RESURF2 doses. The optimum *net* RESURF1 and *net* RESURF2 doses in two-zone double RESURF MOSFETs with a drift length of 20 μm are 2×10^{12} and $10\text{--}12 \times 10^{12} \text{ cm}^{-2}$, respectively. The ON resistance of double RESURF MOSFETs is reduced by increasing the individual doses while keeping the optimum *net* RESURF1 and *net* RESURF2 doses. The double RESURF structure is also effective to suppress gate oxide breakdown, compared with the single RESURF structure, owing to a reduced electric field in the gate oxide.

After device simulation for dose optimization, the authors have fabricated two-zone double RESURF MOSFETs by using

a self-aligned process. The fabricated 4H-SiC (0001) two-zone double RESURF MOSFET with a drift length of 10 μm exhibited a breakdown voltage of 760 V and an ON resistance of 37 $\text{m}\Omega \cdot \text{cm}^2$ (including a drift resistance of 10 $\text{m}\Omega \cdot \text{cm}^2$). The fabricated double RESURF MOSFET with a long drift length of 20 μm exhibited a high breakdown voltage of 1380 V and a low ON resistance of 66 $\text{m}\Omega \cdot \text{cm}^2$ (including a drift resistance of 24 $\text{m}\Omega \cdot \text{cm}^2$). The figure-of-merit (V_B^2/R_{ON}) of this device is 29 MW/cm^2 , which is the best performance among any lateral MOSFETs ever reported. By employing the double RESURF structure, the drift resistance could be reduced to 50% or less, and the breakdown voltage was slightly increased. The double RESURF structure is attractive to achieve both high breakdown voltage and low ON resistance.

REFERENCES

- [1] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and prospects for SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 658–664, Apr. 2002.
- [2] D. Peters, R. Schörner, P. Friedrichs, and D. Stephani, "4H-SiC power MOSFET blocking 1200 V with a gate technology compatible with industrial applications," *Mater. Sci. Forum*, vol. 433–436, pp. 769–772, 2003.
- [3] S. H. Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, and A. R. Hefner, "10-kV, 123- $\text{m}\Omega \cdot \text{cm}^2$ 4H-SiC power DMOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 556–558, Aug. 2004.
- [4] M. Marin, A. Saha, and J. A. Cooper, "A self-aligned process for high-voltage, short-channel vertical DMOSFETs in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1721–1725, Oct. 2004.
- [5] S. Harada, M. Kato, M. Okamoto, T. Yatsuo, K. Fukuda, and K. Arai, "Low ON-resistance in inversion channel IEMOSFET formed on 4H-SiC C-face substrate," in *Proc. Int. Symp. Power Semicond. Devices and ICs*, 2006, pp. 125–128.
- [6] N. Miura, K. Fujihira, Y. Nakao, T. Watanabe, Y. Tarui, S. Kinouchi, M. Imaizumi, and T. Oomori, "Successful development of 1.2 kV 4H-SiC MOSFETs with the very low ON-resistance of 5 $\text{m}\Omega \cdot \text{cm}^2$," in *Proc. Int. Symp. Power Semicond. Devices and ICs*, 2006, pp. 261–264.
- [7] K. Chatty, S. Banerjee, T. P. Chow, and R. J. Gutmann, "High-voltage lateral RESURF MOSFETs on 4H-SiC," *IEEE Electron Device Lett.*, vol. 21, no. 7, pp. 356–358, Jul. 2000.
- [8] J. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF Devices)," in *IEDM Tech. Dig.*, 1979, pp. 238–241.
- [9] S. Banerjee, K. Chatty, T. P. Chow, and R. J. Gutmann, "Improved high-voltage lateral RESURF MOSFETs in 4H-SiC," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 209–211, May 2001.
- [10] S. Banerjee, T. P. Chow, and R. J. Gutmann, "1300-V 6H-SiC lateral MOSFETs with two RESURF zones," *IEEE Electron Device Lett.*, vol. 23, no. 10, pp. 624–626, Oct. 2002.
- [11] W. Wang, S. Banerjee, T. P. Chow, and R. J. Gutmann, "930-V 170 $\text{m}\Omega \cdot \text{cm}^2$ lateral two-zone RESURF MOSFETs in 4H-SiC with NO annealing," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 185–187, Apr. 2004.
- [12] T. Kimoto, H. Kosugi, J. Suda, Y. Kanzaki, and H. Matsunami, "Design and fabrication of RESURF MOSFETs on 4H-SiC (0001), (1120), and 6H-SiC (0001)," *IEEE Electron Devices*, vol. 52, no. 1, pp. 112–117, Jan. 2005.
- [13] M. Okamoto, S. Suzuki, M. Kato, T. Yatsuo, and K. Fukuda, "Lateral RESURF MOSFET fabricated on 4H-SiC (0001) C-face," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 405–407, Jun. 2004.
- [14] S. Suzuki, S. Harada, T. Yatsuo, R. Kosugi, J. Senzaki, and K. Fukuda, "4H-SiC lateral RESURF MOSFET with a buried channel structure," *Mater. Sci. Forum*, vol. 433–436, pp. 753–756, 2003.
- [15] P. Jamet, S. Dimitrijevic, and P. Tanner, "Effects of nitridation in gate oxides grown on 4H-SiC," *J. Appl. Phys.*, vol. 90, no. 10, pp. 5058–5063, Nov. 2001.
- [16] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in Nitric Oxide," *IEEE Electron Device Lett.*, vol. 22, no. 4, pp. 176–178, Apr. 2001.

- [17] L. A. Lipkin, M. K. Das, and J. W. Palmour, "N₂O processing improves the 4H-SiC: SiO₂ interface," *Mater. Sci. Forum*, vol. 389–393, pp. 985–988, 2002.
- [18] K. Fukuda, M. Kato, K. Kojima, and J. Senzaki, "Effect of gate oxidation method on electrical properties of metal-oxide-semiconductor field-effect transistors fabricated on 4H-SiC (0001) face," *Appl. Phys. Lett.*, vol. 84, no. 12, pp. 2088–2090, Mar. 2004.
- [19] H. Yano, H. Hirao, T. Kimoto, H. Matsunami, K. Asano, and Y. Sugawara, "High channel mobility in inversion layers of 4H-SiC MOSFET's by utilizing (1120) face," *IEEE Electron Device Lett.*, vol. 20, no. 12, pp. 611–613, Dec. 1999.
- [20] T. Kimoto, H. Kawano, and J. Suda, "1330 V, 67 mΩ · cm² 4H-SiC (0001) RESURF MOSFET," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 649–651, Sep. 2005.
- [21] H. M. J. Vaes and J. A. Appels, "HV high-current lateral devices," in *IEDM Tech. Dig.*, 1980, pp. 87–90.
- [22] T. Fujihira, "Theory of semiconductor superjunction devices," *Jpn. J. Appl. Phys.*, vol. 36, no. 10, pp. 6254–6262, Oct. 1997.
- [23] Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, "Electronic behaviors of high-dose phosphorus-ion implanted 4H-SiC (0001)," *J. Appl. Phys.*, vol. 96, no. 1, pp. 224–228, Jul. 2004.
- [24] M. Laube, F. Schmid, G. Pensl, G. Wagner, M. Linnarsson, and M. Maier, "Electrical activation of high concentrations of N⁺ and P⁺ ions implanted into 4H-SiC," *J. Appl. Phys.*, vol. 92, no. 1, pp. 549–554, Jul. 2002.
- [25] Y. Negoro, T. Kimoto, and H. Matsunami, "Carrier compensation near tail region in aluminum- or boron-implanted 4H-SiC (0001)," *J. Appl. Phys.*, vol. 98, no. 4, pp. 043 709-1–043 709-7, Aug. 2005.
- [26] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, and H. Matsunami, "Interface properties of metal-oxide-semiconductor structures on 4H-SiC (0001) and (1120) formed by N₂O oxidation," *Jpn. J. Appl. Phys.*, vol. 44, no. 3, pp. 1213–1218, 2005.
- [27] M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto, "Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs," *IEEE Electron Devices*, vol. 52, no. 9, pp. 1954–1962, Sep. 2005.
- [28] M. Rüb, M. Bär, G. Deml, H. Kapels, M. Schmitt, S. Sedlmaier, C. Tolksdorf, and A. Willmeroth, "A 600 V 8.7 Ωmm² lateral superjunction transistor," in *Proc. Int. Symp. Power Semicond. Devices and ICs*, 2006, pp. 305–308.



Masato Noborio (S'06) was born in Nara, Japan, in 1981. He received the B.E. and M.E. degrees in electrical and electronic engineering from Kyoto University, Kyoto, Japan, in 2004 and 2006, respectively. He is currently working toward a Ph.D. degree in the Department of Electronic Science and Engineering, Kyoto University.

His research interests include short-channel effects in SiC MOSFETs, device simulation for SiC devices, designing and fabrication of SiC lateral power MOSFETs, and device processes.



Jun Suda was born in Ashikaga, Japan, in 1969. He received the B.E., M.E., and Ph.D. degrees from Kyoto University, Kyoto, Japan.

From 1992 to 1997, he worked on the growth of ZnSe-based semiconductors by molecular-beam epitaxy and the characterization of ZnMgSSe strained quantum well structures for optoelectronic applications. In 1997, he began researching on group-III nitride semiconductors (III-N) and SiC as a Research Associate at Kyoto University. He is currently a Lecturer in the Department of Electronics Science and Engineering, Kyoto University. His research interests include heteroepitaxial growth of III-N, functional integration of III-N and SiC materials by precise control of the heterointerface, design of wide bandgap semiconductor devices, and characterization of device structure by scanning-probe microscopy. He has authored or coauthored over 50 publications in peer-reviewed journals and international conferences, and he is the holder of 12 pending patents.

Dr. Suda is a member of The Material Research Society, Japan Society of Applied Physics, and Japanese Association for Crystal Growth.



Tsunenobu Kimoto (M'03–SM'06) received the B.E. and M.E. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1986 and 1988, respectively, and the Ph.D. degree in 1996, based on his work on SiC epitaxial growth, characterization, and high-voltage diodes.

He was with Sumitomo Electric Industries, Ltd., in April 1988, where he conducted research on amorphous Si solar cells and semiconducting diamond material. In 1990, he started his academic career as a Research Associate at Kyoto University. From September 1996 to August 1997, he was a Visiting Scientist at Linköping University, Sweden, where he was involved in fast epitaxy of SiC and high-voltage Schottky diodes. He is currently a Professor in the Department of Electronic Science and Engineering, Kyoto University. His main research activities include SiC epitaxial growth, optical and electrical characterization, ion implantation, MOS physics, and high-voltage devices. He has also been involved in nanoscale Si devices and novel materials for nonvolatile memory. He has published over 250 papers in scientific journals and international conference proceedings.

Dr. Kimoto is a member of Japan Society of Applied Physics, Institute of Electronics, Information, and Communication Engineers, and Institute of Electrical Engineers.