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Verification of logic circuits using Mizar and its application to an adder circuit on a radix-$2^k$SD number.

1. Introduction

To answer the request of higher performance from electric equipment, logic circuit is becoming more complicated and more large-scaled. This makes it more difficult to verify correctness of a designed circuit.

Heretofore, to verify a logical circuit, output for every possible state and input should be confirmed by simulation. However, when the scale of a circuit increases, states of circuit increases exponentially, accordingly (Example, when a circuit has 100 return wires, it has $2^{100}$ states.). So it is impossible or very difficult to complete such a simulation for large-scaled circuits.

As a new way to verify correctness of logical circuit, we express logical circuit with mathematical description (called mathematical model). The correctness of the circuits is assured when correctness of the
circuit's mathematical model is verified by a proof checker system.

A proof checker system has been used to verify correctness of proof in mathematics. It can be applied to verifying correctness of a designed circuit with the method we suggest.

In this paper, after introducing the proof checker system Mizar which is used to verify correctness of proof (Section 2), we give some definitions as a preparation for mathematics descriptions of a logical circuit (Section 3). Then, we explain how a logical circuit is described by these definitions, and how its correctness is verified by the system (Section 4). At last, as an example, we apply the method in designing the adder circuit on a radix-$2^k$SD number.

2. Proof checker system Mizar

As an attempt to reconstruct mathematical vernacular, the Mizar project started in 1973. [1]

And, it has become the most important activity in the project to develop the database of mathematics since 1989. Now, more than 2,000 definitions and 20,000 theorems are included in the increasing database.

As a characteristic of Mizar, useful verified proof is accepted by Mizar's library. Using Mizar, besides mathematical proof, a mathematical model can be verified too.

Just as a large-scale circuit can be designed as a combination of
smaller circuits which function has been verified, the correctness of a model can be showed when the model is a combination of smaller models which has been accepted by the library.

3. Preparation for mathematical description of a logical circuit

We give a relation between basic concepts of logical circuits and mathematics as follows:

(1) We think input and output signals as sets. The logic of a signal line has 2 states, 0 and 1. 0 is defined as the empty set $\emptyset$, and 1 is defined as a non-empty set.

It is described as follows at Mizar:

\[
\begin{align*}
definition let a be set; 
redefine attr a is empty; 
antonym $\emptyset$; 
end;
\end{align*}
\]

(2) We consider the expression of every possible states formed by input and output signals. It is described like this:

\[
Ss0 \text{ iff } SAND2 (\text{NOT1 } q2, \text{NOT1 } q1)
\]

(3) We define a circuit as a Boolean function of sets defined above.

For example, NOT circuit writes follows:

\[
\begin{align*}
\text{func NOT1 } a \rightarrow \text{ set equals} \\
\phi \text{ if } \emptyset \\
\text{otherwise } \{ \phi : \text{ not contradiction} \};
\end{align*}
\]
4. A new method of logic circuit's verification using Mizar system

Here, we introduce how the new method works with a simple example.

Consider a 3-bit up counter circuit. The correctness of the circuit can be guaranteed with Mizar at the following steps.

(1) Describing the input and output as sets.

(2) Defining every possible state of input and output as following with the set of step 1. (Fig. 1)

$s_0 = \text{AND3}(\text{NOT1 } q_3, \text{NOT1 } q_2, \text{NOT1 } q_1);
$s_1 = \text{AND3}(\text{NOT1 } q_3, \text{NOT1 } q_2, q_1);
$s_2, s_3, s_4, s_5, s_6, s_7$ is similar to $s_0, s_1.$

(3) Expressing the behavior of 3-bit up counter circuit with Boolean expressions as follows: (Fig. 2)

$s_{nq1} = \text{AND2}(\text{NOT1 } q_1, R)
$s_{nq2} = \text{AND2}(\text{XOR2}(q_1, q_2), R))
$s_{nq3} = \text{AND2}(\text{OR2}(\text{AND2}(q_3, \text{NOT1 } q_1), \text{AND2}(q_1, \text{XOR2}(q_2, q_3))), R)

Here, $q_1, q_2, q_3, R$ are circuit inputs and $s_{nq1}, s_{nq2}, s_{nq3}$ are outputs.

(4) Verifying the correctness of circuit by confirming its Boolean expressions' tautology using Mizar system.

$(s_{ns1} \iff \text{AND2}(s_0, R)) \& (s_{ns2} \iff \text{AND2}(s_1, R)) \& (s_{ns3} \iff \text{AND2}(s_2, R)) \& (s_{ns4} \iff \text{AND2}(s_3, R)) \& (s_{ns5} \iff \text{AND2}(s_4, R)) \& (s_{ns6} \iff \text{AND2}(s_5, R)) \& (s_{ns7} \iff \text{AND2}(s_6, R)) \& (s_{ns0} \iff \text{SOR2}(s_7, \text{NOT1 } R));

Here, $s_0, ..., s_7$ means current states and $s_{ns0}, ..., s_{ns7}$ means next states of current states.
\((\text{sns1 iff } \text{AND2(s0,R)})\) means the next state will be sns1, if and only if the current state is s0 and R is "1".

Behavior of a 3bit up counter circuit
Have 4 inputs(R,q3,q2,q1) and 3 outputs(nq3,nq2,nq1)
States change as follows:
000→001→010→011→100→101→110→111→000→
return to the initial state(000) by the reset input

Signal definitions

![Signal diagram](image)

Input signal definitions
0 0 0 → sns0 = \text{AND3(NOT1 q3, NOT1 q2, NOT1 q1)}
Output signal definitions
0 0 1 → sns1 = \text{AND3(NOT1 nq3, NOT1 nq2, nq1)}

Fig. 1 Definitions of 3bit up counter.

Definitions and proof to correctness of a 3bit up counter

![Definition diagram](image)

Needs to proof these definitions

- \((\text{sns1iff } \text{AND2(s0,R)})\)&
- \((\text{sns2 iff } \text{AND2(s1,R)})\)&
- \((\text{sns3 iff } \text{AND2(s2,R)})\)&
- \((\text{sns4 iff } \text{AND2(s3,R)})\)&
- \((\text{sns5 iff } \text{AND2(s4,R)})\)&
- \((\text{sns6 iff } \text{AND2(s5,R)})\)&
- \((\text{sns7 iff } \text{AND2(s6,R)})\)&
- \((\text{sns0 iff } \text{OR2(s7,NOT1 R)})\);

Definitions of a 3bit up counter

- \((\text{nq1 iff } \text{AND2(NOT1 q1,R)})\)&
- \((\text{nq2 iff } \text{AND2(XOR2(q1,q2),R)})\)&
- \((\text{nq3 iff } \text{AND2(OR2(AND2(q3,NOT1 q1),AND2(q1,XOR2(q2,q3))),R)})\)

Fig. 2 Definitions (cont.) and proof of correctness of 3bit up counter.
5. An application to a radix-2\textsuperscript{k}SD number coded adder circuit

Here, we apply the new method to designing an adder circuit on a radix-2\textsuperscript{k}SD number.

In a radix-2\textsuperscript{k}SD (signed-digit) coded adder circuit, calculations can be finished in a constant time no matter whether there is a ripple carry.

Here, we will verify the correctness of such a circuit of case k=2.

A designed radix-4SD number circuit and signal layouts

\[ \begin{array}{c|c|c|c}
\text{value} & x2 & x1 & x0 \\
\hline
-3 & 1 & 0 & 1 \\
-2 & 1 & 1 & 0 \\
-1 & 1 & 1 & 1 \\
0 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 \\
2 & 0 & 1 & 0 \\
3 & 0 & 1 & 1 \\
\end{array} \]

(y.s are similar)

\[ \begin{array}{c|c|c}
\text{value} & cl & c0 \\
\hline
-1 & 1 & 1 \\
0 & 0 & 0 \\
1 & 0 & 1 \\
\end{array} \]

Fig. 3 Signal layout of radix-4SD number coded adder circuit
## Outputs of PART1 which used radix-4SD number

<table>
<thead>
<tr>
<th>Value</th>
<th>w2 w1 w0 nc1 nc0</th>
<th>other expression</th>
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<tr>
<td>-6</td>
<td>1 1 0 1 1</td>
<td></td>
</tr>
<tr>
<td>-5</td>
<td>1 1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>-4</td>
<td>0 0 0 1 1</td>
<td></td>
</tr>
<tr>
<td>-3</td>
<td>0 0 1 1 1</td>
<td></td>
</tr>
<tr>
<td>-2</td>
<td>1 1 0 0 0</td>
<td>0 + -3</td>
</tr>
<tr>
<td>-1</td>
<td>1 1 1 0 0</td>
<td>-4 + 2</td>
</tr>
<tr>
<td>0</td>
<td>0 0 0 0 0</td>
<td>-4 + 1</td>
</tr>
<tr>
<td>1</td>
<td>0 0 1 0 0</td>
<td>0 + 3</td>
</tr>
<tr>
<td>2</td>
<td>0 1 0 0 0</td>
<td>4 + -3</td>
</tr>
<tr>
<td>3</td>
<td>1 1 1 0 1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0 0 1 0 1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0 1 0 0 1</td>
<td></td>
</tr>
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</table>

Several kinds numerical value expression is possible so that figure increasing number can take out a mark in SD number.

In this study, we represent numerical value by expression surrounded by a square.

Fig. 4 Definitions of radix-4SD number coded adder circuit

The correctness of a 4-SD number adder circuit is verified with the 4 steps described in former section.

First, input and output status can be defined as follows:

**INPUT STATE:**

\[(S_{x3} \text{ iff } \text{SAND3}(x_2, \text{NOT} x_1, x_0)) \&
(S_{x2} \text{ iff } \text{SAND3}(x_2, x_1, \text{NOT} x_0)) \&
(S_{x1} \text{ iff } \text{SAND3}(x_2, x_1, x_0)) \&
(S_{xz} \text{ iff } \text{SAND3}(\text{NOT} x_2, \text{NOT} x_1, \text{NOT} x_0)) \&
(S_{xp1} \text{ iff } \text{SAND3}(\text{NOT} x_2, \text{NOT} x_1, x_0)) \&
(S_{xp2} \text{ iff } \text{SAND3}(x_2, x_1, \text{NOT} x_0)) \&
(S_{xp3} \text{ iff } \text{SAND3}(\text{NOT} x_2, x_1, x_0))\]

Here, \(x_0, x_1, x_2\) express the three inputs of PART1 (Fig.3), \(S_{x3}, S_{x2}, S_{x1}, S_{xz}, S_{xp1}, S_{xp2}, S_{xp3}\) are all possible input states. The expression \(S_{x3} \text{ iff } \text{SAND3}(x_2, \text{NOT} x_1, x_0)\) means that an input state is called \(S_{x3}\) if and only if inputs \(x_2=1', x_1=0', x_0=1'\).
Sym3, Sym2, Sym1, Syz, Syp1, Syp2, Syp3 can be defined similarly.

**OUTPUT STATE:**

Output states can be defined in the same way as follows.

(Snz  iff SAND5(NOT1 nc1, NOT1 nc0, NOT1 nw2, NOT1 nw1, NOT1 nw0))
(Snp1 iff SAND5(NOT1 nc1, NOT1 nc0, NOT1 nw2, NOT1 nw1, nw0))
(Snp2 iff SAND5(NOT1 nc1, NOT1 nc0, NOT1 nw2, nw1, NOT1 nw0))
(Snp3 iff SAND5(NOT1 nc1, nc0, nw2, nw1, nw0))
(Snp4 iff SAND5(NOT1 nc1, nc0, NOT1 nw2, NOT1 nw1, NOT1 nw0))
(Snp5 iff SAND5(NOT1 nc1, nc0, NOT1 nw2, NOT1 nw1, nw0))
(Snp6 iff SAND5(NOT1 nc1, nc0, NOT1 nw2, nw1, NOT1 nw0))

Next, the behavior of PART1 can be described as a Boolean function as follows.

(Snc0 iff SOR8(AND4(NOT1 x2, x1, NOT1 y2, y1),
AND3(NOT1 x2, NOT1 y2, OR2(AND2(x1, x0), AND2(y1, y0))),
AND3(NOT1 x2, NOT1 y2, OR2(AND2(x1, y0), AND2(x0, y1))),
AND3(NOT1 x1, NOT1 y1, OR2(AND4(x2, x0, NOT1 y2, NOT1 y0),
AND4(NOT1 x2, NOT1 x0, y2, y0))),
AND5(x2, x1, y2, y1, AND2(x0, y0)), AND5(x2, x1, y2, NOT1 y1, y0),
AND5(x2, NOT1 x1, x0, y2, y1), AND6(x2, NOT1 x1, x0, y2, NOT1 y1, y0)))

$\text{Snc1, Snw2, Snw1, Snw0}$ can be described in the same way.

Then, the relation between input status and output status is built.

The following expression is showed tautology by Mizar system. So the correctness of PART1 circuit is verified. (Fig. 5)

(Snm6 iff SAND2(xm3, ym3))
(Snm5 iff SOR2(AND2(xm3, ym2), AND2(xm2, ym3)))
(Snm4 iff SOR3(AND2(xm3, ym1), AND2(xm2, ym2), AND2(xm1, ym3)))
(Snm3 iff SOR4(AND2(xm3, yz), AND2(xm2, ym1), AND2(xm1, ym2),
AND2(xz, ym3)))
(Snm2 iff SOR5(AND2(xm3, yp1), AND2(xm2, yz), AND2(xm1, ym1),
AND2(xz, ym2), AND2(xp1, ym3))
(Snm1 iff SOR6(AND2(xm3, yp2), AND2(xm2, yp1), AND2(xm1, yz),
AND2(xz, ym1), AND2(xp1, ym2), AND2(xp2, ym3)))
(\(\text{Snz iff SOR7(AND2(xm3,yp3),AND2(xm2,yp2),AND2(xm1,yp1), AND2(xz,yz),AND2(xp1,ym1),AND2(xp2,ym2),AND2(xp3,ym3))}\) &
(\(\text{Snp1 iff SOR6(AND2(xm2,yp3),AND2(xm1,yp2),AND2(xz,yp1), AND2(xp1,yz),AND2(xp2,ym1),AND2(xp3,ym2))}\) &
(\(\text{Snp2 iff SOR5(AND2(xm1,yp3),AND2(xz,yp2),AND2(xp1,yp1), AND2(xp2,yz),AND2(xp3,ym1))}\) &
(\(\text{Snp3 iff SOR4(AND2(xz,yp3),AND2(xp1,yp2),AND2(xp2,yp1), AND2(xp3,yp2))}\) &
(\(\text{Snp4 iff SOR3(AND2(xp1,yp3),AND2(xp2,yp2),AND2(xp3,yp1))}\) &
(\(\text{Snp5 iff SOR2(AND2(xp2,yp3),AND2(xp3,yp2))}\) &
(\(\text{Snp6 iff SAND2(xp3,yp3)}\)

Here, for example, the expression \(\text{\(\text{Snm5 iff SOR2(AND2(xm3,ym2), AND2(xm2,ym3))}\)}\) means a state is called \(\text{Snm5(5)}\) if and only if the
input state \(\text{\(\text{\$xm3(x=-3) and \$ym2(y=-2)) or (\$xm2(x=-2) and \$ym3(y=-3))\}\)}\)
Other expressions are similar.

The correctness of PART2 can be verified in same way. (Fig.6)

Thus, the behavior of the whole circuit can be expressed by the
following expressions.

\(\text{\(\text{\$xm2 iff SAND3( x2, x1,NOT1 x0))}\)}\)&
\(\text{\(\text{\$xm1 iff SAND3( x2, x1, x0))}\)}\)&
\(\text{\(\text{\$sxz iff SAND3(NOT1 x2,NOT1 x1,NOT1 x0))}\)}\)&
\(\text{\(\text{\$xp1 iff SAND3(NOT1 x2,NOT1 x1, x0))}\)}\)&
\(\text{\(\text{\$xp2 iff SAND3(NOT1 x2, x1,NOT1 x0))}\)}\)&
\(\text{\(\text{\$cm iff SAND2( c1, c0))}\)}\)&
\(\text{\(\text{\$cz iff SAND2(NOT1 c1,NOT1 c0))}\)}\)&
\(\text{\(\text{\$cp iff SAND2(NOT1 c1, c0))}\)}\)&
\(\text{\(\text{\$nm3 iff SAND3( ns2,NOT1 ns1, ns0))}\)}\)&
\(\text{\(\text{\$nm2 iff SAND3( ns2, ns1,NOT1 ns0))}\)}\)&
\(\text{\(\text{\$nm1 iff SAND3( ns2, ns1, ns0))}\)}\)&
\(\text{\(\text{\$nz iff SAND3(NOT1 ns2,NOT1 ns1,NOT1 ns0))}\)}\)&
\(\text{\(\text{\$np1 iff SAND3(NOT1 ns2,NOT1 ns1, ns0))}\)}\)&
(Sn2 iff AND3(NOT1 ns2, ns1, NOT1 ns0)) &
(Sn3 iff AND3(NOT1 ns2, ns1, ns0)) &
(Sns0 iff SOR4(AND4(NOT1 x2, NOT1 x1, NOT1 x0, c0), AND3(x1, NOT1 x0, c0),
AND5(NOT1 x2, NOT1 x1, x0, NOT1 c1, NOT1 c0),
AND5(x2, x1, x0, NOT1 c1, NOT1 c0))) &
(Sns1 iff SOR5(AND5(NOT1 x2, NOT1 x1, NOT1 x0, c1, c0),
AND5(NOT1 x2, NOT1 x1, x0, NOT1 c1, c0), AND3(x1, NOT1 x0, NOT1 c1),
AND5(x2, x1, x0, NOT1 c1, NOT1 c0), AND5(x2, x1, x0, c1, c0))) &
(Sns2 iff SOR7(AND2(c1, NOT1 c0), AND4(NOT1 x2, NOT1 x1, NOT1 x0, c1),
AND3(NOT1 x2, x1, x0), AND3(x2, x1, NOT1 x0), AND2(x2, NOT1 x1),
AND3(x2, NOT1 c1, NOT1 c0), AND2(x2, c1)))

(Snm3 iff AND2(xm2, cm)) &
(Snm2 iff SOR2(AND2(xm2, cz), AND2(xm1, cm))) &
(Snm1 iff SOR3(AND2(xm2, cp), AND2(xm1, cz), AND2(xz, cm))) &
(Snz iff SOR3(AND2(xm1, cp), AND2(xz, cz), AND2(xp1, cm))) &
(Snp1 iff SOR3(AND2(xz, cp), AND2(xp1, cz), AND2(xp2, cm))) &
(Snp2 iff SOR2(AND2(xp1, cp), AND2(xp2, cz))) &
(Snp3 iff AND2(xp2, cp))

The tautology can be showed because part 1 and part 2 have been verified. So the correctness of radix-4SD adder circuit is verified.
Fig. 5 The circuit verified of correctness by Mizar system (PART1)

Fig. 6 The circuit verified of correctness by Mizar system (PART2)
6. Conclusion

We showed it is possible to verify correctness of logical circuit's mathematical model using proof checker Mizar.

This can be considered as a new approach to verifying correctness of logical circuit.

The circuit we proved has been accept by the library of Mizar, and it can be used to prove larger circuits.

When the library is substantially in future, verification of logical circuits in practice can be expected. Verification of cryptogram circuit can be realized in same way.

References

