Characterization and Modeling of the Voltage Dependency of Capacitance and Impedance Frequency Characteristics of Packed EDLCs

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Abstract—Frequency characteristics and their dependence on charge voltage for a packed electric double layer capacitor (EDLC), which consists of a series of connected EDLC cells, are characterized and modeled based on small ac signal analysis. The results indicate that rated capacitance of a packed EDLC is valid only at frequencies lower than 0.01 Hz at the rated charge voltage but the capacitance is lower for frequencies higher than 0.01 Hz and for lower charge voltages. A conventional simple RC-equivalent circuit, consisting of a capacitor and a resistance in series, is inadequate for expressing EDLC frequency characteristics; therefore, a second-order RC equivalent circuit is used as a model for a packed EDLC. The charge voltage dependency in the frequency characteristics of packed EDLC is evaluated, based on this equivalent circuit. The parameters of the equivalent circuit and their charge voltage dependencies are evaluated from the results. The proposed packed EDLC model is validated by charge and discharge operations in an experimental circuit. The results show that the model can accurately assess the charge stored in a packed EDLC.

Index Terms—Capacitive energy storage, frequency response, modeling, voltage dependency.

I. Introduction

THE electric double-layer capacitor (EDLC, also known as a super capacitor) is being utilized in high-power, high-voltage, and high-energy storage as an alternative to, or a compensator for batteries [1]–[10]. Because the charge and discharge operations in an EDLC are not accompanied by chemical reactions, it affords quick response, high input and output currents, is maintenance free, and has a longer operational life [11]–[13]. Although the capacitance of an EDLC is higher than conventional electrolytic capacitors, the rated voltage of a unit cell must be low (<1.0 V for aqueous electrolytes and <3.0 V for organic electrolytes) to prevent an electrolytic process at the electric double layer. Therefore, capacitor cells must be connected in series and used in a packed configuration to obtain sufficiently high output voltage for practical circuit applications.

There have been several research investigations into the energy-storage applications of EDLCs. Many studies have treated a packed EDLC as a simple ideal capacitor or as a capacitor with a resistor in series [3]–[8], [14]. However, these simplified models cannot provide precise frequency characteristics of EDLCs, which are important for evaluating their dynamic behavior and for designing converter circuits connected with an EDLC. Some studies used a higher-order RC equivalent circuit model of an EDLC cell to obtain its precise frequency characteristics [9], [15]. The voltage dependency of the differential capacitance of an EDLC cell, which is attributed to the diffusion of electric double layer, is evaluated electrochemically based on electrocapillary curves [16] and electrically based on the impedance-frequency characteristics [17], [18]. One study [19] implemented the voltage-dependency characteristics in an EDLC cell model whose model parameters were identified from its transient response. The voltage dependence of the capacitance dominates the total stored charge in an EDLC, and thus, affects energy storage and impedance-frequency characteristics of EDLCs. All of these models [9], [15]–[19] have been based on a single EDLC cell. The equivalent circuit model of an EDLC cell becomes nonlinear, however, when the voltage-dependent characteristic is introduced. That is, the model must be expressed by a differential algebraic equation with variable coefficients. When the model is linear, it is valid to model a packed EDLC by multiplying the number of series-connected cells by the averaged equivalent-circuit single-cell model. However, this is not applicable when the EDLC cell and the model are nonlinear. To model a packed EDLC, it is necessary to splice together discrete EDLC cell models, connecting them in series. The completed packed EDLC model becomes much more complicated as the number of series-connected cells increases, and the model equation reaches an impractically high order. A practical alternative is to collectively characterize and model a packed-EDLC condition. This method is especially suitable for studying EDLC because, the model considers a packed EDLC in one casing to attain balanced voltage distribution among cells with its sophisticated layer stack.

There has been no research on characterizing and modeling of frequency characteristics and voltage dependency of impedance for a packed EDLC. Therefore, this paper characterizes and models the capacitance charge-voltage dependency of a packed EDLC, based on measured impedance frequency characteristics. The proposed packed EDLC model is experimentally validated with a large-signal dynamic response during charge and discharge operations.

The paper is organized as follows: Section II describes the EDLC studied in this paper; Section III presents the developed characterization system; Section IV deals with the characterization and modeling of the EDLC; Section V evaluates the

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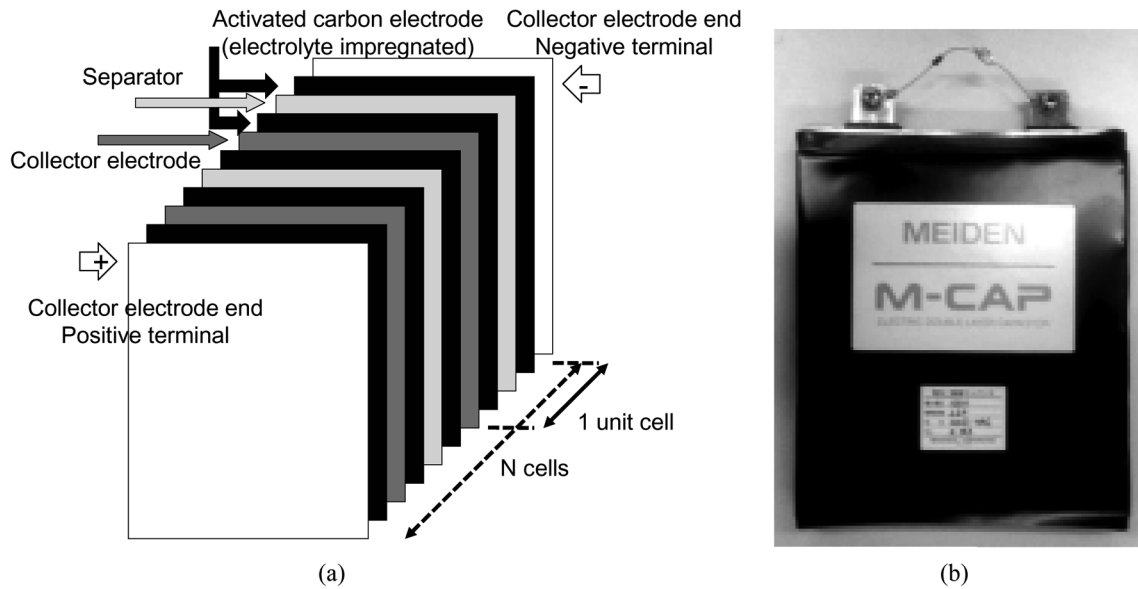
Fig. 1. Studied EDLC (stacked-layer box type). (a) Structure. (b) Appearance.

developed voltage-dependency model based on experimental transient-response results; and Section VI presents the concluding remarks.

II. STRUCTURE OF STUDIED EDLC

Two EDLC structures are typically used for large energy storage. One is the tube (cylindrical) type structure, which consists of film electrodes spirally wound in a tube to increase their area. The other structure has sequentially stacked electrode layers that are packed in a box; this stacked structure results in a larger electrode area. For the stacked electrode layers, there are two methods of providing electrical connection. The most common method is to connect the layers in parallel, such that each layer has electrolytic ions with the same polarity on both sides, forming a unipolar structure. This configuration provides large capacitance, however, it has low rated voltage—the same as that of a single cell. The EDLC described in this paper consists of stacked layers connected in series, as shown in Fig. 1(a). The rated terminal voltage increases in proportion to the number of stacked layers of EDLC unit cells. In this configuration, the capacitance is inversely proportional to the number of stacked cells.

One unit cell of the EDLC consists of two activated-carbon electrodes, a separator, and two collector electrodes. The two activated-carbon electrodes are isolated by the separator to prevent contact with each other. The neighboring collector electrodes, which are connected back to back, are combined as one electrode. The collector electrode adsorbs electrolytic ions with opposite polarity to the front and back side, creating a bipolar structure [20]. The EDLC consists of 44 unit cells. The positive and negative terminals at both ends of the stacked cells provide an interface to the electrical circuit. Consequently, a packed multilayer stack EDLC provides high voltage ratings, just as if discrete EDLC cells were connected in series.

The voltage sharing among the layers is nonuniform, because of small differences in the capacitance and leakage currents

TABLE I
SPECIFICATIONS OF STUDIED EDLC

Type	M-CAP 150S1-44C
Rated voltage	100 V
Maximum current	20 A
Capacitance	2.2 F
Internal resistance	2.1 Ω (25°C)
Number of cells	44
Size	176 (D) × 158 (W) × 29 (H) (mm)
Weight	1.3 kg
Manufacturer	Meidensha Company

among the unit cells. This difficulty exists not only in the series-connected layer-stacked structure of the EDLC, but also in discrete capacitors connected in series. In the studied EDLC, each cell layer in one encapsulated stacked unit is highly uniform; thus, the variation in cell voltage among layers is reduced to approximately ±0.1 V at the rated charge voltage. Therefore, the studied EDLC does not require a special voltage-distribution management system. The EDLC studied here, shown in Fig. 1(b), is manufactured by the Meidensha Company; its specifications are given in Table I.

III. CHARACTERIZATION SYSTEM

The frequency characteristics of impedance are useful for characterizing a capacitor. The capacitance of a single-cell EDLC depends on the charge voltage. Therefore, capacitance of a packed EDLC, consisting of a series-connected multiple-layer stack, definitely depends on the charge voltage. Conventional EDLC characterization apparatus, such as a frequency-response analyzer (FRA) is unsuitable for studying the EDLC, because they are limited to single-cell measurements, and cannot cope with the high dc bias voltage of a packed EDLC. Therefore, this study developed a characterization system for packed EDLC, presented below.
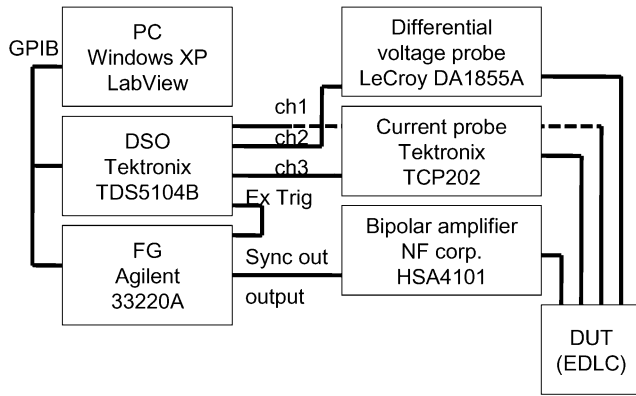
Fig. 2.   Configuration of EDLC characterization system.

Fig. 2 shows the schematic diagram of the characterization system. The system consists of a function generator (FG) and bipolar amplifier for applying a measurement signal, a digital storage oscilloscope (DSO), voltage and current probes for signal detection, and a PC to perform integrated-system control including numerical data processing of the recorded data. For small ac signal analysis, the amplitude of the measurement ac signal must be restricted. The rated voltage of the EDLC is 100 V; therefore, a 1 V peak-to-peak ac voltage serves as the measurement signal. The FG generates a sinusoidal ac voltage waveform at the measurement frequency. The EDLC has quite low impedance, and the FG cannot supply enough current, therefore, the bipolar amplifier is used to boost the signal. The amplifier supplies current corresponding to the applied measurement small ac voltage and maintains the dc charge voltage in the EDLC. Because the measurement ac voltage superimposed on the dc charge voltage is small, the DSO has difficulty detecting it with sufficient accuracy. A decoupling capacitor, generally used to measure a high-frequency signal voltage superimposed on the dc bias voltage, is not applicable for a low frequency and large capacitance measurement. Therefore, this system uses a differential amplifier to subtract the dc bias voltage from the measured voltage signal making it possible for the DSO to measure only the superimposed ac voltage component. The sync output of the FG triggers the DSO through its external trigger terminal to start the measurement. This is done to synchronize the trigger timings of the respective measurements and to measure the ac voltage with lock-in detection. The measurement record length is chosen such that the number of sinusoidal ac waveforms is an integer, to simplify numerical processing and reduce errors. A voltage probe connected to ch1 measures the voltage between the terminals of the device under test (DUT), and the charge voltage is obtained by averaging this voltage. A differential voltage probe connected to ch2 of the DSO subtracts the charge dc voltage from the detected terminal voltage, and extracts only the measurement ac signal component, superimposed on the dc voltage. A current probe connected to ch3 detects the measurement signal current; using a dc-current probe solves the problem of low frequency.

A PC controls the equipment, sweeping the measurement frequency from 1 mHz to 1 MHz, and collects and processes the data. The measurement sequence is implemented with the program LabVIEW, as shown in the flowchart in Fig. 3. The
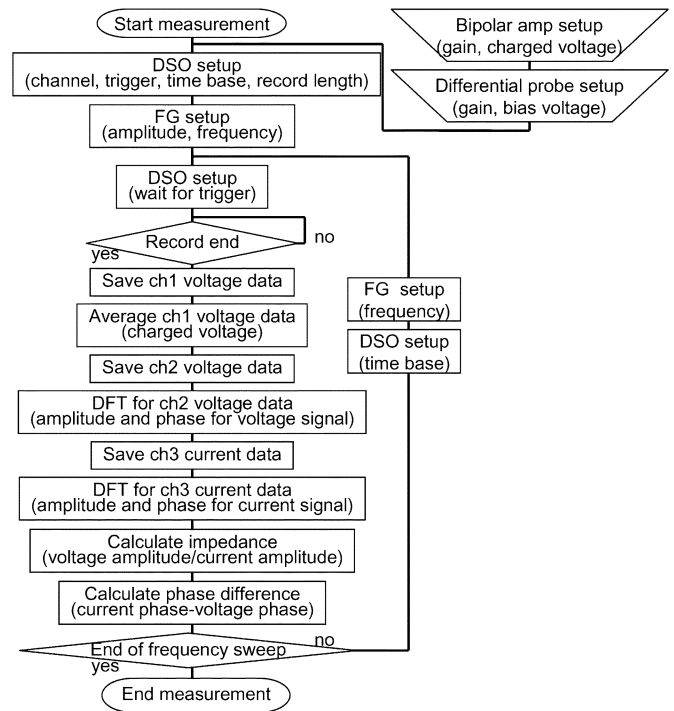

Fig. 3.   Flow chart of characterization sequence.

amplitude and phase of the measured ac signal are calculated by performing discrete Fourier transform (DFT) for the measured ac signal voltage and current, respectively. The complex impedance of the DUT is then evaluated from the amplitude ratio and the phase difference between voltage and current. Then, the resistance and reactance of DUT are extracted. The differential capacitance of the DUT is derived from the obtained reactance and the angular frequency of the measurement signal. The obtained values are stored as the frequency characteristics of the EDLC at the respective charge-voltage conditions.

IV. CHARACTERIZATION AND MODELING OF PACKED EDLC

A. Measured Frequency Characteristics of Packed EDLC

The frequency characteristics of a packed EDLC are measured as the charge-voltage parameter is swept from 5 to 100 V. Fig. 4 shows the measured frequency characteristics of the capacitance and resistance in the EDLC for three different charge voltages (5, 50, and 100 V), at room temperature. The figure indicates that the characteristics substantially change in the frequency range from 0.01 to 10 Hz. Fig. 4(a) shows the frequency characteristics of capacitance. The EDLC capacitances are rated only for frequencies lower than 0.01 Hz with a charge voltage of 100 V; i.e., from the viewpoint of differential capacitance, the rated capacitance (2.2 F) is not obtained for frequencies higher than 0.01 Hz or a charge voltage lower than 100 V. The result also shows that the capacitance of the EDLC is highly dependent on and proportional to the charge voltage. The capacitance at low frequencies (<0.01 Hz) becomes less than 60% of the rated value at the uncharged condition. Therefore, it is easily understood that the stored energy in an EDLC cannot be expressed simply as $\frac{1}{2}CV^2$, which assumes constant capacitance. It also shows that the capacitance becomes nearly zero at frequencies
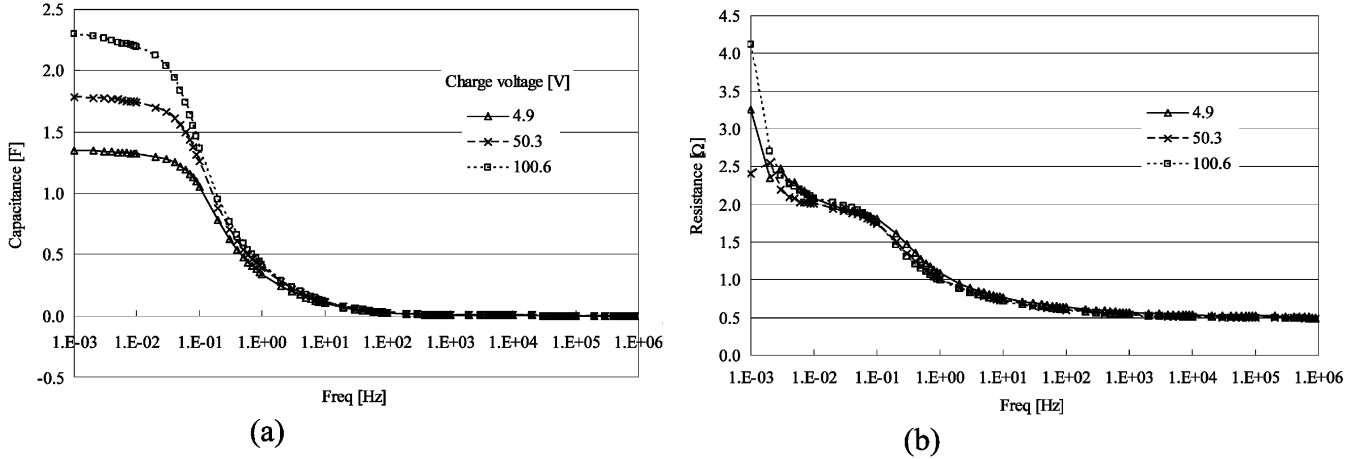
Fig. 4. Measured frequency characteristics of EDLC with regard to the charged voltage parameters. (a) Capacitance. (b) Resistance.

higher than 100 Hz, which results from the limitation of ionic motion in separating charges at the interface between the electrode surface of the activated carbon and the electrolytic solution. However, no significant resonance phenomenon is found, because the studied EDLC structure has less inductance at the electrodes compared to the cylindrical-type capacitor, whose electrodes are spirally wound in the tube.

Fig. 4(b) shows the frequency characteristics of resistance in the EDLC. The resistance also changes with frequency—the resistance decreases as the frequency increases, which is similar to the capacitance behavior. However, the figure shows that the resistance dependence on the charge voltage is insignificant. The dispersion of resistance values among charge-voltage conditions becomes large at extremely low frequencies, because, the EDLC's impedance becomes quite large at these frequencies because of the $(1/j\omega C)$ term, and the relative value of resistance becomes quite small, and the processing error becomes noticeable.

B. Modeling of Packed EDLC Characteristics

The charge-voltage dependency of the capacitance and its frequency characteristics affect the dynamic behavior of the EDLC's charge and discharge operations. This subsection discusses modeling the packed EDLC's frequency characteristics first, and then expands the model to express the voltage dependency.

The dynamics in an electrical circuit are generally expressed by differential algebraic equations based on an equivalent circuit. The equivalent circuit is also used for representing the frequency characteristics. The simplest first-order RC equivalent circuit for an EDLC consists of a capacitor and a series-connected resistance and exhibits constant capacitance and resistance with varying frequency. Therefore, a first-order RC equivalent circuit is insufficient for expressing the frequency characteristics shown in Fig. 4, and higher-order RC equivalent circuit is needed, and is shown in Fig. 5. This circuit, which is adopted as the EDLC model for this paper, is equivalent to the two-cell ladder model [9], [15], or the Debye polarization model [17]. The voltage-dependent characteristics of the EDLC are then discussed, based on model parameters for the respective charge voltages identified by this circuit.
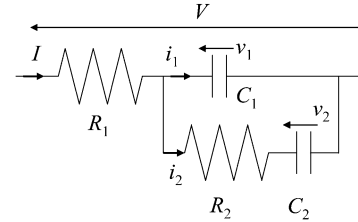

Fig. 5. Equivalent circuit model of EDLC.

The impedance of the equivalent circuit shown in Fig. 5 is given by

$$R + jX = R_1 + \frac{C_2^2 R_2}{(\omega C_1 C_2 R_2)^2 + (C_1 + C_2)^2} - j\frac{\omega^2 C_1 C_2^2 R_2^2 + C_1 + C_2}{\omega\{(\omega C_1 C_2 R_2)^2 + (C_1 C_2)^2\}}. \quad (1)$$

Here, ω is the angular frequency of the ac signal.

A conventional method for evaluating the parameters of the model is the linear least mean square (LMS) method [21], which expresses the equivalent circuit in transfer-function form, and evaluates the coefficients of the transfer function. However, the objective function for minimizing the error in the model has a weighting factor for frequency that emphasizes high-frequency components. Thus, the parameters evaluated using the linear LMS method produce a small error in the high-frequency region, but a large error in the low-frequency region, indicated by the dashed line in Fig. 6. The capacitance in the low-frequency region is mainly responsible for the energy storage in an EDLC. Thus, parameter evaluation using the linear LMS method is inadequate. Therefore, a nonlinear LMS method is adopted to evaluate the parameters of the equivalent circuit.

An objective function for evaluating the parameters of the equivalent circuit model, while minimizing error, is configured with the resistance and capacitance, as given in

$$F = \Sigma_{i=1}^N \left(f_{\mathrm{R}i}^2 + f_{\mathrm{C}i}^2 \right). \quad (2)$$

Here, N is the number of samples, $f_{\mathrm{R}i} = R_1 + \frac{C_2 R_2}{(\omega C_1 C_2 R_2)^2 + (C_1 + C_2)^2} - R_i$ and $f_{Ci} = \frac{(\omega_i C_1 C_2 + C_2)^2 + (C_1 + C_2)^2}{\omega_i^2 C_1 C_2^2 R_2^2 + C_1 + C_2} - C_i$ is the error-evaluation index; R_i and C_i are the measured
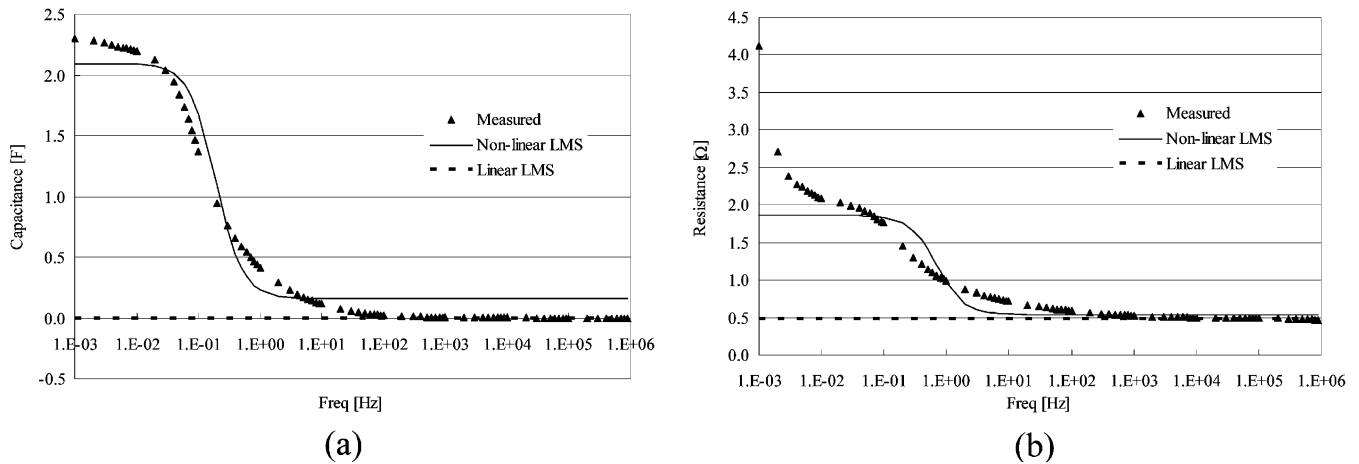
Fig. 6.   Modeled frequency characteristics of EDLC for rated charged voltage (100 V) condition. (a) Capacitance. (b) Resistance.
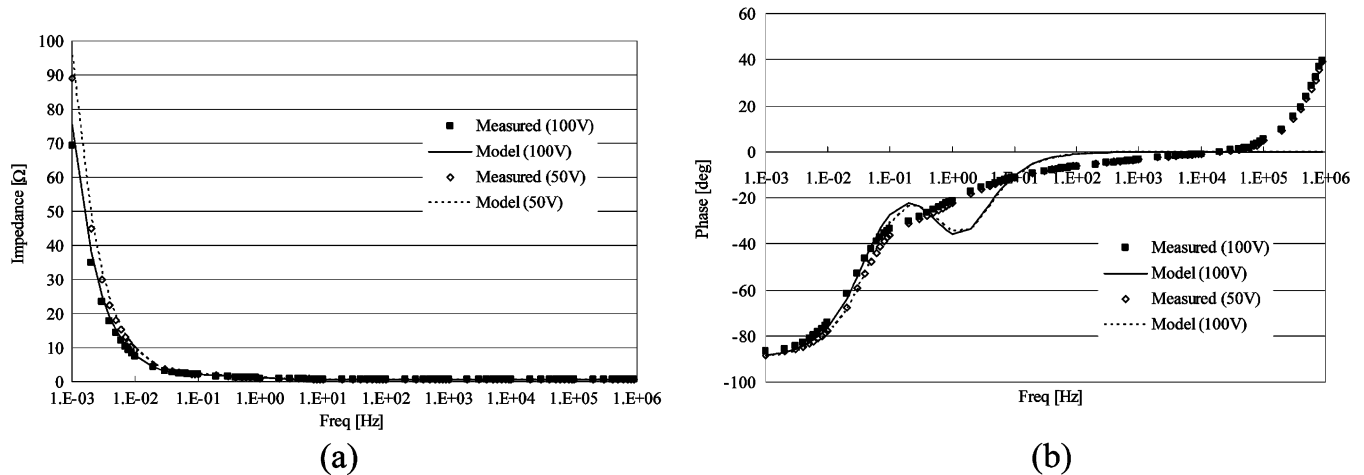

Fig. 7.   Bode plot of impedance to the measured and modeled results for EDLC. (a) Impedance. (b) Phase.

resistance andcapacitance, respectively. The capacitance component of the equivalent circuit is derived from the reactance in (1)

$$C = \frac{(\omega C_1 C_2 R_2)^2 + (C_1 + C_2)^2}{\omega^2 C_1 C_2^2 R_2^2 + C_1 + C_2}. \qquad (3)$$

The influence of the frequency-weighting factor on the objective function is eliminated by adopting the error-evaluation index shown above. The LMS condition for the objective function (2) becomes a nonlinear equation. Therefore, the steepest descendent method is utilized for obtaining the LMS condition by convergence calculation.

An example of identified results for a charge voltage of 100 V is shown as a solid line in Fig. 6. The modeled-frequency characteristics of capacitance are now accurately matched in the low frequency region, except that the model underestimates the capacitance at extremely low frequencies. The transition of capacitance and resistance from around 0.01 to 10 Hz is also accurately modeled by this method. The modeled resistance at extremely low frequencies produces a large error, but there is some uncertainty in the measured result, as shown in Fig. 4(b) and discussed in the last subsection. Therefore, this error is not crit-

ical for the EDLC model. Fig. 7 shows the Bode plot of measured and modeled impedance for the charge voltages of 50 and 100 V. The modeled impedance characteristics shown in Fig. 7(a) are consistent with the measured results. The relative error in impedance, which is calculated from the capacitance and resistance, becomes small because of frequency weighting in reactance. The phase error becomes small at a frequency less than 0.1 Hz, where the EDLC is distinctly capacitive. The phase error fluctuation around 0.1–10 Hz is due to a crossover of the modeled and measured results in capacitance and resistance in Fig. 6. However, the error is not critical, because the impedance of the EDLC in this frequency region is sufficiently small, as shown in Fig. 7(a). Consequently, the second-order RC equivalent circuit can model a vital portion of the packed EDLC frequency characteristics.

Fig. 8 indicates the identified parameters of the equivalent circuit as a function of the charge voltage. Both capacitance components in the equivalent circuit, C_1 and C_2, clearly demonstrate charge-voltage dependency, as shown in Fig. 8(a) and (b). They also show that the voltage dependency of C_2 is more critical than C_1, and that both can be approximated by a linear function of the charge voltage. The value of C_2 at the rated charge voltage becomes approximately half when uncharged;
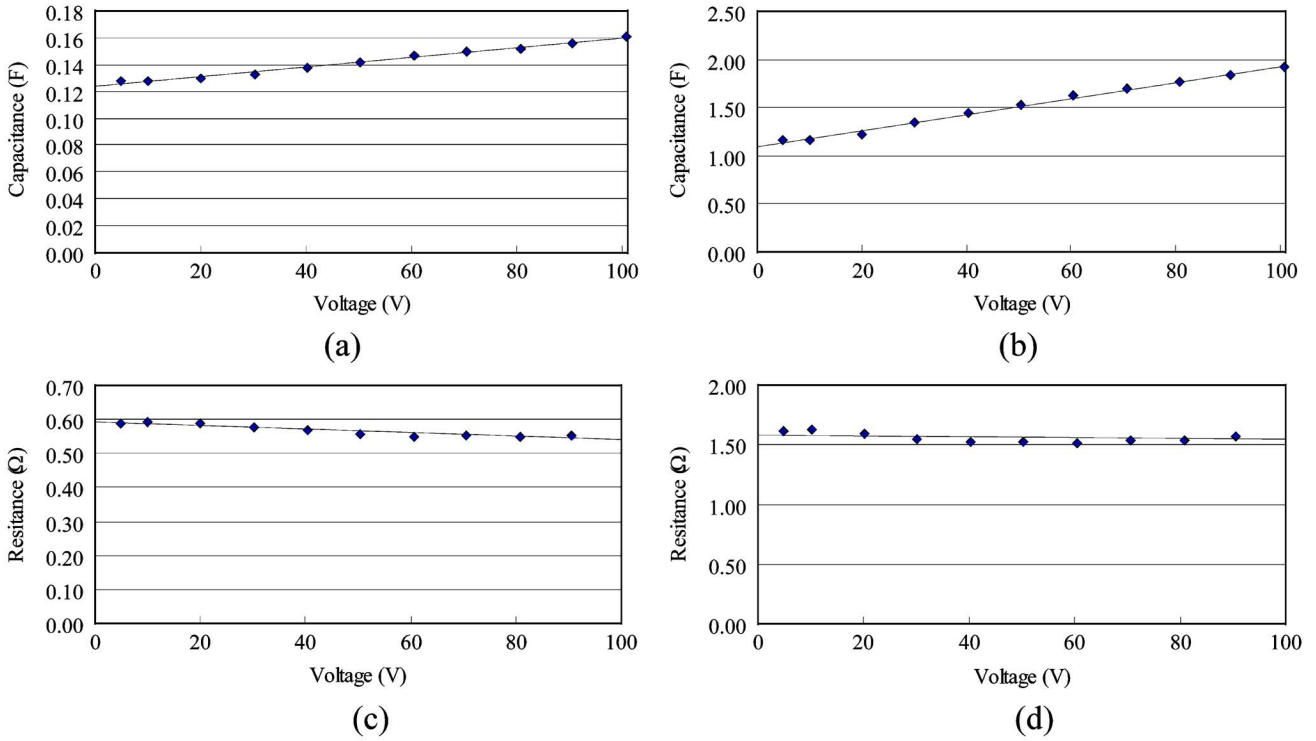
Fig. 8.   Voltage dependency of the parameters in the EDLC equivalent circuit model. (a) C_1. (b) C_2. (c) R_1. (d) R_2.

this is more significant than the measured terminal capacitance. On the other hand, resistances R_1 and R_2, shown in Fig. 8(c) and (d) have weak charge-voltage dependencies, compared to the capacitances. The charge-voltage dependency of the equivalent-circuit parameters are modeled with the first-order linear algebraic formula. The formulas are given in (4), with the coefficients evaluated with the linear LMS method

$$\begin{cases} C_1 = 3.55 \times 10^{-4}V + 0.125 \quad [\text{F}] \\ C_2 = 8.35 \times 10^{-3}V + 1.10 \quad [\text{F}] \\ R_1 = -5.16 \times 10^{-4}V + 0.592 \quad [\Omega] \\ R_2 = -3.79 \times 10^{-4}V + 1.59 \quad [\Omega] \end{cases}. \tag{4}$$

V.   VALIDATION OF PACKED EDLC MODEL IN DYNAMIC RESPONSE

The packed-EDLC model developed in the previous section is based on small signal measurement. This section validates the developed EDLC model by comparing the experimental and simulated results of large-signal transient response in the charge and discharge operations of the EDLC.

The procedure for implementing the voltage dependency of the parameters is provided before discussing the EDLC transient response. The voltage dependency of the parameters in the equivalent circuit given by (4) is based on the charge voltage appearing at the terminal along with a small measurement signal. However, there is a voltage drop across the internal resistance when a charge/discharge current flows. Therefore, the charge voltage at the internal capacitance is different from the EDLC terminal voltage. Hence, the parameters of the EDLC model, i.e., internal capacitances C_1 and C_2, are estimated from charge

voltages, v_1 and v_2. Then the differential and algebraic equations for the equivalent circuit in Fig. 5 are given by (5). The following circuit-simulation results are obtained by solving

$$\begin{cases} i_1 = C_1(v_1)\frac{dv_1}{dt} \\ i_2 = C_1(v_2)\frac{dv_2}{dt} \\ V = R_1 I + v_1 \\ v_1 = R_2 i_2 + v_2 \end{cases}. \tag{5}$$

The results obtained from proposed model are compared with the results from the experiment and the results from the simple first-order RC model, which consist of the fixed capacitance and series resistance values given in Table I.

The result for EDLC charge operation is shown in Fig. 9. Charge operation begins with constant current (1 A), and the constant-voltage operation (50 V) supersedes when the EDLC terminal voltage reaches 50 V. The terminal voltage begins to rise at the instant charge current builds up, at $t = 0$ (s). The measured terminal voltage builds up smoothly with a time constant of several seconds, as shown in Fig. 9(c), and the proposed model suitably simulates this response. The simple RC model, however, shows a non-smooth change. The experimental voltage waveform given in Fig. 9(a) shows the change in the gradient of the slope resulting from the voltage dependency of the capacitance. The proposed model also accurately simulates this behavior, but the simple RC model provides voltage increments with constant time rates, because of its fixed parameter values. The area given by the time integration of current in Fig. 9(b) indicates the charge stored in the EDLC. If the voltage dependency of the capacitance is considered, the error of estimated stored charge in the proposed model is less than that of the simple RC model.
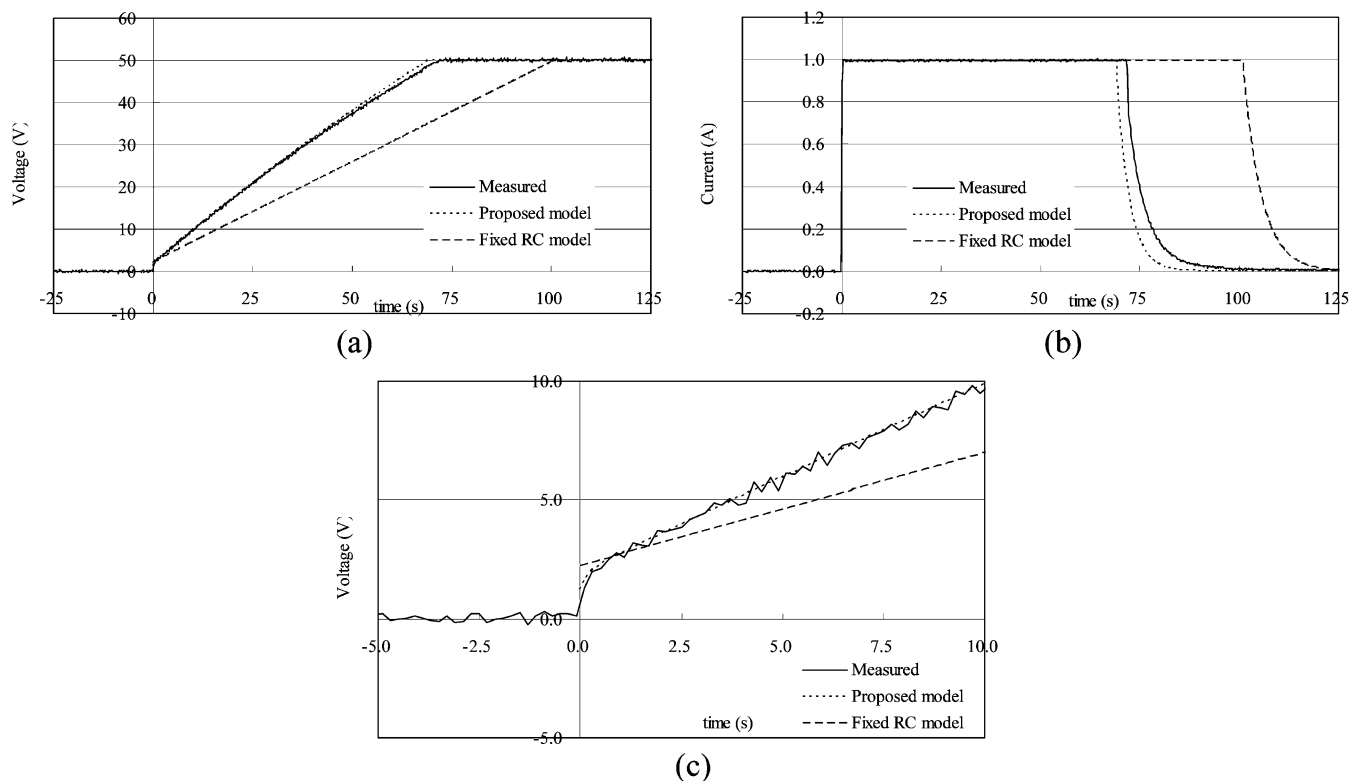
Fig. 9.   Transient response of EDLC for charge operation. (a) Voltage respones. (b) Current response. (c) Voltage response at the beginning of charge operation.
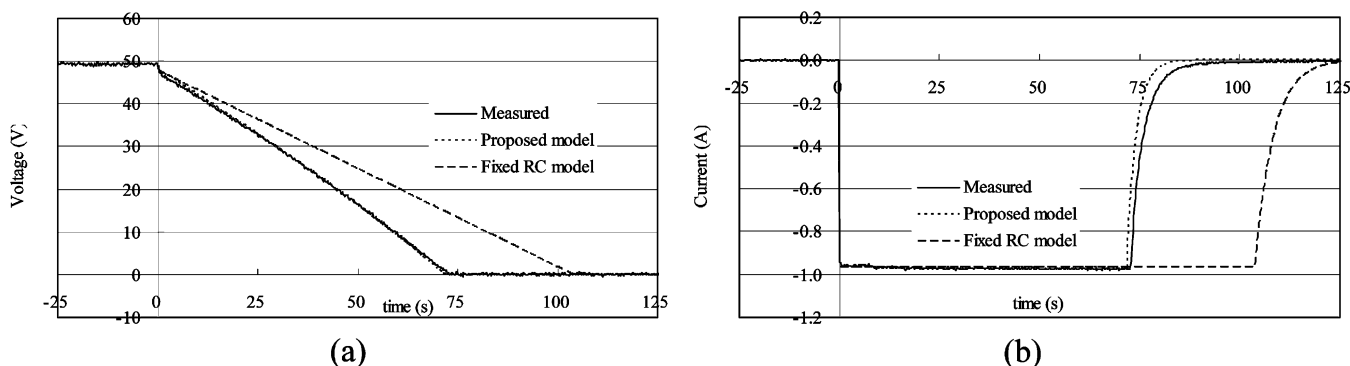

Fig. 10.   Transient response of EDLC for discharge operation. (a) Voltage response. (b) Current response.

Fig. 10 shows the results for EDLC discharge operation. The terminal voltage response given in Fig. 10(a) shows that the proposed model accurately simulates the terminal voltage response, taking the EDLC voltage-dependency characteristics into account. The current response given in Fig. 10(b) also adequately evaluates the ejected charge from the EDLC. However, the simple RC model with fixed parameters cannot simulate this characteristic.

The capacitance in the proposed model, evaluated by the non-linear LMS method, underestimates the capacitance of the EDLC in the low-frequency region, as shown in Fig. 6(a). Therefore, the proposed model charges and discharges a little quicker than the experimental results, as shown in Fig. 9(a) and 10(a). However, the proposed model accurately evaluates the stored charge in packed EDLC by taking the voltage-dependency characteristics into account. Thus, this model is valuable in evaluating the packed EDLC's energy-storage performance.

VI. CONCLUSION

The voltage dependency of the capacitance and the frequency characteristics of impedance for a packed EDLC were characterized and modeled in this study. The packed EDLC studied has large capacitance and high voltage ratings, making conventional characterization systems unsuitable. Therefore, a characterization system for measuring impedance voltage dependency with high dc bias was developed. The results indicate that the capacitance of the packed EDLC displays a clear dependency on charge voltage, and the rated capacitance can be obtained only for the rated charge-voltage condition. The frequency characteristics also show that the rated capacitance is valid at frequencies lower than 0.01 Hz, and the resistance and capacitance of packed EDLC substantially change at frequencies between 0.01 to 10 Hz. These frequency characteristics cannot be modeled using a conventional simple RC equivalent circuit; however, a second-order RC equivalent

circuit can model the packed EDLC, and the parameters were evaluated with a nonlinear LMS method. The evaluated model suitably approximates the frequency characteristics of packed EDLC at the respective charge voltages. The charge-voltage dependency characteristic of the packed EDLC was modeled with the identified parameters of the equivalent circuit for the respective charge voltages. The capacitance in the equivalent circuit shows a clear dependence on the charge voltage; these dependencies were modeled as a linear function of charge voltage. The resistances showed a weak charge-voltage dependency than the capacitance. The proposed voltage-dependent packed EDLC model was evaluated based on small ac signal analysis, then validated with large-signal transient response. The proposed model can consider the variation in the capacitance during charge and discharge operations—something not possible with a conventional RC equivalent circuit with fixed-parameter values. Accordingly, the proposed model can accurately evaluate the stored charge and energy in a packed EDLC. An EDLC is used in a series-connected packed configuration for practical power-electronics applications; therefore, the proposed characterization and modeling method is suitable for modeling practical applications of the EDLC.

REFERENCES

[1] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy, and Y. Liu, "Energy storage systems for advanced power applications," *Proc. IEEE*, vol. 89, no. 12, pp. 1744–1756, Dec. 2001.

[2] M. Marchesoni and C. Vacca, "New dc-dc converter for energy storage system interfacing in fuel cell hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 301–308, Jan. 2007.

[3] M. E. Ortúzar, R. E. Carmi, J. W. Dixon, and L. Morán, "Voltage-source active power filter based on multilevel converter and ultracapacitor DC link," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 477–485, Apr. 2006.

[4] M. Amrhein and P. T. Krein, "Dynamic simulation for analysis of hybrid electric vehicle system and subsystem interactions, including power electronics," *IEEE Trans. Veh. Technol.*, vol. 54, no. 3, pp. 825–836, May 2005.

[5] S. M. Kim and S. K. Sul, "Control of rubber tyred gantry crane with energy storage based on supercapacitor bank," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1420–1427, Sep. 2006.

[6] J. P. Zheng, T. R. Jow, and M. S. Ding, "Hybrid power sources for pulsed current applications," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 37, no. 1, pp. 288–292, Jan. 2001.

[7] R. A. Dougal, S. Liu, and S. R. E. White, "Power and life extension of battery-ultracapacitor hybrids," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 1, pp. 120–131, Mar. 2002.

[8] M. Uzunoglu and M. S. Alam, "Dynamic modeling, design, and simulation of a combined PEM fuel cell and ultracapacitor system for stand-alone residential applications," *IEEE Trans. Energy Conversion*, vol. 21, no. 3, pp. 767–775, Oct. 2006.

[9] R. A. Dougal, L. Gao, and S. Liu, "Ultracapacitor model with automatic order selection and capacity scaling for dynamic system simulation," *J. Power Sources*, vol. 126, no. 1–2, pp. 250–257, Feb. 2004.

[10] C. Xinping, C. Wen-Jen, K. Ya-Chin King, and L. Yi-Kuen, "Electromagnetic energy harvesting circuit with feedforward and feedback DC–DC PWM boost converter for vibration power generator system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 679–685, Mar. 2007.

[11] A. Yoshida, I. Tanahashi, Y. Takeuchi, and A. Nishino, "An electric double-layer capacitor with activated carbon fiber electrodes," *IEEE Trans. Compon., Hybrids, Manufact. Technol.*, vol. CHMT-10, no. 1, pp. 100–102, Mar. 1987.

[12] A. Yoshida, I. Tanahashi, and A. Nishino, "Aluminum collector electrodes formed by the plasma spraying method for electric double-layer capacitors," *IEEE Trans. Compon., Hybrids, Manufact. Technol.*, vol. CHMT-11, no. 3, pp. 318–323, Sep. 1988.

[13] A. Yoshida, K. Imoto, H. Yoneda, and A. Nishimo, "An electric double-layer capacitor with high capacitance and low resistance," *IEEE Trans. Compon., Hybrids, Manufact. Technol.*, vol. 15, no. 1, pp. 133–138, Feb. 1992.

[14] D. Linzen, S. Buller, E. Karden, and R. W. DeDoncker, "Analysis and evaluation of charge-balancing circuits on performance, reliability, and lifetime of supercapacitor systems," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1135–1141, Sep./Oct. 2005.

[15] L. Gao, R. A. Dougal, and S. Liu, "Power enhancement of an actively controlled battery/ultracapacitor hybrid," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 236–243, Jan. 2005.

[16] O. Ikeda, H. Tamura, and Y. Matsuda, "Specific adsorption effects of organic cation on the electroreduction of dimethylfumarate," *J. Electroanal. Chem.*, vol. 111, no. 2–3, pp. 345–358, Aug. 1980.

[17] R. M. Nelms, D. R. Cahela, and B. J. Tatarchuk, "Using a Debye polarization cell to predict double-layer capacitor performance," *IEEE Trans. Ind. Appl.*, vol. 37, no. 1, pp. 4–9, Jan./Feb. 2001.

[18] R. M. Nelms, D. R. Cahela, and B. J. Tatarchuk, "Modeling double-layer capacitor behavior using ladder circuits," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 39, no. 2, pp. 430–438, Apr. 2003.

[19] L. Zubieta and R. Bonert, "Characterization of double-layer capacitors for power electronics applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 199–205, Jan./Feb. 2000.

[20] H. Zaitsu, H. Nara, H. Watanabe, M. Oobe, S. Sugimoto, R. Hatano, and N. Yamamoto, "Uninterruptible power supply system utilizing electric double-layer capacitors," in *Proc. Power Conversion Conf.*, 2007, pp. 230–235.

[21] E. C. Levi, "Complex-curve fitting," *IRE Trans. AC*, vol. 4, pp. 37–44, May 1959.

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